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MSI601
Hardware Reference Manual

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Abstract: This paper is a hardware reference manual for the Micronet Serial Interface (MSI), which is a 1 Mbps LAN interface designed for the ETC601/611 LAN Controller.

(30 printed pages)

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1. INTRODUCTION 1.

This manual describes the MSI601 board which is a RC Micronet Serial Interface designed to work with the Intel 82586 LCC in 1Mbps LAN applications. The MSI601 PCB is designed to be mounted as a satellite print on the RC Ethernet Controller.

The primary function of the MSI601 is to perform Manchester encoding/decoding, provide 1Mhz transmit and receive clocks to the 82586 LCC, and to drive the transceiver cable.

This manual is divided into basically three parts:

- Chapter 2 General Information
- Chapter 3 Programming Information
- Chapter 4 Technical Description

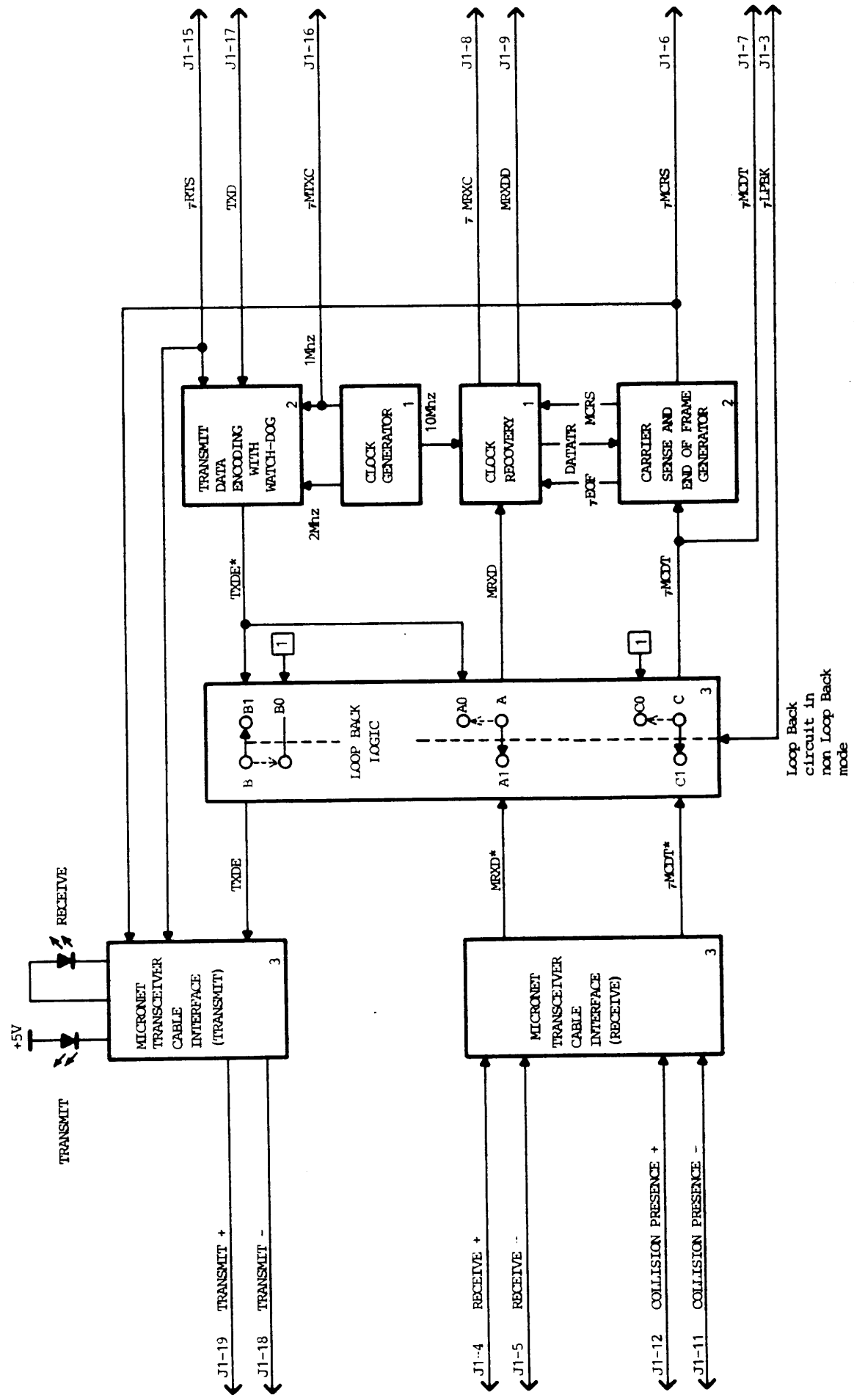
General Information contains a general description of the MSI and provides the user with information concerning specifications and installation. Programming Information is a small chapter which provides the user with information necessary to program the ETC board when using MSI601. Technical Description is a detailed hardware description of the MSI601.

2. GENERAL INFORMATION 2.

2.1 Short Description 2.1

The RC Micronet Serial Interface (MSI) board is designed to work directly with the Intel 82586 LAN Co-processor in 1Mbps local area network applications. The major functions of the MSI are to generate the 1Mhz transmit clock for the 82586, perform Manchester encoding/decoding of transmitted/received frames and provide the electrical interface to the RC Micronet transceiver cable. Diagnostic loopback control enables the MSI to route the Transmit Data signal from the 82586 through its Manchester encoding and decoding circuitry and back to the Receive Data input of the 82586. The combined loopback capabilities of the 82586 and the MSI allow efficient fault detection and isolation by providing sequential testing of the communications interface. An on-board watchdog timer prevents the MSI from locking up in a continuous transmit mode. Figure 1 shows a block diagram of the MSI601.

MSI601 can be mounted as a satellite print on the RC Ethernet Controller (ETC601/ETC611). When mounted on the ETC the MSI601 substitutes the Intel 82501 ESI i.e. a 20-pins dip adapter on the MSI fits directly into the 20-pins socket for the 82501 ESI on the ETC board. Terminating resistors for transceiver cable are located on the ETC board. The MSI601 transceiver cable interface is designed to connect to the RC DCE751 transceiver.



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MSI601

MSI601 FUNCTIONAL BLOCK DIAGRAM

A14751

2.2 Specifications 2.2

2.2.1 Performance Specifications 2.2.1

- 1-Mbps data rate.
- Manchester Encoding/Decoding and Receive Clock Recovery.
- 1-Mhz crystal controlled Transmit Clock Generator.
- Driving/Receiving RC DCE751 transceiver cable.
- Interface compatible with the Intel 82586 LAN Co-processor.
- Watchdog timer circuit to prevent continuous transmissions. 210 ms +/- 20%.
- Diagnostic loopback for fault detection and isolation.

2.2.2 Base Board Interface Circuits 2.2.2

Intel 82586 LCC compatibel

Input from 82586:

TXD Transmit Data is a TTL-level input signal that is directly connected to the serial data output of the 82586.

RTS/ Request To Send is a TTL-level input synchronous to MTXC/ that enables data transmission. RTS/ is driven by RTS/ from 82586.

LPBK/ Loopback is a TTL-level control signal, which enables the loopback mode. In this mode, serial data on TXD is routed through the MSI internal circuits and back to the MRXDD output without driving the transceiver cable.

Output to 82586:

MRXDD Micronet Receive Data is a MOS-level output that can be tied directly to the RXD input of the 82586 and sampled by the 82586 at the negative edge of MRXC/.

MRXC/ Micronet Receive Clock is a MOS-level output that can be tied directly to the 82586 receive clock input RXC/. During idle periods (no incoming frames) there is no Micronet Recieve Clock (MRXC/ is low).

MTXC/ Micronet Transmit Clock is a MOS-level output that can be tied directly to the 82586 transmit clock input TXC/. The frequency of MTXC/ is 1Mhz, and the duty cycle is 50%.

MCRS/ Micronet Carrier Sense is a TTL-level active low output to notify the 82586 that there is activity on the coax-cable. This signal is active when valid data or a collision signal from the micronet transceiver is present. MCRS/ becomes inactive 2 micro sec. +/- 15% after the center of the last bit cell, or when the end of collision presence signal is detected.

MCDT/ Micronet Collision Detect is a TTL-level, active low output which can be connected to the CDT/ input of the 82586. The signal is active low as long as collision persists.

2.2.3 Transceiver Cable Interface Circuits

2.2.3

Compatible with the RC DCE751 transceiver.

Input from DCE751:

Collision Pair is a differential driven input pair tied to the collision presence pair of the DCE751 Micronet transceiver cable. Terminating network is not located on the MSI PCB. Collision presence (+) is positive relative to collision presence (-) when collision is detected.

Receive pair is a differential driven input pair tied to the receive pair of the DCE751 Micronet Transceiver cable. Terminating network is not located on the MSI PCB. The received bit stream is assumed to be Manchester encoded. The first transition on Receive(+) is negative-going and indicates the beginning of the fram. The last transition on Receive (+) is positive-going indicating the end of the frame. Receive(-) has the inverse polarity of Receive(+).

Output to DCE751:

Transmit pair is an output driver pair which generate the differential signal for the transmit pair of the DCE751 Micronet transceiver cable. The output bit stream is Manchester encoded. The first transition on Transmit(+) is negative-going and indicates the beginning of the frame. The last transition on Transmit(+) is positive-going indicating the end of the frame. Transmit(-) has the inverse polarity of Transmit(+). Pull down resistors are not located on the MSI PCB.

2.2.4 Electrical Specifications

Micronet Receiver:

- AM26LS32AC Quad Differential Line Receiver.
- Input voltage range 7 Volt (differential or common mode).
- +/- 0.2V sensitivity.
- Terminating resistors located on baseboard (Equivalent to Intel 82501 ESI termination).

Micronet Driver:

- AM26LS31C Quad Differential Line Driver.
- Output short-circuit protection.
- Differential output voltage across 50 ohm is not less than 1 Volt (either logic state).
- Complementary outputs.
- Pull down resistors located on baseboard (Equivalent to Intel 82501 ESI pull down).

Supply voltage:

+5 Volt +/- 5% 300mA max.

2.2.5 Physical Specifications 2.2.5

Connector to baseboard:

- 20 pins eurodip adapter, pin layout compatible with Intel 82501 ESI. (refer to section 4, diagram 2 for jack list).

Printed circuit board:

- Multilayer
- Width 85 m.m
- Length 151 m.m
- Thickness refer to fig. 2
- An ETC601/ETC611 mounted with MSI601 occupies two slots of a multibus crate.
- The MSI board is attached to the ETC board using 8 screws and 4 spacers.

2.2.6 Environmental Specifications 2.2.6

- Temperatur 0-40 degree C
- Relative humidity 20-80% (non condensing)

2.3 Installation 2.3

This section explains how to mount the MSI601 on the ETC baseboard.

1. Remove Intel 82501 ESI integrated circuit from IC position 69 on ETC baseboard (see fig. 2)

2. Mount 4 spacers on ETC baseboard as indicated on fig. 2.

3. Check that mini-jumper of strap S24 connects pin 1 of S24 to pin 2 as indicated in fig. 2. If not move mini-jumper to S24 pins 1-2.

4. Insert the MSI601 board in ETC socket position 69. Observe that the 20 pins eurodip adapter of the MSI matches the corresponding socket on the ETC baseboard (see fig. 3).

5. Fasten the MSI board to the spacers using 4 screws (M3x6).

6. Verify correct installation by running Ethernet test 2 (ref. 2).

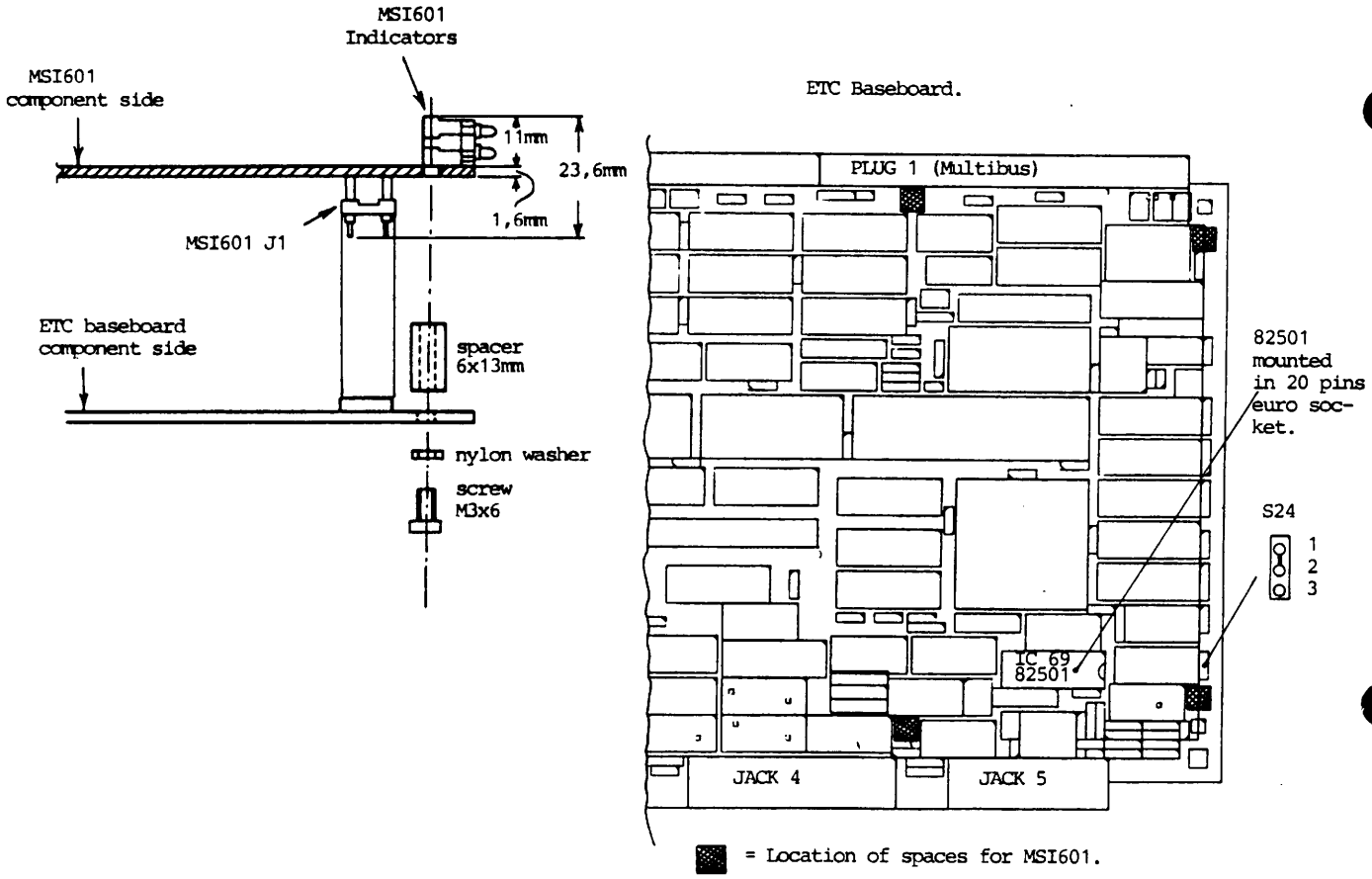


Fig. 2. Location and Installation of spacers.

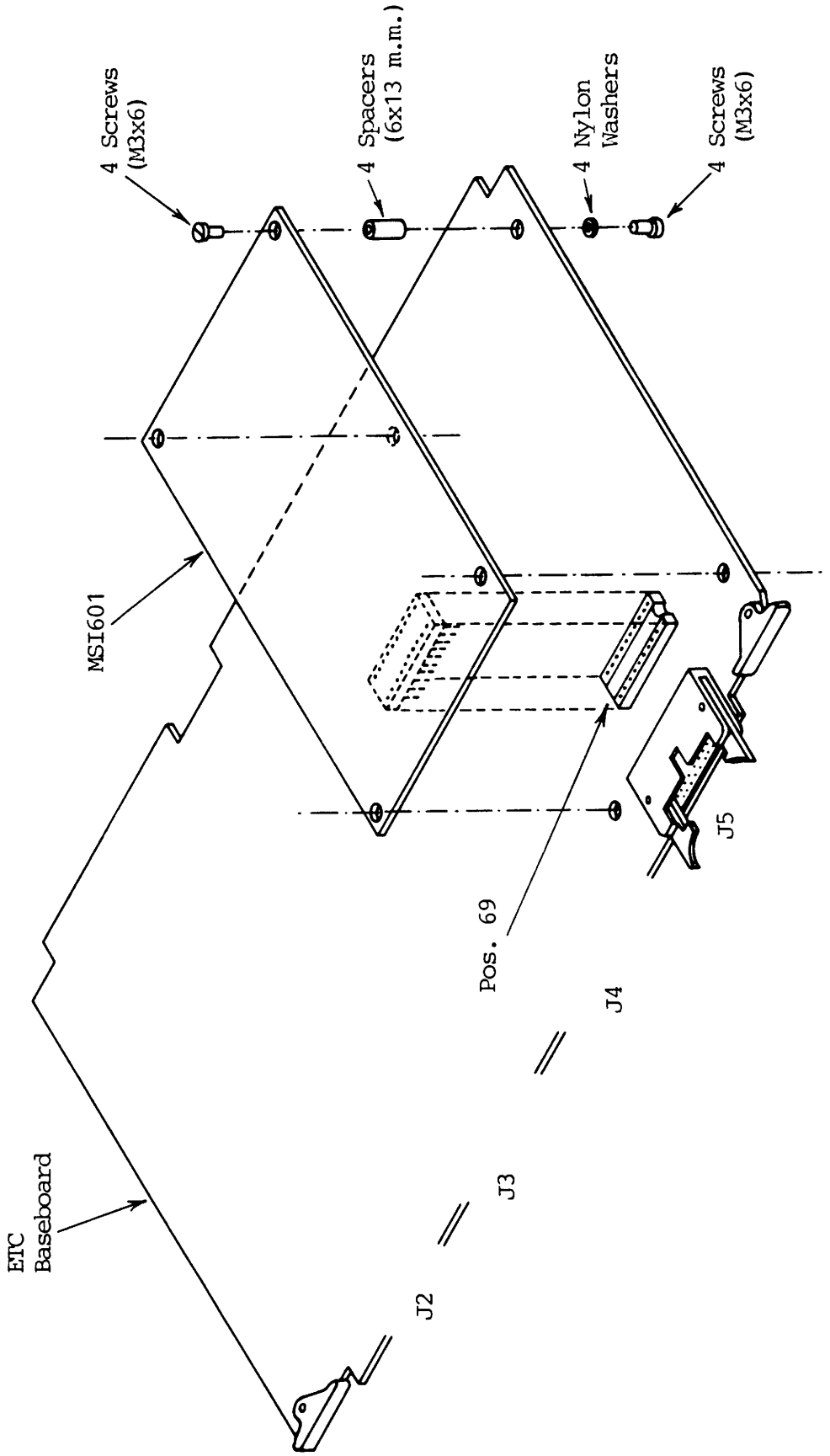


Fig. 3 Inserting MSI601 Board

3. PROGRAMMING INFORMATION 3.

This chapter only describe how to activate/deactivate the LOOP BACK (LPBK/) signal from the ETC baseboard.

The LPBK/ is controlled via the 8255 PPI on the ETC baseboard (ref. 1). Port C bit PC3 of the PPI (Address 0104H) controls the LPBK/ signal as follows:

PC3 = 0 Activates the LPBK/ signal (active low). In the loop back mode the data output (TXD) of the 82586 LCC is routed through the MSI601 transmit logic (Manchester encoding), to the receive logic (Manchester decoding and receive clock recovery) to the MSI receive data output (MRXDD). In the loop-back mode the MSI601 does not drive the transceiver cable.

PC3 = 1 Deactivates the LPBK/ signal (high).

4. TECHNICAL DESCRIPTION 4.

4.1 Functional Description 4.1

This section describes the functions of the MSI601, refer also to MSI601 Functional Block Diagram figure 1, Timing Diagram 1 and Logic Diagrams 1 through 3. Numbers in boxes on block diagram refer to logic diagram numbers.

4.1.1 Clock Generation 4.1.1

A 20Mhz crystal oscillator provides a basic 20Mhz clock source, which drives a divide-by-two, divide-by-five counter. The 10Mhz output is used for data and clock recovery. The 2Mhz output is used for transmit data encoding and generation of a micronet transmit clock (MTXC/=1Mhz).

4.1.2 Transmit Section 4.1.2

Transmitted serial data (TXD) from the 82586, is Manchester encoded using TXD input exclusive-nor MTXC/ clock. Data transmission begins with the Request To Send (RTS/) input going low, which starts the watchdog timer and enables the synchronization FF for transmitted data (TXDE✱). Refer also to timing diagram TD1 and note that the TXDE✱ FF introduces a 1/4-bit delay between TXD input and TXDE✱ output (Transmit+/Transmit- if not in loop back mode).

The watchdog prevents a malfunction in the transmit section from tying up the network indefinity.

The transceiver cable driver is an AM26LS31C differential line driver. Outputs are short-circuit protected.

4.1.3 Receive Section

Manchester encoded data signal is received by a differential receiver, the output of which (MRXD*) is routed to the Manchester decoder (via loop-back logic). The Manchester decoder recovers the receiver clock from the Manchester encoded data using a 4-bit binary counter and a 10Mhz count frequency. The counter is automatically initialized to parallel load of value 8 decimal when there is no activity on the MRXD signal. The first negative transition of MRXD loads the counter with all zeroes and starts the counter, thus synchronizing the counter to the incoming Manchester encoded stream. Counting stops at 8 decimal. Every following data transition of MRXD in the center of a bit cell loads the counter with all zeroes and enables counting. Bit 2 of the counter constitutes the Micronet Receive Clock (MRXC/). The negative transition of MRXC/ occurs 1/4 from the start of a bit cell. At this point the data output (MRXDD) to the 82586 LCC is high if a "1" is received and low if a "0" is received.

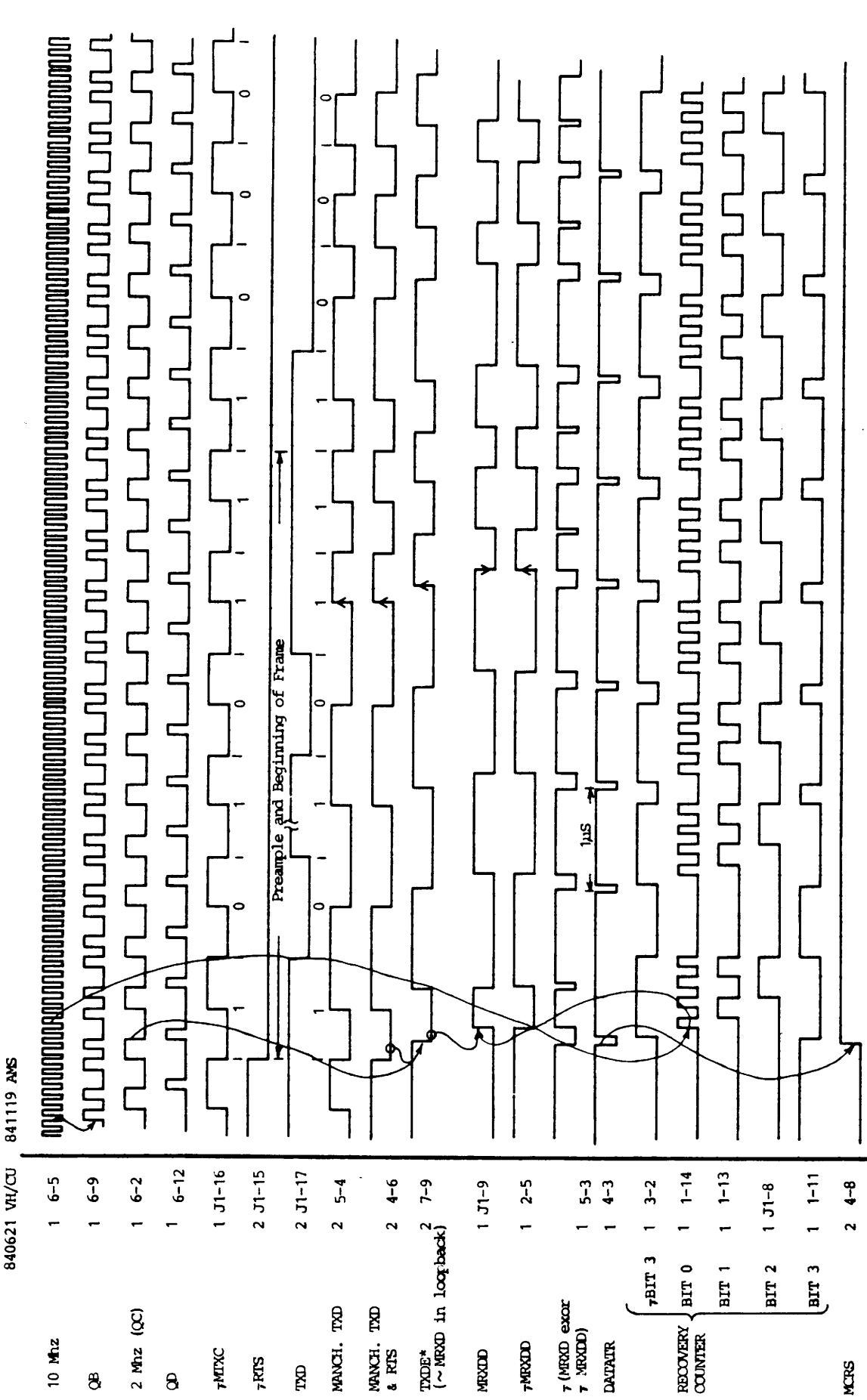
DATATR (Data transition) is a pulse indicating a Manchester data transition (center of bit cell). DATATR activates the Carrier Sense signal (MCRS). MCRS returns to low state when MRXD activity stops, and at this point the End Of Frame (EOF) signal is generated. The EOF signal causes generation of one extra MRXC pulse enabling the 82586 LCC to detect the absence of the MCRS signal. Refer also to timing diagram TD1.

4.1.4 Collision

The collision signal is generated by the RC Micronet transceiver when collision occurs. The signal is received by a differential line receiver, the output of which is active low if collision is presence. The Micronet Collision Detect signal (MCDT/) is routed to the 82586 LCC and the carrier sense circuits. The Carrier Sense (MCRS) becomes true when collision is detected.

4.1.5 Internal Loopback

When active, LPBK/ causes the MSI to route serial data from the TXD input, through the transmit logic (Manchester encoding), to the receive logic (clock recovery) to the MRXDD output, without driving the transmit output pair to the transceiver.



MSI601

MSI601 LOOPBACK MODE
TIMING DIAGRAM

TD1

A14755

4.3 Logic Diagrams with Signal Description 4.3

SIGNAL	DESTINATION	DESCRIPTION
₇MRXC	J1-8	Micronet Receive Clock.
MRXDD	J1-9	Micronet Receive Data Signal.
DATATR	P2	Data transition. A low to high transition indicates that data is being received.
2Mhz	P2	2Mhz clock for micronet data encoding.
₇MTXC	J1-16,P2	Micronet Transmit Clock.
10Mhz	P1	10Mhz clock for micronet clock and data recovery.

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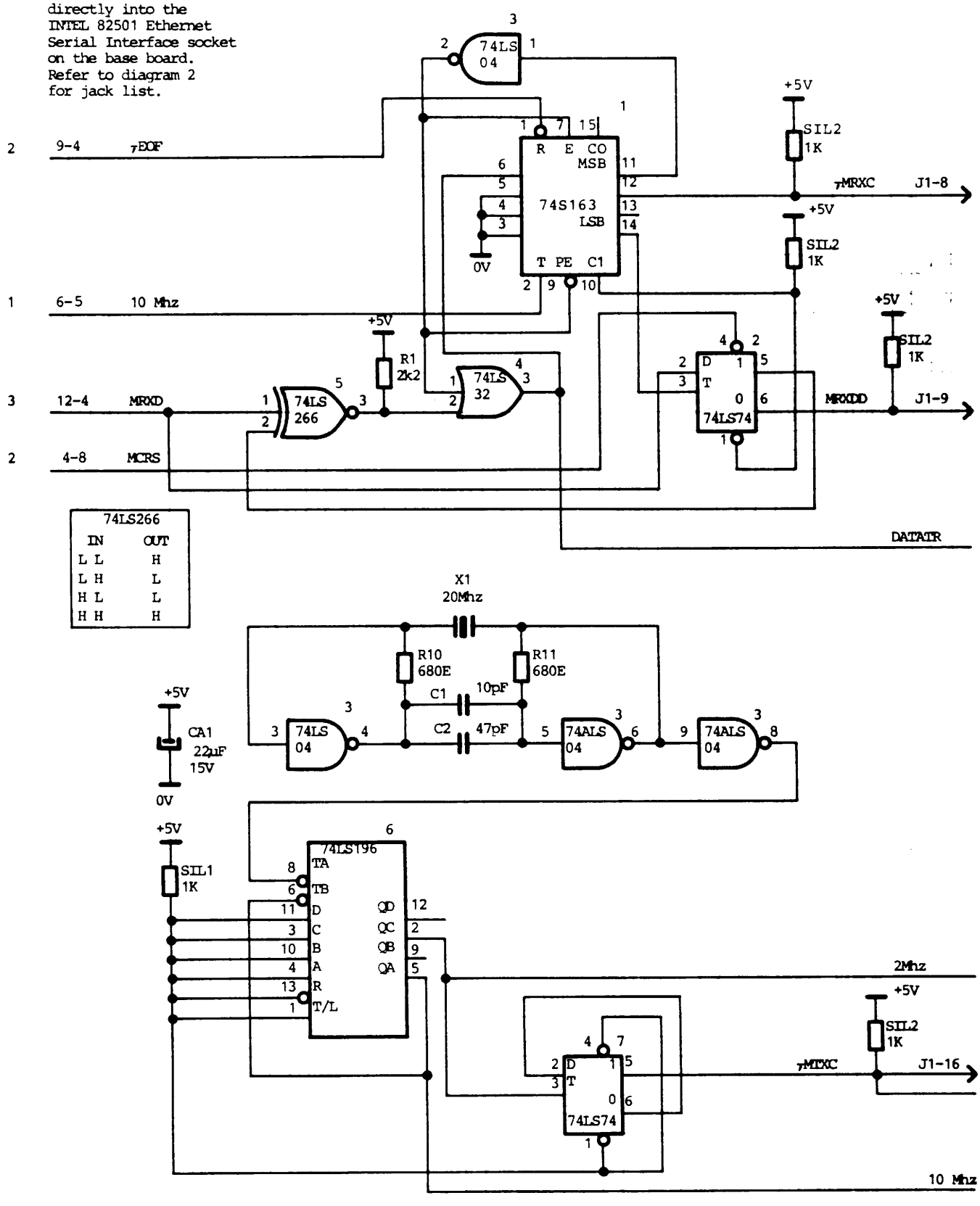
Unit		
MSI601	Clock Recovery and clock generator	P1
Dwg. No. A26366		

Jack 1 is a 20-pin DIP jack, which fits directly into the INTEL 82501 Ethernet Serial Interface socket on the base board. Refer to diagram 2 for jack list.



MSI Micronet Serial Interface

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SIGNAL	DESTINATION	DESCRIPTION
LOGIC 1A	P2	Logic 1 generator.
TXDE*	P3	Micronet Manchester encoded transmit data to loopback circuit.
MCRS	P1	Micronet Carrier sense signal to recovery circuit.
~MCRS	J1-6,P3	Inverted Micronet Carrier Sense signal to indicator and output jack.
~EOF	P1	End of Frame signal.

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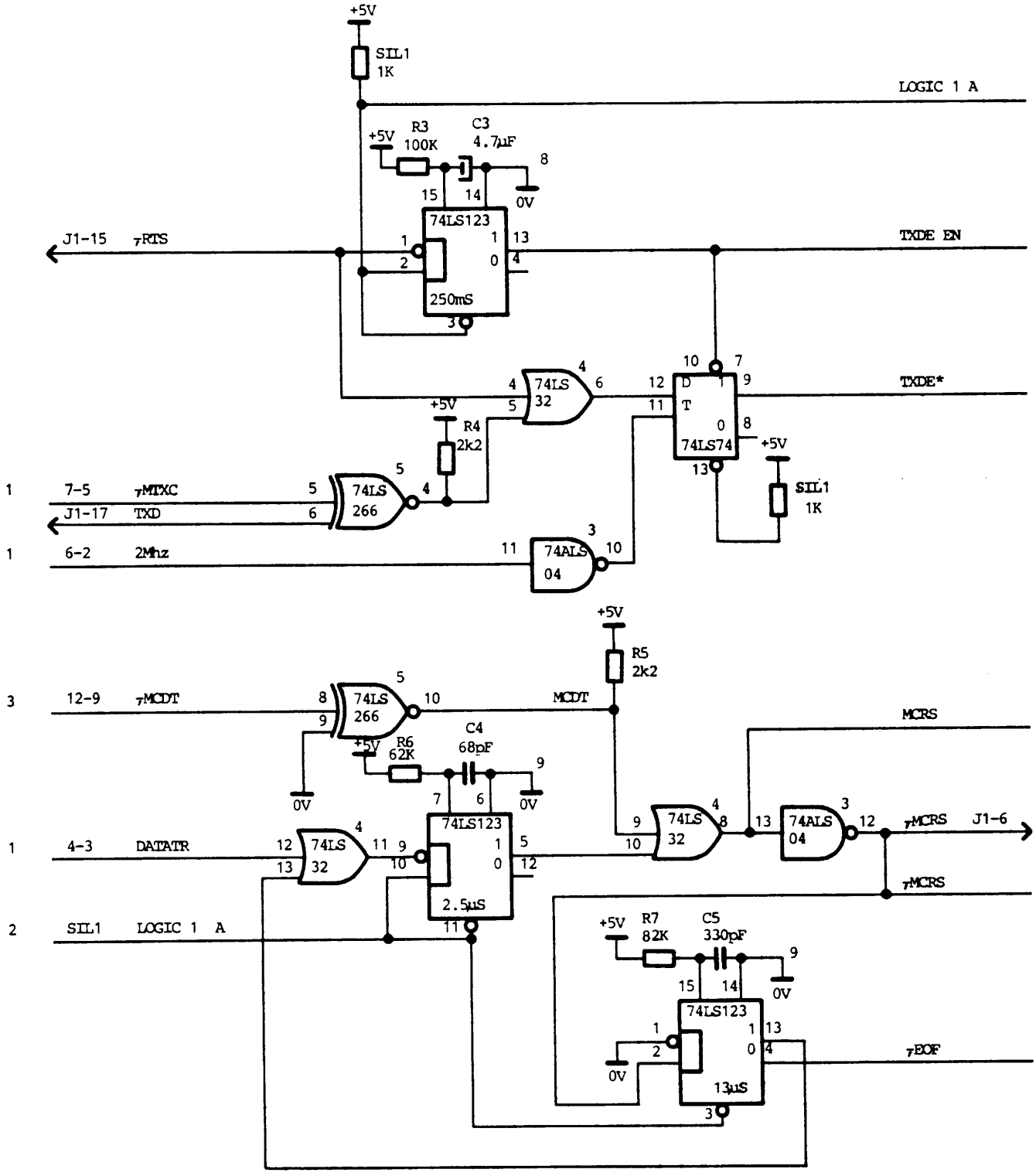
Unit		
MSI601	Transmit Data Encoding, Watchdog and	P2
Dwg. No. A26367	Carrier Sense Generator	



JACK 1 List

DIP PIN	SIGNAL		DIP PIN	SIGNAL	
1	NOT USED		20	+5V	
2	NOT USED		19	TRANSMIT +	
3	7LOOP BACK	(7LPBK)	18	TRANSMIT -	
4	RECEIVE +		17	TRANSMIT DATA	(TXD)
5	RECEIVE -		16	7MICRONET TRANSMIT CLOCK	(7MTXC)
6	7MICRONET CARRIER SENSE	(7MCRS)	15	7REQUEST TO SEND	(7RTS)
7	7MICRONET COLLISION DET.	(7MCDT)	14	NOT USED	
8	7MICTONET RECEIVE CLOCK	(MRXC)	13	NOT USED	
9	MICRONET RECEIVE DATA	(MRXDD)	12	COLLISION PRESENCE +	
10	0 VOLT		11	COLLISION PRESENCE -	

SIGNAL	DESTINATION	DESCRIPTION
₇MCDT*	P3	Micronet Collision Detect signal to loopback circuit.
MRXD*	P3	Received Micronet Manchester encoded data to loopback circuit.
TRANSMIT+ TRANSMIT-	J1-19 J1-18	Micronet transmit pair to transceiver.
MRXD	P1	Received Micronet Manchester encoded data to recovery circuit.
TXDE	P3	Micronet Manchester encoded transmit data to transceiver cable driver.
₇MCDT	J1-7,P2	Micronet Collision Detect to output jack and carrier sense circuit

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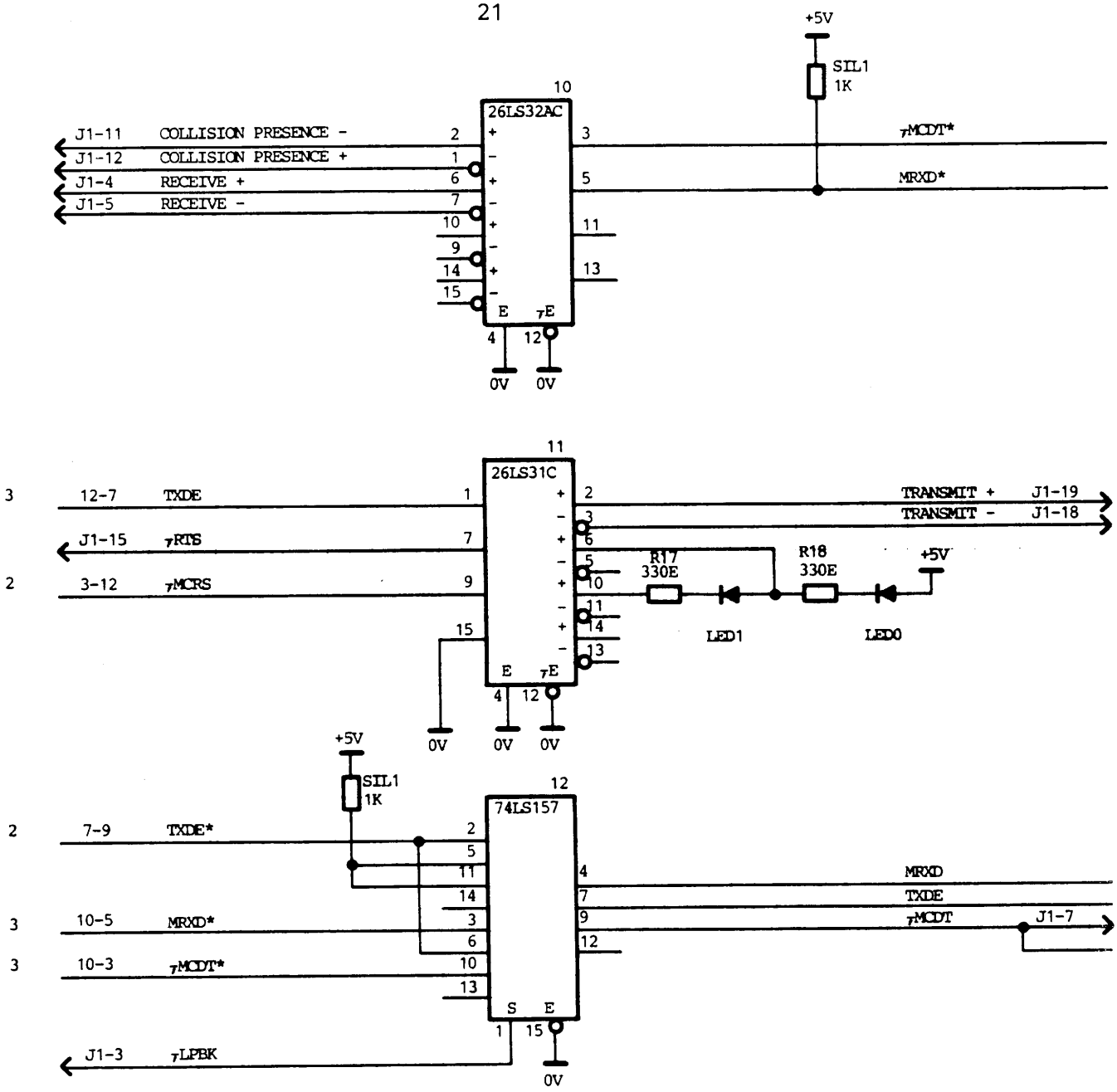
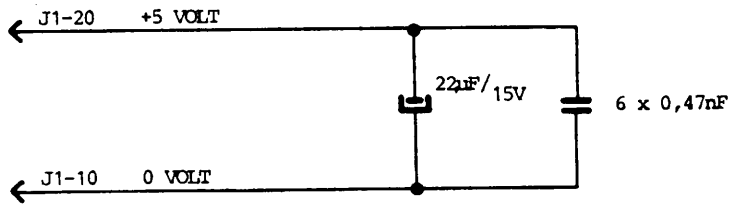
Unit		
MSI601	Transceiver Cable Interface and Loopback	P3
Dwg. No. A26368	Circuits.	





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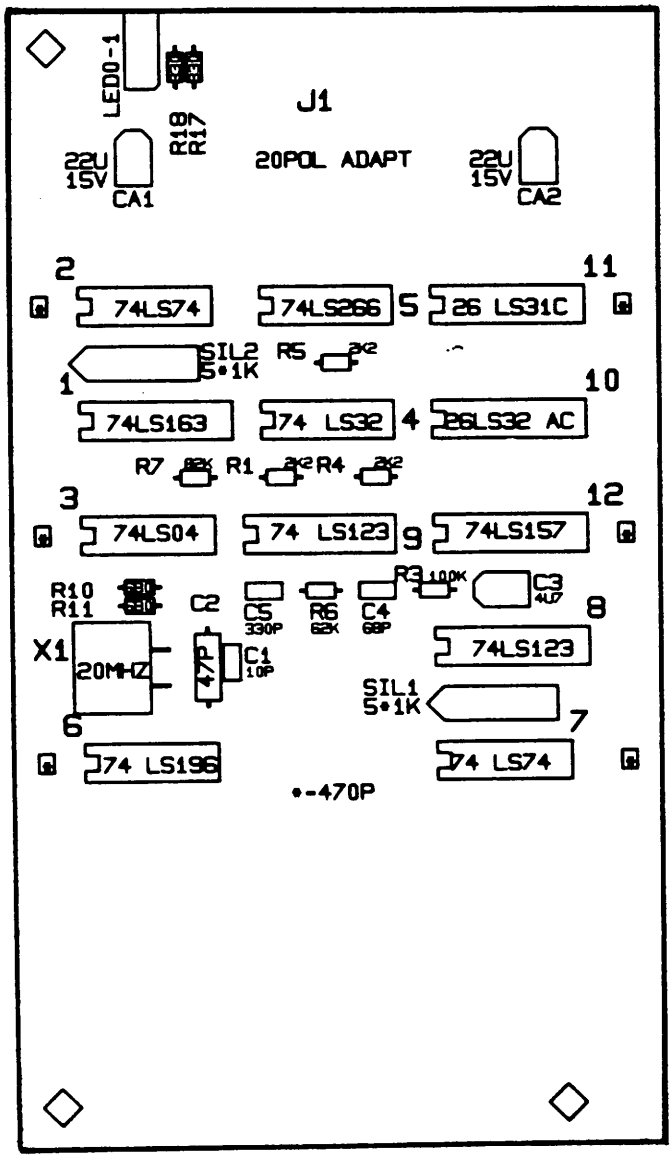
4.4 Assembly Drawing

4.4



COMP.-NOTATION PCB142

A. REFERENCES

1. ETC601/611 Hardware Reference Manual RCSL no. 99 0 00772.

2. ETC601 Hardware Selftest, Users Manual RCSL no. 99 1 09944.

B. INDICES

B.1 Survey of Figures

RETURN LETTER

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