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IFP802
Technical Manual

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Abstract:

This manual contains technical informations including logic diagrams on the IFP802.

(100 printed pages)

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RCSL Nr. 46-F 0087

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1. INTRODUCTION

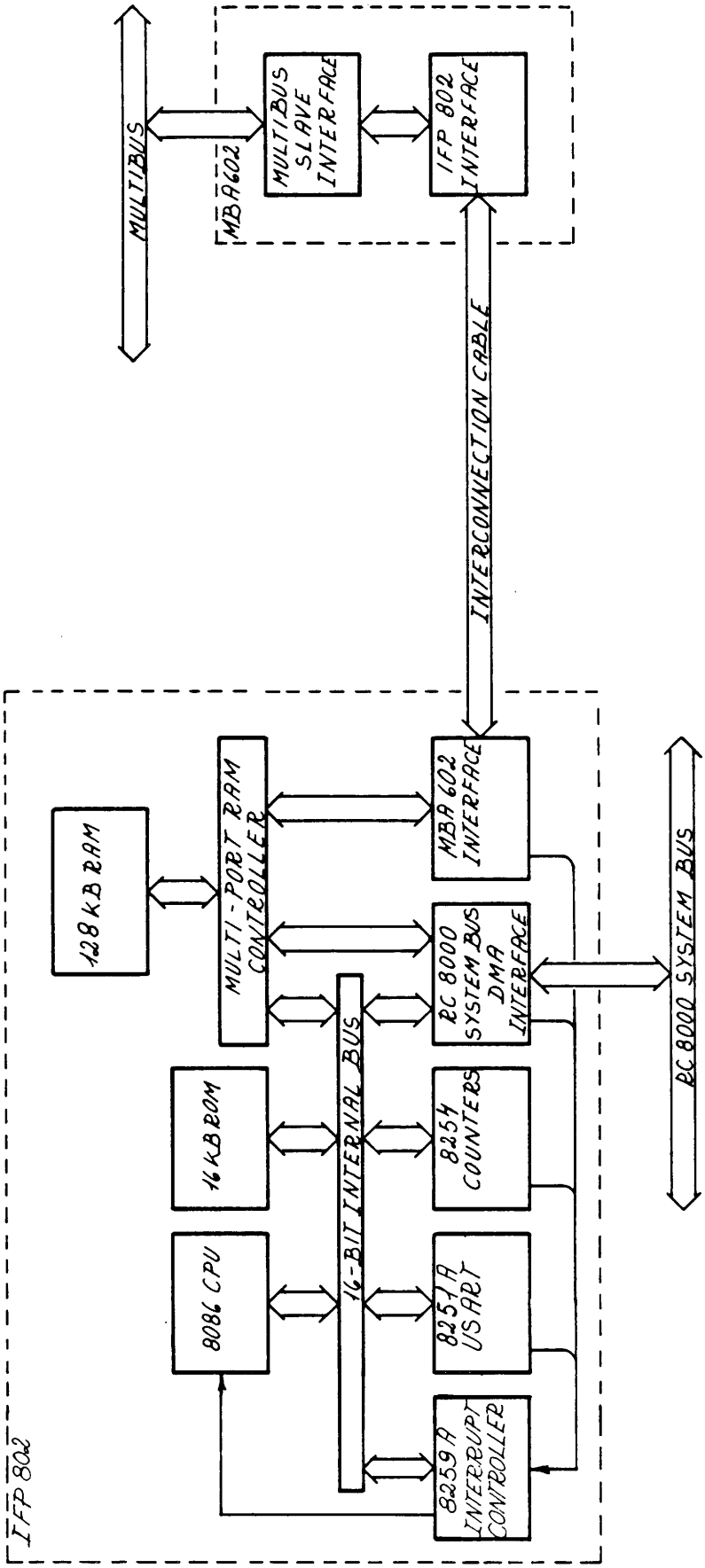
The IFP 802, Interface Processor, is the RC8000 part of two controllers connecting the RC8000 computer system and the Multibus. Connection to the Multibus is provided by the MBA 602, Multibus Adapter. The IFP 802 and the MBA 602 are interconnected by a cable with a maximum length of 12 meters. See fig. 1.

The IFP 802 is an 8086 microprocessor based controller provided with a multi-port RAM with one port reserved for multibus access through the MBA 602. The multi-port RAM is used for communication between RC8000 and Multibus units. Seen from the Multibus the IFP 802 - MBA 602 is a slave unit with 64 K byte RAM.

For test and debugging purposes the IFP 802 is provided with a V.24/V.28 Consol interface.

Transfer of data between the RC8000 memory and the IFP 802 multiport RAM is controlled by a DMA controller. During data transfer from RC8000 memory to the IFP the RC8000 data representation with 3 bytes/word is transformed to the Intel 16-bit representation with 2 bytes/word and with bytes in the reverse order within the word. When data is transferred from the IFP to the RC8000 memory, the Intel 16-bit data representation is converted to the RC8000 24-bit data representation.

RC8000 activates the IFP 802 by means of a DO (data out) instruction, where the transferred data specifies 1 of 4 possible commands. One of the commands generates a reset signal, which has the same effect as a power-on reset. The other 3 commands generate interrupt requests to the 8086 microprocessor.

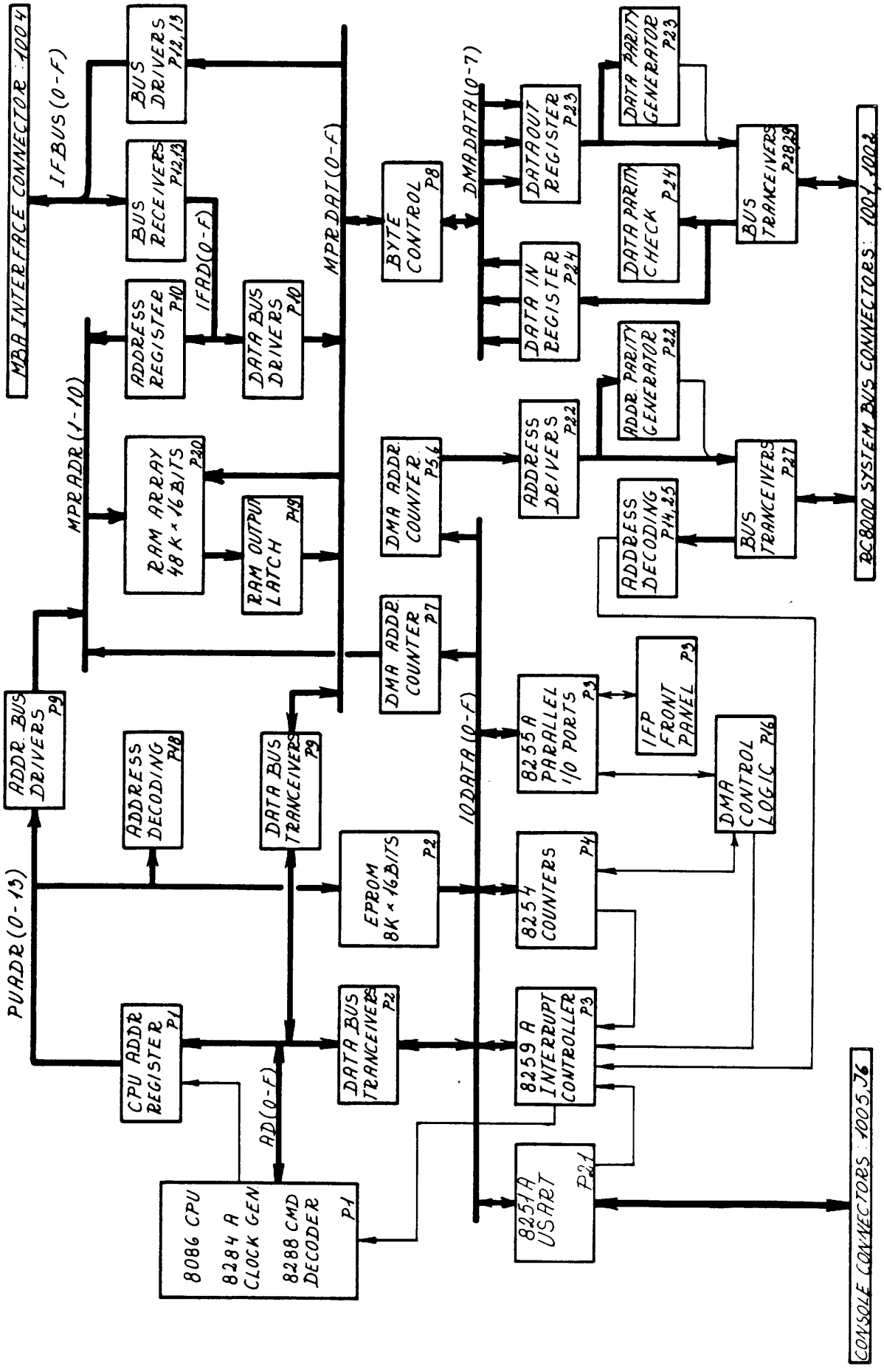


AAJ AGA

IFP 802

R 13943

RC 8000 SYSTEM BUS INTERFACE TO MULTIBUS



IFP 802

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IFP 802 DATA PATHS BLOCKDIAGRAM

3. PROGRAMMING INFORMATION

This chapter provides programming information for the I/O devices controlled by the 8086 microprocessor. For the 8284, 8255A, 8251A and 8259A I/O devices only information depending on the application in the IFP 802 is provided. For a more detailed description of these four devices is referred to the relevant Intel datasheets.

3.1 Initialization

A reset signal for the 8086 system is generated by the following three events:

- power is turned on
- a system reset signal on the RC8000 System Bus
- a reset command to the IFP 802 from the RC8000

The reset signal has the following effect:

- the 8086 executes a jump to location FFFF0H
- the 8255A I/O ports are set to the input mode, i.e. the output signals are inactive
- the DMA Channel is forced to an idle state, waiting for a command
- the RC8000 System Bus access logic is reset
- the 8251A is forced to an idle state, waiting for a new set of control words

The 8254 and the 8259A are not directly affected by the reset signal.

3.2 Memory Addressing

The IFP 802 includes 128 K bytes of dynamic random access memory (RAM) and 16 K bytes of read-only memory (EPROM). The location of RAM and EPROM within the 1 M byte memory address space of the 8086 is shown on the next page.

RAM: from 00000H to 0FFFFH
EPROM: - FC000H - FFFFFH

Access outside the above mentioned address ranges may cause hang up of the CPU in a wait state.

3.3 I/O Addressing

The I/O devices are located within the I/O address space of the 8086. The I/O address decoder operates only on the 8 least significant bits of the I/O address. All devices may therefore be addressed with an immediate byte in the IN and OUT instruction. I/O addresses are assigned according to the table on the next page.

DEVICE	HEX ADDRESS	FUNCTION
8259A	40	Write: ICW1, OCW2, OCW3 Read: Status and Poll
	42	Write: ICW2, ICW3, ICW4, OCW1 (Mask) Read: OCW1 (Mask)
8255 Parallel I/O ports	48	Read: Port A. RC8000 bus access status and switches
	4A	Read: Port B. IFP 802 Device Address switches
	4C	Write: Port C. DMA control and front panel LED's
	4E	Write: Port control
8254 Timers	50	Write: Counter 0. Interval timer Read: Counter 0
	52	Write: Counter 1. DMA byte counter Read: Counter 1
	54	Write: Counter 2. Baud Rate generator Read: Counter 2
	56	Write: Counter control
8251A	58	Write: Transmit data Read: Received data
	5A	Write: Mode or Command Read: Status
RC8000 System Bus Address Counter	80	Write: Loads address bits (8:23)
	82	Write: Loads address bits (0:7)
Multi-port RAM Address Counter	84	Write: Loads address bits (F:0)
	86	Write: Loads address bit (10)
MBA-Access Register	88	Write: MBA-access enabling/disabling

3.4 8254 Counter/Timer

The 8254 contains three independent 16-bit counters. In the IFP 802 Counter 0 is used as an interval timer, which generates interrupt at programmable intervals. Counter 1 is used as byte counter for the DMA channel. Counter 2 is used as Baud Rate generator for the 8251A USART.

3.4.1 Interval Timer

Counter 0 operates in mode 2 as a programable rate generator. It generates interrupts with:

N x 0.8 microseconds intervals

where N is a 16-bit binary number. Counter 0 is loaded with N at initialization or when a new interrupt interval is desired.

The operating mode of the counter is defined by loading the Control Word Register with a Control Byte as shown below.

Address: 56 hex

7	6	5	4	3	2	1	0	
0	0	1	1	X	1	0	0	Control Byte for Counter 0

The binary number N(F-0), defining the interrupt interval is loaded into Counter 0 as two consecutive bytes as described below.

Address: 50 hex

7	6	5	4	3	2	1	0	
N(7-0)								Least Significant Byte

7	6	5	4	3	2	1	0	
N(F-8)								Most Significant Byte

It is important that the bytes are loaded in the order described above. The interrupt interval may be redefined at any time by loading Counter 0 with a new count ratio.

3.4.2 DMA Byte Counter

Counter 1 operates in mode 0, interrupt on Terminal Count. It must be initialized with a Control Byte as shown below.

Address: 56 hex

7	6	5	4	3	2	1	0	
0	1	1	1	0	0	0	0	Control Byte for Counter 1

The binary number CN(F-0), which defines the number of bytes to be transferred by the DMA channel, must be loaded into Counter 1 as two consecutive bytes as shown below.

Address: 52 hex

7	6	5	4	3	2	1	0	
CN(7-0)								Least Significant Byte

7	6	5	4	3	2	1	0	
CN(F-8)								Most Significant Byte

It is important for the operation of the counter that both bytes are loaded and that they are loaded in the order shown above.

3.4.3 Baud Rate Generator

Counter 2 operates in mode 3, square wave mode. It must be initialized with a control Byte as shown below.

Address: 56 hex

7	6	5	4	3	2	1	0	
1	0	1	1	0	1	1	0	Control Byte for Counter 2

The binary number N(F-0) defines the period time as: N x 0,54253 microsecond and a duty cycle of 50% and must be loaded into Counter 2 as two consecutive bytes as shown below.

Address: 52 hex

7	6	5	4	3	2	1	0	
N(7-0)								Least Significant Byte

7	6	5	4	3	2	1	0	
N(F-8)								Most Significant Byte

It is important that the Control Byte is loaded before the initial count, and that the count is loaded as shown above.

3.5 8255A Parallel I/O Ports

The 8255A contains three 8-bit ports (PA, PB and PC), which may be programmed to be either input or output ports in any combination. All ports are used in the IFP 802. After a reset signal, all ports will be in input mode and the control register will be cleared. The operating mode of the ports is defined by loading the Control Word Register with a Control Byte as described below.

Address: 4E hex

7	6	5	4	3	2	1	0	
1	0	0	1	0	0	1	0	Control Byte

Note that only write operations are allowed to the Control Word Register.

3.5.1 Port A

Port A is an input port. It is used to read a status byte containing status for RC8000 System Bus access, DMA status and the state of two switches used for diagnostic purposes.

Address: 48 hex

7	6	5	4	3	2	1	0	
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Port A input

PA0: SBNACK. Indicates that the addressed RC8000 slave unit responded with a NACK (negative acknowledge).

PA1: SBTIMEOUT. Indicates that the addressed RC8000 slave unit did not respond within approximately 4 uS.

PA2: SBPARITY. Indicates parity error in the data received during an RC8000 System Bus read operation.

PA3: SBERROR. Indicates that at least one of the three errors described above has occurred.

PA4: SBREADY. Indicates the completion of a data transfer to or from an RC8000 slave unit.

PA5: DMAINTR. Indicates that the DMA channel has finished an operation. This signal will also generate an interrupt request to the 8086 microprocessor.

PA6: ADJUST switch.

PA7: TEST MODE switch.

PA7 = 0: Switch position SHORT

PA7 = 1: Switch position CONTINOUS.

3.5.2 Port B

Port B is an input port. It is used for reading the switch setting of the IFP802 Device Address switch.

Address: 4A hex

7	6	5	4	3	2	1	0	
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	Port B input

PB0: RC8000 System Bus Address bit 20
PB1: RC8000 System Bus Address bit 19
PB2: RC8000 System Bus Address bit 18
PB3: RC8000 System Bus Address bit 17
PB4: RC8000 System Bus Address bit 16
PB5: Not used
PB6: Not used
PB7: Not used

3.5.3 Port C

Port C is an output port. It is used to control the operation of the DMA Channel and to generate different control signals. The output signals from Port C are used as described below.

PC0: DMARDC. Read command to the DMA Channel. Starts a data transfer from RC8000 to multi-port RAM.
PC1: DMAWRC. Write command to the DMA Channel. Starts a data transfer from multi-port RAM to RC8000.
PC2: MBAINTR. A change from 0 to 1 generates a Multibus interrupt request.
PC3: MBARESET. Controls the -,INIT line on the Multibus. PC3=1 will hold the -,INIT line low.
PC4: Controls 'RC8000 READ' lamp on the IFP802 front panel. PC4=1 turns the lamp on.
PC5: Controls 'RC8000 WRITE' lamp on the IFP802 front panel. PC5=1 turns the lamp on.
PC6: Controls 'MBA ACCESS' lamp on the IFP802 front panel. PC6=1 turns the lamp on.
PC7: Controls 'DIAGNOSTIC' lamp on the IFP802 front panel. PC7=1 turns the lamp on.

The outputs of Port C can be controlled in two different ways as described below.

One write operation controls all Port C outputs.

Address: 4C hex

7	6	5	4	3	2	1	0	
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	Port C output

Any port C output can be set or reset independent of other outputs by using a special format of the Control Byte.

Address: 4E hex

7	6	5	4	3	2	1	0	
0	X	X	X	B2	B1	B0	S	Bit set/reset format

B(2-0) is a binary number, which selects the Port C output bit to be reset or set. B0=LSB.

S=0: Reset selected bit.
S=1: Set selected bit.

3.6 8259A Interrupt Controller

The eight interrupt inputs, IR0 to IR7, are used as described below.

IR0: Interval Timer interrupt (8254 Counter 0).
IR1: Receive interrupt from the USART. Indicates that a character is ready for the CPU.
IR2: Transmit interrupt from the USART. Indicates that the USART is ready to accept a new character for transmission.
IR3: DMA Channel interrupt. Indicates that the DMA Channel has finished an operation.

IR4: Interrupt request from Multibus. Generated at write access to multi-port RAM locations, 4000-4007 hex, from the Multibus.
IR5: COMMAND(1) received from RC8000 System Bus.
IR6: COMMAND(2) received from RC8000 System Bus.
IR7: COMMAND(3) received from RC8000 System Bus.

The 8259A must be initialized with a sequence of three Initialization Command Words, ICW1, ICW2 and ICW4, as described below.

Address: 40 hex

7	6	5	4	3	2	1	0	
X	X	X	1	0	X	1	1	ICW1

Address: 42 hex

7	6	5	4	3	2	1	0	
T7	T6	T5	T4	T3	X	X	X	ICW2

T(7-3) is the 5 most significant bits of the interrupt vector. The 3 least significant bits are set by the 8259A according to the interrupt level.

Address: 42 hex

7	6	5	4	3	2	1	0	
0	0	0	0	0	X	EOI	1	ICW4

EOI=0: Normal EOI (end of interrupt) mode.
EOI=1: Automatic EOI mode.

After the initialization sequence, the 8259A operates in the fully nested mode. IR0 has the highest priority and IR7 the lowest. During operation, the operating mode of the 8259A may be further controlled and modified by means of Operation Command Words (OCW).

Address: 42 hex

7	6	5	4	3	2	1	0	
M7	M6	M5	M4	M3	M2	M1	M0	OCW1

OCW1 controls the Interrupt Mask Register. A write command sets the mask bits and a read command reads the mask. M0 masks IR0, M1 masks IR1 and so forth.

M=0: Enables the corresponding IR input.
M=1: Disables the corresponding IR input.

Address: 40 hex

7	6	5	4	3	2	1	0	
R	SL	EOI	0	0	L2	L1	L0	OCW2

OCW2 is used for end of interrupt, automatic rotation and specific rotation operations.

L(2-0) is used to designate an interrupt level (0-7) to be acted upon for the operation selected by the EOI, SL and R bits.

R, SL EOI	OPERATION
001	Non-specific EOI command
011	Specific EOI command
101	Rotate on non-specific EOI command
100	Rotate in automatic EOI mode (SET)
000	Rotate in automatic EOI mode (CLEAR)
111	Rotate on specific EOI command
110	Set priority command
010	No operation

Address: 40 hex

7	6	5	4	3	2	1	0	
0	ESM	SMM	0	1	P	RR	RIS	OCW3

OCW3 is used to issue various modes and commands to the 8259A.

RR, RIS

00	No action
01	No action
10	Read Interrupt Request Register (IRR) on next read command (addr. 40 hex)
11	Read In-Service Register (ISR) on next read command (addr. 40 hes)

P

0	No Poll Command
1	Poll Command

ESM, SMM

00	No action
01	No action
10	Reset special mask
11	Set special mask

For a detailed description of the operating modes of the 8259A is referred to the data sheet.

3.7 DMA Channel

The DMA Channel transfers data from RC8000 memory or I/O locations to IFP802 multi-port RAM or in the opposite direction. Commands (Read or Write) to the DMA Channel are issued through Port C of the 8255A (see subsection 3.5.3). After termination of a data transfer, status can be read through Port A of the 8255A (see subsection 3.5.1). The number of bytes to be transferred by a DMA operations is controlled by Counter 1 of the 8254 (see subsection 3.4.2).

The source and destination addresses for a DMA transfer are controlled by two counters, the RC8000 System Bus Address Counter (SBAC) and the Multi-Port RAM Address Counter (MPRAC).

The SBAC is a 24-bit counter, which is incremented by 2 for each word (3 bytes) transferred to or from RC8000. It must be initialized with a 16-bit word and a byte as shown below. SBAC(0) is the most significant bit and SBAC(23) the least significant bit.

Address: 80 hex

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
A8	A9	----------												A22	A23

SBAC(8:23)

Address: 82 hex

7	6	5	4	3	2	1	0
A0	A1					A6	A7

SBAC(0:7)

The MPRAC is a 17-bit counter, which is incremented by 1 for each byte transferred to or from the muli-port RAM. The counter must be initialized with a 16-bit word and a byte. MPRAC0 is the least significant bit.

Address: 84 hex

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
AF	AE	AD	AC	AB	AA	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

MPRAC(F-0)

Address: 86 hex

7	6	5	4	3	2	1	0
NOT USED							A10

MPRAC10

3.7.1 DMA Read Operation

A DMA read operation transfers data from RC8000 RAM to IFP802 multi-port RAM. The DMA Channel converts from RC8000 format with 3 bytes/word to Intel format with 2 bytes/word as shown below.

RC8000 RAM

	0	7	8	15	16	23
+6						
+4						
+2	B3		B4		B5	
+0	B0		B1		B2	

=>

MULTI-PORT RAM

	F	8	7	0
+6				
+4	B5		B4	
+2	B3		B2	
+0	B1		B0	

Even start address for MPRAC.

RC8000 RAM

	0	7	8	15	16	23
+6						
+4						
+2	B3		B4		B5	
+0	B0		B1		B2	

=>

MULTI-PORT RAM

	F	8	7	0
+6			B5	
+4	B4		B3	
+2	B2		B1	
+0	B0			

Odd start address for MPRAC.

The address counters (SBAC and MPRAC) and the byte counter (BCNT) must be initialized as specified below.

SBAC: RC8000 buffer start address (word)
MPRAC: Multi-Port RAM buffer start address (byte)
BCNT: Number of bytes - 2

The data transfer is started by a Read Command, DMARDC, to the DMA channel, see subsection 3.5.3.

3.7.2 DMA Write Operation

A DMA write operation transfers data from the IFP802 multi-port RAM to RC8000 RAM (or I/O). The DMA Channel converts from Intel format with 2 bytes/word to RC8000 format with 3 bytes/word as shown below.

MULTI-PORT RAM

	F 8	7 0
+6		
+4	B5	B4
+2	B3	B2
+0	B1	B0

=>

RC8000 RAM

	0 7	8 15	16 23
+6			
+4			
+2	B3	B4	B5
+0	B0	B1	B2

Even start address for MPRAC.

MULTI-PORT RAM

	F 8	7 0
+6		B5
+4	B4	B3
+2	B2	B1
+0	B0	

=>

RC8000 RAM

	0 7	8 15	16 23
+6			
+4			
+2	B3	B4	B5
+0	B0	B1	B2

Odd start address for MPRAC.

The address counters (SBAC and MPRAC) and the byte counter (BCNT) must be initialized as specified below.

SBAC: RC8000 buffer start address - 2 (word)
MPRAC: Multi-Port RAM buffer start address (byte)
BCNT: Number of bytes - 1

Note that only whole words (3 bytes) are transferred to RC8000. In order to ensure that all bytes are transferred, the specified number of bytes must be a multiple of 3.

The DMA operation is started by a Write Command, DMAWRC, to the DMA Channel, see subsection 3.5.3.

3.7.3 DMA Command Termination

One of the following two events will terminate a DMA operation:

1) The specified number of bytes have been transferred.
2) An RC8000 bus error.

At termination, the DMA Channel generates an interrupt request (IR3) and sets the status bit, DMAINTR. IR3 and DMAINTR are cleared, when the current command (DMARDC or DMAWRC) is cleared. The DMA Channel will not accept a new command before the current command has been cleared. If termination is caused by an RC8000 bus error, the status bit, SBERROR, is set, and the status bits, SBNACK, SBTIMEOUT and SBPARITY specify the error type.

3.8 8251A USART

The 8251A is transmitting data between the IFP802 and a connected console via V24/V28 asynchronous serial interface.

After a reset signal, the 8251A will be in idle mode and must be programmed with a set of control words before data transmission is possible.

The general operational characteristics is defined in the Mode Instruction, and must be loaded after internal or external reset.

In asynchronous mode, the Command Instruction must follow the Mode Instruction.

Status can be read at any time during the functional operation. Note that status update can have a max. delay of 28 clock periods (appr. 10 usec) from the actual event affecting the status.

Address: 5A hex

7	6	5	4	3	2	1	0	
1	1	0	0	1	1	1	0	Mode Instruction

(2 stop bits, parity disabled
8 data bits and baud rate
factor = 16).

Address: 5A hex

7	6	5	4	3	2	1	0	
0	IR	RTS	ER	0	RxE	DTR	TxEN	Command Instruction

IR

0 No action

1 Internal Reset Forces 8251A to Mode Instruction Format.

RTS

0 No action

1 Request to send

ER

0 No action

1 Reset Error flags: PE, OE, FE

RxE

0 Receiver disable

1 Receiver enable

DTR

0 No action

1 Data Terminal Ready

TxEN

0 Transmitter disable

1 Transmitter enable

Address: 5A hex

7	6	5	4	3	2	1	0	
DSR	X	FE	OE	PE	X	RxR	TxR	Status Read

DSR Data Set Ready
FE Framing Error; missing stopbit
OE Overrun Error; previous character overwritten
PE Parity Error
RxR Receiver Ready; Character ready for CPU
TxR Transmitter Ready; 8251A ready for character from CPU.

Address: 58 hex

7	6	5	4	3	2	1	0	
D7	D6	D5	D4	D3	D2	D1	D0	Write/Read Data Buffer

Whenever a data chracter is sent to the CPU the 8251A automatically adds a startbit, the programmed number of stopbits and paritybit (if used) to the data chracter, and transmits it as a serial data stream with the programmed rate of 1/16 of the "Baud Rate" defined by counter 2 in the 8254. When the 8251A is ready to accept a new chracter from the CPU the TxRDY output interrupts the Interrupt Controller.

When receiving, the 8251A checks for valid startbit, parity and stopbit, and if no errors are found, the data character will be ready for the CPU when RxRDY interrupts the Interrupt Controller.

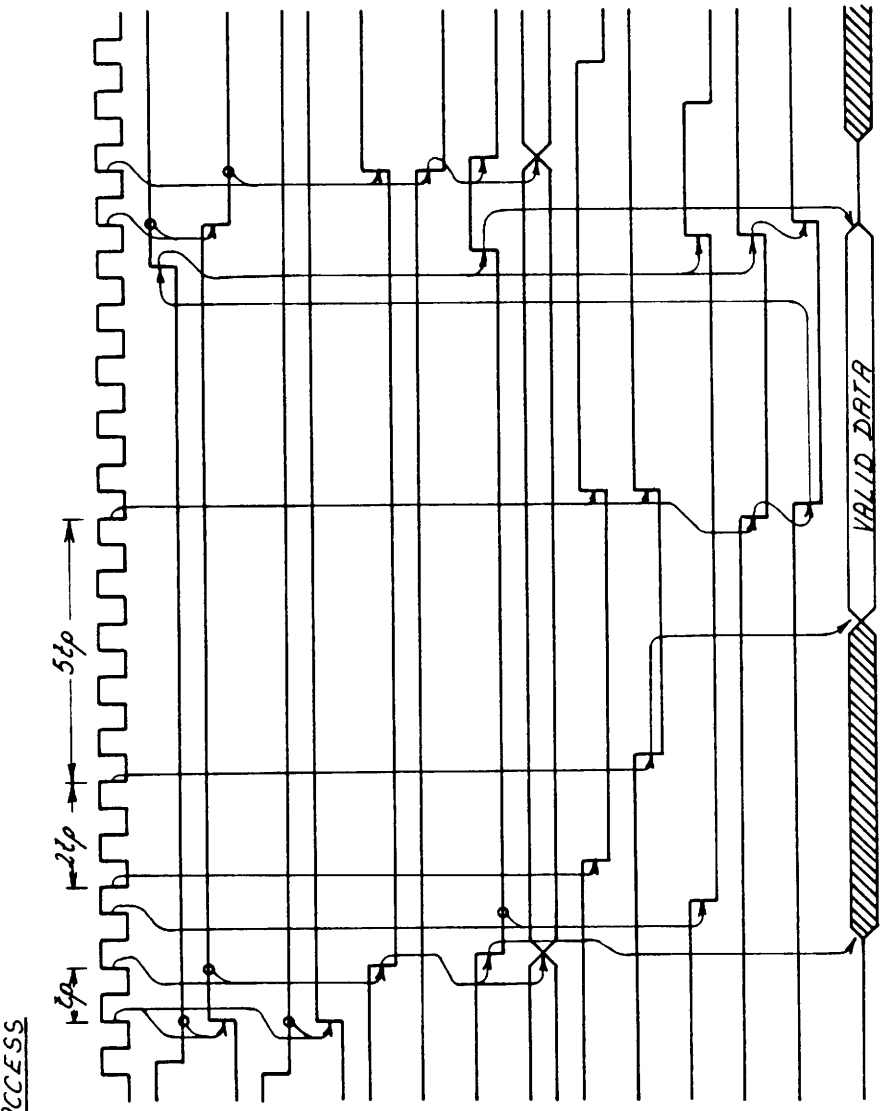
3.9 MBA-Access Register

Access from the Multibus to the IFP802 RAM-array can be enabled/disabled with this register, which can be convenient during selftest of the IFP802.

Address: 88 hex

7	6	5	4	3	2	1	0	
x	x	x	x	x	x	x	ACC	MBA-Access Register

ACC
0 Disable MBA access
1 Enable MBA access



AAJ 810907 AGA 860623

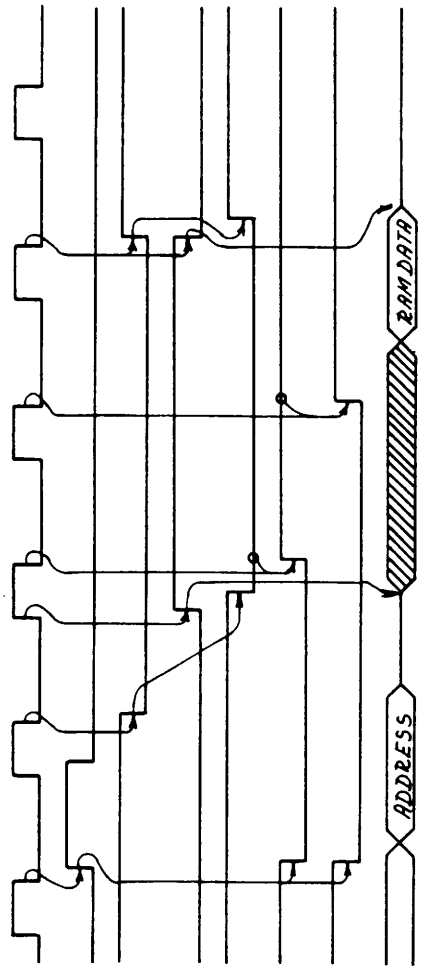
IFP 80

R 13289

MULTI-PORT RAM READ ACCESS

8109 10 AAJ 860625 RGD

8086 READ ACCESS TO MULTI-PORT RAM



IFP 802
R 13286

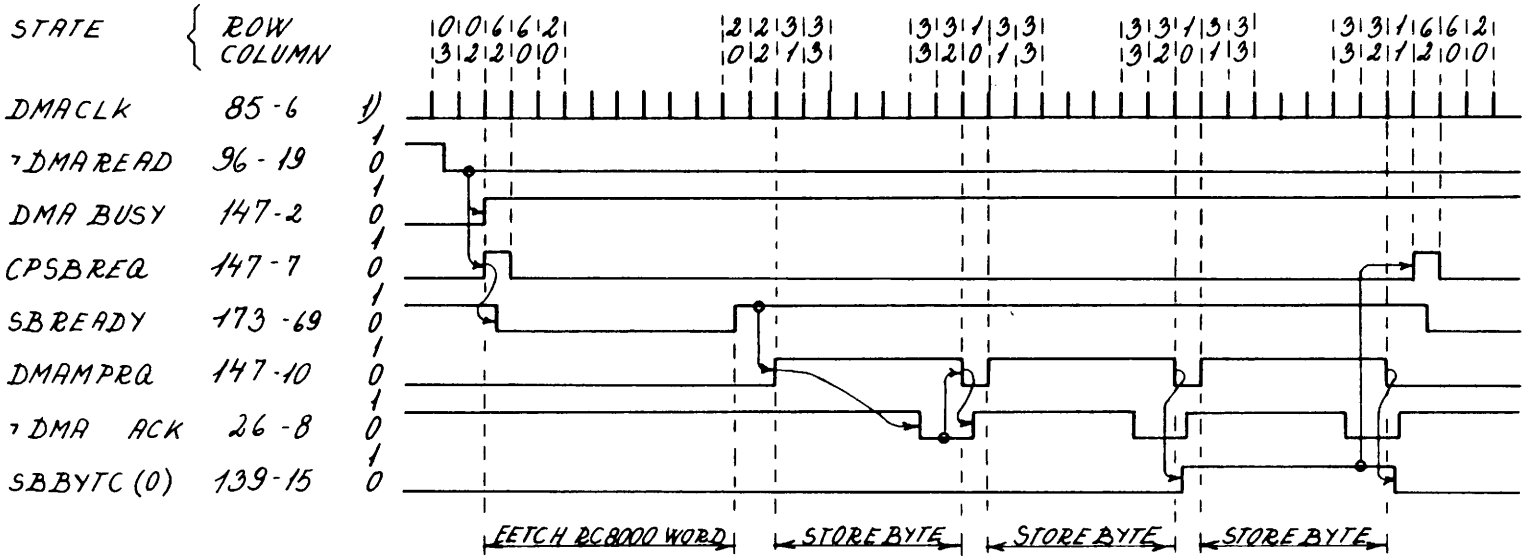
8086 READ ACCESS TO MULTI-PORT RAM

AAJ AGA
810909 860623

IFP 802
R 13287

DMA READ OPERATION

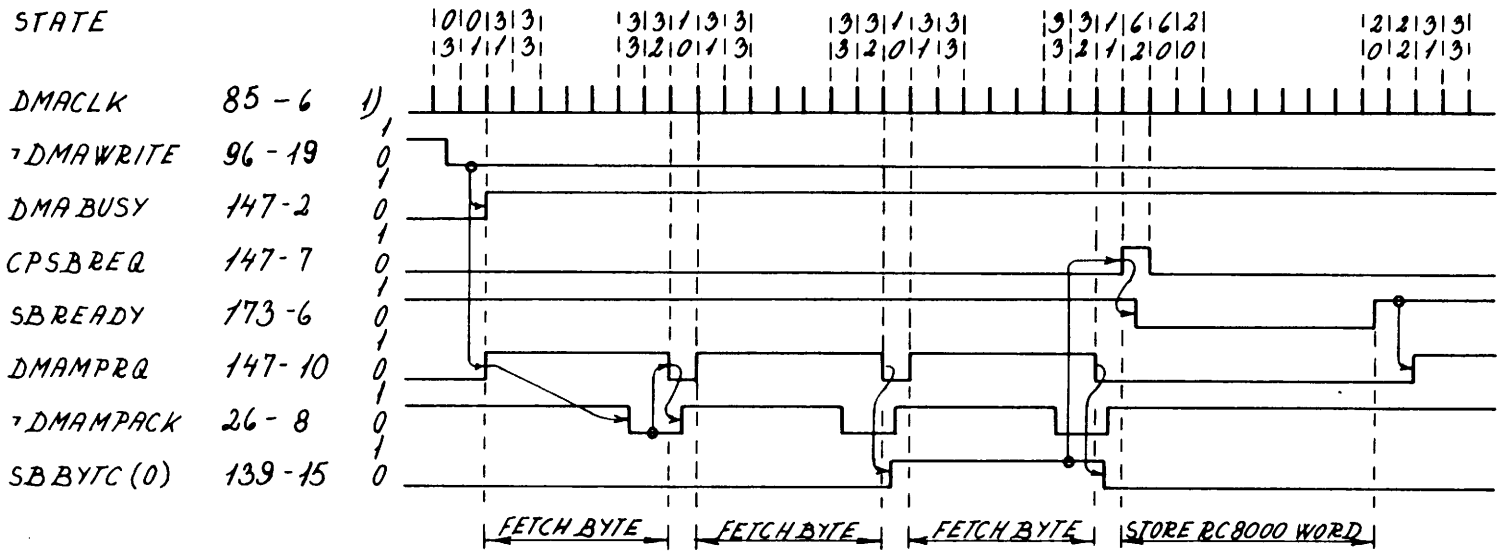
DMA READ OPERATION



1: ⊓⊔ Indicates positive edge of DMACLK.

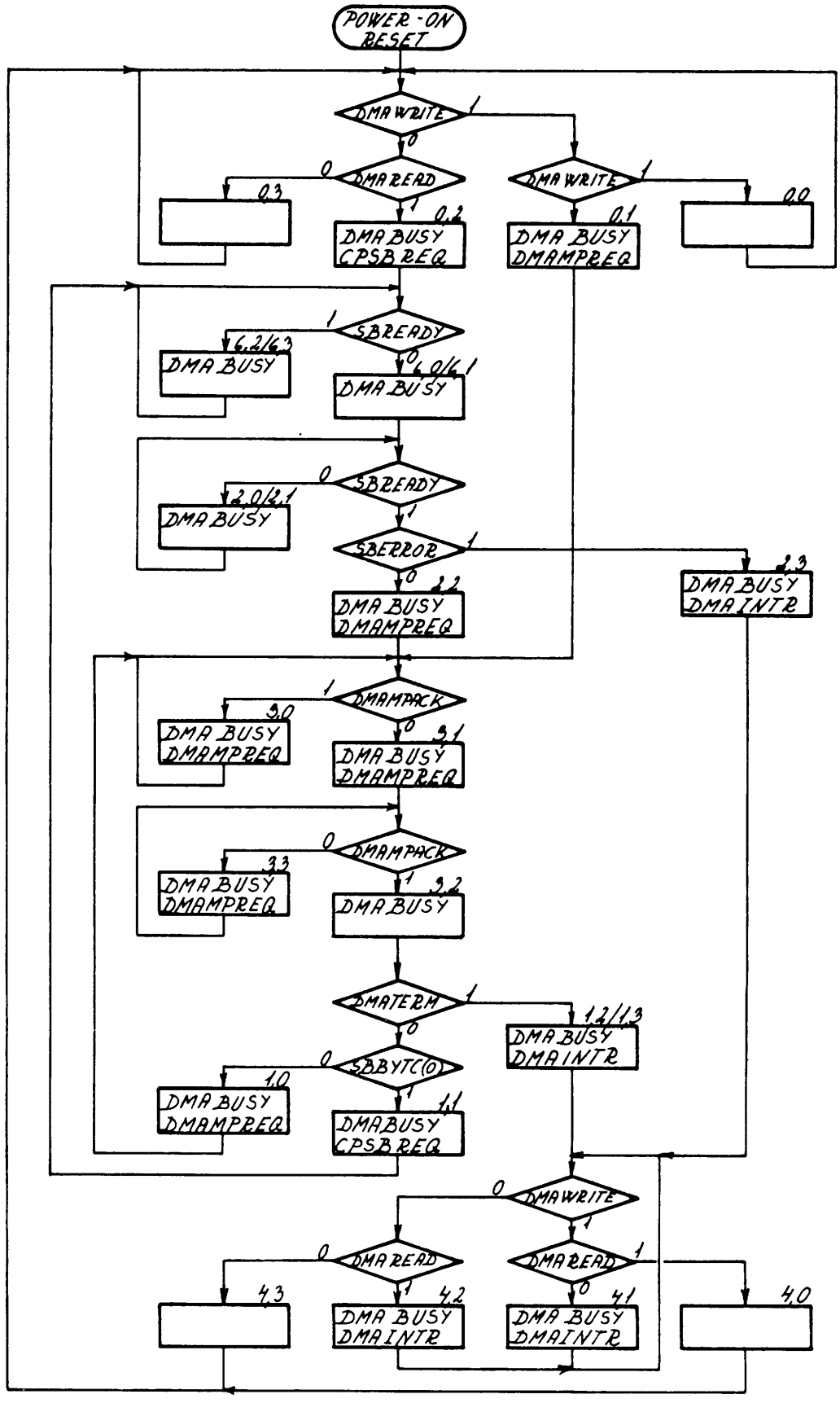
DMA READ: Data transfer from RC 8000 memory to multi-port RAM.

DMA WRITE OPERATION



1: ⊥⊥ Indicates positive edge of DMACLK. T = 90,4 ns.

DMA WRITE: Data transfer from multi-port RAM to RC 8000 memory.



ROW ADDR, CULUMN ADDR

4.3

DMA BUSY DMA INTR — OUTPUT FROM DMA CONTROLLER

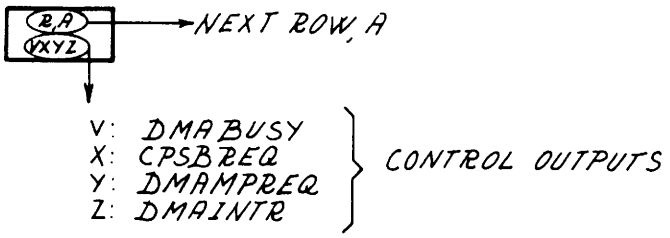
AAJ 811005 AGA 811009

IFP 802

R 13290

DMA CONTROLLER, FLOW DIAGRAM

COLUMN ADDRESS CONDITIONS		ROW	COLUMN			
			0	1	2	3
¬DMAWRITE	¬DMA READ	0	0,0 0000	3,0 1010	6,0 1100	0,0 0000
DMATERM	SBBYTC(0)	1	3,0 1010	6,0 1100	4,0 1001	4,0 1001
SBREADY	SBERROR	2	2,0 1000	2,0 1000	3,0 1010	4,0 1001
A	¬DMAMPACK	3	3,0 1010	3,1 1010	1,0 1000	3,1 1010
¬DMAWRITE	¬DMA READ	4	0,0 0000	4,0 1001	4,0 1001	0,0 0000
DMATERM	SBBYTC(0)	5				
SB READY	SBERROR	6	2,0 1000	2,0 1000	6,0 1000	6,0 1000
A	¬DMAMPACK	7				

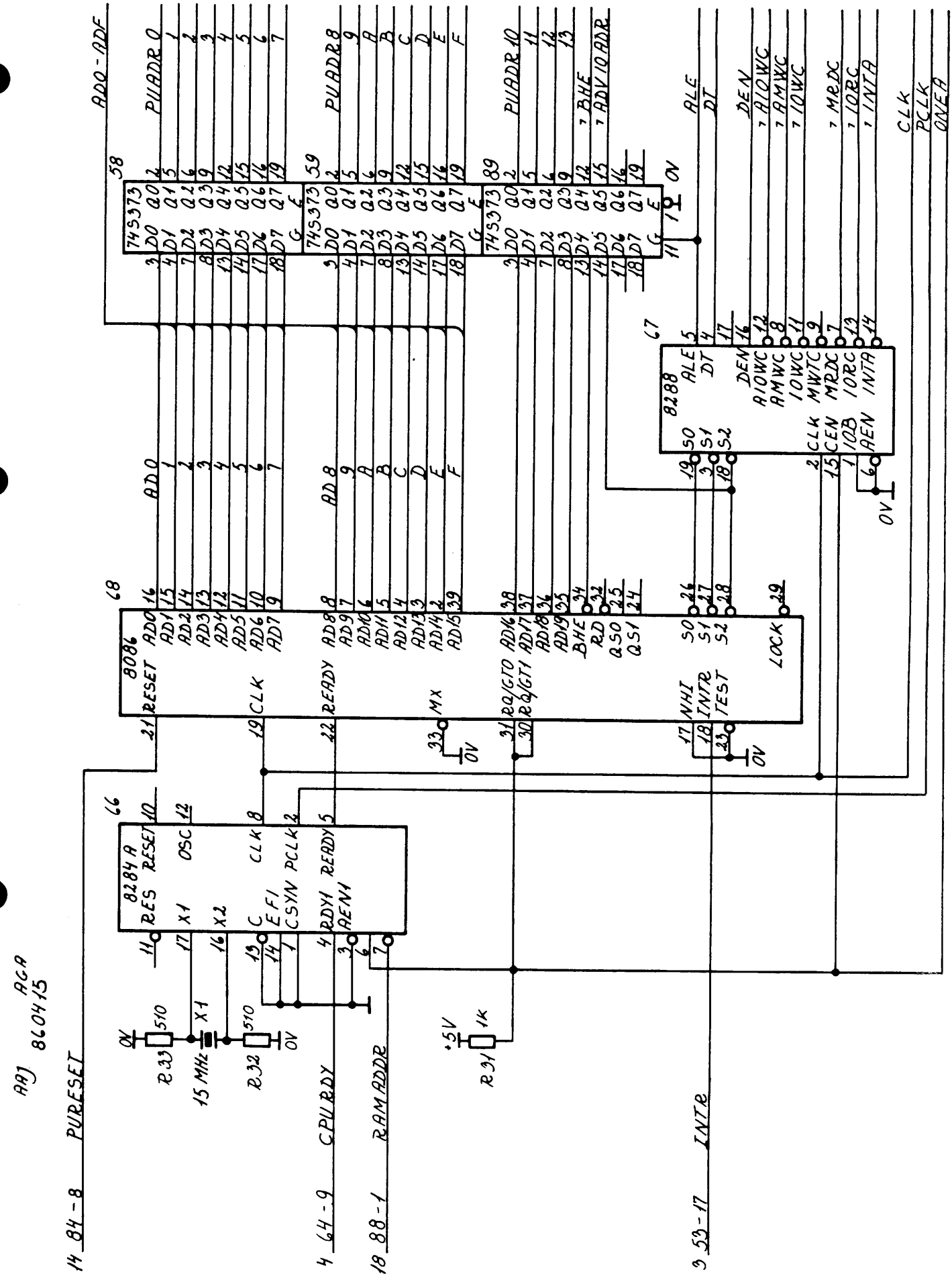


AAJ AGA
811222 830624

IFP 802
R13318

DMA CONTROLLER, STATE TABLE

Signal	Destination	Description
AD(0-F)	1,2,9	Bidirectional, multiplexed address/ data bus from/to 8086 microprocessor. AD0 is the least significant bit.
PUADR0	15	PUADR(0-13) is a 20-bit address bus.
PUADR1	2,3,4,9,18,21	Bits (0-F) are used for both memory
PUADR2	2,3,4,9,18	and I/O addressing. Bits (10-13) are
PUADR(3-7)	2,9,18	the 4 most significant memory address
PUADR(8-D)	2,9	bits.
PUADR(E-F)	9	
PUADR10	9,18	
PUADR(11-13)	18	
-,BHE	15	Bus High Enable. Used in conjunction with PUADR0 for byte control.
-,ADVIOADR	18	Indicates that the address bus contains an I/O address. Generated early in the machine cycle.
ALE	1,4	Strobes the address into the address latches.
DT	2,9	Controls direction of data flow through data bus transceivers.
DEN	18	Controls enabling of data bus transceivers.
-,AIOWC	3,4,21	Advanced I/O write command.
-,AMWC	15,18	Advanced memory write command.
-,IOWC	18	I/O write command
-,MRDC	15,18	Memory read command.
-,IORC	3,4,21	I/O Read command
-,INTA	3	Interrupt acknowledge signal to the interrupt controller.
CLK	1,4	5 MHz clock signal for 8086 processor and support circuits.
PCLK	4	2.5 MHz clock signal used for the interval timer.
ONEA	1,4	Logic one for unused inputs.

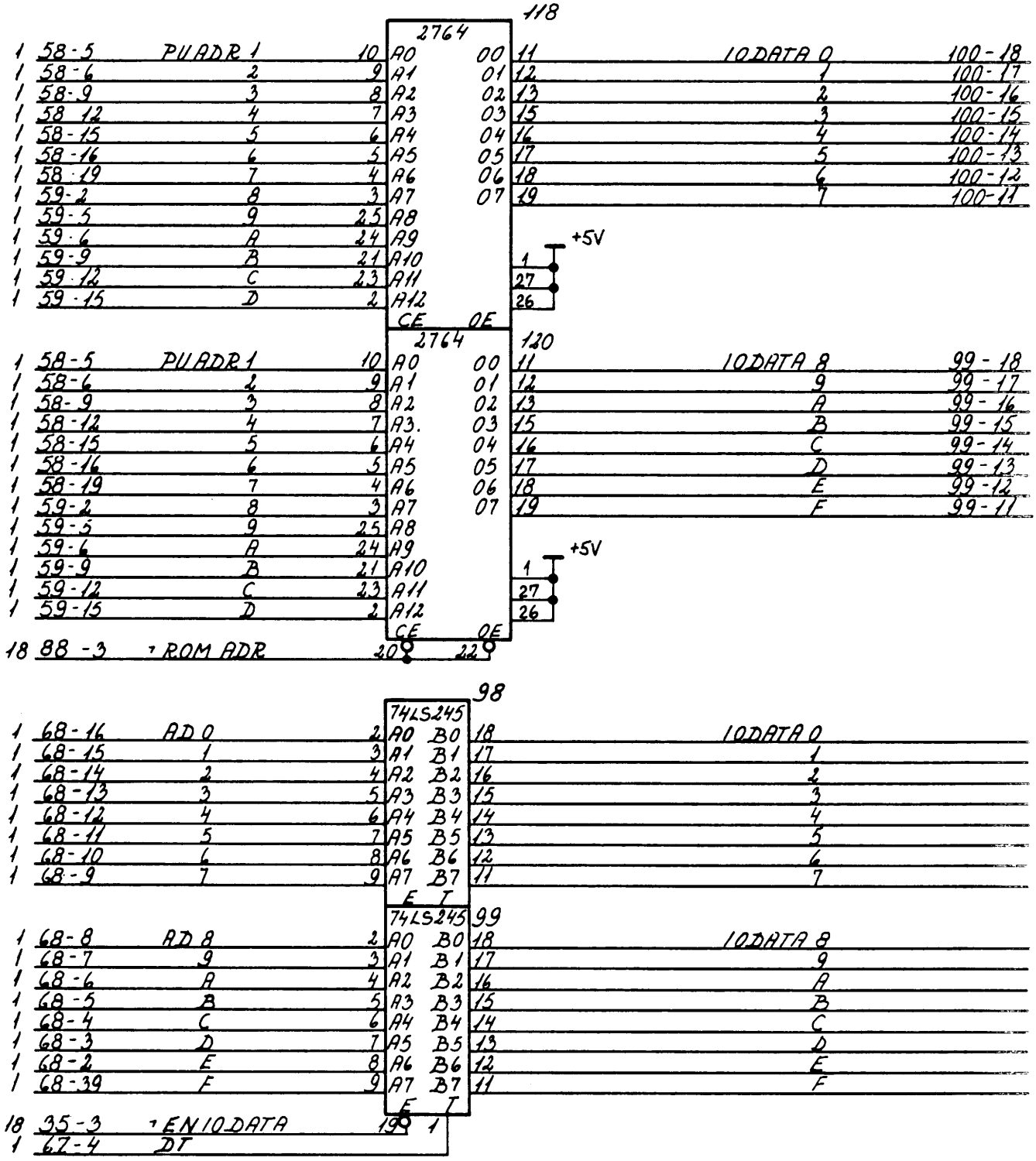


IFP 802
R13914

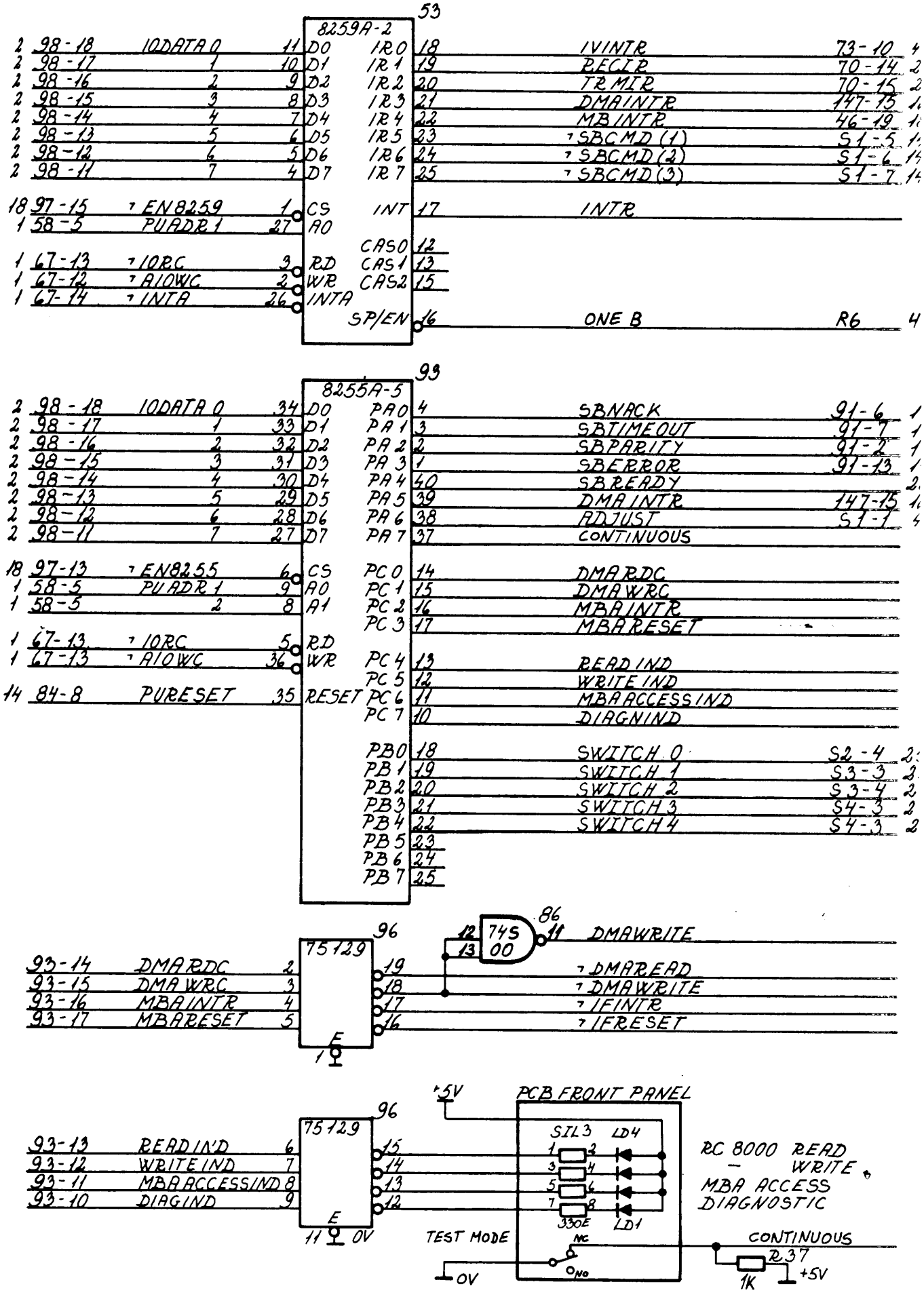
MICROPROCESSOR, CLOCK GENERATOR, COMMAND DECODER, & ADDRESS LATCH

1

Signal	Destination	Description
IODATA0	2,3,4,6,7, 17,21	IODATA(0-F) is a 16-bit
IODATA(1-7)	2,3,4,5,6,7, 17,21	bidirectional data bus, which connects the CPU to EPROM, I/O
IODATA(8-F)	2,5,7	devices and DMA address counters.


118
2764
1 58-5 PUADR 1 10 A0 00 11 IODATA 0 100-18
1 58-6 2 9 A1 01 12 1 100-17
1 58-9 3 8 A2 02 13 2 100-16
1 58-12 4 7 A3 03 15 3 100-15
1 58-15 5 6 A4 04 16 4 100-14
1 58-16 6 5 A5 05 17 5 100-13
1 58-19 7 4 A6 06 18 6 100-12
1 59-2 8 3 A7 07 19 7 100-11
1 59-5 9 25 A8
1 59-6 A 24 A9
1 59-9 B 21 A10
1 59-12 C 23 A11
1 59-15 D 2 A12
CE OE
+5V
1
27
26
120
2764
1 58-5 PUADR 1 10 A0 00 11 IODATA 8 99-18
1 58-6 2 9 A1 01 12 9 99-17
1 58-9 3 8 A2 02 13 A 99-16
1 58-12 4 7 A3. 03 15 B 99-15
1 58-15 5 6 A4 04 16 C 99-14
1 58-16 6 5 A5 05 17 D 99-13
1 58-19 7 4 A6 06 18 E 99-12
1 59-2 8 3 A7 07 19 F 99-11
1 59-5 9 25 A8
1 59-6 A 24 A9
1 59-9 B 21 A10
1 59-12 C 23 A11
1 59-15 D 2 A12
CE OE
+5V
1
27
26
18 88-3 *ROM ADR 20 22
98
74LS245
1 68-16 AD 0 2 A0 B0 18 IODATA 0
1 68-15 1 3 A1 B1 17 1
1 68-14 2 4 A2 B2 16 2
1 68-13 3 5 A3 B3 15 3
1 68-12 4 6 A4 B4 14 4
1 68-11 5 7 A5 B5 13 5
1 68-10 6 8 A6 B6 12 6
1 68-9 7 9 A7 B7 11 7
E T
74LS245 99
1 68-8 AD 8 2 A0 B0 18 IODATA 8
1 68-7 9 3 A1 B1 17 9
1 68-6 A 4 A2 B2 16 A
1 68-5 B 5 A3 B3 15 B
1 68-4 C 6 A4 B4 14 C
1 68-3 D 7 A5 B5 13 D
1 68-2 E 8 A6 B6 12 E
1 68-39 F 9 A7 B7 11 F
E T
18 35-3 *EN IODATA 19 1
1 67-4 DT

Signal	Destination	Description
INTR	1	Interrupt request to CPU from interrupt controller
DMARDC	3	DMA read command. Starts data transfer from RC8000 memory to multi-port RAM.
DMAWRC	3	DMA write command. Starts data transfer from multi-port RAM to RC8000 memory.
MBAINTR	3	Is transferred to the MBA 602, where it generates a Multibus interrupt request.
MBARESET	3	Is transferred to the MBA 602, where it controls the Multibus INIT signal.
READIND WRITEIND MBAACCESSIND DIAGIND	3 3 3 3	Control signals for the indicators on the PCB front panel.
DMAWRITE -,DMAWRITE	8,15,17,25 3,15,16	DMA write command. Controls data transfer from multi-port RAM to RC8000 memory.
-,DMAREAD	16	DMA read command. Controls data transfer from RC8000 memory to multiport RAM.
-,IFINTR	13	Is transferred to the MBA 602, where it generates a Multibus interrupt request.
-,IFRESET	13	Controls the Multibus INIT signal via the MBA 602.
CONTINOUS	3	Control signal from TEST MODE switch on PCB fron panel.

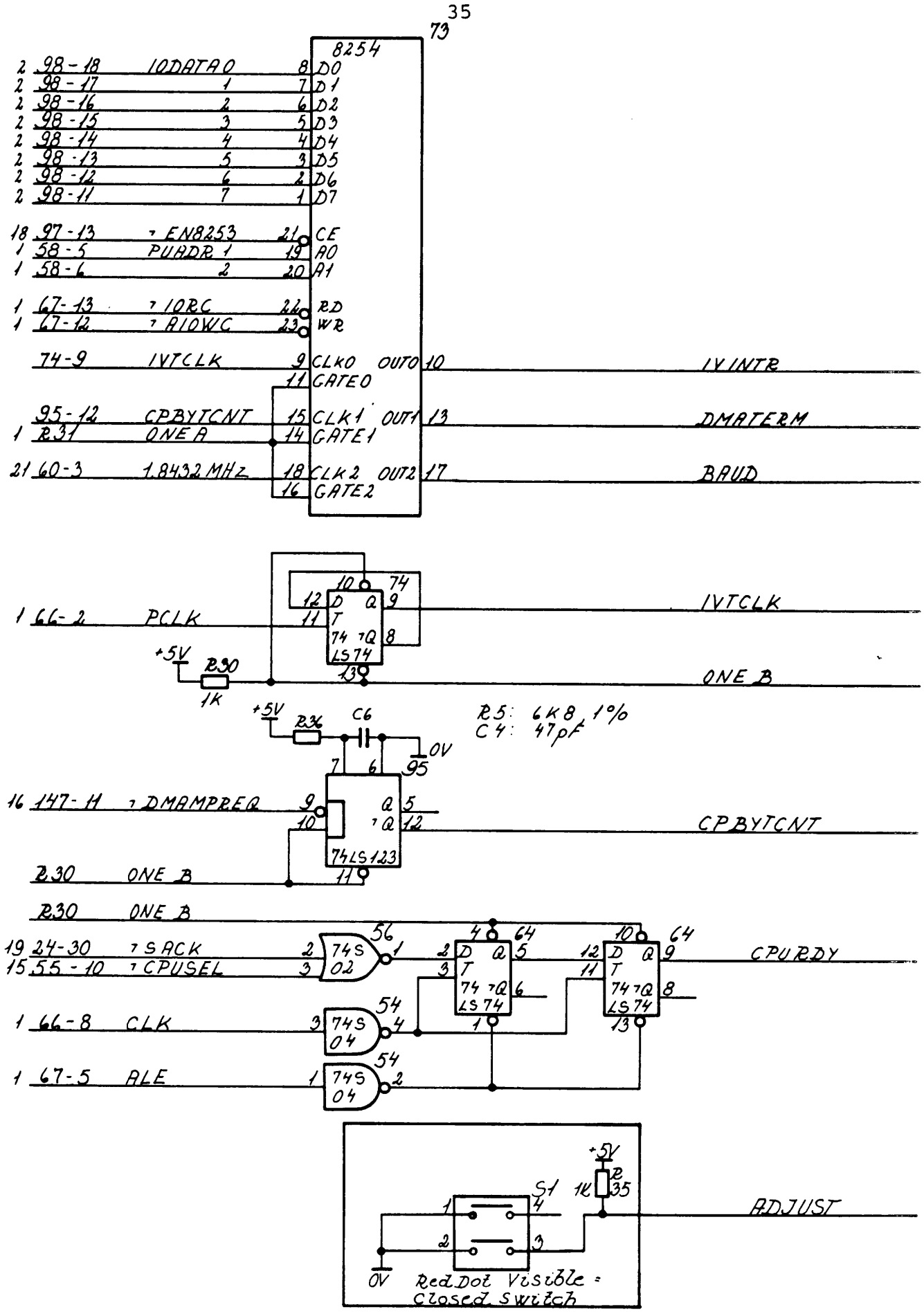


IFP 802

R 13916

. INTERRUPT CONTROLLER
CONTROL SIGNALS TO/FROM DMA, MBA and PCB FRONT PANEL

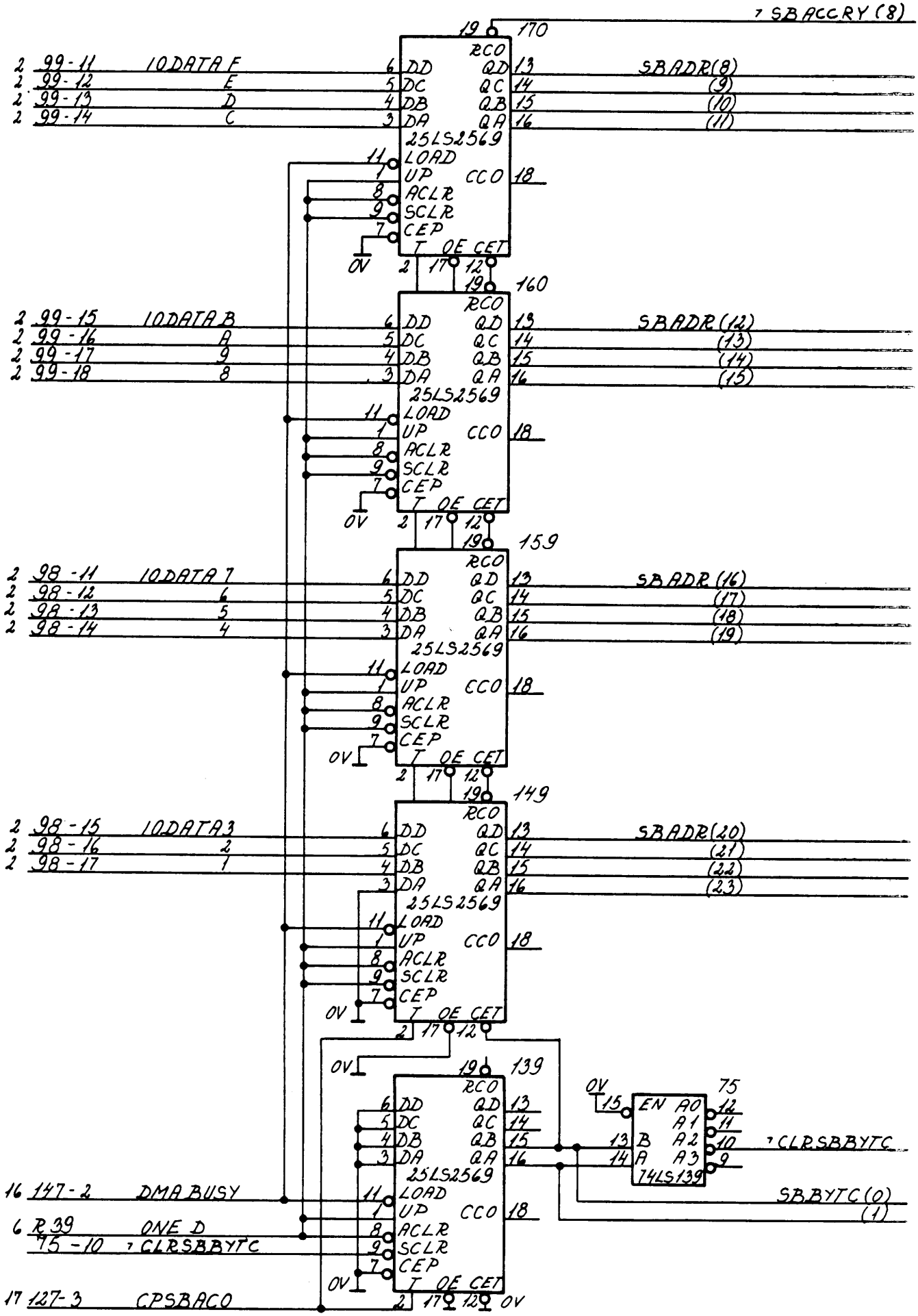
Signal	Destination	Description
IVINTR	3	Interrupt request generated by interval timer.
DMATERM	16	Output from DMA byte counter. Indicates that the DMA has transferred the requested numer of bytes.
BAUD	21	Square wave generator, used as transmit- and receive-clock for USART.
IVTCLK	4	1.25 MHz clock signal for the interval timer.
ONEB	3,4,14,15	Logic one for unused inputs.
CPBYTCNT	4	Clock signal for the DMA byte counter.
CPURDY	1	Ready signal to CPU from RAM controller indicating that it will complete the data transfer.
ADJUST	3	Deskew adjustment possible after reset when switch open.



IFP 802
R 13917

INTERVAL TIMER AND DMA BYTE COUNTER
CPU - RAM ACCESS SYNCHRONIZATION
ADJUST SWITCH

Signal	Destination	Description
-,SBACCRY(8)	6	Carry signal from address counter.
SBADR(8:23)	22	DMA address counter, which controls the RC8000 memory address. SBADR(23) is the least significant bit. The counter is incremented by 2, when a RC8000 word (3 bytes) is transferred.
-,CLRSBBYTC	5	Reset signal for counter, which points at 1 of the 3 bytes in an RC8000 word.
SBBYTC(0)	5,16,17	Counter pointing at 1 of the 3 bytes in the DATAIN or the DATAOUT registers.
SBBYTC(1)	5,17	



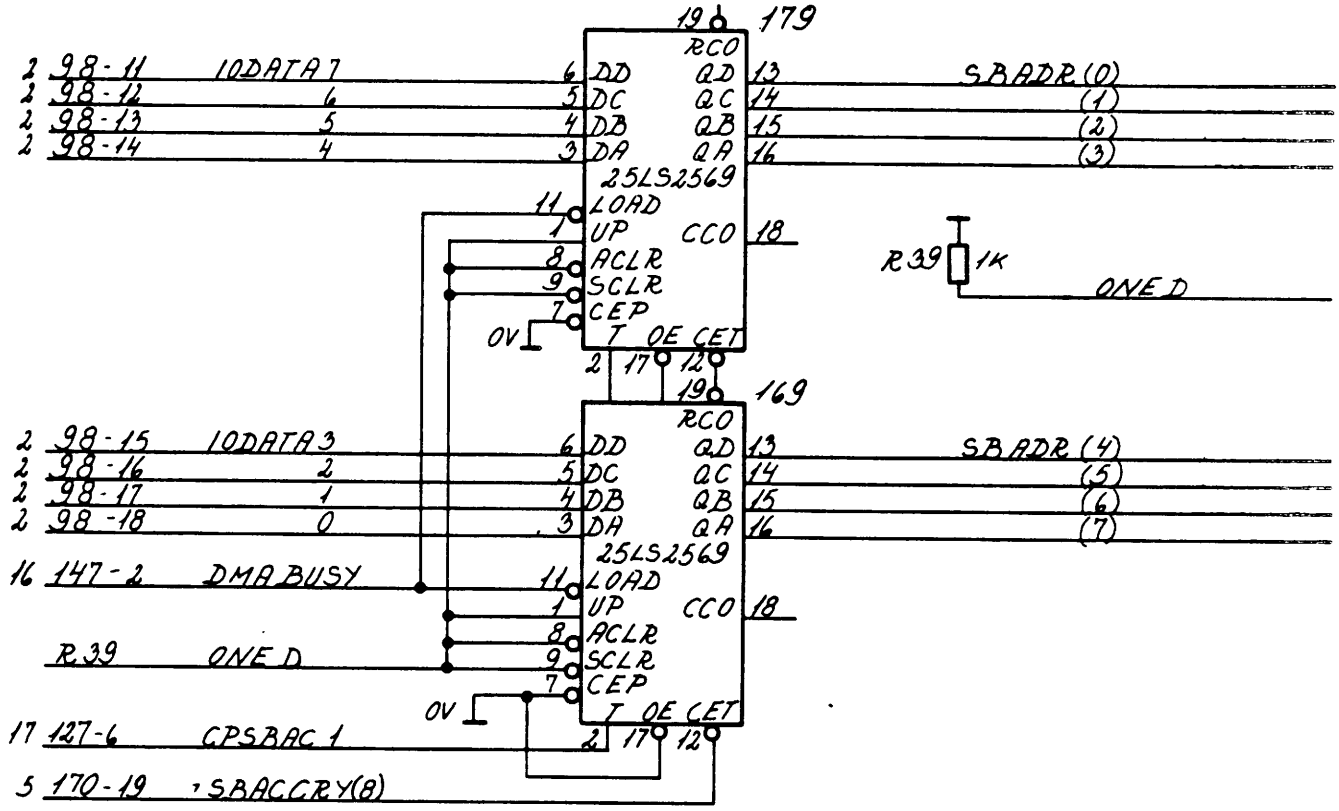
AGA

AAJ

IFP 802 DMA ADDRESS COUNTER FOR RC8000 SYSTEM BUS ADDRESS 5

R 13918

Signal	Destination	Description
SBADR	22	8 most significant bits of DMA address counter, which controls the RC8000 memory address.
ONED	5,6,22,26	Logic one for unused inputs.



AGA

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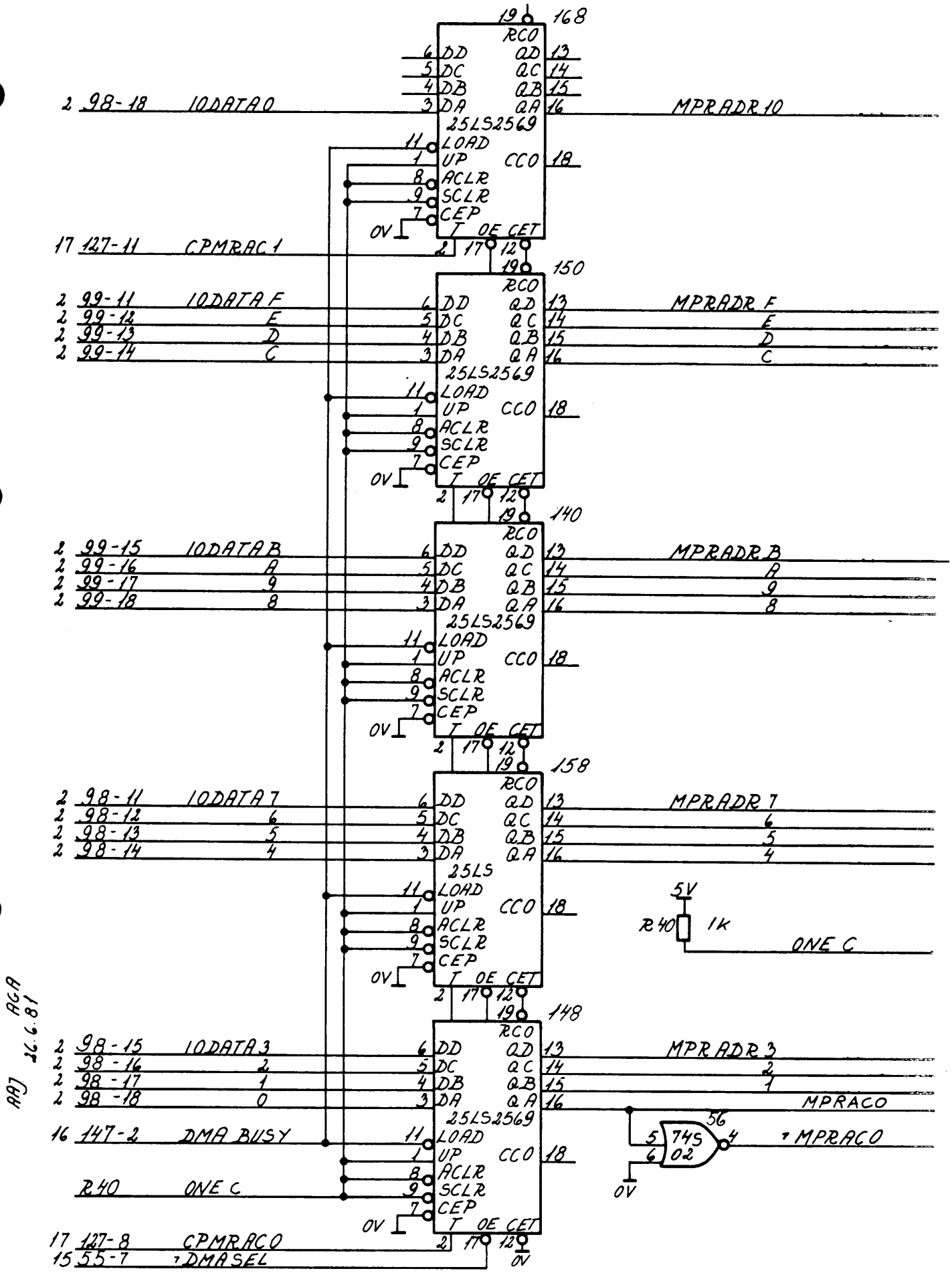
IFP 802 DMA ADDRESS COUNTER FOR RC8000 SYSTEM BUS ADDRESS 6

R 13919

Signal	Destination	Description
MPRADR(1-2)	9,10,19	Output from DMA address counter to multi-port RAM address bus.
MPRADR(3-10)	9,10,18,19	
MPRACO	7,15	Least significant bit of DMA address counter. Used for multi-port RAM byte selection.
-,MPRACO	15	
ONEC	7	Logic one for unused inputs.



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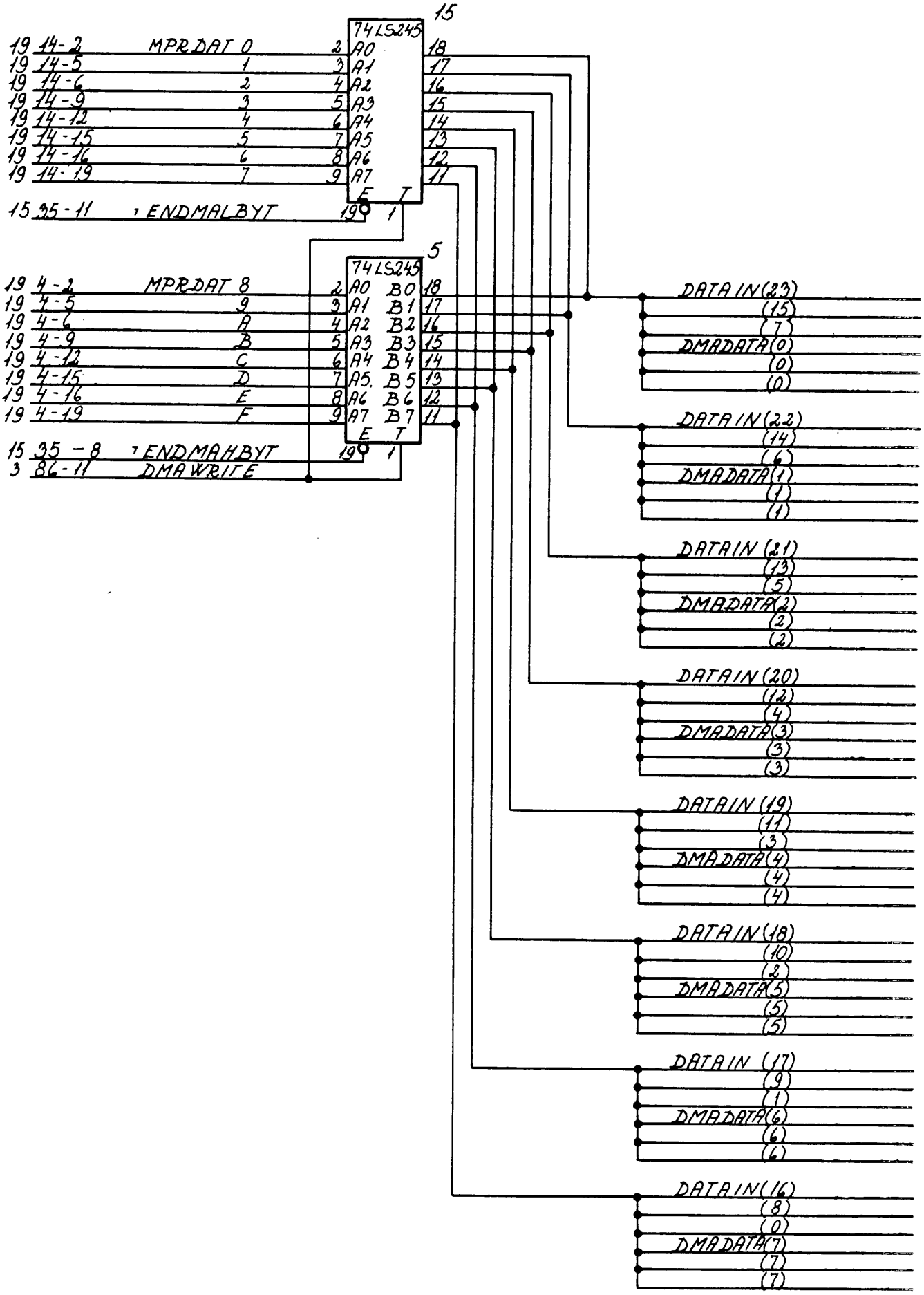
IFP 802 DMA ADDRESS COUNTER FOR MULTI-PORT RAM ADDRESS 7

R 13920

Signal	Destination	Description
DATAIN(0:7)	8,24	8-bit bidirectional data bus, which transfers data between the multi-port RAM data bus and the DATAIN and DATAOUT registers.
DATAIN(8:15)	8,24	
DATAIN(16:23)	8,24	
DMADATA(0:7)	8,23	



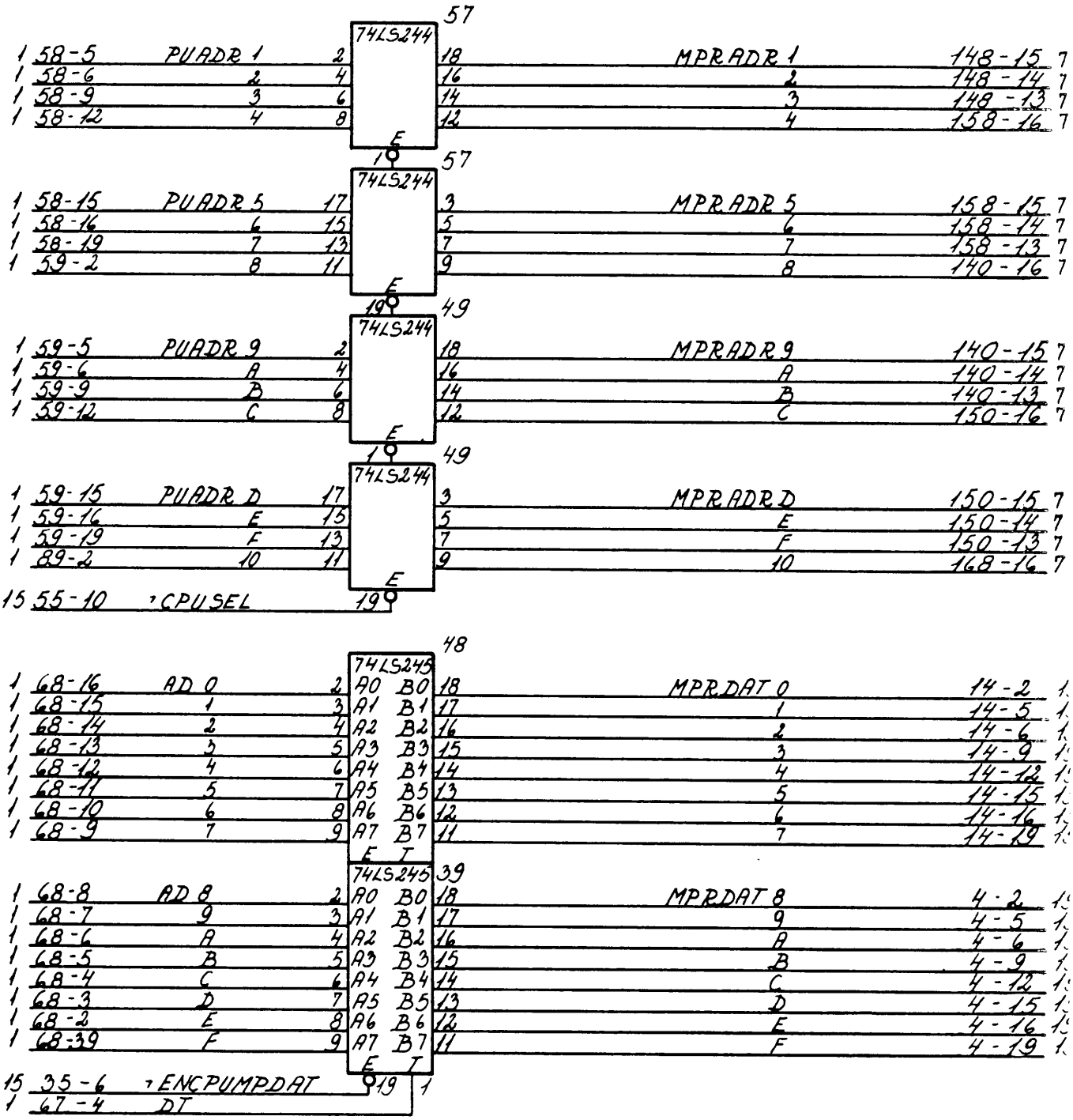
AGA

AAJ

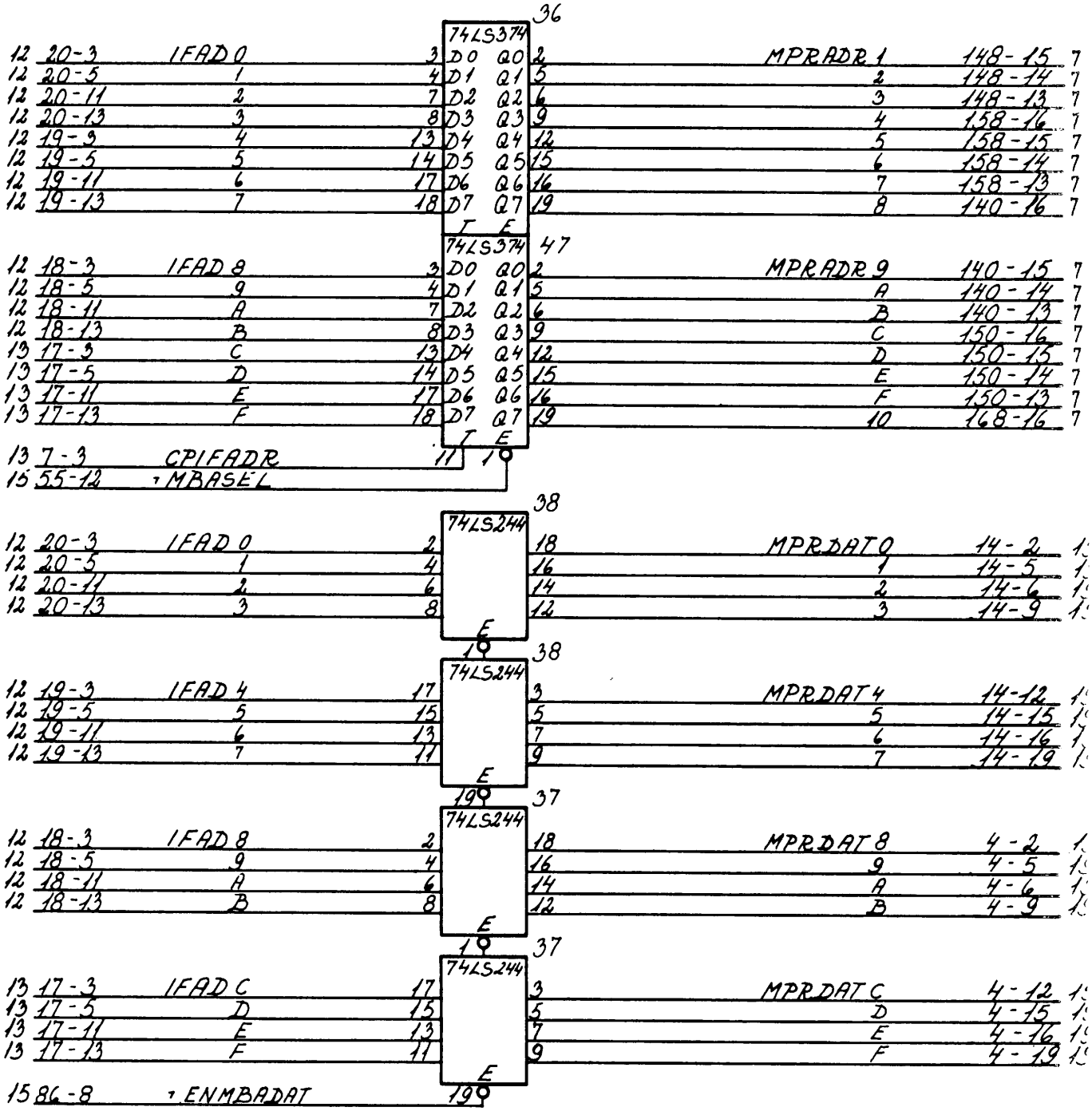
IFP 802 INTERFACE BETWEEN DATAIN, DATAOUT AND MPRDAT BUS 8

R 13921

Signal	Destination	Description
MPRADR(1-2)	7,10,19	Bus drivers for CPU connection to
MPRADR(3-10)	7,10,18,19	multi-port RAM address bus.
MPRDAT(0-B)	8,10,12,19,20	Bus transceivers for CPU connection
MPRDAT(C-F)	8,10,13,19,20	to multi-port RAM data bus.


74LS244
74LS245
PUADR 1
PUADR 5
PUADR 9
PUADR D
AD 0
AD 8
MPRADR 1
MPRADR 5
MPRADR 9
MPRADR D
MPRDAT 0
MPRDAT 8
>CPUSEL
>ENCPUMPDAT
DT
AGA
AAJ

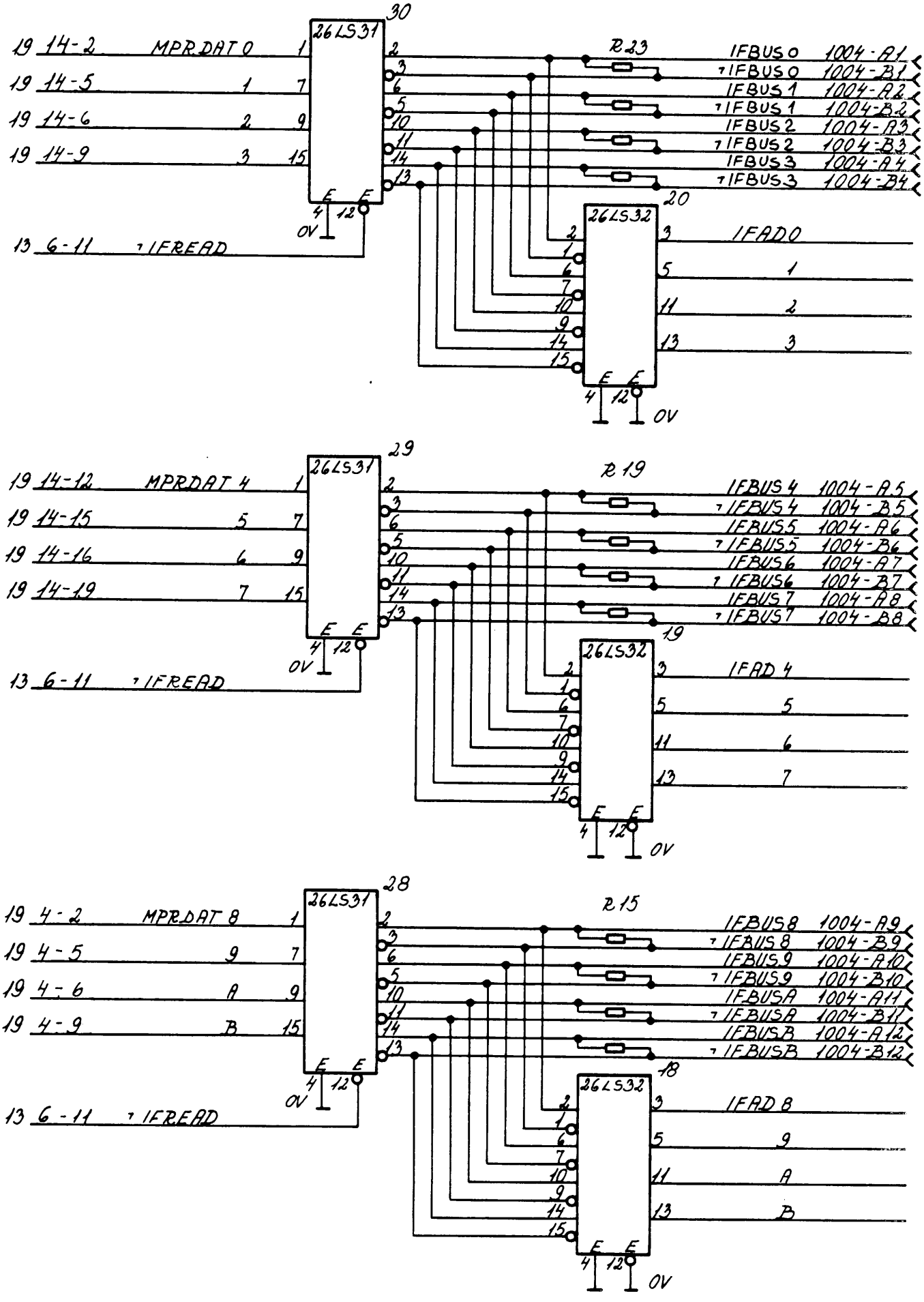
Signal	Destination	Description
MPRADR(1-2)	7,9,19	Input to multi-port RAM address bus
MPRADR(3-10)	7,9,18,19	from MBA interface address register.
MPRDAT(0-B)	8,9,12,19,20	Bus drivers for IFBUS connection to
MPRDAT(C-F)	8,9,13,19,20	multi-port RAM data bus.


36
74LS374
12 20-3 IFAD 0 3 D0 Q0 2 MPRADR 1 148-15 7
12 20-5 1 4 D1 Q1 5 2 148-14 7
12 20-11 2 7 D2 Q2 6 3 148-13 7
12 20-13 3 8 D3 Q3 9 4 158-16 7
12 19-3 4 13 D4 Q4 12 5 158-15 7
12 19-5 5 14 D5 Q5 15 6 158-14 7
12 19-11 6 17 D6 Q6 16 7 158-13 7
12 19-13 7 18 D7 Q7 19 8 140-16 7
T E
74LS374 47
12 18-3 IFAD 8 3 D0 Q0 2 MPRADR 9 140-15 7
12 18-5 9 4 D1 Q1 5 A 140-14 7
12 18-11 A 7 D2 Q2 6 B 140-13 7
12 18-13 B 8 D3 Q3 9 C 150-16 7
13 17-3 C 13 D4 Q4 12 D 150-15 7
13 17-5 D 14 D5 Q5 15 E 150-14 7
13 17-11 E 17 D6 Q6 16 F 150-13 7
13 17-13 F 18 D7 Q7 19 10 168-16 7
T E
13 7-3 CPIFADR 11 1
15 55-12 *MBASEL
38
74LS244
12 20-3 IFAD 0 2 18 MPRDAT 0 14-2 1
12 20-5 1 4 16 1 14-5 1
12 20-11 2 6 14 2 14-6 1
12 20-13 3 8 12 3 14-9 1
E
1
38
74LS244
12 19-3 IFAD 4 17 3 MPRDAT 4 14-12 1
12 19-5 5 15 5 5 14-15 1
12 19-11 6 13 7 6 14-16 1
12 19-13 7 11 9 7 14-19 1
E
19
37
74LS244
12 18-3 IFAD 8 2 18 MPRDAT 8 4-2 1
12 18-5 9 4 16 9 4-5 1
12 18-11 A 6 14 A 4-6 1
12 18-13 B 8 12 B 4-9 1
E
1
37
74LS244
13 17-3 IFAD C 17 3 MPRDAT C 4-12 1
13 17-5 D 15 5 D 4-15 1
13 17-11 E 13 7 E 4-16 1
13 17-13 F 11 9 F 4-19 1
E
15 86-8 *ENMBADAT 19

AG.A

AAJ

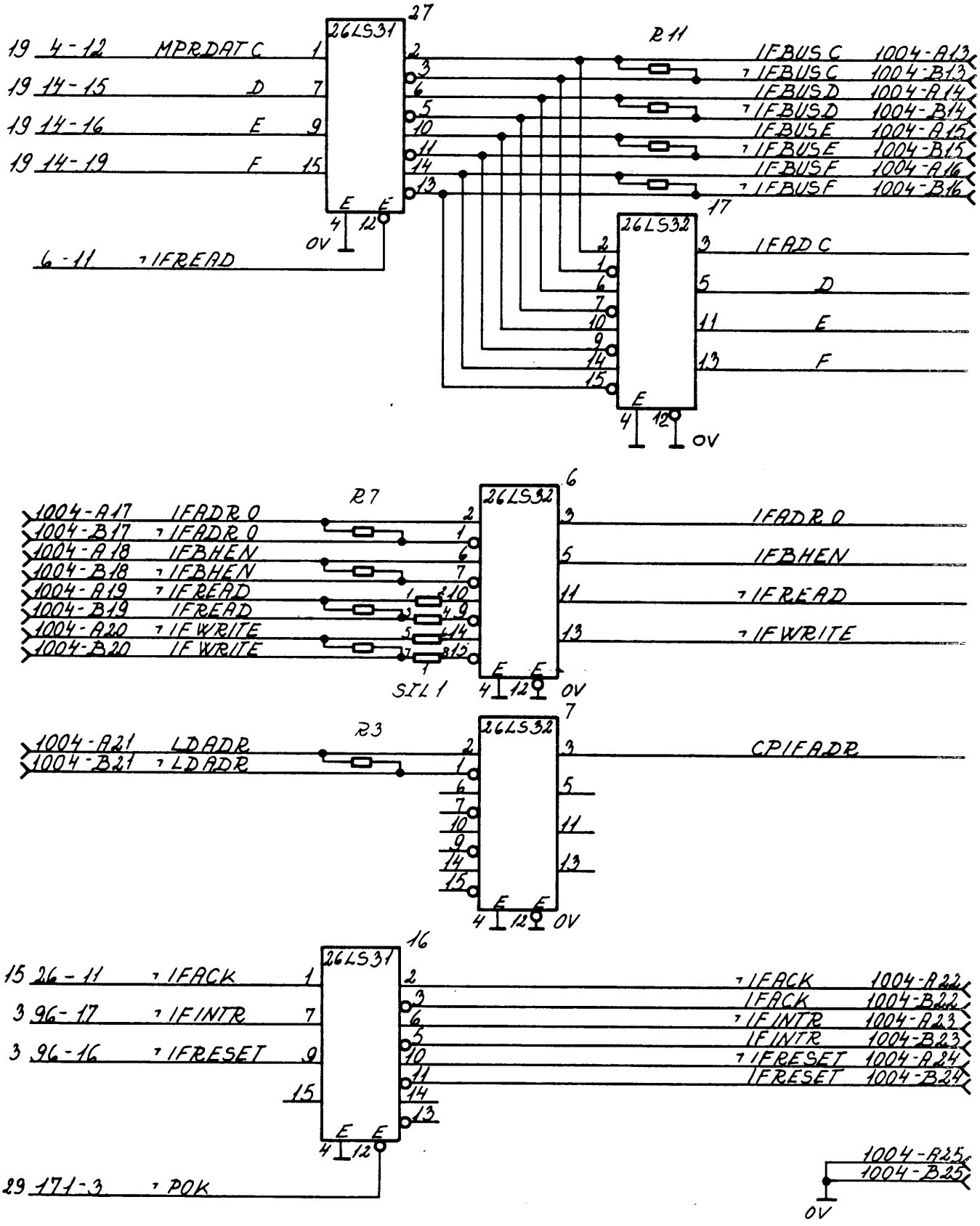
Signal	Destination	Description
IFBUS(0-B) -,IFBUS(0-B)		Bidirectional, multiplexed address/ data tri-state bus, which connectes the IFP 802 and the MBA 602. Differential mode signals.
IFAD (0-B)	10	Multiplexed address and data received from IFBUS.


30
26LS31
19 14-2 MPRDAT 0
19 14-5 1
19 14-6 2
19 14-9 3
13 6-11 ↑IFREAD
OV
R23
IFBUS 0 1004-A1
↑IFBUS 0 1004-B1
IFBUS 1 1004-A2
↑IFBUS 1 1004-B2
IFBUS 2 1004-A3
↑IFBUS 2 1004-B3
IFBUS 3 1004-A4
↑IFBUS 3 1004-B4
20
26LS32
IFAD 0
1
2
3
29
26LS31
19 14-12 MPRDAT 4
19 14-15 5
19 14-16 6
19 14-19 7
13 6-11 ↑IFREAD
OV
R19
IFBUS 4 1004-A5
↑IFBUS 4 1004-B5
IFBUS 5 1004-A6
↑IFBUS 5 1004-B6
IFBUS 6 1004-A7
↑IFBUS 6 1004-B7
IFBUS 7 1004-A8
↑IFBUS 7 1004-B8
19
26LS32
IFAD 4
5
6
7
28
26LS31
19 4-2 MPRDAT 8
19 4-5 9
19 4-6 A
19 4-9 B
13 6-11 ↑IFREAD
OV
R15
IFBUS 8 1004-A9
↑IFBUS 8 1004-B9
IFBUS 9 1004-A10
↑IFBUS 9 1004-B10
IFBUS A 1004-A11
↑IFBUS A 1004-B11
IFBUS B 1004-A12
↑IFBUS B 1004-B12
18
26LS32
IFAD 8
9
A
B

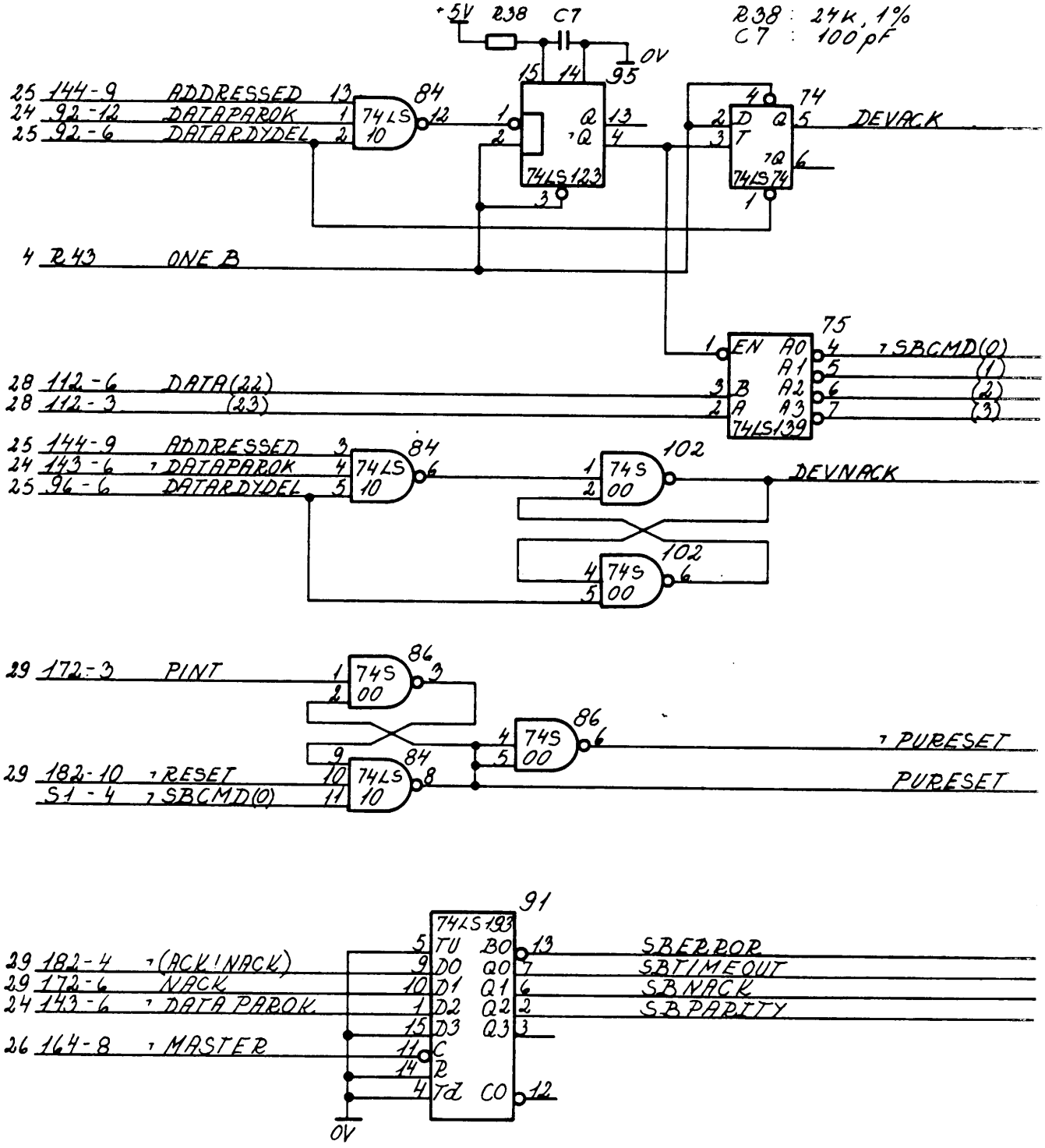
AGA

AAJ

Signal	Destination	Description
IFBUS(C-F) -,IFBUS(C-F)		Bidirectional, multiplexed address/ data tri-state bus, which connects the IFP 802 and the MBA 602. Differential mode signals.
IFAD(C-F)	10	Multiplexed address and data received from IFBUS.
IFADR0	15	Least significant address bit received from the MBA 602.
IFBHEN	15	Byte control signal from MBA 602.
-,IFREAD	12,13,15,17	Memory read command from MBA 602. Is also used to enable IFBUS drivers.
-,IFWRITE	15,17,18	Memory write command from MBA 602.
CPIFADR	10	Clock signal for address register, which holds multi-port RAM address during memory access from MBA.
-,IFACK IFACK		Response to MBA indicating that a memory read or write operation is complete.
-,IFINTR IFINTR		Generates a Multibus interrupt via the MBA 602.
-,IFRESET IFRESET		Controls the -,INIT signal on the Multibus via the MBA 602.


27
26LS31
19 4-12 MPRDATC 1
19 14-15 D 7
19 14-16 E 9
19 14-19 F 15
E E
4 12
0V
6-11 ↑IFREAD
R11
2
3
6
5
10
11
14
13
IFBUSC 1004-A13
↑IFBUSC 1004-B13
IFBUSD 1004-A14
↑IFBUSD 1004-B14
IFBUSE 1004-A15
↑IFBUSE 1004-B15
IFBUSF 1004-A16
↑IFBUSF 1004-B16
17
26LS32
2
1
6
7
10
9
14
15
3 IFADC
5 D
11 E
13 F
E
4 12 0V
6
R7
1004-A17 IFADR0 2
1004-B17 ↑IFADR0 1
1004-A18 IFBHEN 6
1004-B18 ↑IFBHEN 7
1004-A19 ↑IFREAD 10
1004-B19 IFREAD 9
1004-A20 ↑IFWRITE 14
1004-B20 IFWRITE 15
SIL 1
3 IFADR0
5 IFBHEN
11 ↑IFREAD
13 ↑IFWRITE
7
R3
1004-A21 LDADR 2
1004-B21 ↑LDADR 1
3 CPIFADR
16
15 26-11 ↑IFACK 1
3 96-17 ↑IFINTR 7
3 96-16 ↑IFRESET 9
15
↑IFACK 1004-A22
IFACK 1004-B22
↑IFINTR 1004-A23
IFINTR 1004-B23
↑IFRESET 1004-A24
IFRESET 1004-B24
AGA
AAJ
29 171-3 ↑POK
1004-A25
1004-B25
0V

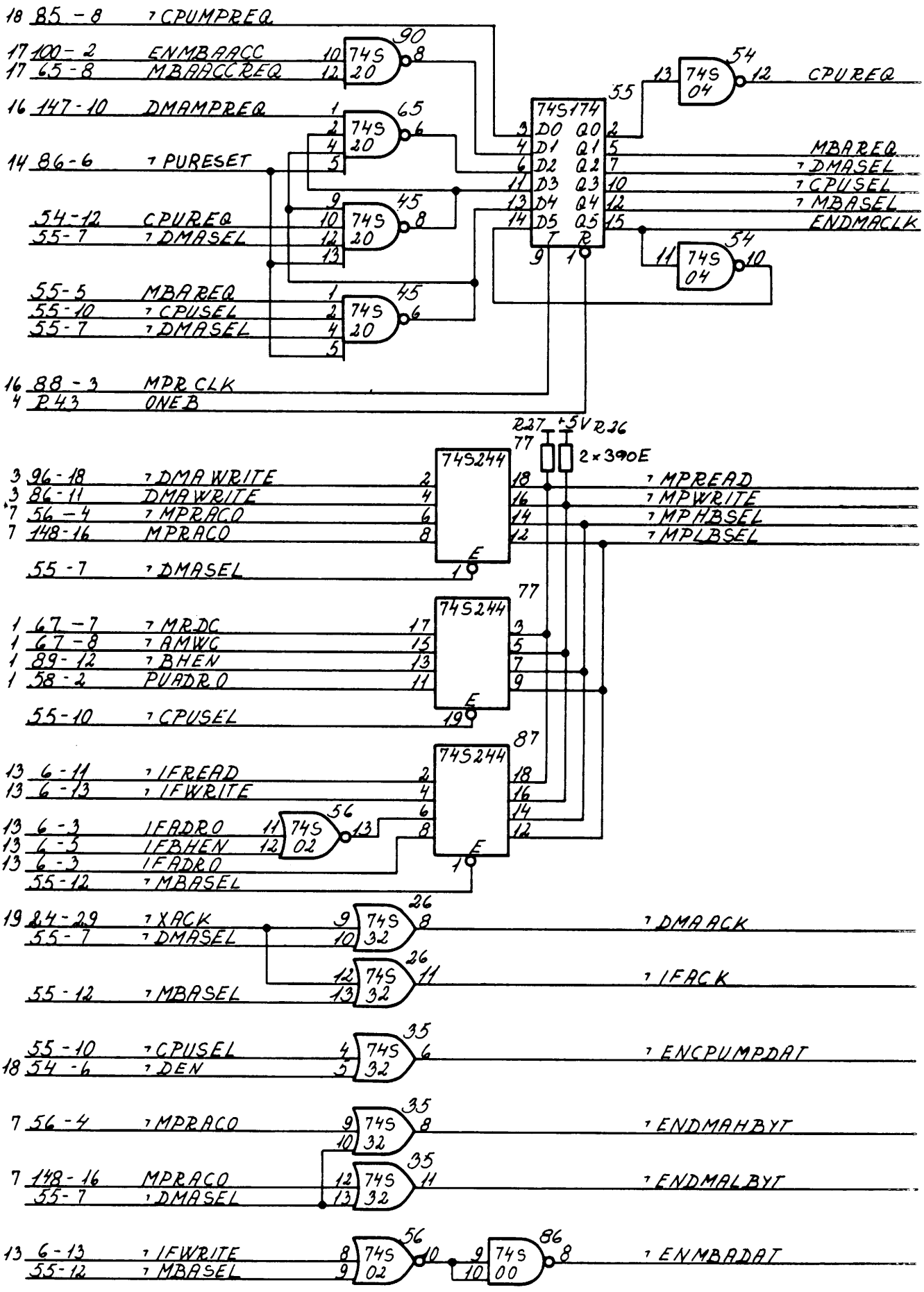
Signal	Destination	Description
DEVACK	29	Acknowledge signal to RC8000 System Bus master, indicating that the IFP has been addressed and received data with correct parity.
-,SBCMD(0)	14	Command received from RC8000 System Bus. Generates a reset signal for the 8086 processor and control logic.
-,SBCMD(1:3)	3	Commands received from RC8000 System Bus. Generate interrupt requests to the 8086 processor.
DEVNACK	29	Response to RC8000 System Bus master, indicating that the IFP has been addressed and received data with parity error.
-,PURESET PURESET	15,16 1,3,14,21	Reset signals for 8086 processor, 8255 I/O port, 8251A USART and DMA control logic. Generated at power-up, by an RC8000 System Reset signal qr by -,SBCMD(0).
SBERROR	3,16	Indicates that an error has occured during an IFP 802 access via the RC8000 System Bus. The following 3 status signals specify the error.
SBTIMEOUT	3	Indicates that the addressed slave unit did not respond within approximately 4 uS.
SBNACK	3	Indicates that the addressed slave unit responded with a NACK (negative acknowledge).
SBPARITY	3	Indicates parity error in the data word received during an RC8000 System Bus read operation.


+5V R38 C7
R38 : 24K, 1%
C7 : 100pF
0V
25 144-9 ADDRESSED
24 92-12 DATAPAROK
25 92-6 DATARDYDEL
84
74LS 10
74LS 123
74
74LS 74
DEVACK
4 R43 ONE B
75
74LS 139
EN A0 A1 A2 A3
B A
¬SBCMD(0)
(1)
(2)
(3)
28 112-6 DATA(22)
28 112-3 (23)
25 144-9 ADDRESSED
24 143-6 ¬DATAPAROK
25 96-6 DATARDYDEL
102
74S 00
DEVNACK
29 172-3 PINT
86
29 182-10 ¬RESET
S1-4 ¬SBCMD(0)
¬PURESET
PURESET
91
74LS 193
TU D0 D1 D2 D3 C P Rd
BO QO Q1 Q2 Q3 CO
29 182-4 ¬(ACK!NACK)
29 172-6 NACK
24 143-6 ¬DATAPAROK
26 164-8 ¬MASTER
SBERROR
SBTIMEOUT
SBNACK
SBPARITY
0V

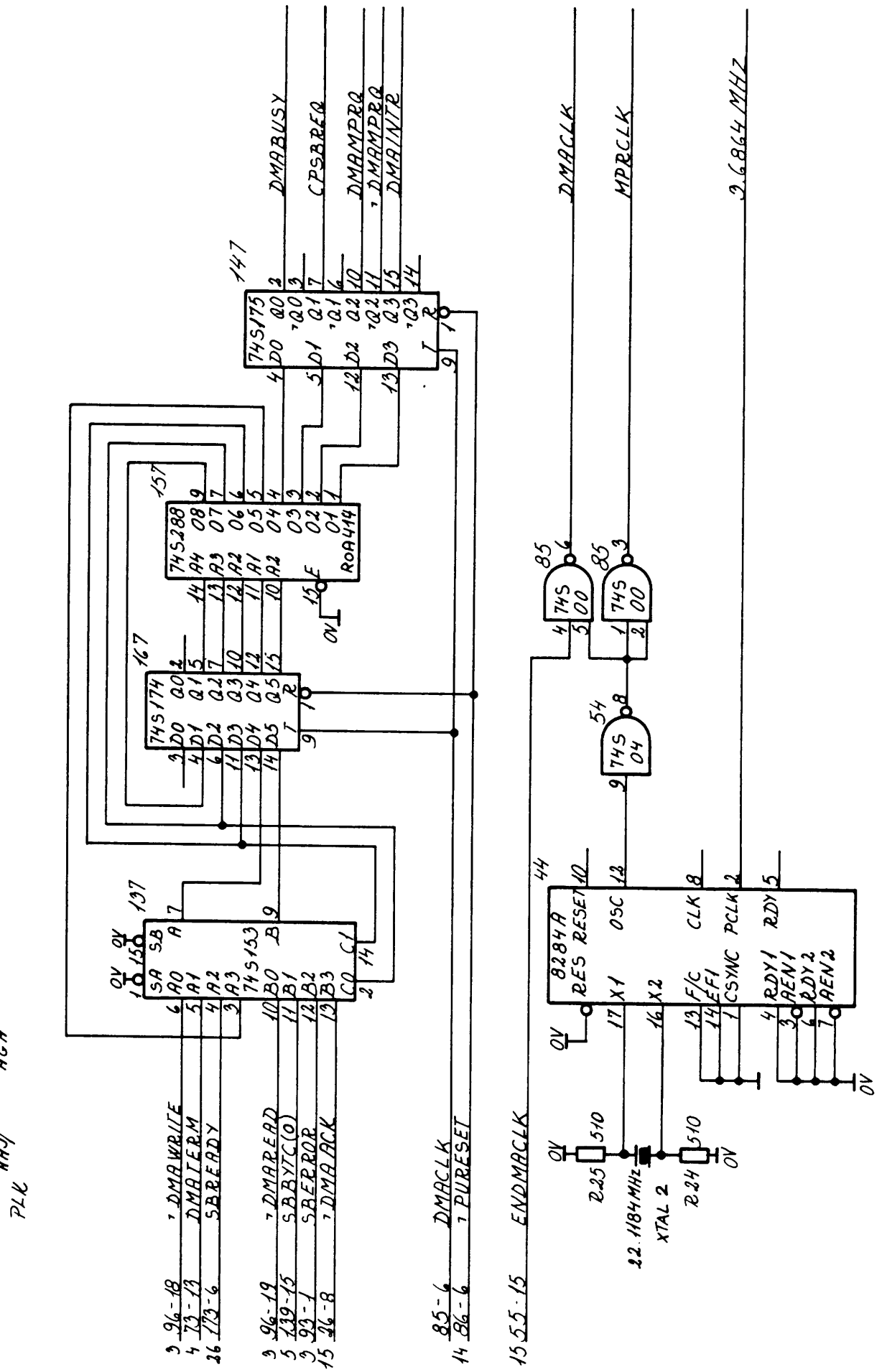
AGA

AAJ

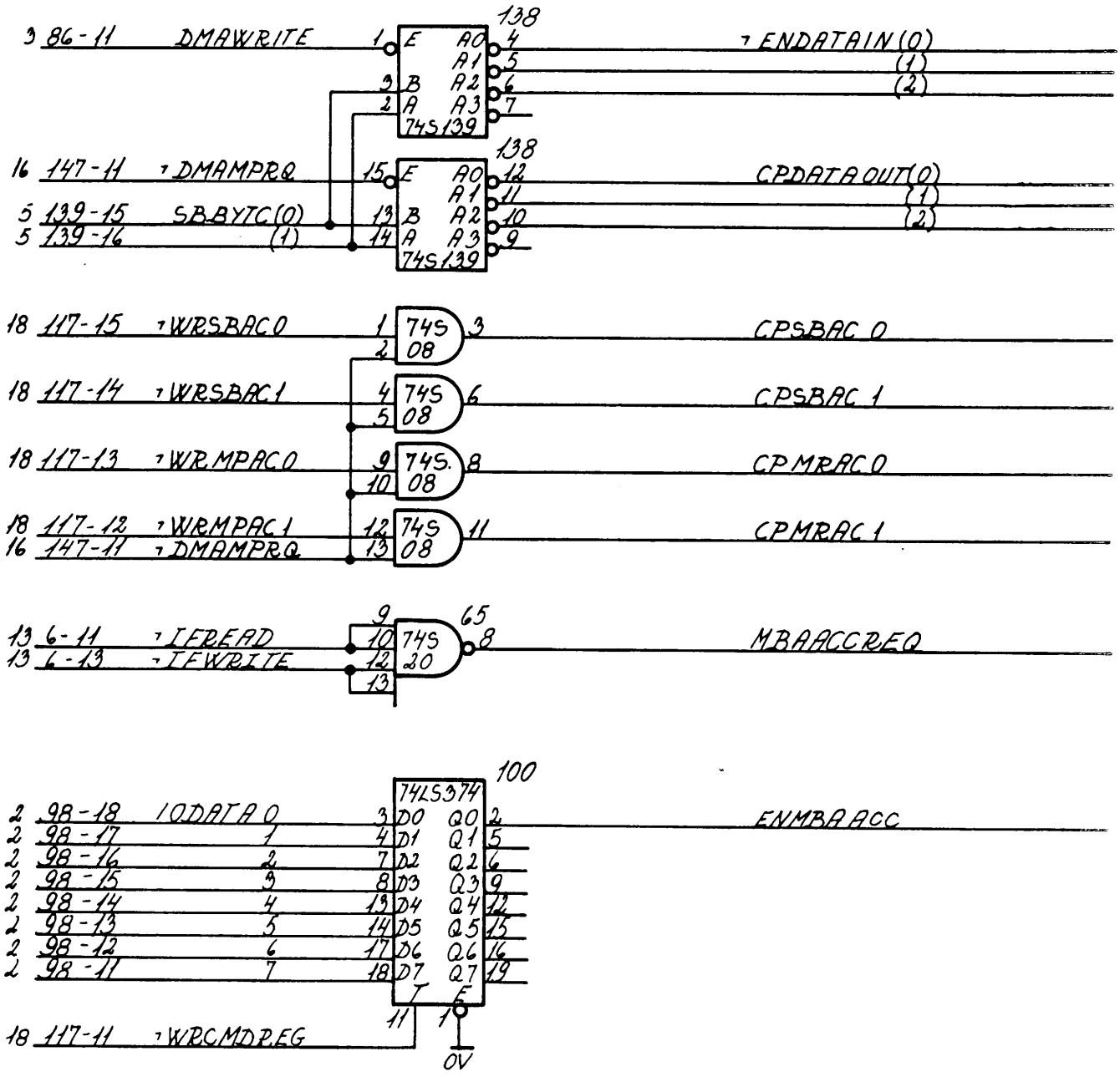
Signal	Destination	Description
CPUREQ	15	Synchronized multi-port RAM access request from 8086 processor.
MBAREQ	15	Synchronized multi-port RAM access request from MBA interface.
-,DMASEL -,CPUSEL	7,15 4,9,15	Selection signals from arbitration logic for multiport RAM access.
-,MBASEL	10,15	Enables address, data and control signals to RAM from DMA, CPU and MBA.
ENDMACLK	15,16	Used to generate 22.1184/2 MHz clock for DMA control logic.
-,MPREAD	19	Read command to RAM controller and enable signal for RAM output register.
-,MPWRITE	19	Write command to RAM controller.
-,MPHBSEL	19	Controls write access to the high byte (bits 8-F) of the RAM.
-,MPLBSEL	19	Controls write access to the low byte (bits 0-7) of the RAM.
-,DMAACK	16	Acknowledge signal from RAM controller to DMA control logic.
-,IFACK	13,18	Acknowledge signal from RAM controller to MBA interface.
-,ENCPUMPDAT	9	Enable signal to CPU data transceivers for data to/from multi-port RAM data bus.
-,ENDMAHBYT -,ENDMALBYT	8 8	Control byte transfer between multi-port RAM data bus and DATAIN/DATAOUT registers for RC8000 System Bus data.
-,ENMBADAT	10	Enables data to multi-port RAM data bus from IFBUS.


18 85-8 ↑CPUMPREQ
17 100-2 ENMBAACC
17 65-8 MBAACCREQ
74S 20
90
16 147-10 DMAMPREQ
65
14 86-6 ↑PURESET
54-12 CPUREQ
55-7 ↑DMASEL
45
55-5 MBAREQ
55-10 ↑CPUSEL
55-7 ↑DMASEL
16 88-3 MPR CLK
4 R43 ONEB
74S174
D0 Q0
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
74S 04
54
55
CPUREQ
MBAREQ
↑DMASEL
↑CPUSEL
↑MBASEL
ENDMACLK
R27 +5V R26
2×390E
77
74S244
3 96-18 ↑DMA WRITE
3 86-11 DMAWRITE
7 56-4 ↑MPRACO
7 148-16 MPRACO
55-7 ↑DMASEL
↑MPREAD
↑MPWRITE
↑MPHBSEL
↑MPLBSEL
1 67-7 ↑MRDC
1 67-8 ↑AMWC
1 89-12 ↑BHEN
1 58-2 PUADR0
55-10 ↑CPUSEL
87
13 6-11 ↑IFREAD
13 6-13 ↑IFWRITE
13 6-3 IFADR0
13 6-5 IFBHEN
13 6-3 IFADR0
55-12 ↑MBASEL
74S 02
56
19 84-29 ↑XACK
55-7 ↑DMASEL
55-12 ↑MBASEL
74S 32
26
↑DMAACK
↑IFACK
55-10 ↑CPUSEL
18 54-6 ↑DEN
35
↑ENCPUMPDAT
7 56-4 ↑MPRACO
↑ENDMAHBYT
7 148-16 MPRACO
55-7 ↑DMASEL
↑ENDMALBYT
13 6-13 ↑IFWRITE
55-12 ↑MBASEL
74S 00
86
↑ENMBADAT
AGA
AAJ

Signal	Destination	Description
DMABUSY	5,6,7	Indicates that the DMA controller is executing a command.
CPSBREQ	26	Prepares a data transfer via the RC8000 System Bus by generating a bus master request.
DMAMPRQ	15	Access request to multi-port RAM arbitration logic from DMA control logic, Increments DMA address counters and DMA byte counter. Loads DATAOUT register in DMA write operations.
-,DMAMPRQ	4,17	
DMAINTR	3	Interrupt request to 8086 processor indicating that the DMA controller has finished an operation.
DMACLK	16	11.0592 MHz clock signal for DMA control logic.
MPRCLK	15,19	22.1184 MHz clock signal for RAM controller and multi-port RAM arbitration logic.
3.6864MHz	21	3.6864 MHz clock signal for USART timing.


DMA CONTROL LOGIC
IFP 802
R 13928
PLK AAJ AGA
74S175
74S288
74S174
74S153
8284A
74S00
74S04
DMABUSY
CPSBREQ
DMAMPRQ
DMAINT2
DMACLK
MPRCLK
3.6864 MHZ
DMAWRITE
DMATERM
SBREADY
DMAREAD
SBBYTC(0)
SBERROR
DMAACK
ENDMACLK
DMACLK
PURESET
12.1184MHz
XTAL 2
R25
R24
510

Signal	Destination	Description
-,ENDATAIN(0) -,ENDATAIN(1) -,endatain(2)	24 24 24	Transfer contents of respectively DATAIN(0:7), DATAIN(8:15) and DATAIN(16:23) to the 8-bit data bus, which is connected to the multi-port RAM data bus.
CPDATAOUT(0) CPDATAOUT(1) CPDATAOUT(2)	23 23 23	Load respectively DATAOUT(0:7), DATAOUT(8:15) and DATAOUT(16:23) with data from multi-port RAM.
CPSBAC0 CPSBAC1	5 6	Clock signals for DMA address counter, which generates RC8000 System Bus address. CPSBAC0 clocks bits (8:23) and CPSBAC1 clocks bits (0:7). When DMABUSY=0 the counter is loaded with data from IODAT bus, and when DMABUSY=1 the counter is incremented.
CPMRAC0 CPMRAC1	7 7	Clock signals for DMA address counter, which generates multi-port RAM address. CPMRAC0 clocks bits (0-F), and CPMRAC1 clocks bit 10. When DMABUSY=0 the counter is loaded with data from IODATA bus, and when DMABUSY=1 the counter is incremented.
MBAACCREQ	15	Memory read or write access request from MBA602.
ENMBAACC	15	Enabling of memory access for MBA602.

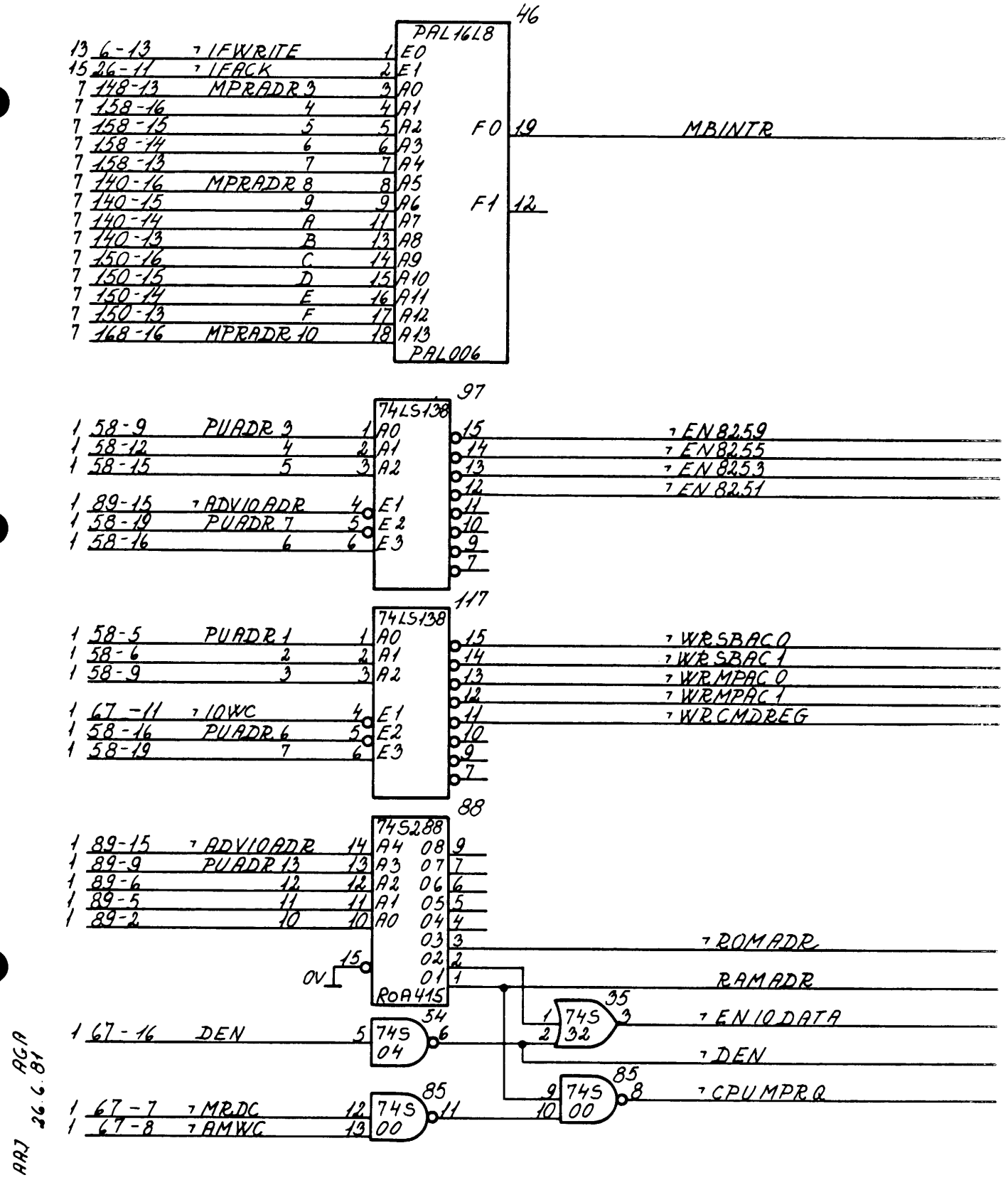

138
3 86-11 DMAWRITE
1 E
2 A
3 B
74S139
A0 4
A1 5
A2 6
A3 7
→ENDATAIN(0)
(1)
(2)
138
16 147-11 →DMAMPRQ
5 139-15 SBBYTC(0)
5 139-16 (1)
15 E
13 B
14 A
74S139
A0 12
A1 11
A2 10
A3 9
CPDATAOUT(0)
(1)
(2)
18 117-15 →WRSBAC0
74S 08
CPSBAC 0
18 117-14 →WRSBAC1
74S 08
CPSBAC 1
18 117-13 →WRMPAC0
74S 08
CPMRAC 0
18 117-12 →WRMPAC1
16 147-11 →DMAMPRQ
74S 08
CPMRAC 1
13 6-11 →IEREAD
13 6-13 →IEWRITE
74S 20
65
MBAACCREQ
100
74LS374
2 98-18 IODATA 0
2 98-17 1
2 98-16 2
2 98-15 3
2 98-14 4
2 98-13 5
2 98-12 6
2 98-11 7
D0 Q0
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
D7 Q7
T
E
11
1
0V
18 117-11 →WRCMDREG
ENMBAACC

AGA

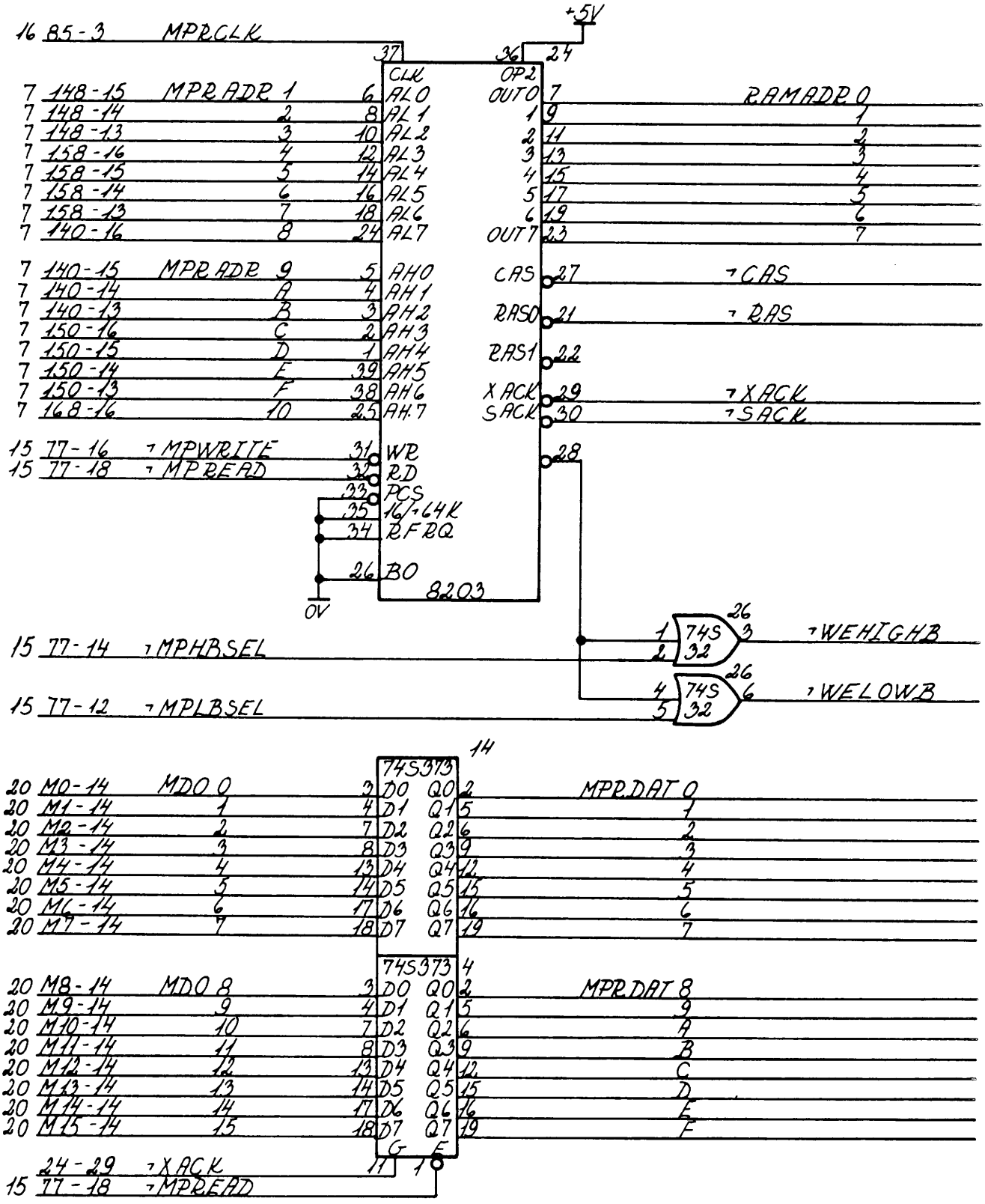
ARX

PLK

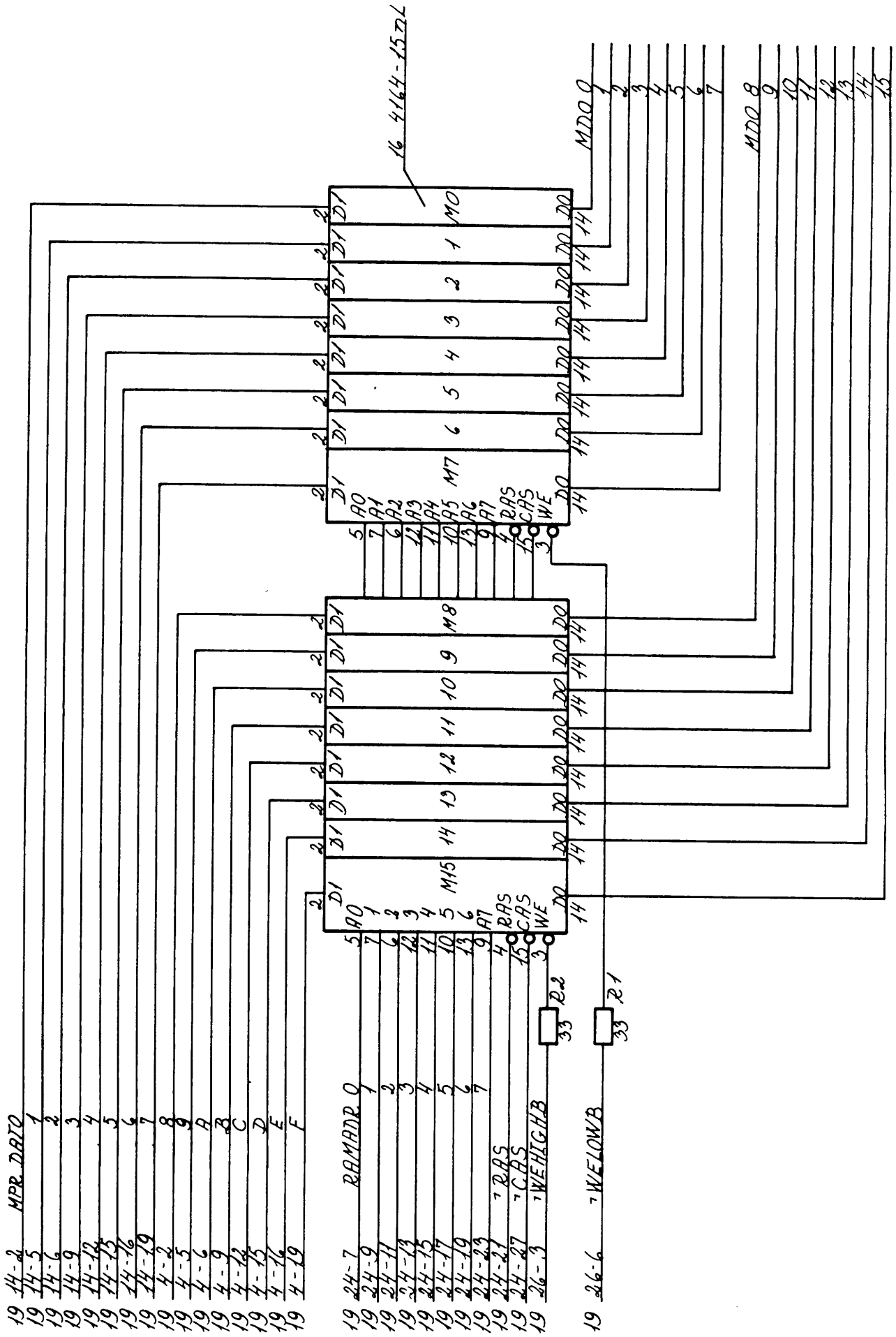
Signal	Destination	Description
MBINTR	3	Interrupt request to 8086 processor. Generated at MBA write access to multi-port RAM locations: 4000-4007 hex.
-,EN8259	3	Enable signal for the 8259A interrupt controller.
-,EN8255	3	Enable signal for the 8255A peripheral interface.
-,EN8254	4	Enable signal for the 8254 interval timer.
-,EN8251	21	Enable signal for the 8251A communication interface.
-,WRSBAC0	17	Write strobe for DMA address counter, which generates RC8000 System Bus address bits 8-23.
-,WRSBAC1	17	Write strobe for DMA address counter, which generates RC8000 System Bus address bits 0-7.
-,WRMPAC1	17	Write strobe for DMA address counter, which generates multi-port RAM address bit 10.
-,ROMADR	2	Enable signal for EPROM memory.
RAMADR	1,18	Indicates that the address on the PUADR address bus is within the RAM address space.
-,ENIODATA	2	Enables IODATA bus transceivers.
-,DEN	15,18	Controls enabling of bus tranceivers between CPU and multi-port RAM data bus.
-,CPUMPRQ	15	Access request to multi-port RAM from 8086 processor.
-,WRCMDREG	17	Write command for the MBA access register


46
PAL16L8
13 6-13 ¬IFWRITE 1 I0
15 26-11 ¬IFACK 2 I1
7 148-13 MPRADR 3 3 A0
7 158-16 4 4 A1
7 158-15 5 5 A2
7 158-14 6 6 A3
7 158-13 7 7 A4
7 140-16 MPRADR 8 8 A5
7 140-15 9 9 A6
7 140-14 A 11 A7
7 140-13 B 13 A8
7 150-16 C 14 A9
7 150-15 D 15 A10
7 150-14 E 16 A11
7 150-13 F 17 A12
7 168-16 MPRADR 10 18 A13
PAL006
F0 19 MBINTR
F1 12
97
74LS138
1 58-9 PUADR 3 1 A0
1 58-12 4 2 A1
1 58-15 5 3 A2
1 89-15 ¬ADVIOADR 4 E1
1 58-19 PUADR 7 5 E2
1 58-16 6 6 E3
15 ¬EN8259
14 ¬EN8255
13 ¬EN8253
12 ¬EN8251
11
10
9
7
117
74LS138
1 58-5 PUADR 1 1 A0
1 58-6 2 2 A1
1 58-9 3 3 A2
1 67-11 ¬IOWC 4 E1
1 58-16 PUADR 6 5 E2
1 58-19 7 6 E3
15 ¬WRSBAC0
14 ¬WRSBAC1
13 ¬WRMPAC0
12 ¬WRMPAC1
11 ¬WRCMDREG
10
9
7
88
74S288
1 89-15 ¬ADVIOADR 14 A4 O8 9
1 89-9 PUADR 13 13 A3 O7 7
1 89-6 12 12 A2 O6 6
1 89-5 11 11 A1 O5 5
1 89-2 10 10 A0 O4 4
O3 3 ¬ROMADR
15 0V O2 2
O1 1 RAMADR
ROM415
54
1 67-16 DEN 5 74S 04 6
35
1 74S 32 3 ¬EN IODATA
2 ¬DEN
85
1 67-7 ¬MRDC 12 74S 00 11
1 67-8 ¬AMWC 13
85
9 74S 00 8 ¬CPUMPRQ
10
AAJ AGA 26.6.81

Signal	Destination	Description
RAMADR(0-7)	20	Address lines to dynamic RAM array.
-,CAS	20	Column address strobe for dynamic RAM array.
-,RAS	20	Row address strobe for dynamic RAM array.
-,XACK	15,19	Transfer acknowledge. Indicates valid data during a read cycle or data written during a write cycle.
-,SACK	4	System acknowledge. Indicates the beginning of a memory access cycle.
-,WEHIGHB	20	Write strobe for dynamic RAM array bits 8-15.
-,WELOWB	20	Write strobe for dynamic RAM array bits 0-7.
MPRDAT(0-B) MPRDAT(C-F)	8,9,10,12,20 8,9,10,13,20	Data from RAM output register to the multi-port RAM data bus.

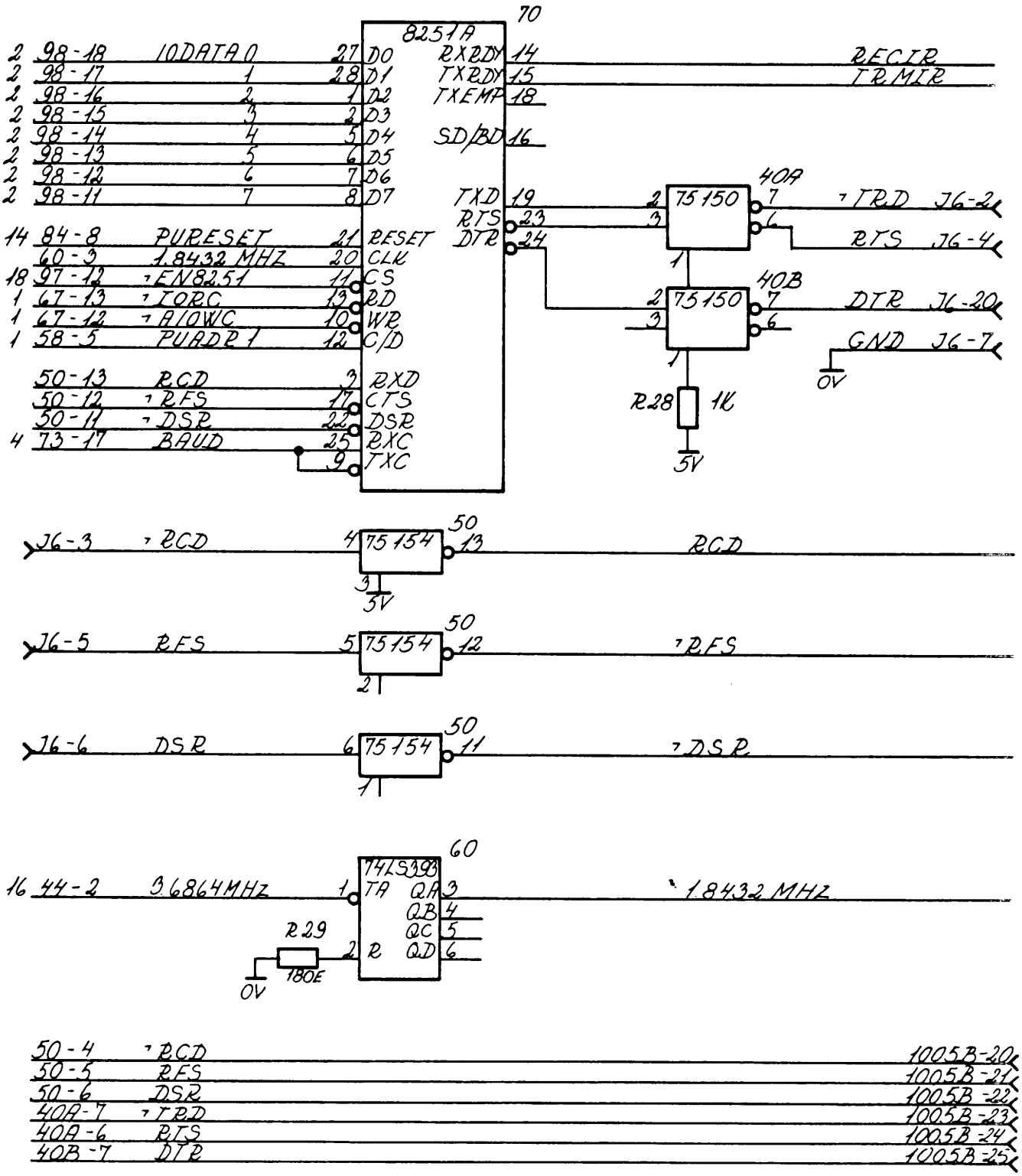

+5V
16 85-3 MPRCLK
CLK
OP2
AL0
AL1
AL2
AL3
AL4
AL5
AL6
AL7
OUT0
OUT7
7 148-15 MPRADR 1
7 148-14
7 148-13
7 158-16
7 158-15
7 158-14
7 158-13
7 140-16
RAMADR 0
7 140-15 MPRADR 9
7 140-14
7 140-13
7 150-16
7 150-15
7 150-14
7 150-13
7 168-16
AH0
AH1
AH2
AH3
AH4
AH5
AH6
AH.7
CAS
RAS0
RAS1
XACK
SACK
→CAS
→RAS
→XACK
→SACK
15 77-16 →MPWRITE
15 77-18 →MPREAD
WR
RD
PCS
16/64K
RFRQ
BO
8203
0V
15 77-14 →MPHBSEL
15 77-12 →MPLBSEL
74S32
→WEHIGHB
→WELOWB
14
74S373
20 M0-14 MDO 0
20 M1-14
20 M2-14
20 M3-14
20 M4-14
20 M5-14
20 M6-14
20 M7-14
D0 Q0
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
D7 Q7
MPR.DAT 0
20 M8-14 MDO 8
20 M9-14
20 M10-14
20 M11-14
20 M12-14
20 M13-14
20 M14-14
20 M15-14
MPR.DAT 8
G
F
24-29 →XACK
15 77-18 →MPREAD

Signal	Destination	Description
MDO(0-7)	19	Data output from dynamic RAM array bits 0-7.
MDO(8-15)	19	Data output from dynamic RAM array bits 8-15.

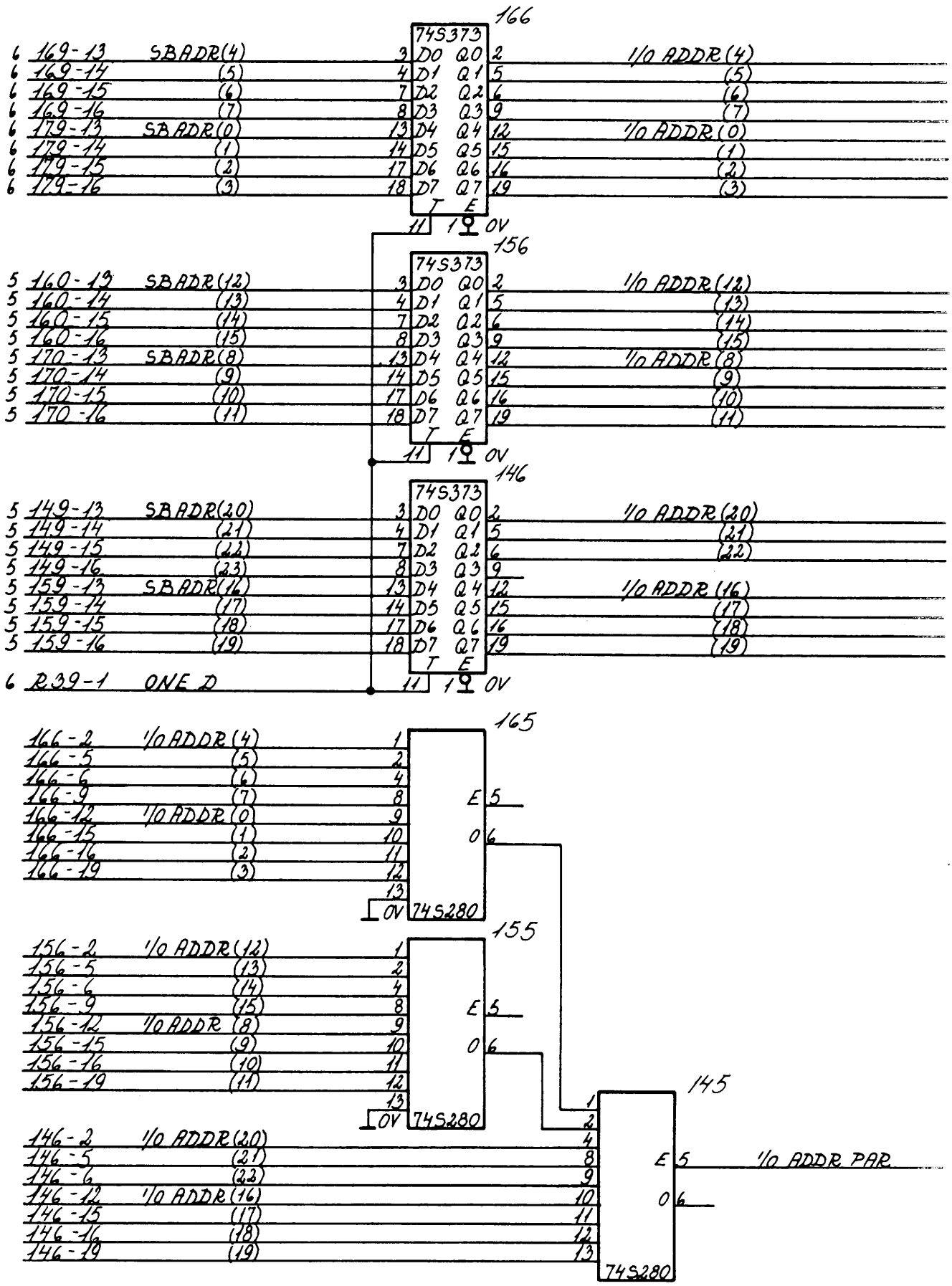

16 4164-15 nr
MDO 0
MDO 8
M0
M7
M8
M15
MPR DATO
RAMADR 0
WEHIGHB
WELOWB
RAS
CAS
WE
R2
R1
33

Signal	Destination	Description
RECIR	3	Receive Interrupt to the 8259A, indicating that the USART contains a charcter to the CPU.
TRMIR	3	Transmit Interrupt to the 8259A, indicating that the USART is ready to accept a new character from the CPU.
-,TRD	J1,J1005	Transmit data, serial data to the console.
RTS	J1,J1005	Request to send, to the console.
DTR	J1,J1005	Data terminal Ready, to the console.
RCD	21	Received data, serial data from the console.
-,RFS	21	Ready for sending, from the console.
-,DSR	21	Data Set Ready, from the console.
1.8432MHz	4,21	Clock signal for the 8254 Baud Rate generator and 8251A system clock.

Note: 71 is front panel connector J1005 is card edge connector.


70
8251A
2 98-18 IODATA 0 27 D0
2 98-17 1 28 D1
2 98-16 2 1 D2
2 98-15 3 2 D3
2 98-14 4 5 D4
2 98-13 5 6 D5
2 98-12 6 7 D6
2 98-11 7 8 D7
14 84-8 PURESET 21 RESET
60-3 1.8432 MHZ 20 CLK
18 97-12 ↑EN8251 11 CS
1 67-13 ↑IORC 13 RD
1 67-12 ↑AIOWC 10 WR
1 58-5 PUADR1 12 C/D
50-13 RCD 3 RXD
50-12 ↑RFS 17 CTS
50-11 ↑DSR 22 DSR
4 73-17 BAUD 25 RXC
9 TXC
RXRDY 14
TXRDY 15
TXEMP 18
SD/BD 16
TXD 19
RTS 23
DTR 24
RECIR
TRMIR
40A
75150
↑TRD J6-2
RTS J6-4
40B
75150
DTR J6-20
GND J6-7
0V
R28 1K
5V
J6-3 ↑RCD
75154
50
RCD
5V
J6-5 RFS
75154
50
↑RFS
2
J6-6 DSR
75154
50
↑DSR
1
16 44-2 3.6864MHz
74LS393
TA QA 3
QB 4
QC 5
QD 6
R 2
R29 180E
0V
↑1.8432 MHZ
50-4 ↑RCD 1005B-20
50-5 RFS 1005B-21
50-6 DSR 1005B-22
40A-7 ↑TRD 1005B-23
40A-6 RTS 1005B-24
40B-7 DTR 1005B-25

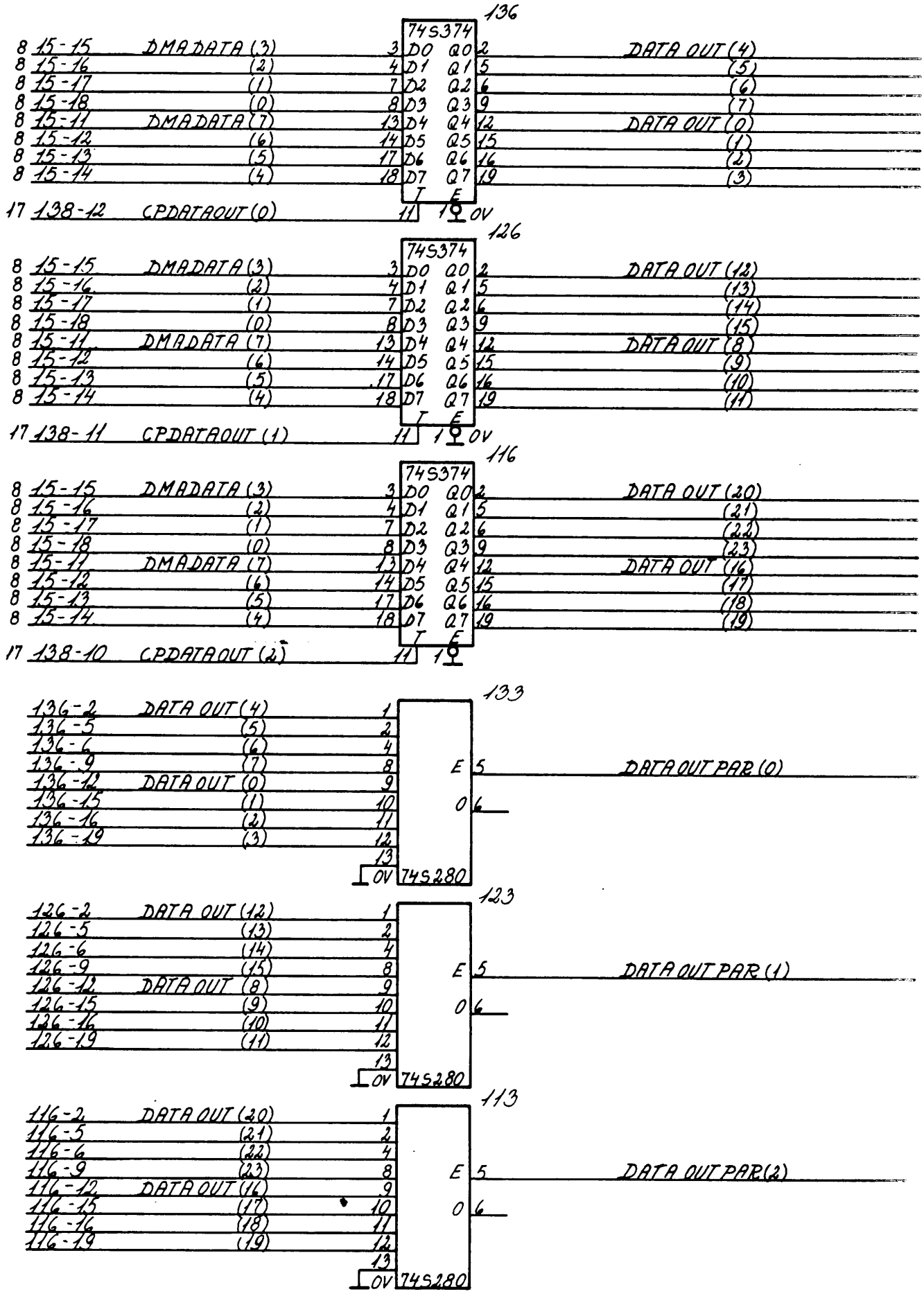
Signal	Destination	Description
I/OADDR(0:22)	22,27	Address register, which holds the RC8000 address during IFP accesses via the RC8000 System Bus.
I/OADDRPAR	27	Parity bit for RC8000 System Bus address. Odd parity is used.


166
74S373
6 169-13 SBADR(4) 3 D0 Q0 2 I/O ADDR(4)
6 169-14 (5) 4 D1 Q1 5 (5)
6 169-15 (6) 7 D2 Q2 6 (6)
6 169-16 (7) 8 D3 Q3 9 (7)
6 179-13 SBADR(0) 13 D4 Q4 12 I/O ADDR(0)
6 179-14 (1) 14 D5 Q5 15 (1)
6 179-15 (2) 17 D6 Q6 16 (2)
6 179-16 (3) 18 D7 Q7 19 (3)
T E
11 1 0V
156
74S373
5 160-13 SBADR(12) 3 D0 Q0 2 I/O ADDR(12)
5 160-14 (13) 4 D1 Q1 5 (13)
5 160-15 (14) 7 D2 Q2 6 (14)
5 160-16 (15) 8 D3 Q3 9 (15)
5 170-13 SBADR(8) 13 D4 Q4 12 I/O ADDR(8)
5 170-14 (9) 14 D5 Q5 15 (9)
5 170-15 (10) 17 D6 Q6 16 (10)
5 170-16 (11) 18 D7 Q7 19 (11)
T E
11 1 0V
146
74S373
5 149-13 SBADR(20) 3 D0 Q0 2 I/O ADDR(20)
5 149-14 (21) 4 D1 Q1 5 (21)
5 149-15 (22) 7 D2 Q2 6 (22)
5 149-16 (23) 8 D3 Q3 9
5 159-13 SBADR(16) 13 D4 Q4 12 I/O ADDR(16)
5 159-14 (17) 14 D5 Q5 15 (17)
5 159-15 (18) 17 D6 Q6 16 (18)
5 159-16 (19) 18 D7 Q7 19 (19)
T E
6 R39-1 ONE D 11 1 0V
165
166-2 I/O ADDR(4) 1
166-5 (5) 2
166-6 (6) 4
166-9 (7) 8 E 5
166-12 I/O ADDR(0) 9
166-15 (1) 10 0 6
166-16 (2) 11
166-19 (3) 12
13
0V 74S280
155
156-2 I/O ADDR(12) 1
156-5 (13) 2
156-6 (14) 4
156-9 (15) 8 E 5
156-12 I/O ADDR(8) 9
156-15 (9) 10 0 6
156-16 (10) 11
156-19 (11) 12
13
0V 74S280
145
146-2 I/O ADDR(20) 1
146-5 (21) 2
146-6 (22) 4
146-12 I/O ADDR(16) 8 E 5 I/O ADDR PAR
146-15 (17) 9
146-16 (18) 10 0 6
146-19 (19) 11
12
13
74S280

AGA

AAJ

Signal	Destination	Description
DATAOUT(0:23)	28	Data output register, which holds data to be transmitted via the RC8000 System Bus.
DATAOUTPAR(0)	29	Parity bit for DATAOUT(0:7). Odd parity is used.
DATAOUTPAR(1)	29	Parity bit for DATAOUT(8:15). Odd parity is used.
DATAOUTPAR(2)	29	Parity bit for DATAOUT(16:23). Odd parity is used.



AGA

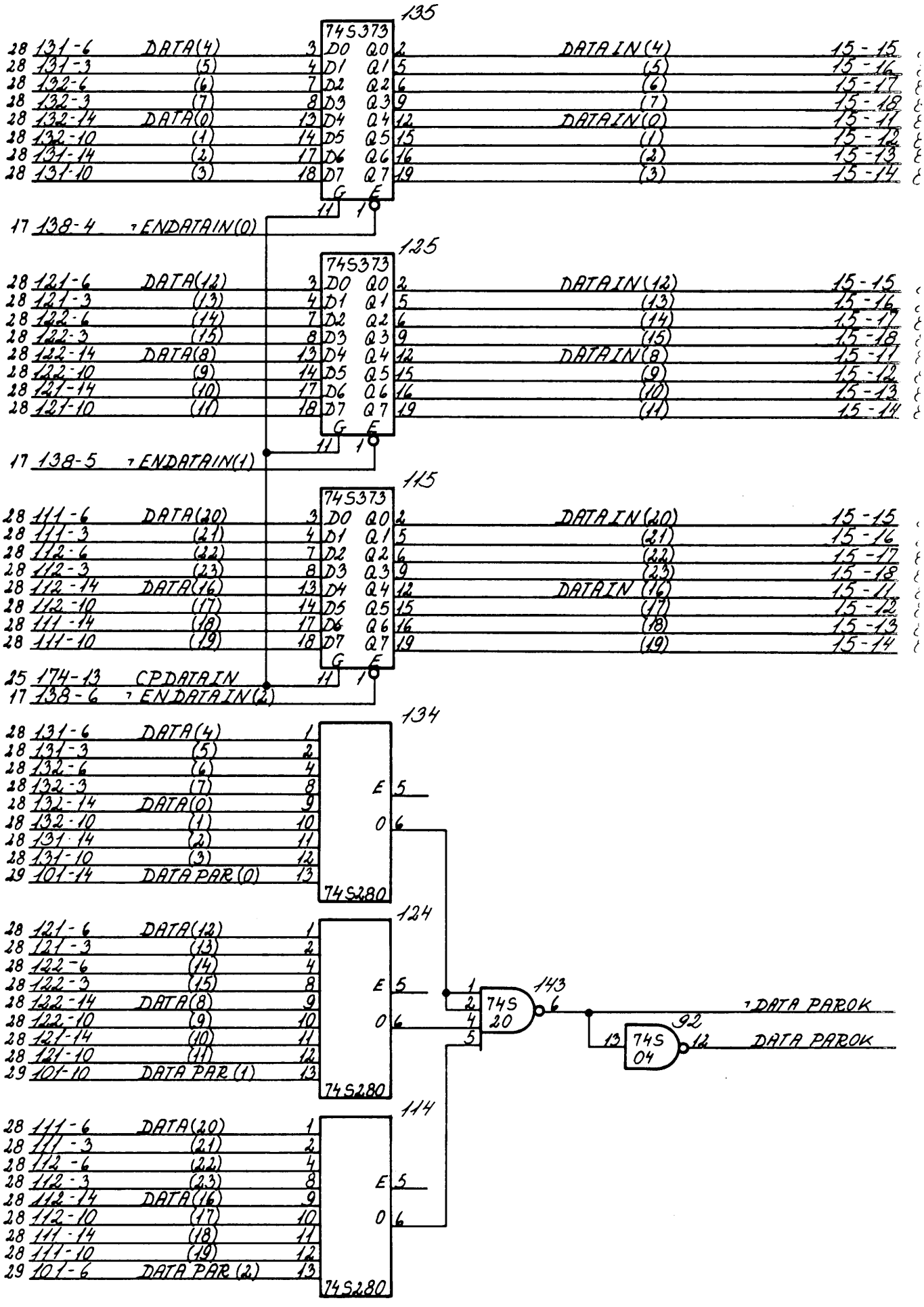
AAJ

IFP 802

R 13935

DATAOUT REGISTER
DATA PARITY GENERATOR

Signal	Destination	Description
DATAIN(0:23)	8	Data input register, which contains data received via the RC8000 System Bus after a read access. DATAIN(0:7), DATAIN(8:15) and DATAIN(16:23) are multiplexed to an 8-bit data bus connected to the multi-port RAM data bus.
-,DATAPAROK	14,24	DATAPAROK=1 indicates that data received via the RC8000 System Bus has correct parity.
DATAPAROK	14	



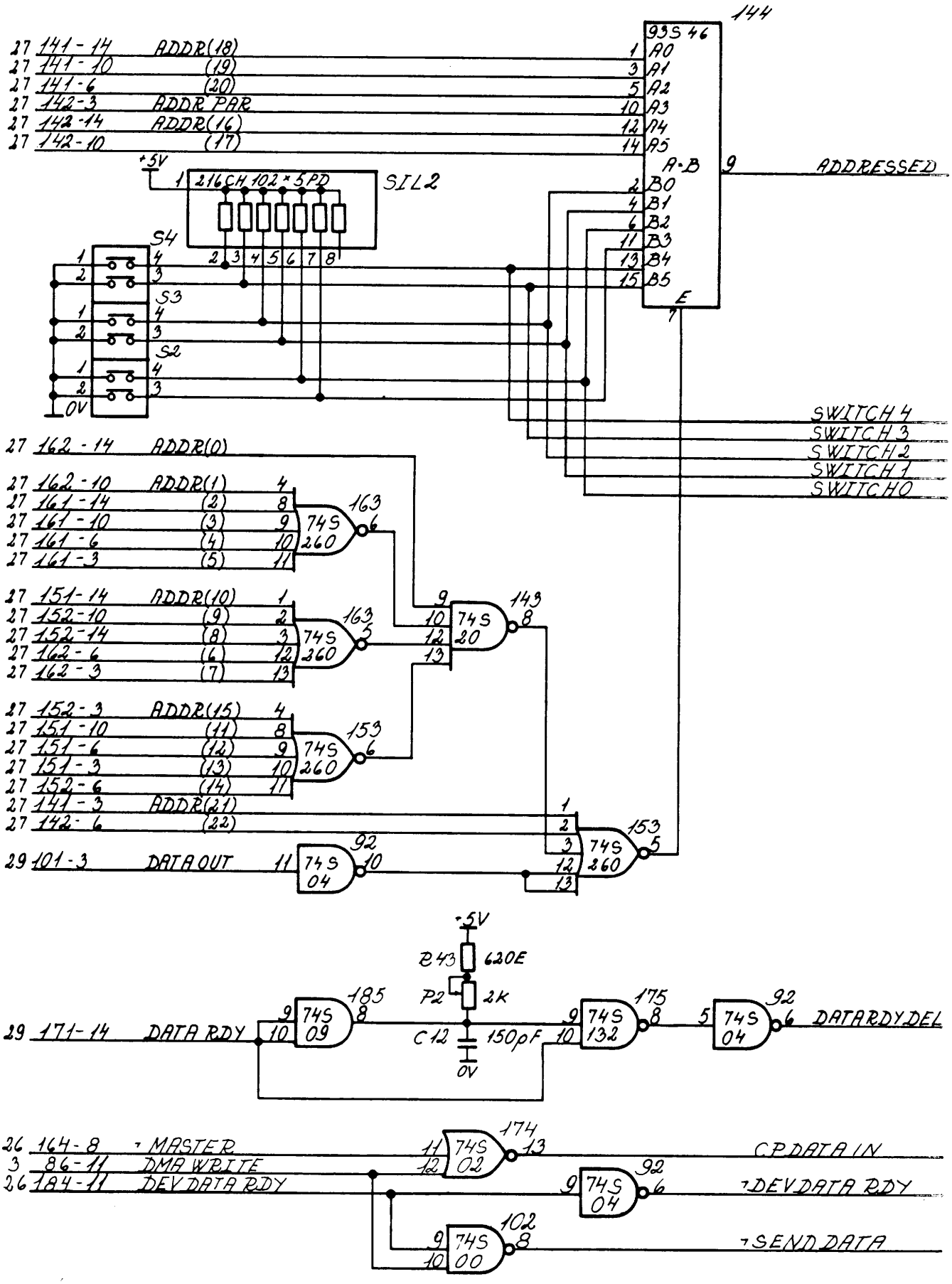
IFP 802

R 13936

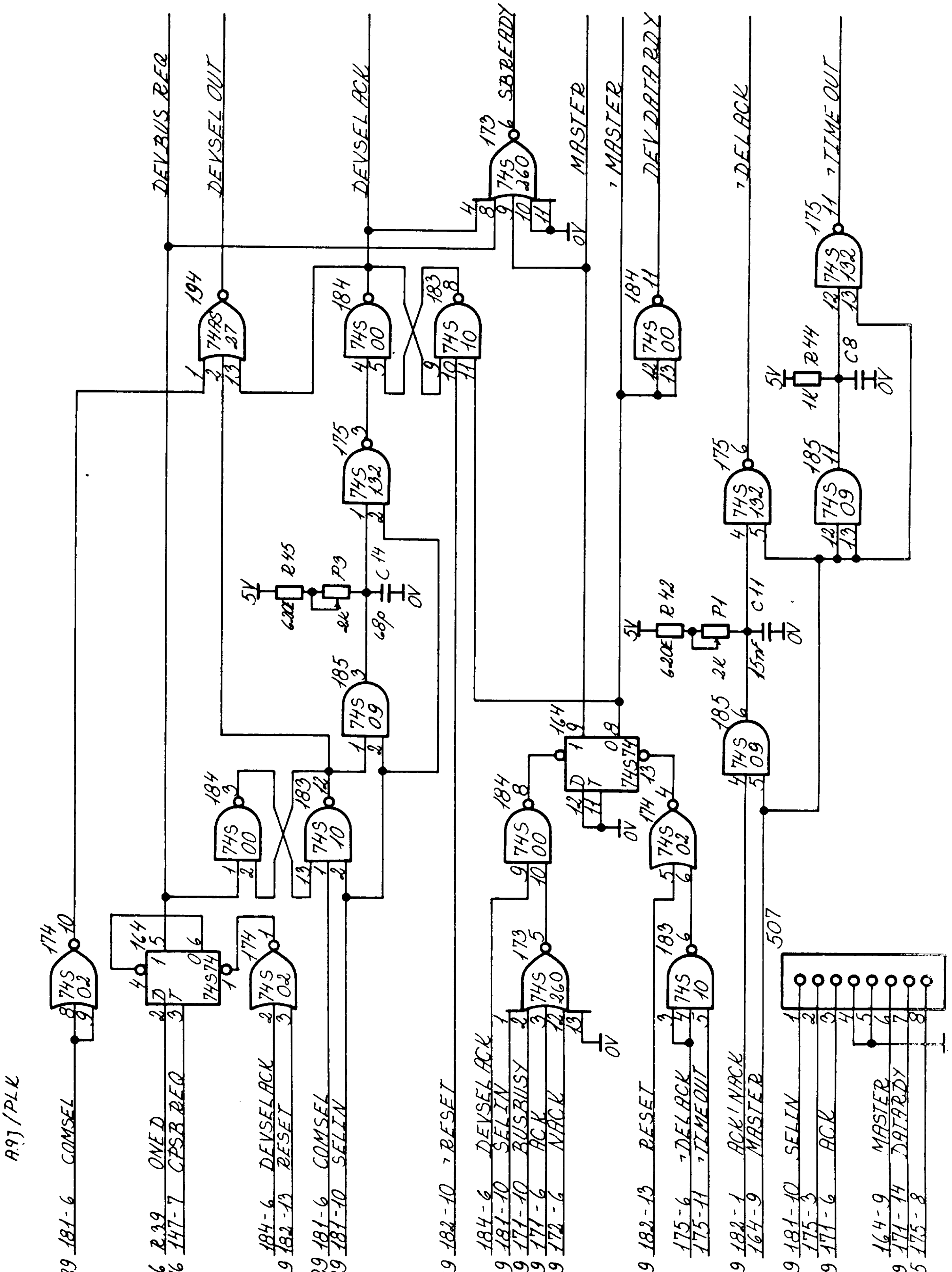
DATAIN REGISTER
DATA PARITY CHECK

24

Signal	Destination	Description
ADDRESSED	14	Indicates that the IFP 802 is addressed as a slave via the RC8000 System Bus.
SWITCH(4-0)	3	Output of Device Address switches to the 8255 Port B.
CPDATAIN	24	Data strobe for DATAIN register.
-,DEVDATARDY	27	Enables the System Bus address drivers.
-,SENDDATA	28,29	Enables the System Bus data drivers.


144
93S46
A0
A1
A2
A3
A4
A5
A·B
E
B0
B1
B2
B3
B4
B5
9
ADDRESSED
27 141-14 ADDR(18)
27 141-10 (19)
27 141-6 (20)
27 142-3 ADDR PAR
27 142-14 ADDR(16)
27 142-10 (17)
+5V
1
216CH 102×5PD
SIL2
S4
S3
S2
0V
SWITCH 4
SWITCH 3
SWITCH 2
SWITCH 1
SWITCH 0
27 162-14 ADDR(0)
27 162-10 ADDR(1)
27 161-14 (2)
27 161-10 (3)
27 161-6 (4)
27 161-3 (5)
74S 260
163
27 151-14 ADDR(10)
27 152-10 (9)
27 152-14 (8)
27 162-6 (6)
27 162-3 (7)
74S 360
74S 20
149
27 152-3 ADDR(15)
27 151-10 (11)
27 151-6 (12)
27 151-3 (13)
27 152-6 (14)
153
27 141-3 ADDR(21)
27 142-6 (22)
29 101-3 DATA OUT
74S 04
92
74S 260
R43 620E
P2 2K
C12 150pF
185
74S 09
74S 132
175
74S 04
29 171-14 DATA RDY
DATARDY.DEL
AAJ 26.6.81 AGA
26 164-8 ·MASTER
3 86-11 DMA WRITE
26 184-11 DEV DATA RDY
174
74S 02
CP DATA IN
·DEV DATA RDY
102
74S 00
·SEND DATA

Signal	Destination	Description
		The diagram shows the bus master selection logic for access to the RC8000 System Bus.
DEVBUSREQ	26,29	Bus master request signal.
DEVSELOUT	29	Bus master selection priority signal. Connected to input of the master with the next lower bus priority.
DEVSELACK	26,29	Bus master selection control signal indicating that the IFP will become busmaster when the current busmaster releases the bus.
SBREADY	3,16	Indicates the completion of a data transfer to or from a slave unit.
MASTER	26	Indicates that the IFP is busmaster.
-,MASTER	14,25,26	
DEVDATARDY	25,29	Generates the DATARDY and BUSBUSY signals.
-,DELACK	26	Delayed acknowledge signal generated by ACK or NACK.
-,TIMEOUT	26	Indicates that the IFP has been busmaster for approximtely 4 uS.

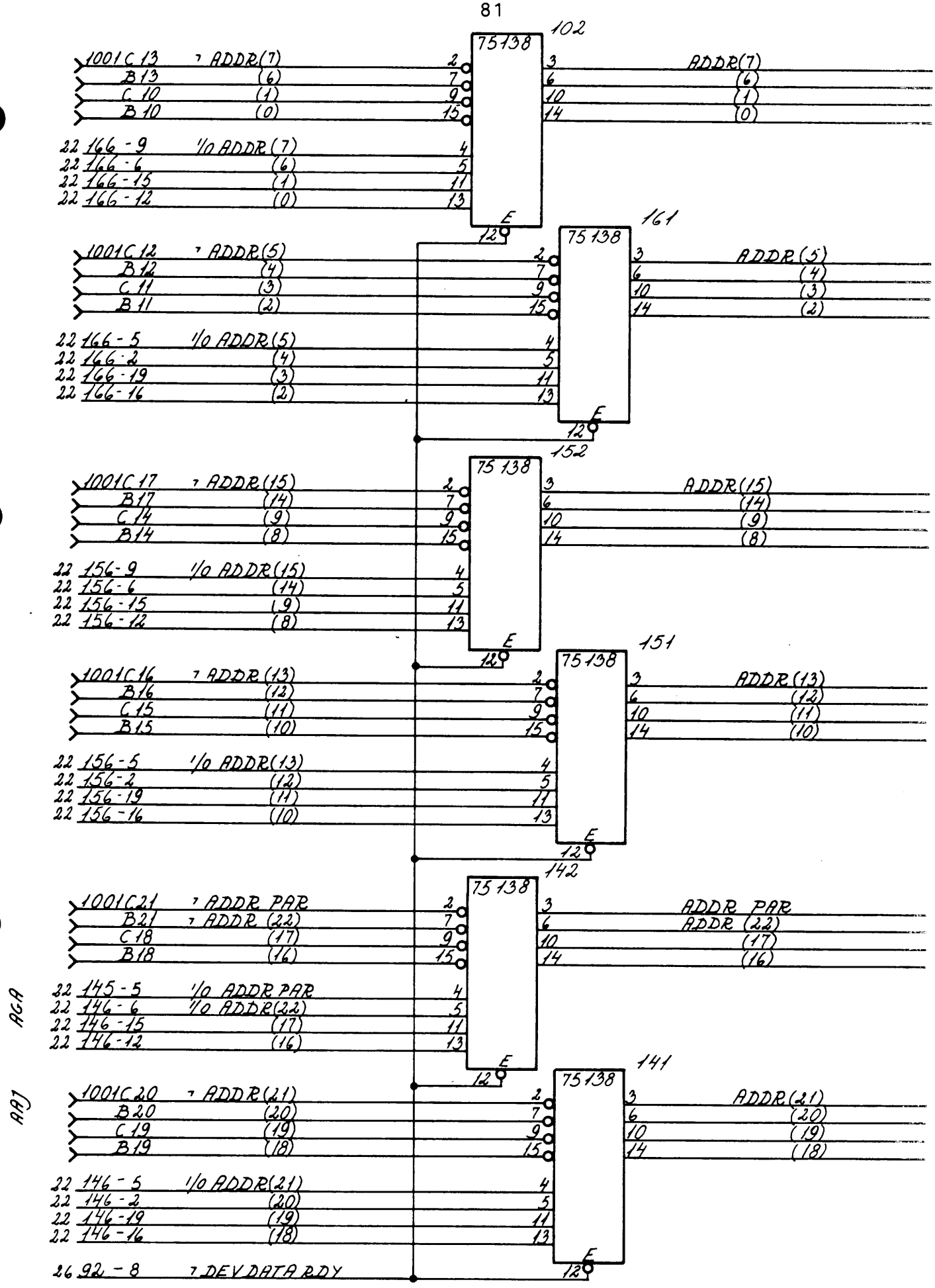


IFP 802

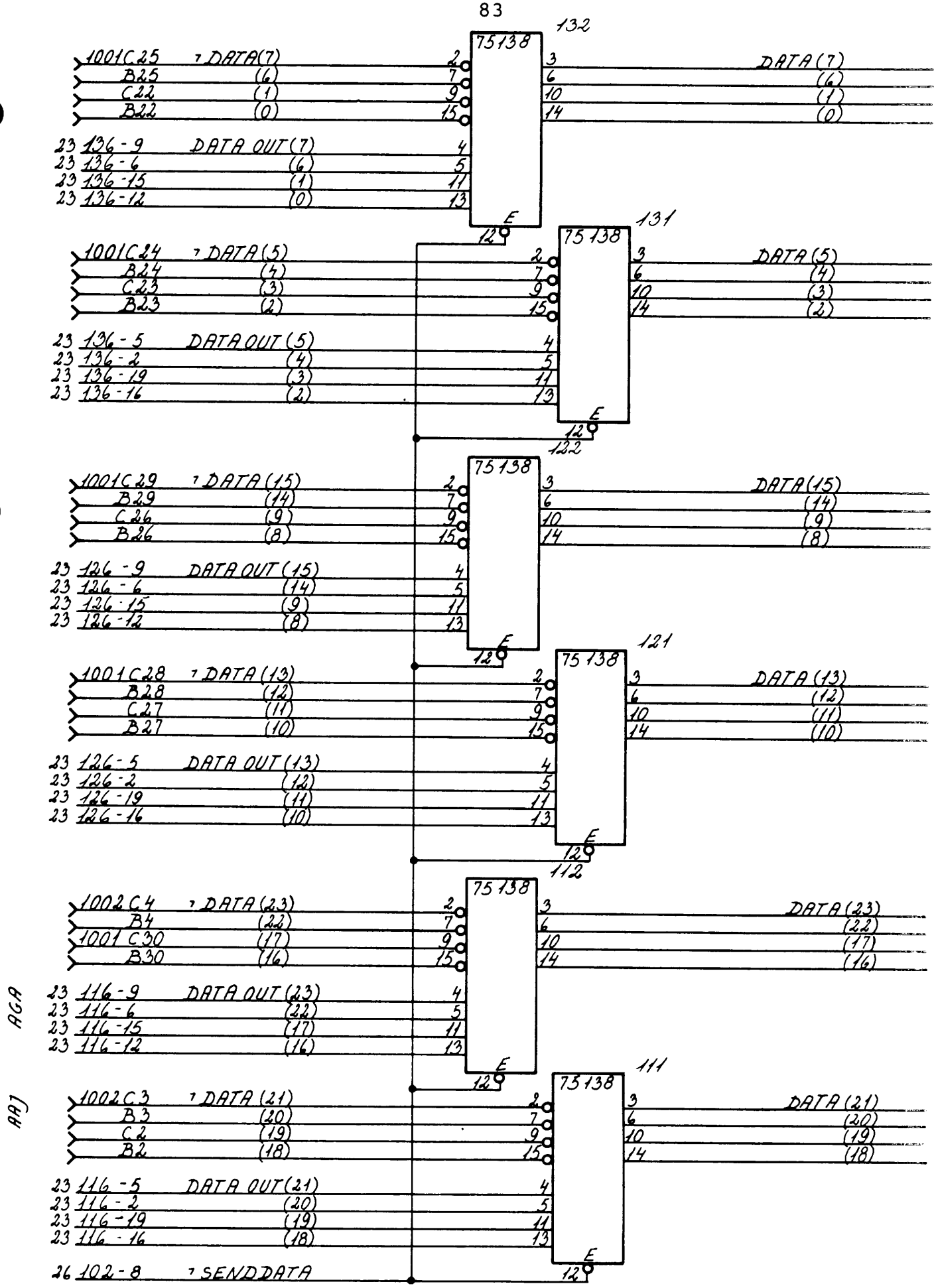
R 13938

RC 8000 SYSTEM BUS, BUS MASTER SELECTION CONTROL

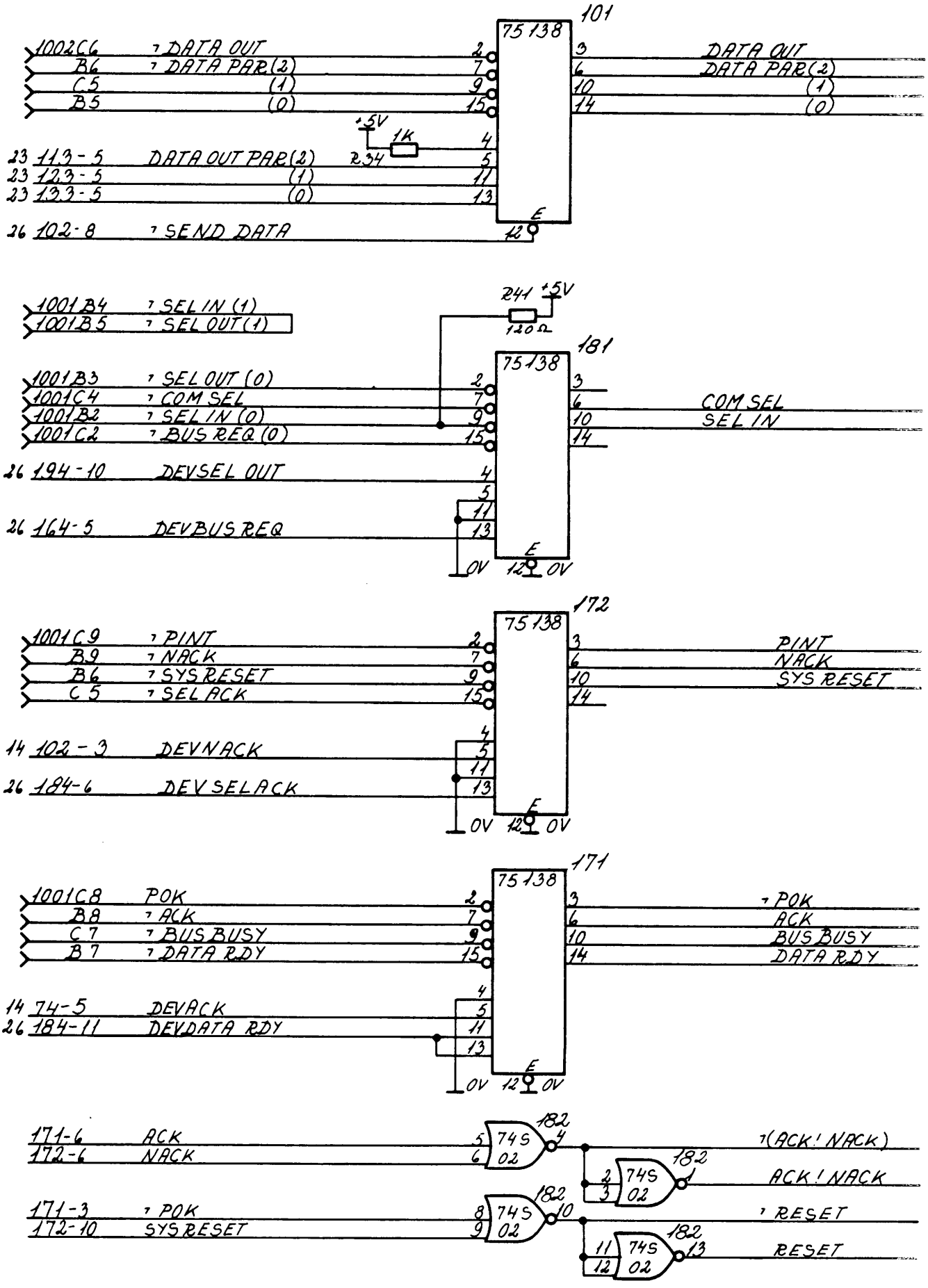
Signal	Destination	Description
ADDR(0:22)	25	Address received from RC8000 System Bus.
ADDRPAR	25	Parity bit for received System Bus address. Odd parity is used.


102
75138
1001C13 ⁊ ADDR(7)
B13 (6)
C10 (1)
B10 (0)
22 166-9 ¹/₀ ADDR(7)
22 166-6 (6)
22 166-15 (1)
22 166-12 (0)
2 7 9 15 4 5 11 13 12 E
3 6 10 14
ADDR(7) (6) (1) (0)
161
75138
1001C12 ⁊ ADDR(5)
B12 (4)
C11 (3)
B11 (2)
22 166-5 ¹/₀ ADDR(5)
22 166-2 (4)
22 166-19 (3)
22 166-16 (2)
ADDR(5) (4) (3) (2)
152
75138
1001C17 ⁊ ADDR(15)
B17 (14)
C14 (9)
B14 (8)
22 156-9 ¹/₀ ADDR(15)
22 156-6 (14)
22 156-15 (9)
22 156-12 (8)
ADDR(15) (14) (9) (8)
151
75138
1001C16 ⁊ ADDR(13)
B16 (12)
C15 (11)
B15 (10)
22 156-5 ¹/₀ ADDR(13)
22 156-2 (12)
22 156-19 (11)
22 156-16 (10)
ADDR(13) (12) (11) (10)
142
75138
1001C21 ⁊ ADDR PAR
B21 ⁊ ADDR(22)
C18 (17)
B18 (16)
22 145-5 ¹/₀ ADDR PAR
22 146-6 ¹/₀ ADDR(22)
22 146-15 (17)
22 146-12 (16)
ADDR PAR
ADDR(22) (17) (16)
AGA
141
75138
1001C20 ⁊ ADDR(21)
B20 (20)
C19 (19)
B19 (18)
22 146-5 ¹/₀ ADDR(21)
22 146-2 (20)
22 146-19 (19)
22 146-16 (18)
ADDR(21) (20) (19) (18)
AAJ
26 92-8 ⁊ DEV DATA RDY

Signal	Destination	Description
DATA(0:21)	24	Data received from RC8000 System Bus.
DATA(22:23)	14,24	


132
75138
1001C25 ↑DATA(7)
B25 (6)
C22 (1)
B22 (0)
23 136-9 DATA OUT(7)
23 136-6 (6)
23 136-15 (1)
23 136-12 (0)
DATA(7)
(6)
(1)
(0)
131
1001C24 ↑DATA(5)
B24 (4)
C23 (3)
B23 (2)
23 136-5 DATA OUT(5)
23 136-2 (4)
23 136-19 (3)
23 136-16 (2)
DATA(5)
(4)
(3)
(2)
122
1001C29 ↑DATA(15)
B29 (14)
C26 (9)
B26 (8)
23 126-9 DATA OUT(15)
23 126-6 (14)
23 126-15 (9)
23 126-12 (8)
DATA(15)
(14)
(9)
(8)
121
1001C28 ↑DATA(13)
B28 (12)
C27 (11)
B27 (10)
23 126-5 DATA OUT(13)
23 126-2 (12)
23 126-19 (11)
23 126-16 (10)
DATA(13)
(12)
(11)
(10)
112
1002C4 ↑DATA(23)
B4 (22)
1001C30 (17)
B30 (16)
23 116-9 DATA OUT(23)
23 116-6 (22)
23 116-15 (17)
23 116-12 (16)
DATA(23)
(22)
(17)
(16)
AGA
111
1002C3 ↑DATA(21)
B3 (20)
C2 (19)
B2 (18)
23 116-5 DATA OUT(21)
23 116-2 (20)
23 116-19 (19)
23 116-16 (18)
DATA(21)
(20)
(19)
(18)
AAJ
26 102-8 ↑SENDDATA

Signal	Destination	Description
DATAOUT	25	DATAOUT=1 indicates transfer of data from master to slave. A 0 indicates data transfer in the opposite direction.
DATAPAR(2)	24	Parity bit for received data, DATA(16:23).
DATAPAR(1)	24	Parity bit for received data, DATA(8:15).
DATAPAR(0)	24	Parity bit for received data, DATA(0:7).
COMSEL	26	Bus master selection control signal.
SELIN	26	Bus master selection priority signal. Indicates that no higher priority units is requesting access to the System Bus.
PINT	14	Power low warning signal from power supply.
NACK	14,26,29	Response from slave indicating that it has received data with parity error or that it is not able to transmit correct data.
SYSRESET	29	System reset signal.
-,POK	29	Signal from power supply indicating that the dc voltages are correct.
ACK	26,29	Response from slave indicating that it has accepted or transmitted data.
BUSBUSY	26	Indicates that the System Bus is being used.
DATARDY	25,26	Indicates to the slave that address (and data) is available on the System Bus.
-,(ACK!NACK)	14,29	Used to generate SBTIMEOUT status.
ACK!NACK	26	ACK or NACK is received.
-,RESET RESET	14,26,29 26	Reset signals generated by -,POK or SYSRESET.


101
75138
1002C6 ⁊ DATA OUT
B6 ⁊ DATA PAR(2)
C5 (1)
B5 (0)
+5V
1K
R34
23 113-5 DATA OUT PAR(2)
23 123-5 (1)
23 133-5 (0)
26 102-8 ⁊ SEND DATA
DATA OUT
DATA PAR(2)
(1)
(0)
241 +5V
120Ω
181
1001B4 ⁊ SEL IN (1)
1001B5 ⁊ SEL OUT(1)
1001B3 ⁊ SEL OUT (0)
1001C4 ⁊ COM SEL
1001B2 ⁊ SEL IN (0)
1001C2 ⁊ BUS REQ (0)
26 194-10 DEVSEL OUT
26 164-5 DEVBUS REQ
COM SEL
SEL IN
OV
172
1001C9 ⁊ PINT
B9 ⁊ NACK
B6 ⁊ SYS RESET
C5 ⁊ SEL ACK
14 102-3 DEVNACK
26 184-6 DEV SEL ACK
PINT
NACK
SYS RESET
171
1001C8 POK
B8 ⁊ ACK
C7 ⁊ BUS BUSY
B7 ⁊ DATA RDY
14 74-5 DEVACK
26 184-11 DEV DATA RDY
⁊ POK
ACK
BUS BUSY
DATA RDY
AGA
AAJ
171-6 ACK
172-6 NACK
182
74S 02
⁊(ACK ! NACK)
ACK ! NACK
171-3 ⁊ POK
172-10 SYS RESET
⁊ RESET
RESET

ROA414 DMA Control PROM

ADDRESS octal	OUTPUTS 8	7	6	5	4	3	2	1
0	0	0	0	0	0	0	0	0
1	0	1	1	0	1	0	1	0
2	1	1	0	0	1	1	0	0
3	0	0	0	0	0	0	0	0
4	0	1	1	0	1	0	1	0
5	1	1	0	0	1	1	0	0
6	1	0	0	0	1	0	0	1
7	1	0	0	0	1	0	0	1
10	0	1	0	0	1	0	0	0
11	0	1	0	0	1	0	0	0
12	0	1	1	0	1	0	1	0
13	1	0	0	0	1	0	0	1
14	0	1	1	0	1	0	1	0
15	0	1	1	1	1	0	1	0
16	0	0	1	0	1	0	0	0
17	0	1	1	1	1	0	1	0
20	0	0	0	0	0	0	0	0
21	1	0	0	0	1	0	0	1
22	1	0	0	0	1	0	0	1
23	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0
26	0	0	0	0	0	0	0	0
27	0	0	0	0	0	0	0	0
30	0	1	0	0	1	0	0	0
31	0	1	0	0	1	0	0	0
32	1	1	0	0	1	0	0	0
33	1	1	0	0	1	0	0	0
34	0	0	0	0	0	0	0	0
35	0	0	0	0	0	0	0	0
36	0	0	0	0	0	0	0	0
37	0	0	0	0	0	0	0	0

OUTPUT 1: DMAINTR*
2: DMAMPREQ*
3: CPSBREQ*
4: DMABUSY*
5: A*
6: ROW ADDR(0)* (least significant)
7: (1)*
8: (2)*

ROA415 Address Decoding PROM

ADDRESS	OUTPUTS							
octal	8	7	6	5	4	3	2	1
0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0
2	0	0	0	0	0	1	0	0
3	0	0	0	0	0	1	0	0
4	0	0	0	0	0	1	0	0
5	0	0	0	0	0	1	0	0
6	0	0	0	0	0	1	0	0
7	0	0	0	0	0	1	0	0
10	0	0	0	0	0	1	0	0
11	0	0	0	0	0	1	0	0
12	0	0	0	0	0	1	0	0
13	0	0	0	0	0	1	0	0
14	0	0	0	0	0	1	0	0
15	0	0	0	0	0	1	0	0
16	0	0	0	0	0	1	0	0
17	0	0	0	0	0	1	0	0
20	0	0	0	0	0	1	1	1
21	0	0	0	0	0	1	1	1
22	0	0	0	0	0	1	1	0
23	0	0	0	0	0	1	1	0
24	0	0	0	0	0	1	1	0
25	0	0	0	0	0	1	1	0
26	0	0	0	0	0	1	1	0
27	0	0	0	0	0	1	1	0
30	0	0	0	0	0	1	1	0
31	0	0	0	0	0	1	1	0
32	0	0	0	0	0	1	1	0
33	0	0	0	0	0	1	1	0
34	0	0	0	0	0	1	1	0
35	0	0	0	0	0	1	1	0
36	0	0	0	0	0	1	1	0
37	0	0	0	0	0	0	0	0

OUTPUT 1: RAMADR
2: -,(ROM or IOADR)
3: -,ENROM
4-8: UNUSED

PAL 006 Multiport Interrupt Address Decoding

TYPE: PAL16L8, AND-OR INVERT ARRAY

INPUT PINS: 1, 2, 3, 4, 5, 6, 7, 8, 9, 11, 13, 14, 15, 16, 17, 18

OUTPUT PIN: 19, 12 (unused)

INPUT																OUTPUT
1	2	3	4	5	6	7	8	9	11	13	14	15	16	17	18	19
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	1
X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	1
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	1
X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	1
X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	1
X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	1
X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	1
X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	1
X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	1
X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	1
X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	1
X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	1
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1

X = do not care.

CONNECTOR 1001, RC8000 System Bus

PIN	A ROW	B ROW		C ROW	
	SIGNAL	GEN	SIGNAL	GEN	SIGNAL
1	+5 VOLTS		+5 VOLTS		+5VOLTS
2	0 VOLT		-,SELIN(0)	181-15	-,BUSREQ(0)
3	-	181-2	-,SELOUT(0)		-,BUSREQ(1)
4	-		-,SELIN(1)		-,COMSEL
5	-	1001B4	-,SELOUT(1)	172-15	-,SELACK
6	-		-,SYSRESET		POB
7	-	171-15	-,DATARDY	171-9	-,BUSBUSY
8	-	171-7	-,ACK		POK
9	-	172-7	-,NACK		-,PINT
10	-	102-15	-,ADDR(0)	102-9	-,ADDR(1)
11	-	161-15	(2)	161-9	(3)
12	-	161-7	(4)	161-20	(5)
13	-	102-7	(6)	102-2	(7)
14	-	152-15	(8)	152-9	(9)
15	-	151-15	(10)	151-9	(11)
16	-	151-7	(12)	151-2	(13)
17	-	152-7	(14)	152-2	(15)
18	-	142-15	(16)	142-9	(17)
19	-	141-15	(18)	141-9	(19)
20	-	141-7	(20)	141-2	(21)
21	-	142-7	(22)	142-2	-,ADDRPAR
22	-	132-15	-,DATA(0)	132-9	-,DATA(1)
23	-	131-15	(2)	131-9	(3)
24	-	131-7	(4)	131-2	(5)
25	-	132-7	(6)	132-2	(7)
26	-	122-15	(8)	122-9	(9)
27	-	121-15	(10)	121-9	(11)
28	-	121-7	(12)	121-2	(13)
29	-	122-7	(14)	122-2	(15)
30	-	112-15	(16)	112-9	(17)
31	+12 VOLTS		+12 VOLTS		+12 VOLTS
32	+5 VOLTS		+5 VOLTS		+5 VOLTS

CONNECTOR 1002, RC8000 System Bus

PIN	A ROW	B ROW		C ROW	
	SIGNAL	GEN	SIGNAL	GEN	SIGNAL
1	+5 VOLTS		+5 VOLTS		+5VOLTS
2	0 VOLT	111-15	-,DATA(18)	111-9	-,DATA(19)
3	-	111-7	(20)	111-2	(21)
4	-	112-7	(22)	112-2	(23)
5	-	101-15	-,DATAPAR(0)	101-9	-,DATAPAR(1)
6	-	101-7	(2)	101-2	-,DATAOUT
7	-				
8	-				
9	-				
10	-				
11	-				
12	-				
13	-				
14	-				
15	-				
16	-				
17	-				
18	-				
19	-				
20	-				
21	-				
22	-				
23	-				
24	-				
25	-				
26	-				
27	-				
28	-				
29	-				
30	-				
31	-12 VOLTS		-12 VOLTS		-12 VOLTS
32	+5 VOLTS		+5 VOLTS		+5 VOLTS

CONNECTOR 1003

PIN	A ROW	B ROW		C ROW	
	SIGNAL	GEN	SIGNAL	GEN	SIGNAL
1	+5 VOLTS		+5 VOLTS		+5VOLTS
2	0 VOLT				
3	-				
4	-				
5	-				
6	-				
7	-				
8	-				
9	-				
10	-				
11	-				
12	-				
13	-				
14	-				
15	-				
16	-				
17	-				
18	-				
19	-				
20	-				
21	-				
22	-				
23	-				
24	-				
25	-				
26	-				
27	-				
28	-				
29	-				
30	-				
31	-				
32	+5 VOLTS		+5 VOLTS		+5 VOLTS

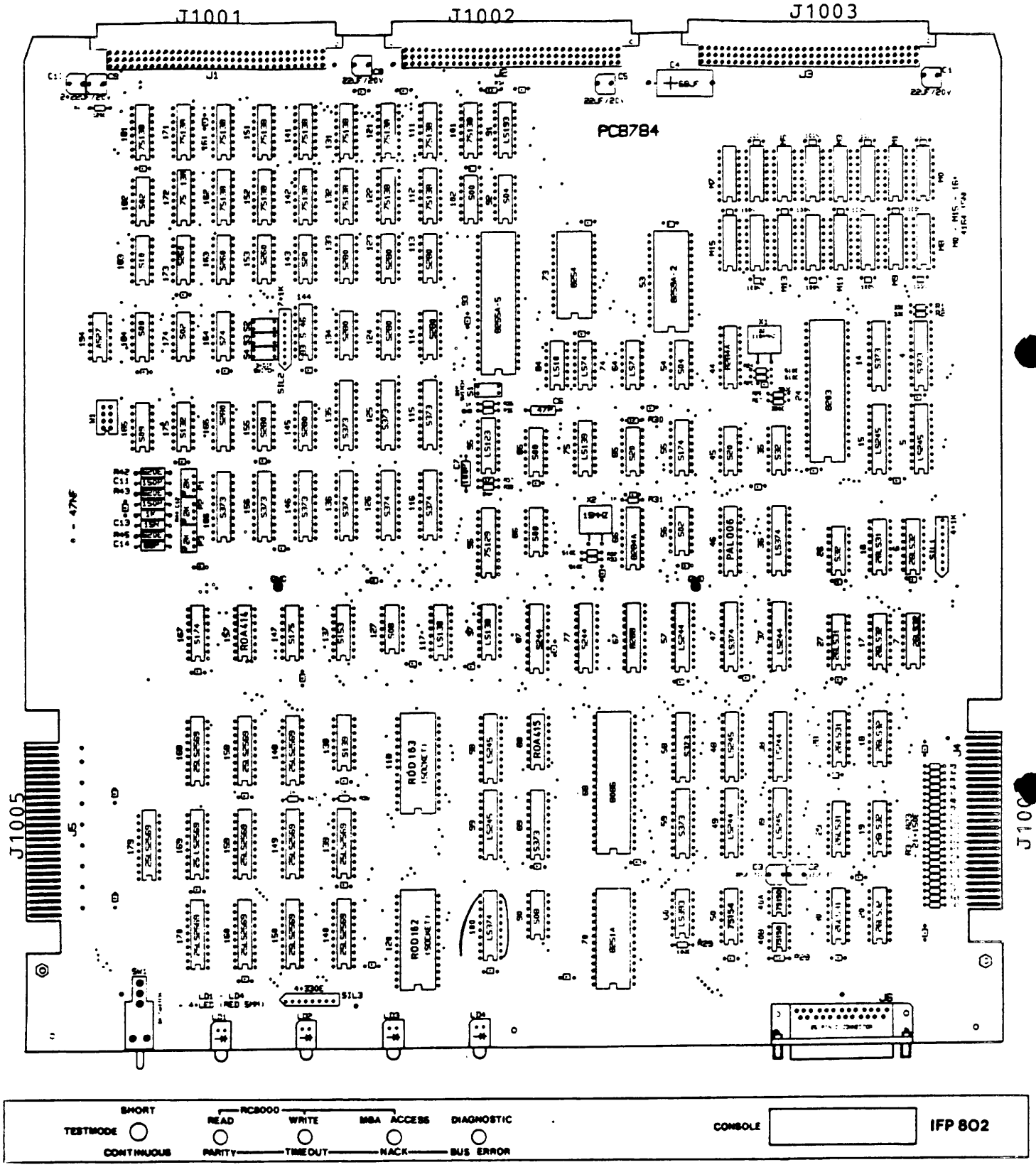
CONNECTOR 1004, MBA Connection

PIN	GEN	SIGNAL	PIN	GEN	SIGNAL
A1	30-2	IFBUS0	B1	30-3	-,IFBUS0
A2	30-6	1	B2	30-5	1
A3	30-10	2	B3	30-11	2
A4	30-14	3	B4	30-13	3
A5	29-2	4	B5	29-3	4
A6	29-6	5	B6	29-5	5
A7	29-10	6	B7	29-11	6
A8	29-14	7	B8	29-13	7
A9	28-2	8	B9	28-3	8
A10	28-6	9	B10	28-5	9
A11	28-10	A	B11	28-11	A
A12	28-14	B	B12	28-13	B
A13	27-2	C	B13	27-3	C
A14	27-6	D	B14	27-5	D
A15	27-10	E	B15	27-11	E
A16	27-14	F	B16	27-13	F
A17		IFADR0	B17		-,IFADR0
A18		IFBHEN	B18		-,IFBHEN
A19		-,IFREAD	B19		IFREAD
A20		-,IFWRITE	B20		IFWRITE
A21		LDADR	B21		-,LDADR
A22	16-2	-,IFACK	B22	16-3	IFACK
A23	16-6	-,IFINTR	B23	16-5	IFINTR
A24	16-10	-,IFRESET	B24	16-11	IFRESET
A25		0 VOLT	B25		0 VOLT

KBL666 MBA Interface Cable, Internal

J1004	Conn. II	Signal	J1004	Conn. II	Signal
A1	1	IFBUS0	A17	28	IFADR0
B1	34	-,IFBUS0	B17	12	-,IFADR0
A2	18	IFBUS1	A18	45	IFBHEN
B2	2	-,IFBUS1	B18	29	-,IFBHEN
A3	35	IFBUS2	A19	13	-,IFREAD
B3	19	-,IFBUS2	B19	46	IFREAD
A4	3	IFBUS3	A20	30	-,IFWRITE
B4	36	-,IFBUS3	B20	14	IFWRITE
A5	20	IFBUS4	A21	47	LDADR
B5	4	-,IFBUS4	B21	31	-,LDADR
A6	37	IFBUS5	A22	15	-,IFACK
B6	21	-,IFBUS5	B22	48	IFACK
A7	5	IFBUS6	A23	32	-,IFINTR
B7	38	-,IFBUS6	B23	16	IFINTR
A8	22	IFBUS7	A24	49	-,IFRESET
B8	6	-,IFBUS7	B24	33	IFRESET
A9	39	IFBUS8	A25	17	0 VOLT
B9	23	-,IFBUS8	B25	50	0 VOLT
A10	7	IFBUS9			
B10	40	-,IFBUS9			
A11	24	IFBUS10			
B11	8	-,IFBUS10			
A12	41	IFBUS11			
B12	25	-,IFBUS11			
A13	9	IFBUS12			
B13	42	-,IFBUS12			
A14	26	IFBUS13			
B14	10	-,IFBUS13			
A15	43	IFBUS14			
B15	27	-,IFBUS14			
A16	11	IFBUS15			
B16	44	-,IFBUS15			

9. ASSEMBLY DRAWING



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