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Author: Poul L. Knudsen

Title:

IFP802
General Information

RCSL Nr. 46-F 0087

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Keywords:

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Abstract:

This manual contains general information on IFP802.

(20 printed pages)

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1 GENERAL DESCRIPTION

IFP802, Interface Processor, is the RC8000 part of the two controllers connecting the RC8000 computer system and the Multibus.
Connection to the Multibus is provided by the MBA602, Multibus Adapter.

The IFP802 is an 8086 microprocessor based controller provided with a multi-port RAM with one port reserved for Multibus access through the MBA602.
The multi-port RAM is used for communication between RC8000 and Multibus units.
Seen from the Multibus the IFP802 - MBA602 is a slave unit with 64 K byte RAM.

Data transfer between RC8000 memory and the IFP802 multi-port RAM is controlled by a DMA controller.
During data transfer the RC8000 data representation with 3 bytes/word is transferred to/from the Intel 16-bit representation.

For selftest and debugging purposes the IFP802 is provided with a V.24/V.28 console interface.

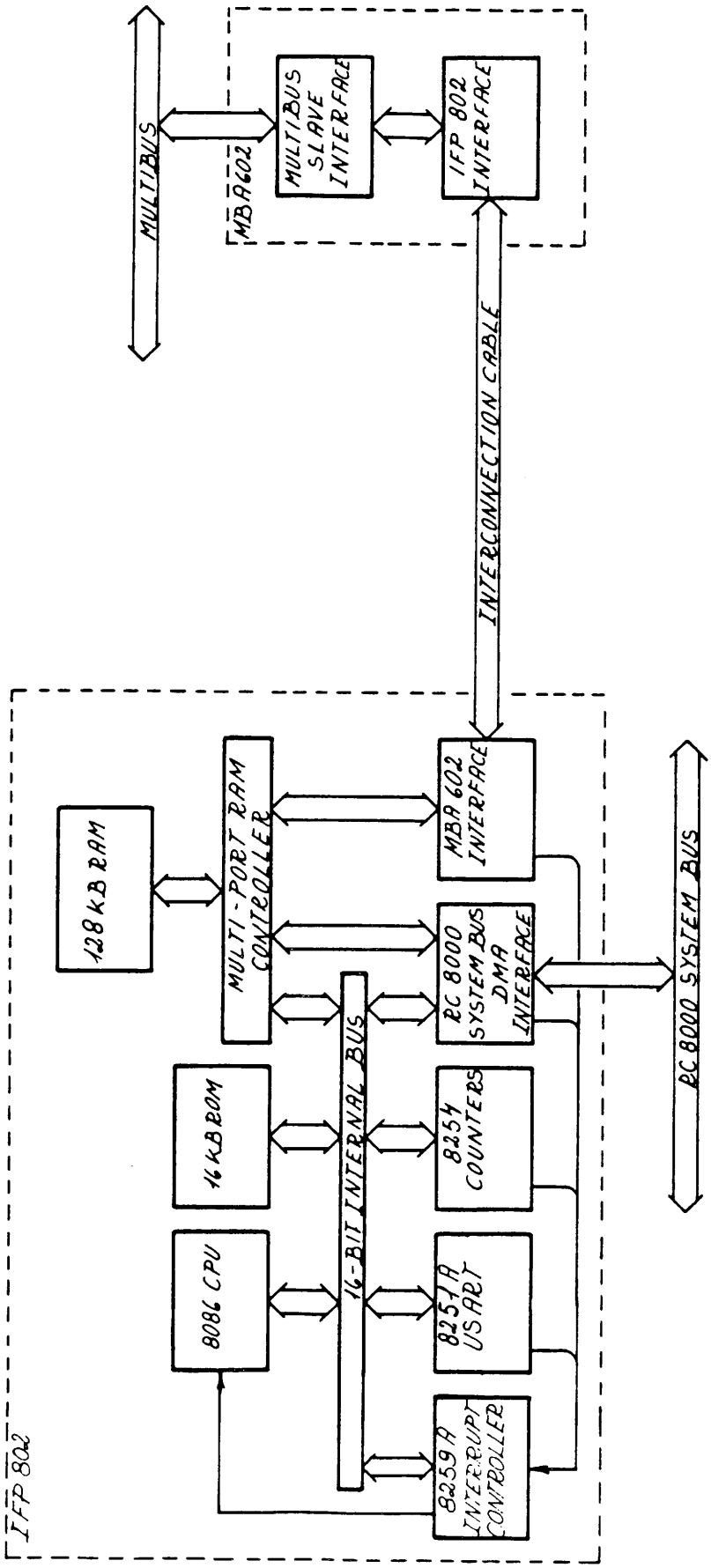


Fig. 1 The logical structure of IFP802.

2. SPECIFICATIONS

2.1 PERFORMANCE SPECIFICATIONS

8086 CPU clock rate	5 MHz
EPROM capacity	16 K bytes
RAM capacity	128 K bytes (Dynamic RAM)
System Interface	Standard RC8000 unified Bus Interface
MBA Interface	Bidirectional, multiplexed address/data tri-state bus with differential mode signals.
Console Interface	V.24/V.28 asynchronous, max. 9600 bps.
Transfer Rates	Transfer rate between IFP802 and RC8000 is depending on the RC8000 system bus load and memory used. Mean access time (read or write) between Multibus and IFP802 will be appr. 0,85 usec and mean cycle time appr. 1,4 usec, but will depend on memory refresh and Multibus load.

2.2 ELECTRICAL SPECIFICATIONS

Supply voltages	+5 V +-5%, 7,2 A
	+12 V +-5%, 0,05 A
	-12 V +-5%, 0,05 A

2.3 ENVIROMENTAL SPECIFICATIONS

Ambient temperature	10 - 35 ^{0}C
Relative humidity (%)	20 - 80 non condensing
Heat dissipation	37 W

2.4 PHYSICAL SPECIFICATIONS

1 slot in a RC8000 controller chassis

Weight	0,9 Kg

3. IDENTIFICATION OF ITEMS

The list below describes the items that can be used in a system

Item		Reference number	Description
1		IFP802	Interface Processor
2		KBL666	Int. IFP-MBA signal cable
3		DDM234	Device Manual for IFP802
4		KBL668	IFP-MBA ext. cable 12 m.
	or	KBL786	IFP-MBA ext. cable 2,5 m.
	or	KBL795	IFP-MBA ext. cable 1,5 m.

4. INSTALLATION

4.1 INSTALLATION OF IFP802 IN THE CONTROLLER CHASSIS

IFP802 must be installed in a free slot in a RC8000 controller chassis.
Connection to the RC8000 System Bus is made via the backplane on the controller chassis.
Connection to the Multibus Adapter, MBA602, is made via an internal cable to J1004 side-connector.
Connection to the console can be made either via the front-mounted connector J6 or via an internal cable to side-connector J1005.

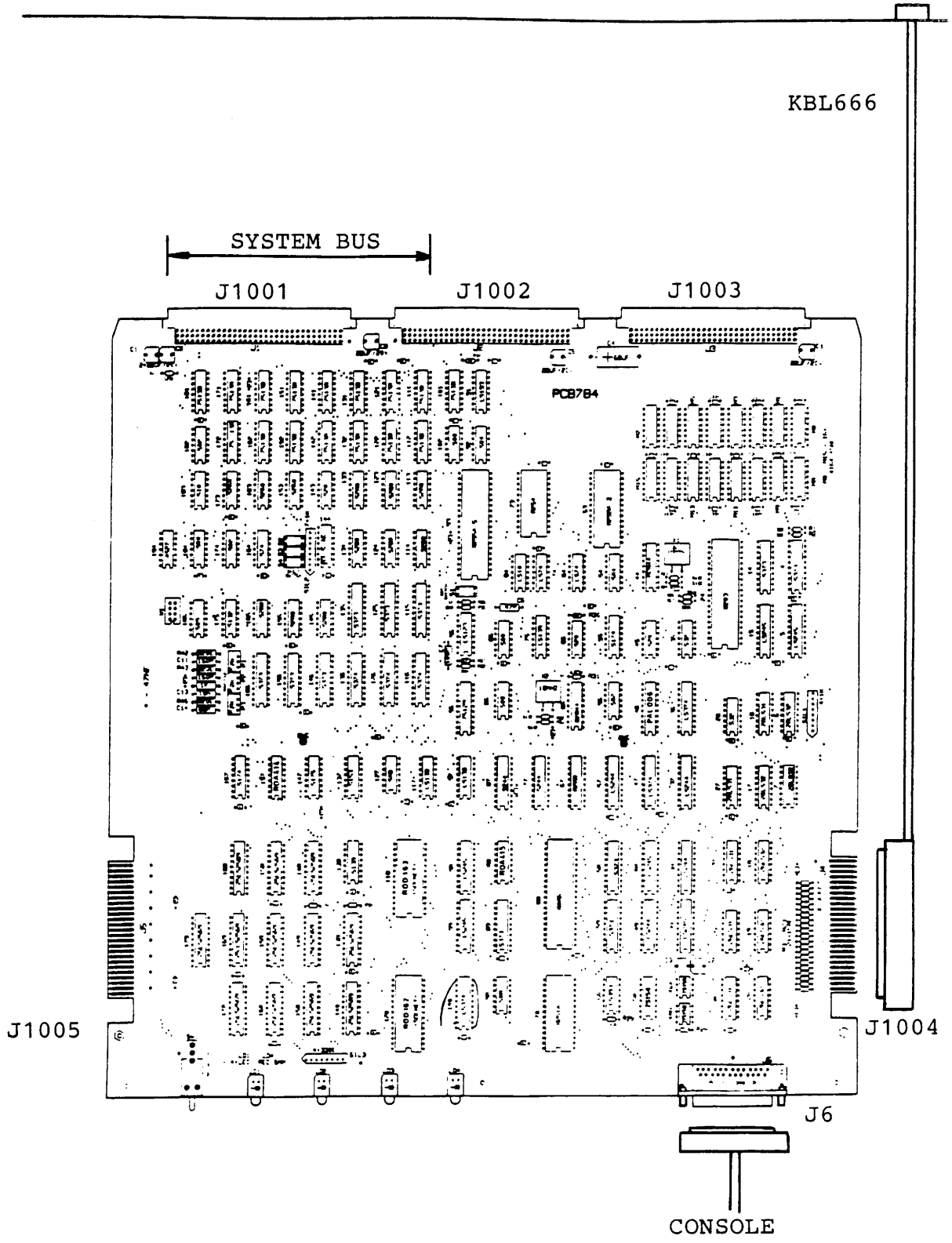


Fig. 2 Cabling of IFP802

4.2 SWITCHES

IFP DEVICE ADDRESS

The device Address is selectable by means of 3 x 2 switches on the PCB. Address bits (16:20) and parity are selectable, whereas the remaining address-bits are fixed. The parity switch must be set to form an even number of one's in the switch row.

Red dot visible =0
(If no red dot in switch:
white dot =0)

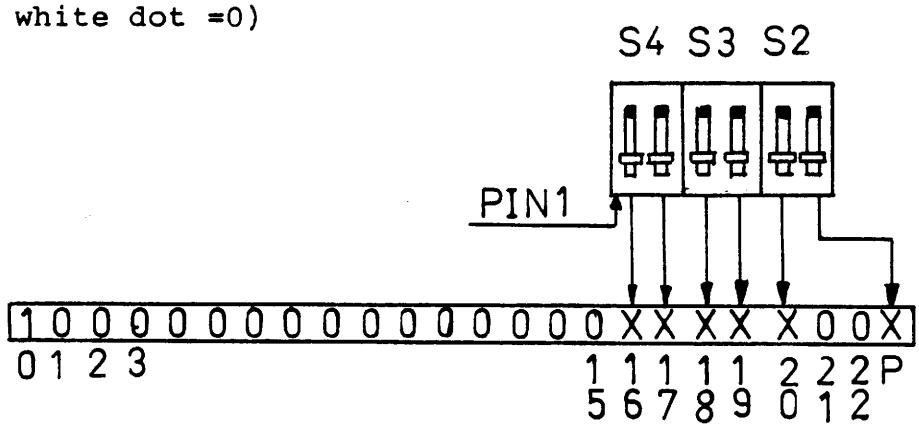


Fig. 3 IFP802 Device Address switch, position 154

DESKEW ADJUST SWITCH

For adjustment of deskew delay, this switch can be set before autoload, which causes the selftest to execute RC8000 DMA-test without checking data and status.

Red dot visible =0

0 = inactive
1 = active

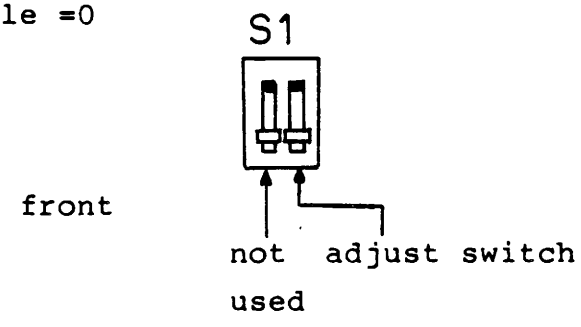


Fig. 4 Deskew adjust switch, position 94

4.3 FRONTPANEL

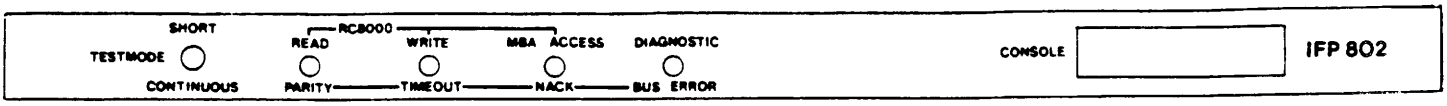


Fig.5 Frontpanel

TESTMODE SWITCH

After power-up or after a system reset, the built-in selftest is entered, and a part of the selftest, or the whole, is executed dependend on the position of this switch.
With the switch in "short" mode the standard selftests (1-5) are executed one time, whereafter the debug-monitor is loaded.
In "continous" mode the extended selftest is included, and the selftests will be executed continously until an error is detected or a new reset is given.
For more detailed information about the selftest consult ref.1

LEDs

These four LEDs are used under both selftest and system-run conditions.

During selftest:
The selftest number in progress is displayed in binary. If an error is detected the selftest number in question will be displayed in binary form. If the number is higher than 2 the "diagnostic" LED will flash, and if the number is lower than 2 the "diagnostic" LED will be turned off.
When the selftest is completed the only LED left on is the "diagnostic" which is cleared by the system software.

SYSTEM-RUN:
With "diagnostic" LED off the ongoing activity is indicated by the LEDs RC8000-read, RC8000-write or MBA-access.
With "diagnostic" LED flashing in short intervals an program exception has occured.
With "Diagnostic" LED flashing constant an RC8000 bus-error is detected and the status is displayed as parity, timeout or nack

CONSOLE

A V.24/V.28 interface is provided for console connection, by which the selftest or on-line monitor can be entered.
The console connected must be configured with 8 databits/ character, 1 stopbit and no parity bit. Baudrates from 9600 to 300 can be used. Type "U" once or twice for identifying the baudrate.

4.4 DESKEW DELAY ADJUSTMENT

The deskew delays for DEVSELACK, DATARDY and ACK/NACK are adjustable by means of P1, P2 and P3 on the PCB.

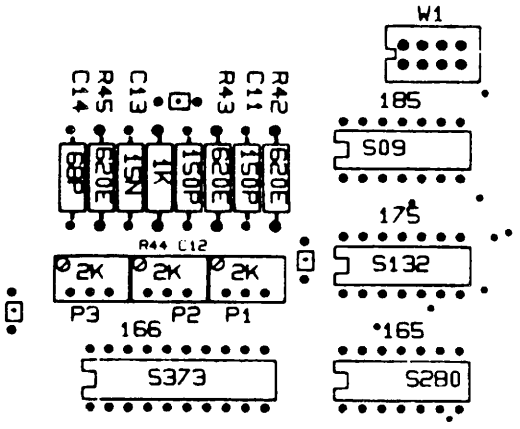


Fig. 6 Potentiometers on the PCB.

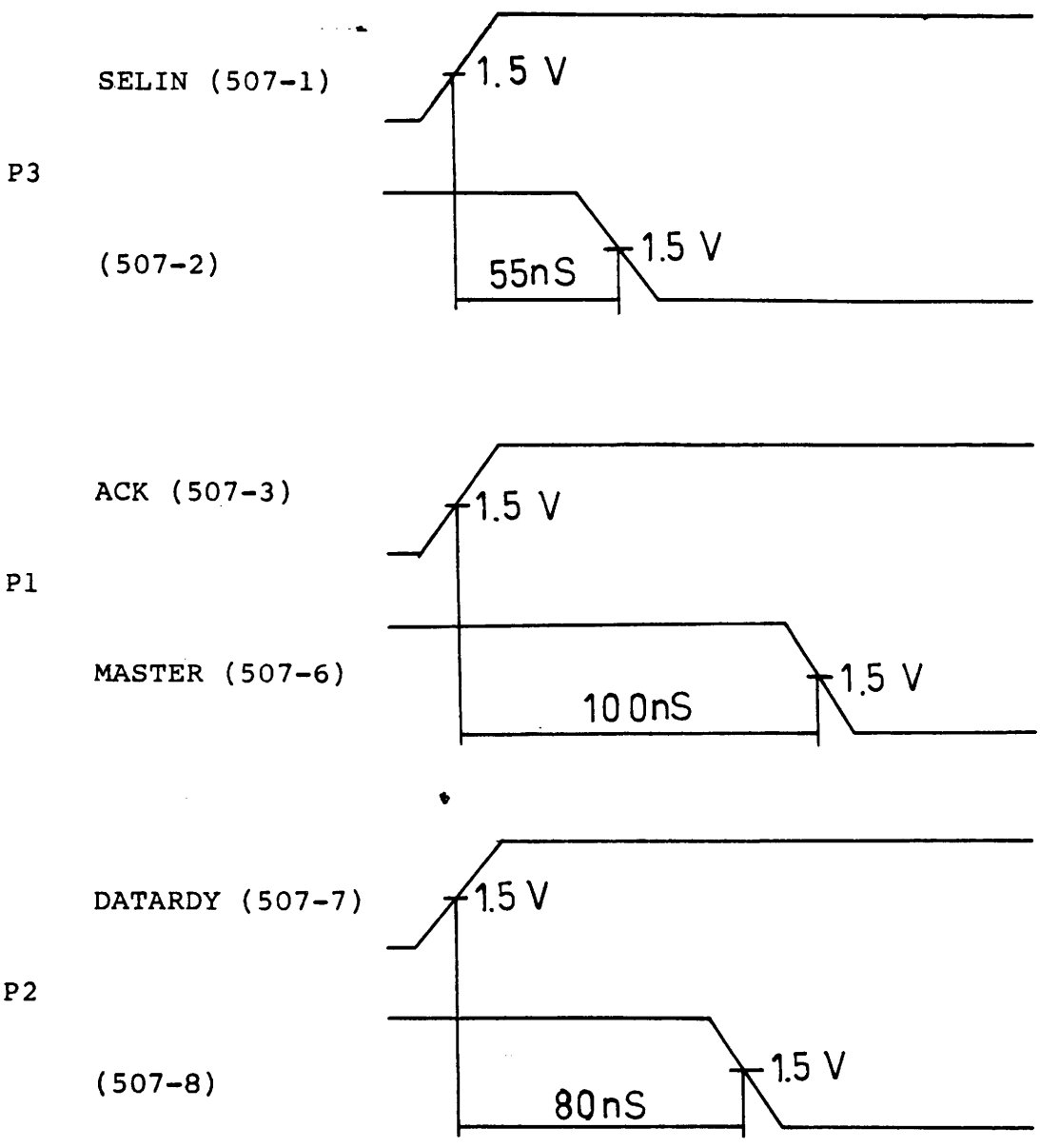
The delays can be adjusted by means of selftest no. 6 which can be started via the console or by activating the adjust switch on the PCB before autoload.

The following procedure is recomended for adjustment of the delays:

1. Turn the potentiometers fully counterclockwise (max. delay)

2. Start the test via the console or via Autoload.

3. Adjust the delays according to the figure below.



5. CHECKOUT

After installation or repair, the functionality must be checked by means of the built-in selftest program.
After power is applied or Autoload-button is depressed, the default part of the selftest is executed. In order to check a greater part of the IFP the extended selftest must be included.
This is done by setting the Testmode switch to continous or by typing <esc> on the terminal, while the selftest is still in progress. In the menu now displayed, you now have to change the default value of "Boot after test" to "N", thereby enabling the extended test.
Let the extended selftest run in loop mode for appr. 1/2 hour.
In order to check the MBA-interface, which can not be done by the selftest, you now have to execute the IFP-TOP test under system for appr. 1/2 hour before the contoller is totally checked.

APPENDIX

Reference number:

1 RCSL 991-10582
IFP802 Hardware Selftest Manual

2 RCSL 991-10584
IFP802 Technical Manual

RETURN LETTER

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Information Department
Lautrupbjerg 1
DK-2750 Ballerup
Denmark