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Title:

MBA 602
Technical Manual

RCSL 42-11592

A/S REGNECENTRALEN
af 1979

Keywords:

MBA 602, IFP 801, Multibus®.

Abstract:

This manual contains technical information including logic diagrams on the MBA 602.

(28 printed pages)

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RCSL 42-i1592

TABLE OF CONTENTS PAGE

1. INTRODUCTION 1.

The MBA 602, Multibus adapter, is the Multibus part of two controllers connecting the RC8000 computer system and the Multibus. Connection to the RC8000 system bus is provided by the IFP 801, interface processor. The MBA 602 and the IFP 801 are interconnected by a flat cable with a maximum length of 12 meters. See figure 1.

The IFP 801 is an iAPX86 microprocessor based controller provided with a multi-port RAM with one port reserved for Multibus access through the MBA 602. The multi-port RAM is used for communication between RC8000 and Multibus units.

The MBA 602 may only act as a slave on the Multibus. A strap field on the MBA 602 allows the multi-port RAM to be divided into a local part and a shared part in 16 K-byte increments. Only the shared part is accessible from the Multibus. The shared part of the multi-port RAM may be located starting at any 16 K-byte boundary within the 1 M-byte address range of the Multibus. Multibus write access to any of the first eight locations of the shared RAM interrupts the iAPX86 processor on the IFP 801.

Under control of the IFP 801 the MBA 602 may generate a non-bus vectored interrupt on any of the eight Multibus interrupt lines. The interrupt is cleared by an I/O write command.

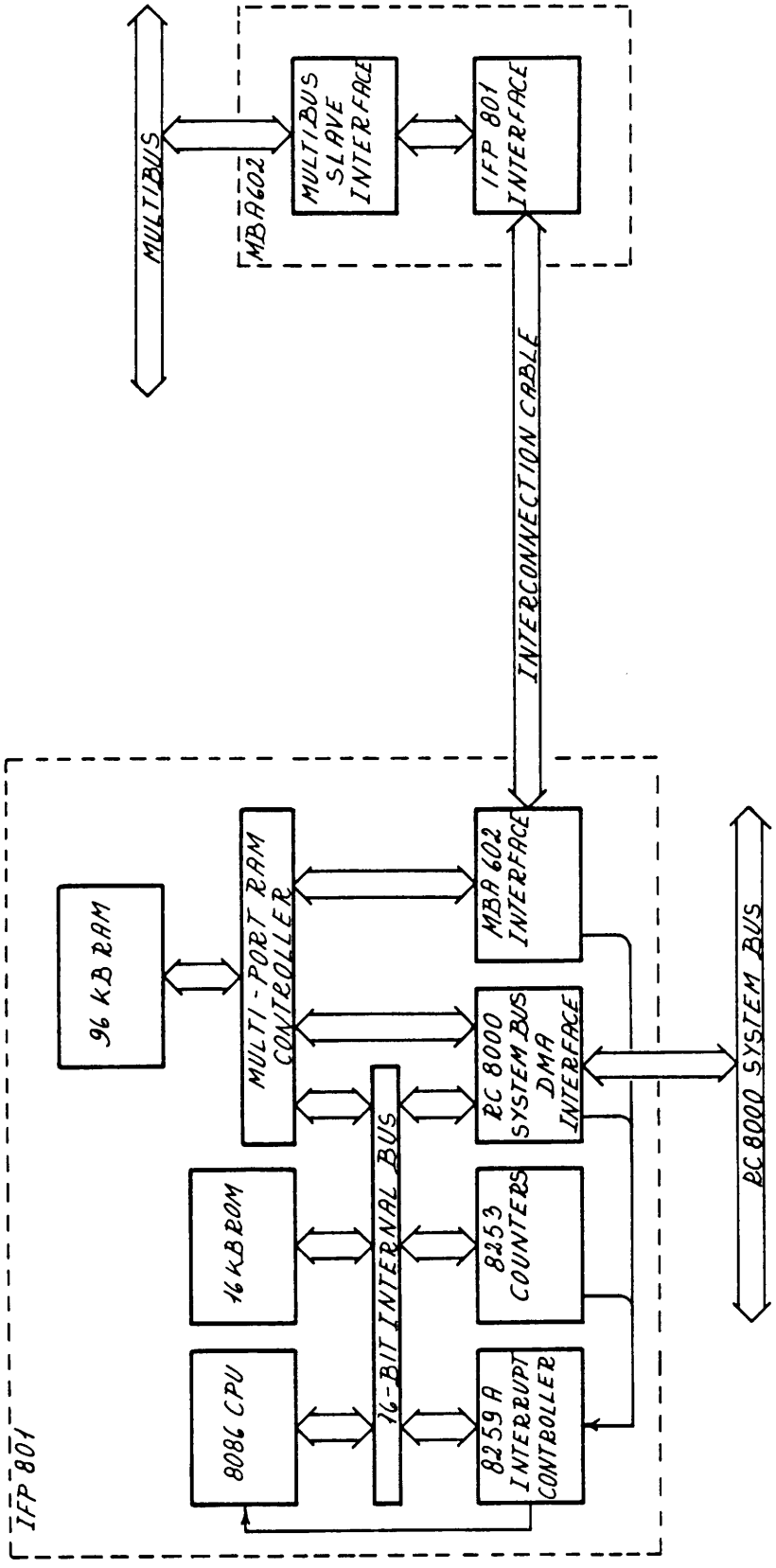
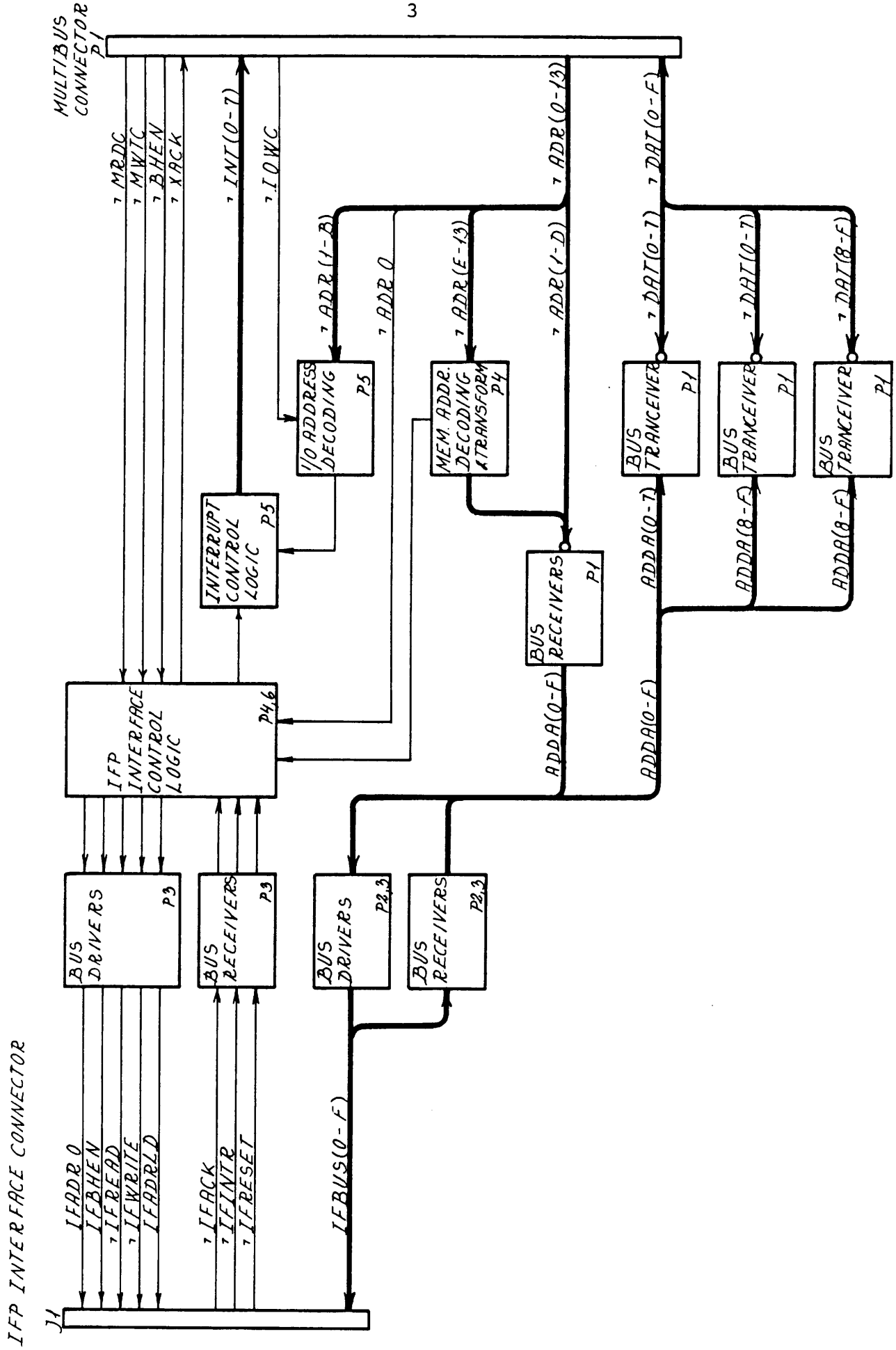


Figure 1: RC8000 System Bus Interface to Multibus.

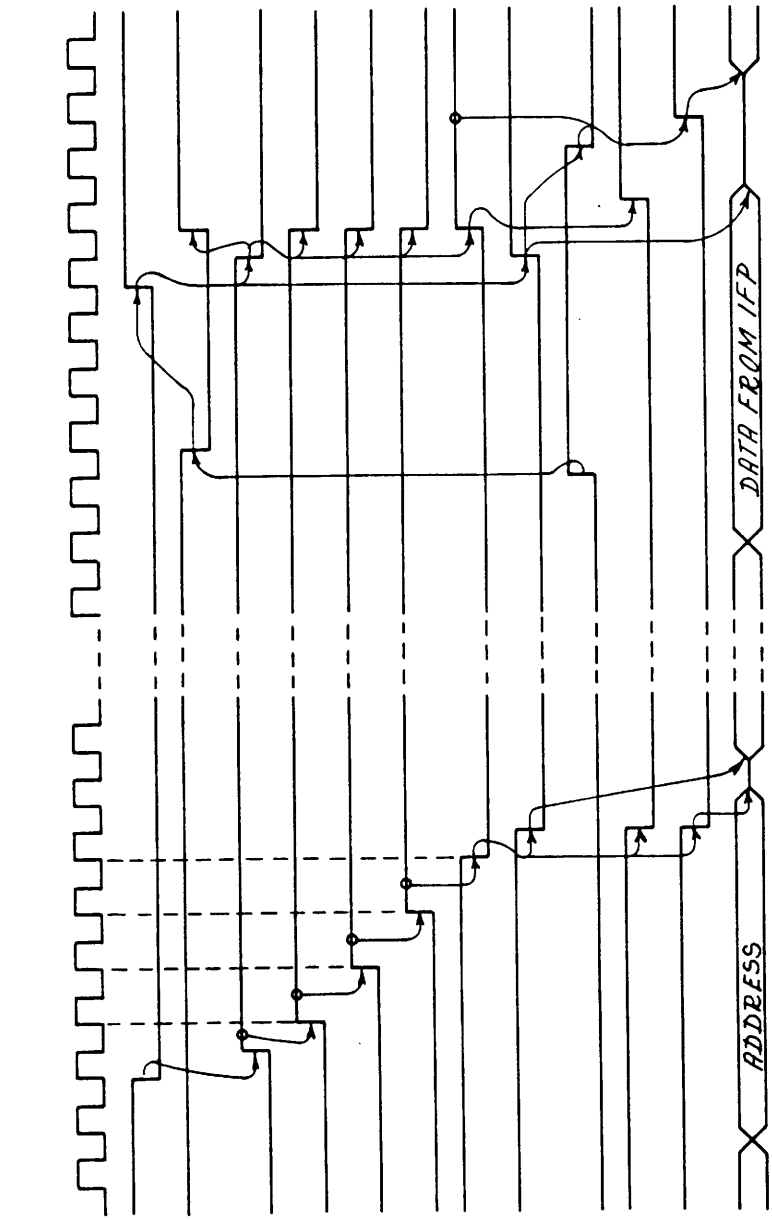


AHJ 810805 AGA 810825

MBA 602
R 13242

MBA 602 MULTIBUS ADAPTER
BLOCK DIAGRAM

8108 14 ARJ 810826 HGA

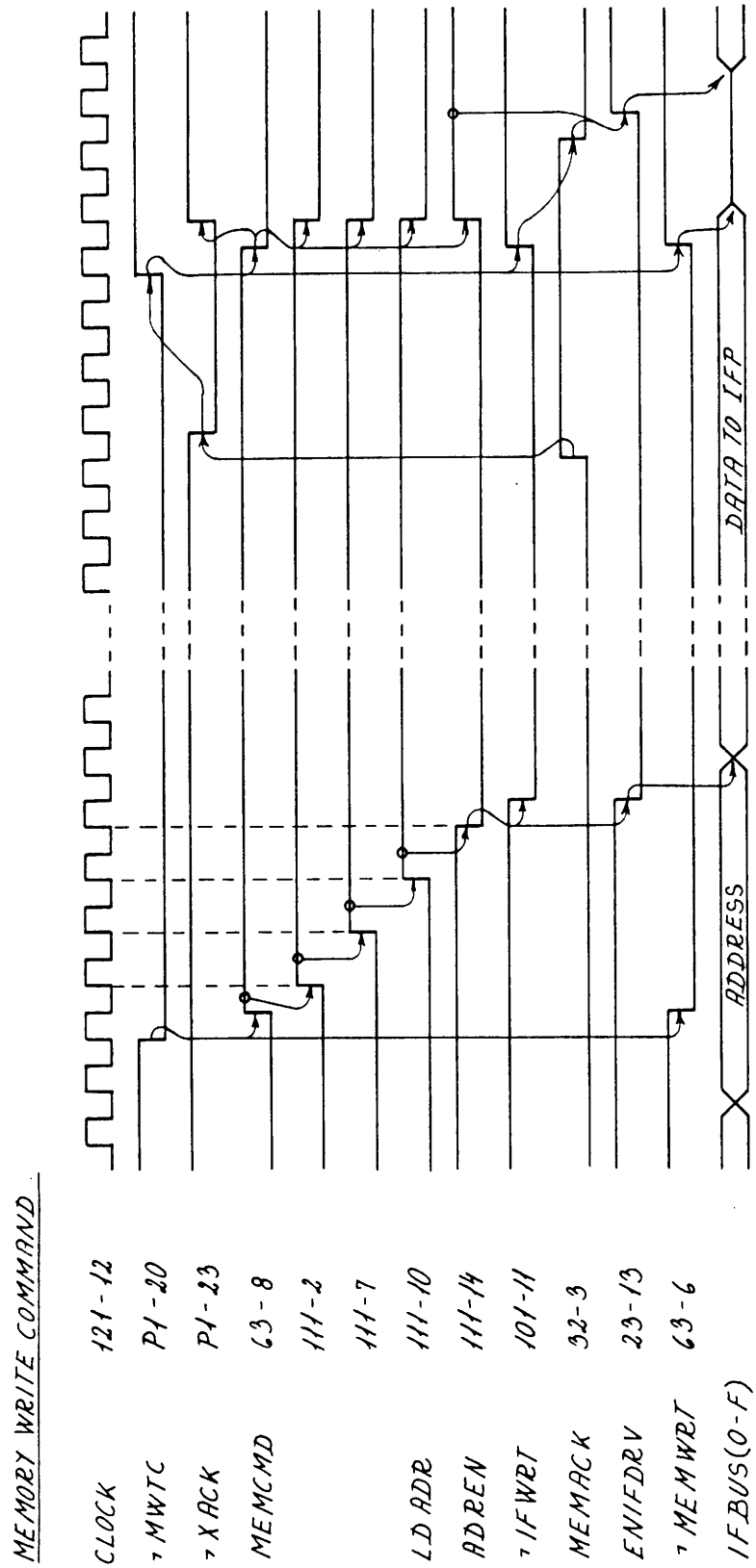


MBA 602

R 13240

MULTIBUS READ ACCESS TO IFP MULTIPORT MEMORY

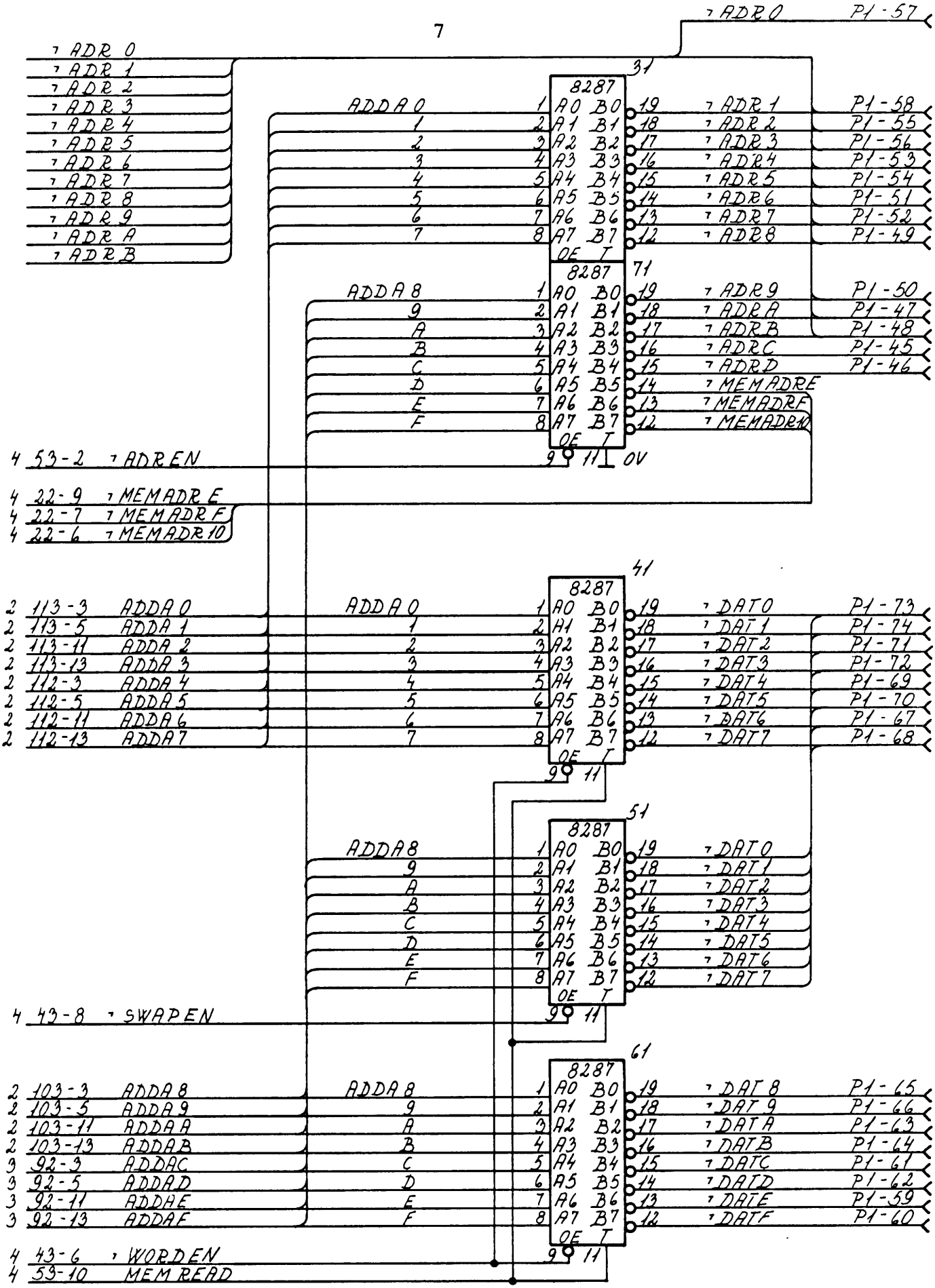
AAJ 810814 AGA 810825



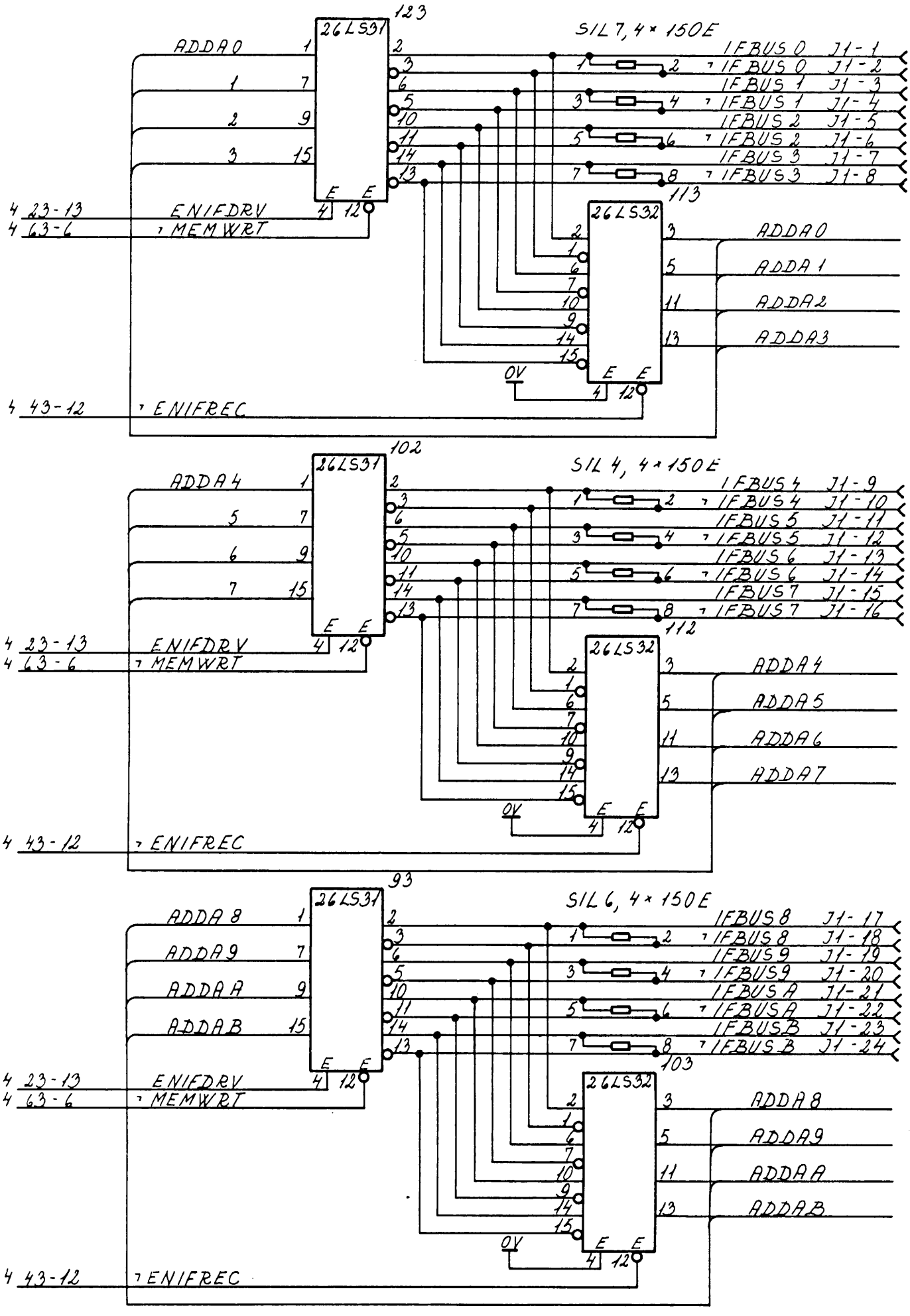
MBA602
R 13241

MULTIBUS WRITE ACCESS TO IFP MULTIPORT MEMORY

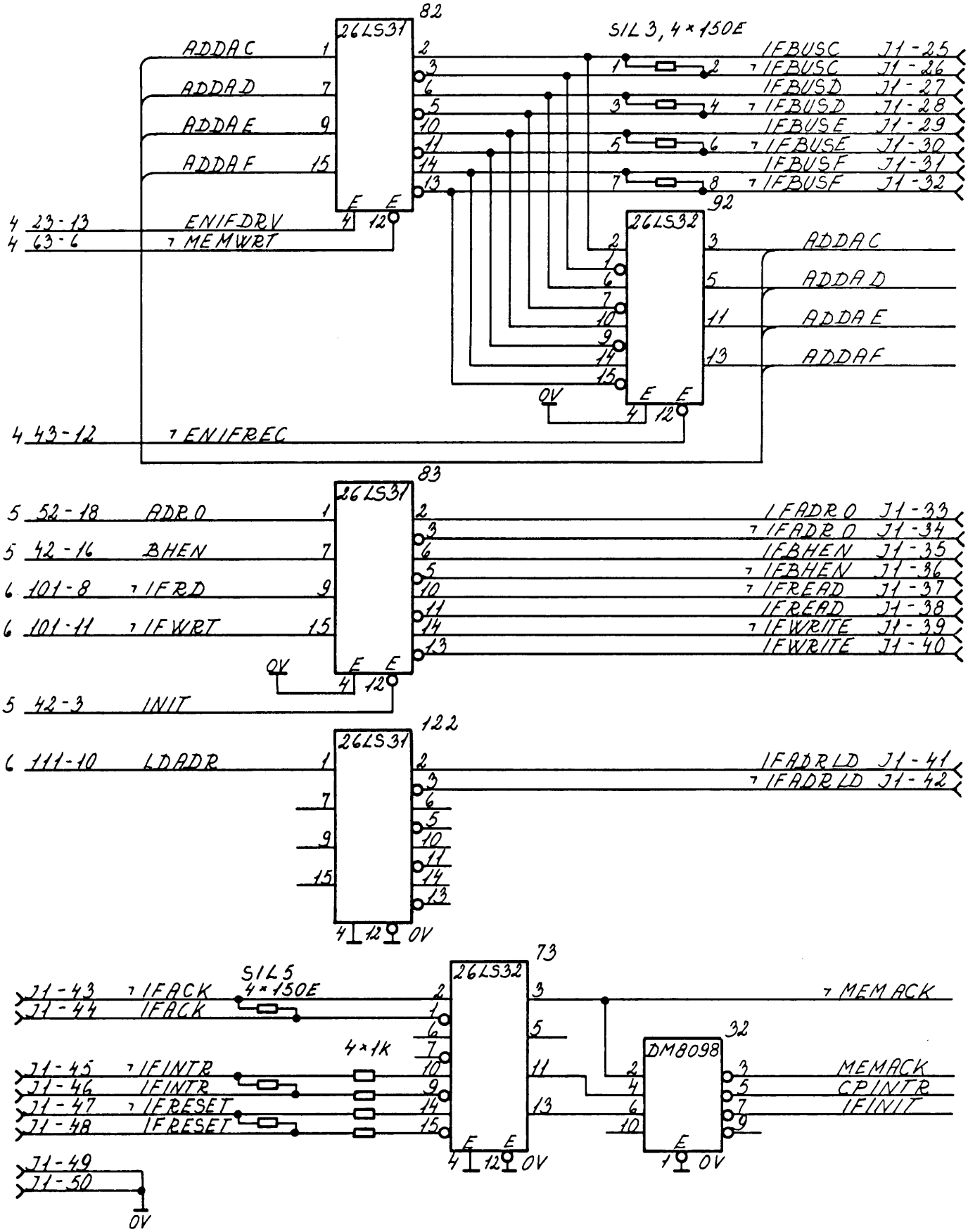
Signal	Destination	Description
-,ADR(0-B)	5	Address signals from Multibus.
ADDA(0-B)	2	Bidirectional, Multiplexed address/data tri-state bus, connecting Multibus drivers/ receivers and IFP interface bus drivers/receivers.
ADDA(C-F)	3	


7 ADR 0
7 ADR 1
7 ADR 2
7 ADR 3
7 ADR 4
7 ADR 5
7 ADR 6
7 ADR 7
7 ADR 8
7 ADR 9
7 ADR A
7 ADR B
7 ADR 0 P1-57
31
8287
ADDA 0
0 A0 B0 19 7 ADR 1 P1-58
1 A1 B1 18 7 ADR 2 P1-55
2 A2 B2 17 7 ADR 3 P1-56
3 A3 B3 16 7 ADR 4 P1-53
4 A4 B4 15 7 ADR 5 P1-54
5 A5 B5 14 7 ADR 6 P1-51
6 A6 B6 13 7 ADR 7 P1-52
7 A7 B7 12 7 ADR 8 P1-49
OE T
71
8287
ADDA 8
8 A0 B0 19 7 ADR 9 P1-50
9 A1 B1 18 7 ADR A P1-47
A A2 B2 17 7 ADR B P1-48
B A3 B3 16 7 ADR C P1-45
C A4 B4 15 7 ADR D P1-46
D A5 B5 14 7 MEMADRE
E A6 B6 13 7 MEMADRF
F A7 B7 12 7 MEMADR10
OE T
9 11 OV
4 53-2 7 ADREN
4 22-9 7 MEMADR E
4 22-7 7 MEMADR F
4 22-6 7 MEMADR 10
41
8287
2 113-3 ADDA 0
2 113-5 ADDA 1
2 113-11 ADDA 2
2 113-13 ADDA 3
2 112-3 ADDA 4
2 112-5 ADDA 5
2 112-11 ADDA 6
2 112-13 ADDA 7
ADDA 0
0 A0 B0 19 7 DAT 0 P1-73
1 A1 B1 18 7 DAT 1 P1-74
2 A2 B2 17 7 DAT 2 P1-71
3 A3 B3 16 7 DAT 3 P1-72
4 A4 B4 15 7 DAT 4 P1-69
5 A5 B5 14 7 DAT 5 P1-70
6 A6 B6 13 7 DAT 6 P1-67
7 A7 B7 12 7 DAT 7 P1-68
OE T
9 11
51
8287
ADDA 8
8 A0 B0 19 7 DAT 0
9 A1 B1 18 7 DAT 1
A A2 B2 17 7 DAT 2
B A3 B3 16 7 DAT 3
C A4 B4 15 7 DAT 4
D A5 B5 14 7 DAT 5
E A6 B6 13 7 DAT 6
F A7 B7 12 7 DAT 7
OE T
9 11
4 43-8 7 SWAPEN
61
8287
2 103-3 ADDA 8
2 103-5 ADDA 9
2 103-11 ADDA A
2 103-13 ADDA B
3 92-3 ADDA C
3 92-5 ADDA D
3 92-11 ADDA E
3 92-13 ADDA F
ADDA 8
8 A0 B0 19 7 DAT 8 P1-65
9 A1 B1 18 7 DAT 9 P1-66
A A2 B2 17 7 DAT A P1-63
B A3 B3 16 7 DAT B P1-64
C A4 B4 15 7 DAT C P1-61
D A5 B5 14 7 DAT D P1-62
E A6 B6 13 7 DAT E P1-59
F A7 B7 12 7 DAT F P1-60
OE T
9 11
4 43-6 7 WORDEN
4 59-10 MEM READ

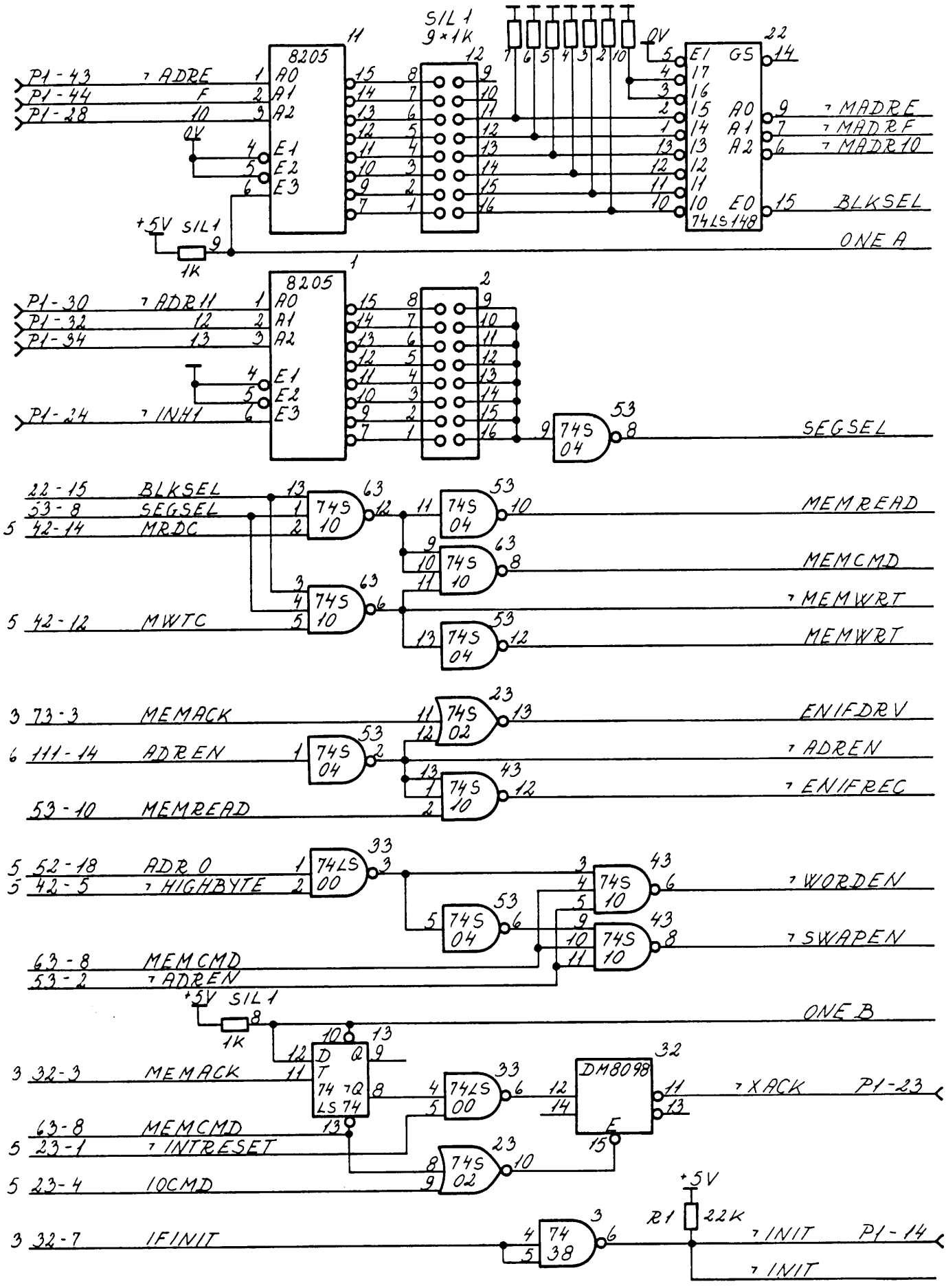
Signal	Destination	Description
IFBUS (0-B) -,IFBUS(0-B)		Bidirectional, multiplexed address/ data tri-state bus, which connects the MBA 602 and the IFP 801. Differential mode signals.
ADDA(0-B)	1	Bidirectional, multiplexed address/ data tri-state bus, connecting Multibus drivers/receivers and IFP interface drivers/receivers.


123
26LS31
ADDA0
ADDA1
ADDA2
ADDA3
4 23-13 ENIFDRV
4 63-6 ↑MEMWRT
4 43-12 ↑ENIFREC
SIL 7, 4 × 150E
IFBUS 0 J1-1
↑IFBUS 0 J1-2
IFBUS 1 J1-3
↑IFBUS 1 J1-4
IFBUS 2 J1-5
↑IFBUS 2 J1-6
IFBUS 3 J1-7
↑IFBUS 3 J1-8
113
26LS32
ADDA0
ADDA1
ADDA2
ADDA3
0V
102
26LS31
ADDA4
ADDA5
ADDA6
ADDA7
4 23-13 ENIFDRV
4 63-6 ↑MEMWRT
4 43-12 ↑ENIFREC
SIL 4, 4 × 150E
IFBUS 4 J1-9
↑IFBUS 4 J1-10
IFBUS 5 J1-11
↑IFBUS 5 J1-12
IFBUS 6 J1-13
↑IFBUS 6 J1-14
IFBUS 7 J1-15
↑IFBUS 7 J1-16
112
26LS32
ADDA4
ADDA5
ADDA6
ADDA7
0V
93
26LS31
ADDA8
ADDA9
ADDAA
ADDAB
4 23-13 ENIFDRV
4 63-6 ↑MEMWRT
4 43-12 ↑ENIFREC
SIL 6, 4 × 150E
IFBUS 8 J1-17
↑IFBUS 8 J1-18
IFBUS 9 J1-19
↑IFBUS 9 J1-20
IFBUS A J1-21
↑IFBUS A J1-22
IFBUS B J1-23
↑IFBUS B J1-24
103
26LS32
ADDA8
ADDA9
ADDAA
ADDAB
0V

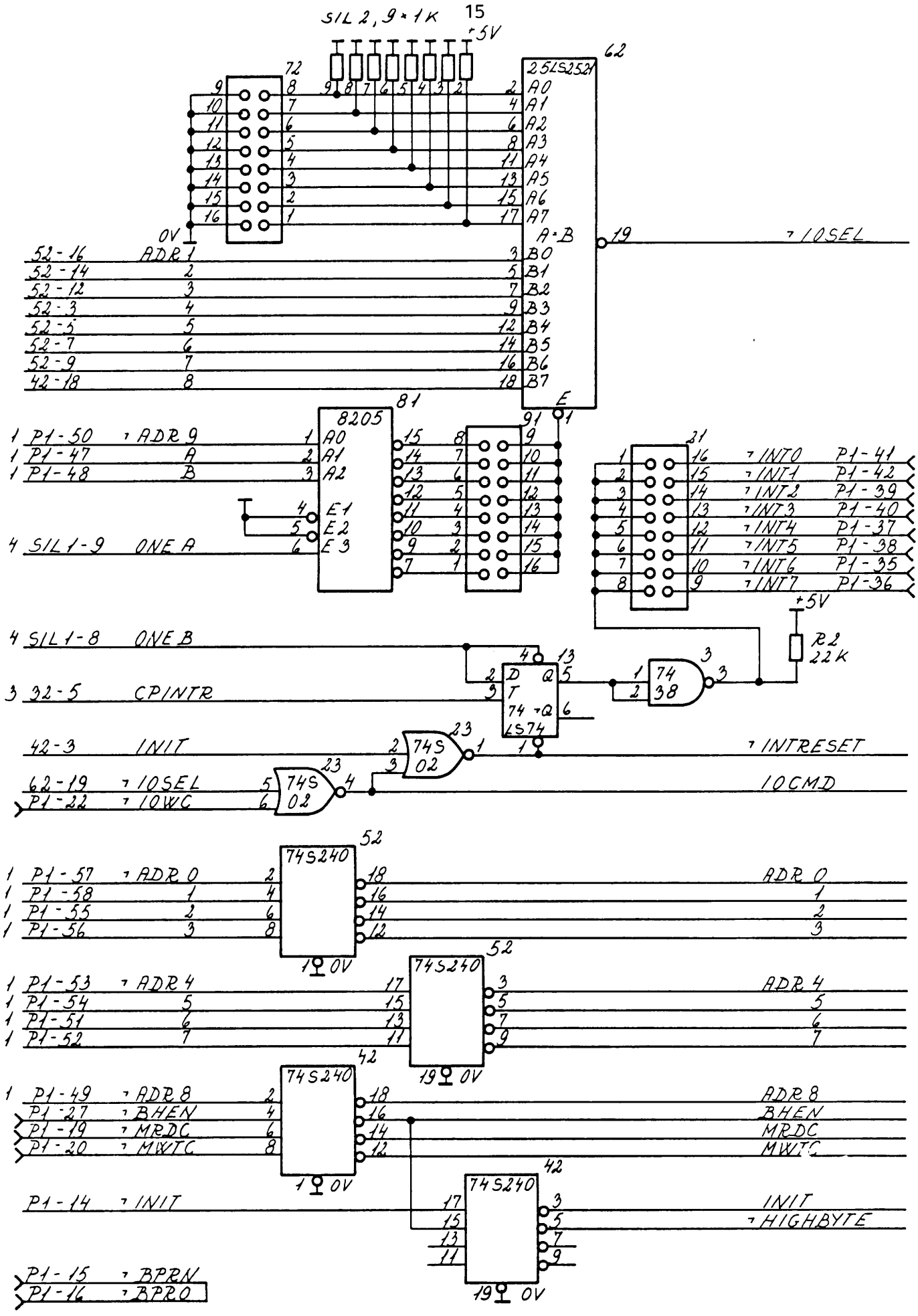
Signal	Destination	Description
IFBUS(C-F) -,IFBUS(C-F)		Bidirectional, multiplexed address/ data tri-state bus, which connects the MBA 602 and the IFP 801. Differential mode signals.
ADDA(C-F)	1	Bidirectional, multiplexed address/ data tri-state bus, connecting Multibus drivers/receivers and IFP interface drivers/receivers.
IFADR0 -,IFADR0		Least significant address bit to IFP 801.
IFBHEN -,IFBHEN		IFBHEN and IFADR0 control byte/word accesses to/from IFP memory.
-,IFREAD IFREAD		Memory read command to IFP.
-,IFWRITE IFWRITE		Memory write command to IFP.
IFADRLD -,IFADRLD		Control signal to IFP indicating that an address is available on the IFBUS.
-,MEMACK MEMACK	3,6 4	Response from IFP indicating that a read or write operation is complete.
CPINTR	5	Sets the Multibus interrupt flip-flop.
IFINIT	4	Reset signal from IFP controlling the -,INIT signal on the Multibus.


82
26LS31
ADDAC
ADDAD
ADDAE
ADDAF
ENIFDRV
MEMWRT
SIL 3, 4 × 150E
IFBUSC J1-25
IFBUSC J1-26
IFBUSD J1-27
IFBUSD J1-28
IFBUSE J1-29
IFBUSE J1-30
IFBUSF J1-31
IFBUSF J1-32
92
26LS32
ADDAC
ADDAD
ADDAE
ADDAF
ENIFREC
83
ADR0
BHEN
IFRD
IFWRT
INIT
IFADR0 J1-33
IFADR0 J1-34
IFBHEN J1-35
IFBHEN J1-36
IFREAD J1-37
IFREAD J1-38
IFWRITE J1-39
IFWRITE J1-40
122
LDADR
IFADRLD J1-41
IFADRLD J1-42
73
SIL5
4 × 150E
4 × 1k
J1-43 IFACK
J1-44 IFACK
J1-45 IFINTR
J1-46 IFINTR
J1-47 IFRESET
J1-48 IFRESET
J1-49
J1-50
MEMACK
32
DM8098
MEMACK
CPINTR
IFINIT

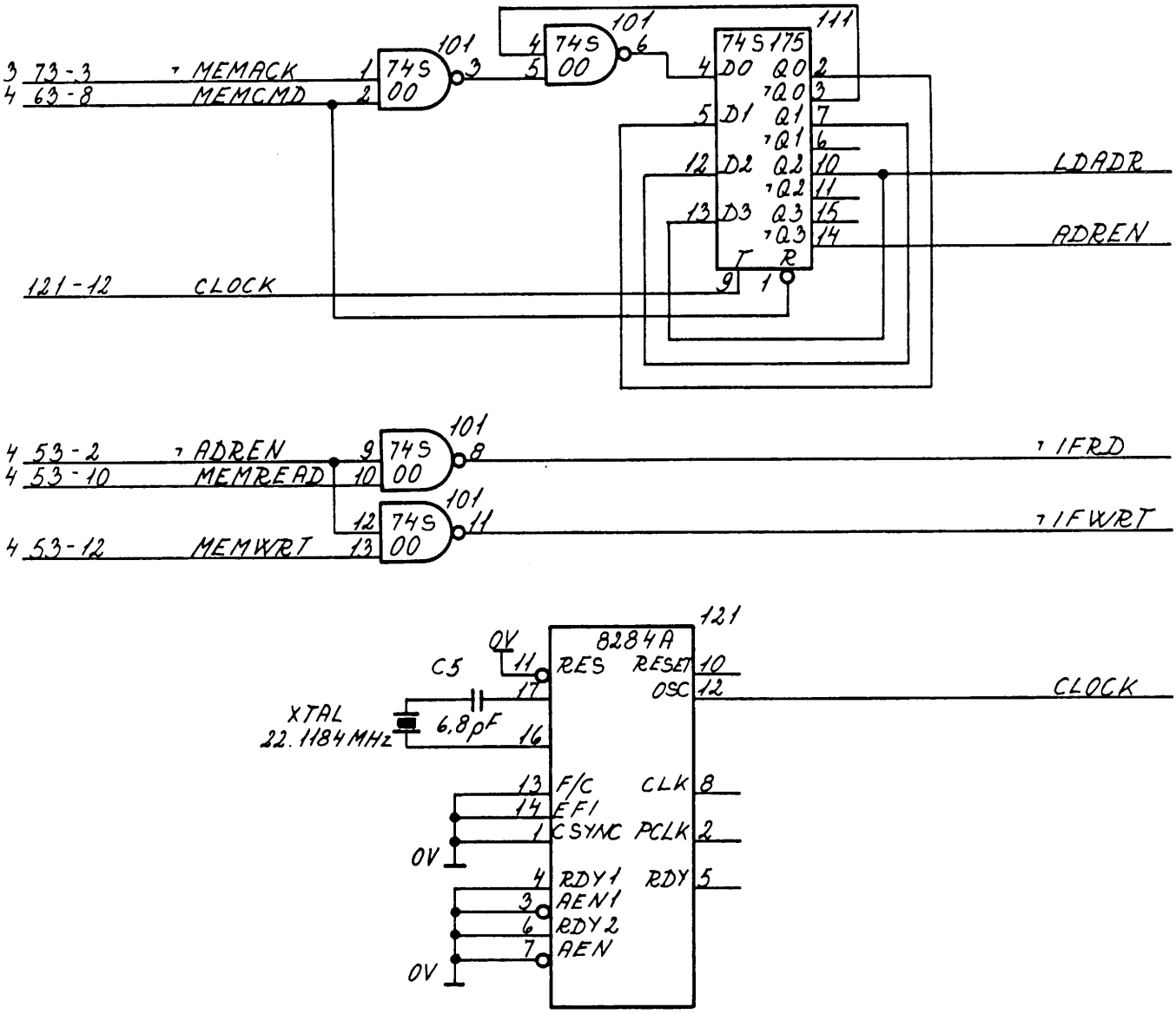
Signal	Destination	Description
-,MADR(E-10)	1	Three most significant bits of the memory address. Generated by the address transformation logic.
BLKSEL	4	Indicates that one of the visible 16 kbyte memory blocks is addressed.
ONEA	4,5	Logic one for unused inputs.
SEGSEL	4	Indicates that the address is within the selected 128 K byte segment.
MEMREAD	1,4,6	A memory read command is received and the address is within the decoded range.
MEMCMD	6	MEMCMD = MEMREAD or MEMWRT.
-,MEMWRT MEMWRT	2,3,4 6	A memory write command is received and the address is within the decoded range.
ENIFDRV	2,3	Enable signal for the IFBUS line drivers.
-,ADREN	1,4,6	Enable signal for Multibus address line receivers.
-,ENIFREC	2,3	Enable signal for the IFBUS line receivers.
-,WORDEN	1	Enable signal for Multibus data tranceiver.
-,SWAPEN	1	Enable signal for the Multibus swap byte data tranceiver.
ONEB	4,5	Logic one for unused inputs.
-,XACK		Control signal to Multibus indicating that a read or write operation is complete.
-,INIT	5	Reset signal to/from Multibus.


SIL 1
9×1K
8205
74S 10
74S 04
74S 02
74LS 00
74LS 148
DM8098
74 38
P1-43
P1-44
P1-28
P1-30
P1-32
P1-34
P1-24
ADRE
ADR11
INH1
MADRE
MADRF
MADR10
BLKSEL
ONE A
SEGSEL
MEMREAD
MEMCMD
MEMWRT
MWTC
MEMACK
ADREN
ENIFDRV
ENIFREC
MEMREAD
ADR 0
HIGHBYTE
WORDEN
SWAPEN
MEMCMD
ONE B
MEMACK
INTRESET
IOCMD
IFINIT
XACK
P1-23
INIT
P1-14
R1 22K
+5V

Signal	Destination	Description
-,IOSEL	5	Output from I/O address decoder.
-,INT(0-7)		Interrupt request signals to Multibus.
-,INTRESET	4,5	Reset signal for interrupt request flip-flop.
IOCMD	4,5	An I/O write command is received and the unit is addressed.
ADR0	3,4	Least significant address signal received from Multibus.
ADR(1-8)	5	Address signals received from Multibus.
BHEN	3,5	Byte control signal from Multibus.
MRDC	4	Memory read command from Multibus.
MWTC	4	Memory write command from Multibus.
INIT	3,5	Reset signal from Multibus.
-,HIGHBYTE	4	Byte control signal from Multibus.


SIL 2,9 * 1K
15
+5V
72
25LS251
62
A0
A1
A2
A3
A4
A5
A6
A7
0V
A*B
19
~IOSEL
52-16 ADR 1
52-14 2
52-12 3
52-3 4
52-5 5
52-7 6
52-9 7
42-18 8
B0
B1
B2
B3
B4
B5
B6
B7
81
8205
E
91
1 P1-50 ~ADR 9
1 P1-47 A
1 P1-48 B
4 SIL 1-9 ONE A
E1
E2
E3
31
~INT0 P1-41
~INT1 P1-42
~INT2 P1-39
~INT3 P1-40
~INT4 P1-37
~INT5 P1-38
~INT6 P1-35
~INT7 P1-36
+5V
R2
22K
4 SIL 1-8 ONE B
3 32-5 CP INTR
D
T
74 ~Q
LS74
74
38
42-3 INIT
74S
02
23
~INTRESET
62-19 ~IOSEL
P1-22 ~IOWC
IOCMD
52
74S240
1 P1-57 ~ADR 0
1 P1-58 1
1 P1-55 2
1 P1-56 3
ADR 0
1
2
3
1 P1-53 ~ADR 4
1 P1-54 5
1 P1-51 6
1 P1-52 7
ADR 4
5
6
7
42
1 P1-49 ~ADR 8
P1-27 ~BHEN
P1-19 ~MRDC
P1-20 ~MWTC
ADR 8
BHEN
MRDC
MWTC
P1-14 ~INIT
INIT
~HIGHBYTE
P1-15 ~BPRN
P1-16 ~BPRO
0V
19

Signal	Destination	Description
LDADR	3,6	Control signal indicating that an address is available on the IFBUS.
ADREN	4	Controls multiplexing of address and data.
-,IFRD	3	Memory read command to IFP. Indicates also that the IFBUS is available for transfer of data from the IFP to the MBA.
-,IFWRT	3	Memory write command to IFP. Indicates also that data is available on the IFBUS:
CLOCK	6	22.1184 MHz clock for logic controlling transfer of address and data between IFP and MBA.


3 73-3
4 63-8
MEMACK
MEMCMD
101
74S 00
74S175
DO Q0
D1 Q1
D2 Q2
D3 Q3
LDADR
ADREN
121-12
CLOCK
4 53-2
4 53-10
ADREN
MEMREAD
4 53-12
MEMWRT
IFRD
IFWRT

121
8284A
C5
6.8pF
XTAL
22.1184MHz
RES
RESET
OSC
CLOCK
F/C
EFI
CSYNC
CLK
PCLK
RDY1
AEN1
RDY2
AEN
RDY
0V

P1: MULTIBUS CONNECTOR

COMPONENT SIDE			CIRCUIT SIDE		
PIN	SOURCE	MNEMONIC	PIN	SOURCE	MNEMONIC
1		0V	2		0V
3		+5V	4		+5V
5		+5V	6		+5V
7	1)	+12V	8	1)	+12V
9	1)	-5V	10	1)	-5V
11		0V	12		0V
13	1)	-,BCLK	14	3-6	-,INIT
15		-,BPRN	16	P1-15	-,BPRO
17	1)	-,BUSY	18	1)	-,BREQ
19		-,MRDC	20		-,MWTC
21	1)	-,IORC	22		-,IOWC
23	32-11	-,XACK	24		-,INH1
25	1)	Reserved	26	1)	-,INH2
27		-,BHEN	28		-,AD10
29	1)	-,CBRQ	30		-,AD11
31	1)	-,CCLK	32		-,AD12
33	1)	-,INTA	34		-,AD13
35	21-10	-,INT6	36	21-9	-,INT7
37	21-12	-,INT4	38	21-11	-,INT5
39	21-14	-,INT2	40	21-13	-,INT3
41	21-16	-,INT0	42	21-15	-,INT1
43		-,ADRE	44		-,ADRF
45		-,ADRC	46		-,ADRD
47		-,ADRA	48		-,ADRB
49		-,ADR8	50		-,ADR9
51		-,ADR6	52		-,ADR7
53		-,ADR4	54		-,ADR5
55		-,ADR2	56		-,ADR3
57		-,ADR0	58		-,ADR1
59	61-13	-,DATE	60	61-12	-,DATF
61	61-15	-,DATC	62	61-14	-,DATD
63	61-17	-,DATA	64	61-16	-,DATB
65	61-19	-,DAT8	66	61-18	-,DAT9
67	41-13, 51-13	-,DAT6	68	41-12, 51-12	-,DAT7
69	41-15, 51-15	-,DAT4	70	41-14, 51-14	-,DAT5
71	41-17, 51-17	-,DAT2	72	41-16, 51-16	-,DAT3
73	41-19, 51-19	-,DAT0	74	41-18, 51-18	-,DAT1
75		0V	76		0V
77	1)	Reserved	78	1)	Reserved
79	1)	-12V	80	1)	-12V
81		+5V	82		+5V
83		+5V	84		+5V
85		0V	86		0V

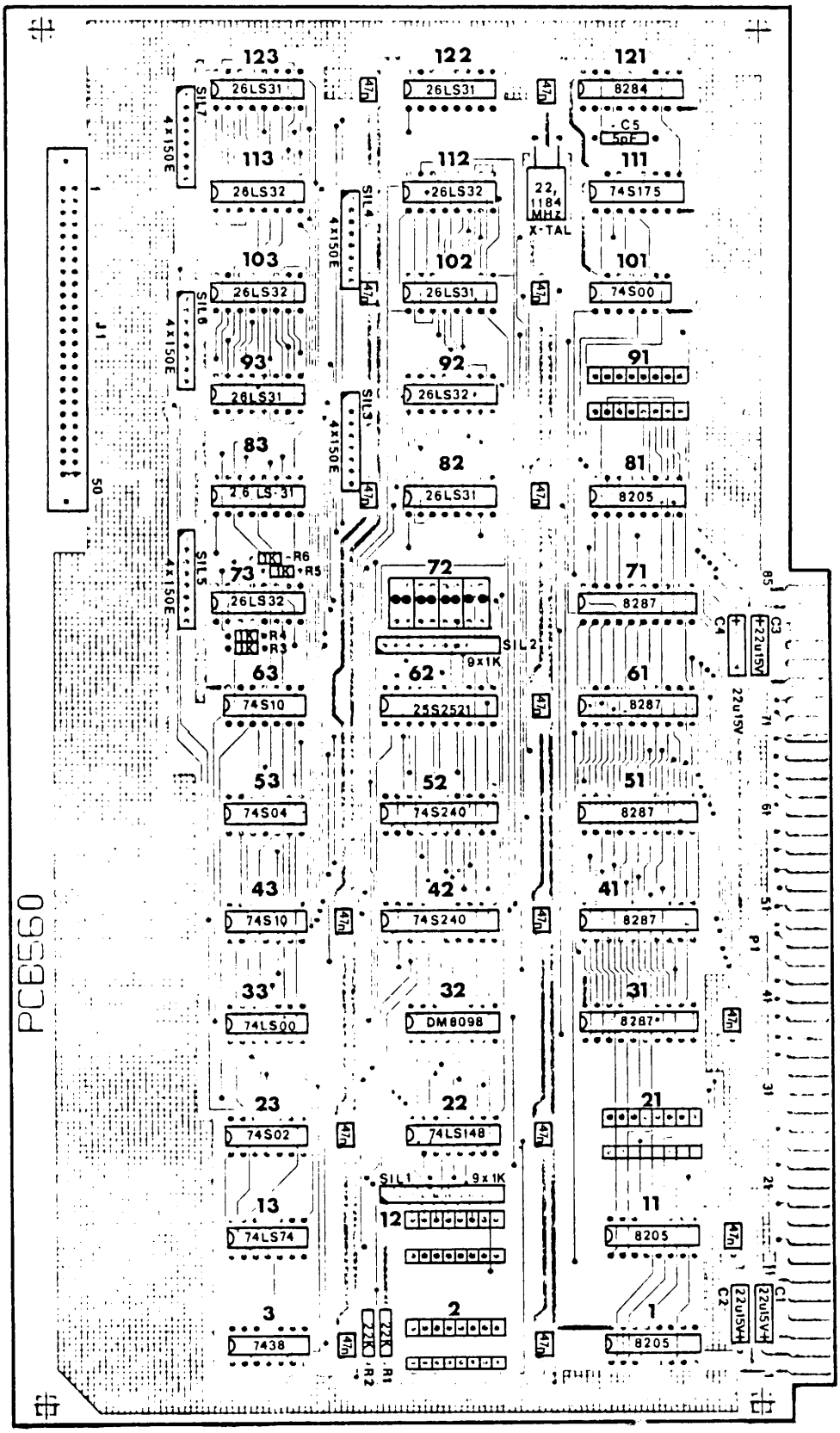
1: The signal is not used on this board.

P1: IFP INTERFACE CONNECTOR

PIN	SOURCE	MNEMONIC	PIN	SOURCE	MNEMONIC
1	123-2	IFBUS0	2	123-3	-, IFBUS0
3	123-6	IFBUS1	4	123-5	-, IFBUS1
5	123-10	IFBUS2	6	123-11	-, IFBUS2
7	123-14	IFBUS3	8	123-13	-, IFBUS3
9	102-2	IFBUS4	10	102-3	-, IFBUS4
11	102-6	IFBUS5	12	102-5	-, IFBUS5
13	102-10	IFBUS6	14	102-11	-, IFBUS6
15	102-14	IFBUS7	16	102-13	-, IFBUS7
17	93-2	IFBUS8	18	93-3	-, IFBUS8
19	93-6	IFBUS9	20	93-5	-, IFBUS9
21	93-10	IFBUSA	22	93-11	-, IFBUSA
23	93-14	IFBUSB	24	93-13	-, IFBUSB
25	82-2	IFBUSC	26	82-3	-, IFBUSC
27	82-6	IFBUSD	28	82-5	-, IFBUSD
29	82-10	IFBUSE	30	82-11	-, IFBUSE
31	82-14	IFBUSF	32	82-13	-, IFBUSF
33	83-2	IFADR0	34	83-3	-, IFADR0
35	83-6	IFBHEN	36	83-5	-, IFBHEN
37	83-10	-, IFREAD	38	83-11	IFREAD
39	83-14	-, IFWRITE	40	83-13	IFWRITE
41	122-2	IFADRLD	42	122-3	-, IFADRLD
43		-, IFACK	44		IFACK
45		-, IFINTR	46		IFINTR
47		-, IFRESET	48		IFRESET
49		GROUND	50		GROUND

COMPONENT LIST

REFERENCE	DESCRIPTION	QTY
U1, U11, U81	P3205	3
U3	SN7438N	1
U13	SN74LS74N	1
U22	SN74LS148N	1
U23	SN74S02N	1
U31, U41, U51, U61, U71	8287	5
U32	DM8098N	1
U33	SN74LS00N	1
U42, U52	SN74S240N	2
U43, U63	SN74S10N	2
U53	SN74S04N	1
U62	AM25LS2521PC	1
U73, U92, U103, U112, U113	AM26LS32PC	5
U82, U83, U93, U102, U122, U123	AM26LS31PC	6
U101	SN74S00N	1
U111	SN74S175N	1
U121	P8284A	1
U72	Switch, 8 position DIP	1
C1-4	Capacitor, tantal, 22 µF, 15 V	4
C5	Capacitor, 6.8 pF	1
+5 V decoupling	Capacitor, 47nF, 16V	16
R1-2	Resistor, 22 Kohm, 1/8W	2
R3-6	Resistor, 1 Kohm, 1/20W	4
SIL1-2	Resistor network, 9x1 Kohm	2
SIL3-7	Resistor network, 4x150 ohm	5
XTAL	Crystal, 22.1184 MHz	1



Pos 2: Memory segment address selection.

Pos 12: Memory address transformation.

Pos 21: Interrupt line selection.

Pos 72, 91: I/O address selection.

MBA 602

Assembly drawing

RETURN LETTER

Title: MBA 602, Technical Manual RCSI. No.: 30-M295

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