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Title:

CPU820 GENERAL INFORMATION

RCSL 42-11592

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1. GENERAL DESCRIPTION 1.

CPU820 is the basic processing unit for a number of RC8000 models including Model 50 and Model 55. The performance of the basic processing unit may be greatly enhanced through cache memory and floating point hardware extensions.

A cache memory (CAM801 or equivalent) gives an overall CPU performance improvement of 2-3 times. The floating point unit reduces execution times for floating point instructions up to approximately 5 times.

CPU820 is a microprogrammed processor with the microprogram stored in a control store composed of fast bipolar programmable read only memories, PROM's. In addition to the microcode for implementation of the RC8000 instruction set the control store contain comprehensive diagnostic routines for test of the CPU itself, the main memory and the cache memory.

The System Bus, which is an asynchronous unified bus, interconnects the processing unit, the main memory and the peripheral device controllers.

One bus cycle of the System Bus transfers:

23 address bits + 1 parity bit and
24 data bits + 3 parity bits.

2. SPECIFICATIONS

2.1 Performance Specifications

Instruction times	see section 2.5
Microinstruction times	variable, 150-300 nS.
Microinstruction	47 bits + 1 parity bit
Control store	
type	bipolar PROM
capacity	4096 words x 48 bits
Interrupt levels	
internal	8
external	56 (for device interrupts)
Real time clock	
resolution	0.1 mS.
stability	better than 4 S./24 hours
Interval timer	interrupt every 25.6 mS.

2.2 Electrical Specifications

Supply voltages	+5 VDC $\pm$ 5%, 30A
	+12 VDC $\pm$ 5%, 0.05A
	-12 VDC $\pm$ 5%, 0.05A

2.3 Environmental Specifications

Ambient temperature	10-35° C
Relative humidity	20-80% without condensation
Heat dissipation	151 watts

2.4 Physical Specifications

Space requirements	2 slots in a RC8000 CPU chassis
Weight	CPU821: 1.2 kg.
	CPU822: 1.0 kg.

2.5 Instruction Execution Times 2.5

Due to the asynchronous nature of CPU, System Bus and main memory, a number of factors, such as System Bus load, System Bus length, memory access time and the like, influence the instruction execution times. The listed approximately instruction times are based on the following assumptions:

Main memory : MEM805 or equivalent.
Cache memory: CAM801, CAM803 or equivalent.
Normal instruction execution (no exceptions).
Not excape mode.
System Bus not used by other units.
Instruction times for CPU820 with cache imply that both instruction and operands are fetched from the cache.

The instruction times include the following address calculations: direct, relative, indexed and combinations of these. Times for other address calculations are listed separately.

INSTRUCTION	INSTRUCTION TIMES IN MICROSECONDS	
	CPU820 with cache	CPU820 without cache
AM	0.50	1.1
AL	0.35	1.1
AC	0.50	1.1
HL	1.0	2.35
HS	2.3	3.60
RL	0.5	2.0
RS	1.55	2.0
RX	1.90	3.25
DL	1.05	3.30
DS	3.00	3.45
XL	1.15	2.50
XS	2.45	3.60

INSTRUCTION	INSTRUCTION TIMES IN MICROSECONDS	
	CPU820 with cache	CPU820 without cache
ZL	0.9	2.40
EL	0.85	2.35
EA	1.05	2.40
ES	1.05	2.40
WA	0.7	2.2
WS	0.7	2.2
WM	5.0/2.5 1)	6.5/3.7 1)
WD	7.65	8.85
AA	1.5	3.75
SS	1.5	3.75
CI	4.35 6)	4.35 6)
CF	2.20 6)	2.20 6)
FA	7.55/4.85 1) 6)	9.25/6.35 1) 6)
FS	7.55/4.85 1) 6)	9.25/6.35 1) 6)
FM	23.15/4.55 1) 6)	24.70/6.35 1) 6)
FD	21.55/8.05 1) 6)	23.25/9.55 1) 6)
LA	0.5	2.0
LO	0.5	2.0
LX	0.5	2.0
AS	0.80/0.75 2) 6)	0.80/0.75, min 1.10 2) 6)
AD	1.50/1.05 2) 6)	1.50/1.05, - 1.10 2) 6)
LS	0.80/0.75 2) 6)	0.80/0.75, - 1.10 2) 6)
LD	0.95/0.90 2) 6)	0.95/0.90, - 1.10 2) 6)
NS	3.10 6)	3.10 - 3.60 6)
ND	4.15 6)	4.15 6)
JL	0.65/0.80 3)	1.30/1.30 3)
SH	0.60/1.25 4)	1.10/2.20 4)
SL	0.60/1.25 4)	1.10/2.20 4)
SE	0.60/1.25 4)	1.10/2.20 4)

INSTRUCTION	INSTRUCTION TIMES IN MICROSECONDS	
	CPU820 with cache	CPU820 without cache
SN	0.60/1.25 4)	1.10/2.20 4)
SO	0.75/1.40 4)	1.10/2.20 4)
SZ	0.60/1.25 4)	1.10/2.20 4)
SX	0.75/1.40 4)	1.10/2.20 4)
SP	1.50/2.15 4)	1.50/2.60 4)
RE	9.80	10.65
JE	1.35/1.50 3)	1.35/1.50 3)
JD	1.85/2.00 3)	1.85/2.00 3)
RI	15.10	16.65
GP	1.85-3.00 5)	1.85-3.00 5)
GG	1.95-2.90 5)	1.95-2.90 5)
DO	1.85	2.15
DI	1.40	2.30

Notes:

1. Without/with FPU801.
2. Left shift/right shift.
3. No link/ with link.
4. No skip/skip.
5. Instruction time depends on register address.
6. Add nx0.15 microseconds. For floating point instructions n is the number of alignment and/or normalization shifts. For shift instructions n is the number of shifts specified by the effective address.

For address calculations not included in the instruction times the times listed below should be added to the instruction times.

ADDRESS CALCULATION	Add microseconds	
	CPU820 with cache	CPU820 without cache
Indirect	0.8	1.4 1)
		1.35 to 2.15 2)
After AM		
+direct	0.15	0.15
+relative	0.15	0.15
+indexed	0.30	0.30
+relative+indexed	0.30	0.30

Notes:

1. Applies to instructions with memory reference.
2. Applies to instructions without memory reference. The time depends on the amount of overlap between instruction fetch and instruction execution.

2.6 Model Compatibility 2.6

The CPU820 is closely software and hardware compatible with previous RC8000 central processing units. It has a completely identical instruction set, and peripheral device controllers, which is connected to the CPU via the System Bus may be used without modifications.

The CPU820 is different from the previous CPU models on one point. It is not possible to execute instructions located in the 4 working registers. An attempt to execute a jump to location 0, 2, 4 or 6 will generate an exception with CAUSE = 0.

Programs (especially test programs) which utilize knowledge of internal implementation details of the CPU to provoke errors may cause error reactions on CPU820 which differ from error reactions on other RC8000 CPUs.

3. INSTALLATION 3.

3.1 Printed Circuit Boards 3.1

CPU820 consists of two printed circuit boards, CPU821 and CPU822, which should be installed in a RC8000 CPU-chassis, CHS806 or equivalent. The unused slots in the chassis may be used for cache memory and hardware floating point expansions. Note that connectors 1001 in the unused slots should be provided with a CBL824 plug. Connections to the System Bus and the internal CPU interconnection bus is made via the backplane on the CHS806. Connections to the Operators Control Panel (OCP), the Front-End Processor Adapter (FPA) autoload cable and the Technician Console are made via side connectors on CPU821 and CPU822. See fig. 1.

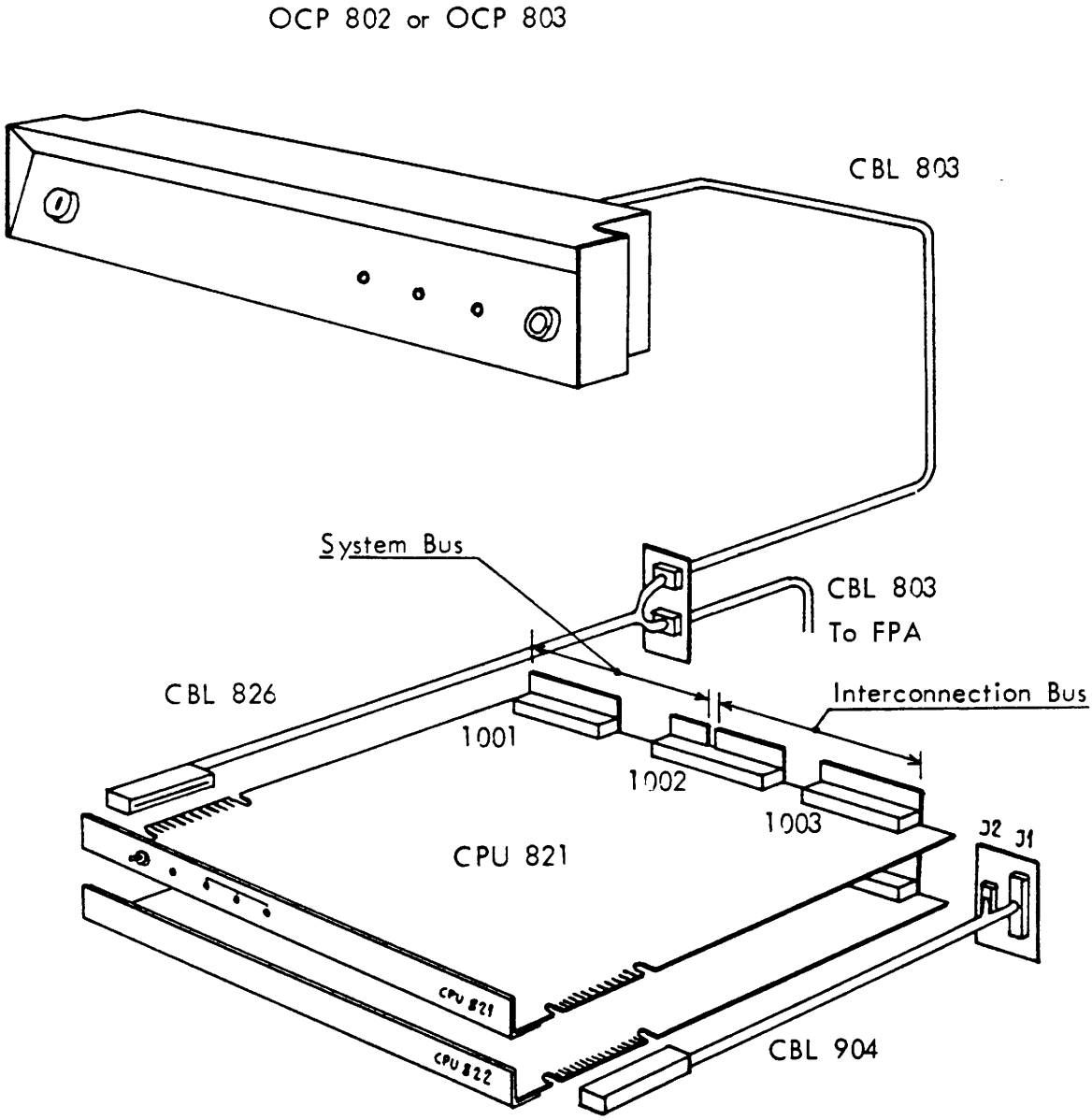
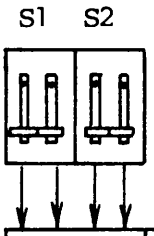


Figure 1: CPU820 installation.

3.2 Operating Mode Selection 3.2

Different operating modes of the CPU820 may be selected by means of 2x2 switches, S1 and S2, located on the CPU821 printed circuit board.



Red dot visible = 0

S1	S2	
0	0	NORMAL MODE OF OPERATION
1	X	POWER RESTART
X	1	POWER-UP TEST
X	X	CONTINOUS TEST
X	X	CONSOLE USED AS TC

POWER RESTART. This mode may be used in conjunction with core memory or semiconductor memory with battery back-up. After power has been turned on the CPU starts instruction execution in the memory location addressed by the contents of location 10 (decimal).

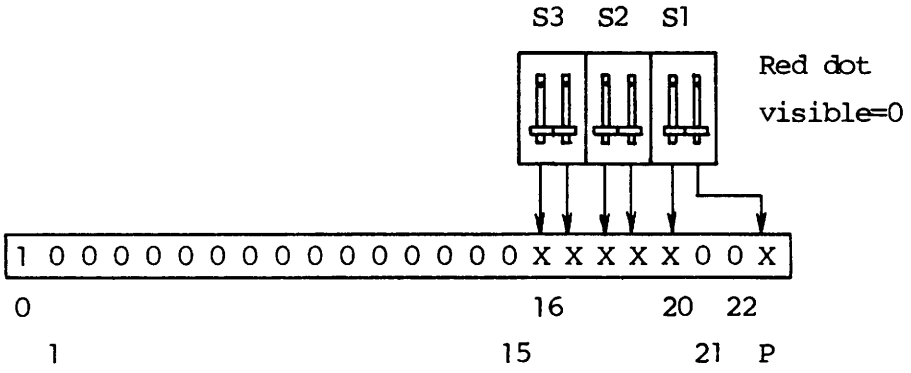
POWER-UP TEST. In this mode a special microprogrammed test is started after power-up. In order to run this test, only a small part of the hardware is required to operate. The test may therefore be useful first time power is applied to a CPU820. The test is described in ref. [1].

CONTINOUS TEST. The microprogrammed diagnostic activated at autoload will be repeated until it is stopped by an error or by operator intervention.

CONSOLE USED AS TC. This mode is reserved for future use.

3.3 CPU Device Address 3.3

The System Bus address of the CPU is selectable by means of 3x2 switches located on the CPU822 printed circuit board. The switches control the address bits (16:20) and the parity bit. The remaining address bits are fixed. Odd parity is used.

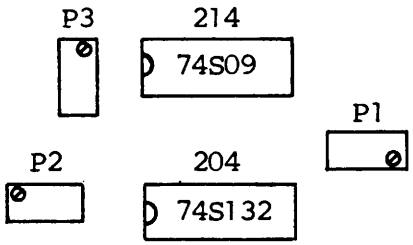


The standard CPU address is:

100 000 000 000 000 000 000 000

3.4 Deskew Delay Adjustments 3.4

The deskew delays for DATARDY, SELIN and ACK/NACK are adjustable by means of 3 potentiometers P1, P2 and P3. The potentiometers are located on the CPU822 printed circuit board.



For adjustment the delays may be activated by means of a microprogrammed test loop. The test loop may be started from the Technician Console by the command: T7.

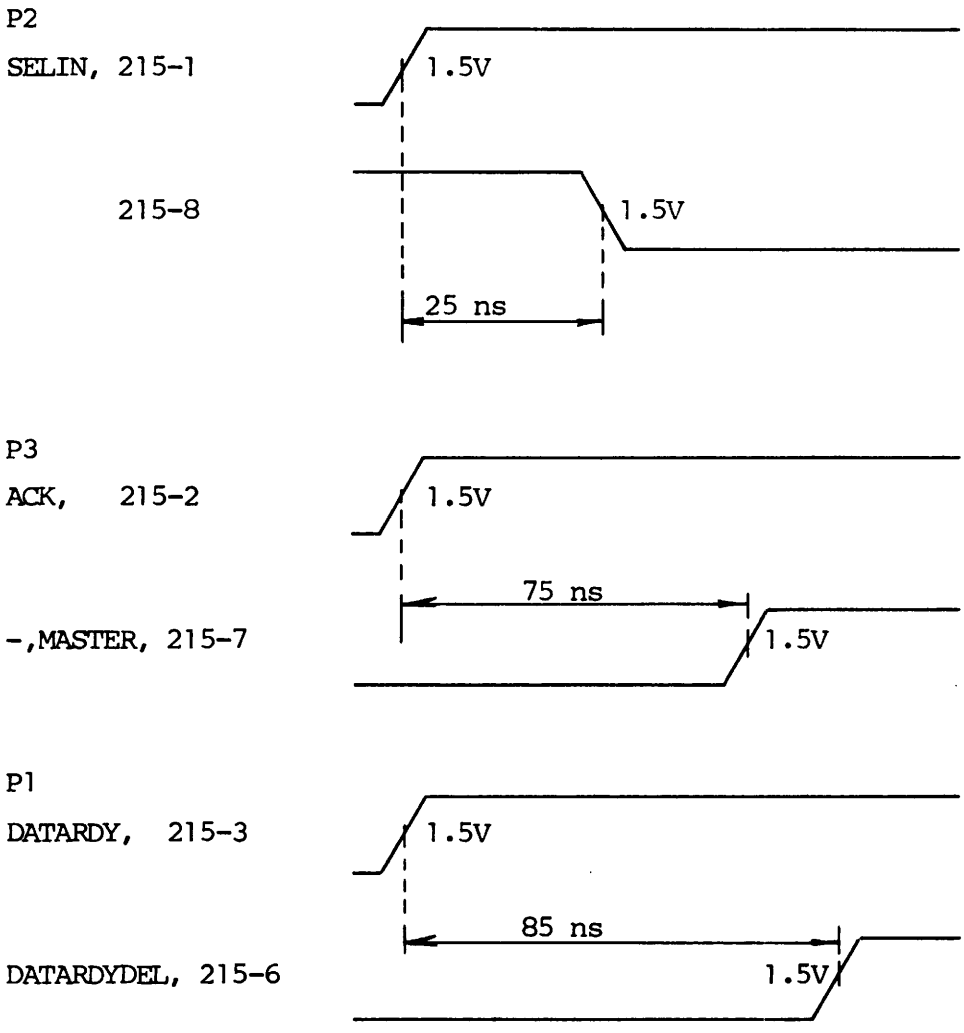
The following procedure is recommended for an initial adjustment of the delays.

1. Turn the potentiometers fully counter-clockwise corresponding to maximum delay.

2. Start the test loop.

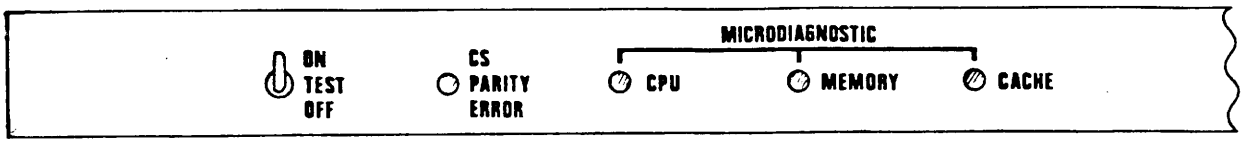
3. Adjust the delays according to the figures below.

The signals to be measured are available on test pins in position 215.



3.5 CPU821 Front Panel Switch and Indicators 3.5

The front panel of the CPU821 printed circuit board is provided with a switch and four LED indicators as shown below.



TEST. With the switch in position ON (normal) the microdiagnostic will be started at autoload. If no errors are detected by the diagnostic the system will be autoloaded at completion of the diagnostic. Detection of an error is indicated by flashing of the AUTOLOADING lamp on the OCP. With the switch in position OFF the microdiagnostic is bypassed at autoload. Se also ref. [1].

CS PARITY ERROR. Light in the indicator indicates parity error in the control store. This error will cause the CPU to stop immediately. The only way to get out of this error situation is to turn the power off and then on again. It should be noted that the indicator may give a dim light under normal operating conditions.

MICRODIAGNOSTIC. During execution of the microdiagnostic the three indicators CPU, MEMORY and CACHE indicate which module is being tested. In case of an error the indicators will indicate in which module the error has been detected.

4. TECHNICIAN CONSOLE 4.

A number of functions may be controlled from the Technician Console. E.g. Display and modification of CPU registers and memory locations, single instruction stepping and control of diagnostic programs. The Technician Console is not necessary for normal operation of the CPU, but it may facilitate trouble shooting.

4.1 Installation of Technician Console 4.1

A TTY compatible terminal with V.24 interface may be used as Technician Console. Connectors for connection of the Technician Console are located at the rear of the CPU chassis (CHS806) and marked: TECHNICIAN CONSOLE J1 and J2. Only one of the connectors may be used for connection at the same time. Fig. 2 shows how different RC terminals may be connected as Technician Console.

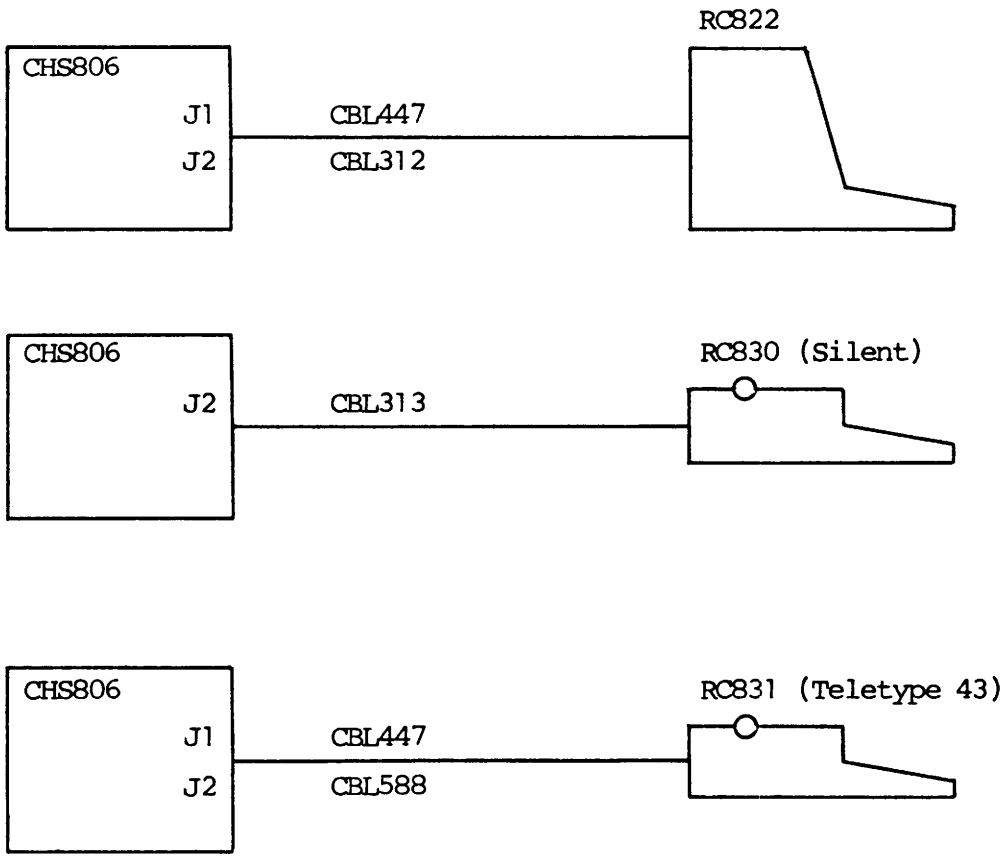
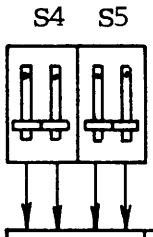


Figure 2: Connection of Technician Console.

Transmission speed for the Technician Console is selected by 2x2 switches, S4 and S5, located on the CPU822 printed circuit board. The number of stopbits is 1 for all transmission speeds. Fig. 3 shows the switch settings for different transmission speeds.



Read dot visible = 0

	TRANSMISSION SPEED bits/sec
0 1 1 0	300
0 1 1 1	600
1 0 0 0	900
1 0 0 1	1200
1 0 1 0	1800
1 0 1 1	2400
1 1 0 0	3600
1 1 0 1	4800
1 1 1 0	7200
1 1 1 1	9600

Figure 3: Transmission speed selection for Technician Console.

4.2 Technician Console Commands 4.2

The formats of the console commands are described below. Octal number representation is used for addresses and contents of registers and memory locations.

ESC

The ESCAPE key may be used to cancel a typed command or parameter. The CPU responds by displaying a ?.

XR<no><CR>

Displays the contents of register <no>.

LR<no>: <cont><CR>

Loads register <no> with the value <cont>.

XD<CR>

Displays the contents of the eight dynamic registers: W0, W1, W2, W3, STATUS, IC, CAUSE and SB.

XS<CR>

Displays the contents of the eight static registers: CPA, BASE, LOWLIM, UPLIM, INTLIM, INF, SIZE and MONTOP.

XW<CR>

Displays the contents of the six registers: WRK0, WRK1, WRK2, WRK3, WRK4, WRK5. The registers are used as auxiliary registers during instruction execution.

XM<loc><CR>

Displays the contents of memory location <loc>.

XN<no><CR>

Displays the contents of <no> consecutive memory locations, starting after the last referenced location.

LM<loc>: <cont><CR>

Loads memory location <loc> with the value <cont>.

LN<CR>

Load next memory location. After the command has been typed the address of the next memory location is displayed. The wanted contents of the memory location must now be typed as <cont><CR>.

S<CR>

Single instruction command. The instruction addressed by IC is executed and the contents of the eight dynamic registers after execution are displayed.

C<CR>

Continue. Starts instruction execution in the memory location addressed by IC.

BELL (=control G)

When the CPU is running it is only possible to stop it from the Technician Console by typing a BELL character. All other characters are echoed but has no effect.

R<loc><CR>

Run. Starts microinstruction execution from control store location <loc>. Typing R0<CR> will simulate a power up.

The following commands concern the microprogrammed tests. A detailed description of the commands may be found in ref. [1].

P<CR>

Proceed the test.

N<CR>

Loop in the test.

T<testno><CR>

Run microprogrammed test number <test no>. The following tests are available.

T0: CPU test, Memory test normal mode, Cache test
T1: CPU test, Memory test short mode, Cache test
T2: CPU test
T3: Memory test normal mode
T4: Memory test short mode
T5: Cache test
T6: Clear and size memory, W3 = last location in memory
T7: Loop to adjust deskew delays.

4.3 Register Addresses

Addresses of registers accessible by means of the XR and LR commands are listed below:

OCTAL ADDRESS	XR	LR
0	W0	W0
1	W1	W1
2	W2	W2
3	W3	W3
4	STAT	STAT
5	ICS	ICD
6	CAUSE	CAUSE
7	SB	SB
10	CPAC	CPAC, CPA
11	BASEC	BASEC, BASE
12	LLIMC	LLIMC, LLIM
13	ULIMC	ULIMC, ULIM
14	ILIMC	ILIMC
15	INF	INF
16	-	-
17	SIZE	SIZE
20	MONTOP	MONTOP
21	CPU VERSION	-
22	DATA SWITCH	DATA SWITCH
23	REG. SWITCH	REG. SWITCH
57	-	CELAR INTR. BIT
60	DATA SWITCH	DISPLAY
61	REG. SWITCH	-
62	RTC	-

DATA SWITCH, REG. SWITCH and DISPLAY are used by some test programs to simulate a CPU800 technical panel.

5. CHECK-OUT PROCEDURE 5.

After installation CPU, main memory and cache memory (if installed) should be checked by means of the microprogrammed tests. The tests may be operated from either the Technician Console or from the Operators Control Panel. Operation from the Technician Console provides better error information and the possibility of running selective tests for CPU, main memory and cache memory etc. A detailed description of the tests and the operation of the tests is given in ref. [1].

After at least 2 error free passes of test T0 the system should be checked by means of the system test programs. These test programs are described in ref. [2].

A. REFERENCES A.

[1] RCSL No 30-M270:
CPU820 MICROPROGRAMMED TESTS

[2] RCSL No 30-M261:
RC8000 Test Operating System (TOP), User's Guide.

RETURN LETTER

Title: CPU820 GENERAL INFORMATION RCSL No.: 30-M281

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Do you find errors in this manual? If so, specify by page.

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How can this manual be improved?

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