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FPA803, Front Processor Adapter Reference Manual

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Keywords:

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Reference Manual.

Abstract:

This paper describes the logical structure of FPA803.

(42 printed pages).

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CONTENTS PAGE

MAIN CHARACTERISTICS 1

Short Description. 1.1

The FPA 801 is an asynchronous controller intended for use as interconnecting medium between the RC 8000 computer and the RC 3600/ RC 3500 computer.

FPA 801 contains two sub-devices, called the TRANSMITTER and the RECEIVER. Refer to fig. 1.1.

Although transmission cannot take place in both directions simultaneously, the FPA 801 acts from a programmer's point of view as two independent devices, each running their own program simultaneously.

FPA 801 is constructed around a 24 bits RALU (Register-Arithmetic-Logic-Unit) which via a micro program performs all of the functions associated with the communication. Refer to block diagram, fig. 1.2.

FPA 801 is physically located in the main frame and occupies one slot of a standard RC 8000 cassette.

Communication with RC 8000. 1.2

Communication with RC 8000 CPU takes place via the standard unified bus. Operations are initiated by means of an output operation, which addresses the receiver or the transmitter. Hereafter the communication takes place via a channel program stored in the memory.

Once started FPA 801 fetches its commands in the channel program and executes the commands without the engagement of the CPU.

Data to be written or read from front end are transferred directly between FPA 801 and memory.

When the channel program has been executed, it is normally terminated with a STOP command which transfers status to memory and interrupts the CPU controlling FPA 801.

FPA 801 commands can be ordered to the transmitter part as well as the receiver part. There are only few differences in the interpretations of the commands, which appear in the "programming Specifications", section 2.

Normally, the transmitter part of FPA 801 is used to transmit a data block to the front end processor, and to receive a single status character as a respond to the transmitted block.

The receiver part is used to receive a data block from front-end processor, and to transmit a single status character as a respond to the received data block.

Communication with Front-End. 1.3

The communication with the front-end takes place via a set of output and a set of input lines. The output lines and input lines are completely symmetrical, each set consisting of:

9 data lines incl. a parity line, and
7 control lines.

For further specifications of the lines, refer to "Interface between FPA 801 and Front-End", section 3.

Included in the control lines is an autoload request line, which is necessary to be able to initiate an autoload procedure in the front-end computer under RC 8000 program control and vice versa.

The communication is asynchronous on character basis. 8-bits characters are used.

The transmission rate is:

max. 600,000 characters/sec.

The timing of the character transfers is under control of two types of request signals and one request acknowledge signal.

The request signals are named:

1. DATA REQUEST and
2. STATUS REQUEST.

The data request is used as a request signal when the transmitter transmits data to front-end, and the status request is used when the receiver transmits status to front-end.

The communication with the front-end utilizes the asynchronous, fully interlocked technique. Each request signal from FPA 801 to front-end must be acknowledged by the front-end to complete the transfer.

When FPA 801 wants to transmit a character, the character is placed on the data lines and the request signal is raised. When the front-end has stored the character, it responds to the request by raising the request acknowledge signal, indicating the reception of the character. Upon the reception of the acknowledge signal, FPA 801 lowers the request signal, which also causes the front-end to lower the acknowledge signal. Fig. 1.3 illustrates the handshake technique.

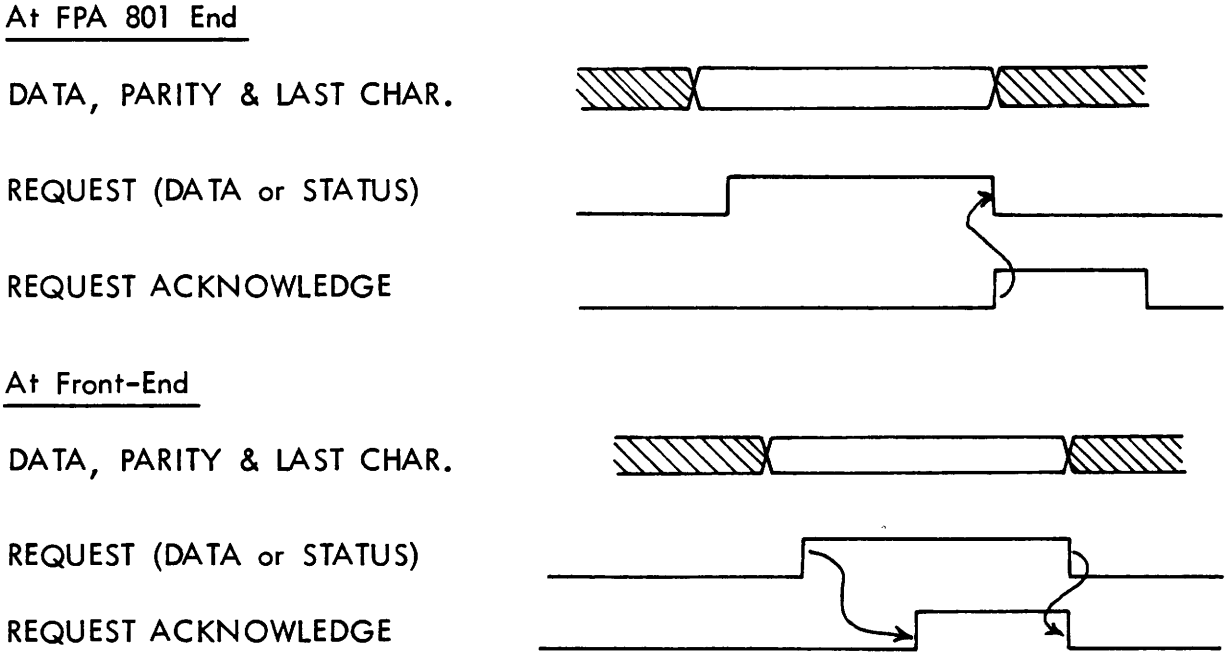


Fig. 1.3

Simultaneously with the emission of the last character in a block the LAST CHAR signal is sent to the front-end.

Also provided in the control lines is a RESET signal which notifies the receiver when the transmitter is reset.

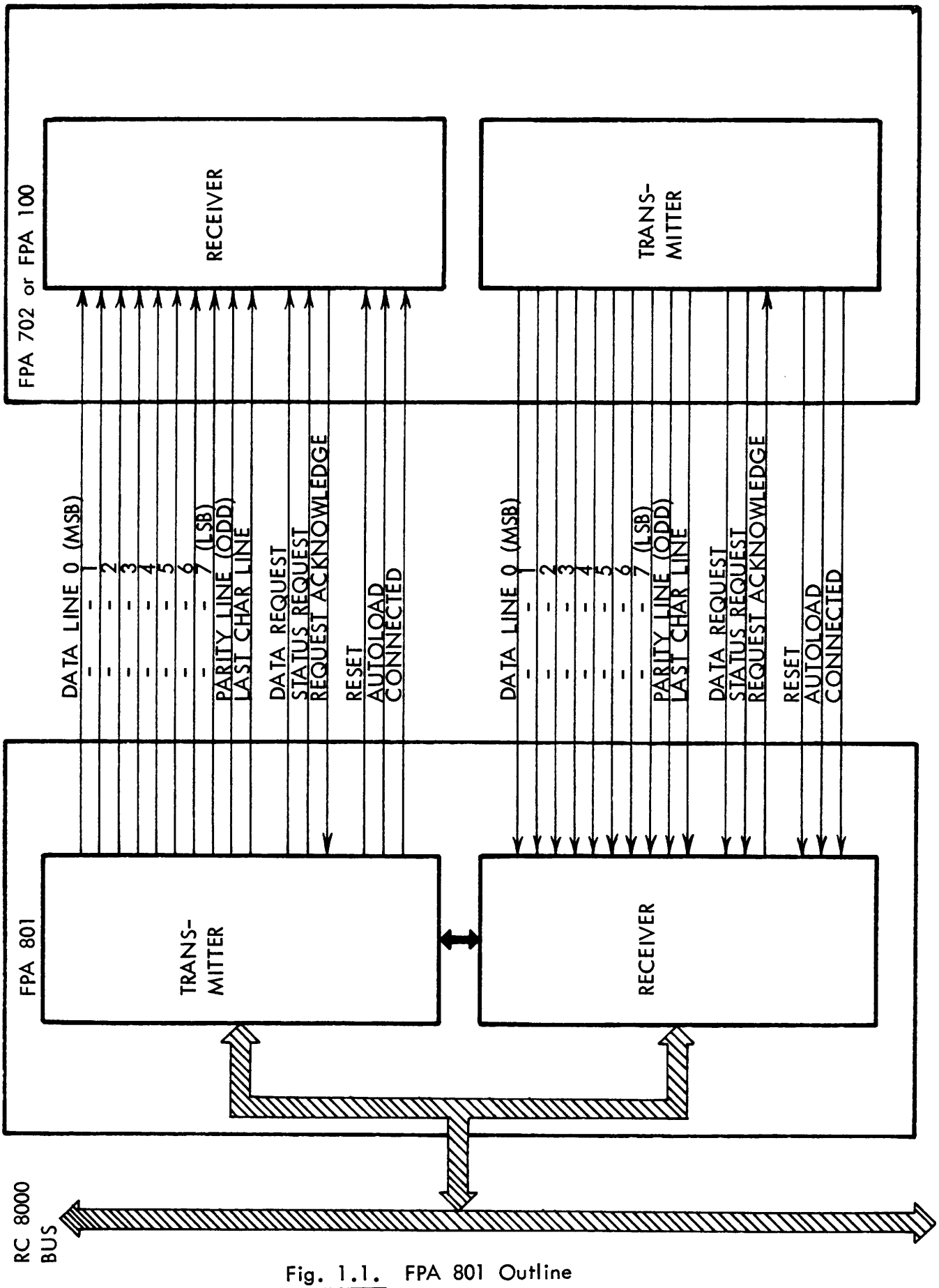


Fig. 1.1. FPA 801 Outline

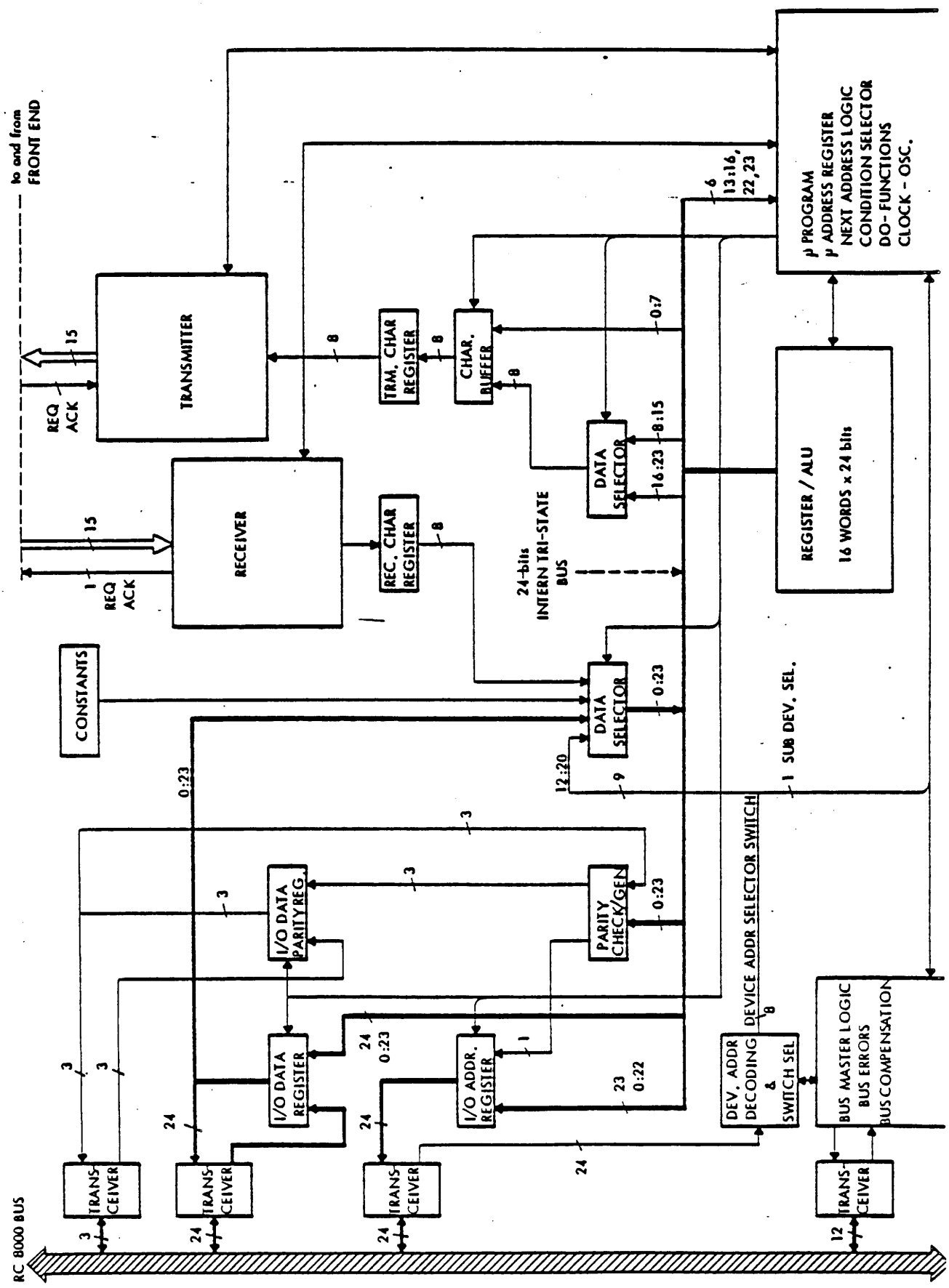


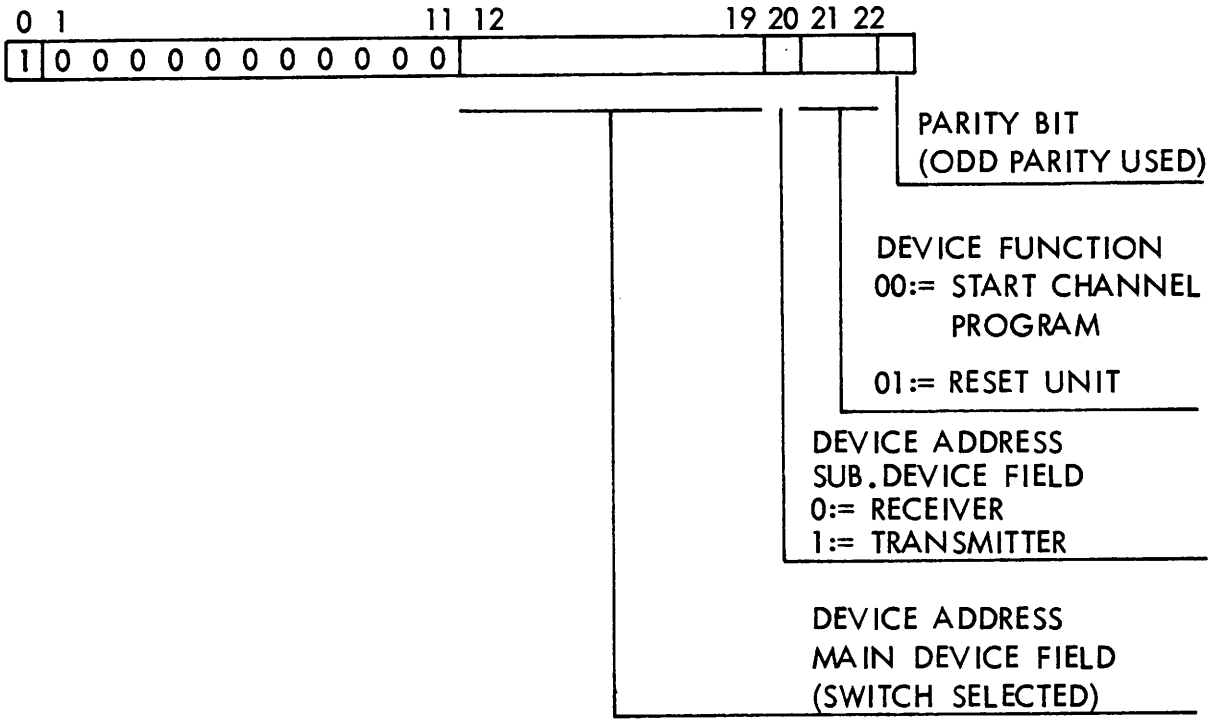
Fig. 1.2

Block Diagram

PROGRAMMING SPECIFICATIONS 2

Device Functions. 2.1

Address Format. 2.1.1



The FPA 801 is a blockorientated device, which is started by means of an output operation. This output operation addresses FPA 801, and the address format is as shown above. The contents of the W-REG is irrelevant.

The response to an output operation is the DATA ACKNOWLEDGE signal, which indicates coincidence between the received main device address and the main device address stored in the FPA 801 device address selector. In case of non-coincidence or parity error the acknowledge signal will not be returned. Input operations are also neglected.

DEVICE ADDRESS (BIT 12 : 20)

By means of these bits the FPA 801 TRANSMITTER or RECEIVER can be addressed.

BIT 12 : 19 constitute the main device field, which is common to the TRANSMITTER and RECEIVER (switch selected). BIT 20 = "0" identifies the RECEIVER and BIT 20 = "1" identifies the TRANSMITTER.

The main device field is used as described, while the total DEVICE ADDRESS (BIT 12 : 20) is used to calculate the DESCRIPTION ADDRESS for TRANSMITTER or RECEIVER:

DEVICE DESCRIPTION ADDRESS =
BASE ADDRESS + DEVICE ADDRESS x 8

ADDRESS OF BASE ADDRESS = 8

DEVICE FUNCTION (BIT 21 : 22)

The FPA 801 utilizes only 2 of 4 possible device functions:

21	22	
0	0	START CHANNEL PROGRAM
0	1	RESET UNIT

Addressing FPA 801 using the two other device function will have the same effect:

21	22	
1	0	START CHANNEL PROGRAM
1	1	RESET UNIT

Start Channel Program. 2.1.2

This function causes the addressed device to start its channel program.

A channel program is always initiated by fetching the first word of the device description, using the device description address.

The first word in the device description contains the address of the first channel command to be executed.

After the execution of the channel command the next one is automatically fetched and executed etc. The channel program is normally terminated by means of the stop command. Concerning abnormal terminations, refer to pages 2-19 and 2-20.

Reset Unit. 2.1.3

This function causes the addressed device to assume an idle and unassigned condition.

Note that device status is not cleared by the RESET UNIT function.

If the TRANSMITTER is reset, a RESET signal will be sent to the receiver in the FRONT-END PROCESSOR.

An unassigned condition is defined as a condition in which the device is not able to generate interrupts.

An idle condition is defined as a condition in which the device awaits addressing. In this condition, the FPA 801 stores possible events.

If a reset function to a device is received while the other device is running, the execution of the reset function is postponed until the other device executes the micro instruction CHANGE DEVICE.

If a reset function to a device is received while the device is running, the reset function will be executed immediately.

PARITY BIT

This bit makes the parity of the address word odd. The parity is automatically checked and generated by FPA 801.

Device Description. 2.1.4

Each subdevice requires the following device description in the memory:

Base addr + 8 x device addr + 0 := Channel Program Address

Base addr + 8 x device addr + 2 := First address of status area

Base addr + 8 x device addr + 4 := Interrupt Destination

Base addr + 8 x device addr + 6 := Interrupt Level

Status Area. 2.1.5

Each subdevice requires the following area for standard status information:

First address + 0 := Current Channel Program Address

First address + 2 := Rem. Char. Count/Current first word addr.

First address + 4 := Current status

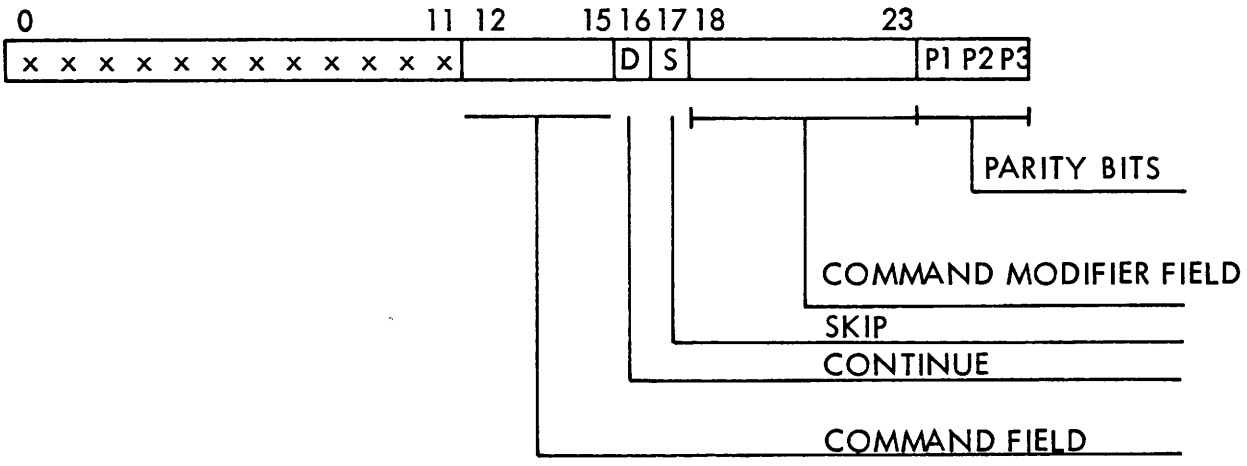
First address + 6 := Event status

Channel Commands. 2.2

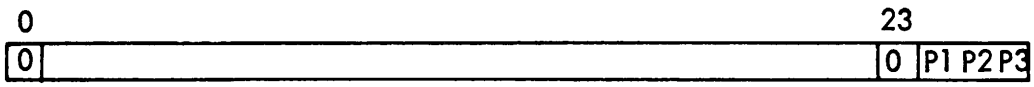
Channel Command Format

WORD 1: CHANNEL COMMAND

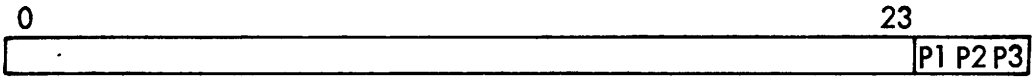
x = don't care bits.



WORD 2: FIRST WORD ADDRESS



WORD 3: CHARACTER COUNT



Channel commands are fetched from RC 8000 memory. The parity bits are automatically generated and checked.

P1 is assigned to BITS 0 : 7 (odd parity)

P2 is assigned to BITS 8 : 15 (odd parity)

P3 is assigned to BITS 16 : 23 (odd parity)

A channel command does always consist of three words. In some cases WORD 2 and 3 are irrelevant.

WORD 1 is always the channel command itself.

The interpretation of the channel command words will be specified during the description.

FPA 801 will accept the following commands:

x = don't care words.

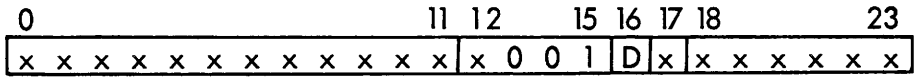
COMMAND	FIRST WORD ADDRESS	CHAR. COUNT
READ	USED	USED
WRITE	USED	USED
SENSE	USED	x
WAIT	x	x
STOP	x	x
CONTROL (no param.)	x	x

Undefined commands are executed as dummy commands; i.e. FPA 801 does nothing but continues with next channel command.

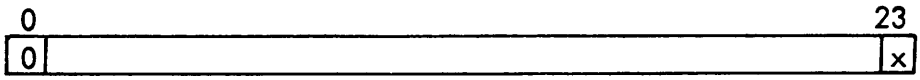
The channel commands of FPA 801 can be executed by the RECEIVER as well as the TRANSMITTER, there are only few differences in the interpretation. These differences will be explained during the description of the individual commands.

Read. 2.2.1

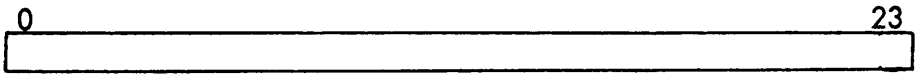
WORD 1: CHANNEL COMMAND



WORD 2: FIRST WORD ADDRESS



WORD 3: CHARACTER COUNT



The read command is interpreted as follows:

Receive characters from the front-end processor and transfer these characters to RC 8000 memory from FIRST WORD ADDRESS and on. The characters are assembled into words (1 word = 3 characters), which are transferred to RC 8000 memory word by word.

The characters are stored as follows:

First	char. is stored in bit positions	0 : 7
Second	- - - - - -	8 : 15
Third	- - - - - -	16 : 23
Fourth	- - - - - -	0 : 7

} word 1 in FIRST WORD ADDRESS

and so on.

If the characters received do not divide by 3, the remaining character positions of the last word will be all zeroes.

Under normal circumstances the channel command will be terminated by either:

1. RECEIVE BLOCK END, i.e. last character detected, or
2. CHARACTER COUNT = 0.

If the channel command has been terminated in this way, the FPA 801 continues with the next channel command.

If the character counter is decreased to zero without simultaneous detection of receive block end, event status bit 4 - BLOCK LENGTH ERROR - will be set to logical 1, provided CONTINUE is not specified, however, the FPA 801 continues to receive characters until receive block end is detected. The characters received under these circumstances are not transferred to RC 8000 memory, but the character counter is still decreased by 1 for every character received.

When receive block end is detected, the character counter will contain a negative figure indicating the number of characters not transferred to memory.

Receive block end detection causes the character counter to be added to the remaining char. count register - STATUS WORD 2, event status bit 1 - PARITY ERROR - to be updated and the command to be terminated. Hereafter, FPA 801 continues with the next channel command.

If received block end is detected while char. count is $\neq 0$, the remaining contents of the character counter is added to the remaining char. count register, event status bit 1 updated, and the command terminated. Hereafter, FPA 801 continues with the next command.

WORD 2 - FIRST WORD ADDRESS

This parameter is interpreted as the start address of the memory area, in which characters received have to be stored. The address is a full word address, i.e. bit 23 is ignored.

WORD 3 - CHARACTER COUNT

This word specifies the maximum number of characters, which must be transferred to memory. The character counter is decremented by 1 for every character received.

Every character received is checked for correct parity (8 bits chars. - odd parity is used). If a parity error is detected, a parity error FF will be set, and FPA 801 continues with the next character. Upon receive block end detection, the contents of the parity error FF are transferred to event status bit 1 - PARITY ERROR IN MEDIUM.

Concerning abnormal termination of the read command, refer to pages 2-19 and 2-20.

CONTINUE (Bit 16)

By means of the continue bit, several read commands can be linked up (data-chaining).

Such a chain consisting of a number of read commands with continue bit = 1, and terminated with a read command with continue bit = 0, acts logically as one read command; however, data are stored in the not necessarily consecutive memory areas specified by the FIRST WORD ADDRESS and CHAR. COUNT of the individual read commands in the chain.

If the character counter is counted to zero without detection of receive block end, the FPA 801 continues with the next read command in the chain.

When receive block end is detected, the remaining char. count is added to the remaining char. count register, and parity status is updated. The char. counts of read commands following receive block end are also added to the remaining char. count register. The chain is regarded as terminated by either:

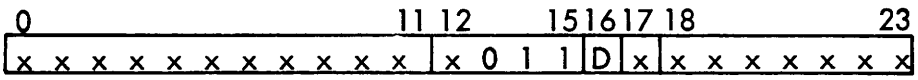
1. A read command with continue = 0.
2. A stop command.
3. Abnormal termination of read commands (errors).

DIFFERENCES IN THE INTERPRETATION OF TRANSMITTER READ COMMANDS AND RECEIVER READ COMMANDS

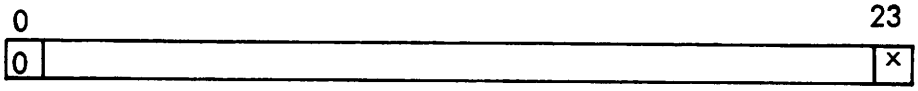
When FPA 801 receives a read command, it awaits a request signal from the front-end, and the addressed device does not enter the reception loop until the request signal of the first character is received. The transmitter part of FPA 801 awaits a STATUS REQUEST, and the receiver part awaits a DATA REQUEST.

Write. 2.2.2

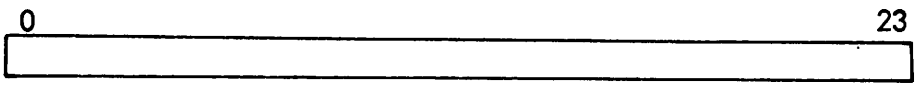
WORD 1: CHANNEL COMMAND



WORD 2: FIRST WORD ADDRESS



WORD 3: CHARACTER COUNT



The write command is interpreted as follows:

Transmit characters to the front-end processor from the RC 8000 memory area specified by FIRST WORD ADDRESS and CHAR. COUNT.

First	char.	is	fetched	from	bit	positions	0 : 7	word 1 from FIRST WORD ADDRESS
Second	-	-	-	-	-	-	8 : 15	
Third	-	-	-	-	-	-	16 : 23	
Fourth	-	-	-	-	-	-	0 : 7	

and so on.

Under normal circumstances this channel command will be terminated when the char. counter is counted to zero, which causes a LAST CHAR. signal to be sent to the front-end processor simultaneously with the last character. Hereafter, FPA 801 continues with the next channel command. Time-out may occur during the transmission, refer to time-out description page 2-17.

Concerning abnormal termination of the command, refer to pages 2-19 and 2-20.

WORD 2 - FIRST WORD ADDRESS

This parameter is interpreted as the start address of the memory area, from which characters to be written are fetched. The address is a full word address, i.e. bit 23 is ignored.

WORD 3 - CHARACTER COUNT

This word specifies the number of characters which have to be transmitted to front-end processor. The character counter is decremented by 1 for every character transmitted.

All characters contain 8 information bits and 1 parity bit (odd parity used).

CONTINUE (Bit 16)

By means of the continue bit it is possible to chain write commands.

Such a chain consisting of a number of write commands with continue bit = 1 and terminated by a write command with continue bit = 0 acts

logically as one write command, however, characters are fetched from the not necessarily consecutive memory areas specified by the FIRST WORD ADDRESS and CHAR. COUNT of the individual write commands in the chain.

The last character signal is generated when the character counter is decreased to zero in the last write command in the chain.

The chain is regarded as terminated by either:

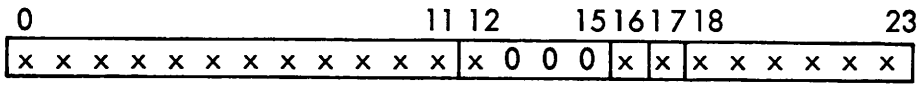
1. Write command with continue = 0.
2. Stop command.
3. Abnormal termination of write command.

DIFFERENCES IN THE INTERPRETATION OF TRANSMITTER WRITE COMMANDS AND RECEIVER WRITE COMMANDS

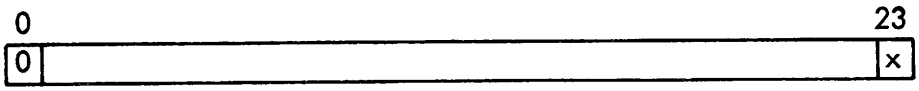
1. A write command ordered to the FPA 801 TRANSMITTER causes the DATA REQUEST signal to be used as timing signal during the communication with the front-end processor, in contradistinction to a RECEIVER write command, which uses the STATUS REQUEST signal.

Sense. 2.2.3

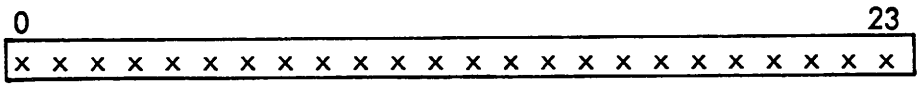
WORD 1: CHANNEL COMMAND



WORD 2: FIRST WORD ADDRESS



WORD 3: CHARACTER COUNT



The sense command is interpreted as follows:

Transfer the contents of FPA 801 status registers to 8000 memory from FIRST WORD ADDRESS and on.

The status registers are:

STATUS WORD 1: CURRENT CHANNEL PROGRAM ADDRESS
STATUS WORD 2: REM. CHAR. COUNT/CURRENT FIRST WORD ADDRESS
STATUS WORD 3: CURRENT STATUS
STATUS WORD 4: EVENT STATUS

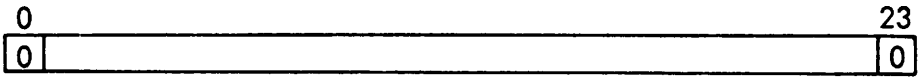
Under normal circumstances the sense command is terminated, when the 4 status words have been correctly transferred to 8000 memory. The termination causes reset of FPA 801 status registers 1, 2, and 4.

Bus time-out, bus communication error, or bus parity error which may occur during the transfer of a status word to memory, cause the event status bit 21 - STATUS TRANSFER ERROR - to be set to logical 1, and FPA 801 attempts to transfer the next status word, however, if these errors occur during transfer of event status, the command will be terminated without clearing of status registers.

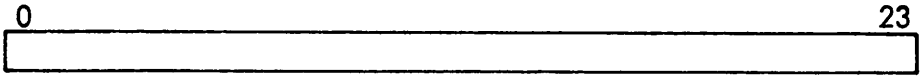
Event status being $\neq 0$ at the start of a new channel program causes an interrupt to be generated and transfer of status registers to 8000 memory. The status address located in the description of the new channel program determines where the status registers are stored.

STATUS REGISTERS

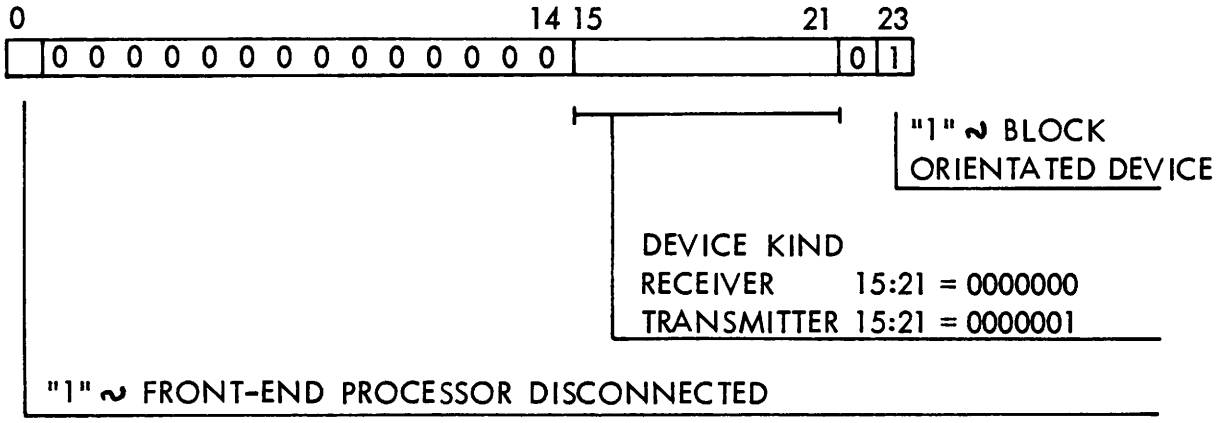
STATUS WORD 1: CURRENT CHANNEL COMMAND ADDRESS



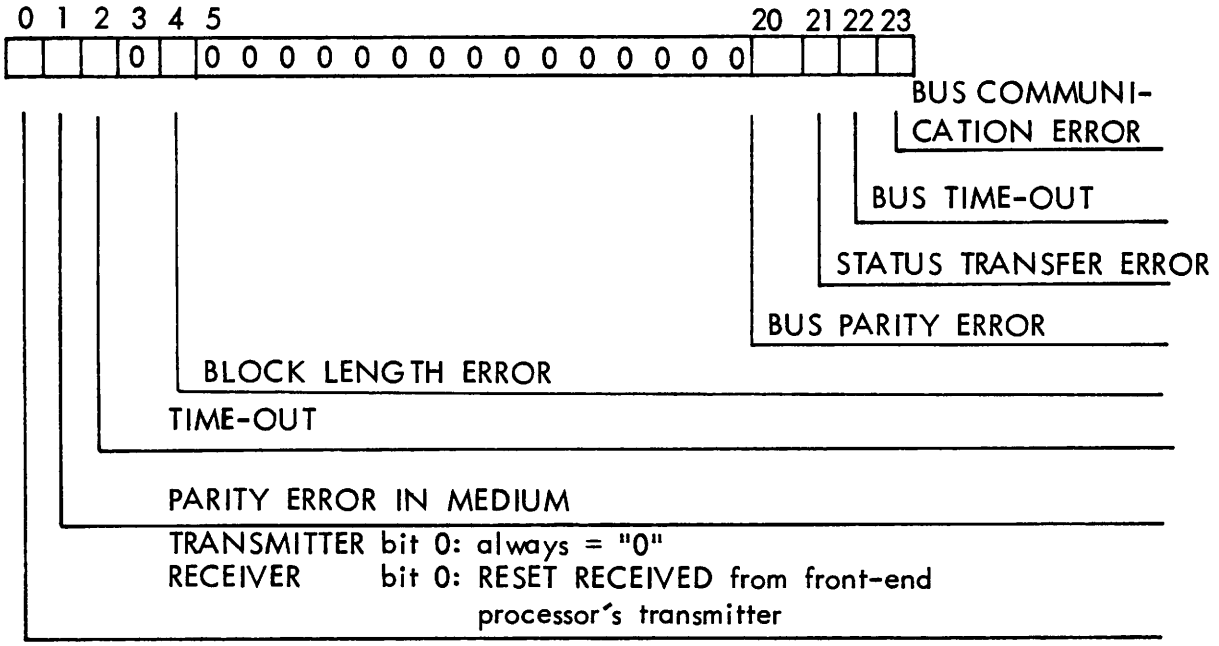
STATUS WORD 2: REMAINING CHARACTER COUNT or CURRENT FIRST WORD ADDRESS



STATUS WORD 3: CURRENT STATUS



STATUS WORD 4: EVENT STATUS



Status registers are also transferred to memory in the following two cases:

1. When a channel program is terminated by the STOP command.
2. When channel commands are terminated on account of error situations.

In these cases status are transferred to memory using the status address located in the device description.

STATUS WORD 1: CHANNEL PROGRAM ADDRESS

Except for errors occuring during fetch of the channel program address, the contents of status word 1 are always the address of the next channel command which is going to be executed, since the channel program address after the completion of FPA 801 μ-program "fetch command" points at the next channel command.

If an error occurs during fetch of command, the channel program address will point at either:

1. FIRST WORD ADDRESS
2. CHARACTER COUNT
3. NEXT CHANNEL COMMAND ADDRESS

Status word 1 is cleared by either:

1. POWER TURN ON
2. SYSTEM RESET
3. THE SUCCESSFUL TRANSFER OF STATUS TO MEMORY

STATUS WORD 2: REMAINING CHAR. COUNT/ CURRENT FIRST WORD ADDRESS

The interpretation of this status word depends on the command executed. Only two commands make use of status word 2; these are:

1. Read command
2. Write command

After normal termination of a read command, status word 2 contains the difference between the ordered number of character transfers and the actual number of characters transferred to memory. Status word is negative, if the number of characters received was greater than the number specified by the char. count parameter, positive if less, and all zero if equal.

After abnormal termination on account of reset from front-end processor, status word 2 contents will be as for normal termination.

After abnormal termination of a read command on account of bus errors the word is considered as incorrectly transferred to the addressed memory cell. Status word 2 will in this situation contain the current first word address, which points at the subsequent memory cell.

The character count of read continue commands ordered after the detection of receive block end will be added to the remaining character count of the previous command.

After normal termination of a write command, status word 2 contains the difference between the ordered number of character transmissions, and the actual number of characters transmitted.

Status word 2 may be positive if time-out (time-out between FPA 801 and front-end processor) has occurred during the transmission. Since FPA 801 contains two character buffers, the remaining char. count will be two characters less than the number of characters acknowledged by the front-end.

After abnormal termination of a write command on account of bus errors the word is considered as incorrectly fetched from the addressed memory cell. Status word 2 will in this situation contain the current first word address, which points at the addressed memory cell.

The character count of write continue commands ordered after time-out between FPA 801 and front-end will be added to the remaining character count of the previous command.

In any case, status word 2 is cleared by either:

1. POWER TURN ON
2. SYSTEM RESET
3. THE SUCCESSFUL TRANSFER OF STATUS TO MEMORY

STATUS WORD 3: CURRENT STATUS

Status word 3 contains the following information:

BIT 0 : Front-end DISCONNECTED

BIT 15 : 21 : DEVICE KIND

BIT 23 : BLOCK ORIENTATED DEVICE

Remaining bits in current status are all zeroes.

Bit 0 is logical 1, if the cable to front is not installed or the power at the front-end is not turned on.

BIT 15 : 21:

Transmitter device kind = 0 0 0 0 0 0 1
Receiver device kind = 0 0 0 0 0 0 0

BIT 23 is always logical 1 in connection with FPA 801, which is a block orientated device.

STATUS WORD 4: EVENT STATUS

Status word 4 contains the following information:

BIT 0 : RESET RECEIVED from front-end

BIT 1 : PARITY ERROR IN MEDIUM

BIT 2 : TIME OUT

BIT 4 : BLOCK LENGTH ERROR

BIT 21 : STATUS TRANSFER ERROR

BIT 22 : BUS TIME-OUT

BIT 23 : BUS COMMUNICATION ERROR

Remaining bits in event status are all zeroes. Every status bit in event status are cleared by either:

1. POWER TURN ON
2. SYSTEM RESET
3. THE SUCCESSFUL TRANSFER OF STATUS TO MEMORY

BIT 0: RESET RECEIVED from Front-End.

Status bit 0 is only valid in connection with the receiver part of FPA 801. When logical 1 it indicates that the transmitter part in the front-end processor adapter has been reset.

The reset signal is continuously supervised during the transfer of characters from front-end transmitter to FPA 801 receiver. If a reset arises, receiver status is transferred to RC 8000 memory and an interrupt generated. After the interrupt, FPA 801 receiver assumes an idle and unassigned condition.

A reset occurring in the unassigned condition or at any other time, when reset is not continuously supervised, is stored in an FF, and causes immediate status transfer and interrupt by new start of the receiver.

BIT 1: PARITY ERROR IN MEDIUM.

This status is set to logical 1 when a parity error is detected in data received from front-end. Detection of a parity error causes no interrupt generation or further error reaction.

BIT 2: TIME-OUT.

Time-out occurs if a REQUEST ACKNOWLEDGE signal is not returned from front-end within a certain time after FPA 801 REQUEST emmission. The time-out detection does not cause interrupt generation, however, the write command will be terminated. In case of time-out during data chaining, the char. counts of possible following write commands to the transmitter will be added to the remaining char. count of the previous transmitter command. The timer may be disabled by means of a strap. See "strapping possibilities" in GENERAL INFORMATION.

BIT 4: BLOCK LENGTH ERROR.

BLOCK LENGTH ERROR is set to logical 1, if the character counter, in a read command with continue bit = 0, is decreased to zero without the simultaneous detection of receive block end.

BLOCK LENGTH ERROR is valid for both the receiver and transmitter part of FPA 801 and causes no interrupt generation.

Detection of BLOCK LENGTH ERROR does not cause termination of the command, FPA 801 continues to receive characters until receive block end, however, characters received after character counter has become 0, are not transferred to memory.

BIT 20: BUS PARITY ERROR.

This status bit is set to logical 1 during DATA-IN communication (data transfer from slave to master), if a parity error in data received from the slave is detected.

Bus parity error causes transfer of status to memory followed by an interrupt.

BIT 21: STATUS TRANSFER ERROR.

This status bit is set to logical 1, if bus time-out [bus parity error] or bus communication error occur during the transfer of status to RC 8000 memory.

BIT 22: BUS TIME-OUT.

Bus time-out is a status signal which may be generated during bus communication, if the slave, as a respond to a DATA READY signal from MASTER, does not return DATA ACKNOWLEDGE or DATA NOT ACKNOWLEDGED within a certain time.

Bus time-out causes transfer of status to memory followed by an interrupt.

BIT 23: BUS COMMUNICATION ERROR.

This status is set to logical 1, if a DATA NOT ACKNOWLEDGE signal is received from the slave.

Bus communication error causes transfer of status to memory followed by an interrupt.

Abnormal Termination

Status bits 0, 20, 22, and 23 may cause abnormal termination. The mode of termination depends on the command or device function executed.

If read or write commands are abnormally terminated, status is transferred to RC 8000 memory and an interrupt is generated. Hereafter the addressed device is placed in an idle and unassigned condition.

The stop command is abnormally terminated only if either:

1. Bus errors during fetch of status address.
2. Bus errors during transfer of event status.
3. Bus error during interrupt.

The sense command does not involve interrupts and is only abnormally terminated if the above mentioned item 1 or 2 is fulfilled. After an abnormal termination of stop or sense, the addressed sub-device is placed in an idle and unassigned condition.

Wait and control commands in connection with FPA 801 does not involve abnormal termination.

When the device function "start channel program" is executed, abnormal termination may occur on account of either:

1. Bus errors during fetch of the base address.
2. Bus errors during fetch of channel program address.
3. Event status being $\neq 0$.
4. Bus errors during fetch of:
    a. CHANNEL COMMAND
    b. FIRST WORD ADDRESS
    c. CHARACTER COUNT

Termination on account of item 1 or 2 causes the addressed device to be placed in an idle and unassigned condition.

Termination on account of item 3 or 4 causes status transfer followed by an interrupt, and hereafter the addressed device is placed in an idle and unassigned condition.

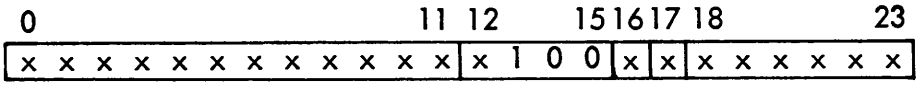
During interrupt generation abnormal termination may occur on account of either:

1. Bus error during fetch of INTERRUPT LEVEL.
2. Bus error during fetch of INTERRUPT DESTINATION.
3. Bus error during transfer of INTERRUPT LEVEL to the CPU, which is identified by means of the INTERRUPT DESTINATION.

In any case, the device which is executing the interrupt is placed in an idle and unassigned condition.

Wait. 2.2.4

WORD 1: CHANNEL COMMAND



x = don't care.

The contents of words 2 and 3 are irrelevant in connection with the wait command.

Apart from the stop command the wait command does not place the addressed device in unaissigned condition.

The wait command places the device in an idle condition.

The command is terminated by either:

1. An attention event.
2. By new start of the device.

In case of an attention event, status will be transferred to memory followed by an interrupt, and hereafter the device is placed in a dummy wait condition, which can only be terminated by means of the device function RESET UNIT.

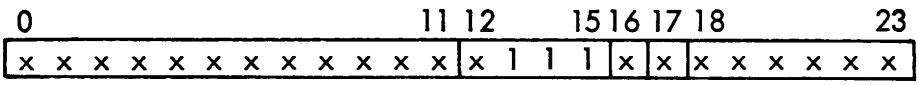
In case of new start of device the wait command terminates without status transfer and interrupt and the addressed device continues with the channel program.

The only attention event in connection with FPA 801 is "RESET RECEIVED" from front-end; and this event is only valid in connection with the receiver part of FPA 801.

As a rule, the wait command should only be used as a single command, and not in channel programs composed of several commands.

Stop. 2.2.5

WORD 1: CHANNEL COMMAND



x = don't care.

The contents of words 2 and 3 are irrelevant.

This command, when normally terminated, causes transfer of status to 8000 memory followed by an interrupt.

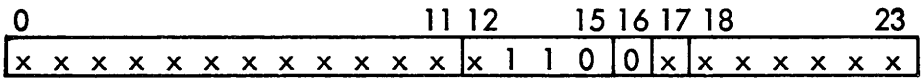
Hereafter, the addressed device is placed in an idle and unassigned condition.

Concerning abnormal termination of the stop command, refer to pages 2-19 and 2-20.

The stop command is used to terminate a channel program.

Control (no Parameter). 2.2.6

WORD 1: CHANNEL COMMAND



x = don't care.

The contents of words 2 and 3 are irrelevant.

This command causes activation of the autoload signal to the front-end processor, if the transmitter part of FPA 801 is addressed.

If the receiver is addressed, the command will be interpreted as an initiate command, which transfers a status character, with all bits equal to logical 0, to the front-end. Time-out may occur during the transmission, refer to time-out, page 2-17. Note that continue must not be ordered in connection with the initiate command.

FPA 801 COMMANDS

COMM. FIELD 12	13	14	15	Continue bit 16	Channel command, word 1	First word address, word 2	Character count, word 3
x	0	0	0	x	SENSE	First word addr.	x
x	0	0	1	D	READ	First word addr.	Char. count
x	0	1	1	D	WRITE	First word addr.	Char. count
x	1	0	0	x	WAIT	x	x
x	1	1	0	x	CONTROL	x	x
x	1	1	1	x	STOP	x	x

x denotes parameters or bits not used.

FPA 801 EVENT STATUS

Bit	Receiver interpretation	Transmitter interpretation
0	RESET RECEIVED	x
1	PARITY ERROR IN MEDIUM	PARITY ERROR IN MEDIUM
2	TIME-OUT	TIME-OUT
4	BLOCK LENGTH ERROR	BLOCK LENGTH ERROR
20	BUS PARITY ERROR	BUS PARITY ERROR
21	STATUS TRANSFER ERROR	STATUS TRANSFER ERROR
22	BUS TIME-OUT	BUS TIME-OUT
23	BUS COMMUNICATION ERROR	BUS COMMUNICATION ERROR

x denotes unused bits.

Unused bits and remaining bits are always zero.

FPA 801 CURRENT STATUS

Bit	Receiver interpretation	Transmitter interpretation
0	FRONT-END DISCONNECTED	FRONT-END DISCONNECTED
21	DEVICE KUND = 0	DEVICE KIND = 1
23	BLOCK ORIENTATED = 1	BLOCK ORIENTATED = 1

Remaining bits are always zero.

Fig. 2.1. Command and Status Survey

INTERFACE BETWEEN FPA 801 AND FRONT-END 3

Timing (Refer to Fig. 3.1). 3.1

As mentioned in section 1 "Main Characteristics" the communication with the front-end utilizes the handshake technique.

Note that the transmitting unit is allowed to raise the request signal, even if the request acknowledge signal is not lowered, which means that it is the rise of the leading edge of the request acknowledge that indicates the reception of the character.

This is done to speed up the transmission, since the transmitting unit does not need to wait for the propagation of the high to low transition of the acknowledge signal.

Upon the reception of the low to high transition of the request acknowledge signal the transmitting unit must lower the request signal. The request signal must be low for at least 100 ns.

The pulse width of request acknowledge must not be less than 30 ns.; however, the signal must not be lowered until the request signal has been lowered. The pulse width of request acknowledge depends on cable delay, driver/receiver propagation delays, and propagation delays in circuits, which utilize the acknowledge signal. When using FPA 801 interface circuits and principle the width of request acknowledge, measured at the output of the line driver, will not be less than 30 ns.

When measured at the outputs of line drivers, data must lead request with at least 20 ns., the same specification is valid for the last character signal. Data must not change as long as the request signal is true.

To compensate for max. cable and receiver skew, the receiving unit must delay the request signal at least 100 ns. before the character is stored.

The pulse width of RESET and AUTOLOAD signals shall be at least 300 ns.

Line Drivers and Receivers. 3.2

The following line drivers and receivers are recommended:

Drivers:

TEXAS	:	SN 75183
NATIONAL	:	DM 8830
Am	:	26LS31

Receivers:

TEXAS	:	SN 75182
NATIONAL	:	DM 8820 A
Am	:	26LS32

The line drivers provide differential output signals, and are used to drive a twisted pair line with an impedance of app. 120 Ω . The drivers are single supplied and use only + 5V.

SN 75183 and DM 8830 are compatible and include gates, which are useful when it is necessary to gate the signals; therefore, this type of driver is used for the control signals.

26LS31 is used for the data, parity, and last character signals, since these signals need no gating.

The line receivers are designed to sense small differential signals in the presence of large common-mode noise; up to $\pm$ 7V. common mode input voltage can be tolerated. The receivers are single supplied and use only + 5V.

SN 75182 and DM 8820 A are compatible and include strobe and terminating resistor (170 Ω). The strobe input is used to strobe all of the control signal receivers with the disconnected signal from the opposite end. This assures that the output of the control signal receivers is always logical 0, if the opposite computer is disconnected (power off or no cable installed etc.).

26LS32 is used as receiver for the data parity and last character signals, since these signals need no gating. No terminating resistor is included in the 26LS32.

Cable Characteristics. 3.3

The cable to be used should have the following characteristics:

Type:	Shielded cable, Min. 16 pairs of twisted wires 0.25 mm^2.
Impedance:	App. 120 Ω .
Max. length:	20 m.

The shield of the cable must be connected to the common zero voltage. Refer to fig. 3.2. The cable should only be terminated in the receiving unit.

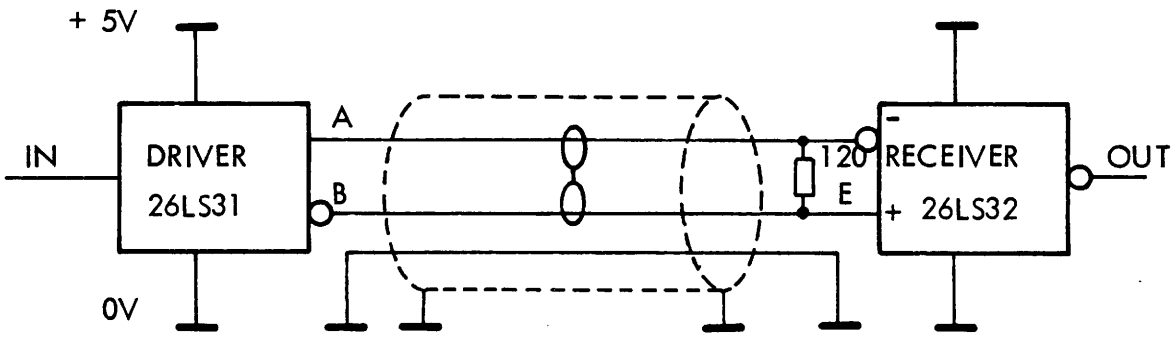


Fig. 3.2.

When a logical 1 exists on the line, A shall be positive in relation to B.

Signal Description. 3.4

DATA LINES 0 : 7 : Data line 0 is the most significant bit, and data line 7 the least significant bit.

PARITY LINE : This line is the parity line making the parity odd.

LAST CHAR LINE : When logical 1 this line indicates the end of the block. The LAST CHAR signal is generated simultaneously with the emission of the last character in the block. The last char. signal must also be generated during status character transmission.

DATA REQUEST LINE : This signal when logical 1 indicates to the receiving unit that a data character is ready on the data lines 0 : 7. The signal is generated by the transmitter in the transmitting unit.

STATUS REQUEST LINE : This signal when logical 1 indicates to the receiving unit that a status character is ready on the data lines 0 : 7. The signal is generated by the receiver in the transmitting unit.

REQUEST ACKNOWLEDGE LINE : When this signal changes from false to true state, it indicates to the transmitting unit that the character on the data lines has been stored in the receiving unit. Upon the reception of the rising edge of the acknowledge signal the transmitting unit is allowed to fetch the next character and place it on the data lines.

RESET LINE : This line when logical 1 indicates to the receiver in the receiving unit that the transmitter in the transmitting unit has been reset.

CONNECTED LINE : This line when logical 1 indicates to the receiving unit that power is on. The connected signal is used to strobe the following control signals:

RESET
REQUEST ACK
DATA REQUEST
STATUS REQUEST
AUTOLOAD

This assures that the output of these receivers is at logical 0 when power in the transmitting unit is turned off, presupposed the connected line is terminated as shown on diagram 31, section 3.2.

AUTOLOAD LINE : This line is necessary to be able to initiate an autoload procedure in the front-end computer under RC 8000 program control. Likewise, the front-end computer may use the line to initiate an autoload procedure in RC 8000.

RC doc. VB 143

A/S REGNECENTRALEN	Designed by VH 10/10 - 75	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.

Unit FPA 801 Dwg. No.

LINE CHARACTERISTICS TIMING

AT FPA 801

Shaded areas ~ undefined condition

DATA & PARITY LINE

LAST CHAR LINE

REQUEST LINE (DATA or STATUS)

REQUEST ACKNOWLEDGE LINE

min 20 ns

min 100 ns

Depends on cable length
max. cable length ~ 20 m ~ cable skew ~ 20 ns

AT FRONT END

DATA & PARITY LINE

LAST CHAR LINE

REQUEST LINE (DATA or STATUS)

REQUEST ACKNOWLEDGE LINE

Depends on cable skew

min 100 ns

min 30 ns

Fig. 3.7

OPERATION 4

Switches and Indicators. 4.1

On the FPA 801 frontpanel is located one switch and two indicators.

The switch is named "AUTOLOAD ENABLE/DISABLE", and is used to enable/disable the autoload signal send to the RC 8000 CPU.

The indicators are named "TRANSMIT" and "RECEIVE".

The transmit indicator is switched on for app. 100 mS every time the data request signal to the opposite controller changes from false to true. The transmit indicator indicates that data is being transmitted to the opposite controller. Note that the transmit indicator is not switched on when status characters are transmitted.

The receive indicator is switched on for app. 100 mS every time a data request from the opposite controller is acknowledged by FPA 801. The receive indicator indicates that data is being received from the opposite controller. Note that the receive indicator is not switched on when status characters are received.

RETURN LETTER

Title: FPA803, Front Processor Adapter, Reference Manual

RCSL No.: 52-AA1099

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