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RC8401
General Information FPA803
Rev. 1

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Abstract:

This paper is a general information for the RC8401 Front-End Processor Adapter.

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1. GENERAL INFORMATION 1.

1.1 General Description 1.1

FPA803 is an asynchronous communication controller intended for use as interconnecting medium between the RC8000 computer and the RC3600/RC3500 computer.

FPA803 contains two sub-devices, called the TRANSMITTER and the RECEIVER.

Normally, the transmitter part of FPA803 is used to transmit a data block to the front-end processor, and to receive a single status character as a respond to the transmitted block.

The receiver part is used to receive a data block and to transmit a single status character as a respond to the received data block.

The communication with the front-end utilizes the asynchronous, fully interlocked technique. Each request signal from FPA803 to front-end must be acknowledged by the front-end to complete the transfer.

When FPA803 wants to transmit a character, the character is placed on the data lines and the request signal is raised. When the front-end has stored the character, it responds to the request signal by raising the request acknowledge signal, indicating the reception of the character. Upon the reception of the acknowledge signal, FPA803 lowers the request signal, which causes the front-end to lower the acknowledge signal thus completing the transfer of the character.

The communication with RC8000 CPU takes place via a unified bus.

Operations are started by means of an output operation, which starts the receiver or the transmitter. Hereafter the communication takes place via a channel program stored in the memory, which is also connected to the unified bus.

Once started, FPA803 fetches its commands in the channel program and executes these commands without the engagement of the CPU.

1.2 Specifications

1.2.1 Performance Specifications

Transmission rate

Max. 600,000 chars./sec.

Transmission mode

Asynchronous on character by character basis, fully interlocked.

Transmission line

A set of input lines and a set of output lines. The output and input lines are completely symmetrical, each set consisting of:

9 data lines including a parity line
7 control lines

Signals to/from Front-End

Data lines 0:7 : Data line 0 is MSB.
Data line 7 is LSB.

Parity line : Odd parity is used.

Last char line : This line points out the last character in a block.

Data request : Indicates to the receiving unit that a data character is ready on the data lines.

Status request : Indicates to the receiving unit that a status character is ready on the data lines.

Request acknowledge line : Indicates to the transmitting unit that the receiving unit has stored the transmitted character. This allows the transmitting unit to transmit the next character.

Reset line : A reset signal is sent to the opposite controller when the transmitter is reset.

Connected line : This signal indicates to the opposite controller that power is on.

Autoload line : This signal is used to initiate an autoload sequence in the opposite computer and vice versa.

Channel commands

The transmitter part of FPA803 as well as the receiver part is able to execute following channel commands:

Read : Receive characters from the opposite controller.

Write : Transmit characters to the opposite controller.

Sense : Transfer status to RC8000 memory.

Control : Transmitter part: Send autoload signal.
Receiver part: Transmit an all zero status character.

Wait : Wait for an attention event or a new start.

Stop : Stop channel program.

1.2.2 Electrical Specifications

Supply voltage

5 VDC $\pm$ 5%/6A

Bus towards CPU

1. Bus characteristic

   Bidirectional, open collector, separate data and address bus.

2. Signal representation

   Logical 1 = low voltage

   $0V \geq Vout_L < 0V45$

   Logical 0 = high voltage

   $4V3 \geq Vout_H$

3. Transceivers

   Texas instrument SN75138

4. Cable

   Characteristic impedance 120E $\pm$ 20% unbalanced.

Communication line towards Front-end

1. Characteristic

   Differential in- and outputs $\pm$ 7V common mode input voltage range.

2. Signal representation

   Logical 1 = line A positive relative to B
   Logical 0 = line A negative relative to B
   Line A or B high level min. 1V8
   Line A or B low level max. 0V4

3. Driver/Receivers

Texas 75183 line drivers/Texas 75182 line receivers are used for control signals.

Am 26LS31 line drivers/Am 26LS32 line receivers are used for data out/in signals.

4. Cable

Characteristic impedance approx. 120E balanced.

1.2.3 Environmental Specifications 1.2.3

Ambient temperature : 10-40°C

Relative humidity : 20-80% (no condensation)

1.2.4 Physical Specifications 1.2.4

FPA803 occupies one slot in a standard CHS802 cassette.

1.3 Identification of Items 1.3

FPA803 : Front-End Processor Adapter

CBL803 : Autoload Cable

1.4 Installation 1.4

This section explains how the FPA803 is installed in the CHS802 cassette, and how to connect FPA803 to the surrounding equipment. Strapping possibilities and adjustment of main device number selector is also explained.

1.4.1 Installation of FPA803

The FPA803 PCB may be inserted in any position of the CHS802 cassette.

PCB plug 1001 and 1002 connect FPA803 to the RC8000 bus.
PCB plug 1003 is not used.

Via PCB plug 1005 characters are received from the front-end, and via PCB plug 1004 characters are transmitted to the front-end.

NOTE: The PCB board should not be removed from or inserted in the cassette which DC-power is present.

Concerning interconnections to the opposite controller, refer to interconnection diagrams, Figures No. 1.4.1, 1.4.2, and 1.4.3.

1.4.2 Strapping Possibilities

1.4.2.1 Main Device Number Straps

The main device number straps (S12 ⟶ S5) consist of 8 straps used to set main device number and 1 strap (S4) used to make the parity of the main device number and the parity control strap even.

The 8 device number straps are located in position 134, and the parity control strap is located between pos. 113 and 123. The straps are shown below in fig. 1.4.4.

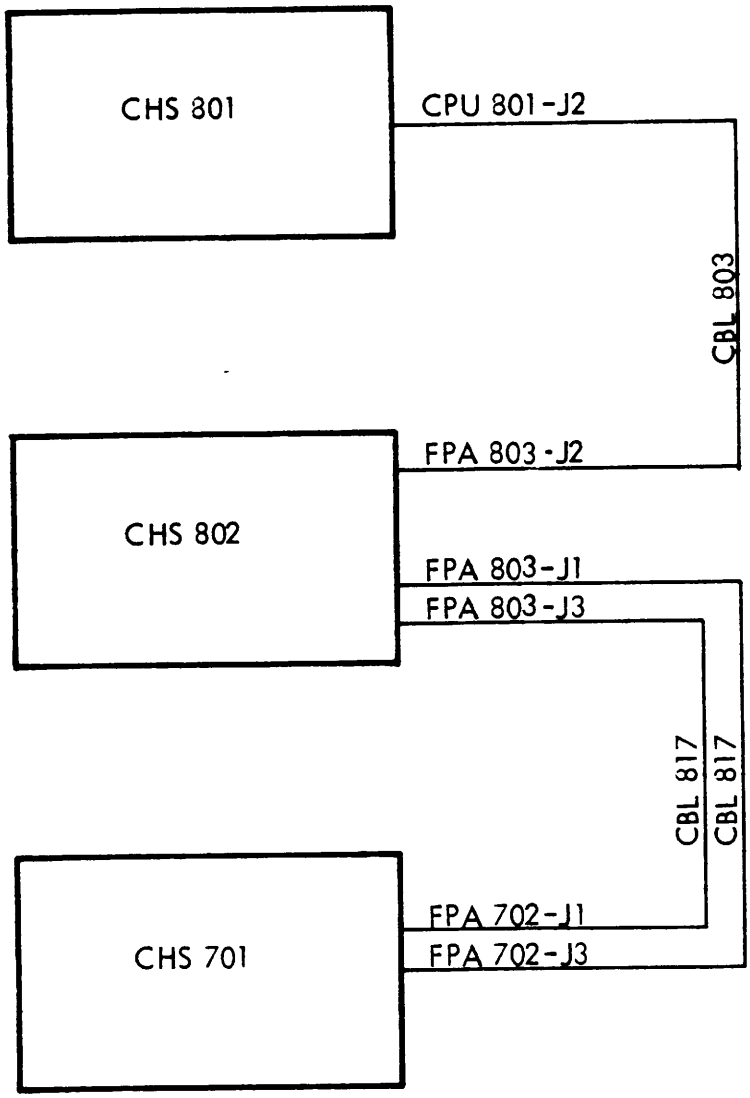


Fig. 1.4.1

FPA803, RC8000 connected to FPA702, RC3600

Interconnection Diagram

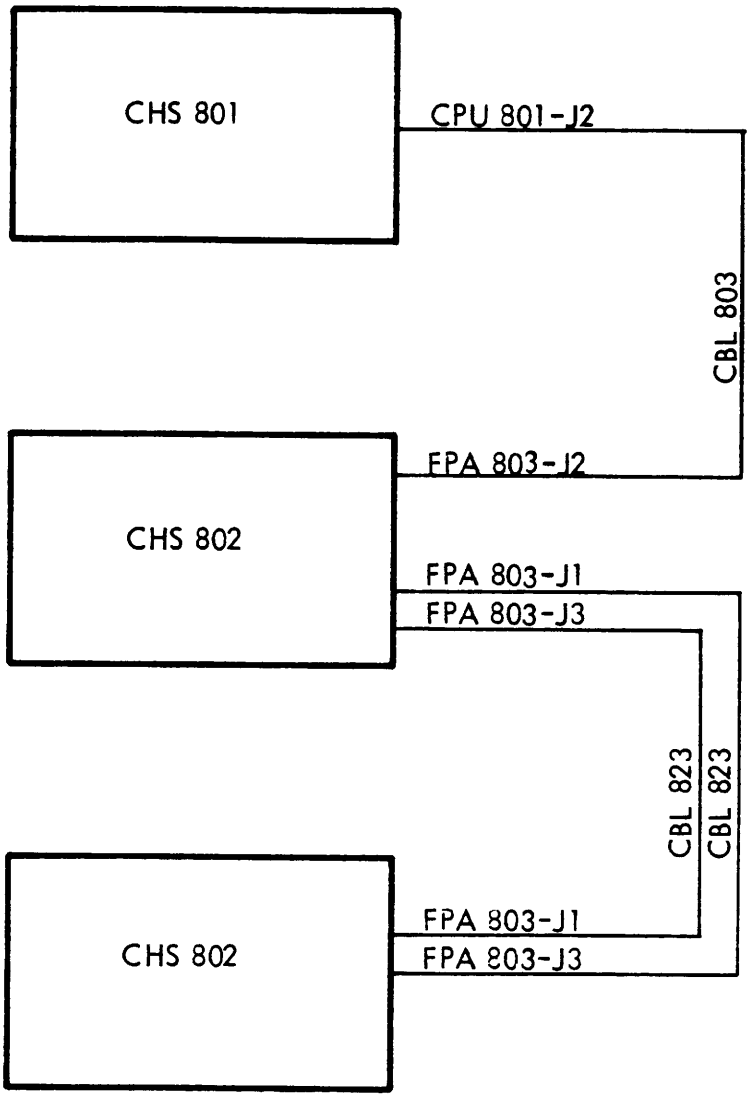


Fig. 1.4.2

FPA803, RC8000 connected to FPA803, RC8000

Interconnection Diagram

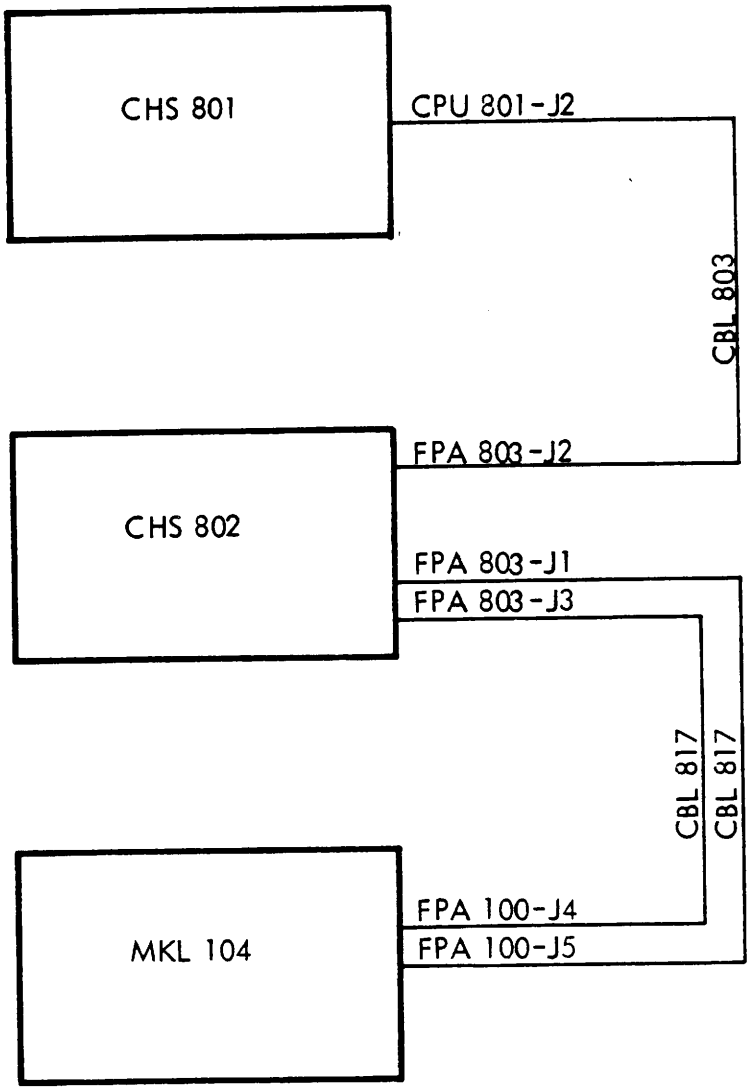


Fig. 1.4.3

FPA803, RC8000 connected to FPA100, RC3500

Interconnection Diagram

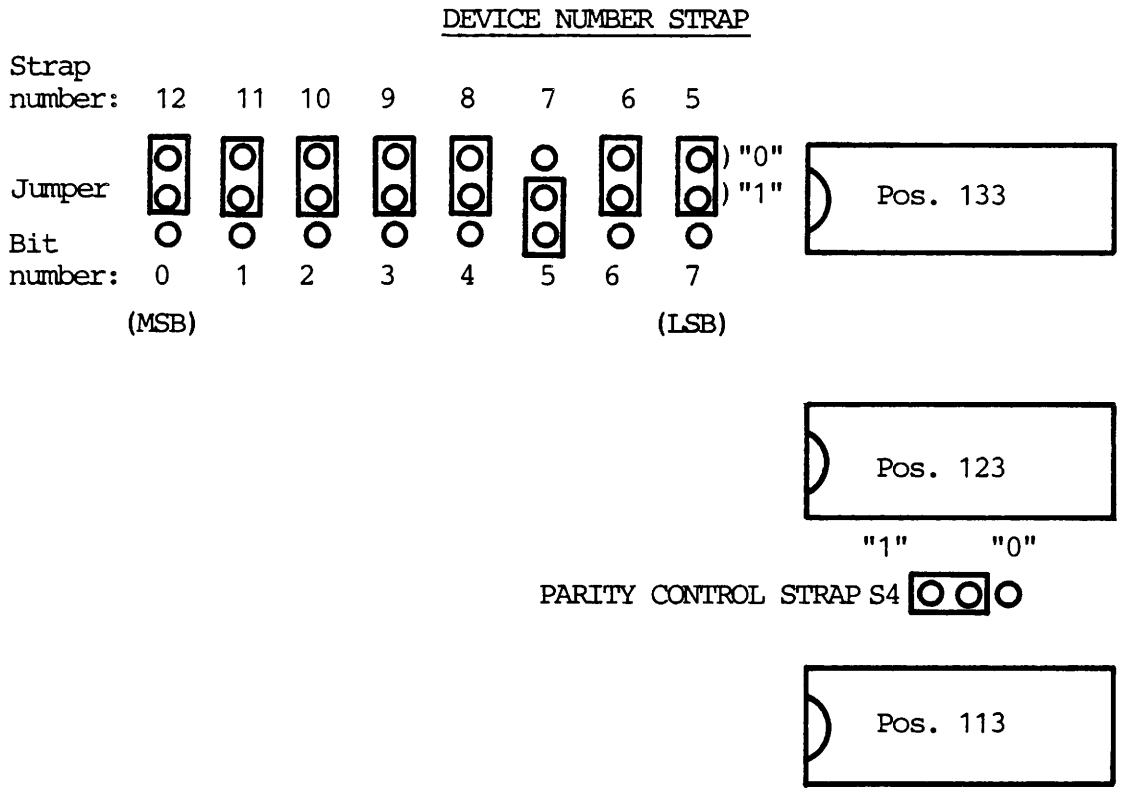


Fig. 1.4.4

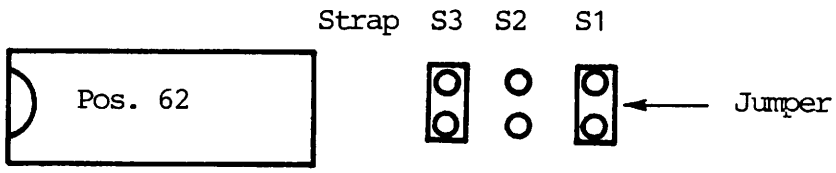
The device number is set by means of jumpers placed in either the "0" or "1" positions. The parity of the device number straps and the parity control strap must always be even. In fig. 1.4.4 the main device number is 8_{10}, which gives parity control strap = "1".

1.4.2.2 Straps for RUN/STOP and SINGLE STEP switches

1.4.2.2

Position 61 (straps S3 ⟶ S1) contains two jumpers, which must be placed as shown in fig. 1.4.5. When the jumpers are removed, the RUN/STOP and SINGLE STEP switches may be inserted (these switches are only used for test purposes). Refer also to DIAGRAM 1 in TECHNICAL MANUAL.

RUN/STOP and SINGLE STEP
switches not mounted:



RUN/STOP and SINGLE STEP
switches mounted:

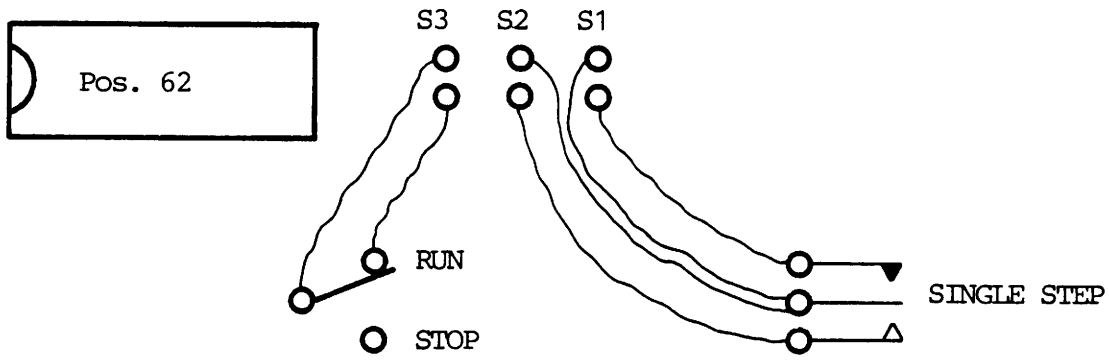
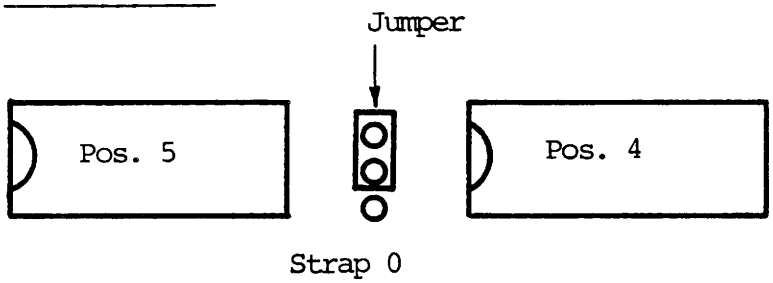


Fig. 1.4.5

1.4.2.3 Strap for Disconnecting of Timer

The FPA contains a timer, which is started every time a character is transmitted to the front-end. Time-out occurs if a REQUEST ACKNOWLEDGE signal is not returned from front-end within 8.5 mS. after the FPA has sent the character (DATA/STATUS REQUEST). Some installations may require the timer to be disabled, which is made possible by means of strap 0 located between position 4 and 5. It is emphasized that the FPA without this timer, will wait in an endless loop if the opposite controller does not respond to DATA/STATUS REQUEST signals. The only way to recover is by means of the RESET UNIT commands from RC8000. Fig. 1.4.6 shows how to disable timer.

TIMER ENABLED



TIMER DISABLED

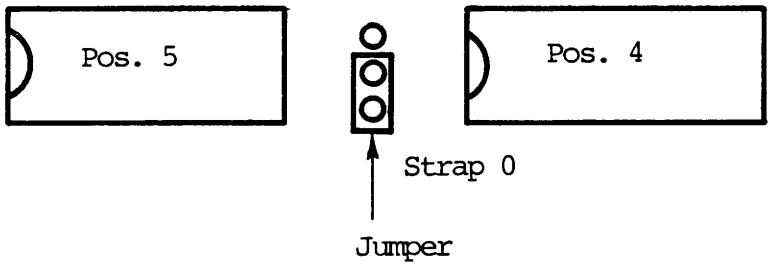


Fig. 1.4.6

1.4.3 Front Panel

On the FPA803 frontpanel is located one switch and two indicators. The switch is named "AUTOLOAD ENABLE/DISABLE" and is used to enable/disable the autoload signal relayed to the RC8000 CPU.

The indicators are named "TRANSMIT" and "RECEIVE". The transmit indicator is switched on for approx. 100 mS. every time the data request signal to the opposite controller changes from false to true, thus indicating when data characters are being transmitted.

The receive indicator is switched on for approx. 100 mS. every time a data request from the opposite controller is acknowledged by FPA803, thus indicating when data characters are being received.

RETURN LETTER

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