RCSL No: 99 0 00805

Edition: Nov. 1984.

Author: Villy Hansen

Title: Technical Manual for FPA 803,

Front-end Procecessor Adapter.

RCSL Nr. 46-F 0087

A/S REGNECENTRALEN
af 1979

Keywords:

RC8000, RC8401, FPA 803, Peripheral Device, Fron-end Processor Adapter, Technical Manual.

Abstract:

This publication is a Technical description of the front-end processor adapter - FPA803 - designed to connect the RC8000 computer to the RC3600 or RC3500 computer.

(134 printed pages).

Printed by A/S Regnecentralen af 1979, Copenhagen

RCSL Nr. 46-F 0087

FOREWORD.

FCO 18-075 is included in this documentation.

CONTENTS PAGE

CONTENTS (continued) PAGE

CONTENTS (continued) PAGE

CONTENTS (continued) PAGE

The FPA 801 is an asynchronous controller intended for use as interconnecting medium between the RC 8000 computer and the RC 3600 / RC 3500 computer.

FPA 801 contains two sub-devices, called the TRANSMITTER and the RECEIVER.

Althougth transmission cannot take place in both directions simultaneously, the FPA 801 acts from a programmers point of view as two independent devices, each running their own program simultaneously.

FPA 801 is constructed around a 24 bits wide tree-state bus (refer to BLOCK-DIAGRAM SECTION 3.1.2)

Sources to the bus are:

1. Register ALU (AM 2901)
2. Data Selector, which gates following registers to the internal bus:
   a.) Device selector switch
   b.) I/O DATA-IN register
   c.) Constant Proms
   d.) Receiver Character register

Destinations on the bus are:

1. Register ALU (AM 2901)
2. Data selector, which routes data to the transmitter character register
3. I/O DATA-OUT Register
4. I/O ADDRESS Register
5. Parity checker / generator

Transfer of data between registers on the bus is under control of the microprogram, which executes following macroinstructions under control of the RC 8000 computer:

a.) Read receive characters from the opposite controller
b.) Write transmit characters to the opposite controller
c.) Sense transfer status to RC 8000 memory

d.) Control — send autoload signal or transmit an all zero character

e.) Wait — wait for an attention event or a new start

f.) Stop — stop channel program

The Register ALU holds the following 16 registers, of which 8 are assigned to the transmitter and 8 are assigned to the receiver:

0. Description Address
1. Channel Program Address
2. First Word Address
3. Character Counter
4. Buffer
5. Remaining Char. Count
6. Event status
7. Command register

The transmitter and receiver register names are identical.

Besides the above mentioned registers the Register ALU contain an arithmetic logic unit, which is used when counters and address registers has to be incremented / decremented and when status bits in the status register is set and cleared.

I/O DATA register and I/O ADDRESS register are via TEXAS 75138 transceivers connected to the RC 8000 standard bus. When I/O DATA register and I/O ADDRESS register data are present on the internal bus the parity is generated / checked by the Parity checker / generator.

Communication with RC 8000 takes place via the standard unified bus. Operations are initrated by means of an output operation, which addresses the receiver or the transmitter. Hereafter the communication takes place via a channel program stored in the memoty. Once started FPA 801 fetches its commands in the channel program and executes the commands without the engagement of the CPU. Data to be written or read from front end are transferred directly between FPA 801 and memory.

When the channel program has been executed, it is normally terminated with a STOP command which transfers status to memory and interrupts the CPU.

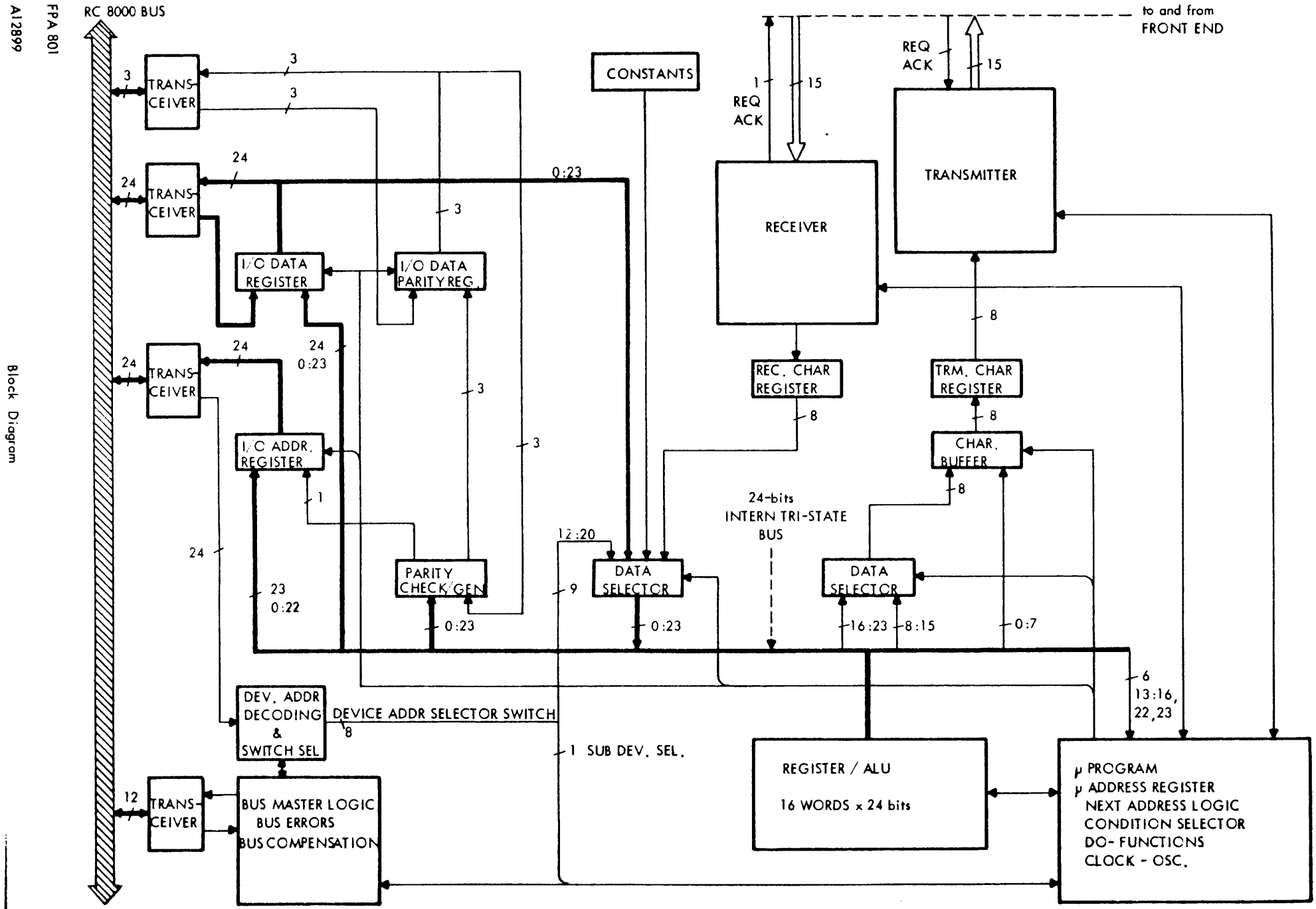
The communication with the opposite controller takes place via a set of output and a set of input lines. The output lines and input lines are completely symmetrical, each set consisting of:

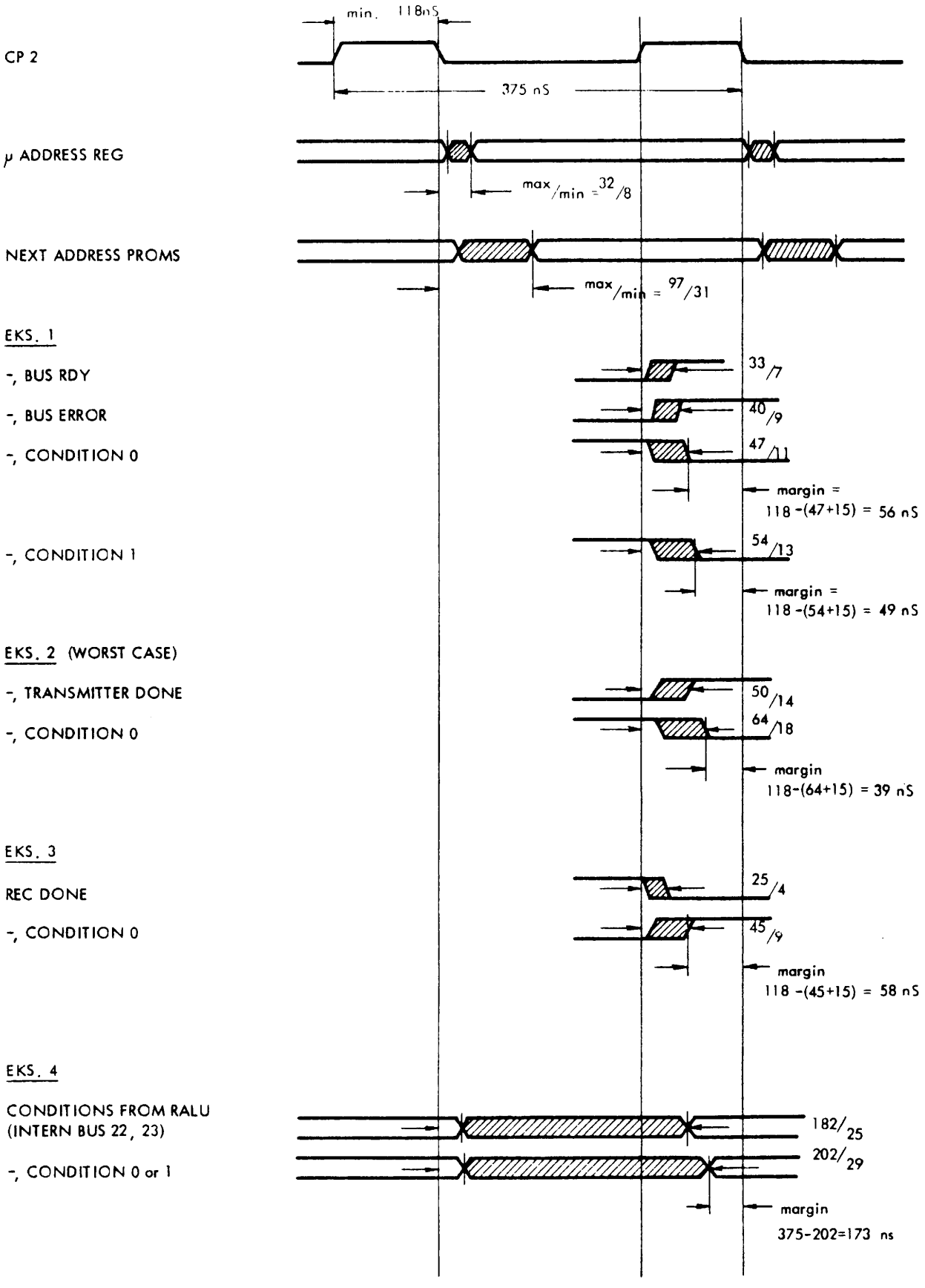
9 data lines incl. a parity line

7 control lines

Included in the control lines is an autoload request line, which is necessary to be able to initiate an autoload procedure in the opposite controller under RC 8000 program control and vice versa. The communication is asynchronous on character basis.

A12899 FPA 801 Block Diagram





800220 VH 800703 JOM

SHADED AREAS = UNDEFINED STATE

FPA 802

A13862

NEXT ADDRESS TIMING

Timing Chart

TC 1

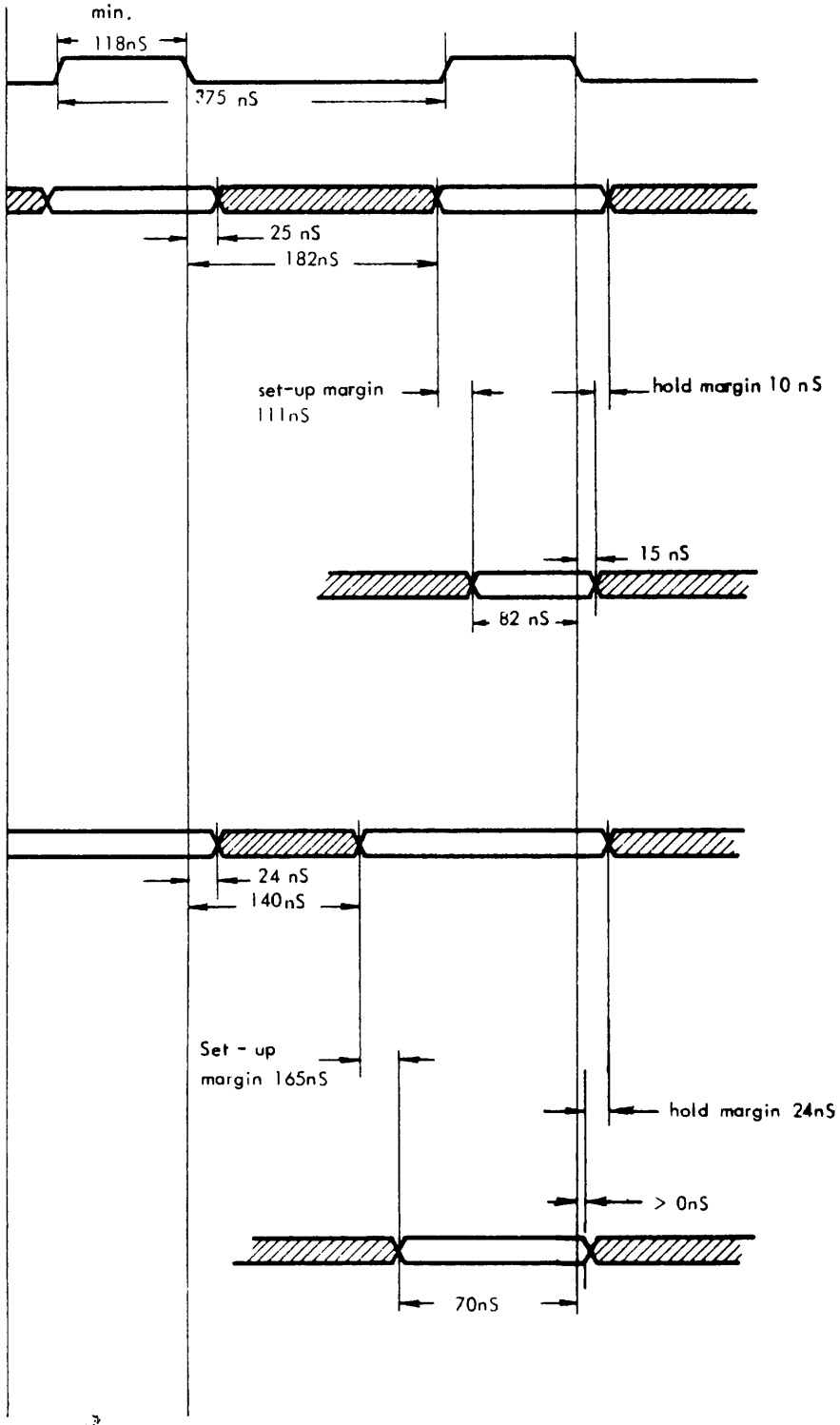
CP 2

INTERNAL BUS
(DATA FROM REGISTER
ALU)

The min value is composed of :

CP 2 → µADDR. REG.	8
µADDR REG.→SOURCE ADDR	12
SOURCE ADDR →BUS	5
	~ 25 nS

The RALU sends data to TRANSMITTER BUFFER or I/O DATA REGISTER or I/O ADDRESS REGISTER. These REGISTERS demands the INTERNAL BUS to be defined as follows :



INTERNAL BUS
(DATA FROM BUS DATA
SELECTOR)

The max. value is composed of :

CP 2 →µADDR. REG	32 nS
µADDR. REG → SOURCE ADDRESS	87 nS
SOURCE ADDR →BUS	21 nS
	~ 140 nS

Data from data selector are send to the RALU via the bus. The RALU demands the bus to be defined as follows :

800220 VH 800703 JOM.

82.09.01 VH 82.09.06 ABP

FPA803

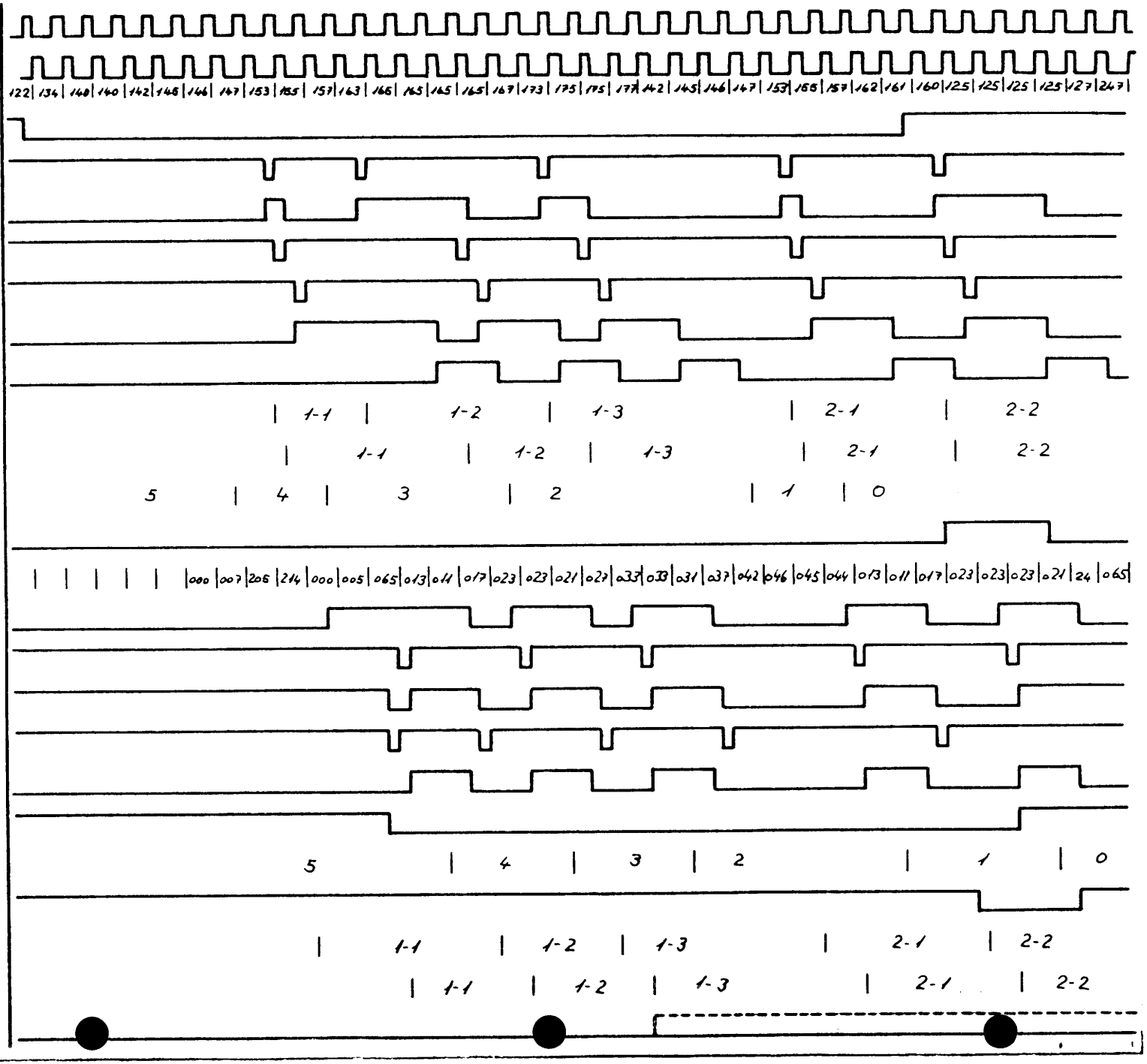
A14246

TRANSMIT/RECEIVE TIMING

(Transmit and Receive 5 characters)

Timing Chart

B1	1	53-11
B2	1	53-9
AT TRANSMITTER		
TRM. BLCK. END	26	33-9
-; CLEAR TRM. DONE	11	42-13
-; TRM DONE	26	32-6
-; CHAR RDY	26	13-7
-; SET REQUEST	26	13-9
REQUEST OUT	26	12-5
REQ ACK IN	26	63-10
TRM CHAR BUFF	27	
TRM CHAR REG	27	
CHAR COUNTER	RALU	
LAST CHAR OUT	26	12-9
AT RECEIVER		
REQUEST IN	2	83-9
-; SET ACK	28	62-9
RECEIVER DONE	28	64-9
-; CLEAR REC DONE	11	42-14
REQ ACK OUT	28	64-6
RECEIVE BLCK END	28	100-9
CHAR COUNTER	RALU	
-; LAST CHAR IN	31	129-5
DATA RECEIVER 0-7	29	
REC CHAR REG 0-7	28	
PARITY ERROR	28	100-7



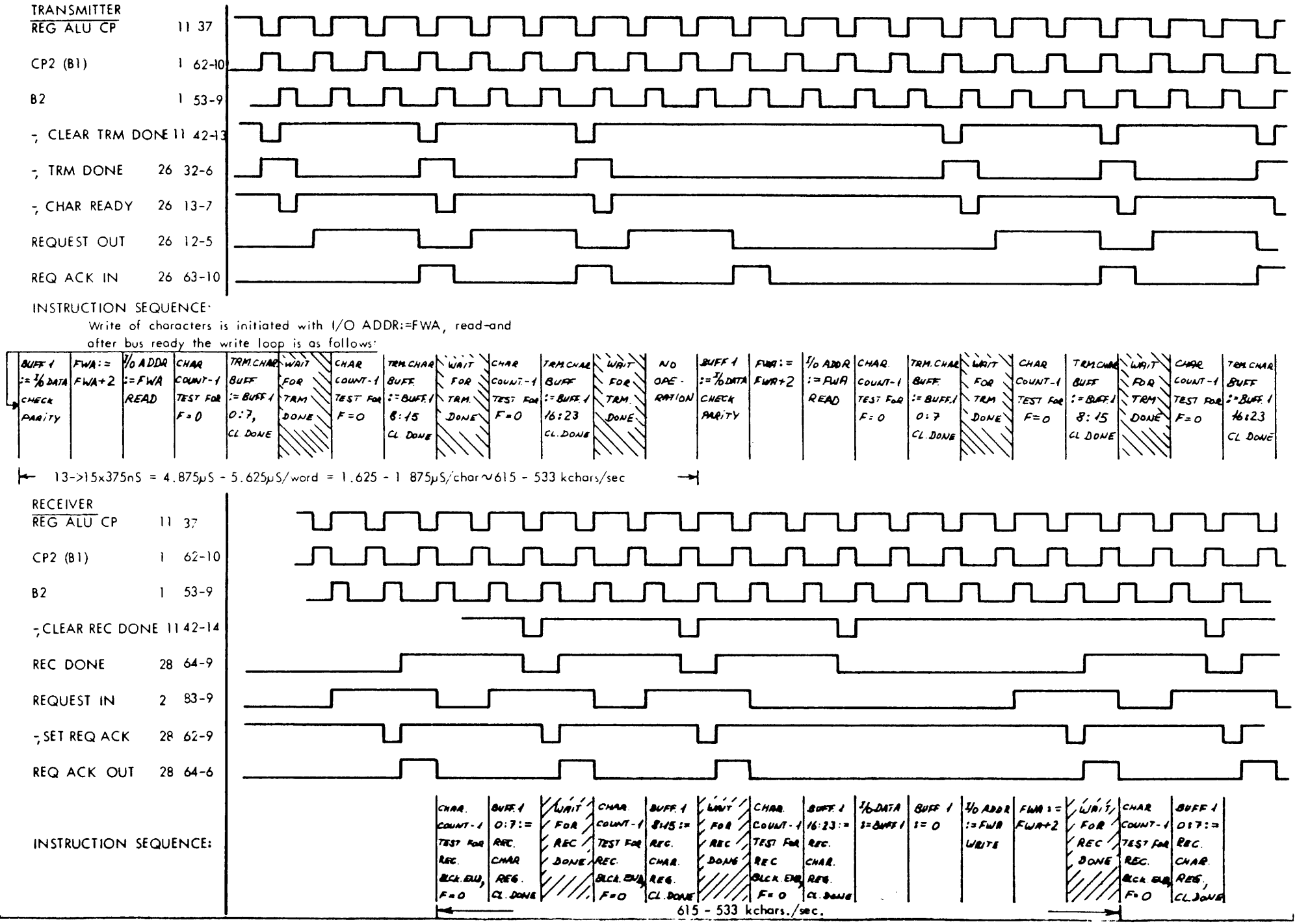
TC 3

TRANSMIT/RECEIVE TIMING DETAIL and calculation of max transmission rate

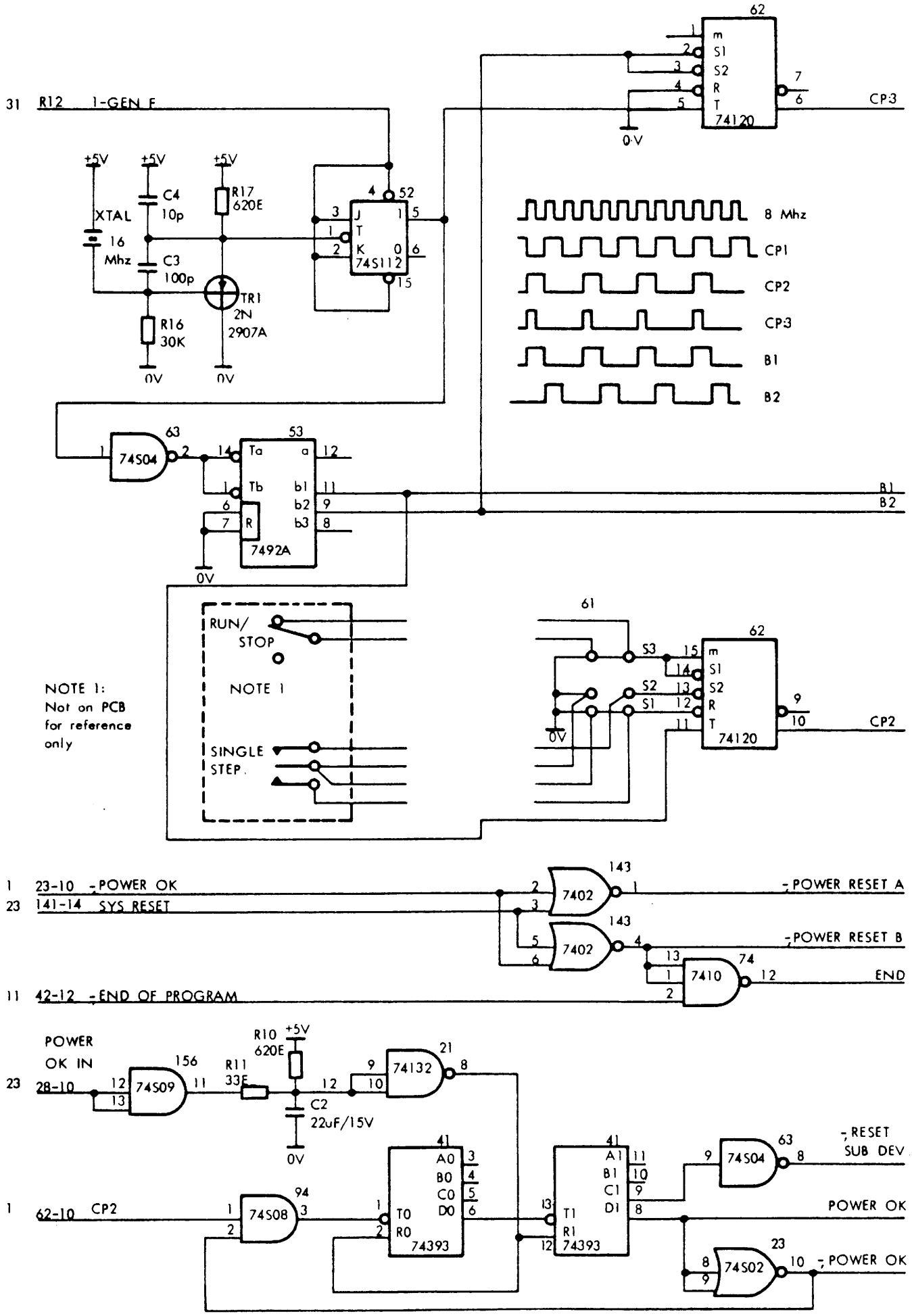
(transmission between 2 FPA 801 s on 10-20 meter cable)

Timing Chart

82.09.01 VH 82.09.06 ABP



SIGNAL	DESTINATION	DESCRIPTION
B 1	26	Clock Pulse ~ 2.666 Mhz.
CP 2	2	Clock Pulse ~ 2.666 Mhz. Period 375 nS, duty cycle 33%.
	3	This CP is used by the μ-address register.
	4	
	11	Clock Pulses to RALU are derived from this pulse.
CP 3	4	Clock Pulse ~ 2.666 Mhz. Period 375 nS, duty cycle 16.6%. This clock pulse strobes the write signal to the μ-address store.
END	2	END signals the end of a channel program.
	26	The signal is also high during the Power Reset condition.
	28	
-, POWER RESET A	4	
	23	
	25	
	26	
-, POWER RESET B	2	
POWER OK	18	This signal together with MASTER and DATA OUT strobes DATA and ADDRESS to RC 8000 BUS.
	21	
-, POWER OK	23	
	30	
-, RESET SUB DEV	4	This signal resets the SUB DEV SEL FF to select of the receiver during power reset, thus inhibiting generation of a RESET LINE OUT signal when POWER OK becomes true.
B 2	2	Clock pulse 2.666 Mhz.
	26	
	28	



82.09.01 VH 82.09.06 ABP Rev. 83.03.03 ABP

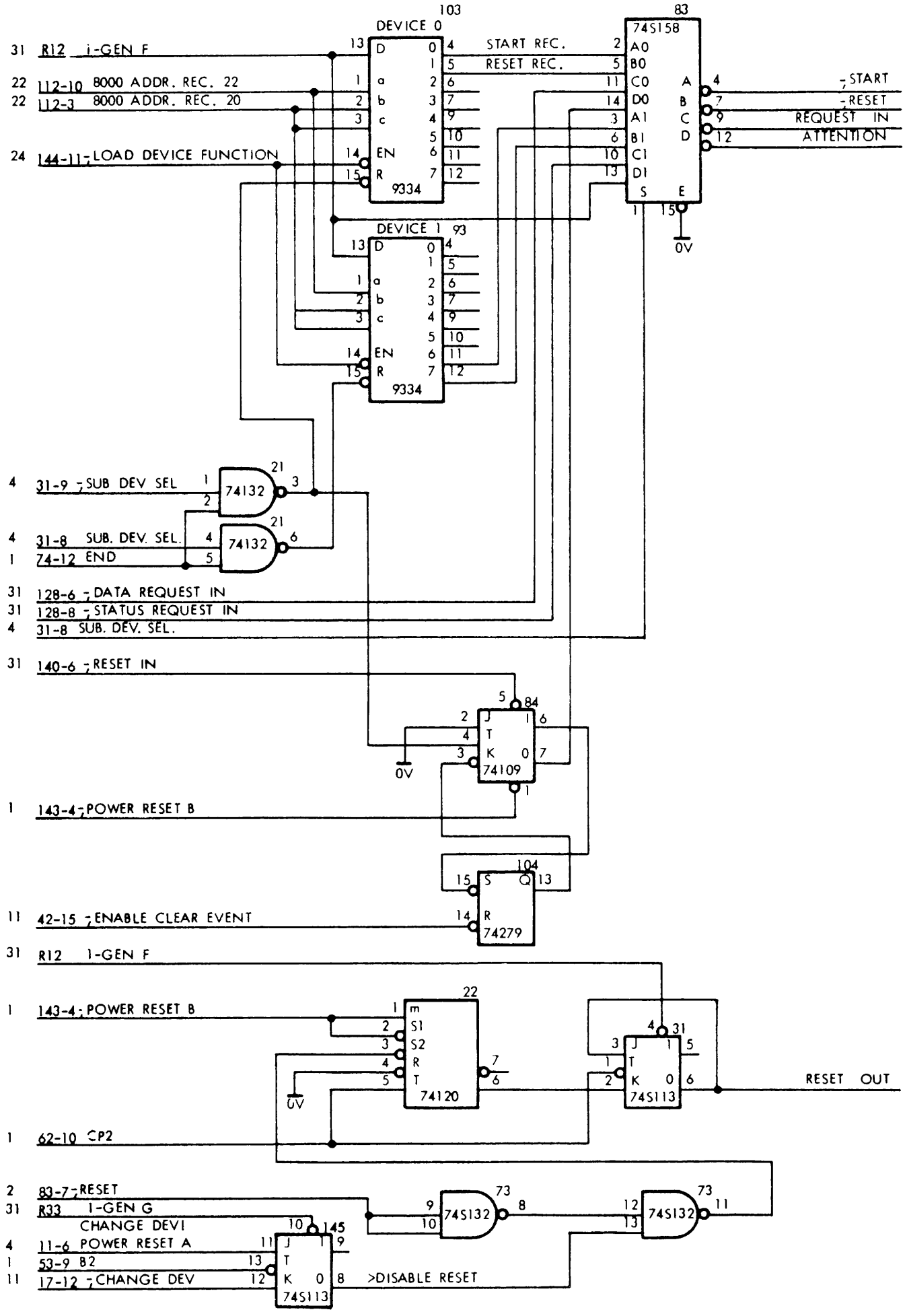
FPA803

A14249

CLOCK OSC. & POWER RESET

Circuit diagram

SIGNAL	DESTINATION	DESCRIPTION
ATTENTION	5	Reset signal received from opposite controller.
-,RESET	5	Device function "Reset unit."
RESET OUT	3 5 11 30	Reset signal to opposite controller. The signal is also used to initiate the μ - address logic
REQUEST IN	5 28	Data or status Request from opposite controller
-,START	5	Device function "Start Channel Program."

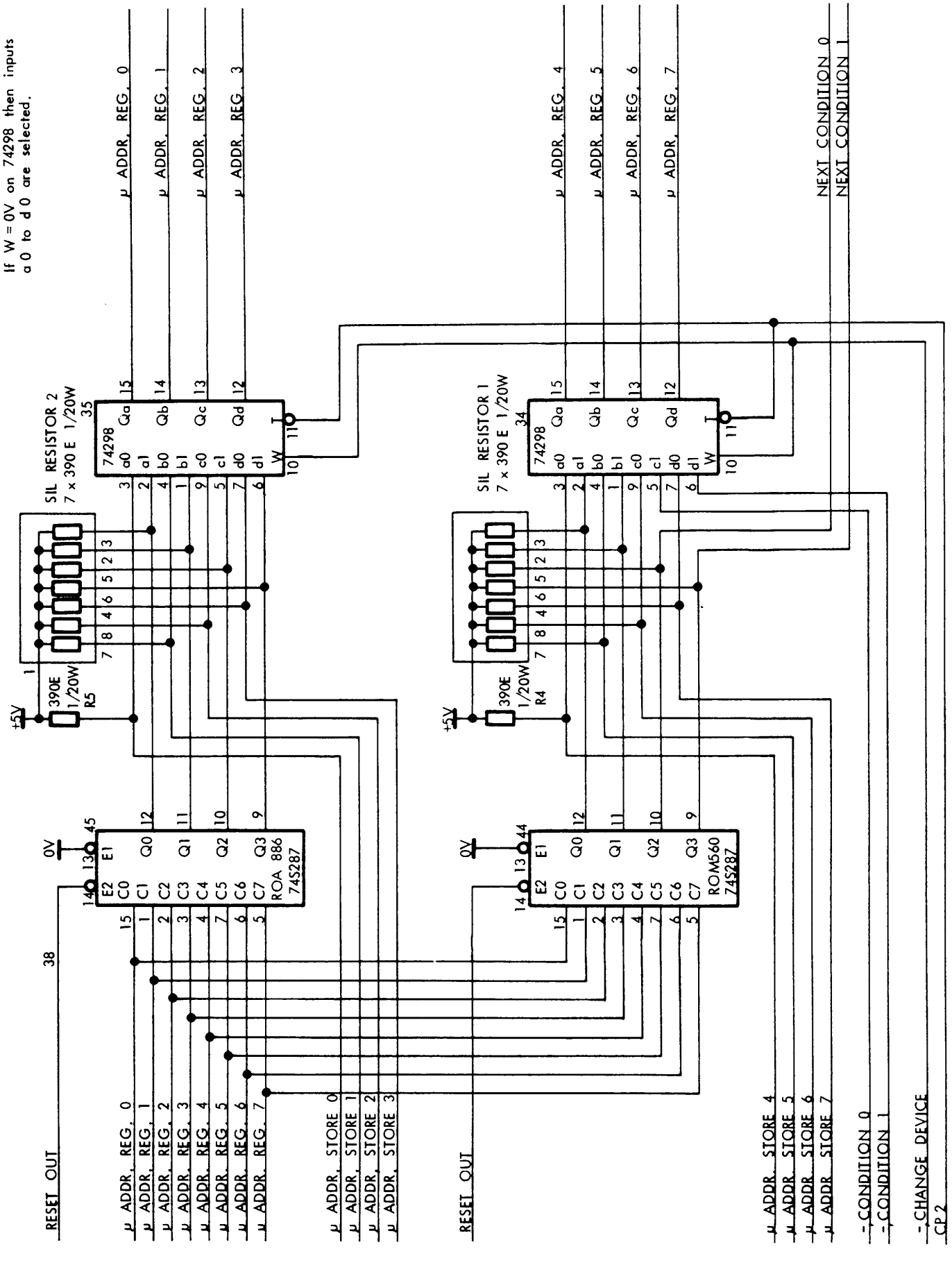


82.09.01 VH 82.09.06 ABP Rev. 83.03.03 ABP

FPA803 DEVICE FUNCTIONS START & RESET 2

A14250 Circuit diagram

SIGNAL	DESTINATION	DESCRIPTION
μ ADDR. REG 0-7	4 5 10 11 12	μ Address Register is used as address to the micro program PROM'S.
NEXT CONDITION 0	5	Next Condition 0 and 1 is generated by the micro program and may be used as the two least significant bits of the next micro address.
NEXT CONDITION 1	5	Refer to next Condition 0



840131 VH 841109 OKJ

FPA803

A14747

μ ADDRESS REGISTER

Circuit Diagram

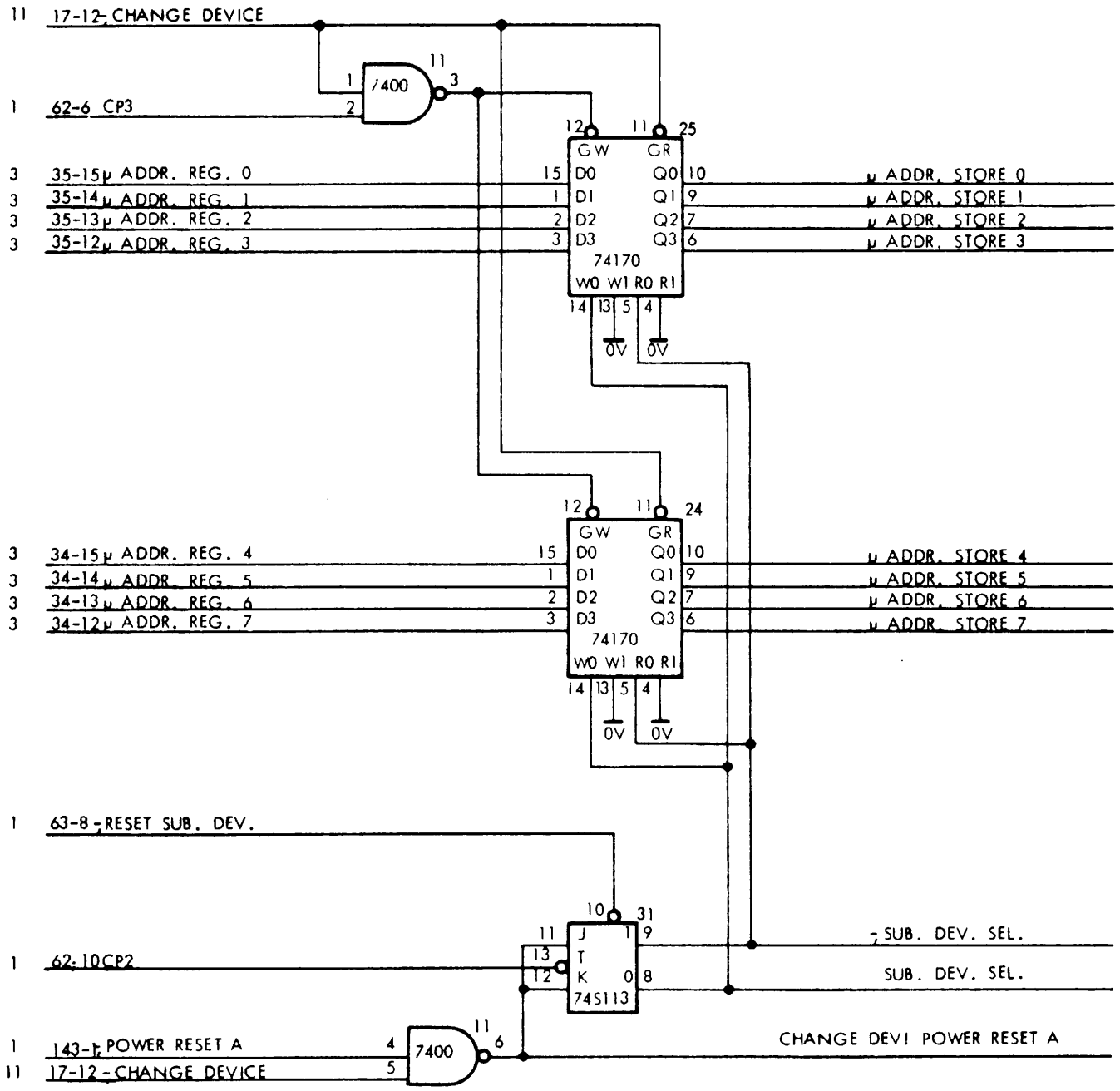
SIGNAL	DESTINATION	DESCRIPTION
u ADDR STORE 0-7	3	The μ Address Store consists of two words, one word for the RECEIVER part of FPA 802 and one word for the TRANSMITTER. The store holds the micro address of the subdevice not currently running.
SUB DEV SEL	2	The Sub Device Selector FF indicates which sub device is currently running.
	5	
	6	
	7	
	8	
	12	
	15	
-, SUB DEV SEL	2	
	30	
CHANGE DEV! POWER RESET A	2	This signal is used to inhibit the RESET OUT signal during change of sub device.

Designed by

Drawn by

Dwg. Office Check

Unit		
FPA803	μ ADDRESS STORE	
Dwg. No. A26049		4

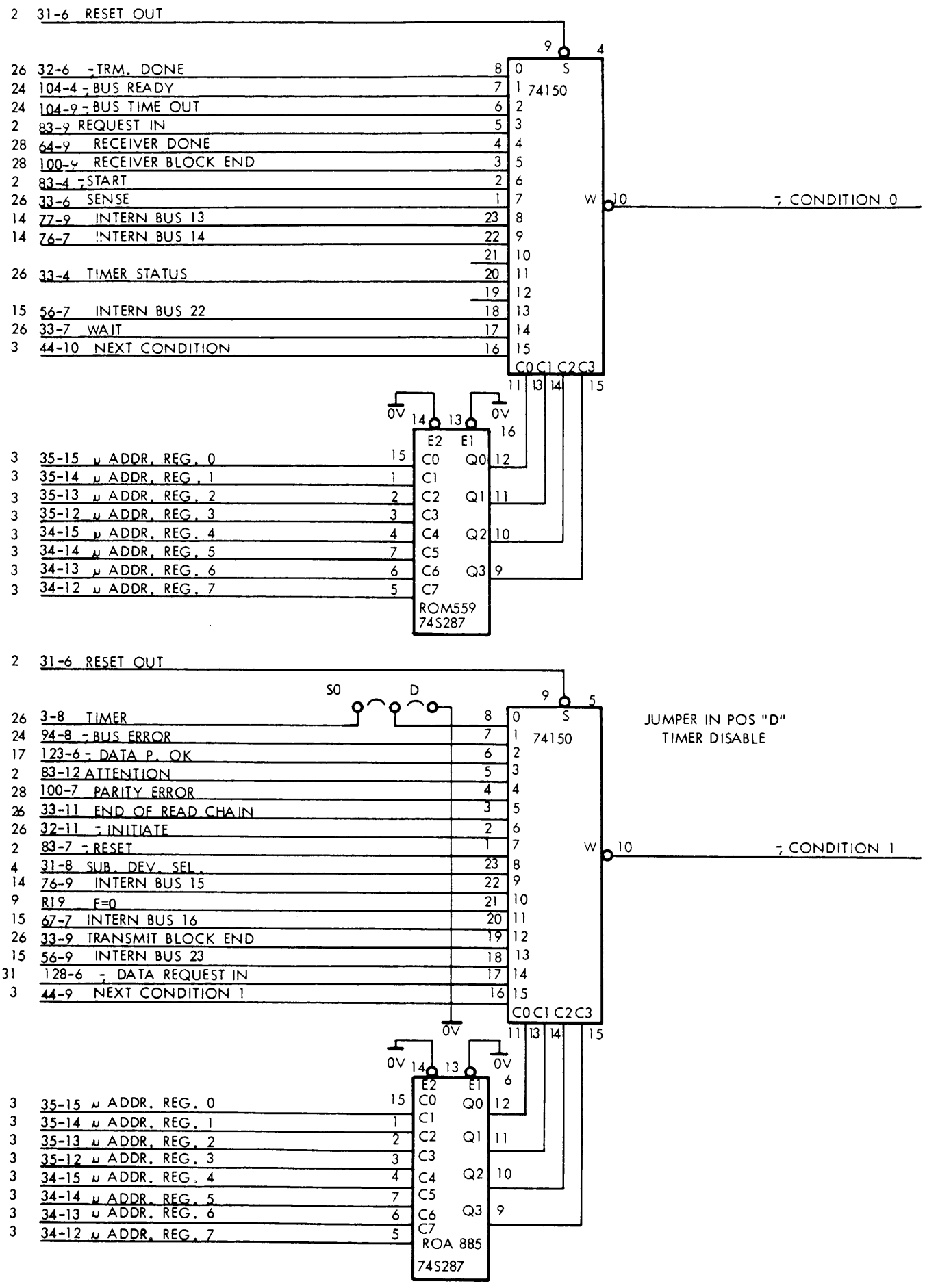


ADDRESS	1	0	
WORD 0	0	0	RECEIVER μ ADDR. STORE
WORD 1	0	1	TRANSMITTER μ ADDR. STORE
WORD 2	1	0	NOT USED
WORD 3	1	1	NOT USED

SUB. DEV. SEL. = "1" ~ TRANSMITTER
SUB. DEV. SEL. = "0" ~ RECEIVER

82.09.01 VH 82.09.06 ABP Rev. 83.03.03 ABP

SIGNAL	DESTINATION	DESCRIPTION
-,CONDITION 0 -,CONDITION 1	3 3	The two outputs from the condition selector is always used as the two least significant bits of the micro address. Condition 1 is the least significant bit. By means of this selector two conditions can be selected at a time, thus making itpossible to, jump to 4 different micro addresses. The 2 x 15 conditions is selected by the micro program via the PROM'S IC 57 and IC 59.



840131 VH 841109 OKJ

SIGNAL	DESTINATION	DESCRIPTION
F = 0 0 : 3	9	Diagrams 6, 7, and 8 show the Register-Arithmetic-Logic-Unit (RALU) used in FPA 802. The RALU performs via a micro-program all of the functions associated with the communication. The data outputs and inputs of the RALU are connected to the FPA 802 internal bus.
F = 0 4 : 7	9	
G 0 : 3	9	
G 4 : 7	9	
INTERN BUS 0-7	13	The RALU contains 16 directly addressable, two port, general purpose registers, and one separate Q-register. The Q-register is not utilized in FPA 802. 8 of the general purpose registers are assigned to the receiver part of FPA 802 and 8 are assigned to the transmitter part. The registers, which have the same meaning in both sub-devices, hold the following information:
P 0 : 3	9	
P 4 : 7	9	

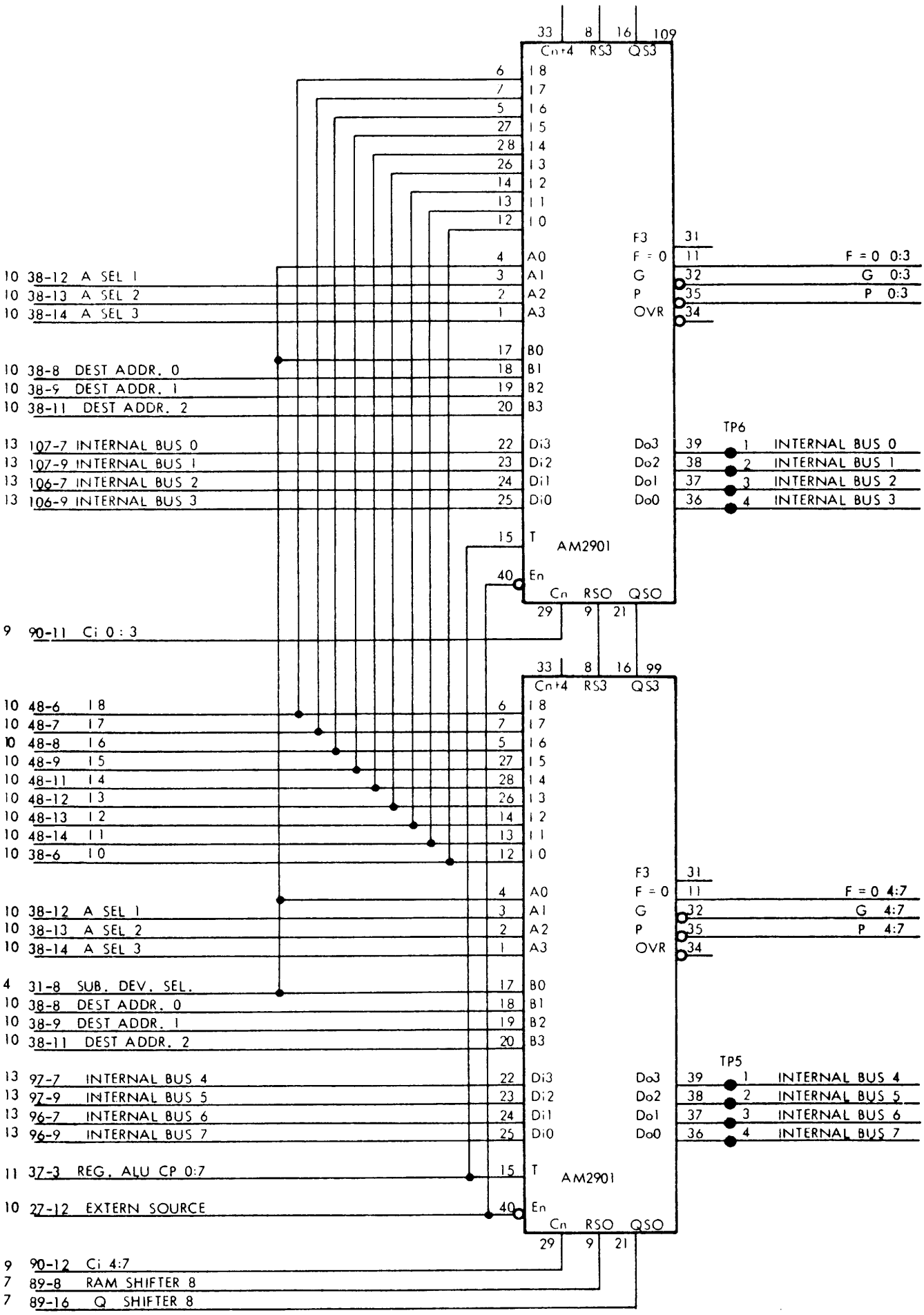
0: Description Address
1: Channel Program Address
2: First Word Address
3: Character Counter
4: Data Buffer
5: Remaining Char. Count
6: Event Status
7: Command Register

The registers are addressed via the micro-program by means of A SEL 1-3 and Destination address 0-2.

Designed by

Drawn by

Dwg. Office Check



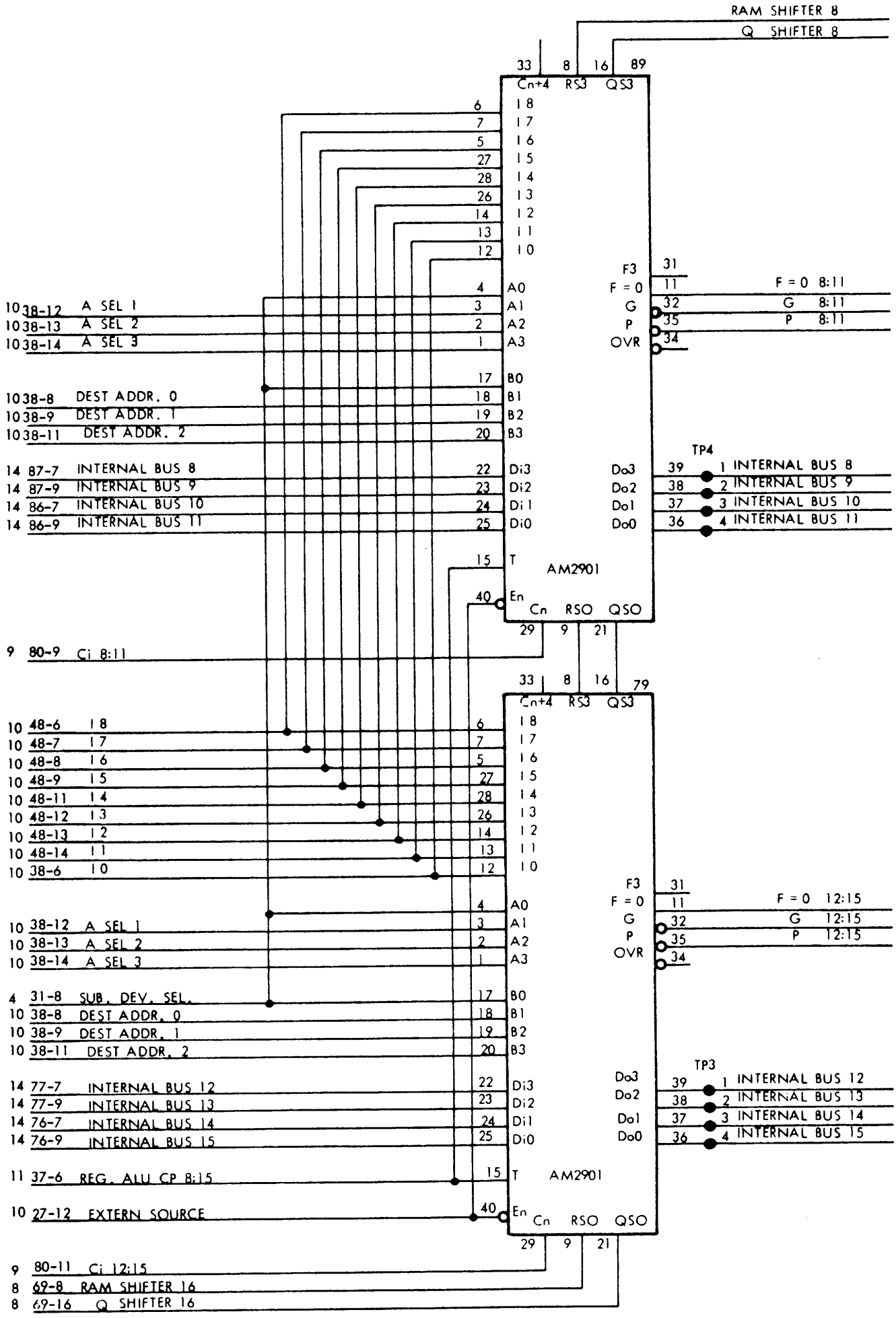
82.09.01 VH 82.09.06 ABP

SIGNAL	DESTINATION	DESCRIPTION
		Continued from Diagram 6
F = 0 8 : 11	9	The RALU function to be executed is under control of the instruction bits 0-7, which are generated by the microprogram. The FPA 802 RALU is connected to utilize the carry look-ahead technique, which makes a cycle time of 215 nS possible, however, additional time is required for the micro Address Register and the RALU address/function PROM's to settle so the total cycle time becomes 305 nS.
F = 0 12 : 15	9	
G 8 : 11	9	
G 12 : 15	9	
INTERN BUS 8 : 15	13	
P 8 : 11	9	G and P outputs are the conventional carry generate and carry propagate signals associated with the look ahead technique.
P 12 : 15	9	
Q SHIFTER 8	6	The F = 0 outputs indicate that the output of the alu is all zeroes. These outputs are all wired together and used as a condition in the microprogram.
RAM SHIFTER 8	6	

Designed by

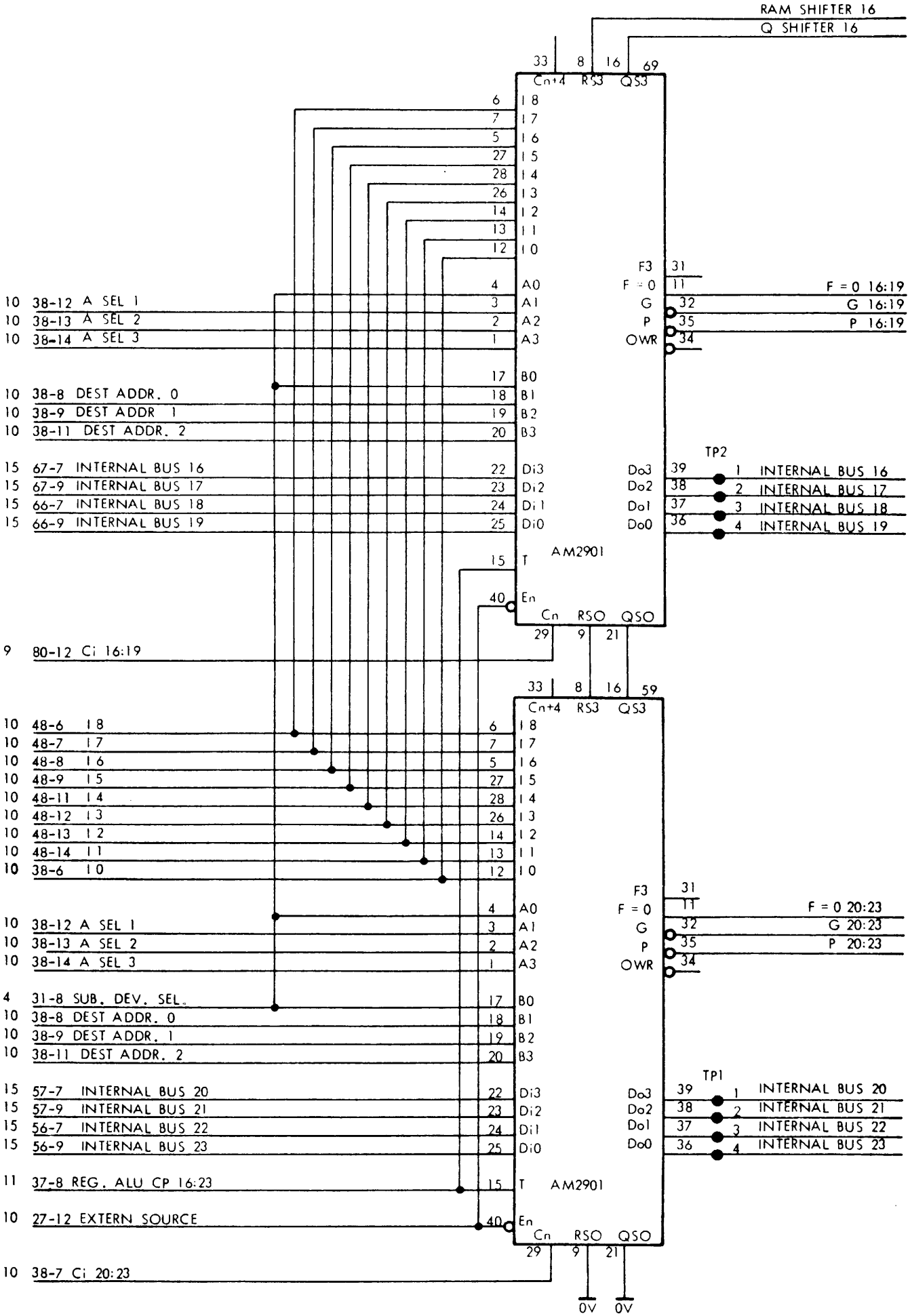
Drawn by

Dwg. Office Check



82.09.01 VH 82.09.06 ABP Rev. 83.03.03 ABP

SIGNAL	DESTINATION	DESCRIPTION
F = 0 16:19	9	
F = 0 20:23	9	
G 16:19	9	
G 20:23	9	
INTERN BUS 16:23	13	
P 16:19	9	
P 20:23	9	
Q SHIFTER 16	7	
RAM SHIFTER 16	7	



82.09.01 VH 82.09.06 ABP

FPA803

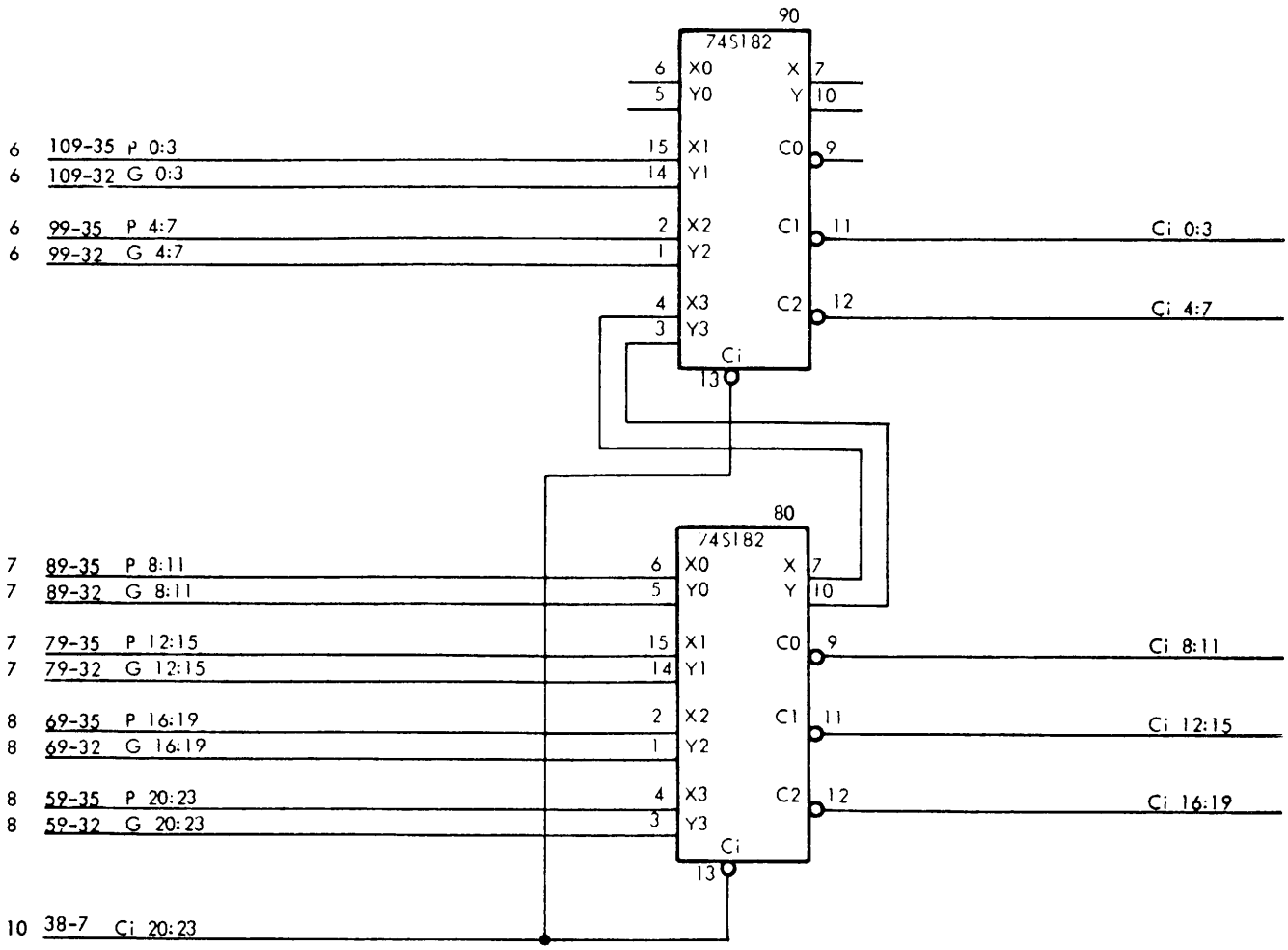
A14256

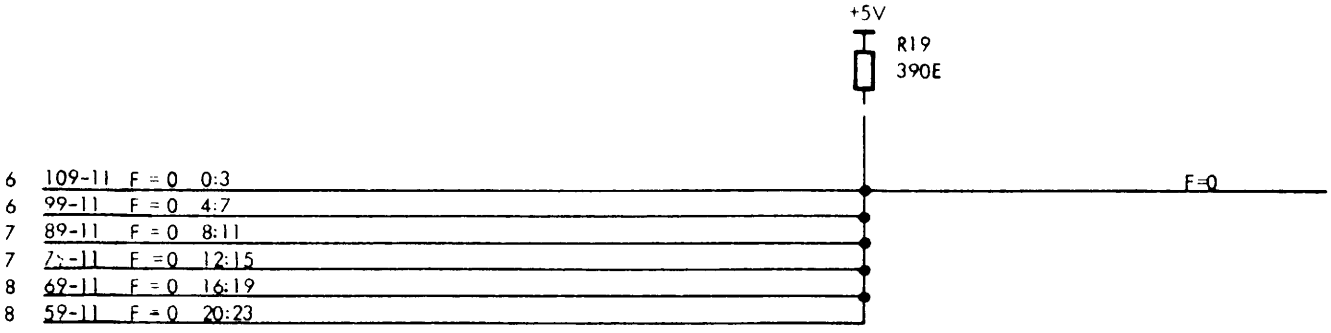
μ CONTROLLER BIT 16:23

Circuit diagram

SIGNAL	DESTINATION	DESCRIPTION
Ci 0 : 3	6	This diagram shows the carry look ahead circuits. The generated Ci outputs are lead to the carry inputs of the respective RALU sections.
Ci 8 : 11	7	
Ci 12:15	7	
Ci 16:19	8	
Ci 4 : 7	6	
F = 0	5	The F = 0 output is a wired - or result of the F = 0 outputs from the different RALU sections. The output is terminated with a 390 E resistor since the F = 0 outputs from RALU sections are open - collectors.

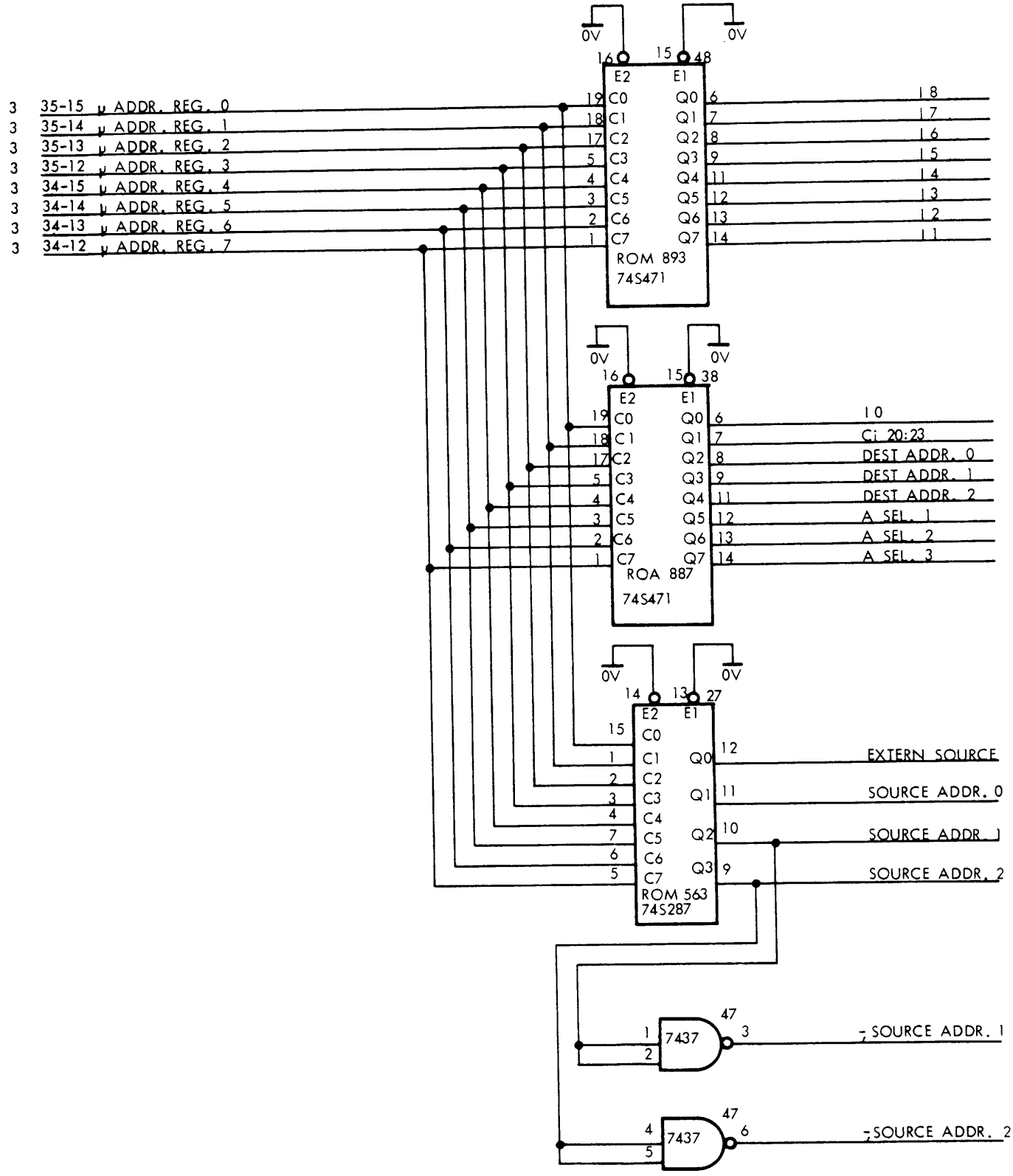
Unit		
FPA803	CARRY LOOK AHEAD & F = 0.	
Dwg. No. A26054		9





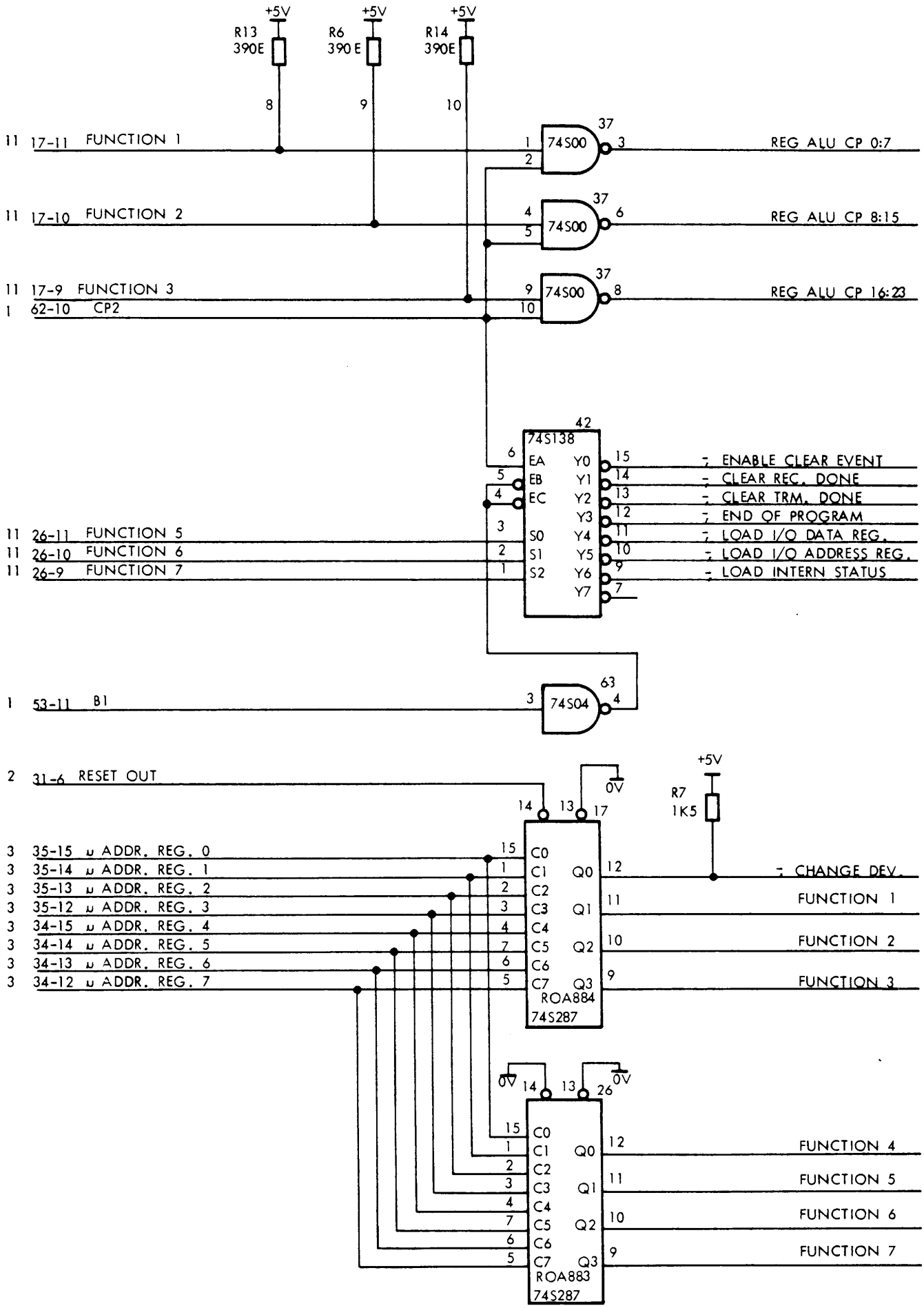
82.09.01 VH 82.09.06 ABP

SIGNAL	DESTINATION	DESCRIPTION
A SEL 1-3	6, 7, 8	The PROM's in this diagram are primarily used in connection with the RALU. I0-I8 are instruction bits to the RALU. A SEL 1-3 and DEST ADDR 0-2 are A and B address 1-3 to the RALU. SOURCE and DEST addresses are used by some registers outside the RALU.
Ci 20:23	8 9	
DEST ADDR 0-2	6,7,8,26,27	The EXTERN SOURCE signal when logical 1 will gate data from the DATA selector to the internal bus, while a logical 0 will gate data from the RALU to the internal bus.
EXTERN SOURCE	6	
	7	Ci 20:23 signal is the carry input to the least significant bit of the RALU.
	8	
	13	
	14	
I0-I8	6, 7, 8	
SOURCE ADDR 0	12	
-, SOURCE ADDR 1	13	
	14	
	15	
-, SOURCE ADDR 2	13	
	14	
	15	



840131 VH... 841109 OKJ

SIGNAL	DESTINATION	DESCRIPTION
-,CHANGE DEVICE	2 3 4	This signal when low causes the Sub Device Selector to change state i.e. the other sub device becomes selected.
-,CLEAR REC. DONE	28	This signal starts the receiver and causes a Request Ack signal to be sent to the opposite controller provided a Request in signal is present.
-,CLEAR TRM. DONE	26	This signal starts the transmitter, loads the transmitter buffer and causes a Request signal to be sent to the opposite controller.
-,ENABLE CLEAR EVENT	2	This signal enables clear of the Reset in FF, which holds the reset received information from the opposite controller.
-,END OF PROGRAM	1	Indicates the end of a channel program.
FUNCTION 1,2,3	This diag.	These bits control the clock pulses to the RALU, and make it possible to transfer 8-bits characters to the RALU.
FUNCTION 4	23 26	This parameter is used to control the Data Out Out FF, and in conjunction with the Load Intern Status signal to set/clear the internal status FF 'S.
FUNCTION 5,6,7	This diag.	These signals are via a 3 to 8 decoder converted to 7 do-functions.
-,LOAD I/O ADDRESS REGISTER.	21 23 24	This signal loads the I/O Address Register from the internal FPA 8u2 bus, and simultaneously a RC 8000 bus transfer is requested.
-,LOAD I/O DATA REG.	18 23	This signal loads the I/O Data Register from the internal FPA 802 bus.
-,LOAD INTERN STATUS	This diag..	Refer to the function 4 signal.
REG ALU CP 0:7	6	Clock pulse to the RALU.
REG ALU CP 8:15	7	Clock pulse to the RALU.
REG ALU CP 16-23	8	Clock pulse to the RALU.

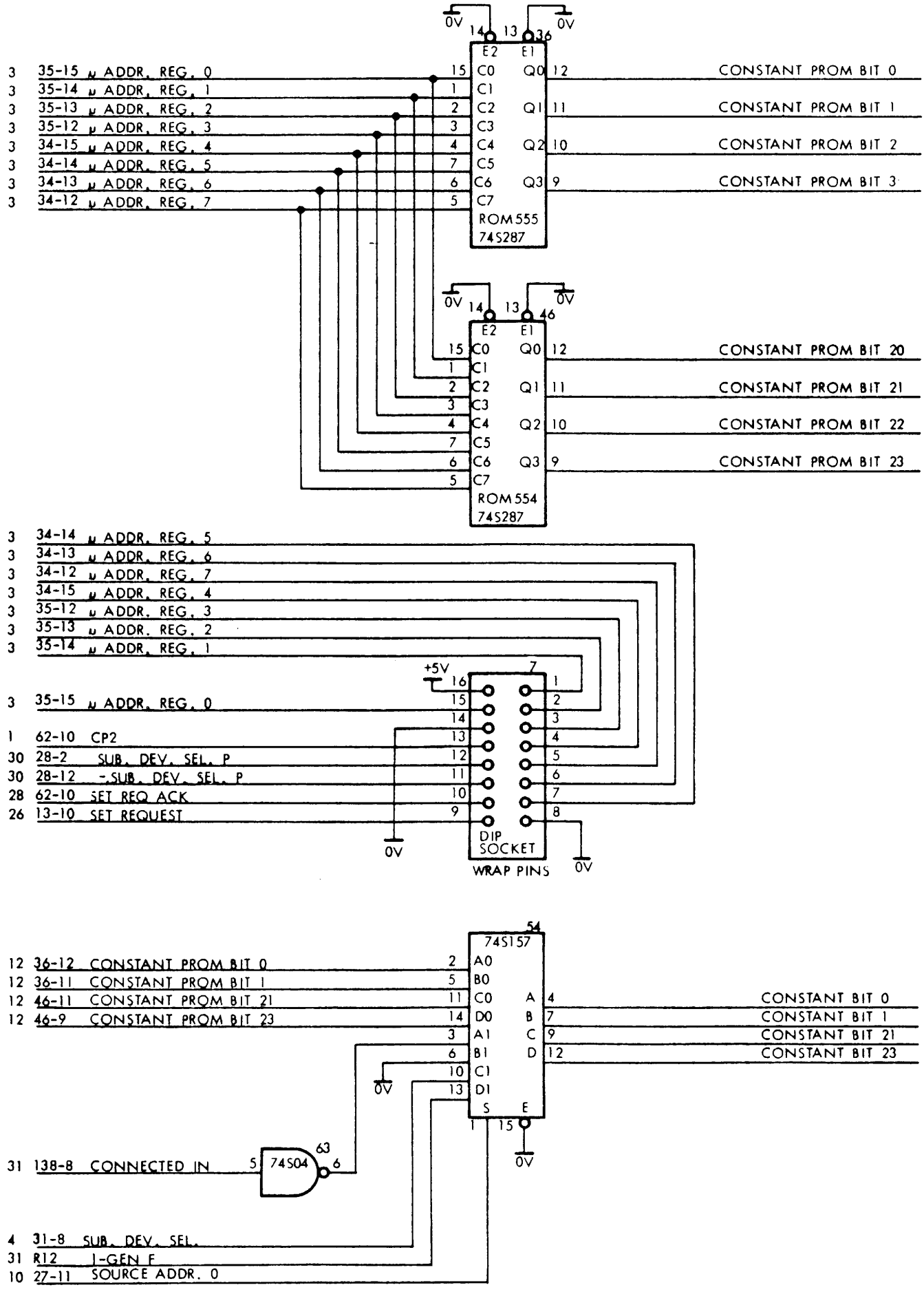


840131 VH 841109 OKJ

FPA803 CONVERTING OF Do-FUNCTIONS F0 to F7 11

A14750 Circuit diagram

SIGNAL	DESTINATION	DESCRIPTION
CONSTANT PROM BIT 0	This diag.	Outputs from the constants circuits are wired to the data selector from which the constants can be send to the internal bus, when the constant PROM'S are selected as source. The constants are used when counters or registers has to incremented or decremented, and when status bits are set.
CONSTANT PROM BIT 1	This diag.	
CONSTANT PROM BIT 2	13	
CONSTANT PROM BIT 4	13	
CONSTANT PROM BIT 20	15	
CONSTANT PROM BIT 21	This diag.	
CONSTANT PROM BIT 22	15	
CONSTANT PROM BIT 23	This diag.	
CONSTANT BIT 0	13	
CONSTANT BIT 1	13	
CONSTANT BIT 21	15	
CONSTANT BIT 23	15	



82.09.01 VH 82.09.06 ABP Rev. 83.03.03 ABP

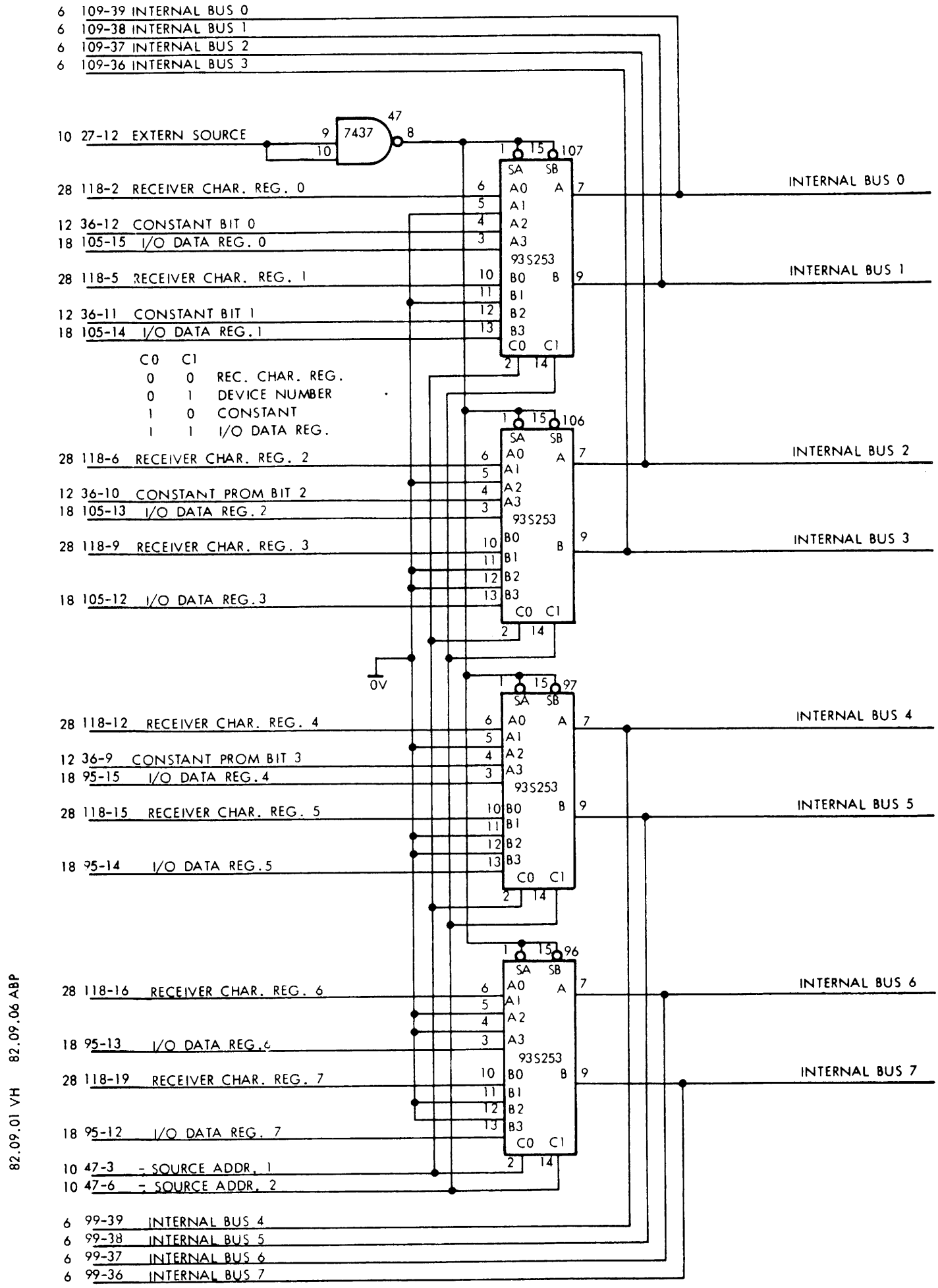
SIGNAL	DESTINATION	DESCRIPTION
INTERNAL BUS 0-23	6, 17, 18, 21, 27	The FPA 802 internal bus is a tri-state bus 24-bits wide. The internal bus has two main sources: 1. The RALU 2. The data selector By means of the data selector 4 different data sources can be gated to the internal bus: 1. RECEIVER CHARACTER REG 2. DEVICE NUMBER SWITCH 3. CONSTANTS 4. I/O DATA REGISTER

Designed by

Drawn by

Dwg. Office Check

Unit		
FPA 802	DATA SELECTOR 0 : 7 TO INTERNAL BUS	
Dwg. No. A25823		13



82.09.01 VH 82.09.06 ABP

FPA803

DATA SELECTOR 0:7 TO INTERNAL BUS

A14263

Circuit diagram

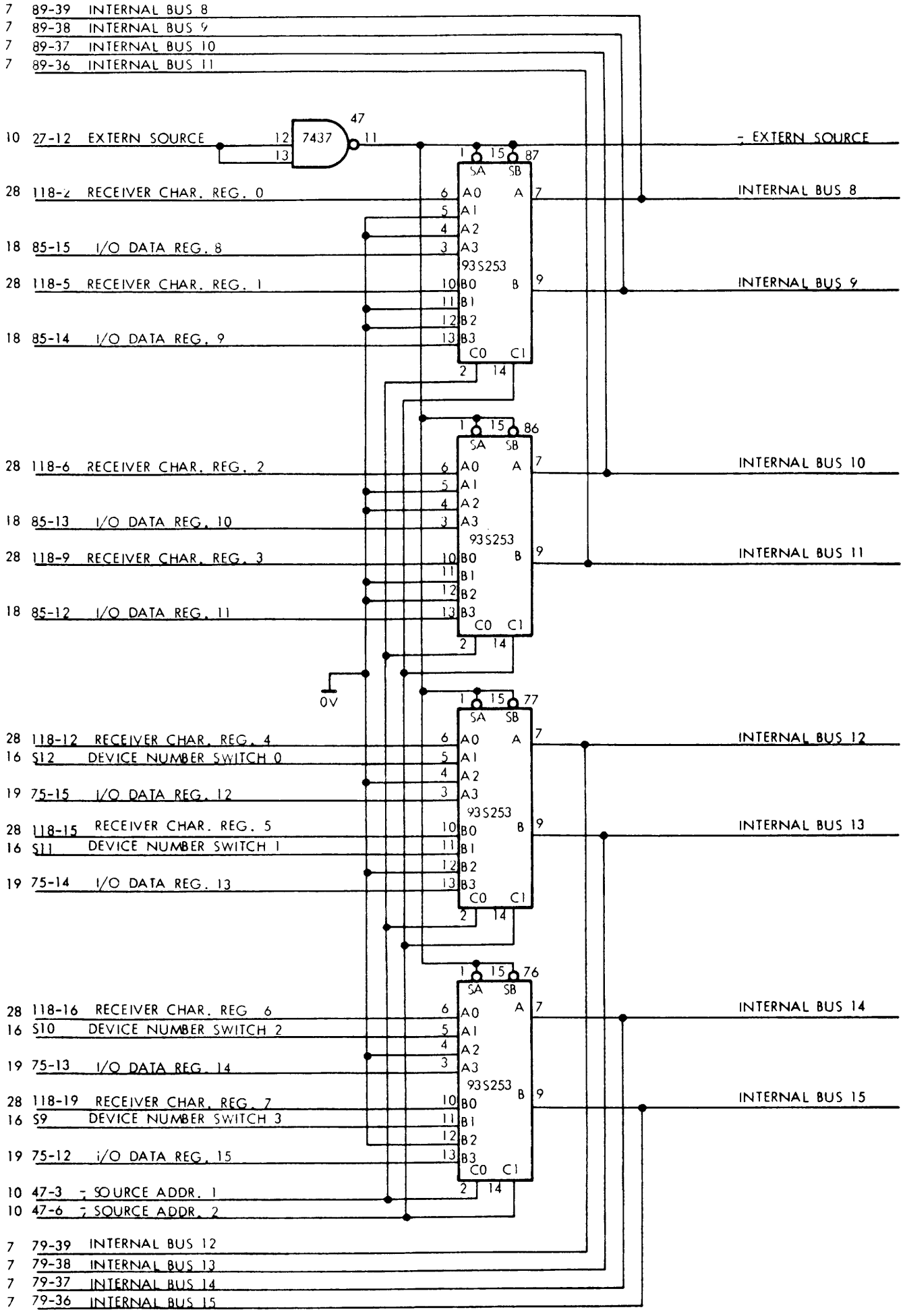
SIGNAL	DESTINATION	DESCRIPTION
INTERNAL BUS 0-23	7, 17, 18, 21, 27	The FPA 802 internal bus is a tri-state bus 24-bits wide. The internal bus has two main sources: 1. The RALU 2. The data selector By means of the data selector 4 different data sources can be gated to the internal bus: 1. RECEIVER CHARACTER REG 2. DEVICE NUMBER SWITCH 3. CONSTANTS 4. I/O DATA REGISTER
-, EXTERN SOURCE	15	

Designed by

Drawn by

Dwg. Office Check

Unit		
FPA803	DATA SELECTOR 8 : 15 TO INTERNAL BUS	
Dwg. No. A26065		14



82.09.01 VH 82.09.06 ABP

FPA803

DATA SELECTOR 8:15 TO INTERNAL BUS

14

A14264

Circuit diagram

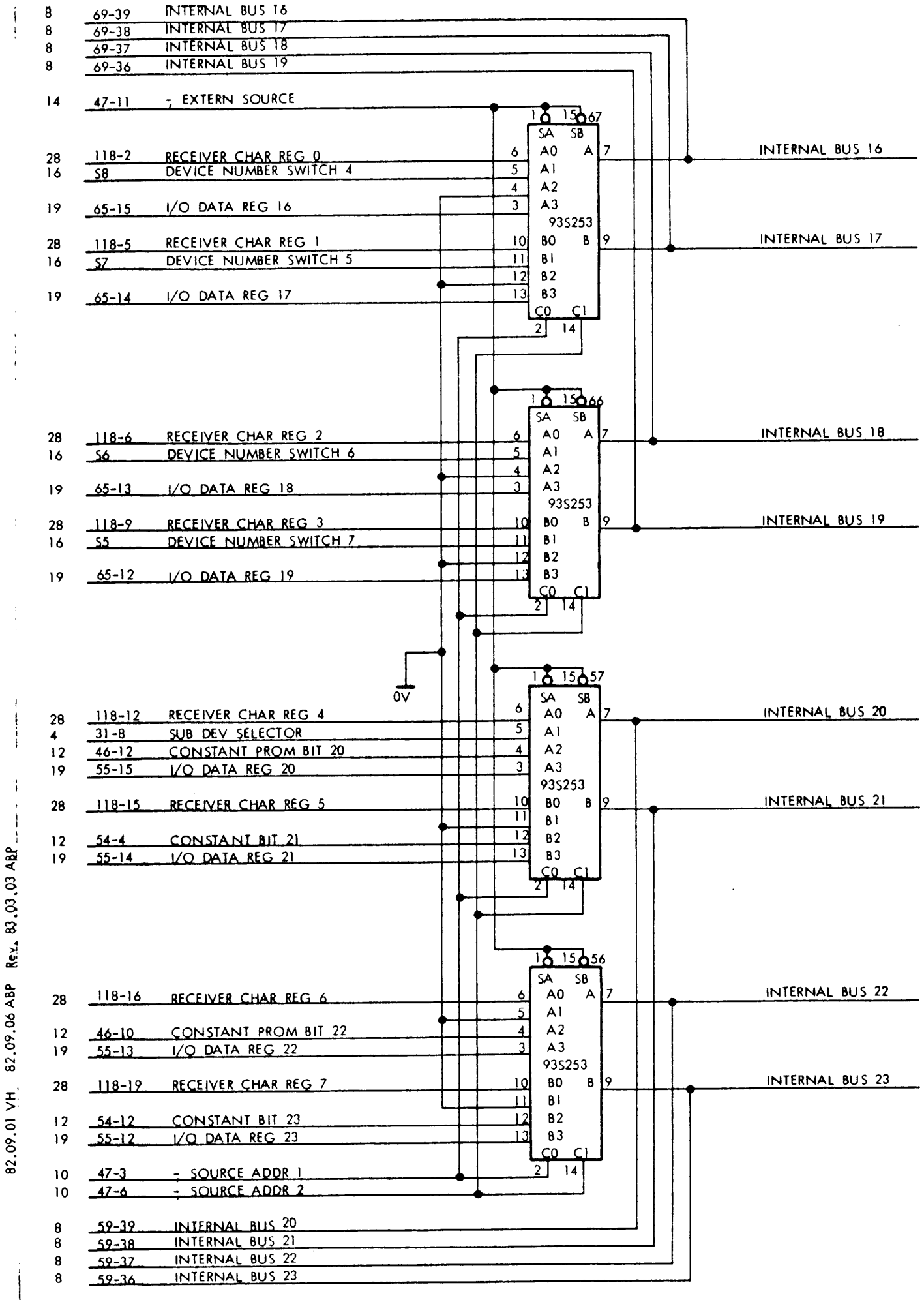
SIGNAL	DESTINATION	DESCRIPTION
INTERNAL BUS 0-23	8, 17, 18, 21, 27	The FPA 802 internal bus is a tri-state bus 24-bits wide. The internal bus has two main sources: 1. The RALU 2. The data selector By means of the data selector 4 different data sources can be gated to the internal bus: 1. RECEIVER CHARACTER REG 2. DEVICE NUMBER SWITCH 3. CONSTANTS 4. I/O DATA REGISTER

Designed by

Drawn by

Dwg. Office Check

Unit		
FPA 802	DATA SELECTOR 16 : 23 TO INTERNAL BUS	
Dwg. No. A25825		15

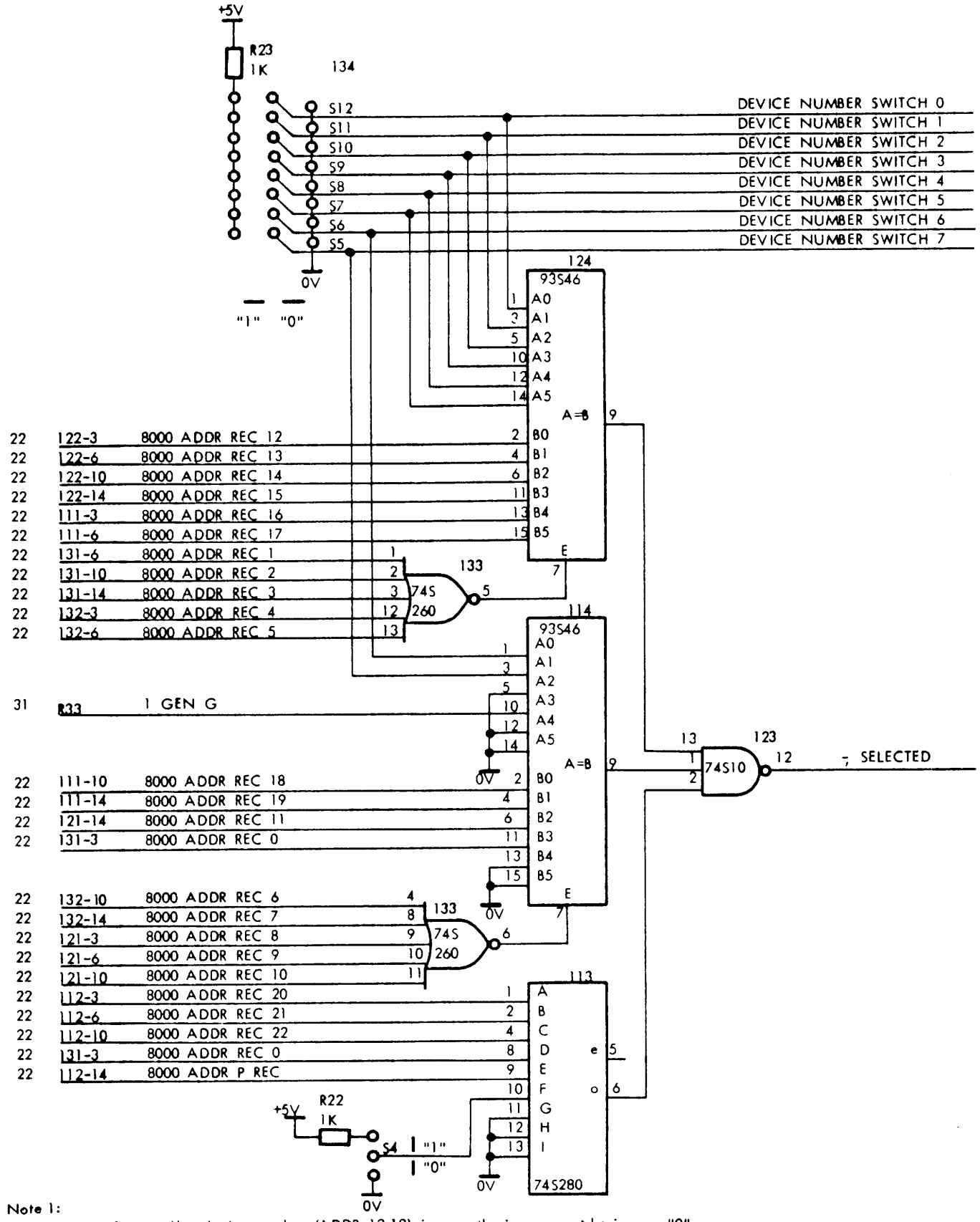


82.09.01 VH 82.09.06 ABP Rev. 83.03.03 ABP

FPA803 DATA SELECTOR 16 · 23 TO INTERN BUS 15

A14265 Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
DEVICE NUMBER SWITCH 0 - 7 (bit 7 = LSB)	15	By means of the device number switch it is possible to change the device number of FPA 801.
-,SELECTED	24	The device number switch is continuously compared with the RC 8000 address bus bits 12 - 19 (bit 20 equal sub-device number). The selected signal is generated when all of the following conditions are fullfilled: 1. Device number coincidence 2. Address bus bits 1-11 = "0" 3. Address bus bits 0 = "1" 4. Parity of address bus = odd When the selected signal becomes logical 1 in a data out instruction to FPA 801, the device function registers are loaded (diagram 2).



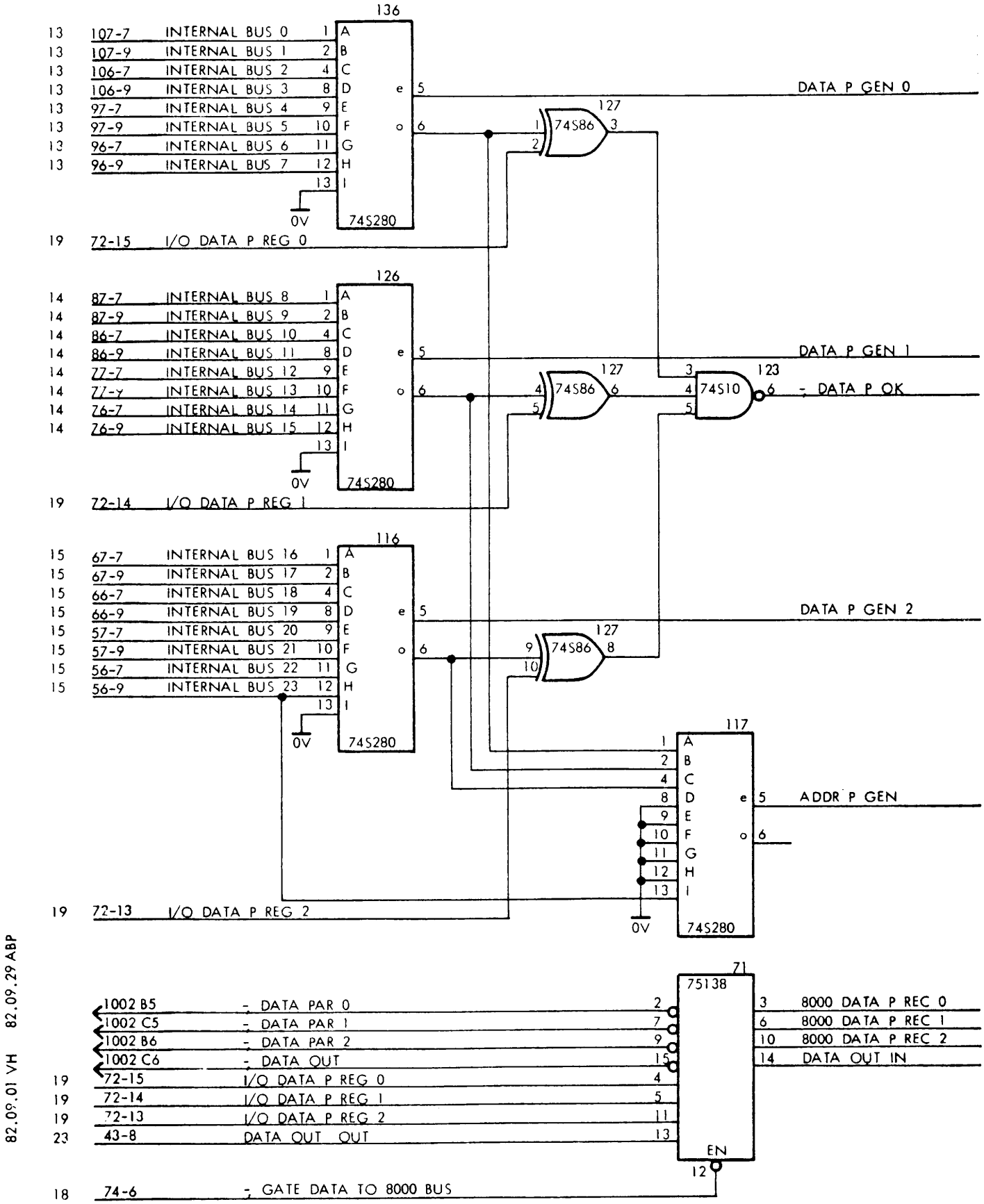
Note 1:
If the parity of controller device number (ADDR 12:19) is even the jumper must be in pos. "0"
If the parity of controller device number (ADDR 12:19) is odd the jumper must be in pos. "1"

74S280	OUTPUT	
Numbers of inputs A->I that are high	e	o
0 - 2 - 4 - 6 - 8	H	L
1 - 3 - 5 - 7 - 9	L	H

82.09.01 VH 82.09.29 ABP Rev. 83.03.03 ABP

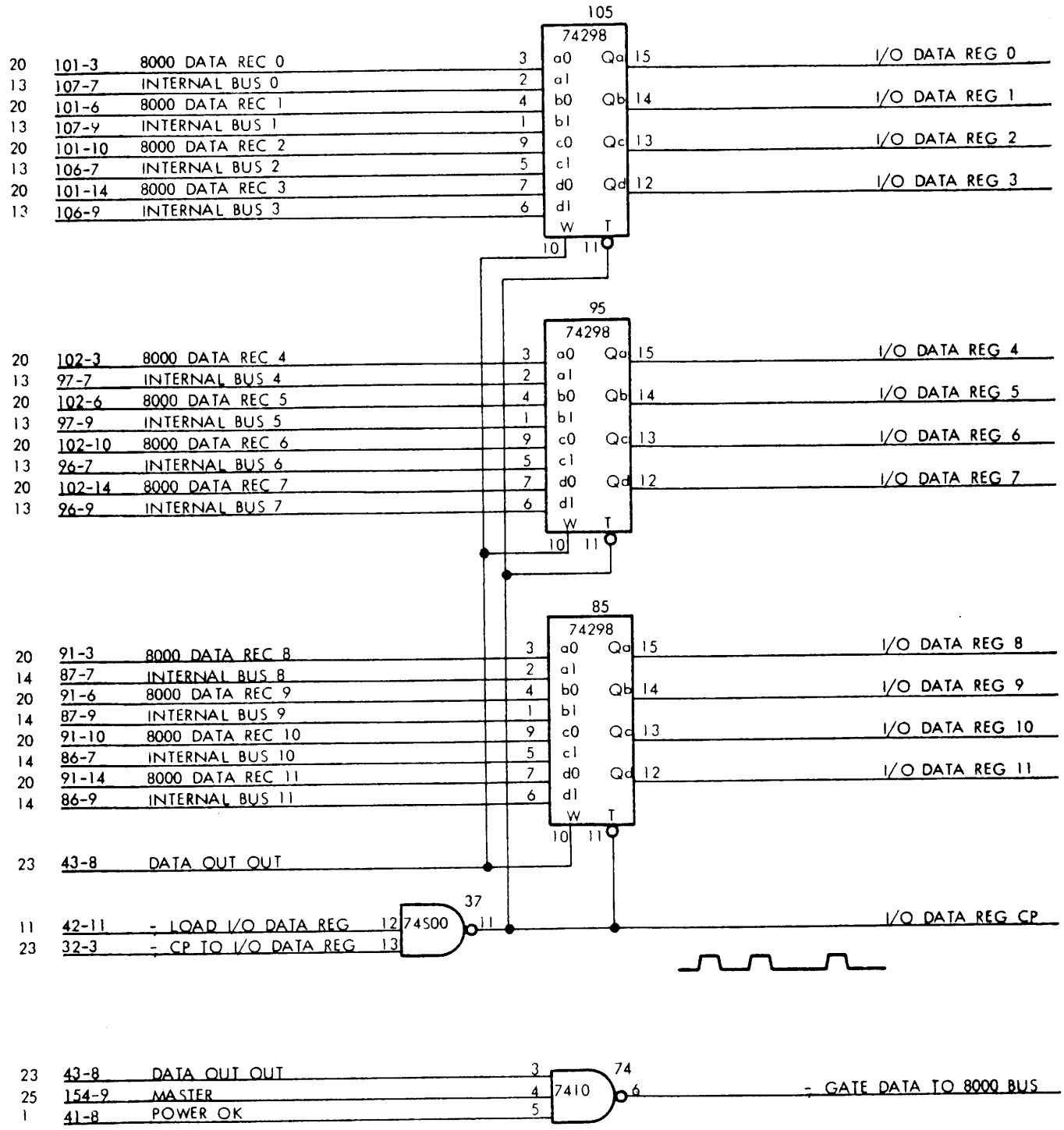
SIGNAL	DESTINATION	DESCRIPTION
ADDR. P. GEN	21	Data parity is checked/generated and address parity generated by means of 4 parity chekers/generators connected to the FPA 801 internal bus.
DATA P. GEN 0	19	
DATA P. GEN 1	19	
DATA P. GEN 2	19	
-,DATA P. GEN OK	5	Data parity involves 3 parity bits, which makes the parity of the 3 characters of the RC 8000 word odd:
DATA OUT IN	24	
8000 DATA P REC. 0	19	Data parity 0 valid for 0:7 Data parity 1 valid for 8:15
8000 DATA P REC. 1	19	Data parity 2 valid for 16:23
8000 DATA P REC. 2	19	The parity bit of the address is bit 23, which makes the parity of the address bits 0 : 23 odd. The data parity ok signal is connected to the condition selector to be used by the microprogram.

Unit		
FPA803	PARITY CHECKER & GENERATOR	
Dwg. No. A26057		17



82.09.01 VH 82.09.29 ABP

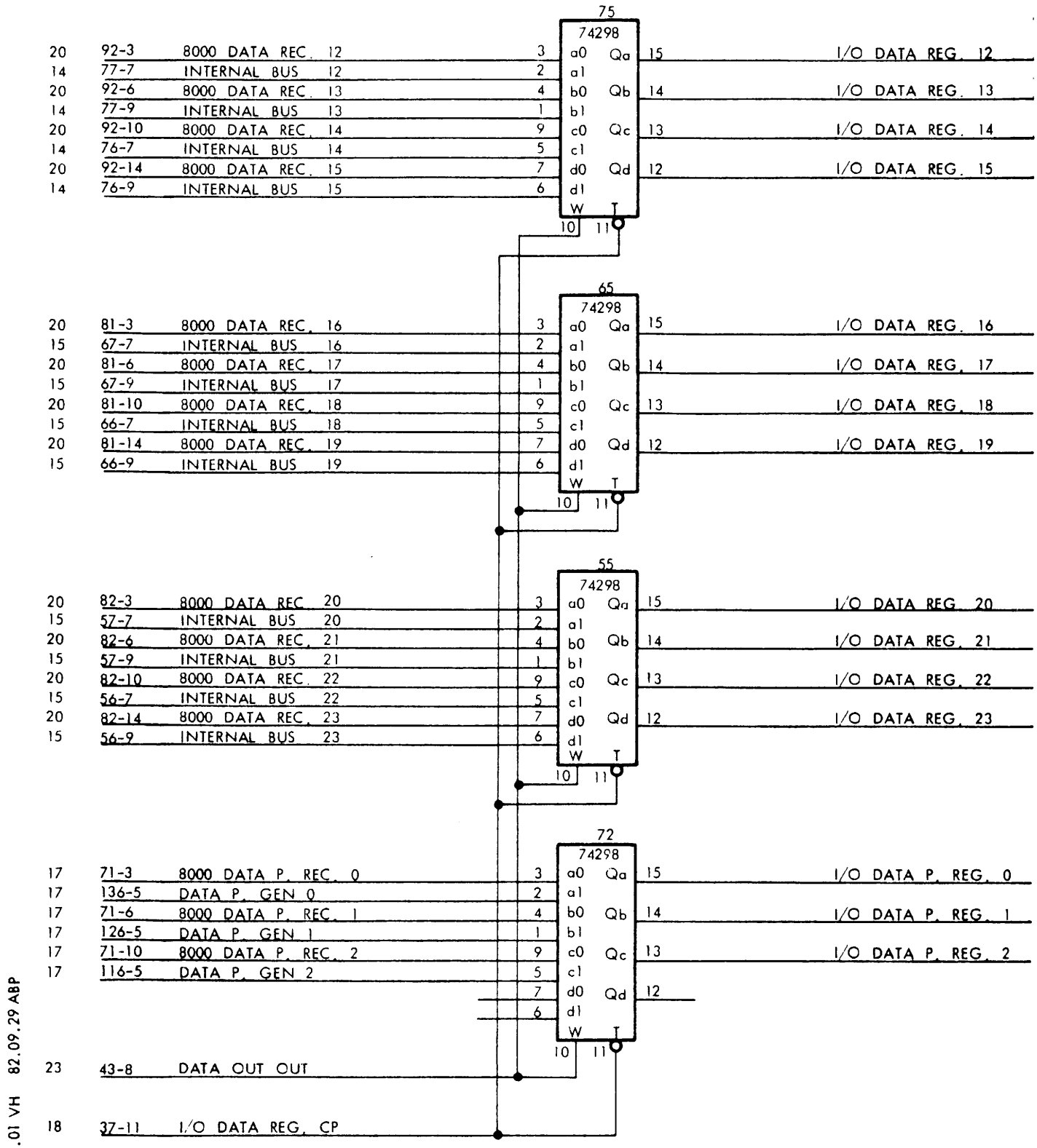
SIGNAL	DESTINATION	DESCRIPTION
I/O DATA REG 0 : 7	13,20	The FPA 801 input/output register has two input ports of which one is connected to the internal bus and one to the RC 8000 data receivers.
I/O DATA REG 8 : 11	14,20	
I/O DATA REG CP	19	The output of the I/O data register is connected to the RC 8000 data transmitters and to the FPA 801 data selector. All data transfer between FPA 801 and RC 8000 bus takes place via this register.
-,GATA DATA TO 8000 BUS	17 20	In case of data-out transfer the I/O data register and the I/O address register is loaded from the internal bus. Simultaneously with load of the I/O address register a bus cycle is requested. When FPA 801 becomes busmaster the I/O data register is gated to the RC 8000 data bus and the I/O address register to the RC 8000 address bus. In case of data-in transfer the I/O address register is loaded from the internal bus and a bus cycle is requested. When FPA 801 becomes bus master the I/O address register is gated to the RC 8000 data bus. When the addressed slave places data on the RC 8000 data bus the data bus lines is deskewed and the I/O data register is loaded with data from the data bus. In both cases a bus ready signal notyfies the microprogram when the bus transfer is complete.



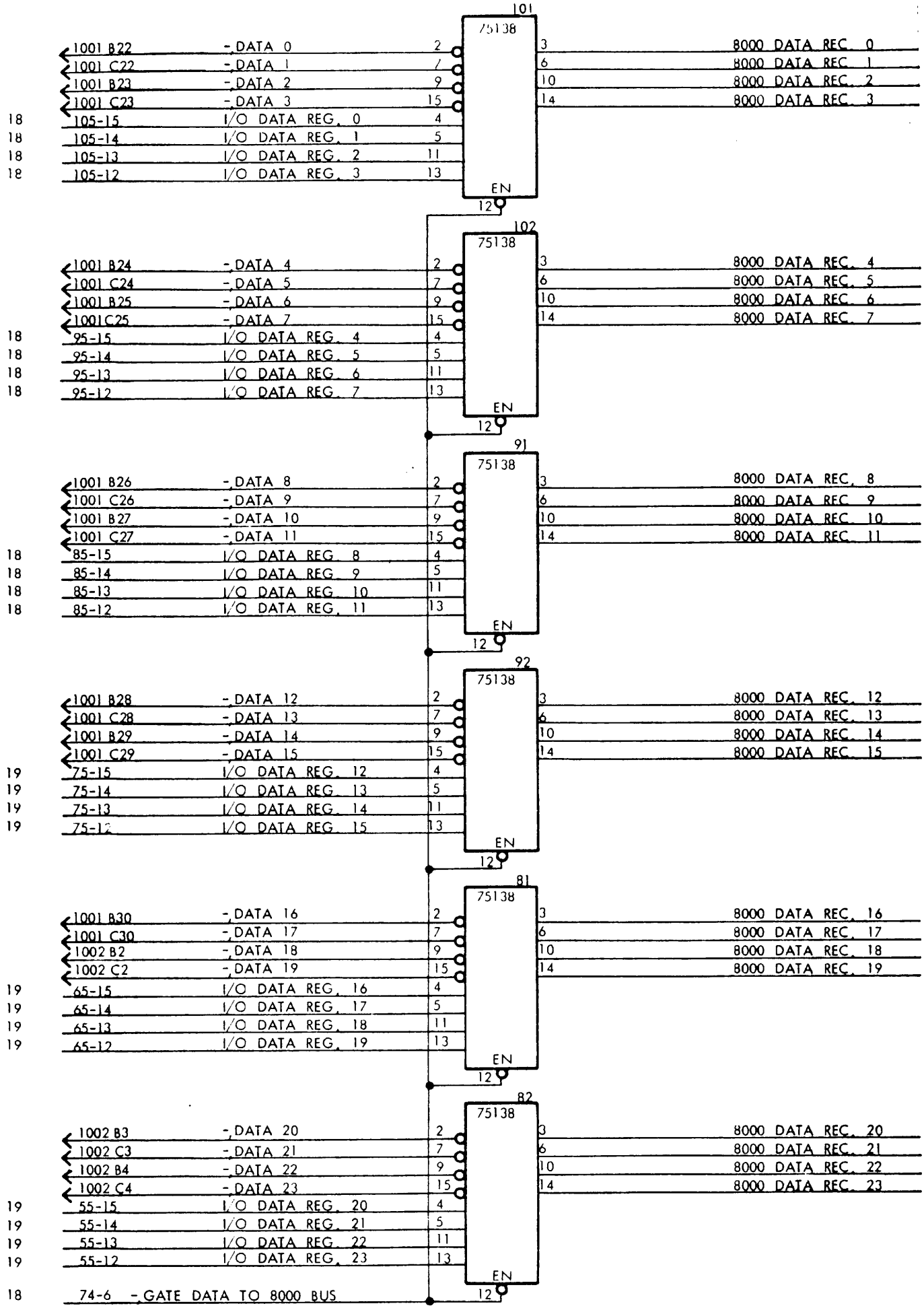
82.09.01 VH 82.09.29 ABP

SIGNAL	DESTINATION	DESCRIPTION
I/O DATA REG. 12 : 15	14,20	The I/O data parity register has two input ports. One port is connected to the RC 8000 data parity receivers and the other to the data parity generator. Output of the I/O data parity register is connected to the data parity checker and to the RC 8000 data parity transmitters (refer to diagram 17). The I/O data parity register serves as buffer for the parity bits received/generated from/to the RC 8000 bus.
I/O DATA REG. 16 : 23	15,20	
I/O DATA P. REG. 0 : 2	17	

Unit		
FPA 801	I/O DATA REGISTER 12 : 23 &	
Dwg. No.	I/O DATA P. REG. 0 : 2	19
A24730		

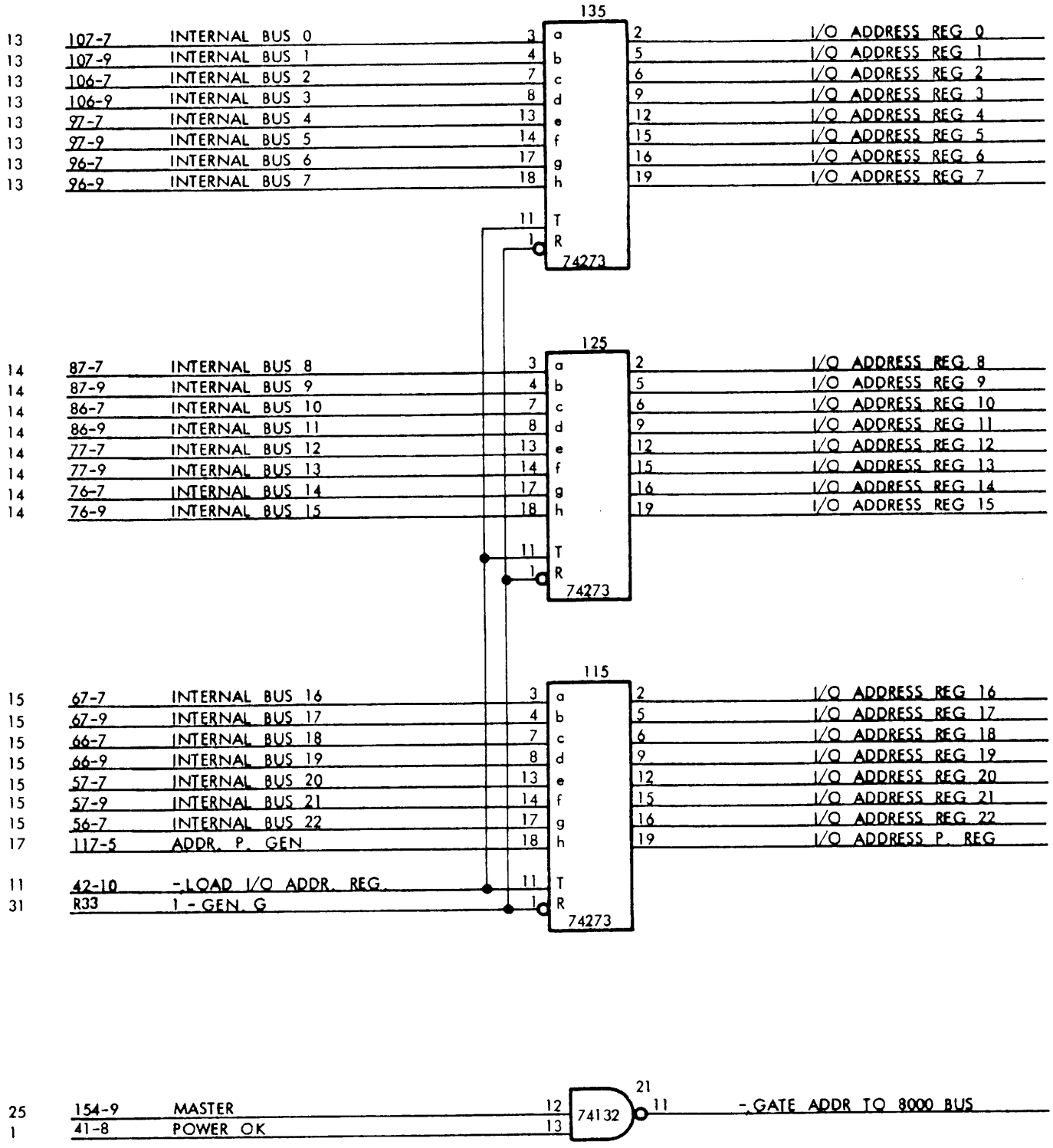

75
74298
20 92-3 8000 DATA REC. 12
14 77-7 INTERNAL BUS 12
20 92-6 8000 DATA REC. 13
14 77-9 INTERNAL BUS 13
20 92-10 8000 DATA REC. 14
14 76-7 INTERNAL BUS 14
20 92-14 8000 DATA REC. 15
14 76-9 INTERNAL BUS 15
3 a0 Qa 15 I/O DATA REG. 12
2 a1
4 b0 Qb 14 I/O DATA REG. 13
1 b1
9 c0 Qc 13 I/O DATA REG. 14
5 c1
7 d0 Qd 12 I/O DATA REG. 15
6 d1
W T
10 11
65
74298
20 81-3 8000 DATA REC. 16
15 67-7 INTERNAL BUS 16
20 81-6 8000 DATA REC. 17
15 67-9 INTERNAL BUS 17
20 81-10 8000 DATA REC. 18
15 66-7 INTERNAL BUS 18
20 81-14 8000 DATA REC. 19
15 66-9 INTERNAL BUS 19
3 a0 Qa 15 I/O DATA REG. 16
2 a1
4 b0 Qb 14 I/O DATA REG. 17
1 b1
9 c0 Qc 13 I/O DATA REG. 18
5 c1
7 d0 Qd 12 I/O DATA REG. 19
6 d1
W T
10 11
55
74298
20 82-3 8000 DATA REC. 20
15 57-7 INTERNAL BUS 20
20 82-6 8000 DATA REC. 21
15 57-9 INTERNAL BUS 21
20 82-10 8000 DATA REC. 22
15 56-7 INTERNAL BUS 22
20 82-14 8000 DATA REC. 23
15 56-9 INTERNAL BUS 23
3 a0 Qa 15 I/O DATA REG. 20
2 a1
4 b0 Qb 14 I/O DATA REG. 21
1 b1
9 c0 Qc 13 I/O DATA REG. 22
5 c1
7 d0 Qd 12 I/O DATA REG. 23
6 d1
W T
10 11
72
74298
17 71-3 8000 DATA P. REC. 0
17 136-5 DATA P. GEN 0
17 71-6 8000 DATA P. REC. 1
17 126-5 DATA P. GEN 1
17 71-10 8000 DATA P. REC. 2
17 116-5 DATA P. GEN 2
3 a0 Qa 15 I/O DATA P. REG. 0
2 a1
4 b0 Qb 14 I/O DATA P. REG. 1
1 b1
9 c0 Qc 13 I/O DATA P. REG. 2
5 c1
7 d0 Qd 12
6 d1
W T
10 11
23 43-8 DATA OUT OUT
18 37-11 I/O DATA REG. CP
82.09.01 VH 82.09.29 ABP

SIGNAL	DESTINATION	DESCRIPTION
8000 DATA REC 0 : 11 8000 DATA REC 12 : 23	18 19	The RC 8000 data bus is a bidirectional 24 bits wide bus. The bus is terminated with 2 x 120 E. 120E is placed in the BUS CONTROL UNIT and 120 E is placed near the last controller on the bus. The bus is driven by open collector circuits cape able of sinking ~ 60 mA. FPA 801 drives the bus by means of the SN 75138, which is a quad bus - transceiver.

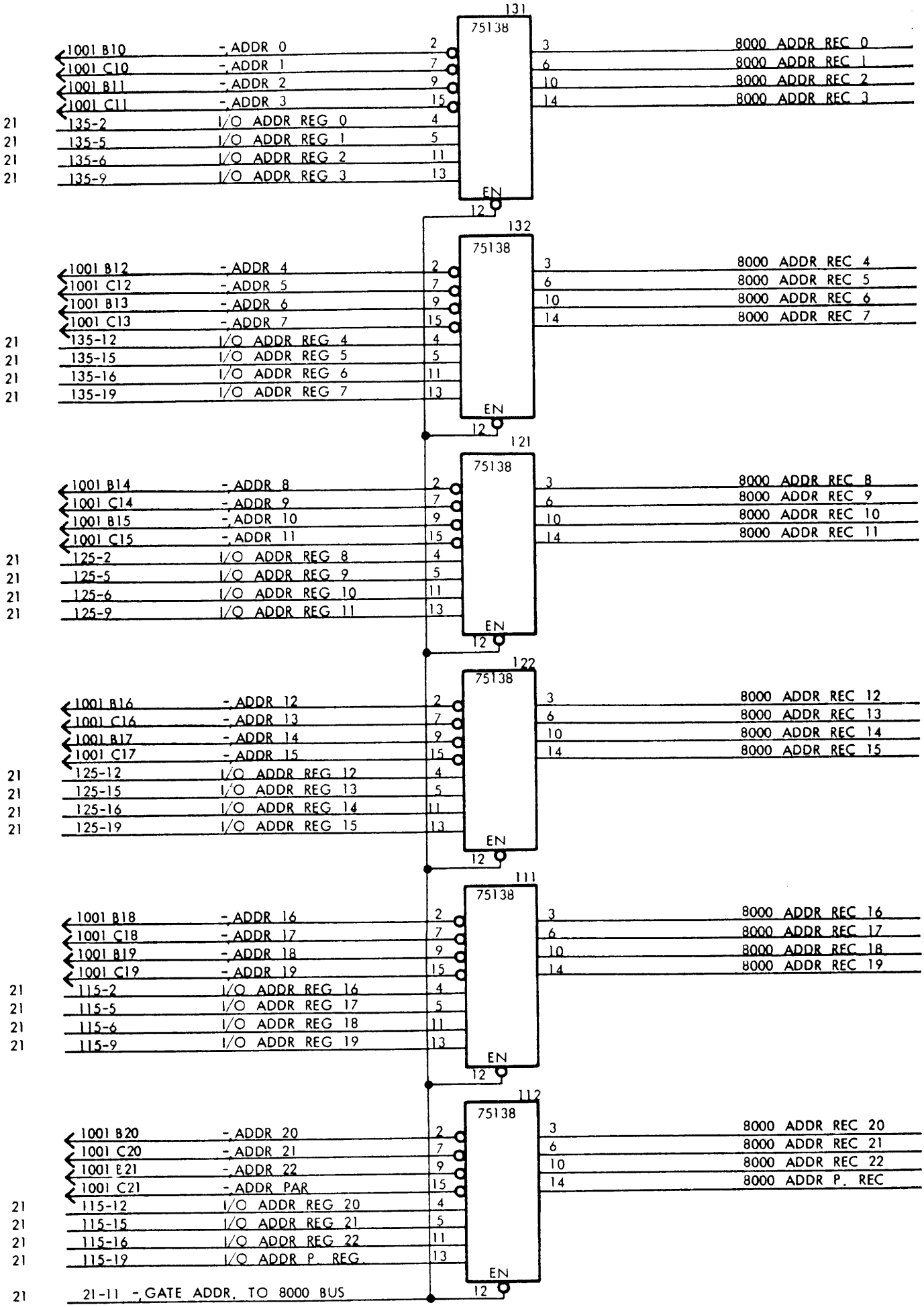


82.09.01 VH 82.09.29 ABP

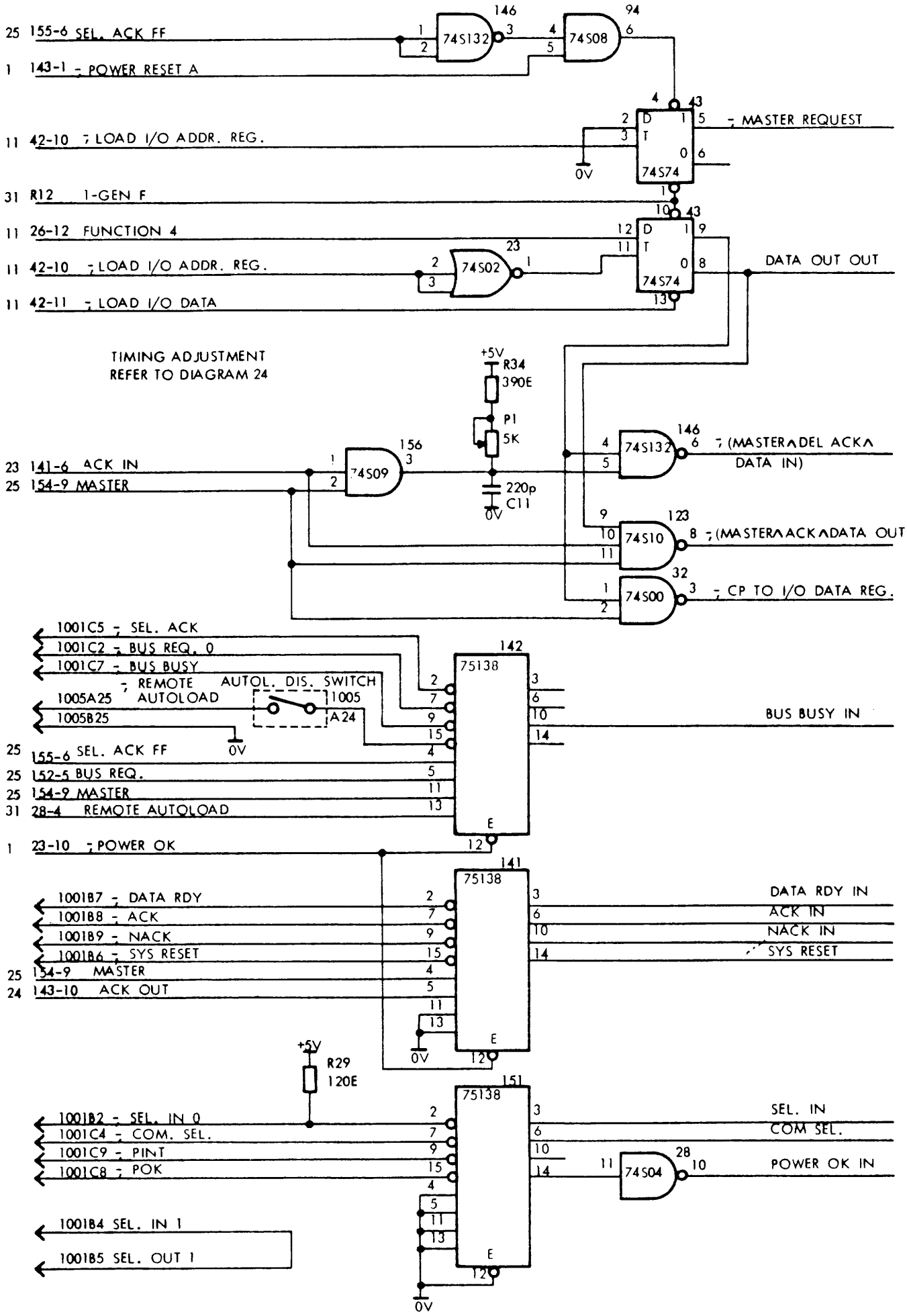
SIGNAL	DESTINATION	DESCRIPTION
I/O ADDRESS REG.	22	The FPA 801 I/O address register serves as buffer for the RC 8000 memory address during data transfers to and from FPA 801 and as buffer for the interrupt destination address during interrupt. A bus request procedure is always initiated simultaneously with the load of the I/O address register, and when FPA 801 becomes busmaster the I/O address register is gated to the RC 8000 bus via the address bus transceivers. The inputs of the I/O address register are connected to the FPA 801 internal bus.


135
13 107-7 INTERNAL BUS 0
13 107-9 INTERNAL BUS 1
13 106-7 INTERNAL BUS 2
13 106-9 INTERNAL BUS 3
13 97-7 INTERNAL BUS 4
13 97-9 INTERNAL BUS 5
13 96-7 INTERNAL BUS 6
13 96-9 INTERNAL BUS 7
3 a
4 b
7 c
8 d
13 e
14 f
17 g
18 h
11 T
1 R
74273
2 I/O ADDRESS REG 0
5 I/O ADDRESS REG 1
6 I/O ADDRESS REG 2
9 I/O ADDRESS REG 3
12 I/O ADDRESS REG 4
15 I/O ADDRESS REG 5
16 I/O ADDRESS REG 6
19 I/O ADDRESS REG 7
125
14 87-7 INTERNAL BUS 8
14 87-9 INTERNAL BUS 9
14 86-7 INTERNAL BUS 10
14 86-9 INTERNAL BUS 11
14 77-7 INTERNAL BUS 12
14 77-9 INTERNAL BUS 13
14 76-7 INTERNAL BUS 14
14 76-9 INTERNAL BUS 15
3 a
4 b
7 c
8 d
13 e
14 f
17 g
18 h
11 T
1 R
74273
2 I/O ADDRESS REG 8
5 I/O ADDRESS REG 9
6 I/O ADDRESS REG 10
9 I/O ADDRESS REG 11
12 I/O ADDRESS REG 12
15 I/O ADDRESS REG 13
16 I/O ADDRESS REG 14
19 I/O ADDRESS REG 15
115
15 67-7 INTERNAL BUS 16
15 67-9 INTERNAL BUS 17
15 66-7 INTERNAL BUS 18
15 66-9 INTERNAL BUS 19
15 57-7 INTERNAL BUS 20
15 57-9 INTERNAL BUS 21
15 56-7 INTERNAL BUS 22
17 117-5 ADDR. P. GEN
11 42-10 -LOAD I/O ADDR. REG.
31 R33 1 - GEN. G
3 a
4 b
7 c
8 d
13 e
14 f
17 g
18 h
11 T
1 R
74273
2 I/O ADDRESS REG 16
5 I/O ADDRESS REG 17
6 I/O ADDRESS REG 18
9 I/O ADDRESS REG 19
12 I/O ADDRESS REG 20
15 I/O ADDRESS REG 21
16 I/O ADDRESS REG 22
19 I/O ADDRESS P. REG
21
25 154-9 MASTER
1 41-8 POWER OK
12
13
74132
11 -GATE ADDR TO 8000 BUS
82,09,29 ABP
82,09,01 VH

SIGNAL	DESTINATION	DESCRIPTION
8000 ADDR. REC 0 - 22	16	The RC 8000 address bus is a bidirectional bus 23 bits wide (excl parity bit). The address bus is driven and terminated as the data bus (refer to diagram 20).
8000 ADDR. P. REC	16	


131
75138
1001 B10 -.ADDR 0
1001 C10 -.ADDR 1
1001 B11 -.ADDR 2
1001 C11 -.ADDR 3
21 135-2 I/O ADDR REG 0
21 135-5 I/O ADDR REG 1
21 135-6 I/O ADDR REG 2
21 135-9 I/O ADDR REG 3
2 7 9 15 4 5 11 13
EN
12
3 6 10 14
8000 ADDR REC 0
8000 ADDR REC 1
8000 ADDR REC 2
8000 ADDR REC 3
132
75138
1001 B12 -.ADDR 4
1001 C12 -.ADDR 5
1001 B13 -.ADDR 6
1001 C13 -.ADDR 7
21 135-12 I/O ADDR REG 4
21 135-15 I/O ADDR REG 5
21 135-16 I/O ADDR REG 6
21 135-19 I/O ADDR REG 7
2 7 9 15 4 5 11 13
EN
12
3 6 10 14
8000 ADDR REC 4
8000 ADDR REC 5
8000 ADDR REC 6
8000 ADDR REC 7
121
75138
1001 B14 -.ADDR 8
1001 C14 -.ADDR 9
1001 B15 -.ADDR 10
1001 C15 -.ADDR 11
21 125-2 I/O ADDR REG 8
21 125-5 I/O ADDR REG 9
21 125-6 I/O ADDR REG 10
21 125-9 I/O ADDR REG 11
2 7 9 15 4 5 11 13
EN
12
3 6 10 14
8000 ADDR REC 8
8000 ADDR REC 9
8000 ADDR REC 10
8000 ADDR REC 11
122
75138
1001 B16 -.ADDR 12
1001 C16 -.ADDR 13
1001 B17 -.ADDR 14
1001 C17 -.ADDR 15
21 125-12 I/O ADDR REG 12
21 125-15 I/O ADDR REG 13
21 125-16 I/O ADDR REG 14
21 125-19 I/O ADDR REG 15
2 7 9 15 4 5 11 13
EN
12
3 6 10 14
8000 ADDR REC 12
8000 ADDR REC 13
8000 ADDR REC 14
8000 ADDR REC 15
111
75138
1001 B18 -.ADDR 16
1001 C18 -.ADDR 17
1001 B19 -.ADDR 18
1001 C19 -.ADDR 19
21 115-2 I/O ADDR REG 16
21 115-5 I/O ADDR REG 17
21 115-6 I/O ADDR REG 18
21 115-9 I/O ADDR REG 19
2 7 9 15 4 5 11 13
EN
12
3 6 10 14
8000 ADDR REC 16
8000 ADDR REC 17
8000 ADDR REC 18
8000 ADDR REC 19
112
75138
1001 B20 -.ADDR 20
1001 C20 -.ADDR 21
1001 E21 -.ADDR 22
1001 C21 -.ADDR PAR
21 115-12 I/O ADDR REG 20
21 115-15 I/O ADDR REG 21
21 115-16 I/O ADDR REG 22
21 115-19 I/O ADDR P. REG.
2 7 9 15 4 5 11 13
EN
12
3 6 10 14
8000 ADDR REC 20
8000 ADDR REC 21
8000 ADDR REC 22
8000 ADDR P. REC
21 21-11 -.GATE ADDR. TO 8000 BUS
82.09.29 ABP
82.09.01 VHL

SIGNAL	DESTINATION	DESCRIPTION
ACK IN	25	The acknowledge in signal is a respond to the data ready signal. Ack in indicates: 1. Data in transfers: The slave has recognized the address and has placed data on the data lines. 2. Data out transfer: The slave has recognized the address and received data correctly.
BUS BUSY IN	25	Indicates to FPA 801 that the bus is being used by another busmaster.
COM SEL	25	The common select signal is lead to all controllers in parallel.
-,CP to I/O DATA REG	18	This signal loads I/O data register during data in transfers (refer to diagram 18).
DATA OUT OUT	17 18 19	This FF is set to logical 1 during data-out transfers and to logical 0 during data-in transfer. The FF controls the Data out transmitter to the 8000 bus and selects the proper data path to the I/O data register.
DATA RDY IN	24	The "and" of data ready in ="1" and master ="0" is delayed 150 nS and then "anded" with data out in = 1 and selected = 1 to form the load device function signal and the acknowledge out signal. The 150 nS compensation delay compensates for: a. skew in the BUS MASTER b. Transceiver skew c. Cable skew d. Address decoding in FPA 801
-,(MASTER ∧ ACK ∧ DATA OUT)	24	This signal generates the bus ready signal during data out transfers (refer to diagram 24)
-,(MASTER ∧ DEL ACK ∧ DATA IN)	24	This signal generates the bus ready signal during data in transfers. The acknowledge signal received from the slave is delayed 120 nS This delay compensates for: a. Skew in the SLAVE b. Transceiver skew c. Cable skew
-,MASTER REQUEST	25	This FF is set to logical 1 when FPA 801 requires access to the RC 8000 bus.
NACK IN	24 25	The not acknowledge signal from the slave causes set of the bus communication error signal.
POWER OK IN	1	This signal originates in the power supply of the CHS 802 chassis. After a delay this signal is used to generate the FPA 801 signal power ok, which is used to initializ the logic.
SEL. IN	25	The select signal is daisy chained through all controllers connected to the RC 8000 bus. If FPA 801 receives the select in signal after having requested bus access, the select out signal to the next controller is inhibited and the select acknowledge signal generated.
SYS RESET	1	

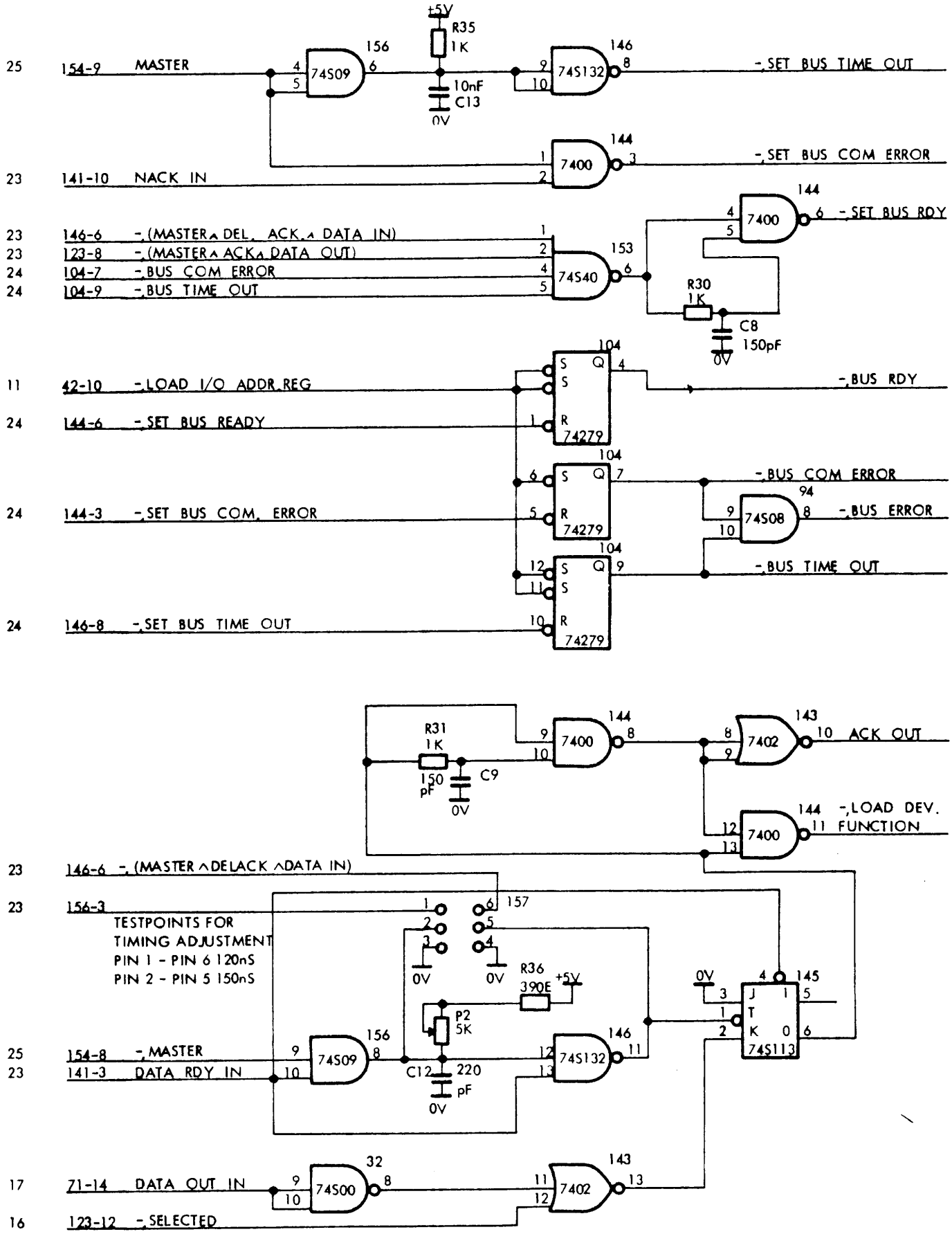


82.09.01 VH 82.09.29 ABP Rev. 83.03.03 ABP

FPA803 DATA TRANSFER LOGIC

A14274 Circuit diagram

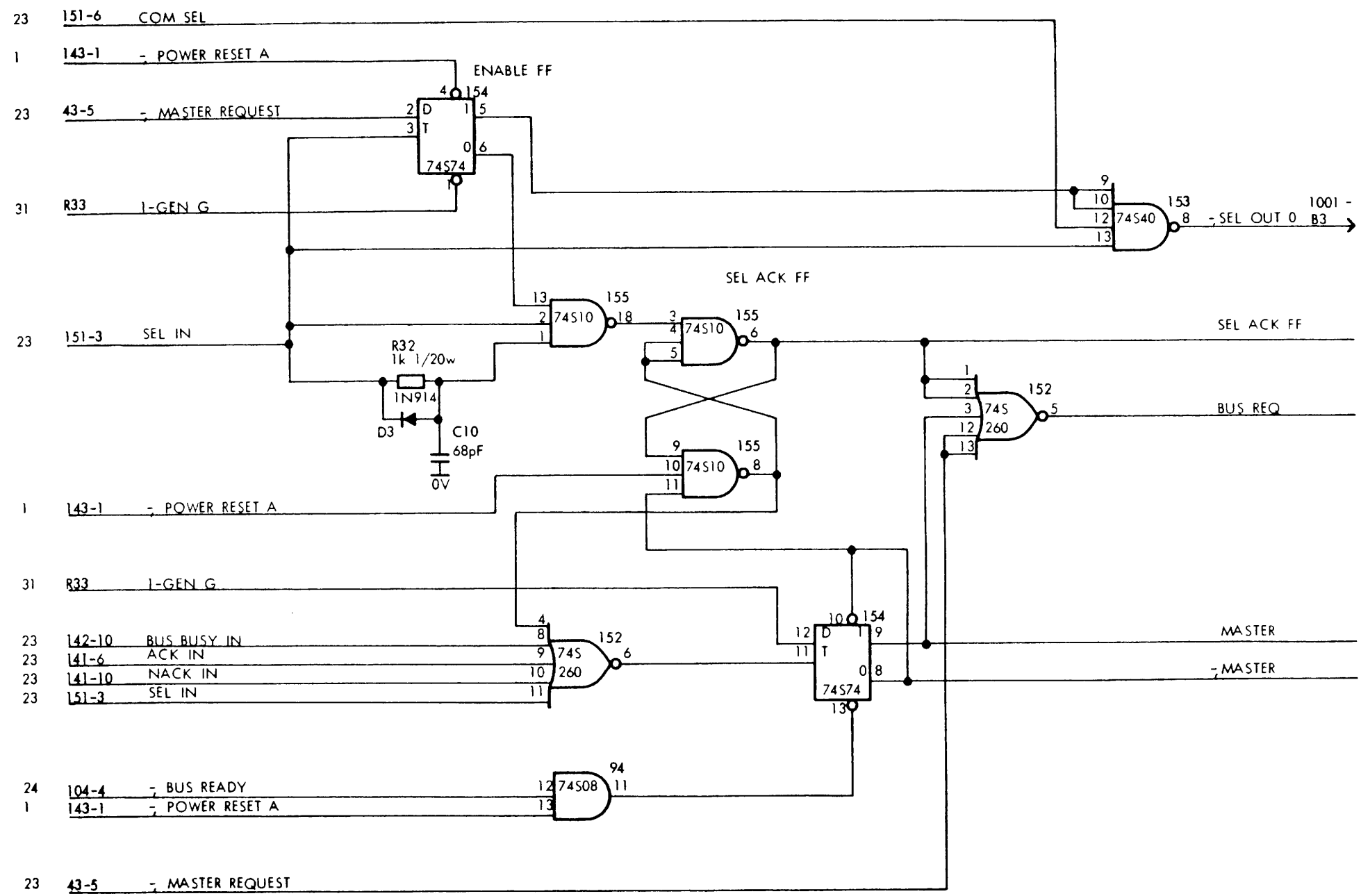
SIGNAL	DESTINATION	DESCRIPTION
ACK OUT	23	The upper part of this diagram shows the bus status circuits.
-,BUS COM ERROR	This diag.	The bus ready FF is cleared when FPA 801 requires access to the RC 8000 bus. The
-,BUS ERROR	5	FF is set to logical 1 when FPA 801 be-
-,BUS RDY	5 25	comes bus master and the slave has responded to the data ready signal by returning ack or nack. The bus ready FF
-,BUS TIME OUT	This diag. 5	is also set to logical 1 in case of bus time out i.e. no respond from the slave at all, however, in this case the bus
-,SET BUS COM. ERROR	This diag.	time out FF is set to logical 1 too. If the slave returns a nack signal the the
-,SET BUS RDY.	This diag.	bus communication error FF is set. The or result of bus time out, bus communication
-,SET BUS TIME OUT	This diag.	error forms the bus error signal, which together with the bus ready and bus time
-,LOAD DEV. FUNCTION	2	out signals is wired to the condition selector to be used by the microprogram. The lower part of the diagram shows the FPA. 801 acknowledge circuits, which are used when FPA 801 is slave. The load device function signal loads the device function register thus starting a reset function or a new channel program. The ack out signal controls the ack- nowledge transmitter.



82.09.01 VH 82.09.29 ABP Rev. 83.03.03 ABP

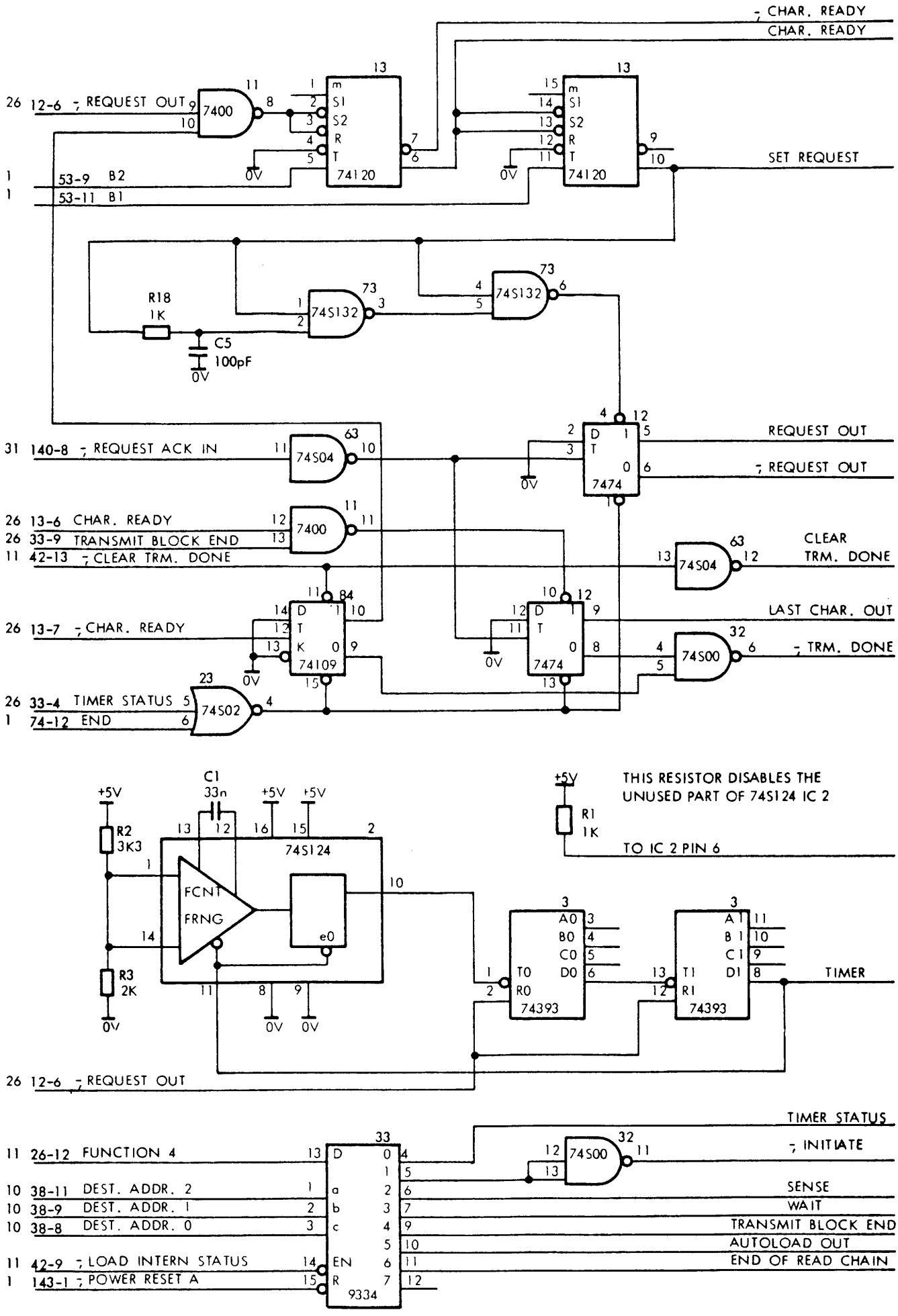
SIGNAL	DESTINATION	DESCRIPTION
BUS REQ	23	The logic on this diagram generates the signals necessary in connection with the bus master selection procedure, which is initiated when FPA 801 sets the master request FF to logical 1. The master request FF causes a bus request signal to be send to the bus control unit (BCU). The BCU responds to the bus request by generating the comman select and select in signals, provided another selection phase is not in progress (SACK line = "1"). The select signal is daisy chained through all controllers connected to the bus. A controller, which has not requested bus control, passes the signal to the next controller, FPA 801 does this by means of the enable FF. A controller which has requested bus control breaks the chain as set the select acknowledge signal to logical 1. The common select signal is connected to all controllers in parrallel. The select signals are cleared simultaneously. By connecting the common select signal to all controllers in parallel the termination of the bus request procedure is made as fast as possible, since the trailling edge of the select signal do not need to ripple through the units.
MASTER	18 21 23	
	24	
	This diag.	
-,MASTER	24 This diag.	
SEL ACK FF	23	
	This diag.	
-,SEL OUT 0	Plug 1001-B3	

Unit		
FPA803	BUS MASTER SELECTION LOGIC	
Dwg. No. A26060		25


23 151-6 COM SEL
1 143-1 -; POWER RESET A
ENABLE FF
23 43-5 -; MASTER REQUEST
74S74
31 R33 1-GEN G
74S40
153
1001 - B3
-; SEL OUT 0
SEL ACK FF
23 151-3 SEL IN
74S10
155
R32 1k 1/20w
1N914
D3
C10 68pF
0V
SEL ACK FF
BUS REQ
152
74S 260
1 143-1 -; POWER RESET A
31 R33 1-GEN G
23 142-10 BUS BUSY IN
23 141-6 ACK IN
23 141-10 NACK IN
23 151-3 SEL IN
MASTER
-; MASTER
24 104-4 -; BUS READY
1 143-1 -; POWER RESET A
74S08
94
23 43-5 -; MASTER REQUEST

SIGNAL	DESTINATION	DESCRIPTION
AUTOLOAD OUT	30	When FPA 802 wants to transmit a character the signal clear transmitter done is generated by the microprogram. This signal loads the transmitter character buffer and starts the transmitter control circuits, which, if the previous request has been acknowledged by the opposite controller, causes the character to be placed on the data lines out, and the request FF to be set. When the character has been placed on the data out lines, i.e. transferred from the transmitter char. buffer to the transmitter char. register, the transmitter done FF is set to logical one. The done signal is led to the condition selector and via the microprogram the next character is fetched and the transmitter char. buffer loaded again. When the opposite controller has recognized the request signal and stored the character, it responds to the request by raising the request acknowledge signal, which clears the FPA 802 request FF. To identify the last character, this character is accompanied by the last character signal. Included in the transmitter circuits is timer, which is started simultaneously with set of the request FF. This timer causes via the microprogram the time out status to be set, if the opposite controller does not respond to the request signal. The lower part of diagram 26 shows some 1 bits register of which 6 are used as internal status signals, which are connected to the condition selector. The microprogram senses these status bits in order to jump through the program correctly. The last register is used for the autoload signal which is app. 1,2 uS wide.
-,CHAR. RDY	This diag. 27	
CLEAR TRM DONE	This diag. 27	
END OF READ CHAIN	5 28	
-,INITIATE	5	
LAST CHAR. OUT	30	
REQUEST OUT	30	
-,REQUEST OUT	This diag.	
SENSE	5	
TIMER	This diag. 5	
TIMER STATUS	This diag. 5	
-,TRM DONE	5	
TRANSMIT BLOCK END	This diag. 5	
WAIT	5	
SET REQUEST	12	

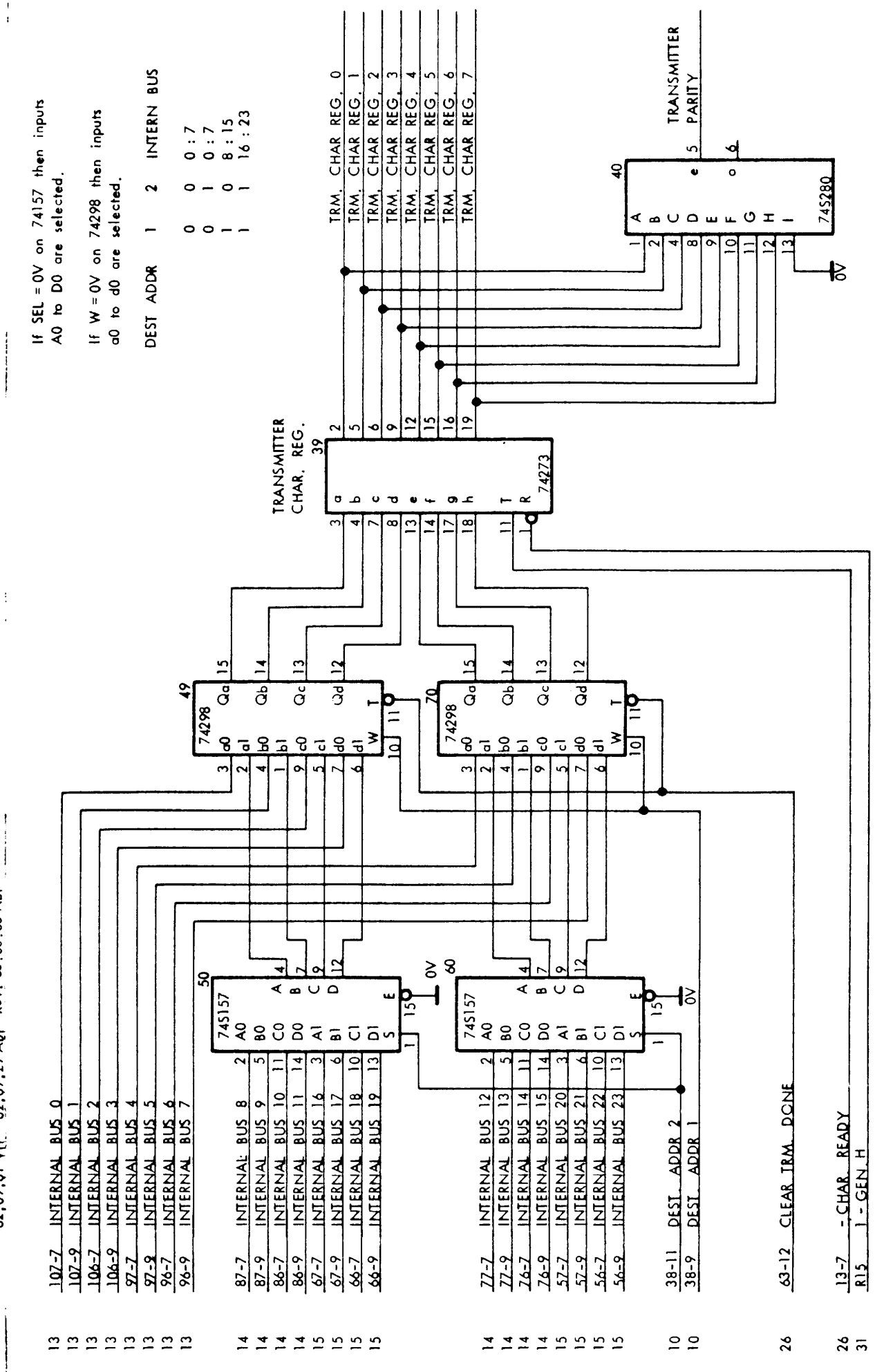
Unit FPA803	TRANSMITTER CONTROL & TIMER -	
Dwg No. A14277	TRM/REC INTERNAL STATUS	26



82.09.01 VH 82.09.29 ABP

SIGNAL	DESTINATION	DESCRIPTION
TRM CHAR REG 0-7	This diag. 29	The transmitter char. buffer and the transmitter char register are two 8-bits registers capeable of storing two characters. The transmitter char. buffer has 3 input ports, which makes it possible to load the register from: 1. Internal bus bits 0-7 or 2. Internal bus bits 8-15 or 3. Internal bus bits 16-23. The transmitter char. register drives the data transmitters to the opposite controller and the parity generator (Refer also to transmitter control circuits diagram 26).
TRANSMITTER PARITY	29	

Unit		
FPA803	TRANSMITTER CHAR. BUFFER & REGISTER	
Dwg. No. A26061		27



82,09,01 VH 82,09,29 ABP Rev. 83.03.03 ABP

FPA803 TRANSMITTER CHAR BUFFER & REGISTER 27

A14279 Circuit Diagram

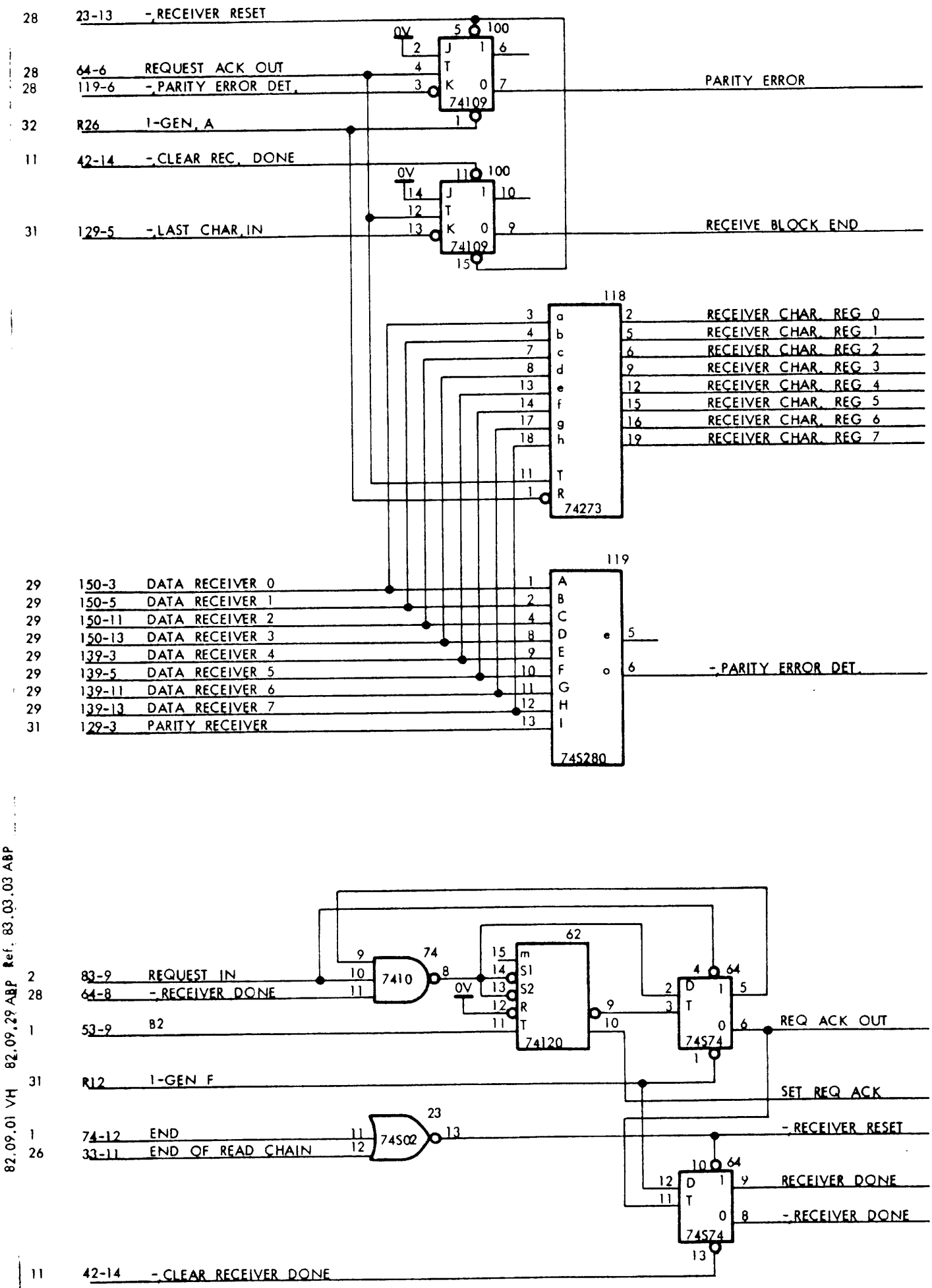
SIGNAL	DESTINATION	DESCRIPTION
PARITY ERROR	5	When FPA 802 enters the receive mode, the microprogram generates the signal clear receiver done, which clears the receive block end FF and the receiver done FF. Upon the reception of a request in signal from the opposite controller the request acknowledged FF is set, the receiver done FF set and the receiver char register loaded with the character from the data input lines. The receiver done signal notifies the microprogram that a character is ready in the receiver char. register. The microprogram stores the character in the RALU and clears the receiver done FF, thus enabling the reception of another character. The last character received must be accompanied by the last char in signal which causes the receive block end FF to be set. The receive block end signal is wired to the condition selector and in this way the microprogram detects the end of the block. The parity error FF is set if the parity of the received character is even, however, the parity error FF is not sensed by the microprogram until receive block end. When 3 chars. have been stored in the RALU, an RC 8000 bus cycle is requested, and 3 characters transferred to RC 8000 memory.
-, PARITY ERROR DET	This diag.	
RECEIVE BLOCK END	5	
RECEIVER CHAR	13, 14, 15	
RECEIVER DONE	5	
-, RECEIVER DONE	This diag.	
-, RECEIVER RESET	This diag.	
REQ ACK OUT	This diag. 30	
SET REQ ACK	12	

Designed by

Drawn by

Dwg. Office Check

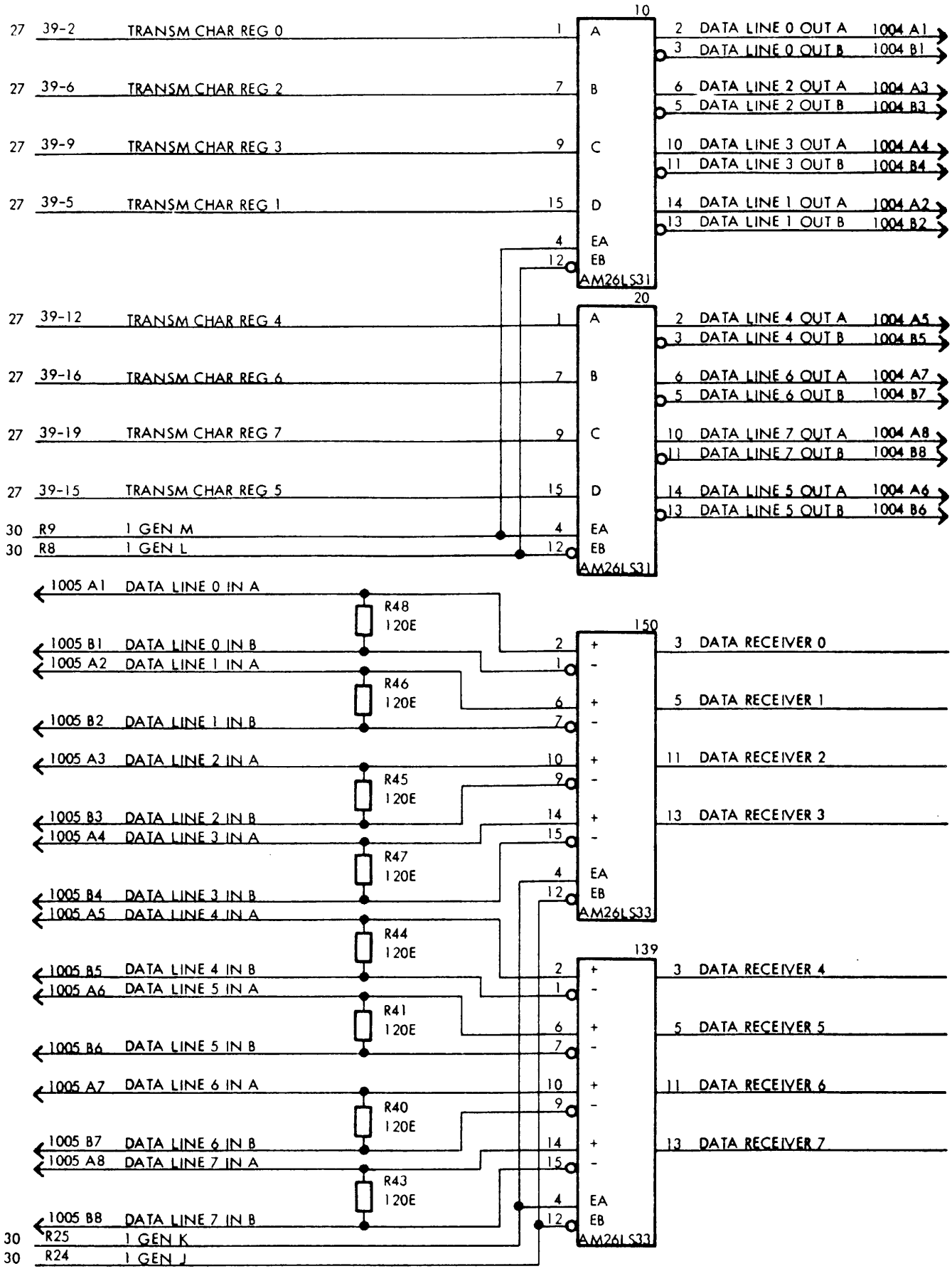
Unit		
FPA803	RECEIVER CONTROL & RECEIVER CHAR. REGISTER	
Dwg. No. A26062		28



82.09.01 VH 82.09.29 ABP Ref. 83.03.03 ABP

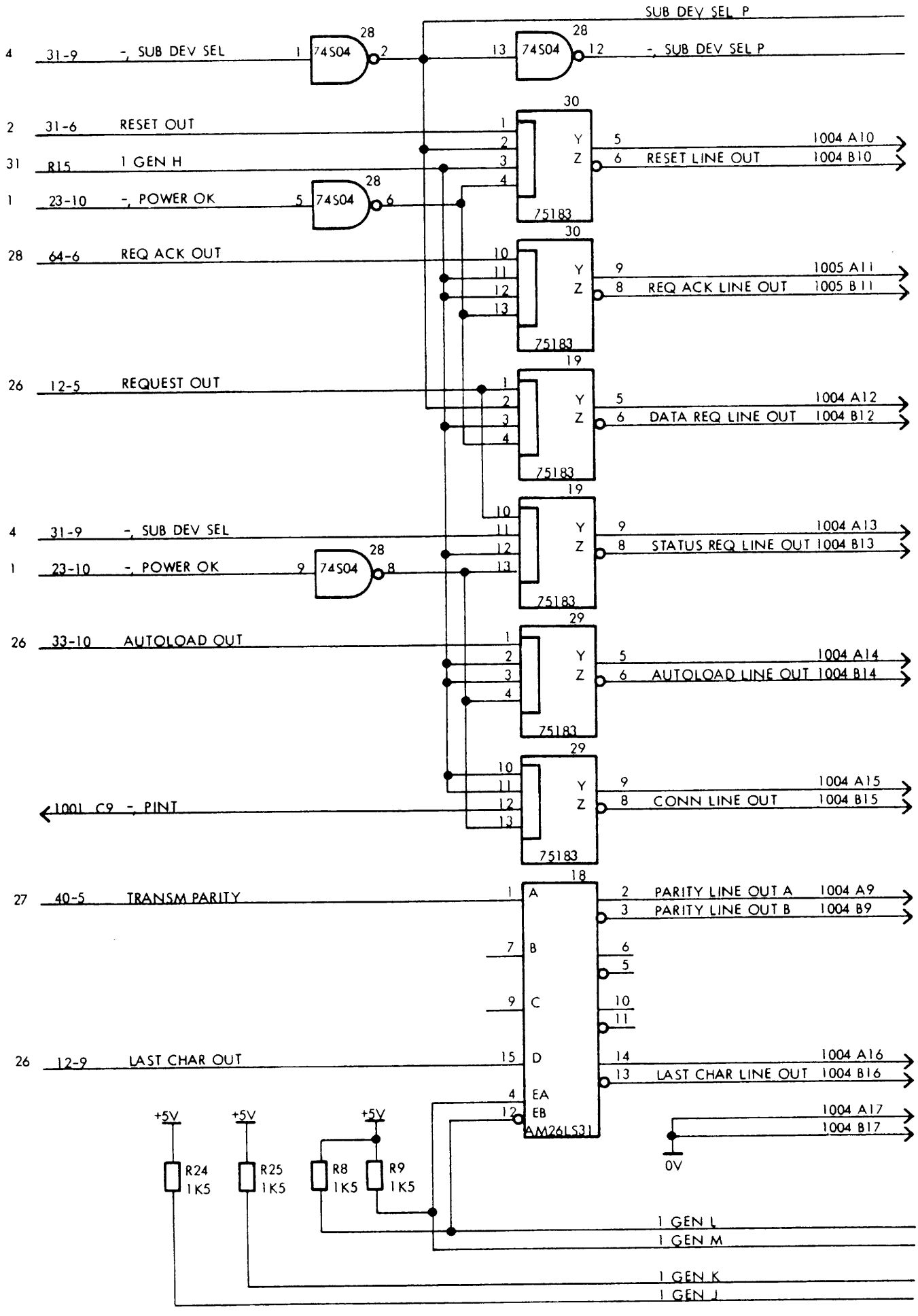
SIGNAL	DESTINATION	DESCRIPTION
DATA LINE OUT A & B 0 - 7	PLUG 1004	The line drivers used in FPA 801 povides ditterential output signals, and are used to drive a twisted pair line with an impedance of app. 120 E. The drivers are single supplied and uses only +5V.
DATA RECEIVER 0 - 7	28	The line receivers used are designed to sense small differential signals in the presence of large common - mode noise; up to ± 7V common mode input voltage can be tolerated. The receivers are single supplied and uses only +5V. Bit 0 of the data lines is alway the most significant bit.

Unit		
FPA803	DATA LINES TO AND FROM FRONT END PROCESSOR	
Dwg. No. A26063		29



82.09.01 VH 82.09.06 ABP

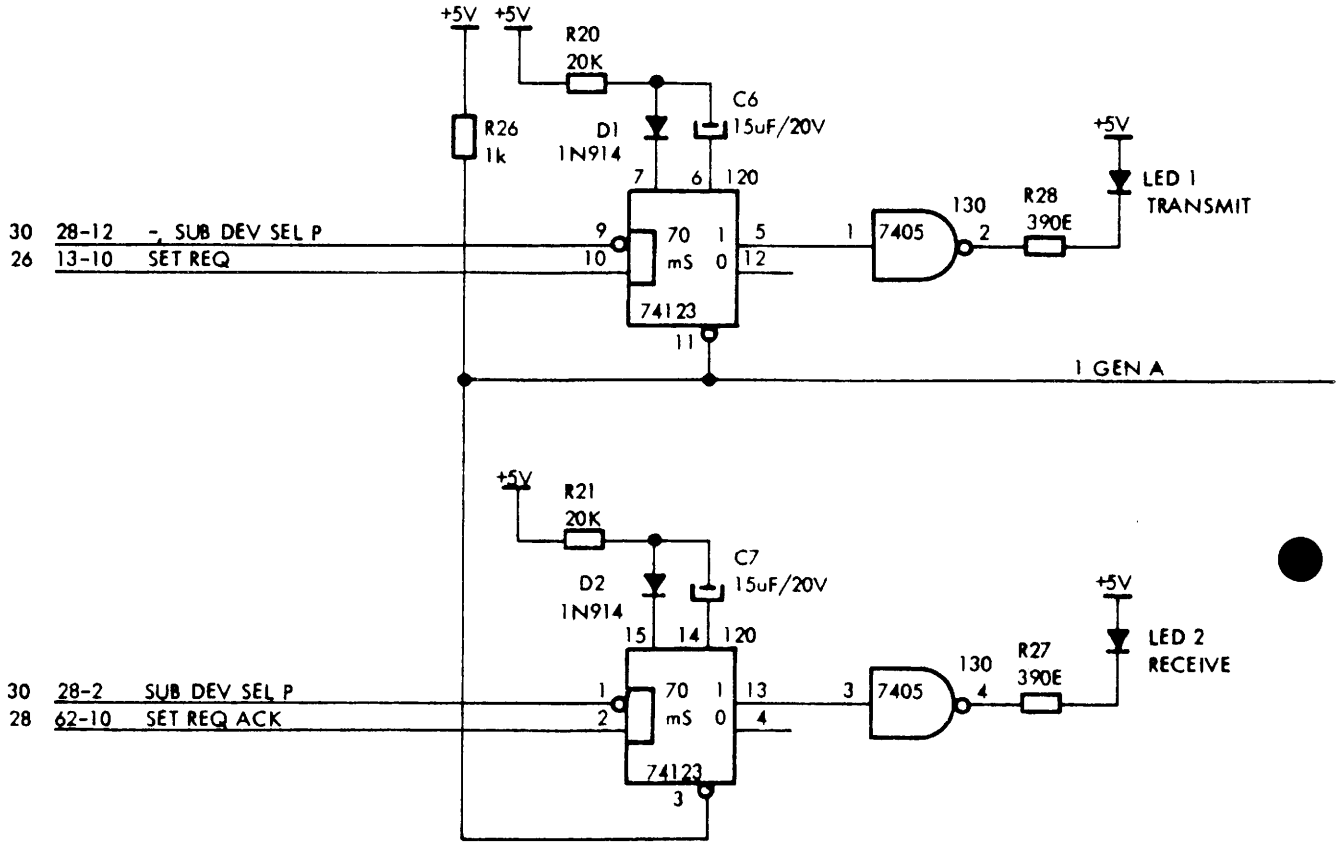
SIGNAL	DESTINATION	DESCRIPTION
RESET LINE OUT	PLUG 1004	This line when logical 1 indicates to the receiver in the opposite controller that the FPA 802 transmitter has been reset.
REQ ACK LINE OUT	PLUG 1005	When this signal changes from false to true state, it indicates to the transmitting unit that the character on the data lines has been stored in the receiving unit. Upon the reception of the rising edge of the acknowledge signal the transmitting unit is allowed to fetch the next character and place it on the data lines.
DATA REQ LINE OUT	PLUG 1004	This signal when logical 1 indicates to the receiving unit that a data character is ready on the data lines 0 : 7. The signal is generated by the transmitter in the transmitting unit.
STATUS REQ LINE OUT	PLUG 1004	This signal when logical 1 indicates to the receiving unit that a status character is ready on the data lines 0 : 7. The signal is generated by the receiver in the transmitting unit.
AUTOLOAD LINE OUT	PLUG 1004	This line is necessary to be able to initiate an auto-load procedure in the front-end computer under RC 8000 program control. Likewise, the front-end computer may use the line to initiate an autoload procedure in RC 8000 (Autoload Line in).
CONNECTED LINE OUT	PLUG 1004	This line when logical 1 indicates to the receiving unit that power is on. The connected signal enables following signals in the receiving unit: RESET IN REQUEST ACK IN DATA REQUEST IN STATUS REQUEST IN REMOTE AUTO LOAD
LAST CHAR LINE OUT	PLUG 1004	When logical 1 this line indicates the end of the block. The last char. signal is generated simultaneously with the emission of the last character in the block.
SUB DEV SEL P	12, 32	
-, SUB DEV SEL P	12	
PARITY LINE OUT	PLUG 1004	The parity line makes the parity odd.

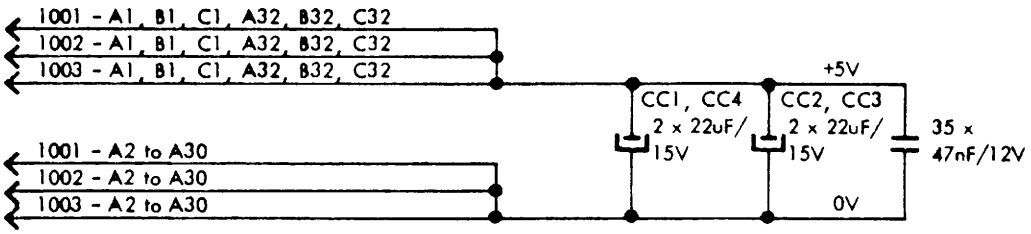


82.09.01 VH 82.09.06 ABP Rev 83.03.03 ABP

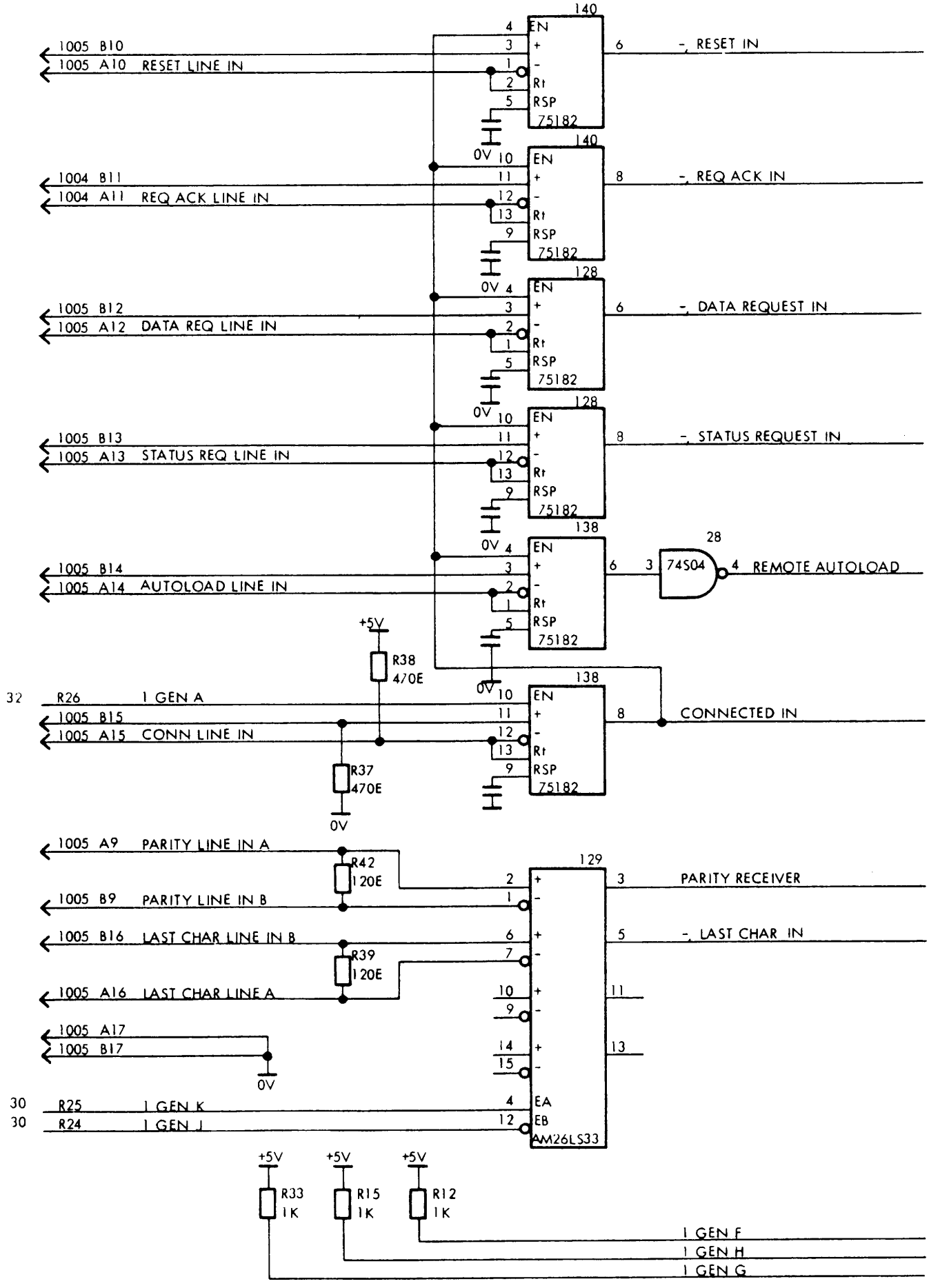
SIGNAL	DESTINATION	DESCRIPTION
-, RESET IN	2	Concerning the description of control signals received from front - end processor refer to the description of the control signals to front - end processor diagram 30.
-, REQ ACK IN	26	
-, DATA REQUEST IN	2	
-, STATUS REQUEST IN	2	
REMOTE AUTOLOAD	23	
CONNECTED IN	31	
	12	
-, LAST CHAR IN	28	
PARITY RECEIVER	28	

Unit		
FPA803	CONTROL LINES FROM FRONT END PROCESSOR	
Dwg. No. A26064		31





82.09.01 VH 82.09.06 ABP Rev. 83.03.03 ABP



82.09.01 VH 82.09.06 ABP Rev. 83.03.03 ABP

800218 VH 800716 JOM

INSTRUCTION

PIN. NO.	PROM 893								PROM 894								PROM 563			
	6	7	8	9	11	12	13	14	6	7	8	9	11	12	13	14	12	11	10	9
	REG. ALU FUNCTION								DEST.				A SEL.				SOURCE ADDR.			
	18	17	16	15	14	13	12	11	10	Ci	0	1	2	1	2	3	E	1	2	3

"0" ~ SELECT REG. ALU
"1" ~ SELECT EXTERN SOURCE

CONDITION SELECT AND NEXT ADDRESS

PIN. NO.	PROM 561				PROM 560				PROM 559				PROM 558			
	12	11	10	9	12	11	10	9	12	11	10	9	12	11	10	9
	CON. SEL. 0				CON. SEL. 1				NEXT ADDRESS							
	0	1	2	3	0	1	2	3	0	1	2	3	4	5	6	7

NEXT CONDITION 1
NEXT CONDITION 0

FUNCTIONS

PIN. NO.	PROM 557				PROM 556			
	12	11	10	9	12	11	10	9
	D	F1	F2	F3	F4	F5	F6	F7

FUNCTIONS F1 : F7
> CHANGE DEVICE

CONSTANTS

PIN. NO.	PROM 555				PROM 554			
	12	11	10	9	12	11	10	9
	0	1	2	3	20	21	22	23

CONSTANT 2^{0}
CONSTANT 2^{1}
CONSTANT 2^{2}
CONSTANT 2^{3}
CONSTANT 2^{19}
CONSTANT 2^{21}
CONSTANT 2^{22}
CONSTANT 2^{23}

800218 VH 800716 JOM

2901A SOURCE

E	A SEL. 1 2 3	2901A SOURCE REGISTER
0	0 0 0	DESCRIPTION ADDRESS
0	0 0 1	CHANNEL PROGRAM ADDRESS
0	0 1 0	FIRST WORD ADDRESS
0	0 1 1	CHARACTER COUNTER
0	1 0 0	BUFFER
0	1 0 1	REMAINING CHAR. COUNT
0	1 1 0	EVENT STATUS
0	1 1 1	COMMAND REGISTER

EXTERNAL SOURCE

E	ADDR. 0 1 2	EXTERN SOURCE REGISTER
1	0 0 0	I/O DATA REGISTER
1	0 0 1	CONSTANT PROM
1	0 1 0	DEVICE NUMBER
1	0 1 1	RECEIVER CHAR. REGISTER
1	1 0 0	
1	1 0 1	EXTERNAL CONSTANTS
1	1 1 0	
1	1 1 1	

FUNCTIONS F5-F6-F7

5 6 7	FUNCTION
0 0 0	⁻ CLEAR EVENT
0 0 1	⁻ CLEAR RECEIVER DONE
0 1 0	⁻ CLEAR TRANSM. DONE
0 1 1	⁻ END OF PROGRAM
1 0 0	⁻ LOAD I/O DATA REG.
1 0 1	⁻ LOAD I/O ADDRESS REG.
1 1 0	⁻ LOAD INTERN STATUS
1 1 1	UNUSEABLE

2901A DESTINATION

ADDR. 0 1 2	F=FUNCTIONS 1 2 3	4 5 6 7	2901A DESTINATION REG.	COMMENTS
0 0 0	SEE COM-MENTS	DON'T CARE	DESCRIPTION ADDRESS	F1, 2 & 3 controls the write pulse to 2901 (REG. ALU CP) as follows :
0 0 1			CHANNEL PROGRAM ADDRESS	
0 1 0			FIRST WORD ADDRESS	
0 1 1			CHARACTER COUNTER	
1 0 0			BUFFER	
1 0 1			REMAINING CHAR. COUNT	
1 1 0			EVENT STATUS	
1 1 1			COMMAND REGISTER	

1 2 3	
No CP at all	0 0 0
CP to bits 16:23	0 0 1
CP to bits 8:15	0 1 0
CP to bits 0:7	1 0 0
CP to bits 0:23	1 1 1

EXTERNAL DESTINATION X=DON'T CARE

ADDR. 0 1 2	F = FUNCTIONS 1 2 3	4	5 6 7	EXTERNAL DESTINATION REG.	COMMENTS
X 0 0	DON'T CARE		0 1 0	TRANSM. CHAR. BUFFER 0:7	F5, 6 & 7 being = 0, 1, 0 generates "CLEAR TRM DONE", which also loads TRM. CHAR. BUFFER
X 0 1			0 1 0	TRANSM. CHAR. BUFFER 0:7	
X 1 0			0 1 0	TRANSM. CHAR. BUFFER 8:15	
X 1 1			0 1 0	TRANSM. CHAR. BUFFER 16:23	
DON'T CARE	DON'T CARE		1 0 0	I/O DATA REGISTER	F5, 6 & 7 being = 1 0 1 loads I/O ADDRESS REGISTER and generates MASTER REQUEST F4 = 0 WRITE, F4 = 1 READ
		1/0	1 0 1	I/O ADDRESS REGISTER	
0 0 0	DON'T CARE	1/0	1 1 0	TIMER STATUS	These 1-bits registers are loaded when F5, 6 & 7 = 1, 1, 0 F4 = 0 clear register F4 = 1 set register
0 0 1		1/0	1 1 0	⁻ INITIATE	
0 1 0		1/0	1 1 0	SENSE	
0 1 1		1/0	1 1 0	WAIT	
1 0 0		1/0	1 1 0	TRANSMIT BLOCK END	
1 0 1		1/0	1 1 0	AUTOLOAD	
1 1 0		1/0	1 1 0	END OF READ CHAIN	
1 1 1		1/0	1 1 0		

INSTRUCTION MICRO CODES

Mnemonic	MICRO CODE I_2	I_1	I_0	Octal Code	ALU SOURCE OPERANDS R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Figure 2. ALU Source Operand Control.

Mnemonic	MICRO CODE I_5	I_4	I_3	Octal Code	ALU Function	SYMBOL
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R∨S
AND	H	L	L	4	R AND S	R∧S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$∧S
EXOR	H	H	L	6	R EX-OR S	R∨S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \vee S}$

Figure 3. ALU Function Control.

Mnemonic	MICRO CODE I_8	I_7	I_6	Octal Code	RAM FUNCTION Shift	Load	Q-REG. FUNCTION Shift	Load	Y OUTPUT	RAM SHIFTER RAM_0	RAM_3	Q SHIFTER Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Figure 4. ALU Destination Control.

I_{210} OCTAL / I_{543} OCTAL / ALU Source / ALU Function	0	1	2	3	4	5	6	7
	A, Q	A, B	Q, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L: R Plus S; C_n = H: R Plus S Plus 1	A+Q / A+Q+1	A+B / A+B+1	Q / Q+1	B / B+1	A / A+1	D+A / D+A+1	D+Q / D+Q+1	D / D+1
1	C_n = L: S Minus R; C_n = H: S Minus R Minus 1	Q−A−1 / Q−A	B−A−1 / B−A	Q−1 / Q	B−1 / B	A−1 / A	A−D−1 / A−D	Q−D−1 / Q−D	−D−1 / −D
2	C_n = L: R Minus S; C_n = H: R Minus S Minus 1	A−Q−1 / A−Q	A−B−1 / A−B	−Q−1 / −Q	−B−1 / −B	−A−1 / −A	D−A−1 / D−A	D−Q−1 / D−Q	D−1 / D
3	R OR S	A∨Q	A∨B	Q	B	A	D∨A	D∨Q	D
4	R AND S	A∧Q	A∧B	0	0	0	D∧A	D∧Q	0
5	$\overline{R}$ AND S	$\overline{A}$∧Q	$\overline{A}$∧B	Q	B	A	$\overline{D}$∧A	$\overline{D}$∧Q	B
6	R EX-OR S	A∨Q	A∨B	Q	B	A	D∨A	D∨Q	D
7	R EX-NOR S	$\overline{A \vee Q}$	$\overline{A \vee B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \vee A}$	$\overline{D \vee Q}$	$\overline{D}$

+ = Plus, − = Minus, ∨ = OR, ∧ = AND, ∨ = EX OR

Figure 5. Source Operand and ALU Function Matrix.

Octal I_{543} I_{210}	Group	Function
4 0	AND	A∧Q
4 1		A∧B
4 5		D∧A
4 6		D∧Q
3 0	OR	A∨Q
3 1		A∨B
3 5		D∨A
3 6		D∨Q
6 0	EX-OR	A∨Q
6 1		A∨B
6 5		D∨A
6 6		D∨Q
7 0	EX-NOR	$\overline{A \vee Q}$
7 1		$\overline{A \vee B}$
7 5		$\overline{D \vee A}$
7 6		$\overline{D \vee Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$∧Q
5 1		$\overline{A}$∧B
5 5		$\overline{D}$∧A
5 6		$\overline{D}$∧Q

Figure 6. ALU Logic Mode Functions.

Octal I_{543} I_{210}	C_n = 0 (Low) Group	Function	C_n = 1 (High) Group	Function
0 0	ADD	A+Q	ADD plus one	A+Q+1
0 1		A+B		A+B+1
0 5		D+A		D+A+1
0 6		D+Q		D+Q+1
0 2	PASS	Q	Increment	Q+1
0 3		B		B+1
0 4		A		A+1
0 7		D		D+1
1 2	Decrement	Q−1	PASS	Q
1 3		B−1		B
1 4		A−1		A
2 7		D−1		D
2 2	1's Comp.	−Q−1	2's Comp. (Negate)	−Q
2 3		−B−1		−B
2 4		−A−1		−A
1 7		−D−1		−D
1 0	Subtract (1's Comp)	Q−A−1	Subtract (2's Comp)	Q−A
1 1		B−A−1		B−A
1 5		A−D−1		A−D
1 6		Q−D−1		Q−D
2 0		A−Q−1		A−Q
2 1		A−B−1		A−B
2 5		D−A−1		D−A
2 6		D−Q−1		D−Q

Figure 7. ALU Arithmetic Mode Functions.

OCTAL I_8 I_7, I_5 I_3, I_2 I_0	CARRY IN 20 : 23	FUNCTION	RAM LOAD	Y-OUT
0 0 0	0	NOOP	NONE	F
* 2 1 4	1	PASS A	F → B	A
3 4 4	1	ZERO	-	F
3 3 5	0	D OR A	-	F
3 1 4	0	A − 1	-	F
3 0 5	0	D + A	-	F
3 0 1	0	A + B	-	F
3 0 4	1	A + 1	-	F
3 0 7	0	PASS D	-	F

* NO CLOCK PULSE TO RAM

FIG. 8 FUNCTIONS USED IN FPA 802

CONDITION MICRO CODES

	CON. SELECT	CONDITION 0	CONDITION 1
0	0 0 0 0	~TRANSMITTER DONE	TIMER
1	0 0 0 1	~BUS READY	~BUS ERROR
2	0 0 1 0	~BUS TIME OUT	~DATA P. OK
3	0 0 1 1	REQUEST IN	ATTENTION
4	0 1 0 0	RECEIVER DONE	PARITY ERROR
5	0 1 0 1	RECEIVE BLOCK END	END OF READ CHAIN
6	0 1 1 0	~START	~INITIATE
7	0 1 1 1	SENSE	~RESET
8	1 0 0 0	INTERN BUS 13	SUB DEV. SELECTOR
9	1 0 0 1	INTERN BUS 14	INTERN BUS 15
10	1 0 1 0		F = 0
11	1 0 1 1	TIMER STATUS	INTERN BUS 16
12	1 1 0 0		
13	1 1 0 1	INTERN BUS 22	INTERN BUS 23
14	1 1 1 0	WAIT	
15	1 1 1 1	NEXT CONDITION 0	NEXT CONDITION 1

800214 VH 800716 JOM

FPA 801 COMMANDS.

COMMAND FIELD 12	13	14	15	CON-TINUE BIT 16	CHANNEL COMMAND WORD 1	FIRST WORD ADDRESS WORD 2	CHARACTER COUNT WORD 3
X	0	0	0	X	SENSE	FIRST WORD ADDR	X
X	0	0	1	D	READ	FIRST WORD ADDR	CHAR COUNT
X	0	1	1	D	WRITE	FIRST WORD ADDR	CHAR COUNT
X	1	0	0	X	WAIT	X	X
X	1	1	0	X	CONTROL	X	X
X	1	1	1	X	STOP	X	X

X denotes parameters or bits not used.

FPA 801 EVENT STATUS.

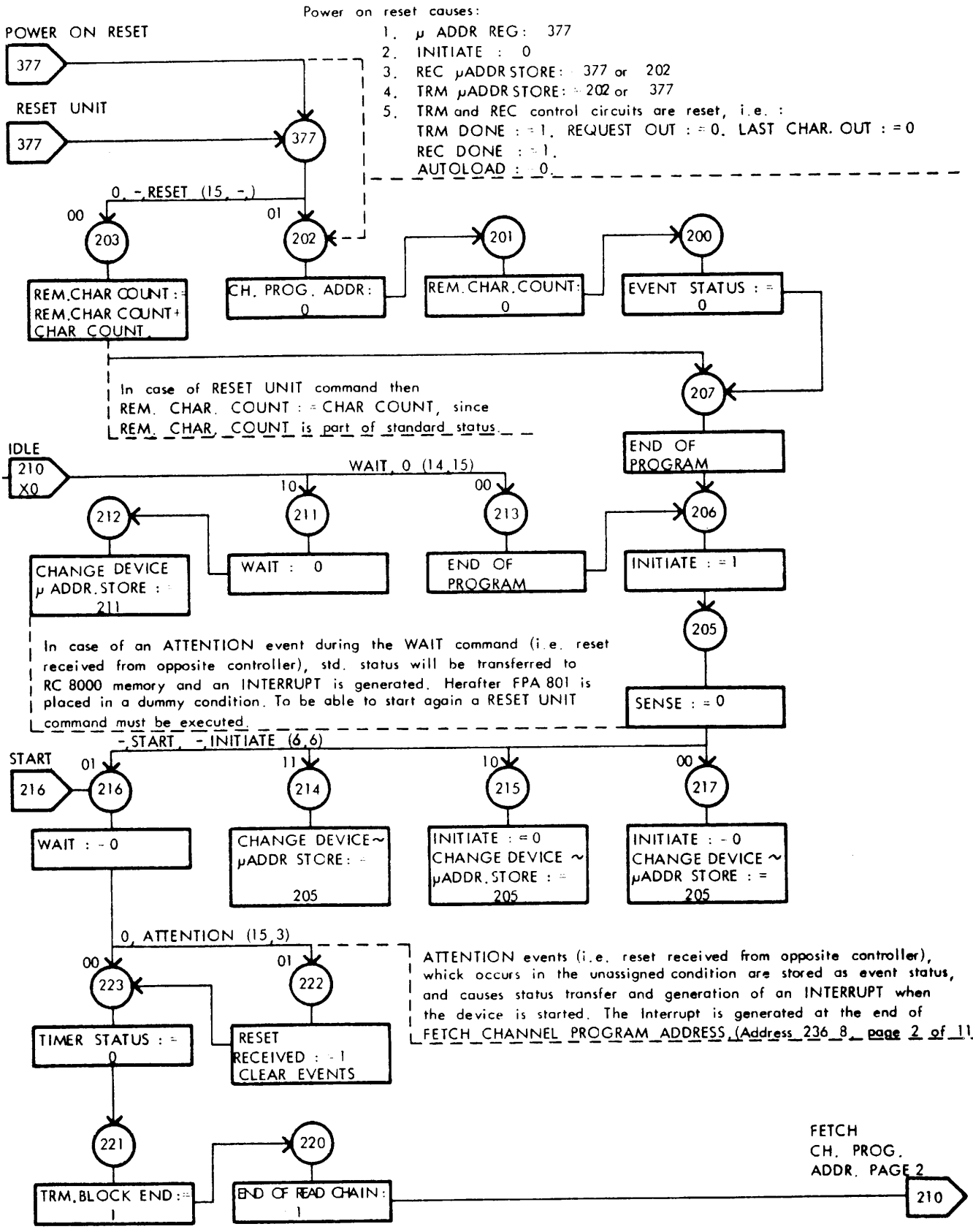
BIT	RECEIVER INTERPRETATION	TRANSMITTER INTERPRETATION
0	RESET RECEIVED	X
1	PARITY ERROR IN MEDIUM	PARITY ERROR IN MEDIUM
2	TIME - OUT	TIME - OUT
4	BLOCK LENGTH ERROR	BLOCK LENGTH ERROR
20	BUS PARITY ERROR	BUS PARITY ERROR
21	STATUS TRANSFER ERROR	STATUS TRANSFER ERROR
22	BUS TIME OUT	BUS TIME OUT
23	BUS COMMUNICATION ERROR	BUS COMMUNICATION ERROR

FPA 801 CURRENT STATUS.

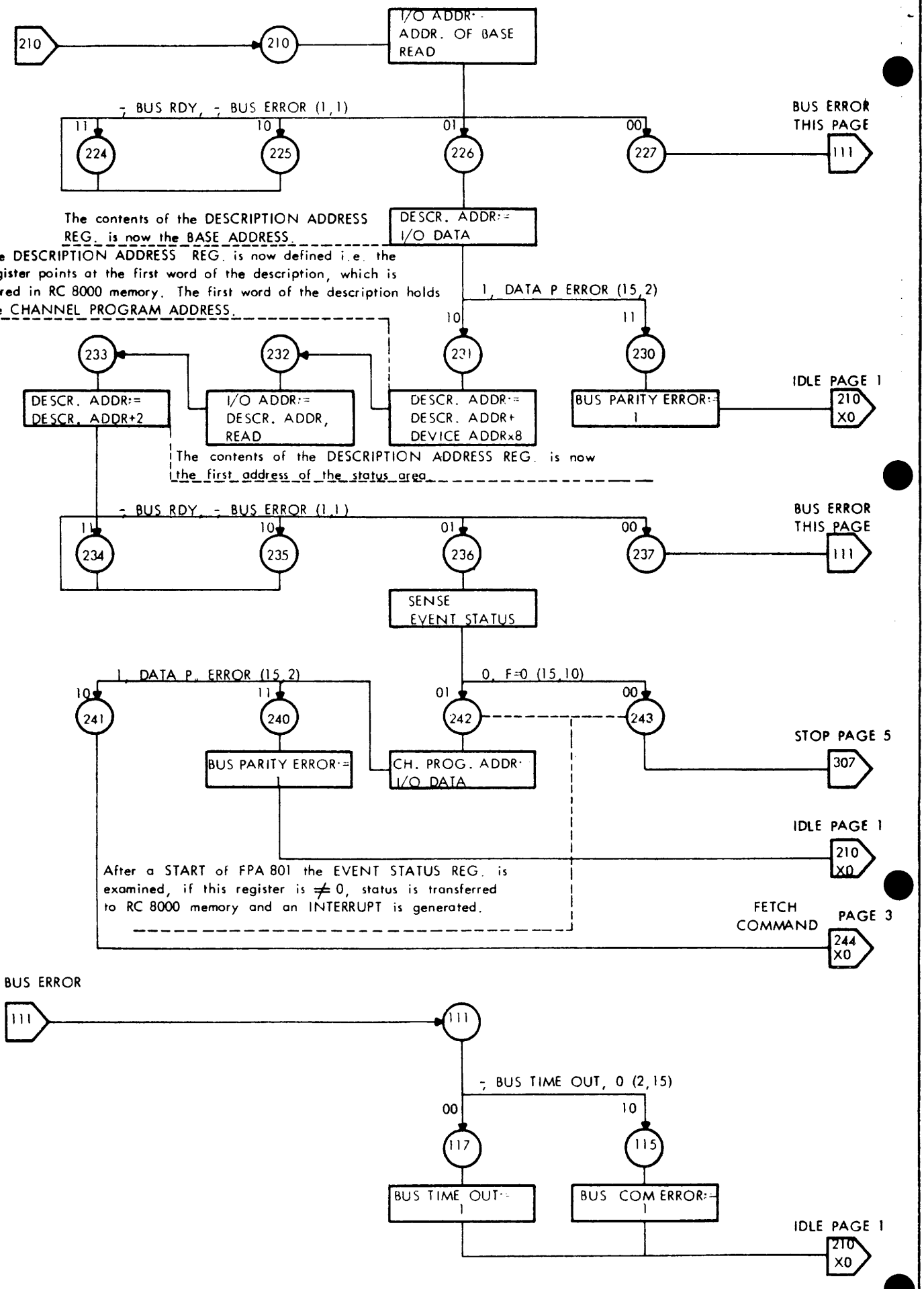
BIT	RECEIVER INTERPRETATION	TRANSMITTER INTERPRETATION
0	FRONT END DISCONNECTED	FRONT END DISCONNECTED
21	DEVICE KIND = 0	DEVICE KIND = 1
23	BLOCK ORIENTATED = 1	BLOCK ORIENTATED = 1

remaining bits are always zero.

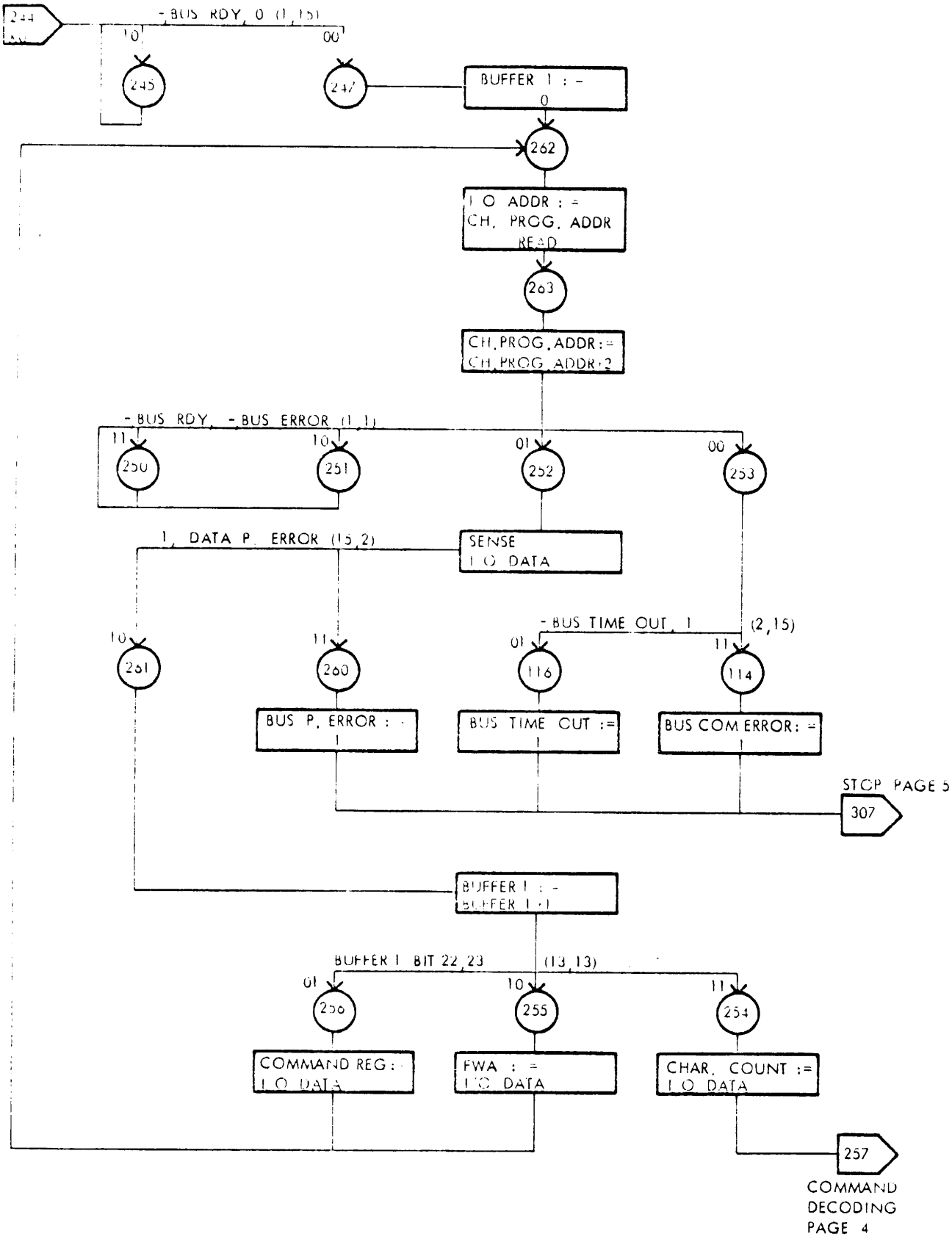
751008 VH 770330 OKJ 770412 LLM, 770412 VH.



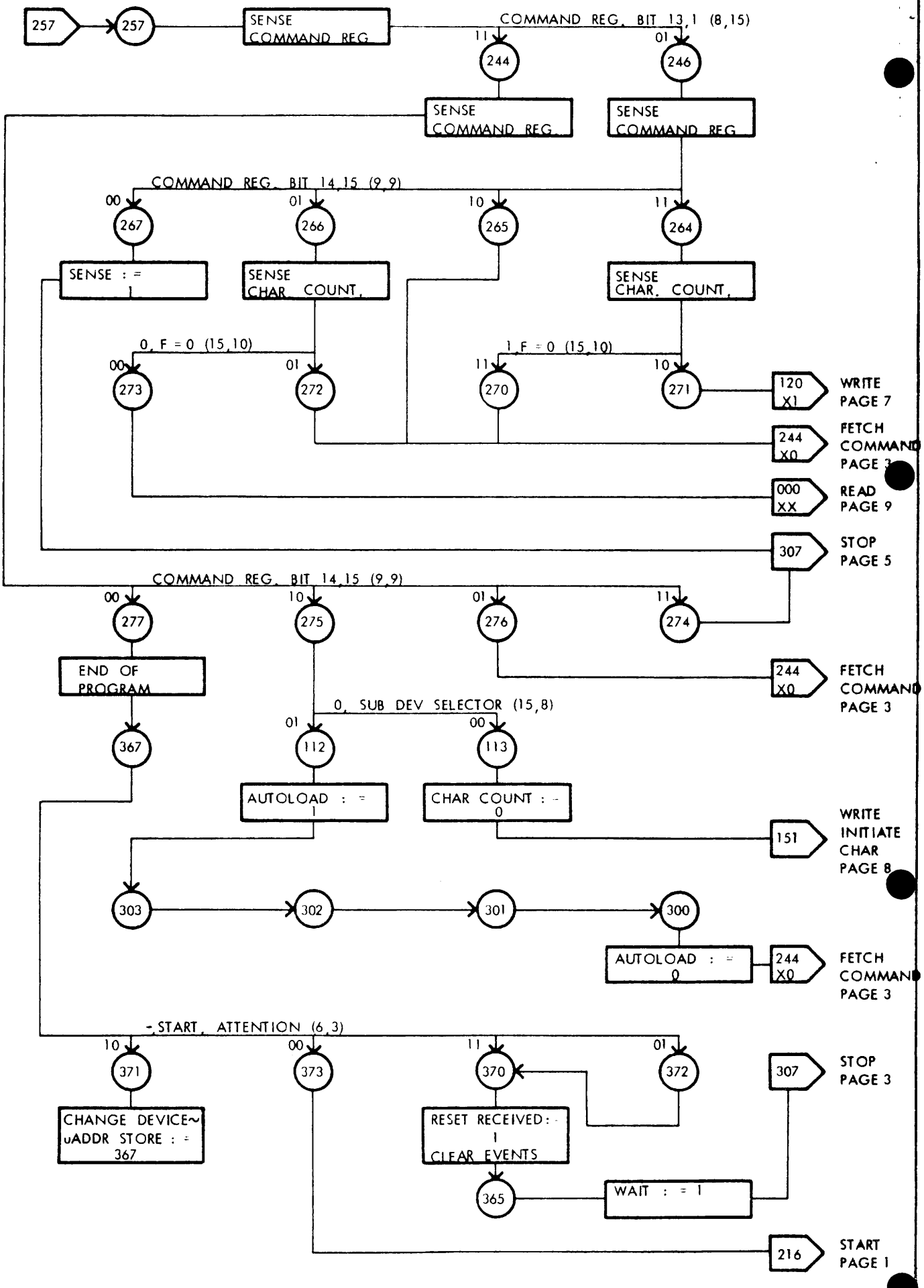
750320 VH. 770331 AMS 770412 LLM. 770412 VH.



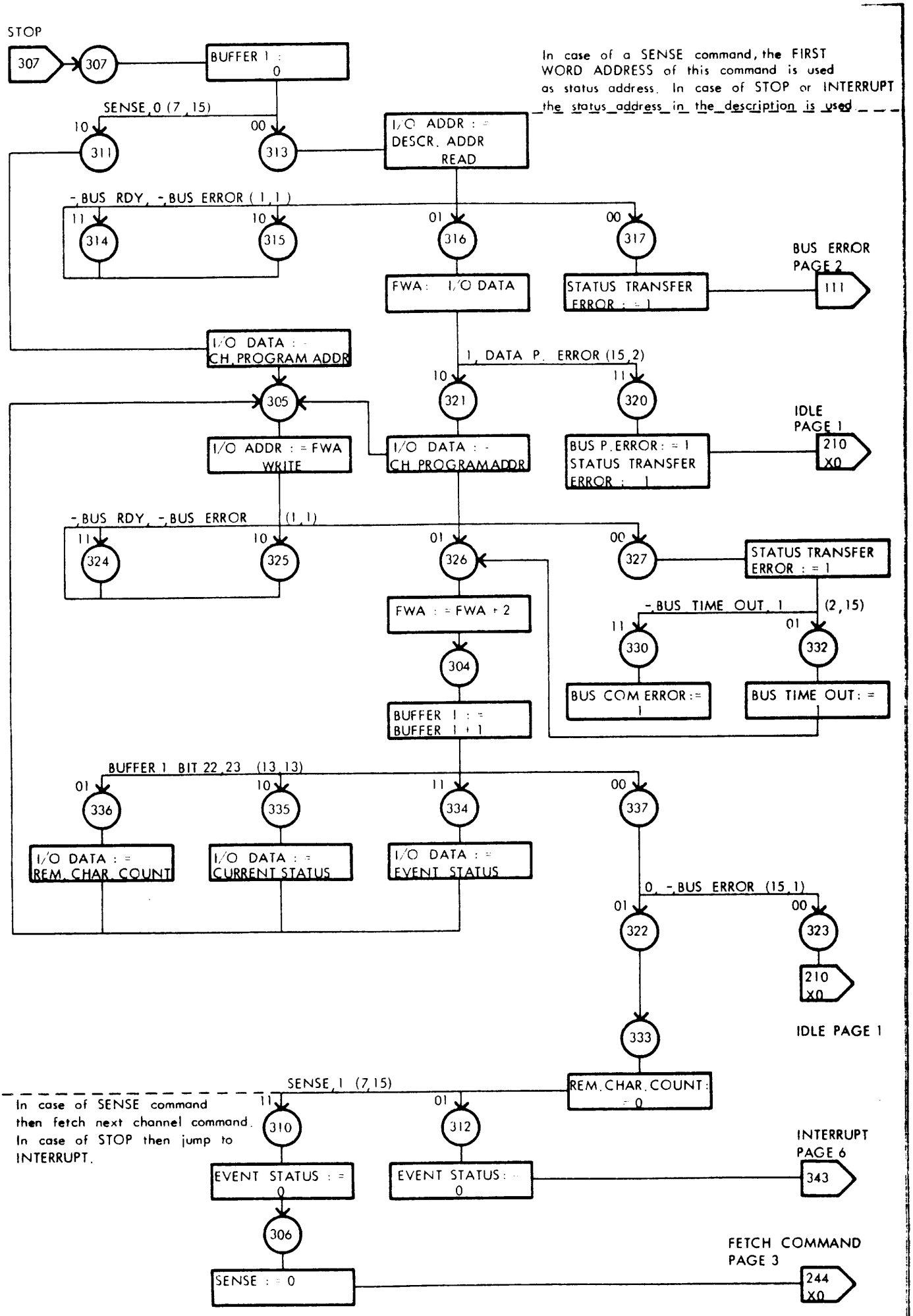
751017 VH 770330 OKJ 770412 LLM, 770412 VH.



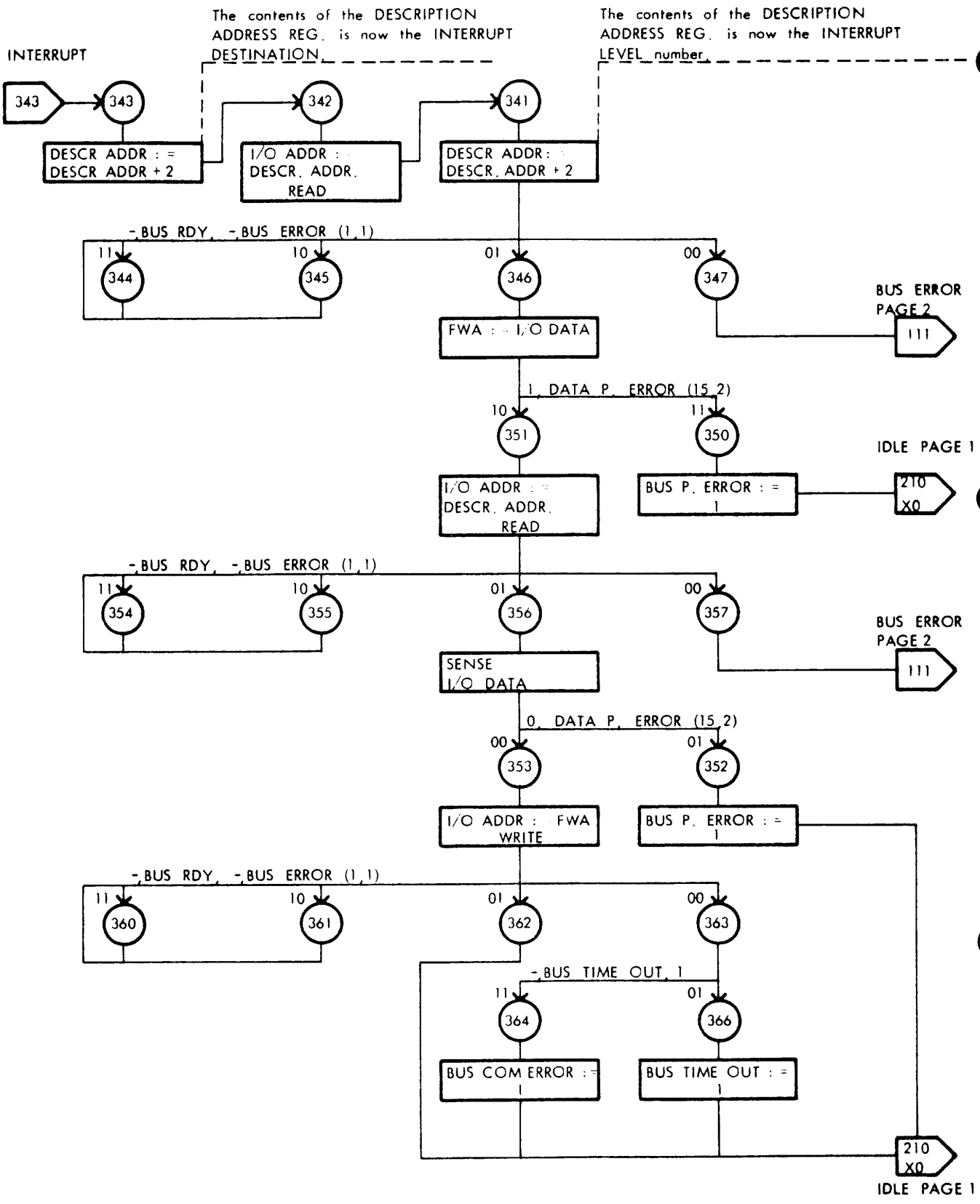
760130 VH. 770331 AMS. 770412 LLM. 770412 VH.



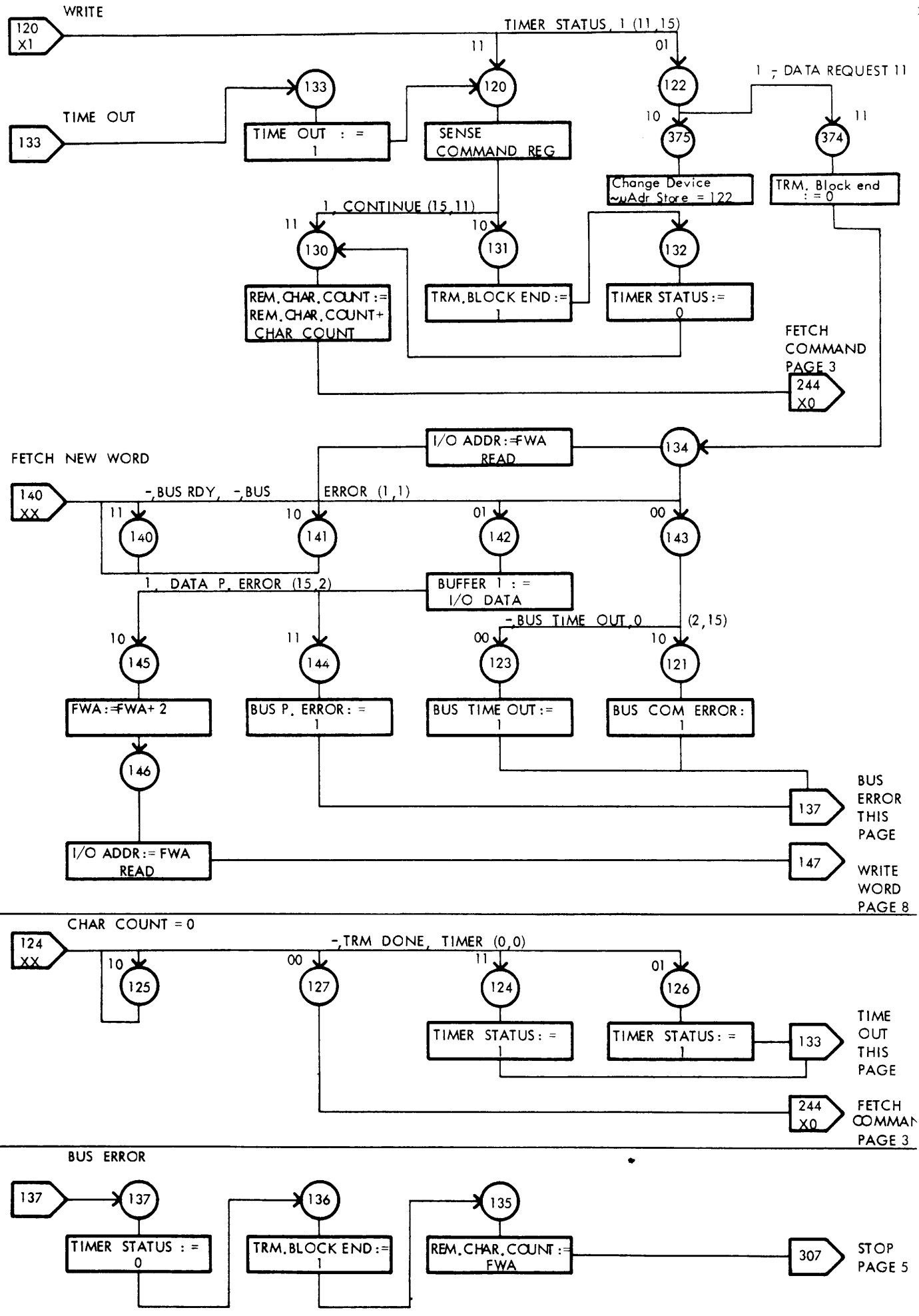
760130 VH. 770331 AMS. 770412 LLM. 770412 VH.



751018 VH 770406 AMS, 770412 LLM, 770412 VH.



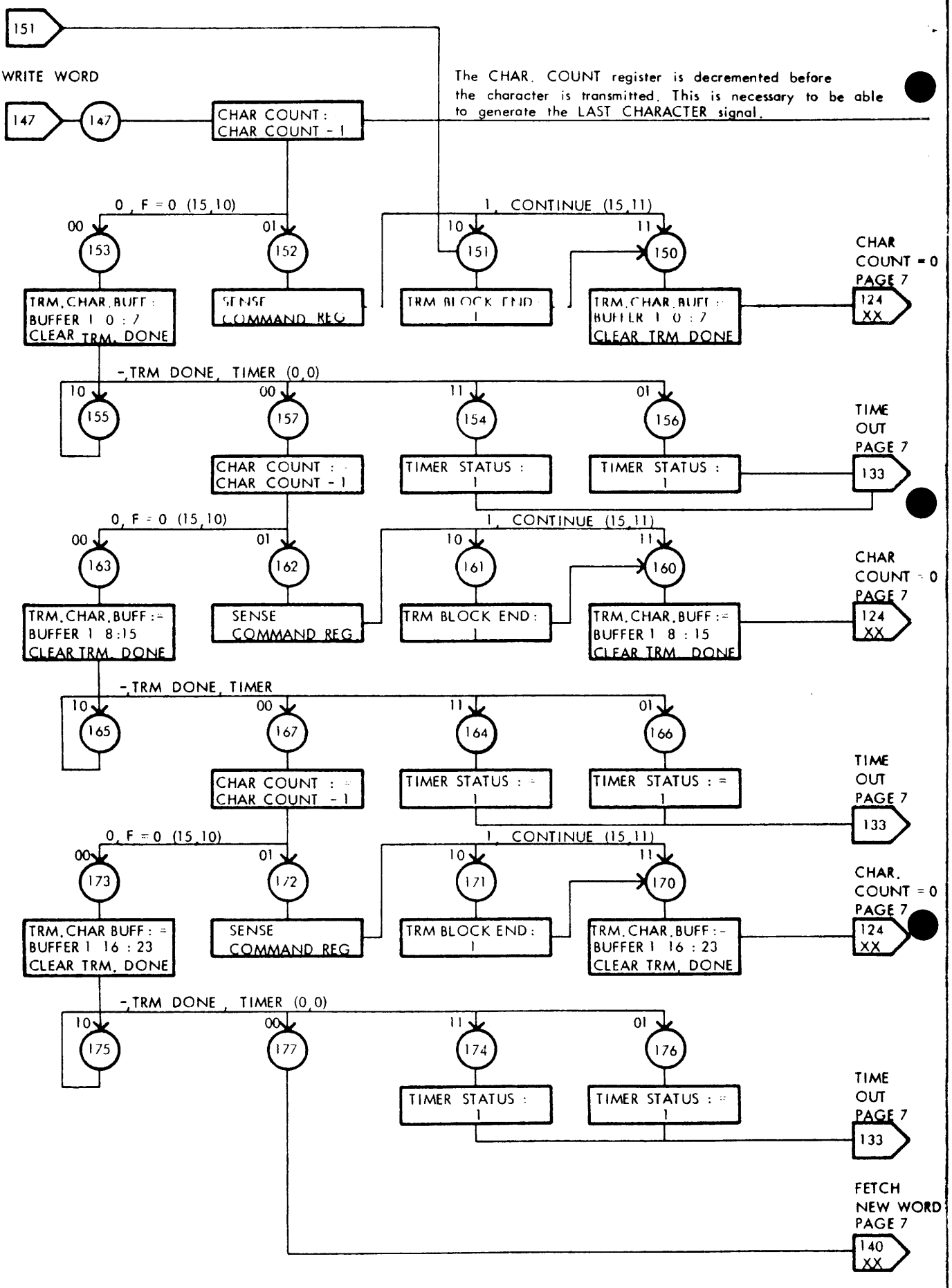
751020 VH. 770406 AMS. 770412 LLM. 770412 VH.



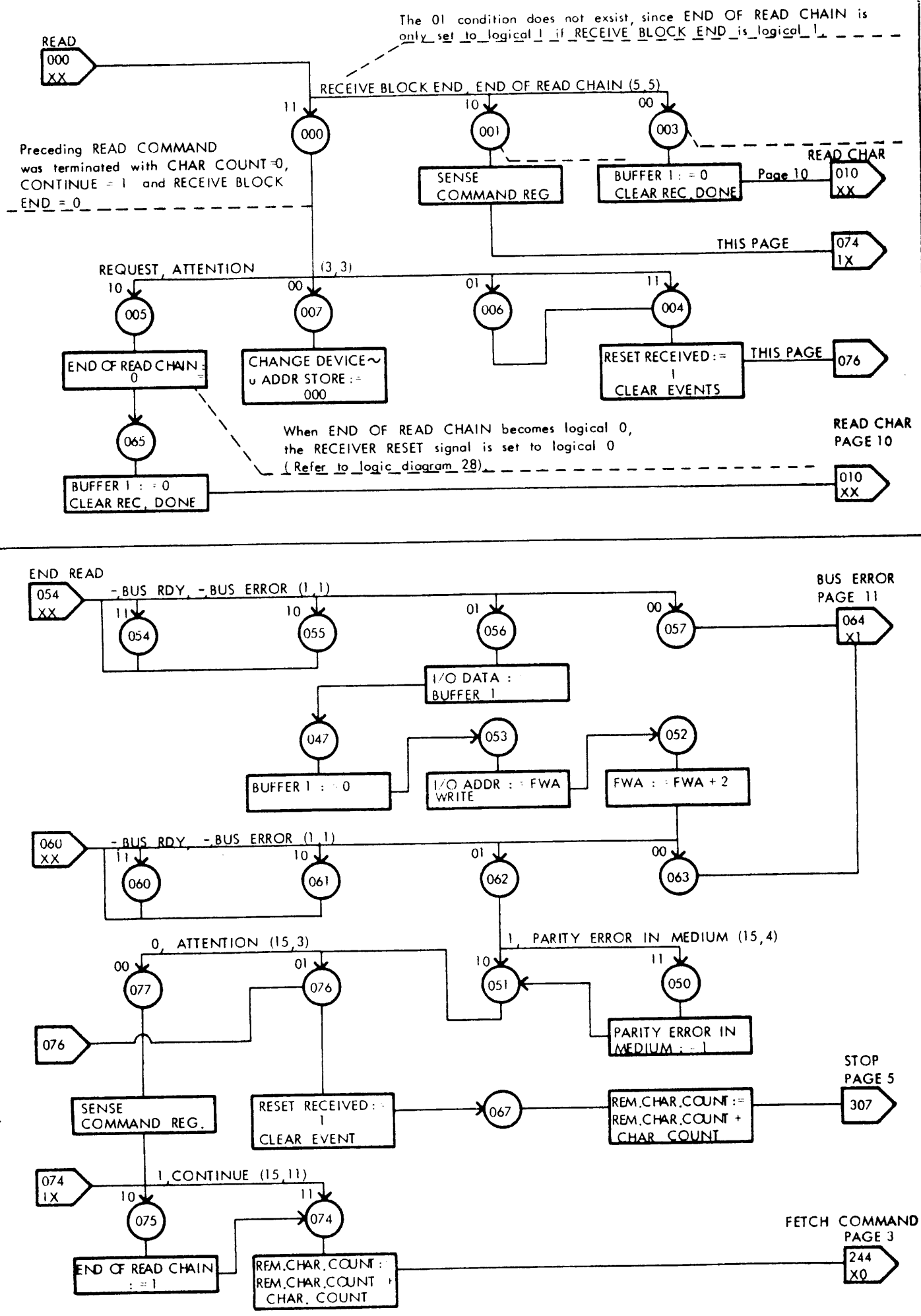
841109 OKJ

840131 VH

WRITE INITIATE CHAR.



760203 VH, 770420 AMS, 770425 LLM 770425 VH



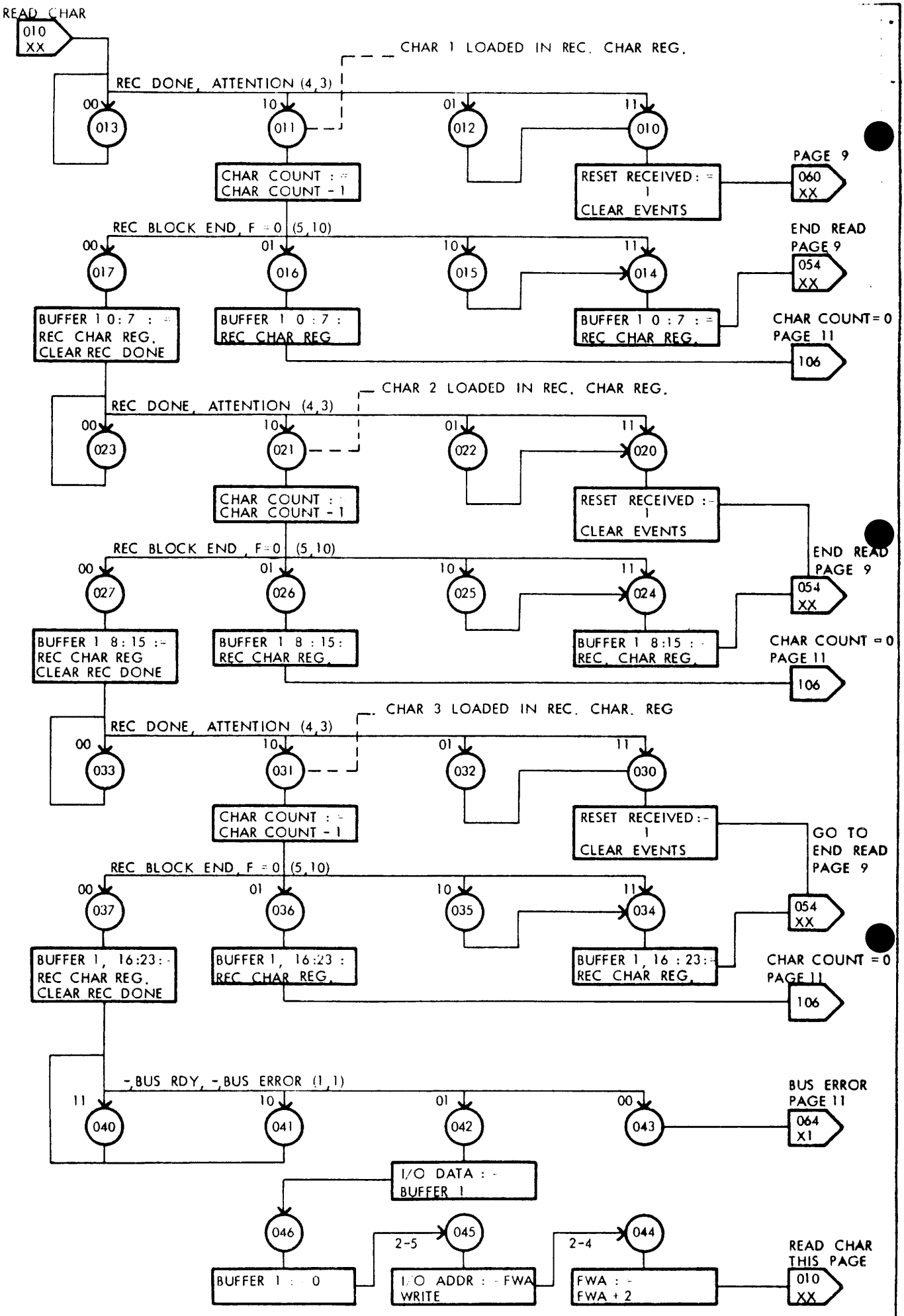
751015 VH, 770425 AMS, 770527 OKJ 770527 VH

FPA 801

READ PROGRAM PART 1

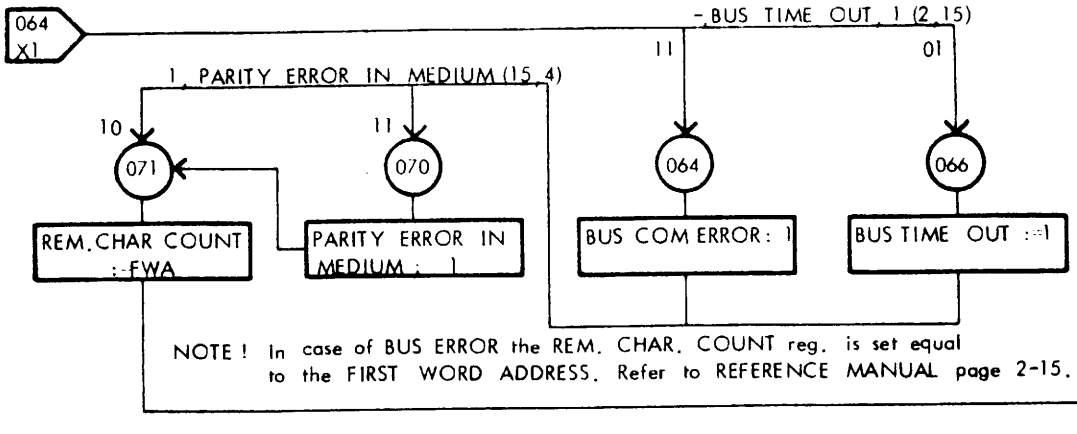
P 9 of 11

A12853

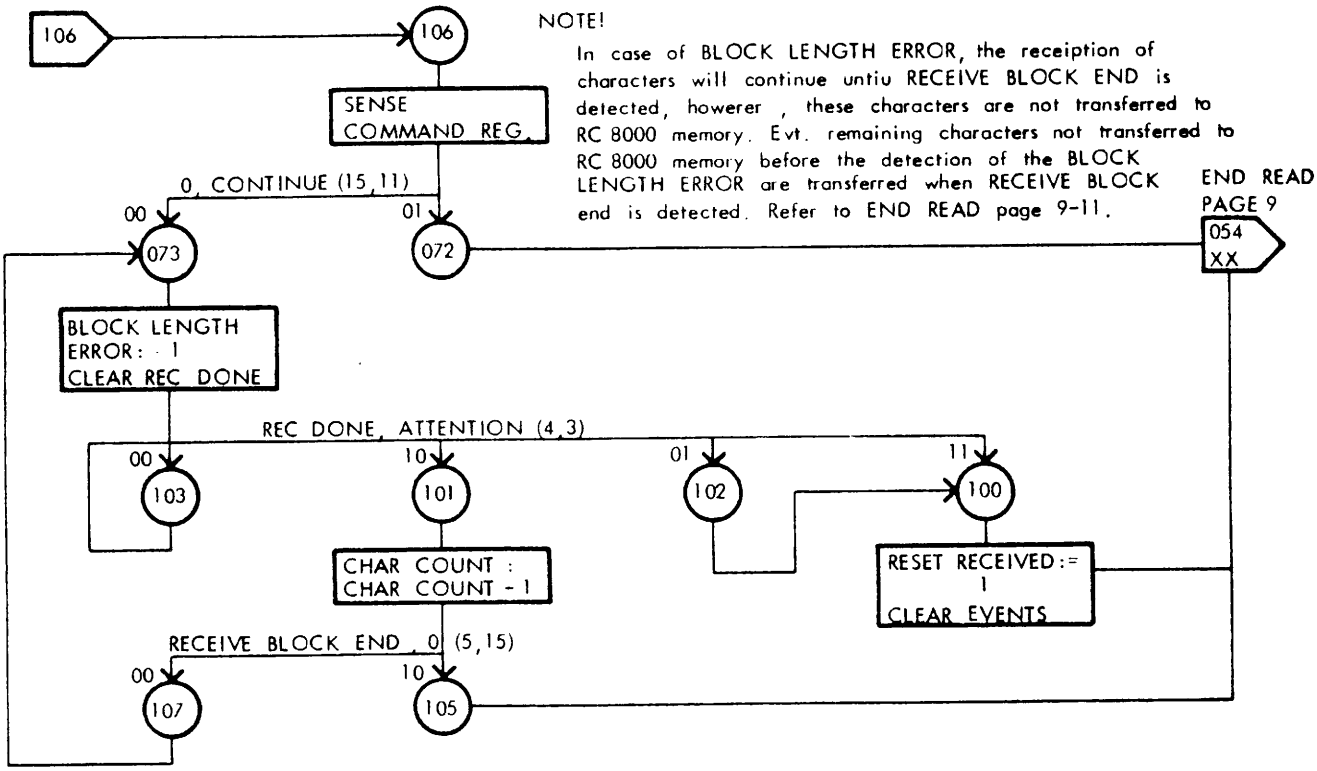


750919 VH, 770420 AMS, 77C425 LLM 770425 VH

BUS ERROR



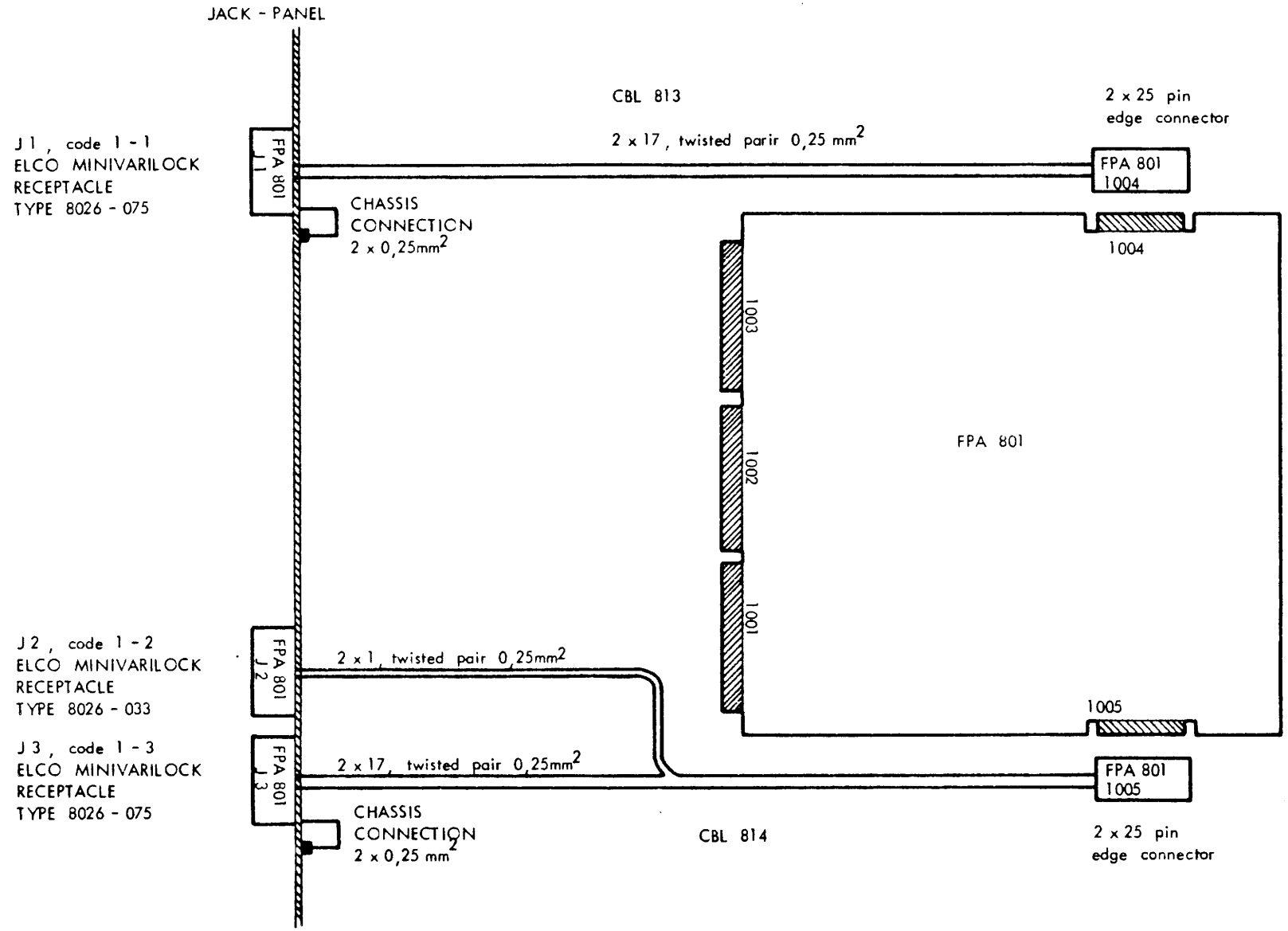
CHAR COUNT = 0



751015 VH. 770420 AMS. 770425 LLM 770425 VH

FPA 801
A12885

ASSEMBLY DRAWING



RC doc. VB 139

A/S REGNECENTRALEN	Designed by VH 2/12 - 76	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.

Unit: FDA 801
Dwg. No.: A2474 8

PLUG 1001 ON PRINTED CIRCUIT BOARD

PLUG 1001 A	SIGNAL	PLUG 1001 B	SIGNAL	PLUG 1001 C	SIGNAL
1	+5V	1	+5V	1	+5V
2	0V	2	7BSEL 0 in	2	7BREQ 0
3	0V	3	7BSEL 0 out	3	7BREQ 1
4	0V	4	7BSEL 1 in	4	7CSEL
5	0V	5	7BSEL 1 out	5	7SACK
6	0V	6	7SYS RESET	6	7DATA OUT
7	0V	7	7DATA RDY	7	7BBSY
8	0V	8	7ACK	8	POK
9	0V	9	7NACK	9	7PINT
10	0V	10	7ADDR (0)	10	7ADDR (1)
11	0V	11	- (2)	11	- (3)
12	0V	12	- (4)	12	- (5)
13	0V	13	- (6)	13	- (7)
14	0V	14	- (8)	14	- (9)
15	0V	15	- (10)	15	- (11)
16	0V	16	- (12)	16	- (13)
17	0V	17	- (14)	17	- (15)
18	0V	18	- (16)	18	- (17)
19	0V	19	- (18)	19	- (19)
20	0V	20	- (20)	20	7ADDR (21)
21	0V	21	7ADDR (22)	21	7ADDR PAR
22	0V	22	7DATA (0)	22	7DATA (1)
23	0V	23	- (2)	23	- (3)
24	0V	24	- (4)	24	- (5)
25	0V	25	- (6)	25	- (7)
26	0V	26	- (8)	26	- (9)
27	0V	27	- (10)	27	- (11)
28	0V	28	- (12)	28	- (13)
29	0V	29	- (14)	29	- (15)
30	0V	30	7DATA (16)	30	7DATA (17)
31	Spec. Voltage	31	Spec Voltage	31	Spec. Voltage
32	+5V	32	+5V	32	+5V

RC doc: VB 139

A/S REGNECENTRALEN	Designed by VH 2/12 - 76	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.

Unit: FPR 801

Dwg. No.: A/H/T?

PLUG 1002 ON PRINTED CIRCUIT BOARD

PLUG 1002 A	SIGNAL	PLUG 1002 B	SIGNAL	PLUG 1002 C	SIGNAL
1	+5V	1	+5V	1	+5V
2	0V	2	7 DATA (18)	2	7 DATA (19)
3	0V	3	- (20)	3	- (21)
4	0V	4	7 DATA (22)	4	7 DATA (23)
5	0V	5	7 DATA PAR (0)	5	7 DATA PAR (1)
6	0V	6	7 DATA PAR (2)	6	
7	0V	7		7	
8	0V	8		8	
9	0V	9		9	
10	0V	10		10	
11	0V	11		11	
12	0V	12		12	
13	0V	13		13	
14	0V	14		14	
15	0V	15		15	
16	0V	16		16	
17	0V	17		17	
18	0V	18		18	
19	0V	19		19	
20	0V	20		20	
21	0V	21		21	
22	0V	22		22	
23	0V	23		23	
24	0V	24		24	
25	0V	25		25	
26	0V	26		26	
27	0V	27		27	
28	0V	28		28	
29	0V	29		29	
30	0V	30		30	
31	Spec. Voltage	31	Spec. Voltage	31	Spec Voltage
32	+5V	32	+5V	32	+5V

PLUG 1004 A	SIGNAL	PLUG 1004 B	SIGNAL
1	DATA LINE 0 OUT A	1	DATA LINE 0 OUT B
2	- 1 -	2	- 1 -
3	- 2 -	3	- 2 -
4	- 3 -	4	- 3 -
5	- 4 -	5	- 4 -
6	- 5 -	6	- 5 -
7	- 6 -	7	- 6 -
8	- 7 -	8	- 7 -
9	PARITY LINE OUT A	9	PARITY LINE OUT B
10	RESET LINE OUT A	10	RESET LINE OUT B
11	REQ ACK LINE IN A	11	REQ ACK LINE IN B
12	DATA REQ LINE OUT A	12	DATA REQ LINE OUT B
13	STATUS REQ LINE OUT A	13	STATUS REQ LINE OUT B
14	AUTOLOAD LINE OUT A	14	AUTOLOAD LINE OUT B
15	CONN. LINE OUT A	15	CONN. LINE OUT B
16	LAST CHAR. LINE OUT A	16	LAST CHAR. LINE OUT B
17	0V	17	0V
18		18	
19		19	
20		20	
21		21	
22		22	
23		23	
24		24	
25		25	

Replaced by Dwg. No.

due to ECN

Replaces Dwg. No.

Design Check

Dwg. Office Check

Drawn by

Designed by VH 1/12 - 76

A/S REGNECENTRALEN

Unit FPA 801

Dwg. No. A-4150

PLUG 1004

On PRINTED CIRCUIT BOARD

RC doc: V8 139

PLUG 1005 A	SIGNAL	PLUG 1005 B	SIGNAL
1	DATA LINE 0 IN A	1	DATA LINE 0 IN B
2	— 1 —	2	— 1 —
3	— 2 —	3	— 2 —
4	— 3 —	4	— 3 —
5	— 4 —	5	— 4 —
6	— 5 —	6	— 5 —
7	— 6 —	7	— 6 —
8	— 7 —	8	— 7 —
9	PARITY LINE IN A	9	PARITY LINE IN B
10	RESET LINE IN A	10	RESET LINE IN B
11	REQ ACK LINE OUT A	11	REQ ACK LINE OUT B
12	DATA REQ LINE IN A	12	DATA REQ LINE IN B
13	STATUS REQ LINE IN A	13	STATUS REQ LINE IN B
14	AUTOLOAD LINE IN A	14	AUTOLOAD LINE IN B
15	CONN. LINE IN A	15	CONN. LINE IN B
16	LAST CHAR LINE IN A	16	LAST CHAR. LINE IN B
17	0V	17	0V
18		18	
19		19	
20		20	
21		21	
22		22	
23		23	
24		24	
25	REMOTE AUTOLOAD	25	0V

Replaced by Dwg. No.

due to ECN

Replaces Dwg. No.

Design Check

Dwg. Office Check

Drawn by

Designed by VH 1/12-76

A/S REGNECENTRALEN

Unit: FPA 801

Dwg. No.: 42751

PLUG 1005
on PRINTED CIRCUIT BOARD

RC doc: VB 139

ANTAL	ENHED	MODUL NR	PA PART NR.	DOK / TEGN. NR	BETEGNELSE
1	STK	FKV 813			FORKANTVINKEL FPA803
1	STK				UMONTERET PRINTKORT PCB 570
3	STK		1301078		STIK ELCO 00-8257-096-000-123
6	STK		27109003		2.5×10 CHJ HFC 9033
3	–		27122005		3×8 UHJ HFC 9030
5	–		28001004		M3 MØTRIK HFC 9805
6	–		28001010		2M5 MØTRIK HFC 9832
3	–		28203001		1/8 (3) FJEDERSKIVE HFC 1280
2	–		34601022		UDTRÆKKERTAP CHS 701-22
4	–		14030007		TESTTÅRNE
1	–		1521009		SWITCH ALCO MTM-106D-RA
1			802011		KONDENS. 5% 63V 10pF
6			802018		—"— 33pF
1			802022		—"— 68pF
2			802024		—"— 100pF
2			802026		—"— 150pF
2			802029		—"— 220pF
1			814003		—"— 10% 250V 10nF
1			814006		—"— —"— 33nF
33			848002		KONDENS. KERAMISK 47nF/12V

BETEGNELSE		UDGAVE	
		02 820114HC	07
		03 820308HC	08
		04	09
PA PART NR	PA TEGN. PART NR	05	10
		06	11
DESIGN [signature]	STYKLISTE	MODUL NR. FPA 803	BLAD 1+
01 UDGAVE 6-11-81			

BETEGNELSE

PA PART NR

PA TEGN PART NR

UDGAVE

C2 C3 C4 C5 C6

IC7 IC8 IC9 IC: IC;

DESIGN

C UDGAVE 6-11-82

STYKLISTE

MODUL NR

TPE 802

BLAD 2+

ANTAL	ENHED	MODUL NR	PA PART NR	DOK / TEGN NR	BETEGNELSE
2	STK		101001		IC SN7400 N
1	-		101003		IC SN7402 N
1	-		101006		IC SN7410 N
1	-		101026		IC SN7474 N
2	-		101045		IC SN74150N
1	-		101064		IC SN7437N
2	-		101074		IC SN74170N
3	-		101082		IC SN74120N
2	-		101101		IC SN74109 N
1	-		101104		IC SN74279N
11	-		101106		IC SN74298N
5	-		101123		IC SN74273N
16	-		101132		IC SN75138N
1	-		101134		IC SN7492AN
2	-		101135		IC SN74393N.
3	-		101139		IC SN75182N
3	-		101140		IC SN75183N
1	-		101142		IC SN74132N
1	-		101005		IC SN7405N
1	-		101062		IC SN74123N
3	-		120010		IC 9334
3	-		136022		IC AM26LS31
3	-		136023		IC AM26LS32

BETEGNELSE	PA PART NR.	PA TEGN. PART NR.	UDGAVE
			02
			03
			04
			05
			06
			07
			08
			09
			10
			11

DESIGN MOS

01 UDGAVE 9-11-81

STYKLISTE

MODUL NR. FPA 802

BLAD 3+

ANTAL	ENHED	MODUL NR.	PA PART NR.	DOK. / TEGN. NR.	BETEGNELSE
2	STK		125001		IC SN 74S00N
2	–		125003		IC SN 74S04N
2	–		125005		IC SN 74S10N
1	–		125010		IC SN 74S40N
3	–		125013		IC SN 74S74N
1	–		125014		IC SN 74S112N
2	–		125015		IC SN 74S113N
1	–		125019		IC SN 74S138N
3	–		125021		IC SN 74S157N
1	–		125022		IC SN 74S158N
2	–		125028		IC SN 74S182N
7	–		125029		IC SN 74S280N
1	–		125032		IC SN 74S02N
1	–		125033		IC SN 74S08N
1	–		125034		IC SN 74S09N
2	–		125036		IC SN 74S132N
1	–		125037		IC SN 74S86N
1	–		125038		IC SN 74S124N
2	–		125039		IC SN 74S260N
12	–		130001		IC 93S253 PC
2	–		130002		IC 93S46
6	–		136001		IC AM2901
1	–		2701030		XTAL 16.000 MHz

ANTAL	ENHED	MODUL NR.	PA PART NR.	DOK. / TEGN NR	BETEGNELSE
1	STK		203015		TRANSISTOR 2N2907A
3	-		302020		DIODE 1N914
2	STK		1144011		SIL BOURNS 4308R-101-391 (7×390E)
2	STK		1205033		POTMETER BOURNS 5K 3299W-1-502
12	-		1103057		MODSTAND 5% 1/8W 1K
1	-		1103064		— " — 2K
1	-		1103069		— " — 3K3
10	-		1103047		— " — 390E
5	-		1103061		— " — 1K5
1	-		1103033		— " — 33 ~~100~~E
2	-		1103052		— " — 620E
1	-		1103092		— " — 30K
2	-		1103088		— " — 20K
2	-		1103049		— " — 470E
11	-		1119129		MODSTAND 2% 0,4W 120E
1	-		1325049		BERG MINIWRAP PINDE (1×2)
12	-				— " — (1×3)
6	-				— " — (1×4)
2	-		1325048		— " — (1×8)
10	-		1307126		MINI JUMP CONNECTOR.
2	-		701012		LED TIL 210
2	-		701042		SIEMENS NUS TIL LED

BETEGNELSE

PA PART NR.

PA TEGN. PART NR.

DESIGN Lars 01 UDGAVE 6-11-81

STYKLISTE

MODUL NR. TPB 803

BLAD 4+

UDGAVE 02 03 04 05 06 07 08 09 10 11

BETEGNELSE

PA PART NR

PA TEGN. PART NR.

UDGAVE

02 8203088HC

01 UDGAVE 9-11-81

DESIGN

STYKLISTE

MODUL NR

EPB 803

BLAD 5

ANTAL	ENHED	MODUL NR	PA PART NR.	DOK / TEGN NR.	BETEGNELSE
1	Stk	ROM554	84201554		IC ROM 554
1	-	ROM555	84201555		IC ROM 555
1	-	ROM556	84201556		IC ROM 556
1	-	ROM557	84201557		IC ROM 557
1	-	ROM558	84201558		IC ROM 558
1	-	ROM559	84201559		IC ROM 559
1	-	ROM560	84201560		IC ROM 560
1	-	ROM561	84201561		IC ROM 561
1	-	ROM563	84201563		IC ROM 563
1	-	ROM893	84201893		IC ROM 893
1	-	ROM894	84201894		IC ROM 894
3	-		1001004		LYT TANTAL 22µF/15V
2	-		1001005		LYT TANTAL 68µF/15V
2	-		1001007		LYT TANTAL 15µF/20V
9	-		1319009		16 PIN SOKKEL
6	-		1319013		40 PIN SOKKEL
2	-		1319016		20 PIN SOKKEL.

97

	** ROM 00893 **								ROA 887 **							
	06	07	08	09	11	12	13	14	06	07	08	09	11	12	13	14
000000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000001	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1
000002	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000003	0	1	1	1	0	0	1	0	0	1	1	0	0	1	0	0
000004	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000005	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
000006	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000007	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000010	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000011	0	1	1	0	0	1	1	0	0	0	0	1	1	0	1	1
000012	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000013	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000014	0	1	1	0	0	0	1	1	1	0	1	0	0	1	0	0
000015	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000016	0	1	1	0	0	0	1	1	1	0	1	0	0	1	0	0
000017	0	1	1	0	0	0	1	1	1	0	1	0	0	1	0	0
000020	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000021	0	1	1	0	0	1	1	0	0	0	0	1	1	0	1	1
000022	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000023	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000024	0	1	1	0	0	0	1	1	1	0	1	0	0	1	0	0
000025	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000026	0	1	1	0	0	0	1	1	1	0	1	0	0	1	0	0
000027	0	1	1	0	0	0	1	1	1	0	1	0	0	1	0	0
000030	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000031	0	1	1	0	0	1	1	0	0	0	0	1	1	0	1	1
000032	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000033	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000034	0	1	1	0	0	0	1	1	1	0	1	0	0	1	0	0
000035	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000036	0	1	1	0	0	0	1	1	1	0	1	0	0	1	0	0
000037	0	1	1	0	0	0	1	1	1	0	1	0	0	1	0	0
000040	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000041	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000042	0	1	0	0	0	1	1	0	0	1	1	0	0	1	0	0
000043	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000044	0	1	1	0	0	0	1	0	1	0	0	1	0	0	1	0
000045	0	1	0	0	0	1	1	0	0	1	1	0	1	0	1	0
000046	0	1	1	1	0	0	1	0	0	1	1	0	0	1	0	0
000047	0	1	1	1	0	0	1	0	0	1	1	0	0	1	0	0
000050	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000051	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000052	0	1	1	0	0	0	1	0	1	0	0	1	0	0	1	0
000053	0	1	0	0	0	1	1	0	0	1	1	0	1	0	1	0
000054	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000055	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000056	0	1	0	0	0	1	1	0	0	1	1	0	0	1	0	0
000057	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000060	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000061	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000062	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000063	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000064	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000065	0	1	1	1	0	0	1	0	0	1	1	0	0	1	0	0
000066	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000067	0	1	1	0	0	0	0	0	1	0	1	0	1	0	1	1
000070	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000071	0	1	0	0	0	1	1	0	0	1	1	0	1	0	1	0
000072	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	** ROM 00893 **								ROA 887 **							
	06	07	08	09	11	12	13	14	06	07	08	09	11	12	13	14
000073	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000074	0	1	1	0	0	0	0	0	1	0	1	0	1	0	1	1
000075	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
000076	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000077	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1
000100	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000101	0	1	1	0	0	1	1	0	0	0	0	1	1	0	1	1
000102	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000103	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000104	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000105	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000106	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1
000107	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000111	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000112	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0
000113	0	1	1	1	0	0	1	0	0	1	0	1	1	0	1	1
000114	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000115	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000116	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000117	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000120	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1
000121	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000122	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000123	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000124	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000125	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000126	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000127	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000130	0	1	1	0	0	0	0	0	1	0	1	0	1	0	1	1
000131	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
000132	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000133	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000134	0	1	0	0	0	1	1	0	0	1	1	0	1	0	1	0
000135	0	1	0	0	0	1	1	0	0	1	1	0	1	0	1	0
000136	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
000137	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000140	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000141	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000142	0	1	1	0	0	0	1	1	1	0	1	0	0	1	0	0
000143	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000144	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000145	0	1	1	0	0	0	1	0	1	0	0	1	0	0	1	0
000146	0	1	0	0	0	1	1	0	0	1	1	0	1	0	1	0
000147	0	1	1	0	0	1	1	0	0	0	0	1	1	0	1	1
000150	0	1	0	0	0	1	1	0	0	1	0	0	0	1	0	0
000151	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
000152	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1
000153	0	1	0	0	0	1	1	0	0	1	0	0	0	1	0	0
000154	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000155	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000156	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000157	0	1	1	0	0	1	1	0	0	0	0	1	1	0	1	1
000160	0	1	0	0	0	1	1	0	0	1	0	1	0	1	0	0
000161	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
000162	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1
000163	0	1	0	0	0	1	1	0	0	1	0	1	0	1	0	0
000164	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000165	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	** ROM 00893 **								ROA 887 **							
	06	07	08	09	11	12	13	14	06	07	08	09	11	12	13	14
000166	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000167	0	1	1	0	0	1	1	0	0	0	0	1	1	0	1	1
000170	0	1	0	0	0	1	1	0	0	1	0	1	1	1	0	0
000171	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
000172	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1
000173	0	1	0	0	0	1	1	0	0	1	0	1	1	1	0	0
000174	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000175	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000176	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000177	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000200	0	1	1	1	0	0	1	0	0	1	1	1	0	1	1	0
000201	0	1	1	1	0	0	1	0	0	1	1	0	1	1	0	1
000202	0	1	1	1	0	0	1	0	0	1	0	0	1	0	0	1
000203	0	1	1	0	0	0	0	0	1	0	1	0	1	0	1	1
000204	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000205	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
000206	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
000207	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000210	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0
000211	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
000212	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000213	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000214	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000215	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
000216	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
000217	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
000220	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0
000221	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
000222	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000223	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000224	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000225	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000226	0	1	1	0	0	0	1	1	1	0	0	0	0	0	0	0
000227	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000230	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000231	0	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0
000232	0	1	0	0	0	1	1	0	0	1	1	0	1	0	0	0
000233	0	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0
000234	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000235	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000236	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	0
000237	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000240	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000241	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000242	0	1	1	0	0	0	1	1	1	0	0	0	1	0	0	1
000243	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000244	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1
000245	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000246	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1
000247	0	1	1	1	0	0	1	0	0	1	1	0	0	1	0	0
000250	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000251	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000252	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000253	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000254	0	1	1	0	0	0	1	1	1	0	0	1	1	0	1	1
000255	0	1	1	0	0	0	1	1	1	0	0	1	0	0	1	0
000256	0	1	1	0	0	0	1	1	1	0	1	1	1	1	1	1
000257	0	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1
000260	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0

	** ROM 00893 **								ROA 887 **							
	06	07	08	09	11	12	13	14	06	07	08	09	11	12	13	14
000261	0	1	1	0	0	0	1	0	0	1	1	0	0	1	0	0
000262	0	1	0	0	0	1	1	0	0	1	1	0	1	0	0	1
000263	0	1	1	0	0	0	1	0	1	0	0	0	1	0	0	1
000264	0	1	0	0	0	1	1	0	0	1	1	1	1	0	1	1
000265	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000266	0	1	0	0	0	1	1	0	0	1	1	1	1	0	1	1
000267	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
000270	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000271	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000272	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000273	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000274	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000275	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000276	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000277	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000300	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0
000301	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000302	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000303	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000304	0	1	1	0	0	0	1	0	0	1	1	0	0	1	0	0
000305	0	1	0	0	0	1	1	0	0	1	1	0	1	0	1	0
000306	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
000307	0	1	1	1	0	0	1	0	0	1	1	0	0	1	0	0
000310	0	1	1	1	0	0	1	0	0	1	1	1	0	1	1	0
000311	0	1	0	0	0	1	1	0	0	1	1	0	0	0	0	1
000312	0	1	1	1	0	0	1	0	0	1	1	1	0	1	1	0
000313	0	1	0	0	0	1	1	0	0	1	1	0	1	0	0	0
000314	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000315	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000316	0	1	1	0	0	0	1	1	1	0	0	1	0	0	1	0
000317	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000320	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000321	0	1	0	0	0	1	1	0	0	1	1	0	0	0	0	1
000322	0	1	1	1	0	0	1	0	0	1	0	0	1	0	0	1
000323	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000324	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000325	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000326	0	1	1	0	0	0	1	0	1	0	0	1	0	0	1	0
000327	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000330	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000331	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000332	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000333	0	1	1	1	0	0	1	0	0	1	1	0	1	1	0	1
000334	0	1	0	0	0	1	1	0	0	1	1	0	0	1	1	0
000335	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
000336	0	1	0	0	0	1	1	0	0	1	1	0	0	1	0	1
000337	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000340	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000341	0	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0
000342	0	1	0	0	0	1	1	0	0	1	1	0	1	0	0	0
000343	0	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0
000344	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000345	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000346	0	1	1	0	0	0	1	1	1	0	0	1	0	0	1	0
000347	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000350	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000351	0	1	0	0	0	1	1	0	0	1	1	0	1	0	0	0
000352	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000353	0	1	0	0	0	1	1	0	0	1	1	0	1	0	1	0

	** ROM 00893 **								ROA 887 **							
	06	07	08	09	11	12	13	14	06	07	08	09	11	12	13	14
000354	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000355	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000356	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000357	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000360	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000361	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000362	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000363	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000364	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000365	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
000366	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000367	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000370	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0
000371	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000372	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000373	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000374	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
000375	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000376	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000377	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	** ROM 00563 **				ROM 00563 **				ROM 00563 **				ROM 00563 **			
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12
000000	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000001	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0
000002	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000003	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000004	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000005	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000006	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000007	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000010	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000011	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
000012	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000013	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000014	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1
000015	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000016	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1
000017	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1
000020	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000021	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
000022	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000023	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000024	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1
000025	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000026	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1
000027	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1
000030	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000031	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
000032	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000033	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000034	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1
000035	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000036	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1
000037	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1
000040	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000041	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000042	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000043	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000044	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000045	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
000046	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000047	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000050	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000051	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000052	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000053	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
000054	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000055	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000056	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000057	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000060	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000061	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000062	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000063	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000064	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000065	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000066	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000067	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
000070	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000071	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
000072	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	** ROM 00563 **				ROM 00563 **				ROM 00563 **				ROM 00563 **			
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12
000073	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000074	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
000075	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000076	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000077	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0
000100	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000101	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
000102	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000103	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000104	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000105	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000106	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0
000107	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000110	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000111	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000112	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000113	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
000114	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000115	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000116	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000117	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000120	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0
000121	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000122	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000123	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000124	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000125	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000126	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000127	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000130	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
000131	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000132	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000133	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000134	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
000135	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
000136	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000137	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000140	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000141	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000142	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
000143	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000144	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000145	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000146	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
000147	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
000150	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000151	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000152	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0
000153	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000154	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000155	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000156	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000157	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
000160	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000161	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000162	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0
000163	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000164	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000165	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	** ROM 00563 **				ROM 00563 **				ROM 00563 **				ROM 00563 **			
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12
000166	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000167	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
000170	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000171	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000172	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0
000173	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000174	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000175	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000176	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000177	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000200	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
000201	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
000202	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
000203	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
000204	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000205	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000206	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000207	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000210	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000211	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000212	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000213	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000214	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000215	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000216	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000217	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000220	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000221	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000222	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000223	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000224	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000225	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000226	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
000227	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000230	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000231	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
000232	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000233	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000234	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000235	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000236	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
000237	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000240	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000241	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000242	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
000243	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000244	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0
000245	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000246	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0
000247	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000250	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000251	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000252	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
000253	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000254	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
000255	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
000256	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
000257	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0
000260	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1

	** ROM 00563 **				ROM 00563 **				ROM 00563 **				ROM 00563 **			
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12
000261	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000262	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
000263	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000264	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
000265	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000266	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
000267	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000270	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000271	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000272	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000273	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000274	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000275	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000276	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000277	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000300	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000301	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000302	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000304	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000305	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
000306	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000307	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
000310	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
000311	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
000312	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
000313	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000314	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000315	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000316	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
000317	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000320	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000321	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
000322	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
000323	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000324	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000325	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000326	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000327	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000330	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000331	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000332	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000333	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
000334	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
000335	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1
000336	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
000337	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000340	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000341	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000342	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000343	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000344	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000345	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000346	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
000347	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000350	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000351	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
000352	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000353	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0

	** ROM 00563 **				ROM 00563 **				ROM 00563 **				ROM 00563 **			
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12
000354	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000355	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000356	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
000357	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000360	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000361	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000362	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000363	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000364	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000365	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000366	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000367	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000370	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
000371	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000372	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000373	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000374	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000375	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000376	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000377	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	** ROA 886				** ROM 00560				** ROM 00559				** ROA 885				**
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12	
000000	0	0	0	0	1	1	1	0	1	1	0	0	1	1	0	0	
000001	1	1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	
000002	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
000003	0	0	0	0	1	1	0	1	0	0	1	0	1	1	0	0	
000004	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	
000005	1	1	0	0	0	1	1	0	1	1	1	1	1	1	1	1	
000006	0	0	0	0	1	1	1	0	1	1	1	1	1	1	1	1	
000007	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
000010	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	
000011	0	0	0	0	1	1	1	1	1	0	1	0	0	1	0	1	
000012	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	
000013	0	0	0	0	1	1	0	1	0	0	1	0	1	1	0	0	
000014	0	1	0	0	1	1	1	1	1	0	0	0	1	0	0	0	
000015	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	
000016	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	
000017	1	0	0	0	1	1	0	0	0	0	1	0	1	1	0	0	
000020	0	1	0	0	1	1	1	1	1	0	0	0	1	0	0	0	
000021	1	0	0	0	1	1	1	0	1	0	1	0	0	1	0	1	
000022	1	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1	
000023	1	0	0	0	1	1	0	0	0	0	1	0	1	1	0	0	
000024	0	1	0	0	1	1	1	1	1	0	0	0	1	0	0	0	
000025	1	0	0	0	1	1	1	0	1	1	1	1	1	1	1	1	
000026	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	
000027	1	0	0	0	1	1	0	1	0	0	1	0	1	1	0	0	
000030	0	1	0	0	1	1	1	1	1	0	0	0	1	0	0	0	
000031	1	0	0	0	1	1	1	1	1	0	1	0	0	1	0	1	
000032	1	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	
000033	1	0	0	0	1	1	0	1	0	0	1	0	1	1	0	0	
000034	0	1	0	0	1	1	1	1	1	0	0	0	1	0	0	0	
000035	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	
000036	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1	
000037	0	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	
000040	0	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	
000041	0	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	
000042	0	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1	
000043	1	1	0	0	1	1	1	0	0	1	0	0	1	1	1	1	
000044	0	0	0	0	1	1	0	1	0	0	1	0	1	1	0	0	
000045	0	1	0	0	1	1	1	0	1	1	1	1	1	1	1	1	
000046	0	1	0	0	0	1	1	0	1	1	1	1	1	1	1	1	
000047	0	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	
000050	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	
000051	1	1	0	0	1	0	1	1	1	1	1	1	1	1	0	0	
000052	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	
000053	0	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1	
000054	0	1	0	0	1	1	1	1	1	0	0	0	1	0	0	0	
000055	0	1	0	0	1	1	1	1	1	0	0	0	1	0	0	0	
000056	0	1	0	0	0	0	1	0	1	1	1	1	1	1	1	1	
000057	1	1	0	0	1	1	1	0	0	1	0	0	1	1	1	1	
000060	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	
000061	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	
000062	0	1	0	0	1	1	0	1	1	1	1	1	0	0	1	0	
000063	1	1	0	0	1	1	1	0	0	1	0	0	1	1	1	1	
000064	1	1	0	0	1	1	0	1	1	1	1	1	0	0	1	0	
000065	0	0	0	0	1	1	0	1	0	0	1	0	1	1	0	0	
000066	1	1	0	0	1	1	0	1	1	1	1	1	0	0	1	0	
000067	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1	
000070	1	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	
000071	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1	
000072	0	1	0	0	1	1	1	1	1	0	0	0	1	0	0	0	

	** ROA 886				** ROM 00560				** ROM 00559				** ROA 885			
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12
000073	0	0	1	0	1	1	0	0	0	0	1	0	1	1	0	0
000074	0	1	0	1	0	1	1	0	1	0	0	0	1	1	1	1
000075	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
000076	1	1	0	0	0	0	1	0	1	1	1	1	1	1	1	1
000077	1	1	0	0	1	1	1	1	1	1	1	1	1	1	0	1
000100	0	1	0	0	1	1	1	1	1	0	0	0	1	0	0	0
000101	0	0	1	0	0	1	1	0	1	0	1	0	1	1	1	1
000102	0	0	1	0	1	1	0	0	1	1	1	1	1	1	1	1
000103	0	0	1	0	1	1	0	0	0	0	1	0	1	1	0	0
000104	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000105	0	1	0	0	1	1	1	1	1	0	0	0	1	0	0	0
000106	1	1	0	0	1	0	0	1	1	1	1	1	1	1	0	1
000107	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1
000110	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000111	0	0	1	0	0	1	1	1	0	1	0	0	1	1	1	1
000112	0	0	1	1	0	0	0	0	1	1	1	1	1	1	1	1
000113	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1
000114	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1
000115	0	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1
000116	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1
000117	0	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1
000120	1	0	1	0	1	1	0	1	1	1	1	1	1	1	0	1
000121	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1
000122	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
000123	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1
000124	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1
000125	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0
000126	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1
000127	0	1	0	1	0	1	1	0	1	0	0	0	1	1	1	1
000130	0	1	0	1	0	1	1	0	1	0	0	0	1	1	1	1
000131	1	0	1	0	1	0	0	1	1	1	1	1	1	1	1	1
000132	1	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1
000133	1	0	1	0	1	1	0	0	1	1	1	1	1	1	1	1
000134	0	1	1	0	1	1	0	0	1	0	0	0	1	0	0	0
000135	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1
000136	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
000137	1	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1
000140	0	1	1	0	1	1	0	0	1	0	0	0	1	0	0	0
000141	0	1	1	0	1	1	0	0	1	0	0	0	1	0	0	0
000142	0	1	1	0	1	1	1	0	1	1	1	1	0	1	0	0
000143	1	0	1	0	0	1	0	0	0	1	0	0	1	1	1	1
000144	1	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1
000145	0	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1
000146	0	1	1	0	0	0	1	0	1	1	1	1	1	1	1	1
000147	0	1	1	0	1	0	0	1	1	1	1	1	0	1	0	1
000150	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0
000151	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1
000152	0	1	1	0	1	1	0	1	1	1	1	1	1	1	0	1
000153	0	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
000154	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1
000155	0	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
000156	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1
000157	1	1	1	0	1	0	0	0	1	1	1	1	0	1	0	1
000160	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0
000161	1	1	1	0	1	1	0	0	1	1	1	1	1	1	1	1
000162	1	1	1	0	1	1	0	0	1	1	1	1	1	1	0	1
000163	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0
000164	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1
000165	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0

	** ROA 886				** ROM 00560				** ROM 00559				** ROA 885				**
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12	
000166	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	
000167	1	1	1	0	1	0	0	1	1	1	1	1	0	1	0	1	
000170	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	
000171	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	
000172	1	1	1	0	1	1	0	1	1	1	1	1	1	1	0	1	
000173	1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	
000174	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	
000175	1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	
000176	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	
000177	0	1	1	0	1	1	0	0	1	0	0	0	1	0	0	0	
000200	0	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	
000201	0	0	0	1	1	1	0	0	1	1	1	1	1	1	1	1	
000202	0	0	0	1	0	1	0	0	1	1	1	1	1	1	1	1	
000203	0	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	
000204	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
000205	0	0	0	1	1	1	1	1	0	1	1	0	0	1	1	0	
000206	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	
000207	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1	
000210	1	0	0	1	1	1	1	0	1	0	0	0	1	0	0	0	
000211	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	
000212	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
000213	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1	
000214	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
000215	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
000216	1	0	0	1	1	0	0	0	1	1	1	1	1	1	0	0	
000217	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
000220	0	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	
000221	1	0	0	1	1	1	0	0	1	1	1	1	1	1	1	1	
000222	1	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1	
000223	1	0	0	1	0	1	0	0	1	1	1	1	1	1	1	1	
000224	1	0	0	1	1	1	1	0	1	0	0	0	1	0	0	0	
000225	1	0	0	1	1	1	1	0	1	0	0	0	1	0	0	0	
000226	1	0	0	1	1	1	0	1	1	1	1	1	0	1	0	0	
000227	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	
000230	0	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1	
000231	1	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	
000232	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	
000233	1	0	0	1	1	1	1	1	1	0	0	0	1	0	0	0	
000234	1	0	0	1	1	1	1	1	1	0	0	0	1	0	0	0	
000235	1	0	0	1	1	1	1	1	1	0	0	0	1	0	0	0	
000236	0	1	0	1	1	0	0	0	1	1	1	1	0	1	0	1	
000237	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	
000240	0	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1	
000241	0	1	0	1	0	1	1	0	1	0	0	0	1	1	1	1	
000242	0	1	0	1	1	1	0	0	1	1	1	1	0	1	0	0	
000243	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1	
000244	1	1	0	1	1	1	1	1	1	0	0	1	1	0	0	1	
000245	0	1	0	1	0	1	1	0	1	0	0	0	1	1	1	1	
000246	1	1	0	1	1	1	1	0	1	0	0	1	1	0	0	1	
000247	1	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1	
000250	0	1	0	1	1	1	0	1	1	0	0	0	1	0	0	0	
000251	0	1	0	1	1	1	0	1	1	0	0	0	1	0	0	0	
000252	1	1	0	1	1	1	0	0	1	1	1	1	0	1	0	0	
000253	0	0	1	0	1	1	1	1	0	1	0	0	1	1	1	1	
000254	0	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	
000255	1	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1	
000256	1	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1	
000257	0	1	0	1	1	1	1	0	0	0	0	1	1	1	1	1	
000260	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1	

	** ROA 886				** ROM 00560				** ROM 00559				** ROA 885			
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12
000261	0	1	0	1	1	1	1	1	1	0	1	1	1	0	1	1
000262	1	1	0	1	0	0	0	0	1	1	1	1	1	1	1	1
000263	0	1	0	1	1	1	0	1	1	0	0	0	1	0	0	0
000264	1	1	0	1	1	1	0	1	1	1	1	1	0	1	0	1
000265	0	1	0	1	0	1	1	0	1	0	0	0	1	1	1	1
000266	1	1	0	1	1	0	0	1	1	1	1	1	0	1	0	1
000267	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1
000270	0	1	0	1	0	1	1	0	1	0	0	0	1	1	1	1
000271	1	0	1	0	1	1	0	0	1	1	0	1	1	1	1	1
000272	0	1	0	1	0	1	1	0	1	0	0	0	1	1	1	1
000273	0	0	0	0	1	1	0	0	1	0	1	0	1	0	1	0
000274	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1
000275	0	0	1	0	1	0	0	1	1	1	1	1	0	0	0	1
000276	0	1	0	1	0	1	1	0	1	0	0	0	1	1	1	1
000277	1	1	1	1	0	0	1	0	1	1	1	1	1	1	1	1
000300	0	1	0	1	0	1	1	0	1	0	0	0	1	1	1	1
000301	0	0	1	1	1	1	0	0	1	1	1	1	1	1	1	1
000302	0	0	1	1	0	1	0	0	1	1	1	1	1	1	1	1
000303	0	0	1	1	1	0	0	0	1	1	1	1	1	1	1	1
000304	1	0	1	1	1	1	1	1	1	0	1	1	1	0	1	1
000305	1	0	1	1	1	1	1	0	1	0	0	0	1	0	0	0
000306	0	1	0	1	0	1	1	0	1	0	0	0	1	1	1	1
000307	0	0	1	1	0	1	0	1	1	1	1	0	1	1	1	1
000310	0	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1
000311	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000312	0	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1
000313	0	0	1	1	1	1	1	1	1	0	0	0	1	0	0	0
000314	0	0	1	1	1	1	1	1	1	0	0	0	1	0	0	0
000315	0	0	1	1	1	1	1	1	1	0	0	0	1	0	0	0
000316	1	0	1	1	1	1	0	0	1	1	1	1	0	1	0	0
000317	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1
000320	0	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1
000321	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000322	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1	1
000323	0	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1
000324	1	0	1	1	1	1	1	0	1	0	0	0	1	0	0	0
000325	1	0	1	1	1	1	1	0	1	0	0	0	1	0	0	0
000326	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1
000327	1	0	1	1	1	1	0	1	0	1	0	0	1	1	1	1
000330	1	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1
000331	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000332	1	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1
000333	0	0	1	1	1	1	0	1	1	1	1	0	1	1	1	1
000334	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000335	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000336	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000337	1	0	1	1	1	0	0	0	1	1	1	1	1	0	0	0
000340	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000341	0	1	1	1	1	1	1	0	1	0	0	0	1	0	0	0
000342	0	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1
000343	0	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1
000344	0	1	1	1	1	1	1	0	1	0	0	0	1	0	0	0
000345	0	1	1	1	1	1	1	0	1	0	0	0	1	0	0	0
000346	0	1	1	1	1	1	0	1	1	1	1	1	0	1	0	0
000347	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1
000350	0	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1
000351	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0
000352	0	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1
000353	1	1	1	1	1	1	0	0	1	0	0	0	1	0	0	0

	** ROA 886				** ROM 00560				** ROM 00559				** ROA 885				**
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12	
000354	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	
000355	0	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	
000356	0	1	1	1	1	0	0	1	1	1	1	1	0	1	0	0	
000357	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	
000360	1	1	1	1	1	1	0	0	1	0	0	0	1	0	0	0	
000361	1	1	1	1	1	1	0	0	1	0	0	0	1	0	0	0	
000362	0	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1	
000363	1	1	1	1	1	1	1	0	0	1	0	0	1	1	1	1	
000364	0	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1	
000365	0	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1	
000366	0	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1	
000367	1	1	1	1	1	1	0	1	0	1	1	0	1	1	0	0	
000370	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	
000371	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
000372	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	
000373	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	
000374	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	
000375	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
000376	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
000377	0	0	0	1	1	0	0	0	1	1	1	1	1	1	1	0	

	** ROA 884				** ROA 883				** ROM 00555				** ROM 00554			
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12
000000	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000001	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000002	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000003	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1
000004	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0
000005	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000006	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000007	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
000010	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0
000011	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000012	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000013	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000014	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000015	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000016	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000017	0	0	1	1	1	0	0	1	1	1	1	1	1	1	1	1
000020	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0
000021	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000022	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000023	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000024	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000025	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000026	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000027	0	1	0	1	1	0	0	1	1	1	1	1	1	1	1	1
000030	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0
000031	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000032	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000033	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000034	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000035	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000036	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000037	1	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1
000040	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000041	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000042	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
000043	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000044	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
000045	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
000046	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000047	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000050	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0
000051	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000052	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
000053	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
000054	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000055	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000056	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
000057	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000060	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000061	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000062	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000063	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000064	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	0
000065	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1
000066	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
000067	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000070	1	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0
000071	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000072	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	** ROA 884 **				ROA 883 **				ROM 00555 **				ROM 00554 **			
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12
000073	1	1	1	1	1	0	0	1	1	0	0	0	0	0	0	0
000074	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000075	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000076	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0
000077	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000100	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0
000101	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000102	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000103	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000104	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000105	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000106	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000107	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000110	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000111	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000112	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000113	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000114	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	0
000115	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	0
000116	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
000117	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
000120	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000121	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	0
000122	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000123	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
000124	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000125	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000126	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000127	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000130	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000131	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000132	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000133	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0
000134	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
000135	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000136	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000137	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000140	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000141	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000142	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000143	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
000144	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1
000145	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
000146	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
000147	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000150	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1
000151	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000152	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000153	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1
000154	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000155	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000156	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000157	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000160	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1
000161	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000162	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000163	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1
000164	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000165	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	** ROA 884				** ROA 883				** ROM 00555				** ROM 00554			
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12
000166	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000167	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000170	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1
000171	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000172	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000173	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1
000174	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
000175	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000176	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000177	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000200	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000201	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000202	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000203	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000204	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000205	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000206	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000207	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
000210	1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	1
000211	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000212	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
000213	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
000214	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
000215	1	1	1	0	0	1	1	0	1	1	1	1	1	1	1	1
000216	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000217	1	1	1	0	0	1	1	0	1	1	1	1	1	1	1	1
000220	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000221	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000222	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0
000223	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000224	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000225	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000226	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000227	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
000230	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1
000231	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000232	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
000233	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
000234	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000235	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000236	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000237	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
000240	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1
000241	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000242	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000243	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000244	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000245	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000246	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000247	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000250	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000251	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000252	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000253	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
000254	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000255	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000256	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000257	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000260	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1

	** ROA 884				** ROA 883				** ROM 00555				** ROM 00554			
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12
000261	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000262	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
000263	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
000264	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000265	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000266	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000267	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000270	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000271	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000272	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000273	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000274	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000275	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000276	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000277	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
000300	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000301	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000302	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000304	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000305	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
000306	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000307	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000310	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000311	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
000312	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000313	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
000314	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000315	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000316	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000317	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0
000320	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1
000321	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
000322	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
000323	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000324	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000325	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000326	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
000327	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0
000330	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	0
000331	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000332	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
000333	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000334	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
000335	1	1	1	1	0	0	1	1	0	0	1	1	1	0	1	0
000336	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
000337	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000340	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000341	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
000342	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
000343	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
000344	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000345	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000346	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000347	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
000350	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1
000351	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
000352	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1
000353	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1

	** ROA 884				** ROA 883				** ROM 00555				** ROM 00554			
	09	10	11	12	09	10	11	12	09	10	11	12	09	10	11	12
000354	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000355	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000356	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000357	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
000360	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000361	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000362	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000363	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000364	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	0
000365	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
000366	1	1	1	1	1	1	1	1	0	0	0	0	0	1	0	0
000367	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000370	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	0
000371	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
000372	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000373	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000374	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1
000375	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
000376	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
000377	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

KC doc V8 140

A/S REGNECENTRALEN	Designed by VH 25/11-75	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.

Unit FPA 801
Dwg. No. A10836

TRANSMITTER JACK

J1

J1
ELCO MINIVARILOCK, RECEPTACLE, TYPE 8026-075, CODE 1-1

PIN.	GEN. ADR	SIGNAL NAME	
A 1		DATA LINE 0 OUT	A
A 2		" 0 "	B
A 3		" 1 "	A
A 4		" 1 "	B
A 5		" 2 "	A
A 6		" 2 "	B
A 7		" 3 "	A
B 7		" 3 "	B
B 6		" 4 "	A
B 5		" 4 "	B
B 4		" 5 "	A
B 3		" 5 "	B
B 2		" 6 "	A
B 1		" 6 "	B
C 1		" 7 "	A
C 2		" 7 "	B
C 3		PARITY LINE OUT	A
C 4		"	B
C 5		RESET LINE OUT	A
C 6		"	B
C 7		REQ ACK LINE IN	A
D 7		"	B
D 6		DATA REQ LINE OUT	A
D 5		"	B
D 4		STATUS REQ LINE OUT	A
D 3		"	B
D 2		AUTOLOAD LINE OUT	A
F 1		"	B
E 2		CONN. LINE OUT	A
E 3		"	B
E 5		LAST CHAR. LINE OUT	A
E 6		"	B
E 4			
F 7			
E 6			
F 2			
F 1			
H 1			
J 1			
J 2			
J 6			
J 7			
K 7			
K 6		0 VOLT	
K 5		"	
K 3			

J1
ELCO. MINIVARILOCK, RECEPTACLE, TYPE 8026-075, CODE 1-1

PIN	GEN. ADR	SIGNAL NAME
K 2		
K 1		
L 2		
L 3		
L 4		
L 5		
L 6		
L 7		
M 7		
M 6		
M 5		
M 4		
M 3		
M 2		
M 1		
N 1		
N 2		
N 3		
N 4		
N 5		
N 6		
N 7		
P 7		
P 6		
P 5		
P 4		
P 3		
P 2		SHIELD
P 1		SHIELD

ACF 1975

J2

ELCO MINIVABILOCK, RECEPTACLE, TYPE 8026-033, CODE 1-2

PIN	GEN. ADDR.	SIGNAL NAME
A2		REMOTE AUTOLOAD
A3		0V
A4		
A5		
A6		
A7		
B1		
B2		
B3		
B5		
B6		
B7		
C1		
C2		
C6		
C7		
D1		
F1		
E2		
E6		
E7		
F1		
F2		
F3		
F5		
F6		
F7		
H2		
H3		
H4		
H5		
H6		
H7		

75 VH.

21/10-

JACK for AUTOLOAD SIGNAL

A-7??

RC doc. VS 140

A/S REGNECENTRALEN	Designed by VH	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.
	25/11-75						

Unit: FPA 801
Dwg. No.: A12887

RECEIVER JACK

J3

J3

ELCO MINIVARILOCK, RECEPTACLE, TYPE 8026-075, CODE 1 -3

PIN.	GEN. ADR	SIGNAL NAME	
A 1		DATA LINE 0 IN	A
A 2		— 0 —	B
A 3		— 1 —	A
A 4		— 1 —	B
A 5		— 2 —	A
A 6		— 2 —	B
A 7		— 3 —	A
B 7		— 3 —	B
B 6		— 4 —	A
B 5		— 4 —	B
B 4		— 5 —	A
B 3		— 5 —	B
B 2		— 6 —	A
B 1		— 6 —	B
C 1		— 7 —	A
C 2		— 7 —	B
C 3		PARITY LINE IN	A
C 4		—	B
C 5		RESET LINE IN	A
C 6		—	B
C 7		REQ ACK LINE OUT	A
D 7		—	B
D 6		DATA REQ LINE IN	A
D 5		—	B
D 4		STATUS REQ LINE IN	A
D 3		—	B
D 2		AUTOLOAD LINE IN	A
E 1		—	B
E 2		CONN. LINE IN	A
E 3		—	B
E 5		LAST CHAR LINE IN	A
E 6		—	B
E 7			
F 7			
F 6			
F 2			
F 1			
H 1			
J 1			
J 2			
J 6			
J 7			
K 7			
K 6		0 VOLT	
K 5		—	
K 3			

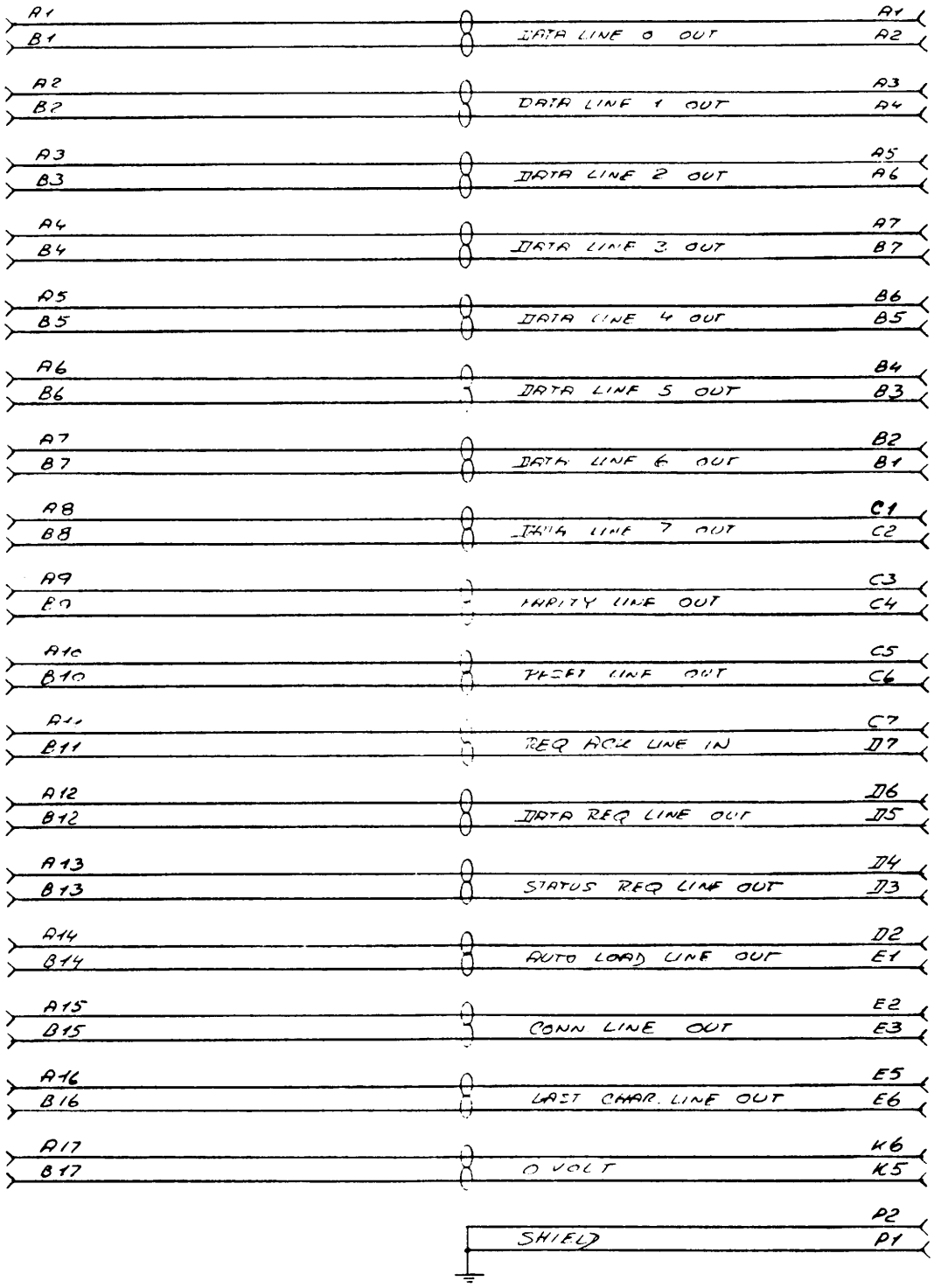
J

ELCO, MINIVARILOCK, RECEPTACLE, TYPE 8026-075, CODE -

PIN	GEN. ADR	SIGNAL NAME
K 2		
K 1		
L 2		
L 3		
L 4		
L 5		
L 6		
L 7		
M 7		
M 6		
M 5		
M 4		
M 3		
M 2		
M 1		
N 1		
N 2		
N 3		
N 4		
N 5		
N 6		
N 7		
P 7		
P 6		
P 5		
P 4		
P 3		
P 2		SHIELD
P 1		SHIELD

J1004

J 1 , code 1-1
FLCO MINIVARILOCK
RECEPTACLE
TYPE 8026-075



Designed by VH 20/10 - 75	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.	

A/S REGNECENTRALEN

Unit: FPA 801
Dwg. No.: A12888

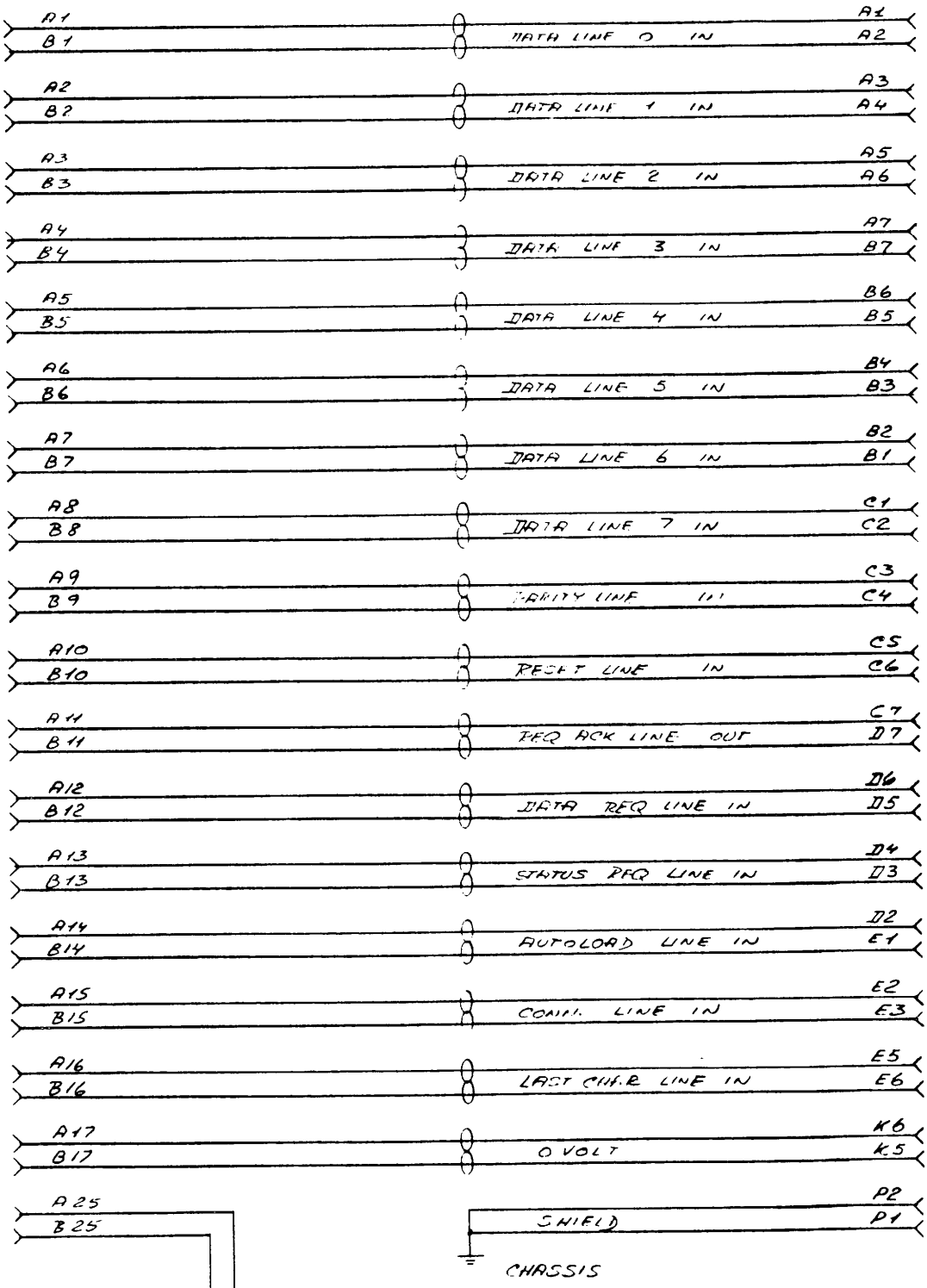
TRANSMITTER - MELLEMKABEL
CBL A13

AC doc VB 140

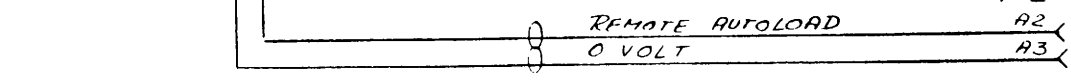
AGF 1973

J 1005

J 3 , CODE 1-3
ELCO MINIVARILOCK
RECEPTACLE
TYPE 8026-075



J 2 , code 1-2
ELCO MINIVARILOCK
RECEPTACLE
TYPE 8026-033



Designed by VH 20/10-75	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.			

A/S REGNECENTRALEN

Unit FPA 801

Dwg. No. A 112887

RECEIVER - MELLEMKABEL.
CPL ø 1:1

RC doc V8 140

AGF 1973

RC doc. VB 140

A/S REGNECENTRALEN	Designed by VH 25/11-75	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.

Unit FPA 801
Dwg. No. A12880

CBL 817

Cable type: Std. Parsnoet 24 par m. skærm NEK

I = Interconnection, T = Twisted pairs. Length of cable: max 20 m.

Cable between FPA 801 - FPA 100/702

P1 ELCO MINI VARILOCK, RECEPTACLE, TYPE 8026-075, CODE -
P2 CANNON DB 52 P

P1 PIN	I	T	GEN. ADDR.	SIGNAL NAME	I	P2 PIN
A1		8		hvid/grå		1
A2		8				2
A3		8		hvid/sort		3
A4		8				4
A5		8		grå/blå		5
A6		8				6
A7		8		hvid/orange		7
B7		8				8
B6		8		grøn/orange		9
B5		8				10
B4		8		brun/orange		11
B3		8				12
B2		8		grå/orange		13
B1		8				14
C1		8		grøn/hvid		15
C2		8				16
C3		8		grøn/brun		17
C4		8				35
C5		8		grå/grøn		34
C6		8				33
C7		8		hvid/brun		32
D7		8				31
D6		8		grå/brun		30
D5		8				29
D4		8		sort/brun		28
D3		8				27
D2		8		grå/sort		26
E1		8				25
E2		8		blå/hvid		24
E3		8				23
E5		8		blå/orange		22
E6		8				21
E7		8		blå/grøn		37
F7		8				38
F6						
F2		8		blå/brun		39
F1		8				40
H1		8		sort/grøn		41
J1						42
J2						
J6						
J7						
K7						
K6				sort/blå		20
K5				sort/orange		19
K3						

P1 ELCO MINIVARILOCK, RECEPTACLE, TYPE 8026-075, CODE -
P2 CANNON DB 52 A

P PIN	I	T	GEN. ADDR.	SIGNAL NAME	I	P2 PIN
K2						
K1						
L2						
L3						
L4						
L5						
L6						
L7						
M7						
M6						
M5						
M4						
M3						
N2						
M1						
N1						
N2						
N3						
N4						
N5						
N6						
N7						
P7						
P6						
P5						
P4						
P3						
P2				Shield		51
P1				Shield		52

RETURN LETTER

Title: Technical Manual for FPA803 Front-end Processor Adapter

RCSL No.: 99 0 00805.

A/S Regnecentralen af 1979/RC Computer A/S maintains a continual effort to improve the quality and usefulness of its publications. To do this effectively we need user feedback, your critical evaluation of this manual.

Please comment on this manual's completeness, accuracy, organization, usability, and readability:

Do you find errors in this manual? If so, specify by page.

How can this manual be improved?

Other comments?

Name: _____ Title: _____

Company: _____

Address: _____

Date: _____

Thank you

42-i 1288

. . . . . Fold here . . . . . .

. . . . . Do not tear - Fold here and staple . . . . . .

Affix
postage
here

REGNECENTRALEN
af 1979
Information Department
Lautrupbjerg 1
DK-2750 Ballerup
Denmark

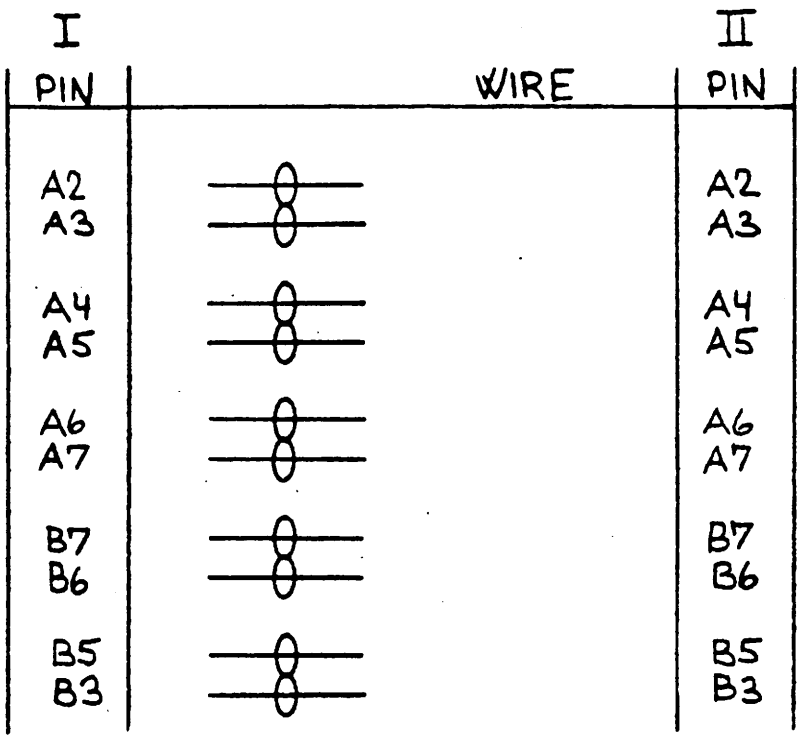
CONNECTOR I: ELCO PLUG 8026-033-000-725

CONNECTOR II: ELCO PLUG 8026-033-000-725

CABLE : 5 x 2 x 0,25 mm^2

LENGTH : 150 cm

HC



2.10.75

R 2124

CBL 803

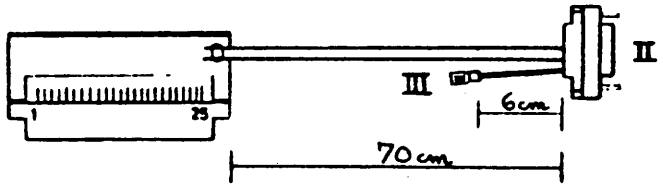
CONNECTOR I : ELCO KANTSTIK 2×25 POL LODDE

CONNECTOR II : ELCO RECEPT 8026-075-000-801

CONNECTOR III : SPADESKO 6,3mm, FORTIN., RØD

CABLE : 18 × 2 × 0,14 mm^2

HC



I	WIRE	II
A1 B1		A1 A2
A2 B2		A3 A4
A3 B3		A5 A6
A4 B4		A7 B7
A5 B5		B6 B5
A6 B6		B4 B3
A7 B7		B2 B1
A8 B8		C1 C2
A9 B9		C3 C4
A10 B10		C5 C6
A11 B11		C7 D7
A12 B12		D6 D5
A13 B13		D4 D3
A14 B14		D2 E1
A15 B15		E2 E3
A16 B16		E5 E6
A17 B17		K6 K5
III		P2 P1

BEMÆRK:

OPSPÆNDINGSPLADE CHS 801-19

PÅSKRUES ELCO RECEPT, INDEN TRÅDNING AF STIK.

11.2.76

6.4.76

CBL 813

R 21215

CONNECTOR I : ELCO KANTSTIK 2x25 POL. LODDE

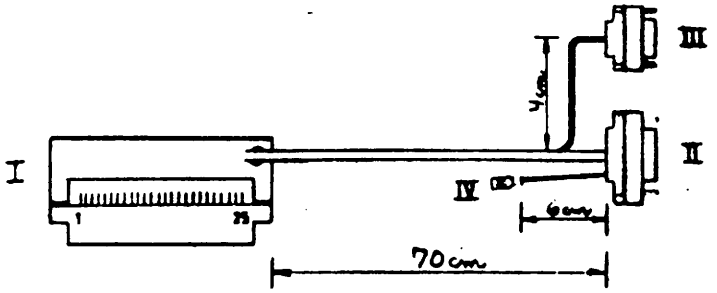
CONNECTOR II : ELCO RECEPT 8026-075-000-801

CONNECTOR III : ELCO RECEPT 8026-033-000-801

CONNECTOR IV : SPADESKO 6,3mm, FORTIN. RØD.

CABLE : 19 × 2 × 0,14 mm²

HC



I	WIRE	II
A1 B1		A1 A2
A2 B2		A3 A4
A3 B3		A5 A6
A4 B4		A7 B7
A5 B5		B6 B5
A6 B6		B4 B3
A7 B7		B2 B1
A8 B8		C1 C2
A9 B9		C3 C4
A10 B10		C5 C6
A11 B11		C7 D7
A12 B12		D6 D5
A13 B13		D4 D3
A14 B14		D2 E1
A15 B15		E2 E3
A16 B16		E5 E6
A17 B17		K6 K5
A25 B25		P2 P1

II	WIRE	IV
A? A3		IV

BEMÆRK:
OPSPÆNDINGSPLADE CHS 801-20
PÅSKRUES ELCO RECEPT INDEN
TRÅDNING AF STIK.

11.2.76
6.4.76

CBL 814

R 21216

I PIN	WIRE	II PIN
A1	HVID	1
A2	GRÅ	2
A3	HVID	3
A4	SORT	4
A5	GRÅ	5
A6	BLÅ	6
A7	HVID	7
B7	ORANGE	8
B6	GRØN	9
B5	ORANGE	10
B4	BRUN	11
B3	ORANGE	12
B2	GRÅ	13
B1	ORANGE	14
C1	GRØN	15
C2	HVID	16
C3	GRØN	17
C4	BRUN	35
C5	GRÅ	34
C6	GRØN	33
C7	HVID	32
D7	BRUN	31
D6	GRÅ	30
D5	BRUN	29
D4	SORT	28
D3	BRUN	27
D2	GRÅ	26
E1	SORT	25
E2	BLÅ	24
E3	HVID	23
E5	BLÅ	22
E6	ORANGE	21
E7	BLÅ	37
F7	GRØN	38
F2	BLÅ	39
F1	BRUN	40
H1	SORT	41
J1	GRØN	42
K6	SORT/BLÅ	20
K5	SORT/ORANGE	19
P2	SHIELD	51
P1	SHIELD	52

CONNECTOR I: ELCO PLUG 8026-075-000-701

CONNECTOR II: CANNON DE 52 P

CABLE TYPE : PARSNOET 21 x 2 x 0,14 mm² M SHIELD

LENGTH : 5m.

CBL 817

Hc

11.2.76
29.3.76

R 21217