RC 4000 GENERAL TECHNICAL DESCRIPTION

CENTRAL PROCESSOR

Chapter 6. INPUT/OUTPUT SYSTEM.

RCdoc: VB217 June 1968/MSP
pp. 6-1:6-16

Chapter 6

I N P U T / O U T P U T S Y S T E M

6.1. GENERAL.

[Figures 6.1-1, 6.3-2]

RC 4000 has, in principle, two data channels, a Low Speed Data Channel (LDC) and a High Speed Data Channel (HDC). Each of these data channels is shared among several input/output units.

Sharing of a data channel among several devices requires that each device has a separate buffer register, which transmits or receives one character at a time to or from the external data medium.

Data transfer via HDC take place in blocks. Data are transferred directly to or from the internal core store on a cycle-stealing basis. The block transfer is not under program control, i.e. program execution proceeds simultaneously with the HDC input/output operations. Specification and initiation of the block transfer are performed via the LDC; therefore all devices, which are connected to the HDC, are also connected to the LDC.

The data transfer via LDC is performed character by character under microprogram control. The LDC communicates directly with the internal working registers. Transmission of data via LDC is mainly used in connection with slow character-oriented devices such as typewriters, paper tape readers, and paper tape punches.

All input/output operations via LDC can be handled by a single program instruction, INPUT/OUTPUT (IO), which has the standard instruction format. The effective address of the instruction indicates the device address (18 bits) and the device command (6 bits). A data word (max. 24 bits) is transferred to or from the specified working register (W-register).

The program instruction, AUTOLOAD WORD (AW), controls a series of 4 input operations via LDC. This instruction reads four 6-bit characters, and is used for initial program loading from the paper tape reader.

The IO instruction and the AW instruction are described in the RC 4000 REFERENCE MANUAL. Figure 6.1-1 shows in schematic form the structure of the

RC 4000 Low Speed Data Channel (LDC). The LDC is based upon an Input/Output Controller (IOC) and an input/output ring bus system. A single ring busline is shown on Figure 6.3-2 in a schematic form. The busline system has 24 bits for transfer of data to or from the device buffers and 8 bits for transfer of channel control signals. The transfers of data between the working registers and the device buffers take place one at a time under program control. Transfers between buffer registers and the external data media are, however, controlled independently by the device controllers; thus several of these transfers can take place simultaneously.

The electronics belonging to different devices may be placed in separate cabinets. In each cabinets where one or more devices have to be connected to the data channel, the Low Speed Bus Interface (LBI) is inserted in the ring bus system. The installation described below has 3 of these LBI's called BLR, BLS, and BLT.

Some Device Controllers can be connected directly to the LBI, whereas others require that a Device Interface is inserted between the LBI and the Device Controller.

The following sections, which cover the LDC, describe the IOC and the LBI. A description of the HDC that is included in the manuals for the RC 4000 system configurations that are equipped with the HDC.

6.2. INTRODUCTION TO THE LDC.

As mentioned the Low Speed Data Channel (LDC) is based upon a ring bus system with 32 buslines. The buslines can be sensed by the CPU and all peripheral devices connected to the system. The buslines are equipped with gates to make it possible to control the buslines from any peripheral device or the CPU.

8 of the 32 buslines are used for channel control signals. Some of these are used for defining what type of information the 24 data buslines are transferring in a specific time interval. The possible types of information on the data buslines are Device Address, Device Command, and Data Word, the latter as input or output information.

The input/output operation, which is controlled by the microprogram belonging to the IO instruction, can briefly be described as follows. The input/output operation can be divided into a Selection Phase and a Data Phase. In the Selection Phase the Device Address and the Device Command

are available for all devices on the 24 data buslines. The addressed device responds to these by sending its Ready and Connected status bits via 2 of the channel control buslines. These bits are transferred to the Exception Register (EX(22:23)). If they indicate that the device is free, i.e. connected and ready, one of the channel control signals selects the device. If not the input/output operation is rejected and the computer proceeds immediately to the next instruction. If selection takes place, the device will accept the device command code from the buslines.

In the Data Phase a Data Word (max. 24 bits) is transferred from the specified W-register to the selected device or vice versa. The direction depends on the device command type. The device command is given by 6 bits, 2 of which specify the 4 types, Sense, Control, Read, and Write. The Sense command gives rise to transfer of a Data Word from the selected device to the selected W-register. The Write and Control commands imply transfer from the W-register to the selected device. The Read command does not involve any data transfer. When the Data Phase is terminated, the device is left to its own control. As long as the initiated operation is in progress, the device must generate a busy signal.

The specific function of the 32 buslines and the timing of these are described in Section 6.4. in connection with the Low Speed Bus Interface Units. The effect of different device commands is stated in the section for the device in question as well as the data format and status word signification. In Section 6.3. follows a description of the Input/Output Controller, which includes the electronics linking the central processor and the input/output ring bus system.

6.3. INPUT/OUTPUT CONTROLLER.

6.3.1. Introduction.

[Figure 6.3-1]

It has been mentioned that the IOC is a link between the central processor and the ring bus system of the LDC. Beyond this, IOC links to some extent the Interrupt Unit (ITR) to the central processor. Figure 6.3-1 shows the contents of IOC and the connections to the central processor and the external ring busline system.

As it can be seen on Figure 6.3-1, the information to be transmitted via IOC must be placed in the SB register. During the selection phase of the IO instruction we have the device address and the device command placed in SB(0:17) and SB(18:23), respectively. During the data phase of an output operation, we have the data word in SB.

6.3.2. Device Address and Device Command.

[IOC - 10,11,13]

In the selection phase the contents of the SB register are as follows:

SB(12:17) specifies the device address
SB(18:23) specifies the device command.

The bits 0 through 11 of the effective address (SB(0:11)) are neglected in the actual installation, but can be used for a later extension of the device address field.

SB(12:13) specifies 1 out of 4 device groups. The computer can be equipped with one or more of these groups. To each group belongs a group selection circuit and a ring bus system. SB(14:17) specifies then a device in a group. The 4 bits pass a decoding network which as output has the device address in 1 out of 16 code. The device address (Device Address (0:15)) is transferred to all the peripheral devices on the buslines IOC BUS(0:15).

The device command code of 6 bits is divided into a basic command field of 2 bits and a modifier field of 4 bits:

SB(22:23): Basic command field
SB(18:21): Modifier field.

The 16 possible modifications are specific for each type of devices. In the microprogram, controlling the input/output operations, only the following 4 basic commands are recognized:

SB(22,23) = b00 Sense
SB(22,23) = b01 Control
SB(22,23) = b10 Read
SB(22,23) = b11 Write

The device commands, Sense, Control, and Read have different microprograms. The microprogram of the Write command is identical with that of the Control command. A description of the microprograms can be found in Chapter 8. The command code is transferred to all external devices in the Selection Phase via the ring buslines IOC BUS(18:23).

6.3.3. Output Multiplexer.

[IOC - 02,03,10,11,14:17]

During execution of the IO or AW instructions 3 categories of information can be transmitted to the outgoing buslines IOC BUS(0:23) via the output multiplexer circuits. The device address and the device command are transmitted during the selection phase. The corresponding multiplexer gate signal is the IO Selection Signal. A data word or a parameter word is transmitted during the Data Phase according as the device command is a Write or a Control command. A parameter word is for example an analog multiplexer address. The multiplexer gate signal for this information is IO Data Transfer Signal.

During the Data Phase in a Sense command, all outgoing buslines are set to 1.

6.3.4. Input Multiplexer.

[IOC - 04:09]

The Input Multiplexer can be considered as an extension of the internal busline system of the central processor. It can accept up to 4 sets of inputs. 3 of these are reserved for the Interrupt Register, IR, the Interrupt Mask Register, IM, and the Data Word, IO data. The input multiplexer gate signals are:

GiBUSfIR $\vee$ ManGiBUSfIR
GiBUSfIM $\vee$ ManGiBUSfIM
GiBUSfIOdata.

6.3.5. Connected/Ready Status.

[IOC - 12,21]

The addressed device must response to the IO Selection signal by sending 2 status bits indicating if the device is connected and if it is ready for starting the next operation. The device is connected if it is able to give an acceptable response to the input/output instructions. The received status bits, IO Connected and IO Ready, are transferred to the Exception register:

EX(22):= -,IO Connected
EX(23):= -,IO Ready $\wedge$ IO Connected.

The microprogram for the IO or AW instructions is interrupted if it detects that IO Connected ∧ IO Ready = 0. After the interruption the computer proceeds immediately to the next instruction.

6.3.6. Control and Timing Circuits.

[IOC - 01,10,12,13]

The register element Output Operation is used for storing information about the direction of the data transfer. Output Operation = 1 if the latest input/output instruction was a Control or a Write command. In the Data Phase, SB or a logical 1 is gated to the outgoing buslines IOC BUS determined by the output operation.

The register element Group(0) is set to 1 if the device address is less than 16. The channel control buslines IO Enable, IO Selection, and IO Data Transfer are inactive when Group(0) = 0.

The delay circuits in connection with IO Data Transfer, GiIOCBUSfSB, and IO Selection Signal ensure that the data on IOC BUS[0:23] are really valid when the channel control signals advertise them.

6.3.7. Cable Connections to LBI.

[IOC - 26]
[Figure 6.3-2]

Figure 6.3-2 shows the cable connections between IOC and the LBI. 4 standard signal cables connect the units to one another. The LBI have 4 I-connectors and 4 O-connectors. The succession in which the LBI are connected to one another is arbitrary. The O-connectors of the last LBI have to be equipped with Termination Plugs in which the ring-busline are closed. In the actual system we have 3 LBI, BLR, BLS, and BLT. The connectors are identified with numbers as the following table indicates:

Connector Identification:

	IOC	BLR		BLS		BLT	
		I	O	I	O	I	O
a	1021	1601	1602	1301	1302	1201	1202
b	1022	1603	1604	1303	1304	1203	1204
c	1023	1605	1606	1305	1306	1205	1206
d	1024	1607	1608	1316	1308	1207	1208

6.4. LOW SPEED BUS INTERFACE UNITS, BLR, BLS, AND BLT.

6.4.1. Introduction.

The connection of I/O devices to the LDC is performed by means of the 3 Low Speed Bus Interface (LBI) units called BLR, BLS, and BLT. The following description covers all 3 LBI and in consequence of this, general names are used instead of actual descriptors. An actual descriptor is formed by adding a letter C, R, S, or T accordingly as the signal is generated in IOC, BLR, BLS, or BLT. For example, IO Ready is the general name for IOT Ready generated in BLT.

The LBI includes circuits for conversion of the balanced busline signals to signals with RCLM300 logic levels and vice versa. Beyond this gating of data words to the buslines and to some extend decoding of device command word (Sense, Control, Read, and Write).

6.4.2. Busline Functions.

During execution of an input/output instruction the necessary data and control signals are transferred via 32 buslines between the central processor and an external device. Some of the buslines are time-shared in the manner that the buslines to different times transfer different types of information during execution of the input/output instruction. The current type of information on these buslines are defined by the signals on special control buslines. The functions of the different buslines are stated in the following. The descriptors refer to the output busline signals available for the connected interface units and controllers.

IO BUS(0:23) By means of these buslines a device address, a device command, and a parameter or data word can be transferred from the central processor to an external device. The same buslines are used to transfer a data word from device to central processor. The input/output sequence is divided in a selection phase and a data phase.
In the Selection Phase:
IO BUS(12:17) transfers the device address and
IO BUS(18:23) transfers the device command.
In the Data Phase:
IO BUS(0:23) transfers a parameter or a data word.

IO Selection — The signal on this busline indicates the Selection Phase where device address and command information are on the buslines IO BUS(0:23). The signal is controlled by a micro command.

IO Data Transfer — The signal indicates the Data Phase.

In a Sense command, data and status information are transferred from the selected device to the central processor.

In a Control or Write command, a parameter or data word is sent from the central processor to the buslines IO BUS(0:23).

In a Read command, IO Data Transfer will appear as a short pulse just indicating the completion of the command.

IO Activate — This signal can be used in the Device Controller or Interface to activate the control circuits. In the Selection Phase, IO Activate indicates that selection has to take place. In the Data Phase, IO Activate appears in the Control and Write commands when a parameter or data word has been available on IO BUS(0:23) for about 1.5 microseconds.

IO Enable — The signal indicates the period of the IO instruction. If IO Enable = 1, the addressed device must reply to the busline signals; if IO Enable = 0, no devices must be attached to the channel.

IO Reset In — The reset signal on this busline is generated in the central processor, in a period after the point, where System Power has been switched on. System Power is on when power is on in central processor and in all LBI. This is indicated on the Operator Console, by the indicator System Power.

IO Ready — The busline is used for transmitting the device ready status signals to the central processor. (EX-register).

IO Connected — The busline is used for transmitting the device connected status signals to central processor (EX-register).

IO Power OK — The signal indicates that Power is on. If IO Power OK = 0, the buslines are not controlled and the devices must not respond to the signals.

6.4.3. Operational Description.

[Figures 6.4-1, 6.4-2]

Transmission of data and control signals on LDC is controlled by the microprogram for the IO instruction. The device address and device command are given by the effective address of the IO instruction. The data or parameter word to be transferred must be placed in the W-register specified by the IO instruction. The data word received from a device will be placed in the selected W-register.

Figures 6.4-1 and 6.4-2 show the timing of the input/output sequence. The sequence depends on, first, the ready and connected status for the addressed device, second, the device command version, namely Sense, Control, Read, or Write.

The sequence can be divided into a Selection Phase and a Data Phase. In the Selection Phase (IO Selection = 1), the device address (1 out of N codes) and the device command are transmitted via the buslines IO BUS(0:23) to all devices. The selected device sends its ready and connected status bits via buslines IO Ready and IO Connected. The status bits are received in the exception register EX. The microprogram tests the EX register and terminates if the device is not ready or not connected. See timing chart Figure 6.4-1.

If the device is free, i.e. ready and connected, an activation signal, IO Activate, is sent on the busline. The response of this signal is a selection of the device after which the information about the specific device command is stored. This must be completed before IO Selection returns to zero.

The microprogram now follows 1 of 3 routes depending on the device command versions 1) Sense, 2) Control or Write, and 3) Read. In this phase, the Data Phase, IO Data Transfer = 1. If the device command is a Sense command, the device has to send a status and data word via the buslines IO BUS(0:23) to the central processor; see Figure 6.4-1. The word

is received in the selected W-register. The Data Phase is terminated after transmission of this word.

In the Data Phase for Control or Write commands, the parameter or data word from the selected W-register is transmitted via IO BUS(0:23), and received in a device buffer register. See Figures 6.4-1 and 6.4-2.

If the device command is a Read command, no data transfer will take place, and the Data Phase is of very short duration. See Figure 6.4-2.

6.5. PROGRAM DESCRIPTION.

The input/output system is under supervision of the microprogram. The following micro commands are relevant:

IO Selection Signal = MC(45) $\vee$ MCB(45)
IO Data Transfer Signal = MC(44) $\vee$ MCB(44)
IO Timing Signal = MC(21) $\vee$ MCB(21)
Test IO = MC(20)
GiBUSfIOdata = MC(22)

It should be noted that three of the commands are buffered, i.e. the commands are independent of the control bistable Running Mode.

6.5.1. Ring Bus Specifications.

```
begin
  comment The 8 Channel Control Buslines are used to send the control sig-
    nals
                    IO Enable
                    IO Selection
                    IO Data Transfer
                    IO Activate
                    IO Power OK
                    IO Reset
    from CPU to the peripheral devices and to send the response signals
                    DEV Ready
                    DEV Connected
    from the selected device, DEV, to CPU. The declarations below assume
    that the LBI are connected in the following order IOC - BLR - BLS -
    BLT - IOC.
        DEVT Ready is only 1 provided the selected device, DEV, is in
```

```
  BLT and has the status bit Ready = 1. A similar notation is used for
  DEV Connected. Power OK is generated in CPU whereas BLR Power OK,
  BLS Power OK, and BLT Power OK are generated in their respective u-
  nits;
register
  IO Enable(0:0), Flow Direction(0:0);
comb net
  IO Selection(0:0) = IO Enable ∧ IO Selection Signal,
  IO Data Transfer(0:0) = IO Enable ∧ IO Data Transfer Signal,
  IO Activate(0:0) = IO Timing Signal,
  IOC Power OK(0:0) = Power OK,
  IOR Power OK(0:0) = IOC Power OK ∧ BLR Power OK,
  IOS Power OK(0:0) = IOR Power OK ∧ BLS Power OK,
  IOT Power OK(0:0) = IOS Power OK ∧ BLT Power OK,
  IOC Reset(0:0) = Power OK,
  IOR Reset(0:0) = IOC Reset,
  IOS Reset(0:0) = IOR Reset,
  IOT Reset(0:0) = IOS Reset ∨ IOT Power OK,
  IOC Ready(0:0) = 1,
  IOR Ready(0:0) = IOC Ready ∧ -,DEVR Ready,
  IOS Ready(0:0) = IOR Ready ∧ -,DEVS Ready,
  IOT Ready(0:0) = IOS Ready ∧ -,DEVT Ready,
  IO Ready(0:0) = -,IOT Ready,
  IOC Connected(0:0) = 1,
  IOR Connected(0:0) = IOC Connected ∧ -,DEVR Connected,
  IOS Connected(0:0) = IOR Connected ∧ -,DEVS Connected,
  IOT Connected(0:0) = IOS Connected ∧ -,DEVT Connected,
  IO Connected(0:0) = -,IOT Connected;
comment Before we continue to a description of the 24 Data Buslines, it
  is necessary to examine Device Address, which is an encoding of the
  device address SB(14:17). The outcome of the encoding is a selection
  of just one out of 16 lines;
comb net
  Device Address(0:15) =   (SB(14:17) = b0000)
                         con(SB(14:17) = b0001)
                         ...
                         con(SB(14:17) = b1111);
```

```
WRITE AND CONTROL:
  comment Both commands causes a transfer of data from the central processor
    to a peripheral device. The outcome of this operation depends on the
    selected device. The register element, Flow Direction = 1. The data in
    the W-register are transferred to SB at time 4500;
Time 4000:
  wait 1000;
Time 5000:
  IO Data Transfer Signal:= 1;
  comment IO BUS(0:23), which is equal to the contents of W;
  wait 1500;
Time 6500:
  IO Timing Signal:= 1;
  comment The signal often controls the setting of the device buffer;
  wait 1000;
Time 7500:
  IO Timing Signal:= 0; wait 3000;
Time 10500:
  IO Data Transfer Signal:= 0; IO Enable:= 0; goto INPUT OUTPUT;
READ:
  comment The read command directs the device to start a transfer of the
    next character from the external data medium into its buffer. The de-
    vice is busy until this operation is completed;
Time 4000:
  wait 500;
Time 4500:
  IO Data Transfer Signal:= 1; wait 500;
Time 5000:
  IO Data Transfer Signal:= 0; IO Enable:= 0; goto INPUT OUTPUT;
SENSE:
  comment A sense command is a request to a device to transfer the contents
    of its buffer to a W-register. The register element, Flow Direction = 0;
Time 4000:
  wait 500;
Time 4500:
  IO Data Transfer Signal:= 1;
```

```
  comment The contents of the lines IO BUS from the central processor to the
    device are all 1, whereas the contents of the same lines from the device
    back to the central processor equal the data of the device;
  wait until GiBUSfIOdata;
  comment This micro command opens the arithmetic bus system for the input/-
    output data;
Time 6500:
  wait 500;
Time 7000:
  IO Data Transfer Signal:= 0; IO Enable:= 0; goto INPUT OUTPUT;
end;
```