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TEST OF

DISPLAY AND DECODING NETWORKS (ARU)

FOR THE RC 4000 COMPUTER

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NOTATION

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1. Theory
2. Test Schedule

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1. Theory
2. Test Schedule

NOTATION

Single Micro Instruction:	Activate the Single Micro Instruction pushbutton on the Technical Control Panel.
X:= Y	Set X equal to Y.
X = Y	If the test is correct X should be equal to Y.
X:= -1	Set X equal to all ones.
-	Signifies a don't care condition in a test table.
QQ(8 9 1 1 2) 0 5 3	Signifies the bit positions 8, 9, 10, 15, and 23 in the QQ register.

PART I. REGISTER DISPLAY AND BUS TEST

1. THEORY

This test includes a check of the 28 individual set and reset pushbuttons plus the 2 collective set and reset pushbuttons for the register display system. Moreover, the display registers (DR(-1:23) and DP(0:2)) are also tested for malfunctioning.

The BUS system is tested by applying the same testschedule for each register, and it is investigated if any of the bits are interchanged. The IR register cannot participate in this test since it is not possible to alter its contents from the display panel.

2. TEST SCHEDULE

2.1. Initialize Test

Select all the registers and set their contents equal to all ones. MAR:= x20y13 whereby SUM = AR + SB + 1, i.e. the output from the adder circuitry is all ones, and this is also the case for the AND output.

2.2. General Testpattern.

The general testpatterns applied to a register QQ(r:s) should be as follows:

QQ(r	r+1	r+2	...	s-1	s)	
1	1	1	...	1	1	collective set
0	1	1	...	1	1	individual reset
1	0	1	...	1	1	individual reset and set
1	1	0	...	1	1	individual reset and set
.	.	.	...	.	.	
1	1	1	...	0	1	individual reset and set
1	1	1	...	1	0	individual reset and set
1	1	1	...	1	1	individual set
0	0	0	...	0	0	collective reset
1	1	1	...	1	1	collective set

2.3. Test List

The table below lists the registers to be tested. The bits to be examined by the general testpatterns are marked with X.

		DR(-1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22)	DP(0	1	2)
Select	W0		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x	x	x
-	W1		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x	x	x
-	W2		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x	x	x
-	W3		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x	x	x
-	IC					x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x						
-	SC												x	x	x	x	x	x	x	x	x	x	x	x	x				
-	FR		x	x	x	x	x	x	x	x	x	x	x																
-	SB		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x		x	x	x
-	SE		x	x	x	x	x	x	x	x	x	x	x	x															
-	AR	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x				
-	AE		x	x	x	x	x	x	x	x	x	x	x	x															
-	BR		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x				
-	BE		x	x	x	x	x	x	x	x	x	x	x																
-	PR																			x	x	x	x	x	x				
-	EX																							x	x				
-	IM		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x				

IM(p):= SB(p) when MAR:= x12y12 and Single Micro Instruction is activated.

PART II. DISPLAY SELECTION

1. THEORY

The purpose of this test is to verify whether the register selector does select all the registers or not. This is simply tested by applying different numbers to the registers, and then repeat the register selection to see if the registers still have their correct contents.

2. TEST SCHEDULE

Select w0; w0:= 0; w0(17):= 1
Select w1; w1:= 0; w1(16):= 1
Select w2; w2:= 0; w2(15):= 1
Select w3; w3:= 0; w3(14):= 1
Select IC; IC:= 0; IC(13):= 1
Select SC; SC:= 0; SC(12):= 1
Select FR; FR:= 0; FR(11):= 1
Select SB; SB:=-1; MAR:= x12y12; Single Micro Instruction; IM = -1
MAR:= x12y13; Single Micro Instruction; IR = 0
The bit corresponding to the Interval Timer is set to 1 after the specified time period.
SB:= 0; SB(10):= 1
Select SE; SE:= 0; SE(9):= 1
Select AR; AR:= 0; AR(8):= 1
Select AE; AE:= 0; AE(7):= 1
Select BR; BR:= 0; BR(6):= 1
Select BE; BE:= 0; BE(5):= 1
Select PR; PR:= 0; PR(7):= 1 (PR(7) is bit position number 23 in the display field)
Select EX; EX:= 0; EX(22):= 1

The test data are now applied to the registers. The registers are selected anew and the results should be:

		DR(-1	0	1	2	3	4	5	6	7	8	9	1 0	1 1	1 2	1 3	1 4	1 5	1 6	1 7	1 8	1 9	2 0	2 1	2 2	2 3)	DP(0	1	2)	
Select	W0		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0		0	0	0	
-	W1		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0		0	0	0	
-	W2		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0		0	0	0	
-	W3		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0		0	0	0	
-	IC		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0		0	0	0	
-	SC		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0		0	0	0	
-	FR		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	
-	SB		0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	
-	SE		0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	
-	AR		0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	
-	AE		0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	
-	BR		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	
-	BE		0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	
-	PR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		0	0	0	
-	EX		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0		0	0	0	
-	IR		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	0	0	NB
-	IM		0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		0	0	0	

NB: The bit corresponding to the Interval Timer is 1.

PART III. DECODING NETWORKS (ARU)

1. THEORY

The test schedule evaluated here is meant for testing the decoding networks in ARU for single errors. The circuits are tested for stuck-at-1 and stuck-at-0, whenever possible.

The underlined name is the descriptor of the network under test. Test Point defines where the output of the network can be found. In Circuits are listed the circuits (<actual bord position> <circuit letter>) employed to implement the decoding. Assumptions tell whether the test must be preceded by another test. f is the correct output for the network.

2. TEST SCHEDULE

ICaddr Error

Test Point: 176A (ARU049)
Circuits: 168A, 232D, 176A, (ARU049)
Assumptions: no
Note: The testpattern is for a 16K core store

IC(5 6 7 8)	f
0 0 0 0	0
0 0 0 1	1
0 0 1 0	1
0 1 0 0	1
1 0 0 0	1

ICaddr ST

Test Point: 175C (ARU049)
Circuits: 233A, 233B, 175A, 175B, 175C, (ARU049)
Assumptions: ICaddr Error is tested
Note: The testpattern is for a 16K core store

IC(5 6 7 8 9 1 1 1 1 1 1 1 1 1 1 2) 0 1 2 3 4 5 6 7 8 9 0	f
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	1
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0	1
0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0	1
0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0	1
0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0	1
0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0	1
0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0	1
0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	1
0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0	1
0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	1
0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0	1

SC ≠ 0

Test Point: 175J (ARU067)
Circuits: 180A, 180B, 175F, 175G, 175J, (ARU067)
Assumptions: no

SC(1 1 1 1 1 1 1 1 1 2 2 2 2)	f
1 2 3 4 5 6 7 8 9 0 1 2 3	
0 0 0 0 0 0 0 0 0 0 0 0 0	0
0 0 0 0 0 0 0 0 0 0 0 0 1	1
0 0 0 0 0 0 0 0 0 0 0 1 0	1
0 0 0 0 0 0 0 0 0 0 1 0 0	1
0 0 0 0 0 0 0 0 0 1 0 0 0	1
0 0 0 0 0 0 0 0 1 0 0 0 0	1
0 0 0 0 0 0 0 1 0 0 0 0 0	1
0 0 0 0 0 0 1 0 0 0 0 0 0	1
0 0 0 0 0 1 0 0 0 0 0 0 0	1
0 0 0 0 1 0 0 0 0 0 0 0 0	1
0 0 0 1 0 0 0 0 0 0 0 0 0	1
0 0 1 0 0 0 0 0 0 0 0 0 0	1
0 1 0 0 0 0 0 0 0 0 0 0 0	1
1 0 0 0 0 0 0 0 0 0 0 0 0	1

SC(11) ≠ SC(12)

Test Point: 179G (ARU067)
Circuits: 179G, (ARU067)
Assumptions: no

SC(1 1)	f
1 2	
0 0	0
0 1	1
1 0	1
1 1	0

SC < 38 ∧ SC > -38

Test Point: 168C (ARU067)
Circuits: 180C, 175H, 188A, 188B, 175K, 175L, 188C, 180D, 168C, (ARU067)
Assumptions: SC ≠ 0 is tested

SC(1 1 1 1 1 1 1 1 1 2 2 2 2)	f
1 2 3 4 5 6 7 8 9 0 1 2 3	
1 1 1 1 1 1 1 0 0 0 0 0 0	0
0 0 0 0 0 0 0 1 1 0 0 0 0	0
0 0 0 0 0 0 0 1 0 1 0 0 0	0
0 0 0 0 0 0 0 1 0 0 1 1 0	0
0 1 1 1 1 1 1 1 1 1 1 1 1	0
1 0 1 1 1 1 1 1 1 1 1 1 1	0
1 1 0 1 1 1 1 1 1 1 1 1 1	0
1 1 1 0 1 1 1 1 1 1 1 1 1	0
1 1 1 1 0 1 1 1 1 1 1 1 1	0
1 1 1 1 1 0 1 1 1 1 1 1 1	0
1 1 1 1 1 1 0 1 1 1 1 1 1	0
1 1 1 1 1 1 1 0 1 1 1 1 1	0
1 1 1 1 1 1 1 1 0 0 1 1 1	0
1 1 1 1 1 1 1 1 0 1 0 1 1	0
1 1 1 1 1 1 1 1 0 1 1 0 0	1
1 1 1 1 1 1 1 1 0 1 1 0 1	0
0 0 0 0 0 0 0 0 0 0 0 0 0	1
1 1 1 1 1 1 1 1 1 1 1 1 1	1

SB ≠ 0

Test Point: 373C (ARU089)
Circuits: 298A, 298B, 180A, 373B, 365L, 365M, 376L, 376M, 373C, (ARU089)
Assumptions: no

SB(0 1 2 3 4 5 6 7 8 9 1 1 1 1 1 1 1 1 1 2 2 2 2)	f
0 1 2 3 4 5 6 7 8 9 0 1 2 3	
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0	1
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	1
0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0	1
0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	1
0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	1
0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1
0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1
0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1
0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1
0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1
0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1
0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1
0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1

SB ≥ 64

Test Point: 300F (ARU089)
Circuits: 373D, 300E, 300F, (ARU089)
Assumptions: SB ≠ 0 is tested

SB(0 1 2 3 4 5 6 7 8 9 1 1 1 1 1 1 1 1)	f
0 1 2 3 4 5 6 7	
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0	1
0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

SB $\leq$ -65 $\vee$ SB $\geq$ 0

Test Point: 373G (ARU089)
Circuits: 298C, 298D, 370D, 370E, 373G, (ARU089)
Assumptions: no

SB(0 1 2 3 4 5 6 7 8 9	1 1 1 1 1 1 1 1) 0 1 2 3 4 5 6 7	f
1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	0
1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 0	1
1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 0 1	1
1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 0 1 1	1
1 1 1 1 1 1 1 1 1 1	1 1 1 1 0 1 1 1	1
1 1 1 1 1 1 1 1 1 1	1 1 1 0 1 1 1 1	1
1 1 1 1 1 1 1 1 1 1	1 1 0 1 1 1 1 1	1
1 1 1 1 1 1 1 1 1 1	1 0 1 1 1 1 1 1	1
1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1	1
1 1 1 1 1 1 1 1 1 0	1 1 1 1 1 1 1 1	1
1 1 1 1 1 1 1 1 0 1	1 1 1 1 1 1 1 1	1
1 1 1 1 1 1 1 0 1 1	1 1 1 1 1 1 1 1	1
1 1 1 1 1 1 0 1 1 1	1 1 1 1 1 1 1 1	1
1 1 1 1 1 0 1 1 1 1	1 1 1 1 1 1 1 1	1
1 1 1 1 0 1 1 1 1 1	1 1 1 1 1 1 1 1	1
1 1 1 0 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1
1 1 0 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1
1 0 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1
0 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1	1

SBaddr Error

Test Point: 370C (ARU049)
Circuits: 233C, 373E, 232E, 232F, 370C, (ARU049)
Assumptions: no
Note: The testpattern is for a 16K core store

SB(0 1 2 3 4 5 6 7 8)	f
0 0 0 0 0 0 0 0 0	0
0 0 0 0 0 0 0 0 1	1
0 0 0 0 0 0 0 1 0	1
0 0 0 0 0 0 1 0 0	1
0 0 0 0 0 1 0 0 0	1
0 0 0 0 1 0 0 0 0	1
0 0 0 1 0 0 0 0 0	1
0 0 1 0 0 0 0 0 0	1
0 1 0 0 0 0 0 0 0	1
1 0 0 0 0 0 0 0 0	1

SBaddr ST

Test Point: 370B (ARU049)
Circuits: 233D, 373F, 370B, (ARU049)
Assumptions: SB ≠ 0, SBaddr Error are tested
Note: The testpattern is for a 16K core store

SB(0 1 2 3 4 5 6 7 8 9 1 1 1 1 1 1 1 1 1 1 2)	f
0 1 2 3 4 5 6 7 8 9 0	
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0	1
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0	1
0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0	0
0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0

AR(-1) = AR(0)

Test Point: 222A (ARU078)
Circuits: 222A, (ARU078)
Assumptions: no

AR(-1 0)	f
0 0	1
0 1	0
1 0	0
1 1	1

AR(0) = AR(1)

Test Point: 222B (ARU078)
Circuits: 222B, (ARU078)
Assumptions: no

AR(0 1)	f
0 0	1
0 1	0
1 0	0
1 1	1

AR(1) = AR(2)

Test Point: 222C (ARU078)
Circuits: 222C, (ARU078)
Assumptions: no

AR(1 2)	f
0 0	1
0 1	0
1 0	0
1 1	1

AR ≠ 0

Test Point: 214F (ARU078)
Circuits: 356A, 356B, 241A, 365E, 365F, 370A, 214F, (ARU078)
Assumptions: no

```
AR(-1 0 1 2 3 4 5 6 7 8 9 1 1 1 1 1 1 1 1 1 1 2 2 2 2)    f
                          0 1 2 3 4 5 6 7 8 9 0 1 2 3

   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     0
   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1     1
   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0     1
   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0     1
   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0     1
   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0     1
   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0     1
   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0     1
   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0     1
   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0     1
   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0     1
   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0     1
   0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0     1
   0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0     1
   0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0     1
   0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0     1
   0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     1
   0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     1
   0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     1
   0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     1
   0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     1
   0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     1
   0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     1
   0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     1
   0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     1
   0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     1
   1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     1
```

AR = 0

Test Point: 382J (ARU078)
Circuits: 382J, (ARU078)
Assumption: AR ≠ 0 is tested

```
AR(-1 0 1 2 3 4 5 6 7 8 9 1 1 1 1 1 1 1 1 1 1 2 2 2 2)    f
                          0 1 2 3 4 5 6 7 8 9 0 1 2 3

   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     1
   1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     0
```

AR > 0

Test Point: 382L (ARU078)
Circuits: 382K, 382L, (ARU078)
Assumptions: AR ≠ 0 is tested

```
AR(-1 0 1 2 3 4 5 6 7 8 9 1 1 1 1 1 1 1 1 1 1 2 2 2 2)    f
                          0 1 2 3 4 5 6 7 8 9 0 1 2 3

   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1     1
   0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     0
   1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0     0
```

AF ≠ 0

Test Point: 300H (ARU079)
Circuits: 356C, 365G, 356D, (ARU078)
300G, 300H, (ARU079)
Assumptions: AR = 0 is tested

AF(-1	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37)	f
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Round

Test Point: 213G (ARU079)
Circuits: 222A, 365H, 222B, 365J, (ARU078)
365K, 213E, 213F, 213G, (ARU079)
Assumptions: no

AR(-1	0	1)	AE(1 1	1 2	1) 3	f
0	0	0	1	1	0	0
1	1	1	1	1	0	0
1	1	0	1	0	1	0
0	0	1	1	0	1	0
0	1	1	0	-	1	0
1	0	1	0	1	-	0
0	1	-	1	-	-	1
1	0	-	1	-	-	1
1	1	0	-	1	-	1
0	0	1	-	1	-	1
0	0	0	-	-	1	1
1	1	1	-	-	1	1

BR(1) = BR(2)

Test Point: 222D (ARU079)
Circuits: 222D, (ARU079)
Assumption: no

BR(1	2)	f
0	0	1
0	1	0
1	0	0
1	1	1

BRaddr ST

Test Point: 157M (ARU079)
Circuits: 241C, 241D, 366L, 366M, 157M, (ARU079)
Assumptions: no

```
BR(6 7 8 9 1 1 1 1 1 1 1 1 1 2)    f
           0 1 2 3 4 5 6 7 8 9 0

   0 0 0 0 0 0 0 0 0 0 0 0 0 0     0
   0 0 0 0 0 0 0 0 0 0 0 0 1 0     1
   0 0 0 0 0 0 0 0 0 0 0 1 0 0     1
   0 0 0 0 0 0 0 0 0 0 1 0 0 0     1
   0 0 0 0 0 0 0 0 0 1 0 0 0 0     1
   0 0 0 0 0 0 0 0 1 0 0 0 0 0     1
   0 0 0 0 0 0 0 1 0 0 0 0 0 0     1
   0 0 0 0 0 0 1 0 0 0 0 0 0 0     1
   0 0 0 0 0 1 0 0 0 0 0 0 0 0     1
   0 0 0 0 1 0 0 0 0 0 0 0 0 0     1
   0 0 0 1 0 0 0 0 0 0 0 0 0 0     1
   0 0 1 0 0 0 0 0 0 0 0 0 0 0     1
   0 1 0 0 0 0 0 0 0 0 0 0 0 0     1
   1 0 0 0 0 0 0 0 0 0 0 0 0 0     1
```

EX(22,23) ≠ 0

Test Point: 382M (ARU102)
Circuits: 382M, (ARU102)
Assumptions: no

```
EX(2 2)    f
   2 3

   0 0     0
   0 1     1
   1 0     1
```

FR(6) ∨ FR(7)

Test Point: 92A (ARU070)
Circuits: 92A, (ARU070)
Assumptions: no

```
FR(6 7)    f

   0 0     0
   0 1     1
   1 0     1
```

FR(10) ∨ FR(11)

Test Point: 92J (ARU070)
Circuits: 92J, (ARU070)
Assumptions: no

```
FR(1 1)    f
   0 1

   0 0     0
   0 1     1
   1 0     1
```

FR(0:5) = 9

Test Point: 92K (ARU070)
Circuits: 168D, 92K, (ARU070)
Assumptions: no

FR(0 1 2 3 4 5)	f
0 0 1 0 0 0	0
0 0 1 0 1 1	0
0 0 1 1 0 1	0
0 0 0 0 0 1	0
0 1 1 0 0 1	0
1 0 1 0 0 1	0
0 0 1 0 0 1	1

MMode ∨ -,PROTECT

Test Point: 245J (ARU105)
Circuits: 249A, 249B, 249C, 249D, 249E, 249F, 249G, 253A, 241B, (ARU104)
245J, (ARU105)
Assumptions: no

PK(0 1 2)	PR(1 1 1 1 2 2 2 2) 6 7 8 9 0 1 2 3	MMode	f
0 0 0	1 - - - - - - -	1	1
0 0 1	1 0 - 1 - 1 - -	0	1
0 1 0	1 - 0 1 - - 1 -	0	1
0 1 1	1 1 1 0 - - - 1	0	1
1 0 0	1 - - - 0 1 1 -	0	1
1 0 1	1 1 - - 1 0 - 1	0	1
1 1 0	1 - 1 - 1 - 0 1	0	1
1 1 1	1 - - 1 - 1 1 0	0	1
0 0 0	1 0 0 0 0 0 0 0	0	0
0 0 1	1 1 0 0 0 0 0 0	0	0
0 1 0	1 0 1 0 0 0 0 0	0	0
0 1 1	1 0 0 1 0 0 0 0	0	0
1 0 0	1 0 0 0 1 0 0 0	0	0
1 0 1	1 0 0 0 0 1 0 0	0	0
1 1 0	1 0 0 0 0 0 1 0	0	0
1 1 1	1 0 0 0 0 0 0 1	0	0

MMode is set to 1 as follows:

PR:= b 10000000; PK:= b 000; MAR:= x4y18; Single Micro Instruction;
MMode = 1

MMode is set to 0 as follows:

PR:= b 10000000; PK:= b 100; MAR:= x4y18; Single Micro Instruction;
MMode = 0