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DSC 801
Logic Diagrams and
Functional Description

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CONTENTS DRAWING NO.

SIGNAL	DESTI-NATION	DESCRIPTION
DATA 0:7	P3	Tristate output from busreceiver register bits 0:7. Gated to DATA A-bus by Sel byte 0.
DATA 8:15	P3	Tristate output from busreceiver register bits 8 : 15. Gated to DATA A-bus by Sel byte 1.
*DATA 16:19	P2	Output from Bus receiver bits 16:19

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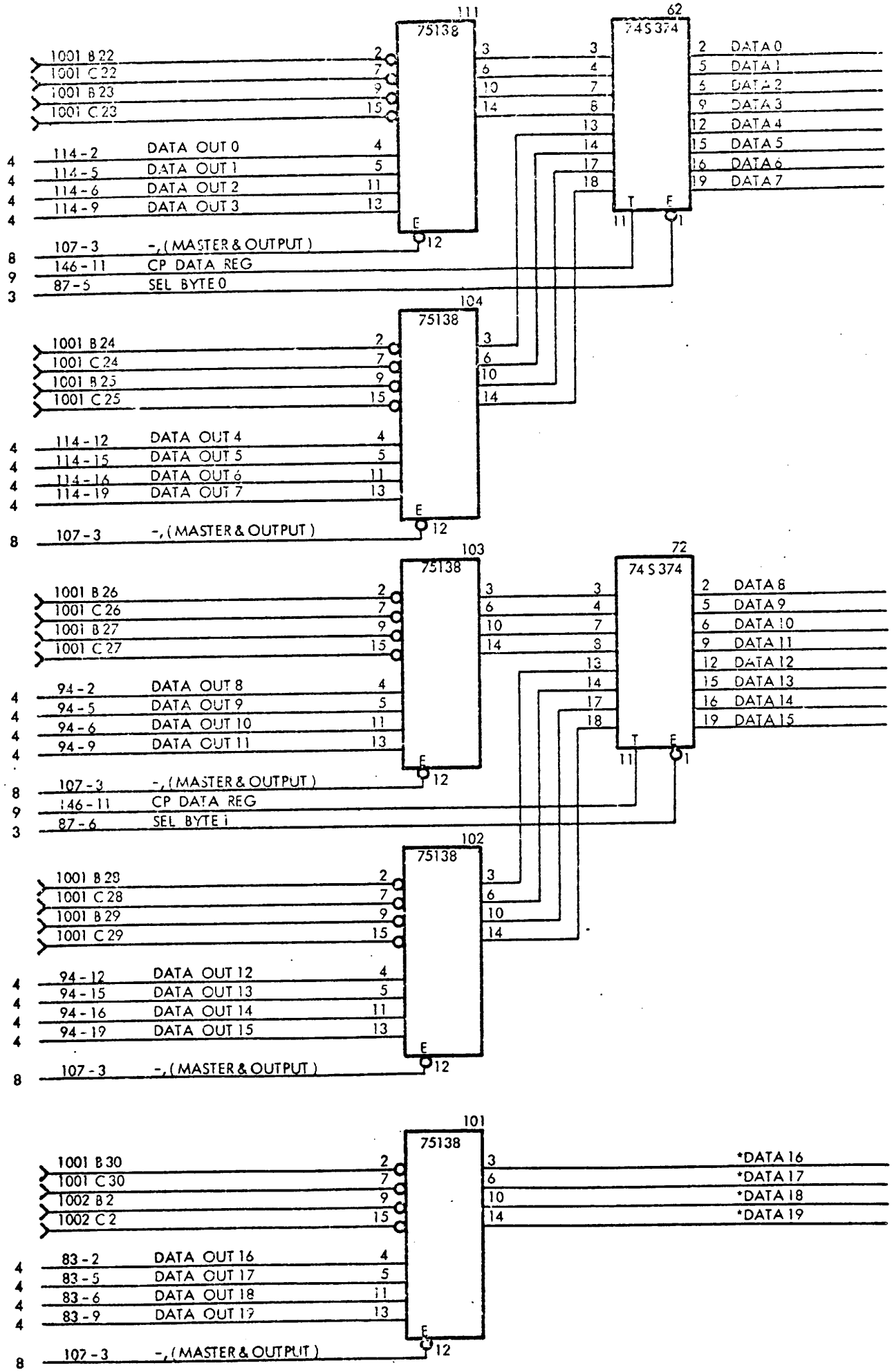

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BUSTRANSCEIVERS AND DATAIN REGISTERS
LOGIC DIAGRAM

P 1

R11655

SIGNAL	DESTI-NATION	DESCRIPTION
DATA 16-23	P3	Tristate output from bus receiver register bits 16:23. Gated to DATA A bus by Sel byte 2.
Datapar 0:2	P3	Output from busreceiver register parity bit 0:3. Used for parity checking of resp. Data 0:7, Data 8:15 and Data 16:23.
Buscheck	P21	Indicates an erroneous bustransfer to or from RC8000. May be Time out or Nack received. Used for microprogram sequencing.
NACK	P24	Indicates that the slave has detected a busparityerror. Used for microprogram sequencing.
ACC 0:7	P3	Tristate output of Accumulator register. Gated to DATA A bus by Sel ACC.
Parity error	P21	Even parity on selected byte DATA A bus. Used for microprogram sequencing.
Parity B	P4	Parity bit generated for DATA B bus to bustransmitter registers.

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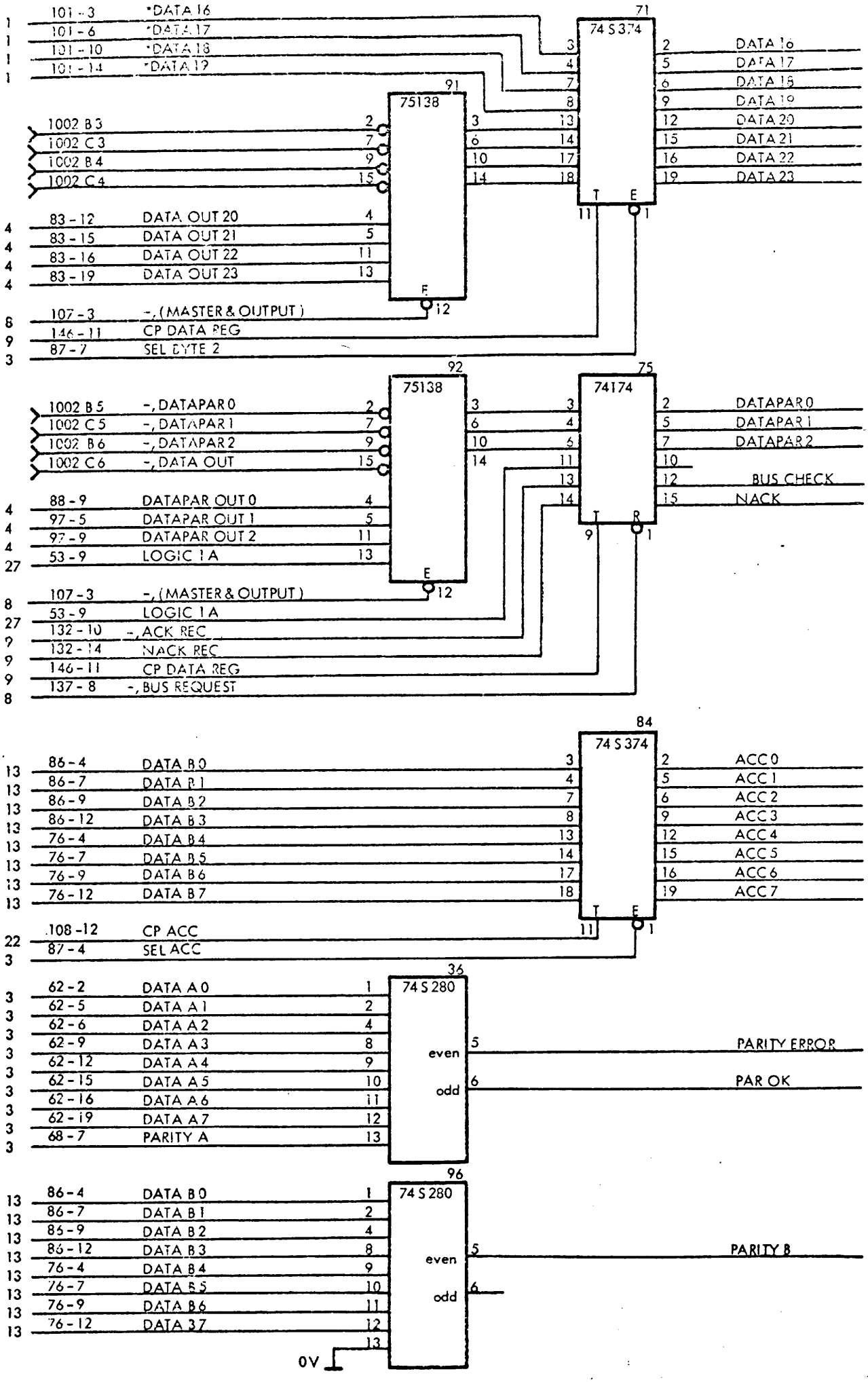

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DSC 801 BUSTRANSCEIVERS, DATAINPUTREGISTER, AC PARITY CHECKER GENERATOR
LOGIC DIAGRAM

P 2

R11656

SIGNAL	DESTI-NATION	DESCRIPTION
DATA A 0:7	P2 P10 P20	DATA A BUS Source for ALU, Register store and Fifobuffer.
Parity A	P2	Parity bit on DATA A BUS
ACC parity	P3	Parity bit for Accumulatorregister.
SEL ACC, SEL byte 0:2		Tristate control signals for selecting the input to DATA A-bus.

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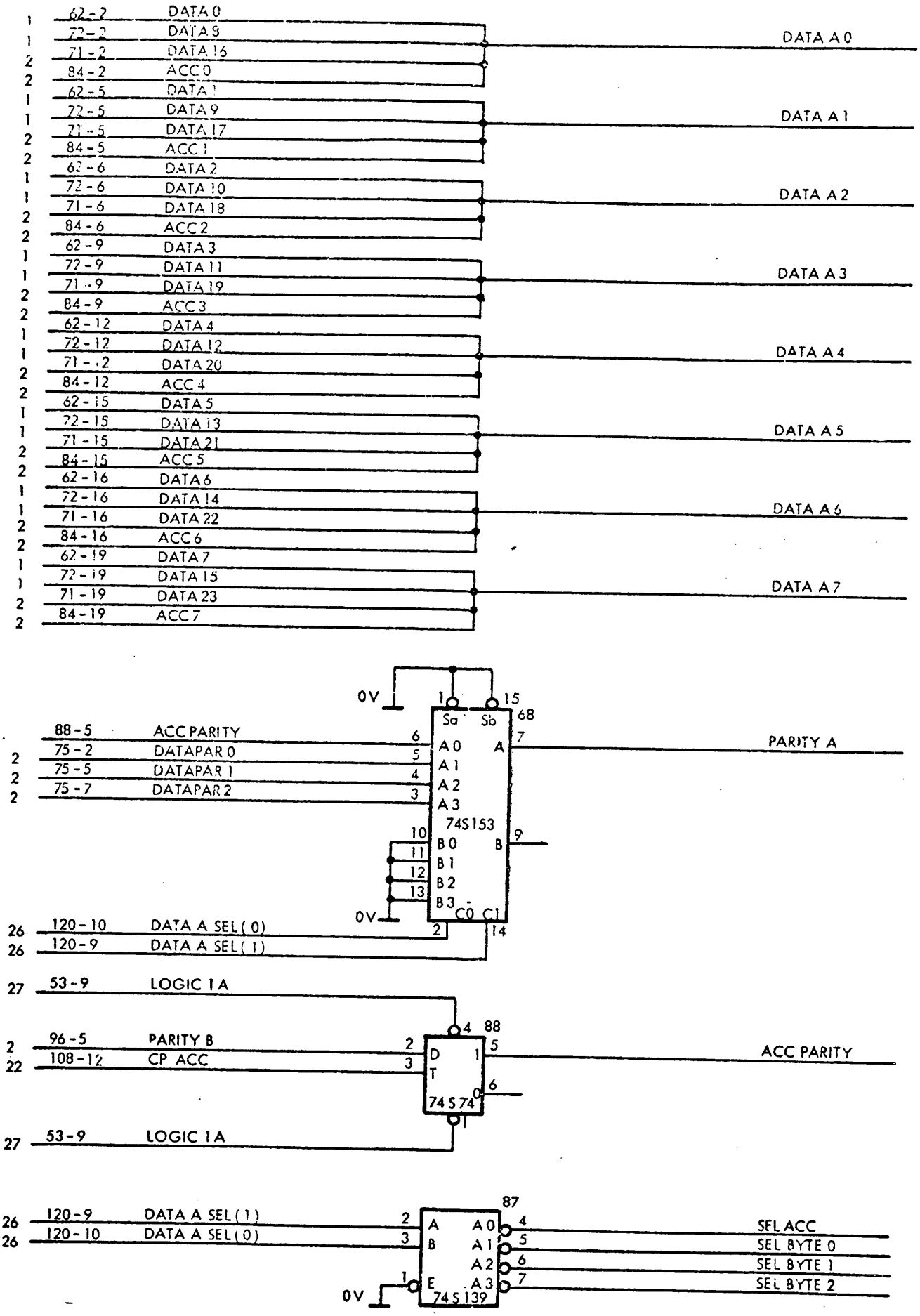

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R11657

"TRISTATING" OF A-SOURCE
LOGIC DIAGRAM

P3

SIGNAL	DESTI-NATION	DESCRIPTION
DATA OUT 0:19	P1	Data and parity register outputs
DATA OUT 20:23		to be transmitted on RC 8000 bus.
DATAPAR OUT 0:2	P2	

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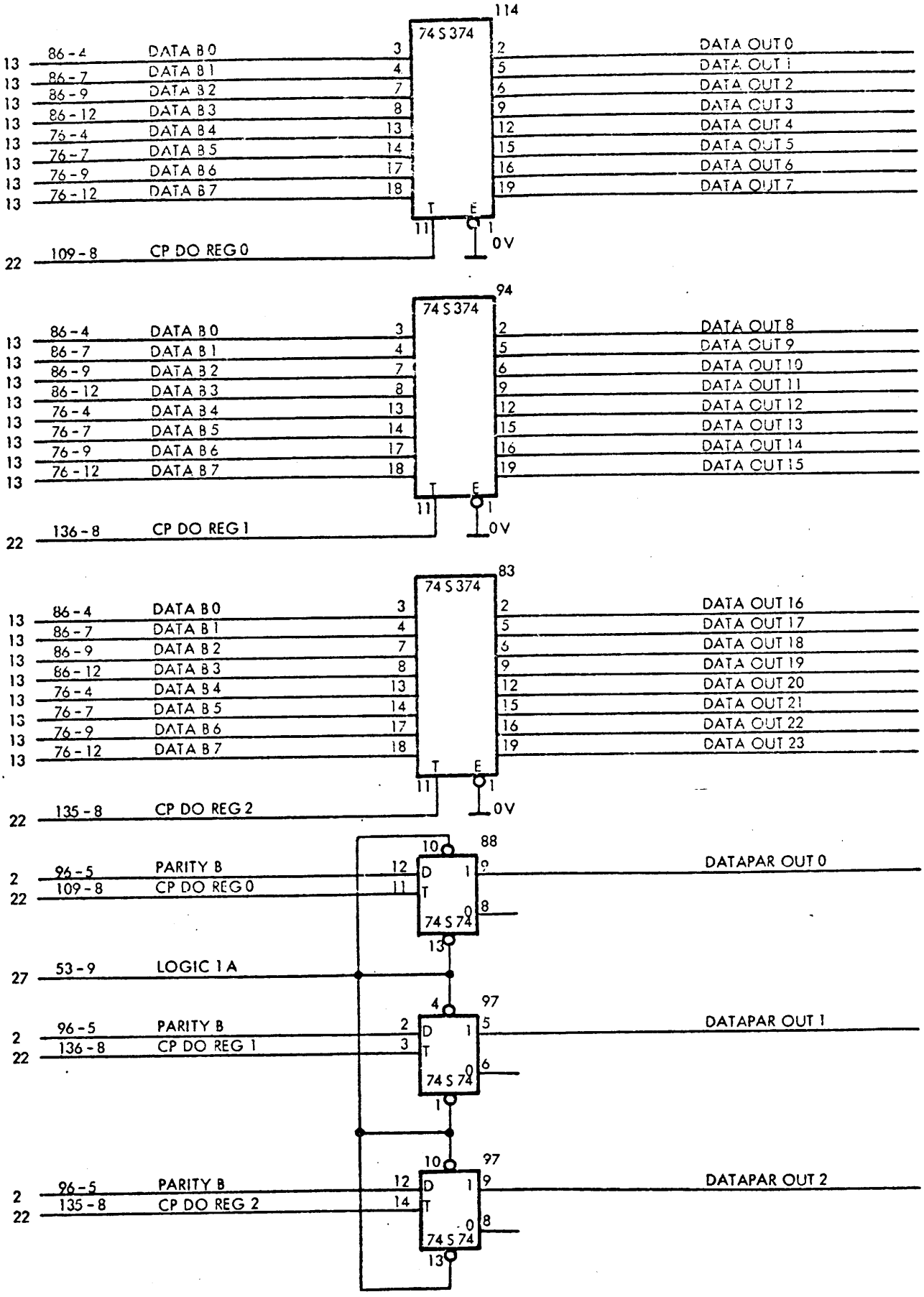

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SIGNAL	DESTI-NATION	DESCRIPTION
DEVADDR 0:22, DEVADDRPARITY	P6	Output from RC 8000 Bus address receives.

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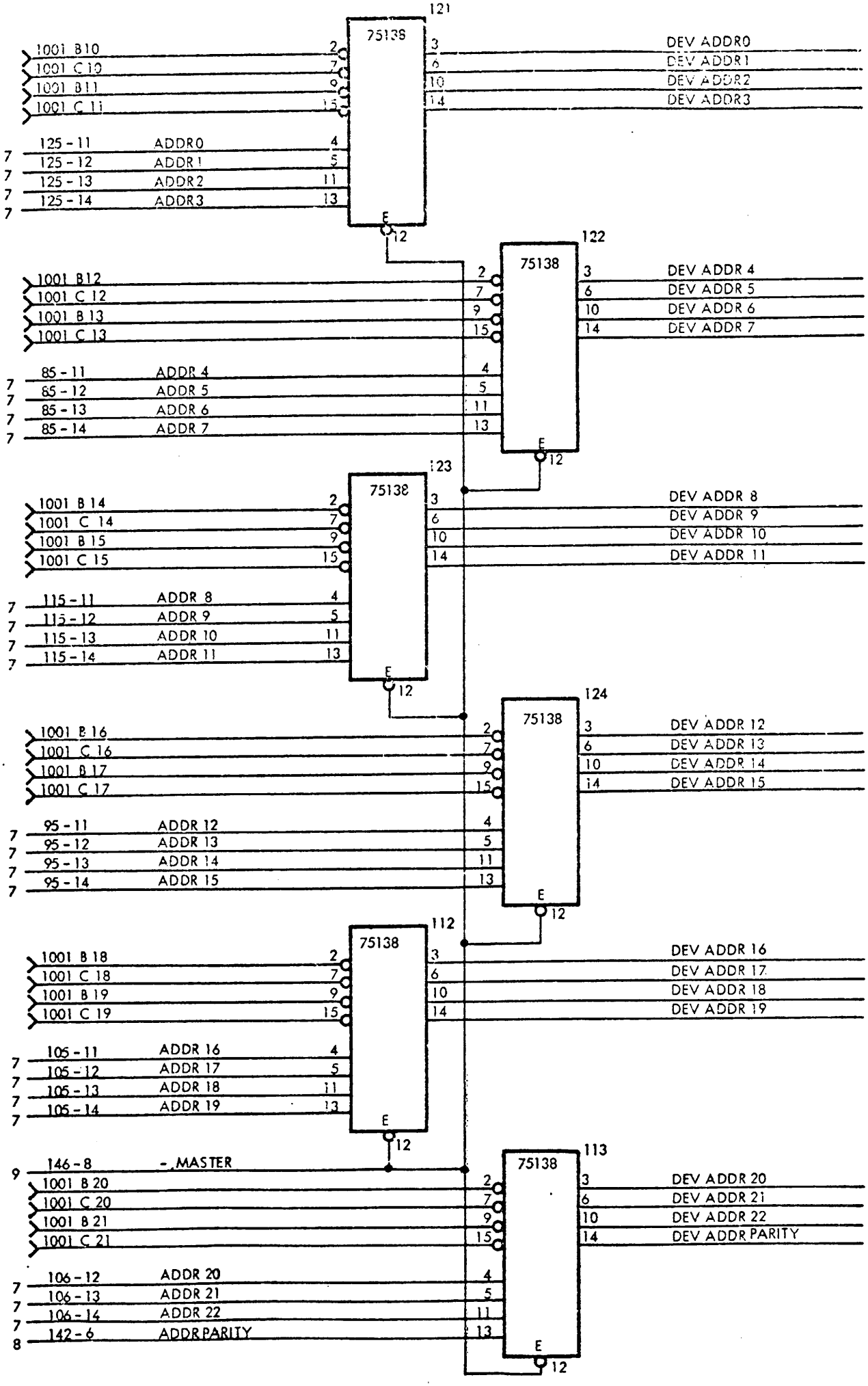

DSC 801
R11659

BUS ADDRESS TRANSCEIVERS
LOGIC DIAGRAM

SIGNAL	DESTI-NATION	DESCRIPTION
-,DEVADDR	P14	Low whenever the address on RC 8000 bus compares with the Addressswitch setting, and parity is odd.
ADDRSW 13-18	P10	Output of the Deviceaddressswitches. Used for computing base address.

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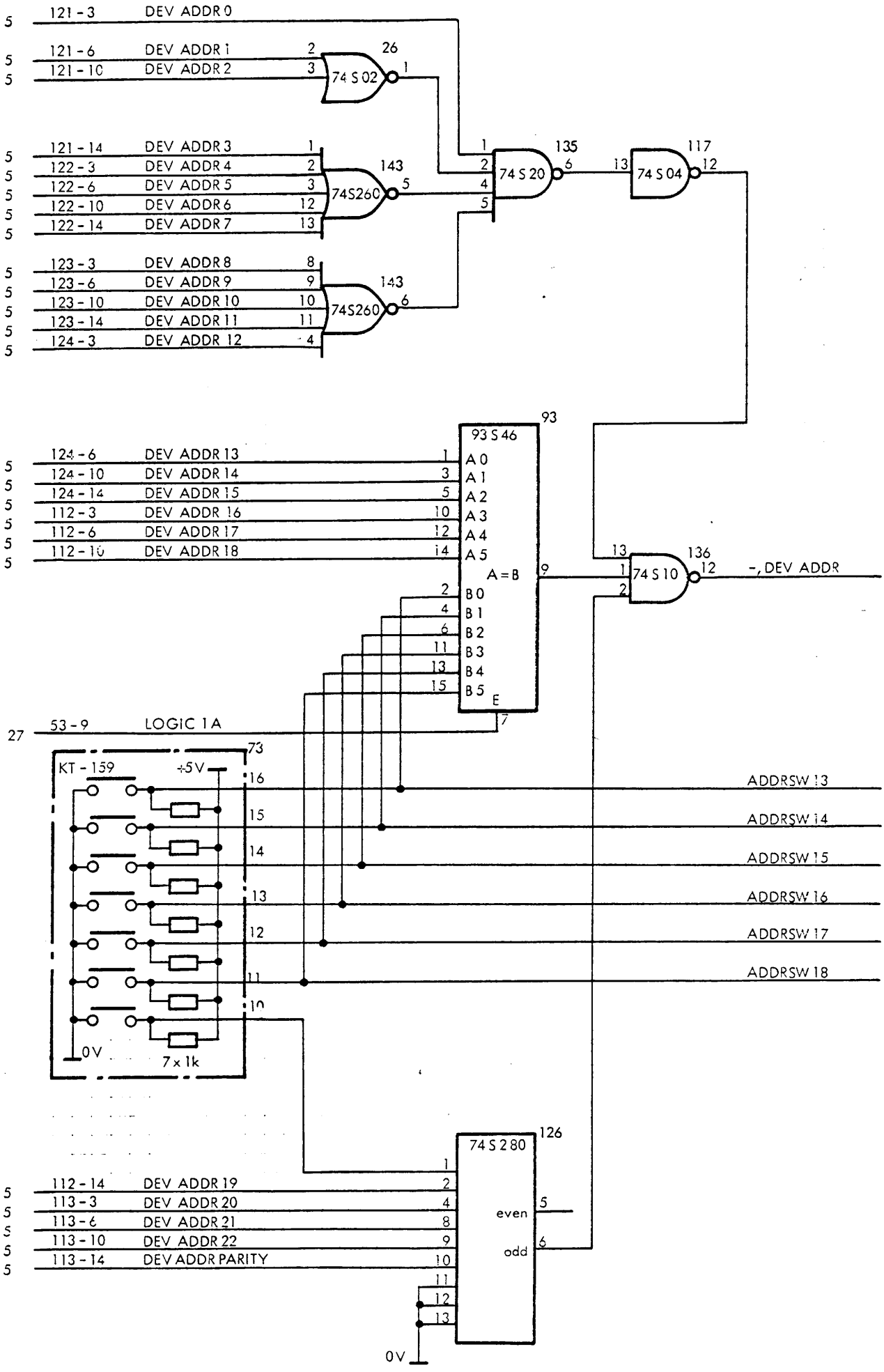

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SIGNAL	DESTI-NATION	DESCRIPTION
ADDR 0:22	P5	Outputs of the address register counter to be transmitted on the RC 8000 bus.

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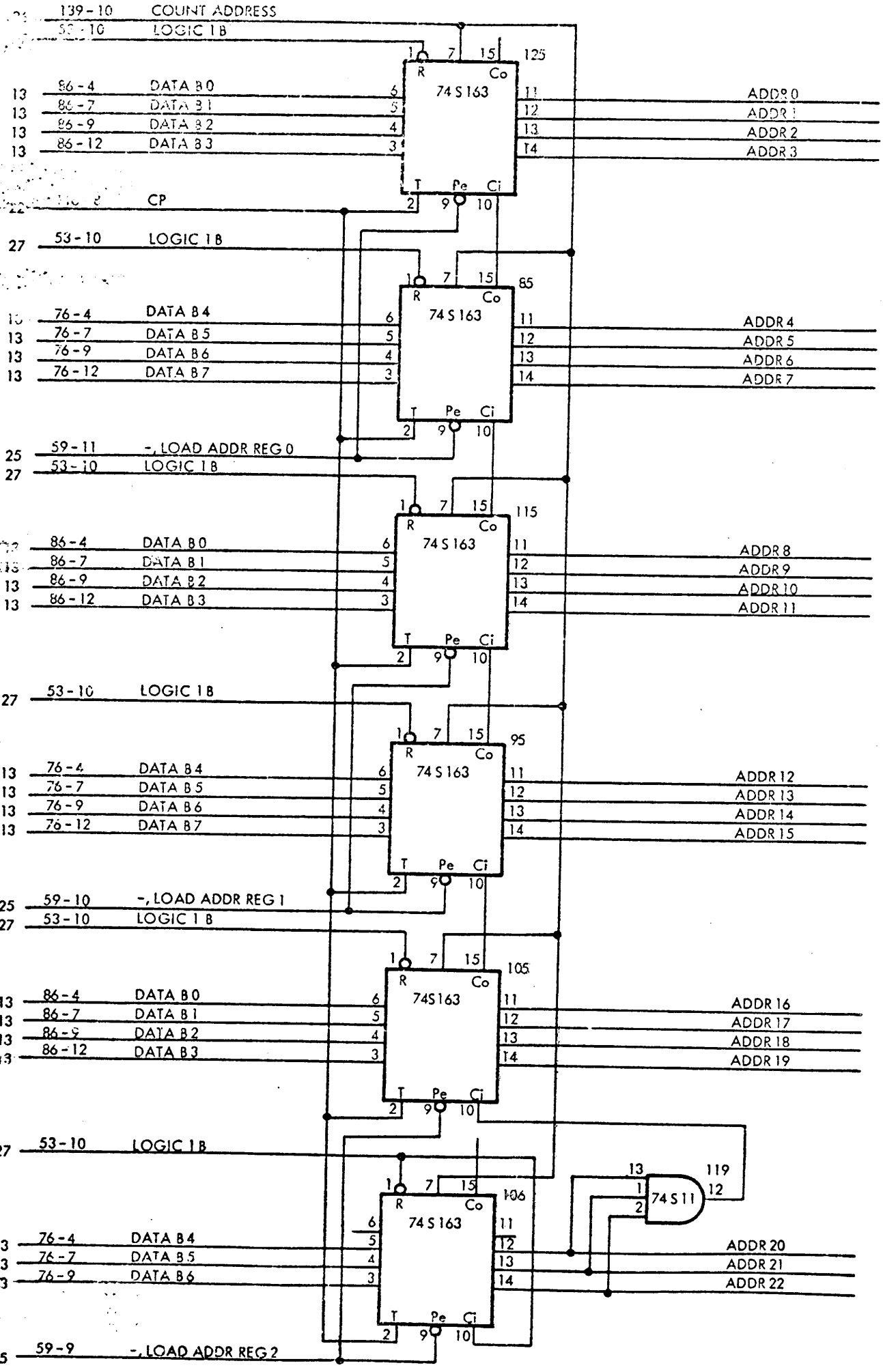

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R11661

BUS ADDRESS COUNTER REGISTER
LOGIC DIAGRAM

SIGNAL	DESTI-NATION	DESCRIPTION
Addr parity	P5	Is the parity on the address register counter on P7, making the addressparity on RC 8000 bus odd.
-,(OUTPUT & MASTER)	P1 P2	Controls datatransmission on RC 8000 bus
BUS REQ	P9	Initiates a RC 8000 busselection, and inhibits the next select in signal from propagating to the next controller on bus.
-,BUS REQ	P2	Resets Busstatus and Parity register.
PINT	P21	Power interrupt signal from RC 8000 BUS. Used for microprogram sequencing.
POK	P18	Power OK signal from RC 8000 BUS. Used for clearing of Handshake flip-flop.
-,POK	P8	The inverse of POK or-ed togther with System Reset from BUS to create a
-,Clear	P12	-,clear signal used for Master clearing

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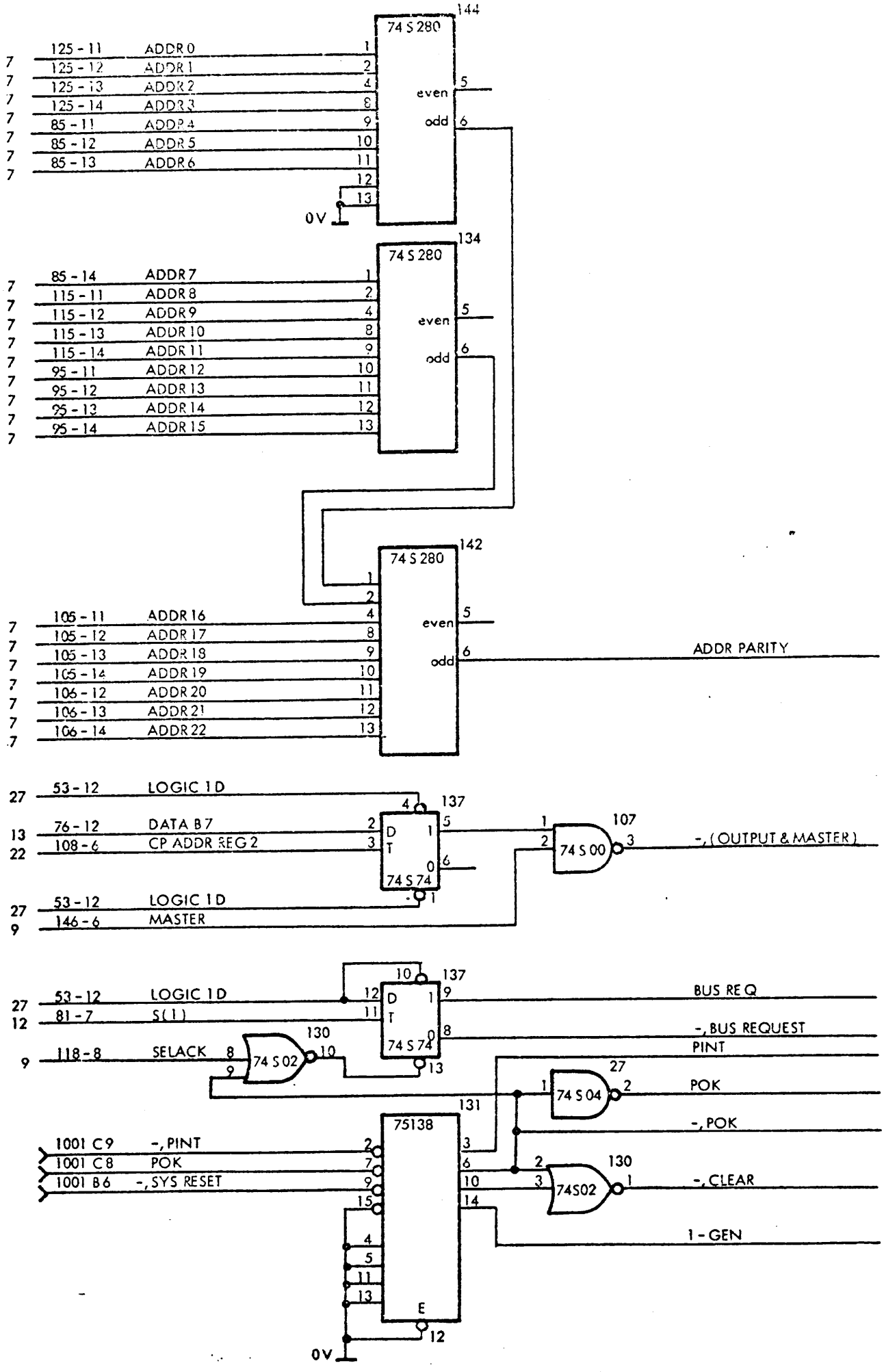

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SIGNAL	DESTI-NATION	DESCRIPTION
Com sel	P9	Selection signal from bus
Sel in	P9	Selection signal from bus. The controller may be selected when Com sel and Sel in are true.
-,ACK REC	P2	Inverse of ACK REC.
BUS BUSY	P9	The received Busy state from RC 8000 bus.
DRDY	P14	Strobe signal from another master on the RC 8000 Bus.
ACK REC	P9	Data acknowlege from a slave on RC 8000 bus.
NACK REC	P2, P9	Data not acknowledged from a slave on RC 8000 BUS (Bus parity error).
-,(ACK! NACK)	P9	The inverse of
ACK! NACK	P9	the bus transfer conclusion signal.
-,SEL OUT	P9	Selection signal propagated to next controller on RC 8000 BUS.
SEL ACK	P9	Selection signal accepted, bustransfer about to begin.
MASTER	P8,P9	BUStransfer to progress.
-,MASTER	P5	The inverse of MASTER
CPDATAREG	P1,P2	Delayed ACK!NACK or Time out.

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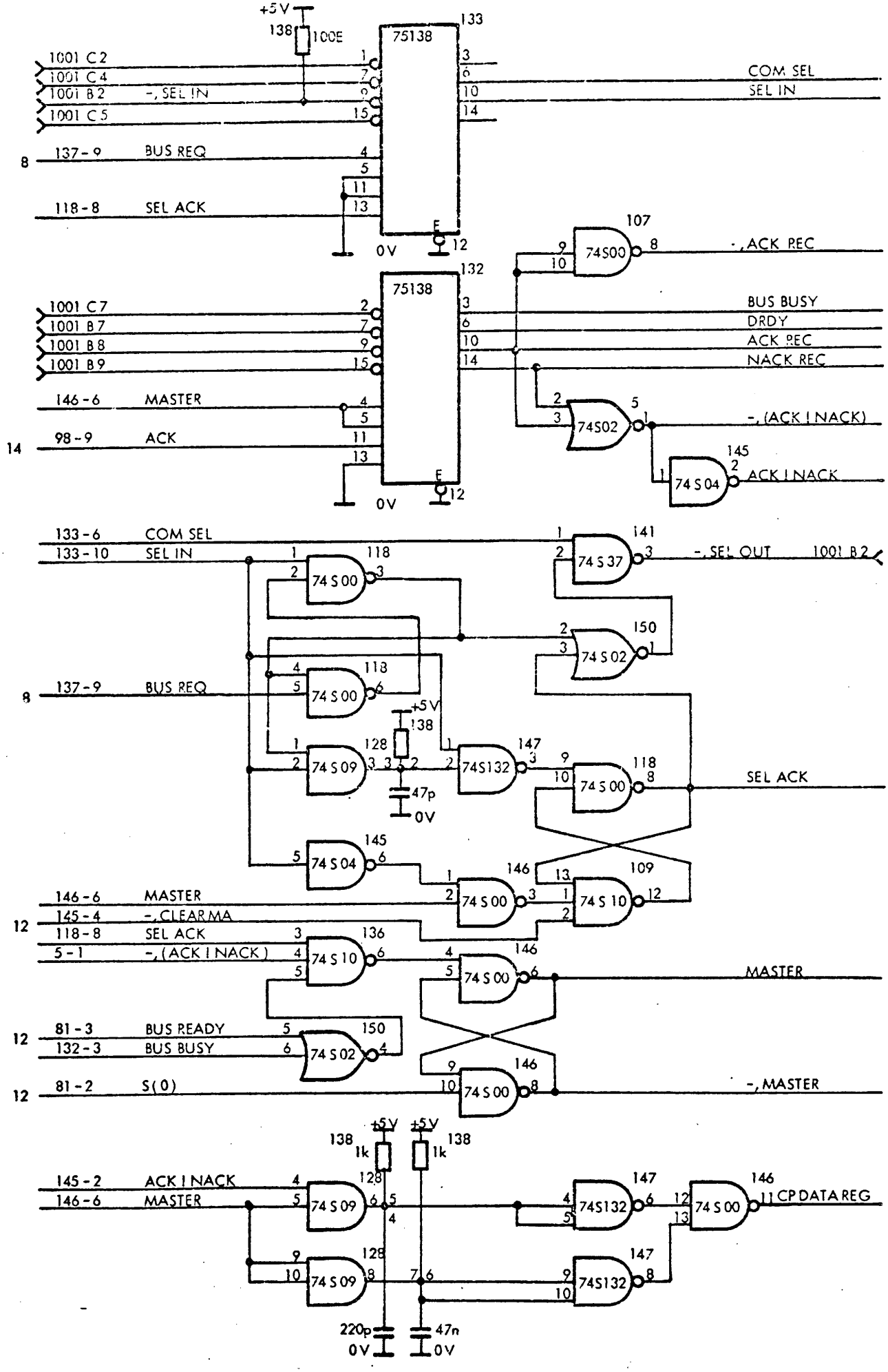

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SIGNAL	DESTI-NATION	DESCRIPTION
SUM 0:7	P13	Output from ALU
CARRY OUT	P24	Carry output from ALU on arithmetical operations. Used for microproprogram sequencing.
DATA C 0:7 B	P13	Part of DATA C BUS. Addressswitches and device selectors register to be gated on here.

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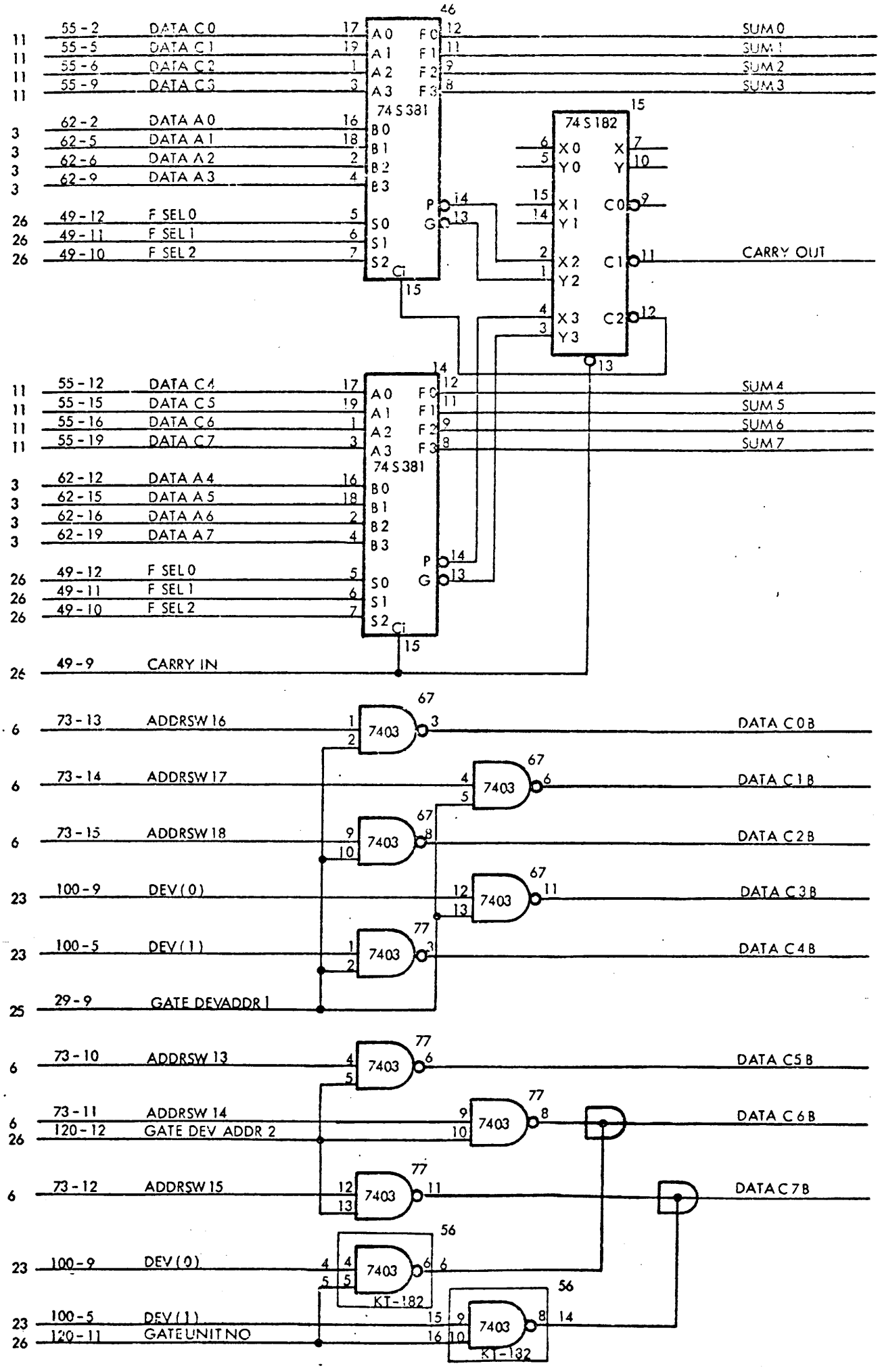

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R11664

ALU, C-SOURCE
LOGIC DIAGRAM

P10

SIGNAL	DESTI-NATION	DESCRIPTION
DATA C0:7	P10,P13	DATA C BUS amplified and in case of writing into RAM latched. Contains the selected Register/Ward. Used as operand on the ALU and as input to tag register.

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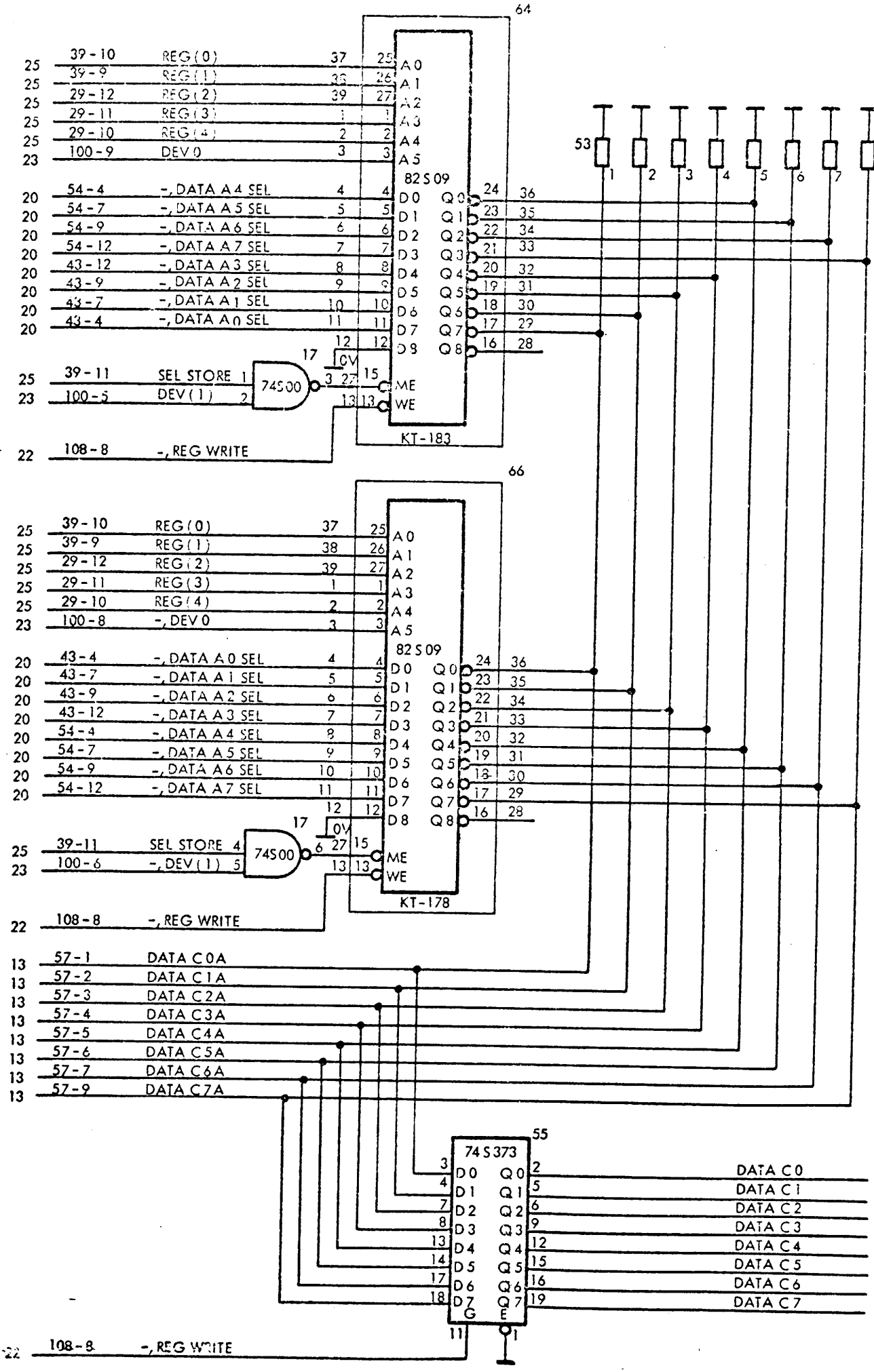

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R11665

MEMORY
LOGIC DIAGRAM

P11

SIGNAL	DESTI-NATION	DESCRIPTION
S(0)	P9,P12	Bit 0 in Bustransfer sequences. Enables bus transfer after selection. High during Bustransfer, i.e. Bus output data registers must be stable or bus input data registers are about to change.
BUSREADY	P9,P22	= -, S(0). Proceed signal to clockgenerator
S(1)	P8,P12	Bit 1 in Bustransfer sequences. Sets Busrequest flipflop.
S(0)*	P12	S(0) New value
S(1)*	P12	S(1) New value
SYNACK	P12	Synchronised Delayed Bustransfer conclusion signal.
-,SYNACK	P12	= not SYNACK
-,(SYNACK&RECYCLE)	P12	Condition together with and urgent for gang idle or setting busrequest immediately.
-,Clear MA	P12 P9, P21, P23	Clear Microprogramaddress register if Master clear or clockpulse time out.
MCLEAR	P12 P22	Masterclear signal. Conditioned by Send tag.

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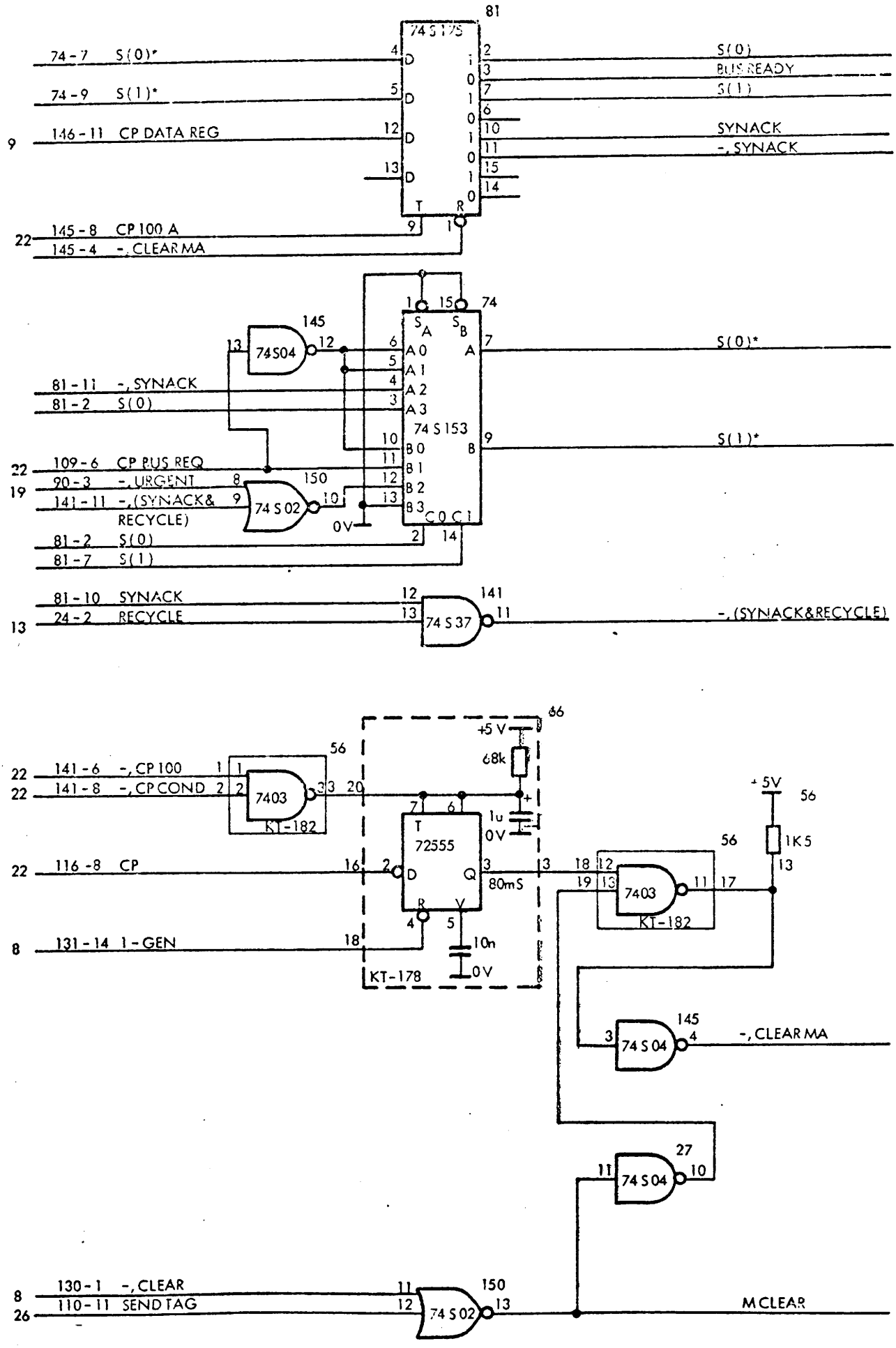

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SIGNAL	DESTI-NATION	DESCRIPTION
-,ZERO	P24	Low when ALU-output equals zero. Used for microprogram sequencing.
DATA B 0:7	P2 P4, P7	DATA B BUS
RECYCLE	P12, P17	Signal to Discadaptor requesting 16 more bytes read or written.
READ	P19 P20	Redundant Tagcode bit meaning Readcommand to Disc adaptor
READ! WRITE	P19	Redundant tagcode bit meaning Read- or Write-command to Disc adaptor.
TAG PARITY, TAG 0:3	P16	Tagcode with odd parity to be transmitted to Disc adaptor.
DATA C 0:7 A		Part of DATA C-BUS sources. On this page constant store.

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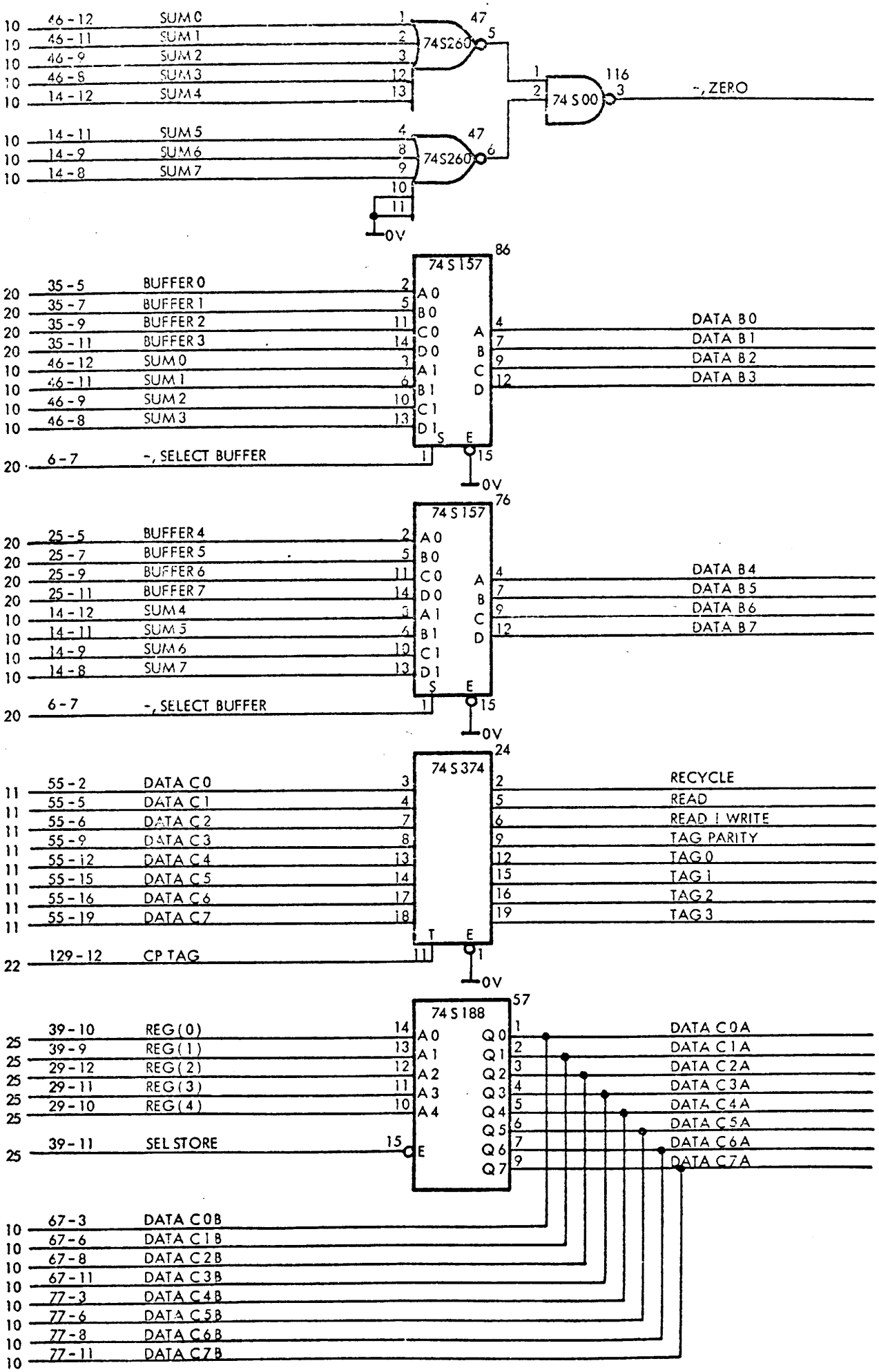

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SIGNAL	DESTI-NATION	DESCRIPTION
-,CLEAR COMM	P14	Clears start- or reset-command for current device.
RESET	P23	Reset command to current device. Resets microprogramaddress register.
START	P24	START command to current device. Used for sequencing microprogram.
-, DEVICE PRESENT	P14	Low if controller is addressed and a zero bit is stored in the addressed "device present"-RAM location.
-,DEV ADDR SYNC	P14	Synchronized "addressed" and strobed from RC 8000 bus. Stores a Start- or Reset-command.
ACK	P9	Acknowledge for addressing to be sent to Busmaster.

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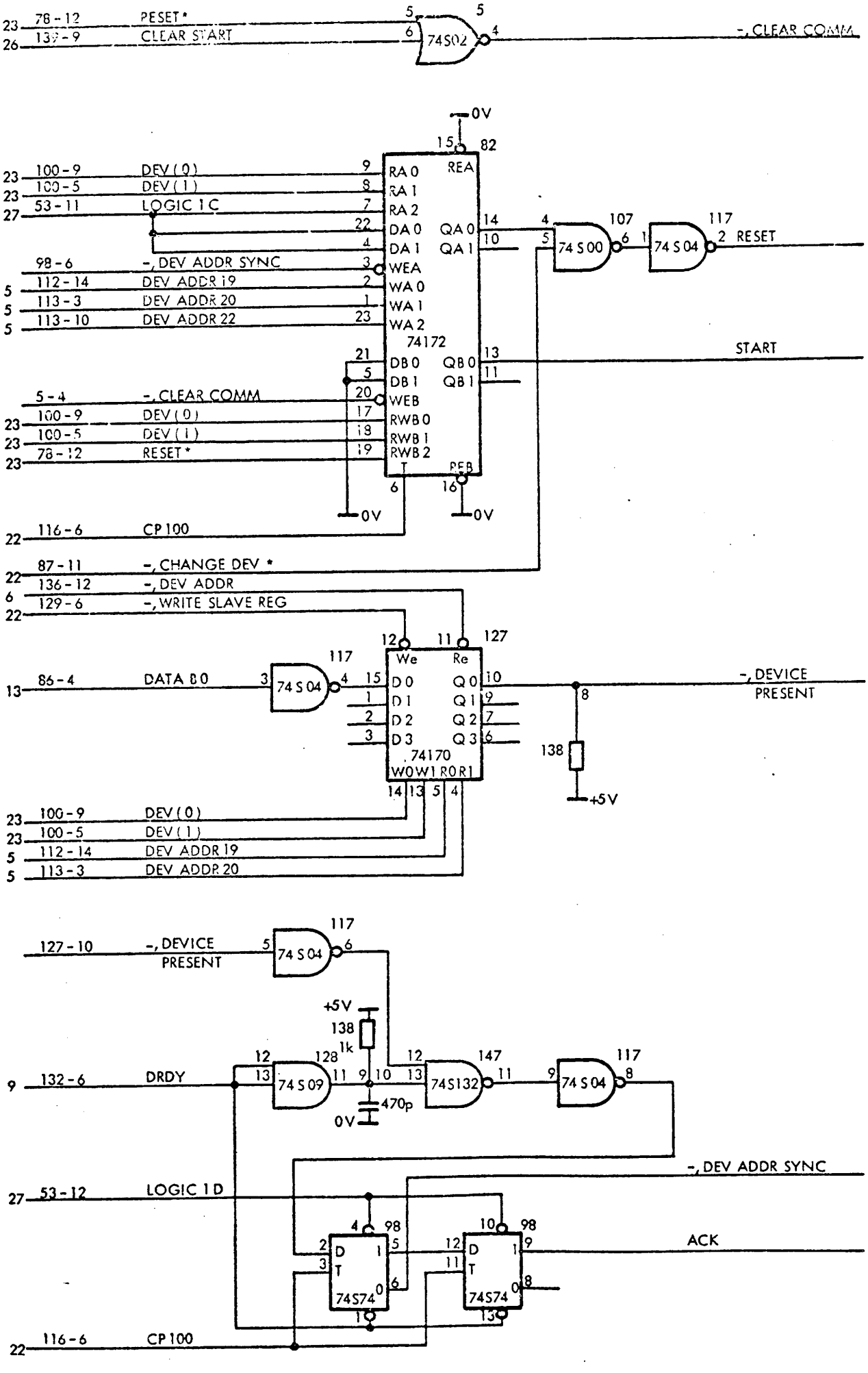

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R11668

START/RESET CIRCUIT
LOGIC DIAGRAM

P 14

SIGNAL	DESTI-NATION	DESCRIPTION
BUSOUT 0:7	DSA	Databyte or command specifier to Disc adaptor.

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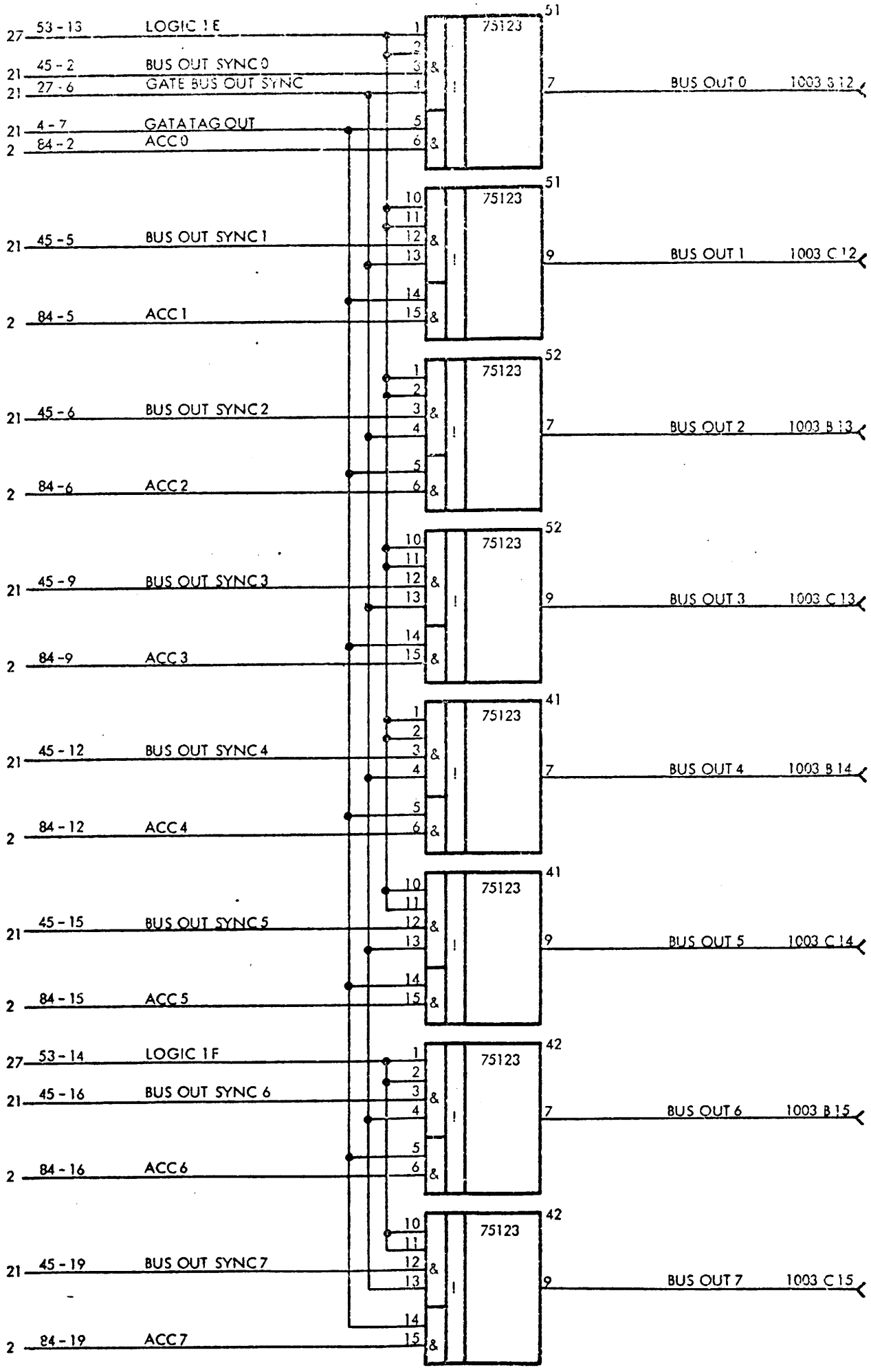

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SIGNAL	DESTI-NATION	DESCRIPTION
BUS OUT PARITY	DSA	Odd parity bit for BUS OUT 0:7
TAG BUS 0:3		
TAG BUS PARITY	DSA	Tag command with odd parity to Disc adaptor.
TAG OUT XMT	DSA	Signal to Discadaptor meaning that a Tag command is available on Tag bus and Bus out.
SYNC OUT	DSA	Signal to Discadaptor meaning write data available on bus out or read data accepted on bus in.

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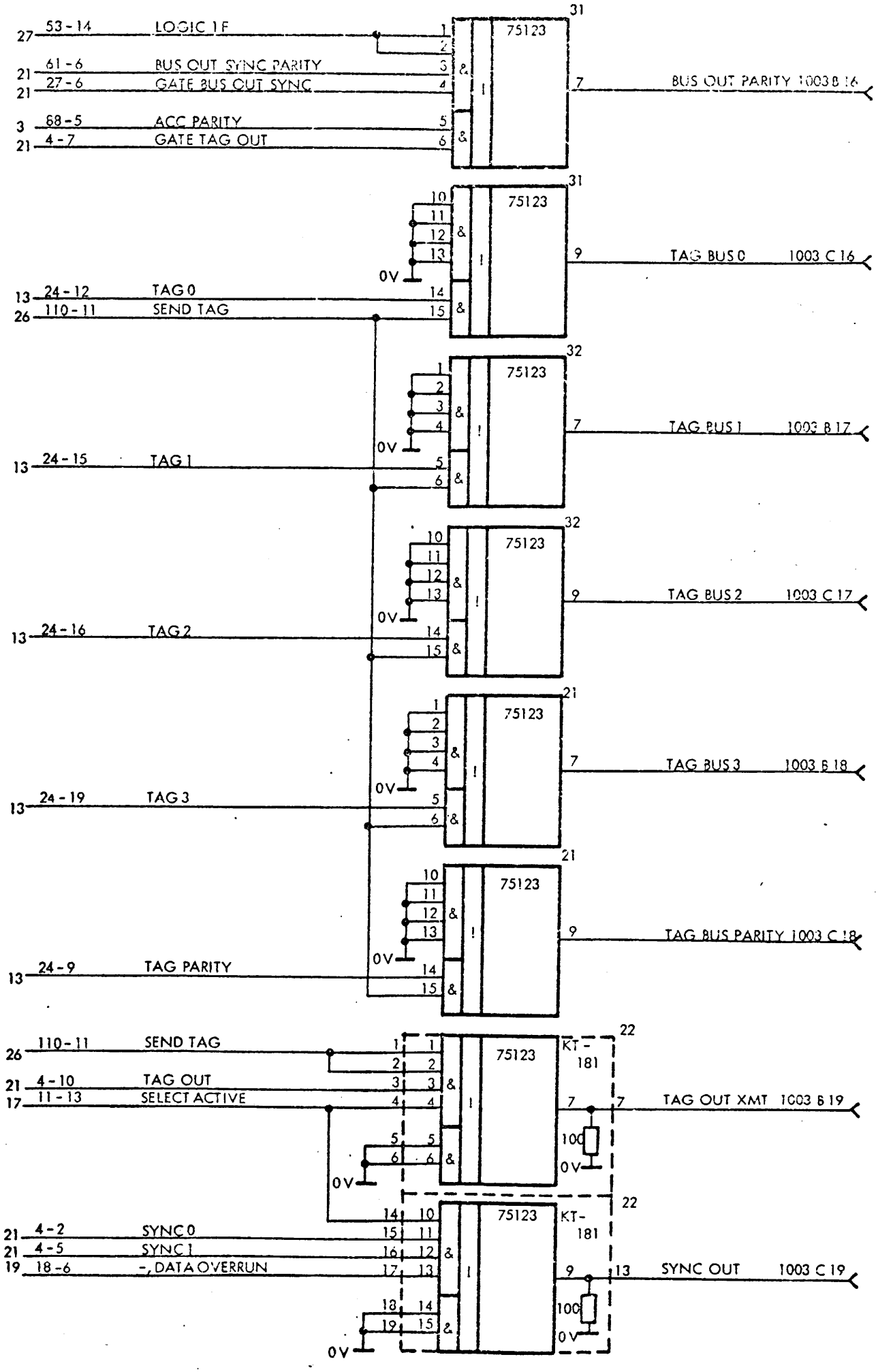

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SIGNAL	DESTI-NATION	DESCRIPTION
SELECT HOLD	DSA	Logic one on the select line to the Discadaptor.
RESPONSE XMT	DSA	Signal sent to Discadaptor as response on CHECKEND or NORMAL END.
SELECT ACTIVE	P16	Signal from DSA meaning Discadaptor connected and ready to receive TAG commands.
BUS IN 0:4	P20, P21	Input lines from Disc adaptor carrying data or status.

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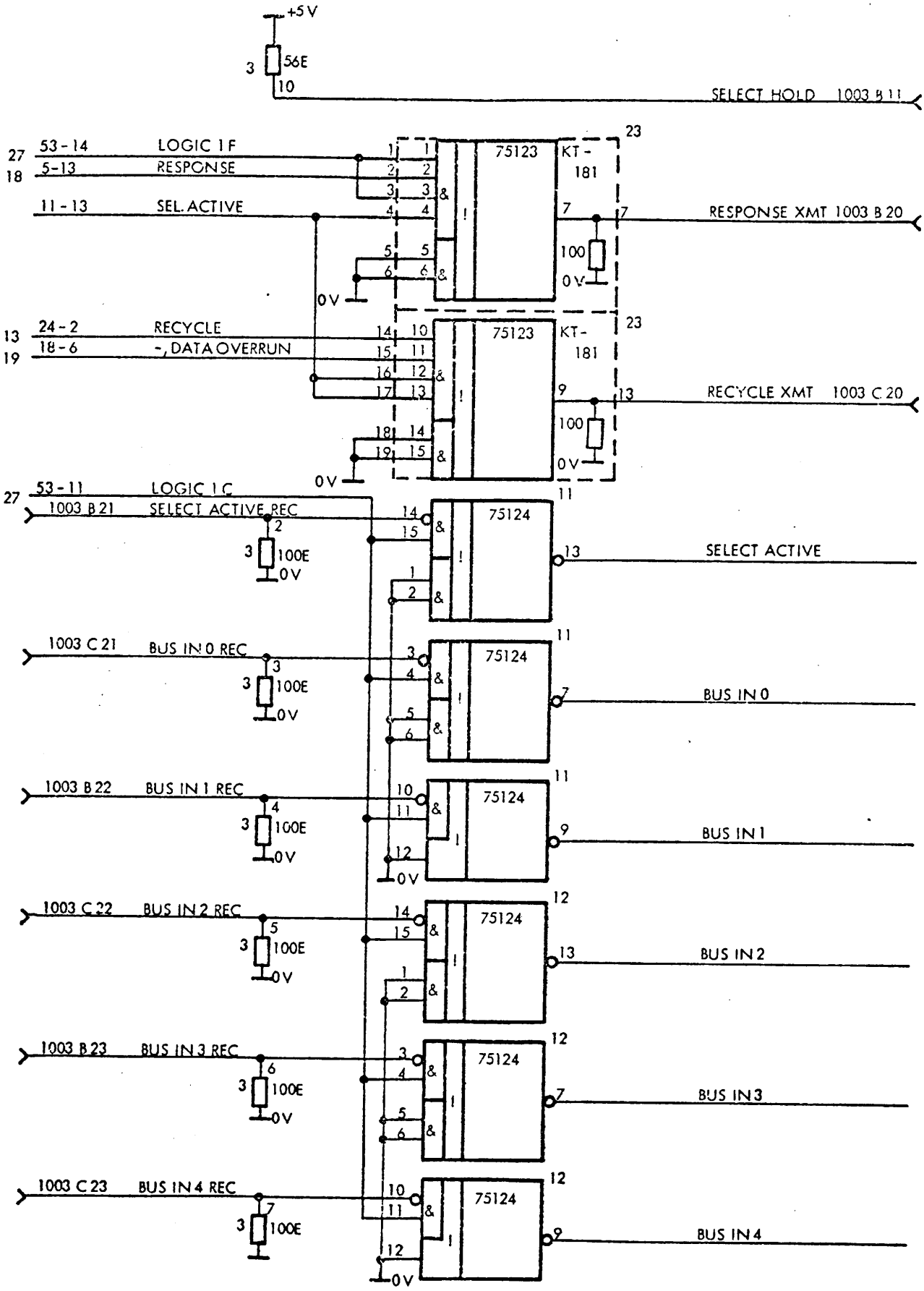

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SIGNAL	DESTI-NATION	DESCRIPTION
BUS IN S:7	P20 P21	Inputlines from Discadaptor carrying data or status.
-,CHECKEND	P18	CHECKEND inverted.
DA INT	P24	Signal from Discadaptor going high when selected sector arrives under the read/ write heads of one of the connected drives. Used for microprogram sequencing.
TAG VALID ! CHECKEND & SEND TAG	P18	Conclusion signal for first phase of a Tag command sequence.
SYNCIN	P19 P21	Signal from Disc adaptor meaning that write data is requested on BUSOUT or read data is available on BUS IN lines.
NORMAL ! CHECKEND & BUS IN LATCH	P18	Tag command sequence conclusion signal.
CHECKEND	P18 P19 P21	Tag command sequence conclusion signal indicationg an error.
HANDSHAKE	P21	Signal meaning that a Tag command is being executed, necessary for cleaning up after master reset.
-,BUS IN LATCH	P18	Latched BUSIN control signal from microprogram. Generates:
RESPONCE	P17 P18	Refer to RESPONCE XMT on Page 17.

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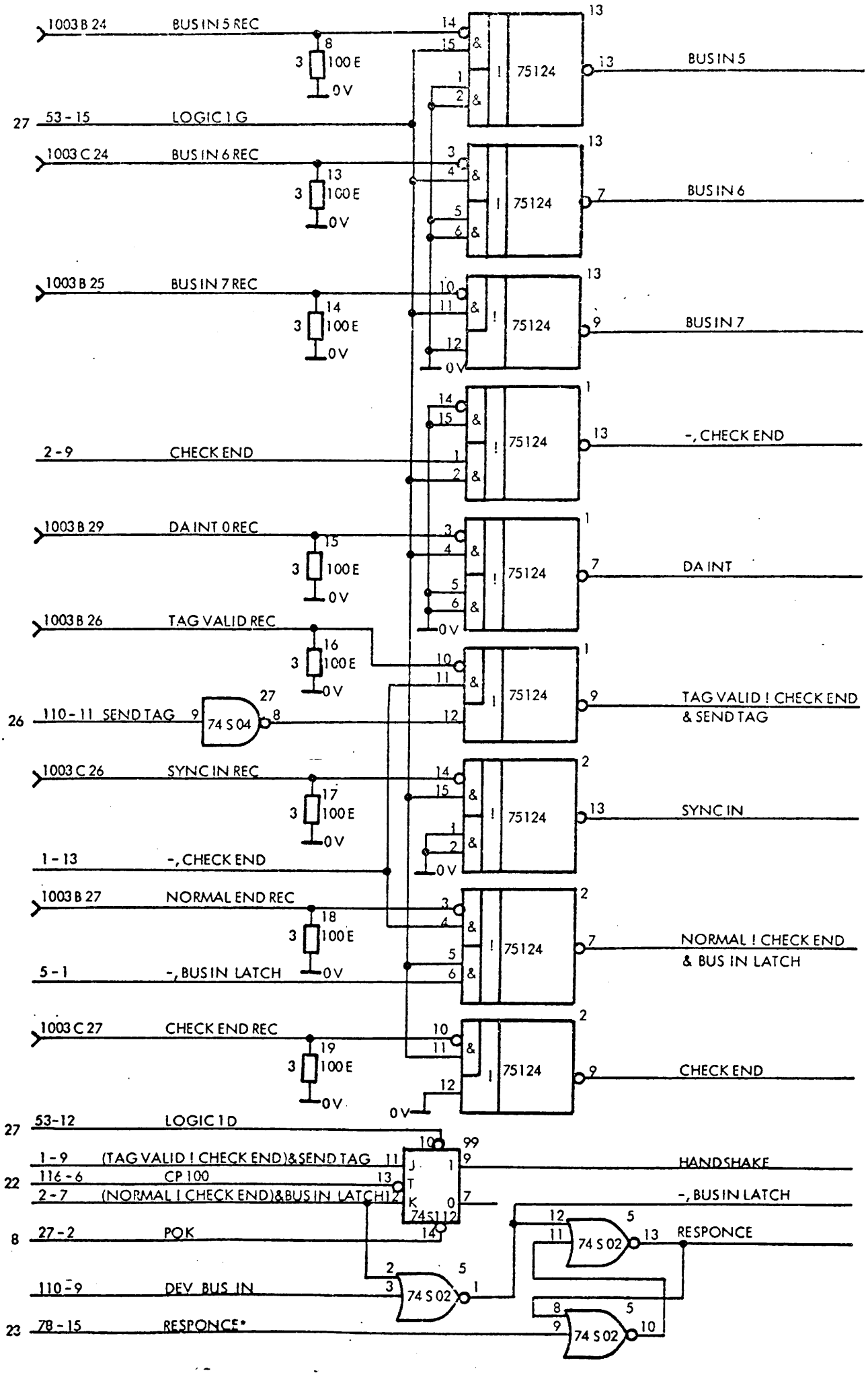

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SIGNAL	DESTI-NATION	DESCRIPTION
ACCESS 1	P19 P20 P22	Fifo buffer control signal indicating that microprogram has access in the Fifo buffer.
-,ACCESS 1	P20	
-,DATA OVERRUN	P16 P17 P19	Goes low if Sync in arrives, and the Fifo buffer is not able to accept or deliver a data byte (buffer is resp. full or empty). Inhibits Sync out in response to the Sync in, thus making the DSA create the proper status bit for later sensing.
-,CHECKENDSYNC	P19	Syncronized value of CHECKEND.
-,BUFFERADDR 0:3	P20	Address to Fifo buffer RAM
BUFFERHALF	P19 P24	Indicates that the buffer is more than half full when writing and less than half full when ready. Used by microprogram for proper reset of RECYCLE line.
-,I READY	P19	Indicates when high, that buffer is empty on read, and buffer is full on write.
-, II READY	P19	Indicates when high that buffer is empty on write and buffer is full on read.

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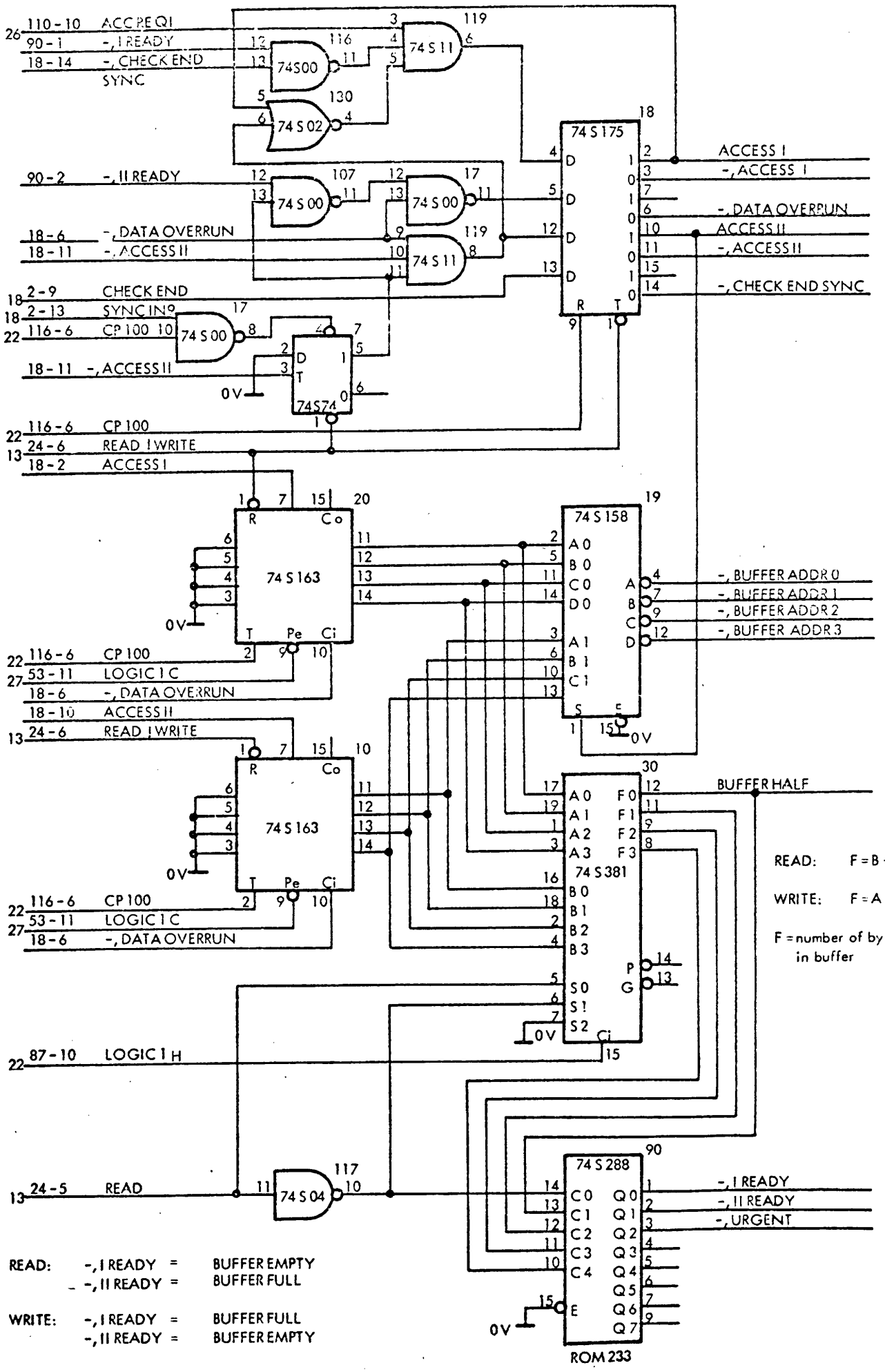

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SIGNAL	DESTI-NATION	DESCRIPTION
-,Write buffer	P20	Write enable to FIFO buffer RAM
-,Select buffer	P13	High on Read and ACCESS 1. Used for routing buffer output to DATA B BUS.
-,DATA A 0:7 SEL	P11	Selector output to Register store input.
BUFFER 0:7	P13 P21	Fifo buffer output

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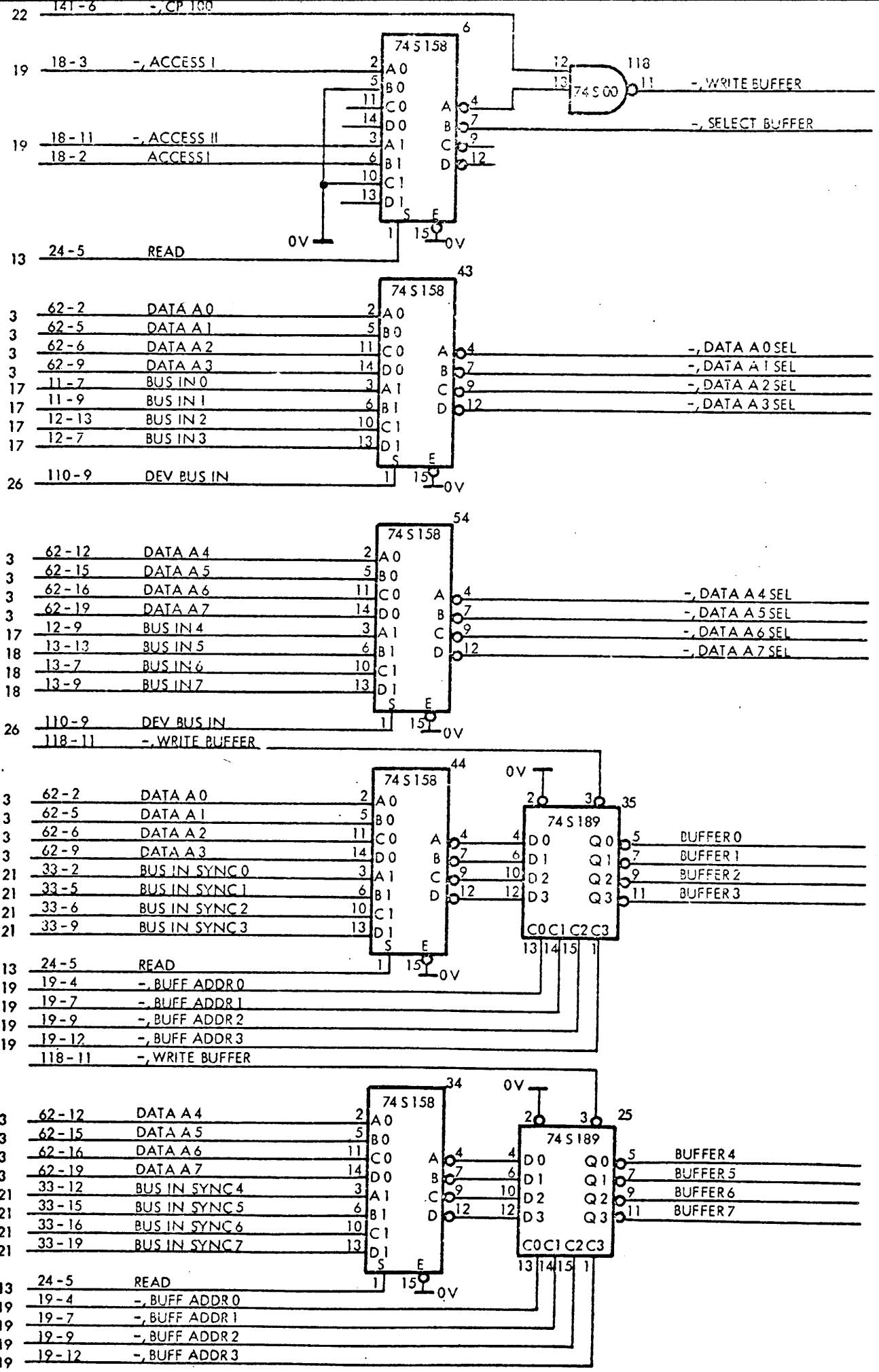

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R11674

FIFO, MEMORY INPUT SELECTOR
LOGIC DIAGRAM

P 20

SIGNAL	DESTI-NATION	DESCRIPTION
BUS IN SYNC 0:7	P20	Latched read-data from Disc adaptor.
BUS OUT SYNC 0:7,	P15,P21	Write data to Disc adaptor
BUS OUT SYNC PARITY	P21	with odd parity.
GATE BUS OUT SYNC	P15, P21	Gates BUS OUT SYNC to BUS OUT 100 ns before 100 ns after Sync out.
SYNC 0,		Signals for generating.
SYNC 1	P21,P16	Sync out pulses.
GATE TAG OUT	P21,P15 P16	Gates tag command on BUS OUT to DSA
TAG OUT	P16	Tag strobe to DSA
-,DISCEND	P21 P22	Low, when Tag command is accepted and still being executed.
DISCEND	P22	High when -,DISCEND LOW
		These signals are used as Proceed-signals to clock generator.
ERROR	P24	Conditional branch. If an error indicator is selected by microprogram, and the actual value is true, the two least significant bits in Next Microprogram Address (Next MP ADDR 7:8) are forced to disregard their programmed values.

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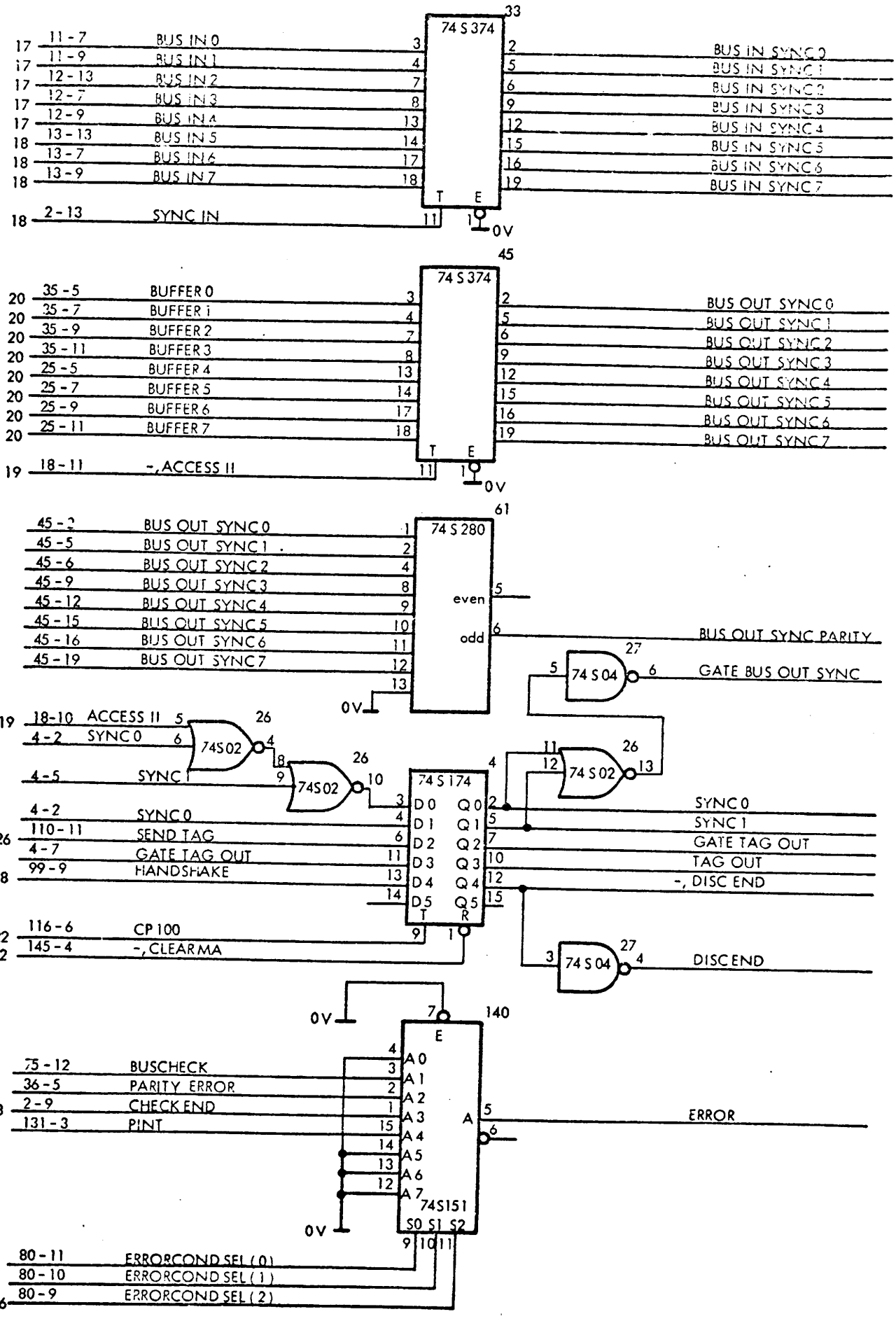

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SIGNAL	DESTI-NATION	DESCRIPTION
-,CP100	P22,P12	Masterclock, 10 MH_z from which all clocks, load functions and write enables are derived after the delay of one logic level (inversion after and). Except for certain synchronation flip flops, all clock times are the negative edge of this signal delayed.
-,CP COND	P22,P12	Condition signal excluding at least every second of the master clock pulses.
CP 100	P14,P18 P19,P11 P22	Freerunning version of Masterclock. Inverted. Used for synchronization purposes.
CP	P7, P12, P23	System clock defining end of a micro-instruction.
CP ACC	P2, P3	Load Accumulator pulse.
CP ADDR REG2	P8	Load Address register 2-pulse.
-,REG Write	P11	Write enable to Register store.
CP TAG	P13	Load Tag register pulse.
CP 100 A	P12	See CP100
CP DEV CNT	P23	Clock to Device number counter.
-,Write Slave REG	P14	Load Device present bit in slave register.

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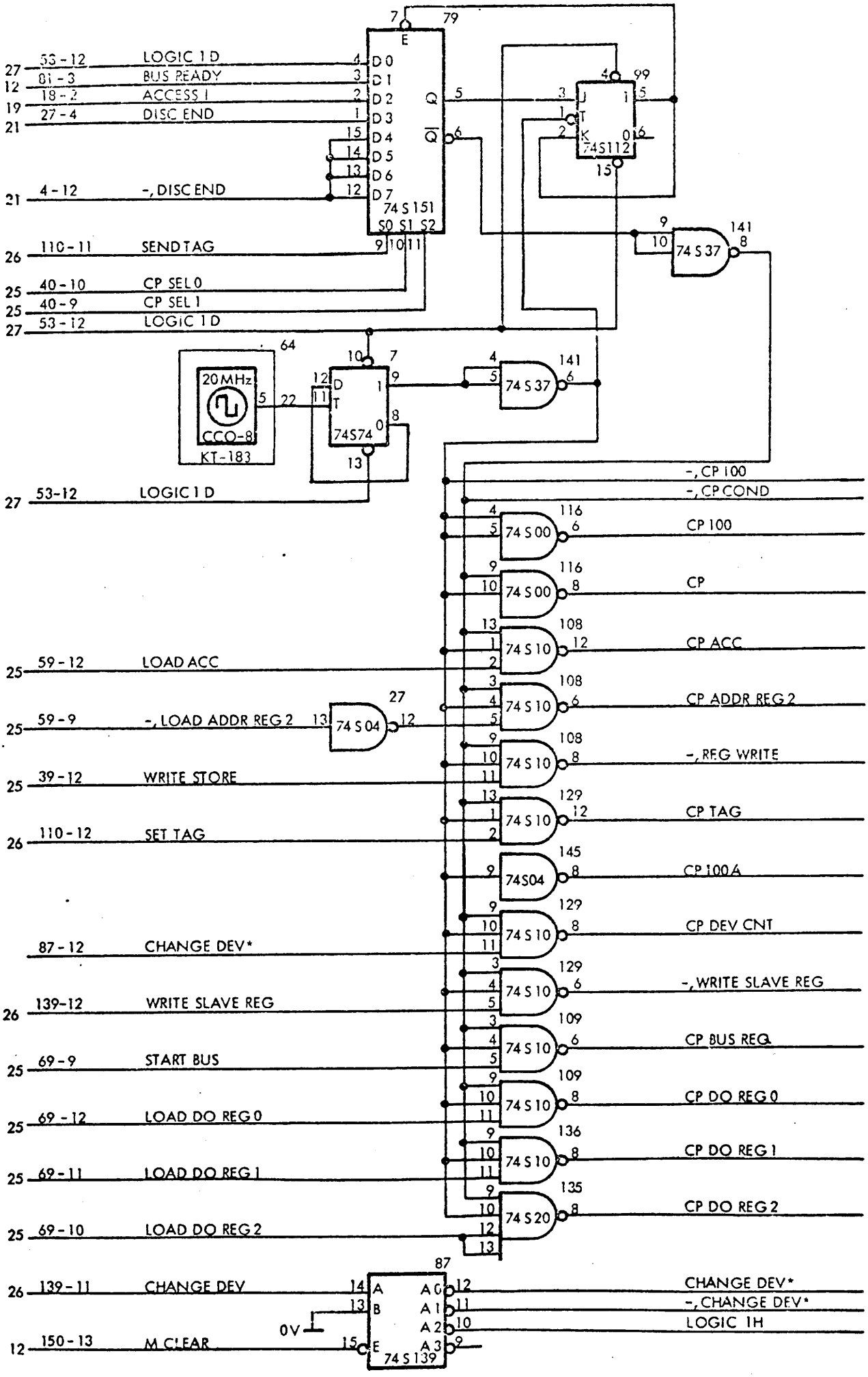

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R11676

CLOCKGENERATOR CIRCUIT
LOGIC DIAGRAM

P 22

SIGNAL	DESTI-NATION	DESCRIPTION
CP BUS REG	P12	Clock bus request flip flop
CP DO REG 0:2	P4	Load Data out registers 0:2, pulses.
CHANGEDEV*	P22	Enables CP DEV CNT this side Selects.
-,CHANGEDEV*	P23	Saved return microaddress for next device. Both high when Master cleared.

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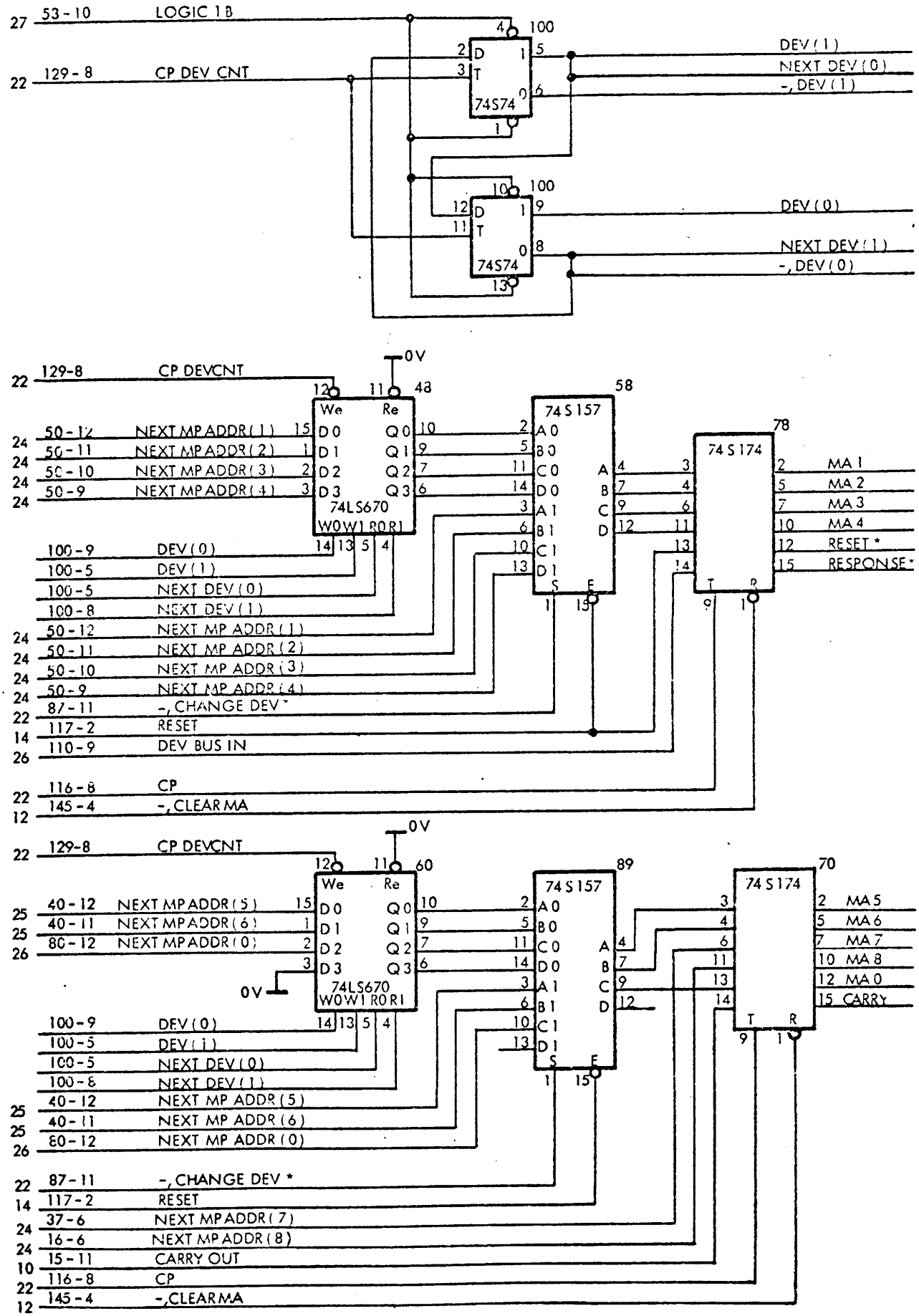
27 53-10 LOGIC 1B
22 129-8 CP DEV CNT
74S74
100
DEV(1)
NEXT DEV(0)
-,DEV(1)
DEV(0)
NEXT DEV(1)
-,DEV(0)
22 129-8 CP DEVCNT
0V
74LS670
W0W1R0R1
74S157
74S174
58
78
48
24 50-12 NEXT MP ADDR(1)
24 50-11 NEXT MP ADDR(2)
24 50-10 NEXT MP ADDR(3)
24 50-9 NEXT MP ADDR(4)
100-9 DEV(0)
100-5 DEV(1)
100-5 NEXT DEV(0)
100-8 NEXT DEV(1)
24 50-12 NEXT MP ADDR(1)
24 50-11 NEXT MP ADDR(2)
24 50-10 NEXT MP ADDR(3)
24 50-9 NEXT MP ADDR(4)
22 87-11 -,CHANGE DEV*
14 117-2 RESET
26 110-9 DEV BUS IN
22 116-8 CP
12 145-4 -,CLEAR MA
MA1
MA2
MA3
MA4
RESET*
RESPONSE*
22 129-8 CP DEVCNT
0V
74LS670
W0W1R0R1
74S157
74S174
60
89
70
25 40-12 NEXT MP ADDR(5)
25 40-11 NEXT MP ADDR(6)
26 80-12 NEXT MP ADDR(0)
0V
100-9 DEV(0)
100-5 DEV(1)
100-5 NEXT DEV(0)
100-8 NEXT DEV(1)
25 40-12 NEXT MP ADDR(5)
25 40-11 NEXT MP ADDR(6)
26 80-12 NEXT MP ADDR(0)
22 87-11 -,CHANGE DEV*
14 117-2 RESET
24 37-6 NEXT MP ADDR(7)
24 16-6 NEXT MP ADDR(8)
10 15-11 CARRY OUT
22 116-8 CP
12 145-4 -,CLEAR MA
MA5
MA6
MA7
MA8
MA0
CARRY
761111 PKA 761111ERC

SIGNAL	DESTI-NATION	DESCRIPTION
DEV (0:1)	P10,P11 P14, P23	Output of Device number counter counts in the order (00 01 11 10)
NEXT DEV(0:1)	P23	Indicates next device number in the sequence.
-,DEV (0:1)	P11	the inverse of DEV(0:1)
MA0:8	P24,P25 P26	Microprogram address.
RESET*	P14	Synchronized RESET Command.
RESPONSE*	P18	RESPONSE Signal to DSA.
CARRY		Delayed Carryoutput from ALU.

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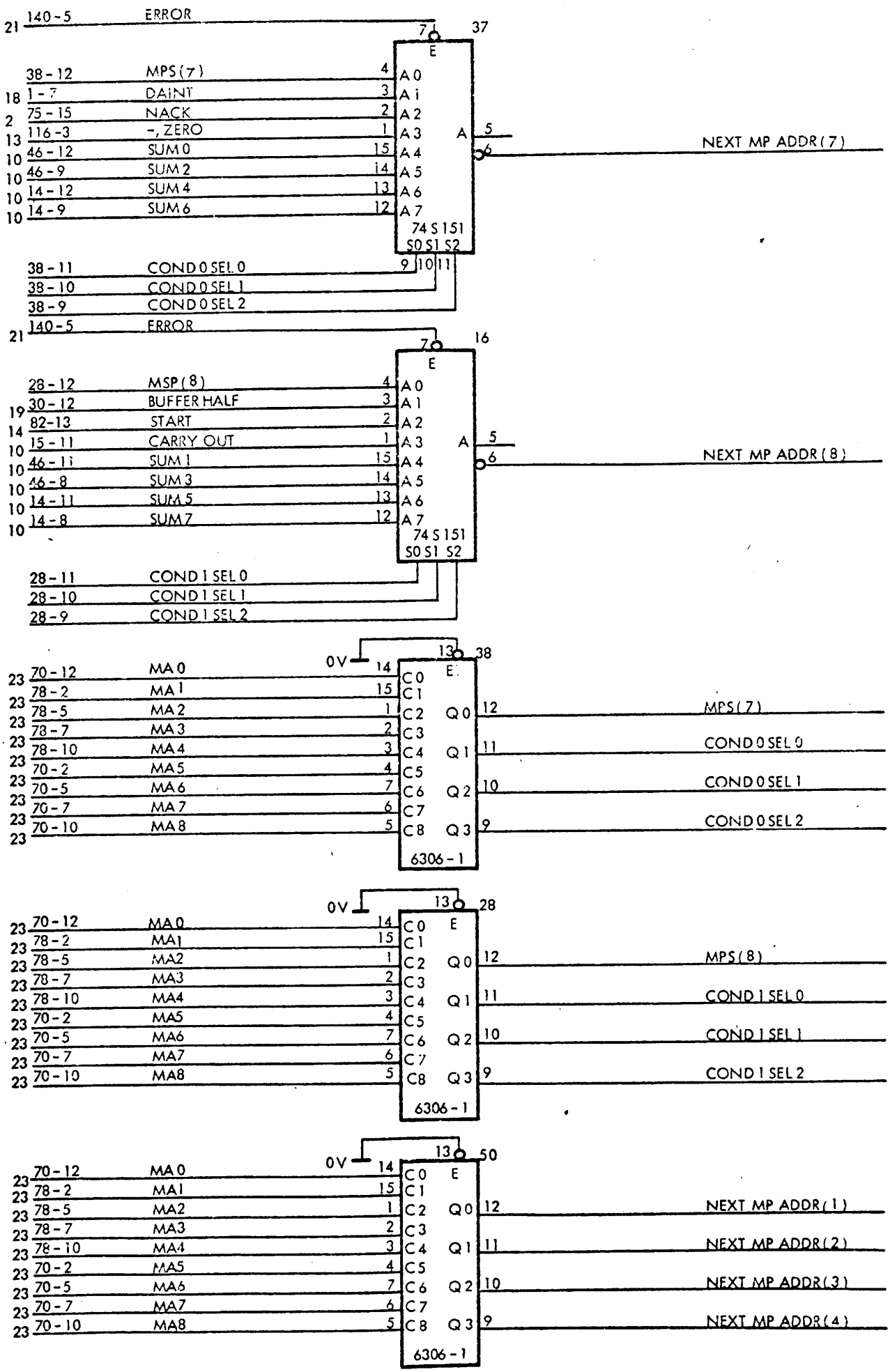

761111 ERC

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SIGNAL	DESTI-NATION	DESCRIPTION
Next MPADDR (7:8)	P23	Least significant bits in next micro instruction address field, used for conditional branching.
MPS 7, MPS 8	P24	Defines NEXT MP ADDR (7:8) when not conditioned.
COND0SEL0:2, COND1SEL0:2	P24	Selects branch conditions
NEXT MPADDR (1:4)	P23	Direct branch address bits.

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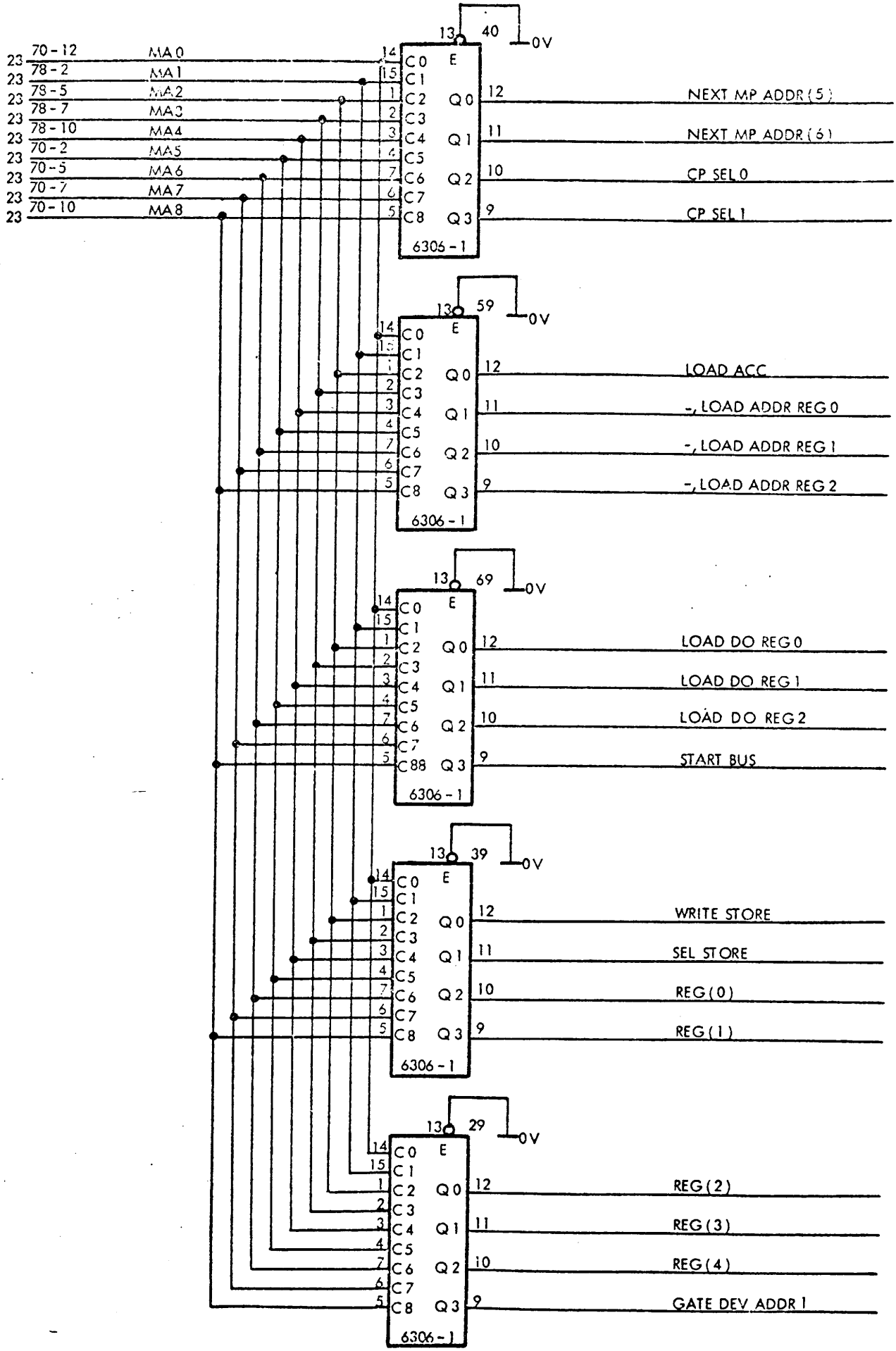

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SIGNAL	DESTI-NATION	DESCRIPTION
NEXT MPADDR (5:6)	P23	Direct branch address bits.
CPSEL 0:1	P22	Selection of proceed condition.
LOAD ACC	P22	Load ACC command.
-,LOAD ADDR REG(0:2)	P7, P22	Load Commands to Busaddress registers.
LOAD DO REG (0:2)	P22	Load Commands to Data out registers.
START BUS	P22	Start Command to bus logic.
Write store	P22	Generate write pulse to register store.
Sel store	P11, P13	Select Register store or constant store.
REG(0:4)	P11,P13	Address to Register or constant store.
Gate dev addr 1	P10	Gate part 1 of address switches and device number on BASTA B bus.

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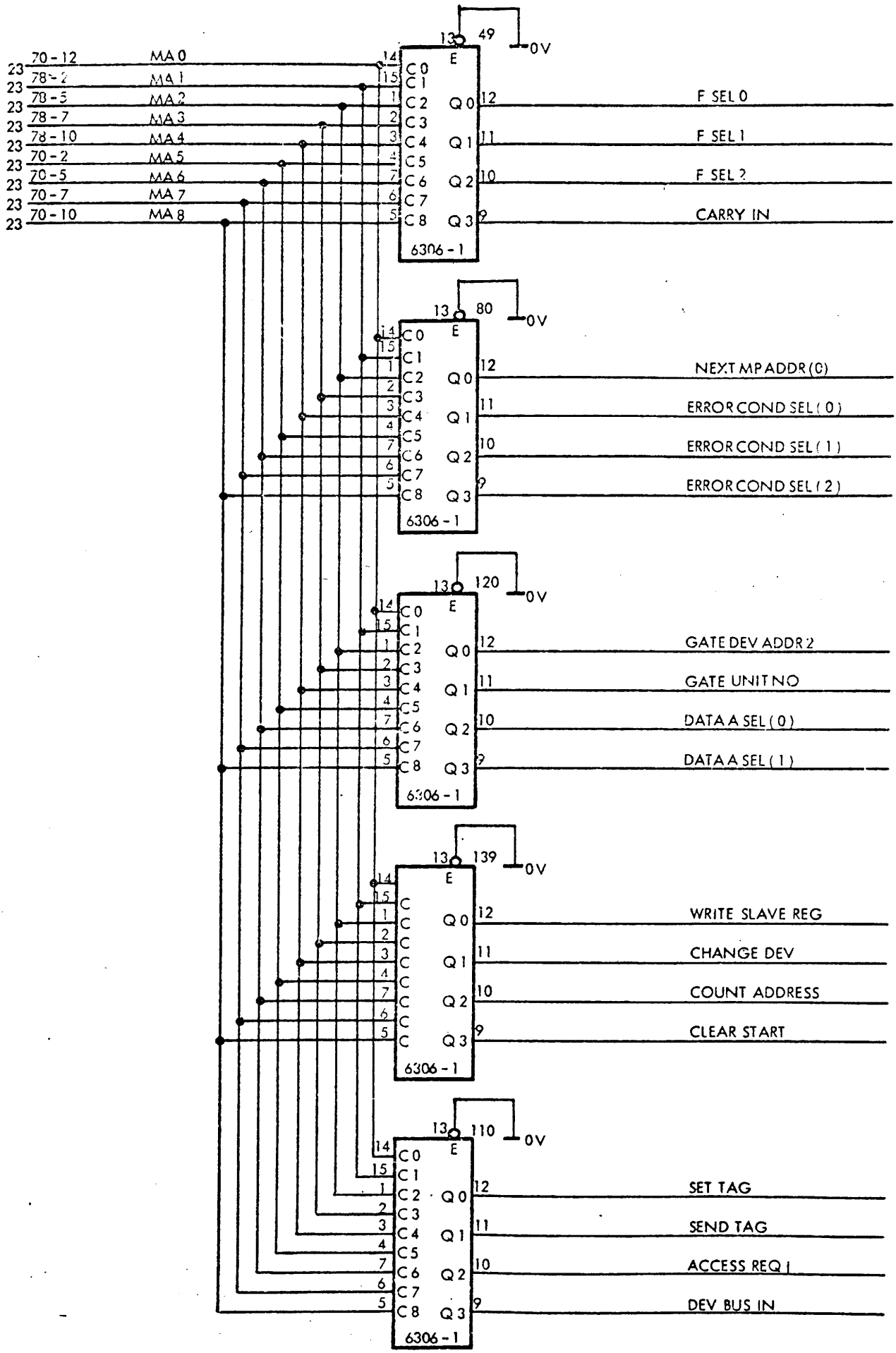
70-12 MA0
78-2 MA1
78-5 MA2
78-7 MA3
78-10 MA4
70-2 MA5
70-5 MA6
70-7 MA7
70-10 MA8
23
6306-1
F SEL 0
F SEL 1
F SEL 2
CARRY IN
NEXT MP ADDR (0)
ERROR COND SEL (0)
ERROR COND SEL (1)
ERROR COND SEL (2)
GATE DEV ADDR 2
GATE UNIT NO
DATA A SEL (0)
DATA A SEL (1)
WRITE SLAVE REG
CHANGE DEV
COUNT ADDRESS
CLEAR START
SET TAG
SEND TAG
ACCESS REQ 1
DEV BUS IN
0V

SIGNAL	DESTI-NATION	DESCRIPTION
F SEL 0:2,		
Carry in	P10	ALU control.
NEXT MPADDR (0)	P23	Most significant direct branch address bit.
Error card sel (0:2)	P21	Select error branch condition
GATE DEV ADDR 2	P10	Gates part 2 of address switches on DATA B bus.
GATE UNIT NO	P10	Gates Driveunit no. (DEV(0:1)) with unit in bit 7 on DATA B bus.
DATA A SEL(0:1)	P1, P2 P3	Select source on DATA A tristate bus.
WRITE SLAVE REG	P22	Write command to device present slave register.
CHANGE DEV	P22	Command to let next drive process take over.
Count address	P7	Count command to Bus address register/ counter.
Clear Start	P14	Clear Start command bit
SET TAG	P22	Load tag register command
SEND TAG	P21	Send tag to DSA command
ACCESS REQ 1	P19	Gain access to FIFO buffer.
DEV BUS IN	P18, P20 P23	Select BUS IN from DSA as input data to Registerstore and acknowledge Tag command termination.

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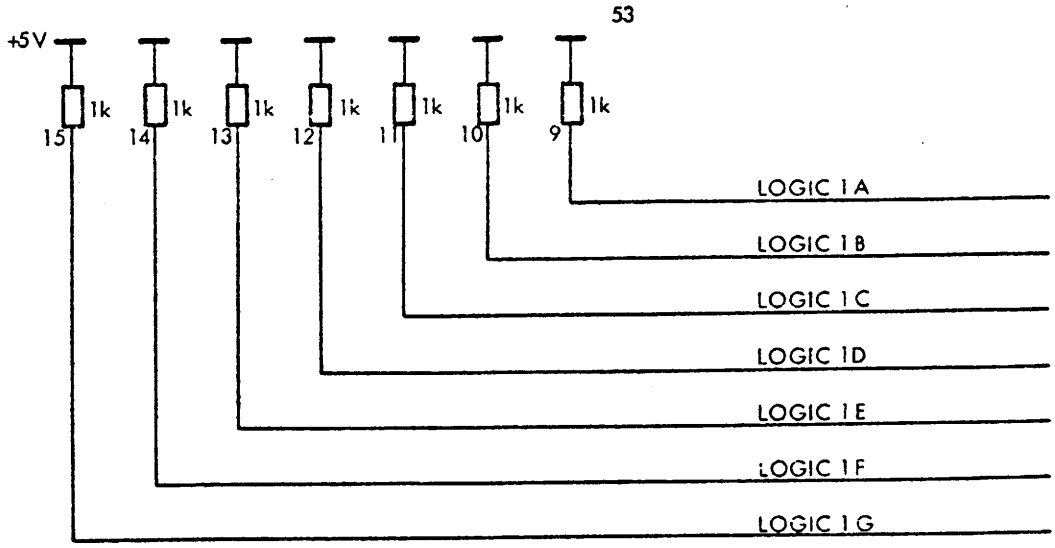

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