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Title:

DSC 801
Technical Description

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Abstract:

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1. General 1.

The Disc Storage Controller is a microprogrammed link between RC8000 mainstorage and the adapter DSA 801, which converts a channel program written in standard form in mainstorage into the proper sequences at commands to the adapter and the drives, transfers data between mainstorage and DSA, and keeps the RC8000 software informed about the state of the system.

The individual drives are controlled by their own channelprogram, timesharing the DSA and the DSC.

The microprogram in the DSC is a reentrant program with four incarnations and four sets of registers, one for each drive maintaining control of the whole channel except the registers belonging to the other three coroutines, until one of the waitingpoints is reached.

When a coroutine arrives to a waiting point, it executes a "change device"-command, which saves the next-micropramaddress indicated in the command, switches over to the registerset of the next coroutine in a permanent "round robin" queue and proceeds in the microprogram address saved for this coroutine.

The microinstruction time is 200 ns except when waiting for an external event such as RC8000 - bustransfer finished or disc command accepted, where the time is prolonged with an integer multiple of 100 nSec.

2. Datapathes 2.

The DSC 801 Controller consists of the datapathes shown in the block diagram (dwg no. P11682).

Data is lead from RC8000 main storage to the 16 byte FIFO buffer via Bus receivers, input registers and the A bus, or from the FIFO buffer via outputregisters and bustransmitters to the mainstorage. This part of the dataflow is controlled by the microprogram, while data between the FIFIO buffer and the DISC Adapter is controlled by the discadapter syncpulses, both during reading and writing. The microprogramcontrolled part of the FIFO is on the diagrams identified by "access I"- Signals, while the signalnames derived from "access II" all designate adapter control of the FIFO.

The Register store is a 4 x 32 bytes RAM, where the unitnumber counter (dev (0:1)) is used as an index address (32 bytes per unit). This store is used by microprogram for storing core addresses, bytecounts channel-program-counter, -commands and -parameters, and statusinformation.

3. Control pathes 3.

The DSC 801 is controlled by a microprogram, which in turn is controlled by a microprogramcontroller, shown in the blockdiagram dwg. no. R 11966.

The microprogramstore is a 512 words by 52 bits table entered by a microprogramaddress, latched in a m.p. addressregister. This register may be considered as the machinestateregister.

The output of the microprogramstore controles the machine : 7 output bits define seven of the next state (m.p. address), and 11 bits are used to condition the last two m.p. address bits.

Two outputs define which internal or external event should activate the next systemclockpulse. The systemclockpulses define the moments of stateshifts.

The remaining 32 outputlines control the dataregisters, datapathes and the ALU.

A special controle lmc "change device" hands the control over to another microprocess, that is the same microprogram run with another set of variables and perhaps in another phase. As function of a command on this lmc, the controller saves the current next microprogramaddress, switches to the variables of the next process, fetches the saved m.p. address for this process and continues in this address.

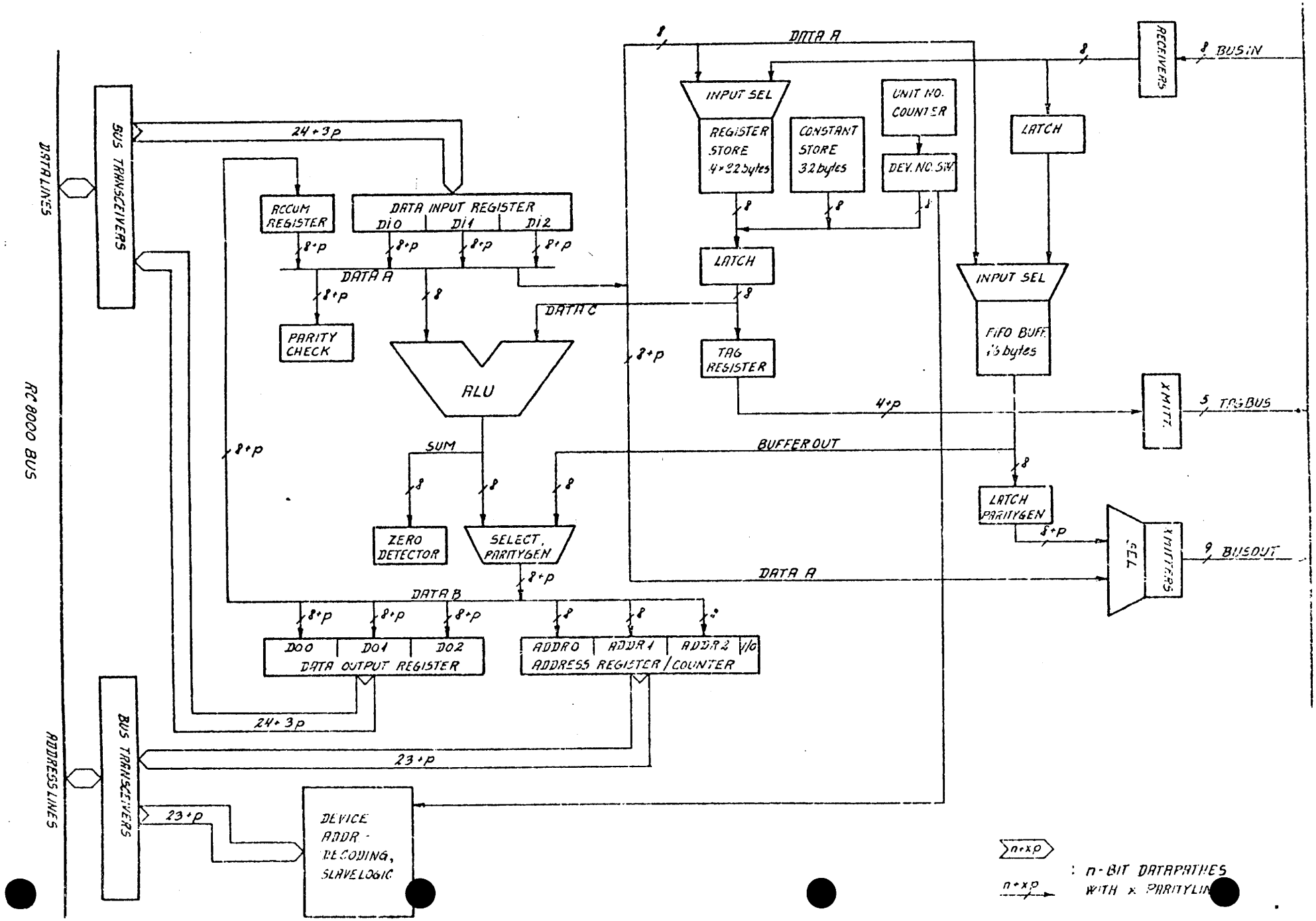
761004 PKA 761004 A03

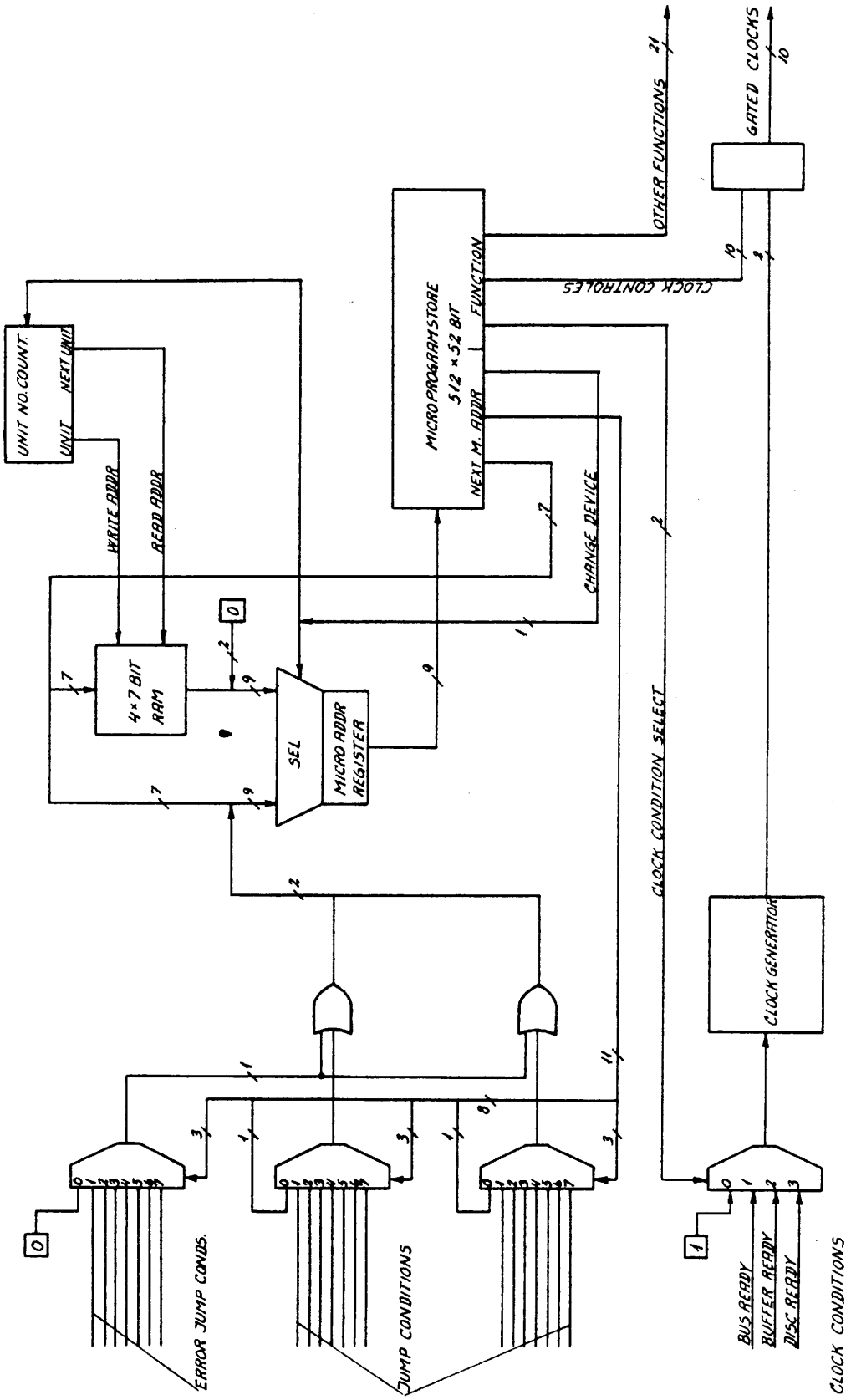
DSC 801

F 11682

DATAPATHES IN DSC 801

RC 8000 BUS





770422 PKA 770422 ROB

DSC 801

R 11891

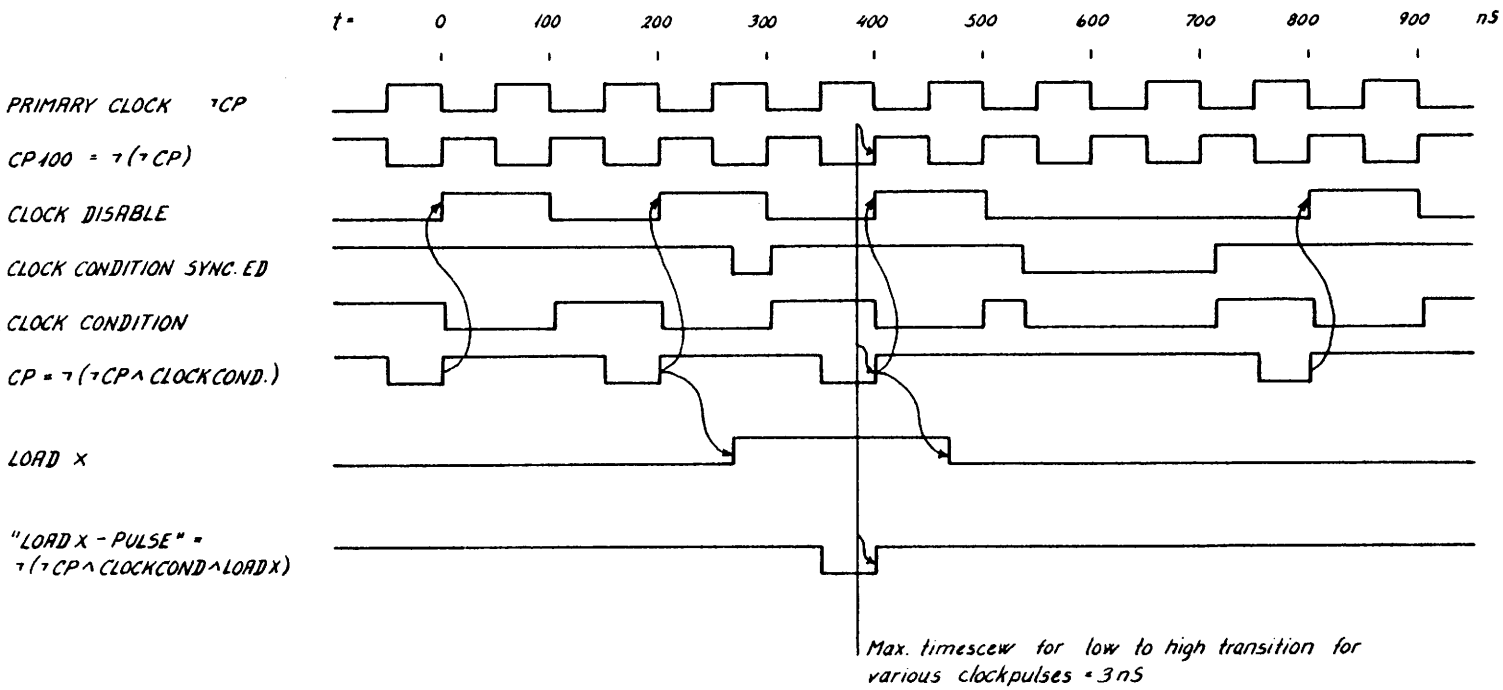
MICROPROGRAM CONTROLE

770422 PKA 770422 AOB

DSC 801

R 11890

CLOCK GENERATOR
TIMING DIAGRAM



CLOCKPULSE TIMING (examble)

770422 PKA 770422 AOB

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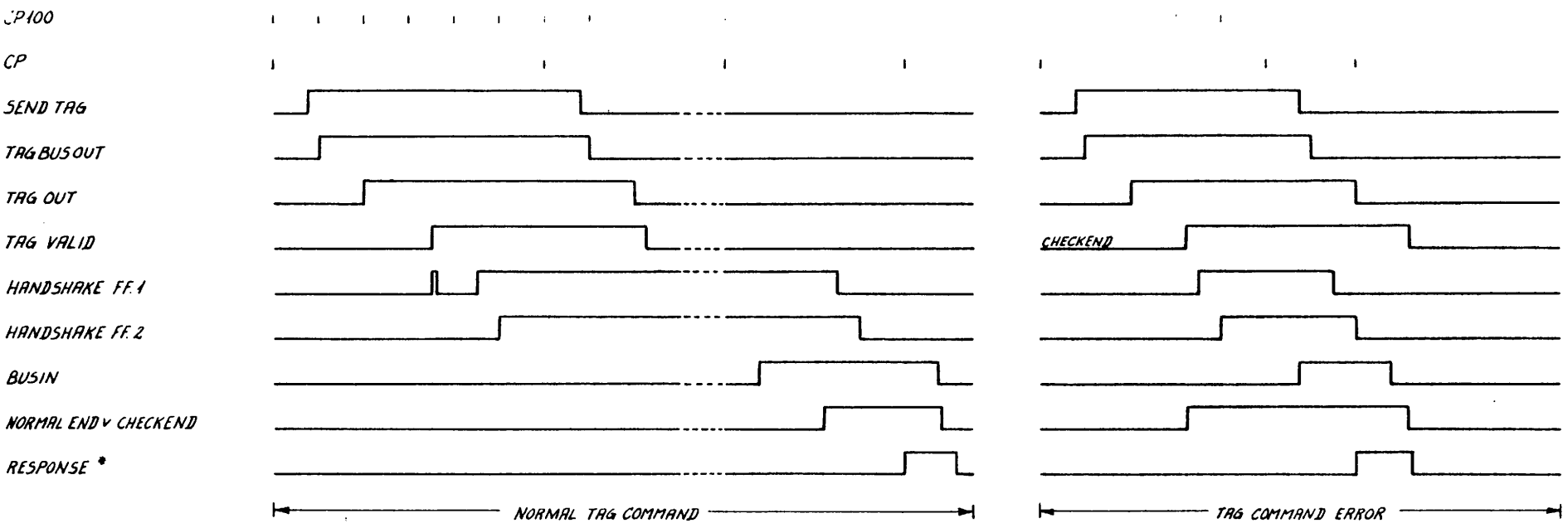
TAG COMMAND - HANDSHAKING
TIMING DIAGRAM

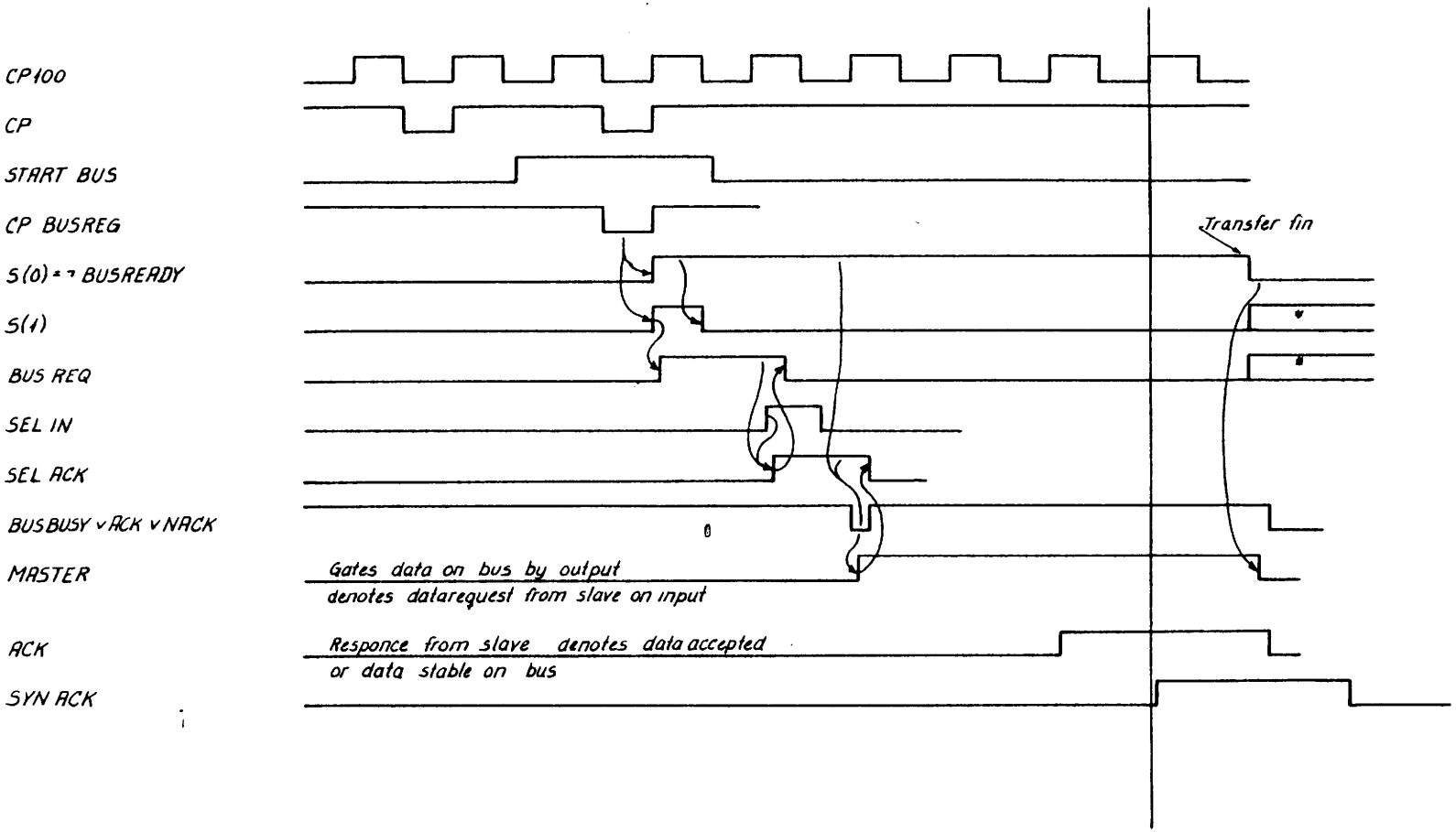


770422 PKR 770422 AOB

DSC 801

R 11887

BUS TRANSFER
TIMING DIAGRAM

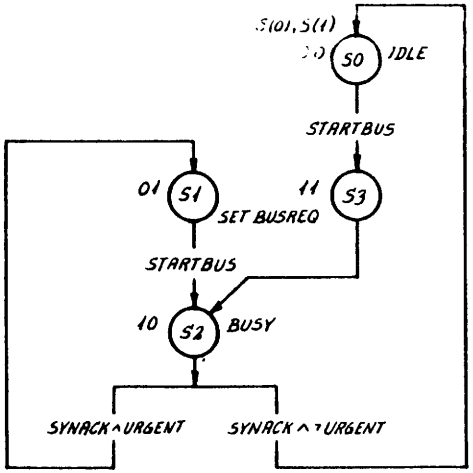


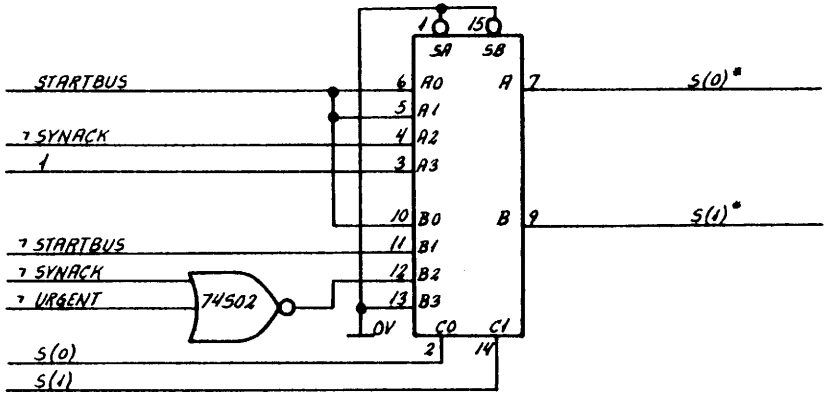
*: If next datatransfer is urgent, a new busreq is set before the bus is released but datatransfer is not started before so commanded by microprogram

DSC 801

P 11889

SYNCHRONOUS BUSLOGIC, STATEDIAGRAM AND STATEGENERATOR





S(1) ⇒ SET BUSREQUEST

S(0) = XFERENABLE (= ENABLE SET MASTER)

¬S(0) = BUSREADY

URGENT = RECYCLE ∧ (READ ⊕ ¬BUFFERHALF)

STATE	CONDITION	NEXTSTATE	S(0)*	S(1)*
S0	¬STARTBUS	S0	0	0
	STARTBUS	S3	1	1
S3	TRUE	S2	1	0
S2	¬SYNACK	S2	1	0
	SYNACK ∧ URGENT	S1	0	1
	SYNACK ∧ ¬URGENT	S0	0	0
S1	¬STARTBUS	S1	0	1
	STARTBUS	S2	1	0

RETURN LETTER

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How can this manual be improved?

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