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RC3502, VDC Testprogram Package
User's Guide

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Abstract:

This manual describes a reliability test of the video display controller (VDC201). It is split up into two subprograms, one testing against another VDC as a mirror, and one testing the circuit line with a maximum of 8 terminals connected.

(26 printed pages)

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RCSL 42-i1592

FOREWORD

First edition: RCSL No 30-M277.
This manual describes a reliability test of the VDC. It can be used for two purposes, one which is testing the video display controller alone, testing most hardware functions (must be connected to an auxiliary VDC), and another one which is testing the circuit line with a maximum of 8 stations connected (each station must contain the related test mirror process).

The VDC test is a test package in the RC3502 test system, TOP80, and must have this as a parent process, see ref. [2].

It is written in Real Time Pascal (RC3502 implementation).

Jan Nielsen
A/S REGNECENTRALEN af 1979, March 1981

Second edition: RCSL No 30-M298.
This second edition is made to introduce dynamic test buffers and a test log book.

The dynamic testbuffers can for test "a" be from 1 to 254 bytes, for test "b" from 1 to 32000 bytes.

The log book can give an impression of how the hardware has been handled.

Jan Nielsen
A/S REGNECENTRALEN af 1979, October 1981

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1. INTRODUCTION

1.1 Configuration Requirements

A minimum configuration for the RC3502-test system with a connection to an RC8000 or another load medium possibility for loading the test system TOP80 and the test. For test "A" there must be two VDC's connected with a two pair cable and a mirror process, which are linked, created, and started by the VDC test. The mirror process could be placed in another RC3502. For test "B", there is required one VDC, a two pair circuit line and at least one terminal (RC850) including the related test mirror.

1.2 Parameter Values

Param No	text	default	min.	max.
000	TESTPROGRAM	: A	A	B
001	NO OF RUNS	: 20	1	integer
002	MODULE NO (MASTER)	: 16	0	126
003	CHANNEL	: -1	-1	7
004	MODULE NO (MIRROR)	: 18	0	124
006	DATACHECK	: YES	NO	YES
010	MIN BLOCKSIZE	: 1	1	param No 011
011	MAX BLOCKSIZE	: 254	1	254 for test A 32000 for test B
018	DATA KIND	: 4	0, 1, 3, 4	
049	MAX MESSAGE	: 10	1	integer

Param No 003 specifies actual station number (if -1, it means all possible).

1.3 Load Test 1.3

How to load in general, see ref. [1].

TOP80 and the VDC test is loaded and started as described in ref. [2]. If testing against RC3502 mirror process is wanted, this can either be done in the same or other RC3502. If it is wanted to be done in the same RC3502, a mirror process for a slave VDC is included when the test is loaded. Otherwise you must load the second RC3502 with the bootfile BOOTMIR. The second RC3502 is started in the following way, when loaded:

It will then write:

```
> mirror
**start of vdc test mirror**
**ver. 81.02.24**


mirror module no.:
```

When you have filled in a valid no. ($10 \leq no < 126$), normally 18, it will write:

```
>>>mirror process started
```

if the creation of the slave VDC process was successful else it will write:

```
******mirror creation error: [error cause]******
```

Up till 10 mirrors could be started, replying to the question. (Note: That a mirror with a module no. 10 greater or smaller than one already started could not be started. And that there always should be a difference of 2 between a new mirror started and one already existing, due to the controller occupying two interrupt levels.

2. DYNAMIC TEST BUFFERS 2.

With the blocksize parameters an arbitrary databuffer size can be selected. These buffers are not allocated when the test is initiated, but dynamic allocated when the test is started. There is allocated 32 buffers of the maximum size, 2 transmitbuffers and 2 receivebuffers for each channel.

If the allocation meets limitations in memory, it is tried to start the test with 1 transmitbuffer and 1 receivebuffer per channel.

If this also fails the test tries to get buffers with half the size and so on.

The buffer-allocation can fail in two ways. It finds no buffers at all, OR it finds to few buffers of the size to have at least 1 transmitbuffer and 1 receivebuffer per channel. In the last case it is recommendable to restart the test with smaller buffers. In both cases the test will be terminated.

If the allocation of buffers succeeds the test will write as follows:

```
*** maximum test buffer size     : 254
*** maximum queue depth for xfer:   2
```

3. TEST A, RC3502 MIRROR, RELIABILITY 3.

Test A is a verification of proper operation of the video display controller hardware by transferring data/commands between master and mirror as defined by the circuit protocol, see ref. [3]. To check all controller operations possible, the VDC in test should be placed in either ends of the circuit line, to test all of its functions properly.

3.1 Test Strategy 3.1

The VDC test and the mirror process (with a slave VDC connected in same or other RC3502) are intended to simulate a normal circuit line with 8 stations. It is the mirror process that handles the slave VDC in a way, so that it acts as 8 secondary stations. It is therefore recommended to run the test twice swopping the VDCs. If this is done, all functions in the VDC are checked by the test program. In fig. 1 left of the vertical line the concerned processes are shown, right of the line, the hardware is shown.

The testing starts with a connection phase, where an attempt to connect the specified number of stations is made. Note that switch S4 (right) on the VDC must be open (see fig. 2). This causes the VDC to make longer flags so that the mirror can catch up with the primary.

In the beginning of the test, it is tried to generate errors with code (1, 2, 8, 12, 13) (ref. [4] or ref. [5]), to check that these are generated correctly. If this was not the case, an error with associated error code no. is written. All except error code 13 is generated, when the test places the code no. in the first byte of the databuffer.

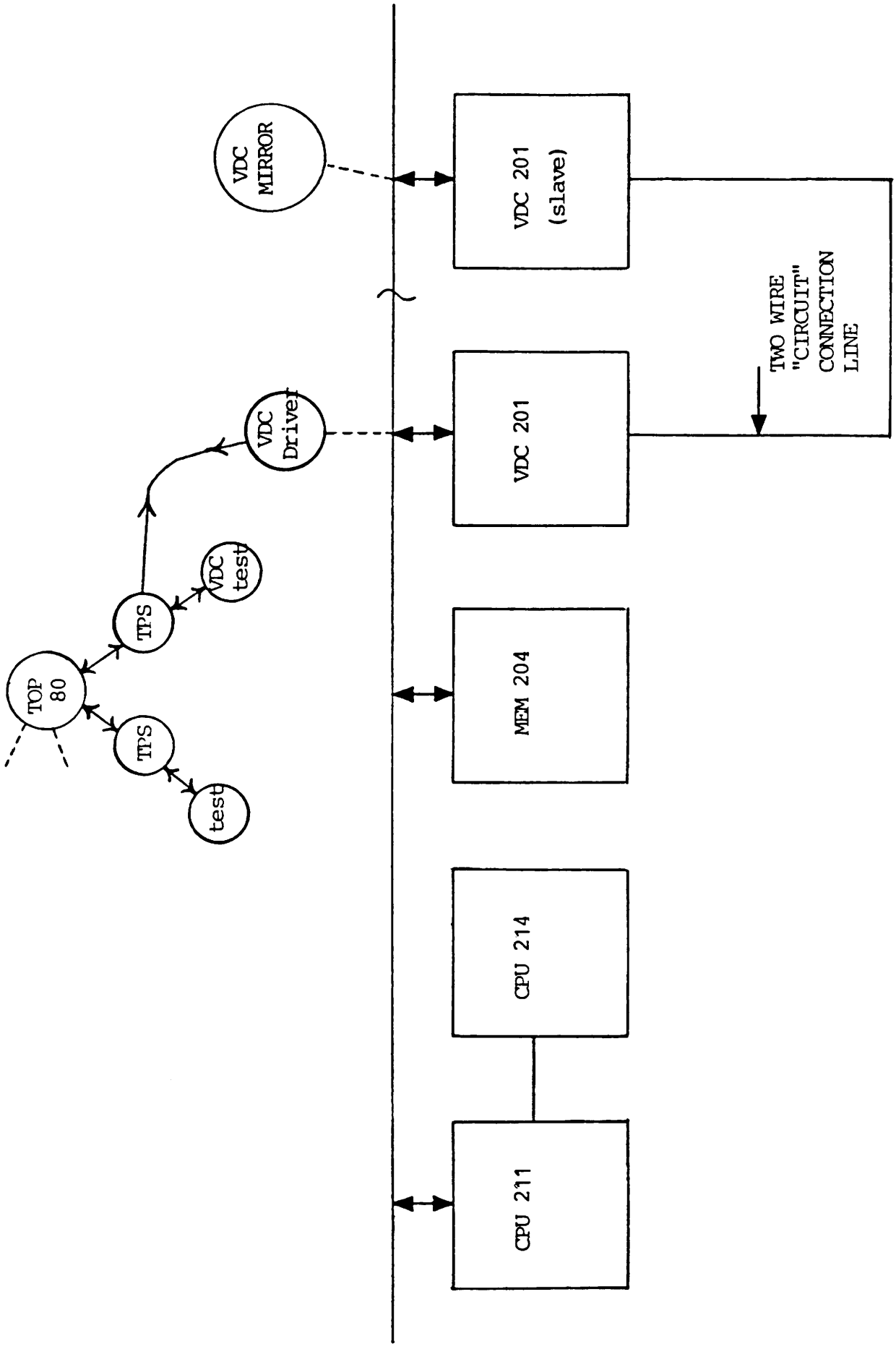
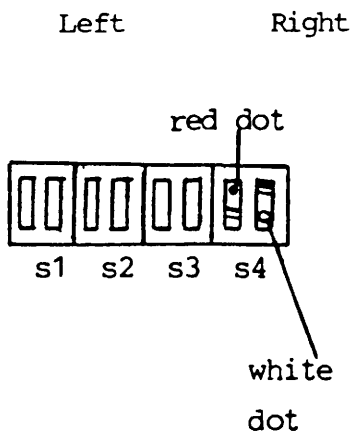


Figure 1: Test A, soft and hard configuration.



when S4 left is open the VDC microprogram will loop in its init phase.

s4 right must be open on primary when testing

Figure 2: VDC switch setting.

The mirror then performs the wanted action (e.g. when the mirror receives code 8 for timeout it does not reply within the timeout limit).

Error code 13 is generated by requesting a receive frame that is smaller than the transmitted.

If all errors were generated correctly, the test will proceed to the transfer data part. The first 4 "stations" will repeat their transfer with an increasing buffersize from minimum size to maximum size and decreasing back to minimum size (the growth is one byte per transfer). The last 4 "stations" will repeat their transfer with decreasing buffersize from maximum size to minimum size and increasing back to maximum size. This will test the frame recognition, when scanning the secondaries and use the line as much as possible.

The data patterns used in the transferred buffers can either be all zeroes (0), all ones (1) or counting (4). All ones can be used to check the automatic zero insertion.

Note: That pointers in the data buffer is pointing in the part that contains datapattern. The two first bytes are reserved for information to the mirror about errorgeneration. That is why the maximum blocksize of this subtest is 254 and not 256.

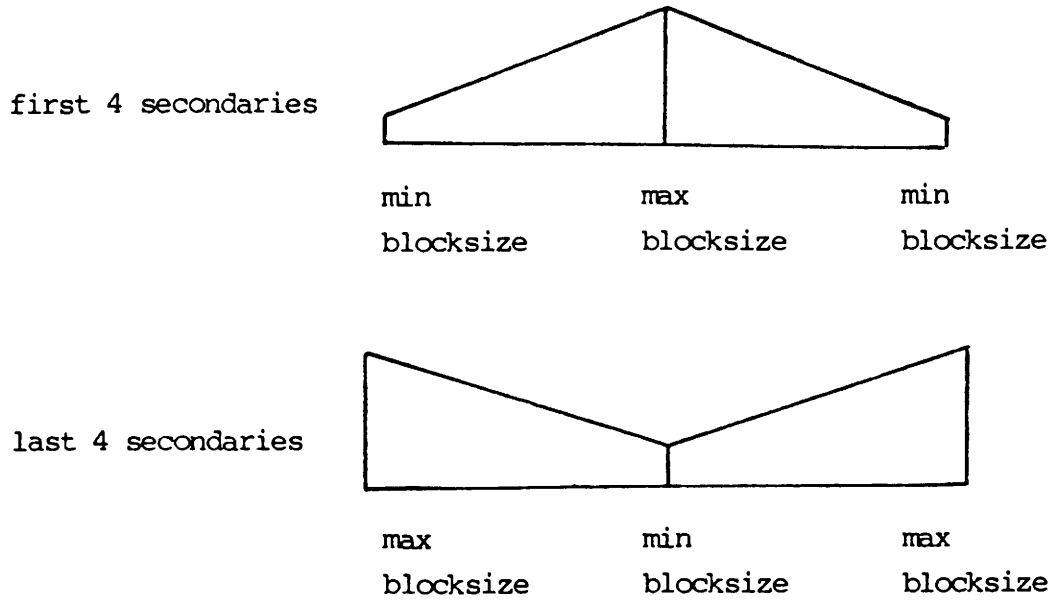


Figure 3: Blocklength variation during one run.

3.2 Error Messages

3.2

If an error is detected during operation an associated errortext is written on the output media.

The errortexts associated to the hardware are:

<secondary has unsolited buffer>:
The related secondary has a buffer not yet returned, because of a line disconnection.

<answer reset during communication>:
The station sent 'Anser Reset' during normal communication. (code 1).

<reset req, station had short intervention>:
The station sent 'Reset' indicating it wants to be reset (code 2).

<time out in communication with station>:
Time-out, i.e. no response from the station within 10ms. (code 8).

<cannot get access to line for 1 sec>:
Controller cannot get access to line for 1 sec, i.e. carrier signal persists (code 15).

<CRC-error or abort detected>:
Framing or FCS error (code 15).

<data error, hard error>:
The expected and received patterns is printed.

<data received when not receive ready>:
I-field received when master's RR was 0 (code 12).

<data field too long for buffer>:
Received I-field was too long for buffer (code 13).

<sequence number error, not in synchronism>:
Sequence number in header invalid (code 14).

<error in event code generation>:
The errorcode was of a not expected type.

<underrun because of bustimeout>:
Receiver underrun, buserror (code 10).

<overrun because of bustimeout>:
Transmitter overrun, buserror (code 11).

<Blocklength error>.
The received datablock was not of expected size.

The following three error messages indicate that the concerned process is not started correctly and proceeding has no meaning.

<fatal error in creation of tps>,
<fatal error in creation of mirror>,
<fatal error in creation of driver>,

4. TEST B, CIRCUIT LINE, RELIABILITY 4.

Test B is a verification of proper operation of the circuit line with one or more RC850 connected (maximum 8) by transferring data/commands between master and secondaries as defined by the circuit protocol, ref. [3]. The secondaries must contain the associated mirror processes to run the test. The function in the VDC by which it will act as a secondary is not checked when running this subtest.

4.1 Test Strategy 4.1

This subtest is the same as test "A", except for the fact that it does not make any attempt to generate error codes as in test "A" and it is intended to run with maximum 8 RC850s. For further description see sections 2.1 and 2.2. Fig. 4 shows the processes concerned and the hardware (example with 4 stations).

It is possible to run this subtest with datapattern 3, which generates a readable text on screen of the RC850.

The text is:

VDC TEST IN PROGRESS

If the buffer is greater than this, the rest will contain the readable alphabet.

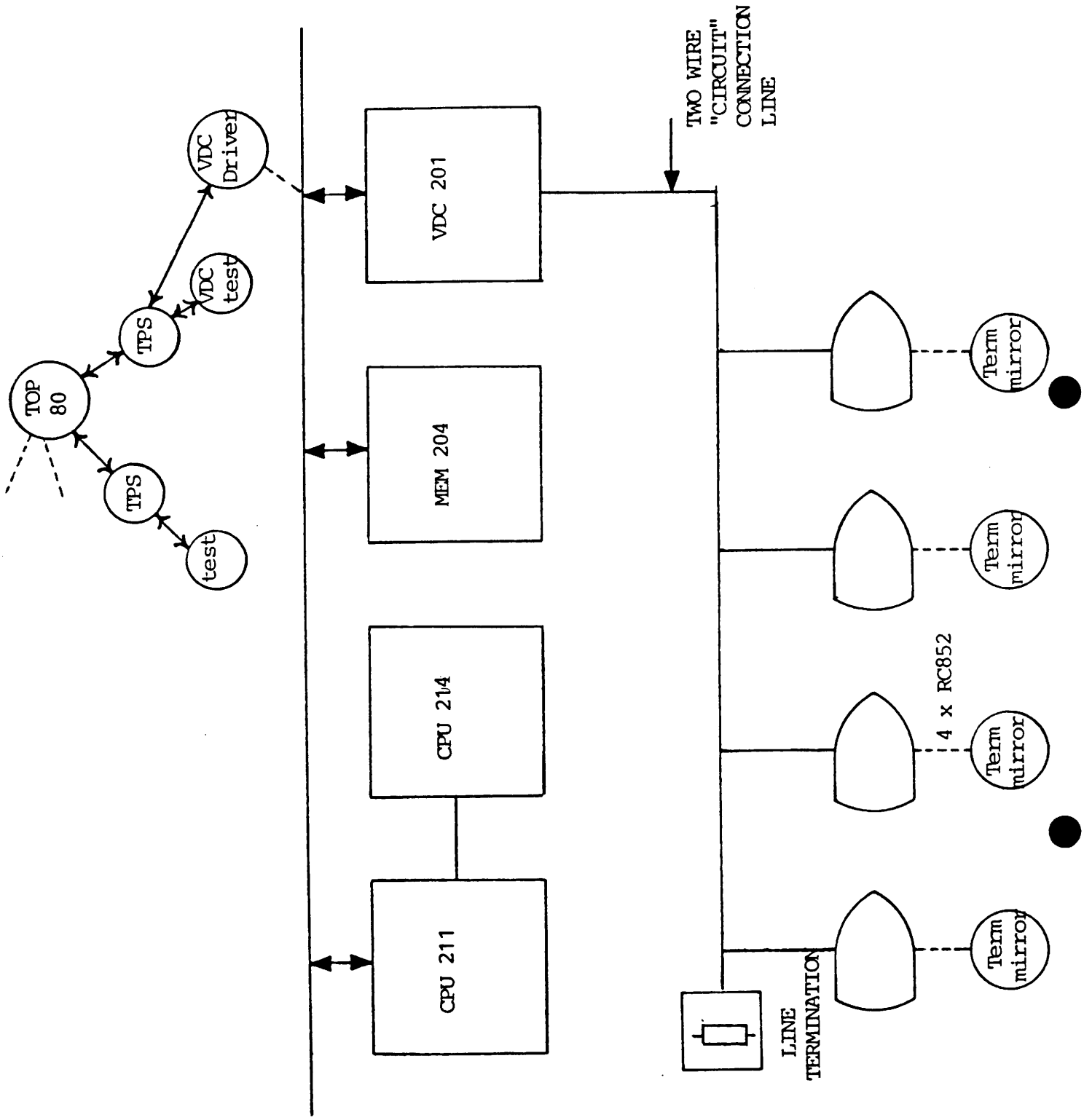


Figure 4: Test B, soft and hard configuration.

5. LOG BOOK 5.

The test contains a log book that can be used to get information about the 64 internal controller register or a log of the past (earlier control and interrupt words) from a cyclic buffer of 256 word resident in the driver. The log book is identified by the name <VDCPRINT<NO>>, where <NO> is the same number identifying the test.

Commands to <VDCPRINT<NO>> are:

<r> : giving a printout of the 64 internal controller registers. See ref. [5].

<i> : giving a printout of the 256 words from cyclic buffer in the controller. Each word is either a controlword or an interrupt word.

5.1 Controller Registers 5.1

The layout of the 64 controller registers could be seen in ref. [5] fig. 3.2.1. It is printed on 16 lines with each line containing 4 register Pairs, equvalent to the way the registers are used (one channel occupies 4 registers).

```
select info:reg

*** controller registers ***

register no  0 until :  3 contains :   23 47   00 06   31 f6   01 00
register no  4 until :  7 contains :   03 67   00 06   2d ae   01 00
register no  8 until : 11 contains :   23 47   00 06   29 66   01 00
register no 12 until : 15 contains :   42 a7   00 06   69 9e   01 00
register no 16 until : 19 contains :   63 47   00 06   43 16   01 00
register no 20 until : 23 contains :   43 67   00 06   3e ce   01 00
register no 24 until : 27 contains :   63 47   00 06   3a 86   01 00
register no 28 until : 31 contains :   63 47   00 06   36 3e   01 00
register no 32 until : 35 contains :   ff ff   02 00   00 00   02 e7
register no 36 until : 39 contains :   00 38   02 00   00 00   86 ff
register no 40 until : 43 contains :   43 43   02 ff   00 67   02 00
register no 44 until : 47 contains :   02 00   00 00   02 18   39 3c
register no 48 until : 51 contains :   05 05   01 06   29 66   00 00
register no 52 until : 55 contains :   0e 14   00 06   27 42   00 39
register no 56 until : 59 contains :   00 00   01 00   00 84   00 00
register no 60 until : 63 contains :   00 00   02 00   a4 03   ff ff
```

Figure 5: Example of Controller Register output.

5.2 Interrupt/Control Words 5.2

The 256 words of the cyclic buffer are printed with 8 words per line. The first printed word is the oldest event. If the buffer has been filled more than once, a line like the following is printed

97 mod 256 words lost.

The control words is presented in hexadecimal and must be one of the controlwords to the controller, ref. [5].

The interrupt words are presented like this

```
0   1   2   3   4 | 5   6   7 | 8   9  10  11 | 12 | 13  14  15
                  |           |               |    |
                  |           |               |    |
RR  SR  SN  U   X | RX  RX  TX| error-event   |    | subdevice
  T   T   T       T CHG Data Data             |    |
```

Where bit 12 is set to 1, to be able to differentiate interrupt words from controlwords. An example of an interrupt word could look like this: a4 08.

```
select info:int

*** interrupt/control -  words ***

247 mod 256 words lost.
03 33   42 0c   43 34   a4 0c   43 34   03 94   00 85   45 0c
03 34   42 0d   43 35   a4 0d   43 35   03 95   45 0d   03 35
00 86   42 0e   43 36   a4 0e   43 36   03 96   45 0e   03 36
00 87   62 0f   43 37   84 0f   43 37   03 97   65 0f   03 37
00 80   42 08   03 30   a4 08   03 30   00 81   62 09   03 31
84 09   03 31   00 82   62 0a   03 32   84 0a   03 32   00 83
62 0b   03 33   84 0b   03 33   00 84   42 0c   03 34   a4 0c
03 34   00 85   42 0d   03 35   a4 0d   03 35   00 86   42 0e
03 36   a4 0e   03 36   00 87   62 0f   03 37   84 0f   03 37
00 80   00 81   00 82   00 83   00 84   00 85   00 86   00 87
43 30   03 90   67 08   03 30   00 80   43 31   03 91   84 08
03 30   47 09   03 31   00 81   a4 09   03 31   43 32   03 92
47 0a   03 32   00 82   a4 0a   03 32   43 33   03 93   47 0b
03 33   00 83   a4 0b   03 33   43 34   03 94   47 0c   03 34
00 84   a4 0c   03 34   43 35   03 95   47 0d   03 35   00 85
a4 0d   03 35   43 36   03 96   47 0e   03 36   00 86   a4 0e
```

Figure 6: Example of interrupt/control-words.

A. REFERENCES A.

[1] RCSL No 52-AA988:
PASCAL80 on the RC3502 Computer, How to Use the RC3502

[2] RCSL No 30-M280:
RC3502, TOP80, Test Operating System, User's Guide

[3] RCSL No 31-D598:
CIRCUIT Protocol, Reference Manual

[4] RCSL No 31-D616:
RC3502 VDC201 CIRCUIT Master Driver

[5] RCSL No 31-D599:
VDC201/291, Reference Manual

[6] RCSL No 31-D637:
VDC201, Technical Manual

[7] RCSL No 31-D636:
VDC201/291 General Information

B. EXAMPLES OF OUTPUT

B.

```
>top
new/vdc
vdc initiated as vdc02
Select function:
>vdc02
** vdc 201 test **** ver 81.09.27 **
testprogram        :a
a: mirror in rc3502
b: terminal mirror
Select test:
>vdcprint02
select info:
>vdc02
a
Select function:
list
** vdc 201 test **** ver 81.09.27 ** LIST OF PARAMETERS :
p000  testprogram        :      a
p001  no of runs         :     20
p002  module no (master) :     16
p003  channel            :     -1
p004  module no (mirror) :     18
p006  datacheck          :    yes
p010  min blocksize      :      1
p011  max blocksize      :    254
p018  data kind          :      4
p049  max message        :     50
Select function:
start
Select function:
*** maximum test buffer size     :   254
*** maximum queue depth for xfer :     2
run no.     1

** station : 0  connected

** station : 1  connected

** station : 2  connected

** station : 3  connected

** station : 7  connected

** station : 6  connected

** station : 5  connected

** station : 4  connected
```

C. SPECIALITIES C.

The RC850 mirror process will be supplied as PROM (ROA408-ROA409-ROA410), which must be placed in the terminal(s) before running test-B.

The driver is started when the test is started and not removed before the test is killed by TOP. Therefore do not change p002 (module No) without killing the test first.

RETURN LETTER

Title: RC3502, VDC Testprogram Package User's Guide RCSL No.: 30-M298

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