PN: 99001311
Date: 1989-10-20
Author: Henning Jakobsen

RC3502 MEM Testprogram Package

User's Guide

RC International

Keywords:

RC3502, RAM-Memory, testprogram

Abstract:

This manual describes a reliability test of the RAM-memory MEM204, MEM205/206, and MEM207/208/209 which consists of nine different sub-tests numbered from "a" to "i".
The tests are: address test, bit selection test, worst case complement test, jumping test, move byte test, move word test, general reliability test, eprom checksum test, and MEM207/208/209 functional test.

(13 printed pages)

TABLE OF CONTENTS

Page

1. INTRODUCTION

This manual describes the memory reliability test of the MEM204, MEM205/206, and MEM207/208/209. The testprogram consists of 9 different subtests numbered "a" to "i". "a" is an address test, first writing all the addresses within the test area, thereafter only reading and checking for modifications. "b" is a bit selection test, which tries to set one bit at a time in each memory cell. "b" is a bit selection test, which tries to set one bit at a time in each memory cell. "c" is a worst case complement test, it only writes in the first run. "d" is a jumping test, which jumps with increasing distances until the distance is half the test area. The pattern is 010101 - or 1010101 - every second time. "e" is a move test, which moves bytes by means of "moveb". "f" is a move test, which moves words by means of "moveg". "g" is a general reliabilty test, which starts loading with 0's. Each address is read and verified. Then a single 1 is substituted in one bit position, and the altered word is written back in the same location. And finally the word is reread to verify the newly entered 1 is still there. The procedure is repeated for all databits, leaving the memory filled with 1's. The same procedure is taken filling with 0's. The refresh circuit is tested in test "g" which includes a 3 minutes pause.

"h" checks the checksums in eproms, and "i" tests the error detection and correction functions i MEM207/208/209.

Subtest "a", "b", and "e" may run in external memory too.

The MEM test is a testpackage in the RC3502 test system, TOP35, and must have this as a parent process.

It is written in Real Time Pascal (RC3502 implementation).

1.1 Configuration Requirements

A minimum configuration for the RC3502 testsystem and a memory to be tested. A load possibility for the testsystem (e.g. RC8000 connection, LAN connection, or TES modules with the testsystem).

1.2 Parameter Values

Param No.	Text	Default	Min	Max.
0	TESTPROGRAM	g	a	i
1	NO OF RUNS	1	1	32767
2	MODULE NO	200	128	254
3	FIRST ADDR (K byte)	0	0	31
4	FIRST ADDR (byte)	0	0	HFFFC
6	DATA CHECK	YES	NO	YES
7	PARITY CHECK	YES	NO	YES
8	STOP ON PARITY ERR	NO	NO	YES
10	TEST SIZE-1 (K wrd)	127	0	511
11	TEST SIZE-1 (Words)	1023	0	32767
12	MEM205/209 RAM start	200	0	216
49	MAX ERROR MESSAGES	10	1	32767

Param No. 2 gives module no computed as 192 + 2 * (DIPswitch setting) (in hex: A0, A2, ... C0, C2,...EE). External modules are numbered from hex 80.

First byte no to be tested is given by param no 003 * 1024 + param no 004. Examples: Param no 003 = 8 and param no 004 = 0 means start in hex 2000. Param no 003 = 0 and param no 004 = h3400 means start in hex. 3400.

Test area size in words is given by param no 010 * 1024 + param no 011 + 1. Maximum value (511,1023) gives four MEM205 modules (31,1023) gives one MEM204 module.

Param No. 8 controls test of multible bit errors, NO means that only one-bit errors are tested, YES means that multible errors are tested (this gives a bus parity error, which stops the CPU).

1.3 Load and Start of the Test

How to laod in general, see ref. 1. TOP35 and the MEM-test is loaded and started as described in ref. 2.

*** Note the following:

Because the test is written in the high level language Real Time Pascal, some special actions are taken in start of the test to get the wanted memory as buffers. Therefore it is recommendable to start up the memory test before any other, so that these others cannot steal buffers which should be tested.

When the test has written the actual testing size, this critical phase has ended. (Do not start anything else in the meantime).

The actual testing size will be the nearest possible or greater than the wanted one. The smallest accepted size is 2 words. Be aware of that the special way to allocate memory may give you a testing buffer placed outside the wanted area.

The different tests can be run with or without check of data (Param No. 006), and with or without error message for parity errors (Param No. 007).

Before executing of subtest a - g every module with any unused area are tested for module selection (the module no is written in byte 4).

To be successful subtest i must run alone. No DMA transfers must be performed, i.e. MFCxxx and COM205 must be inactive, and the console must not be used. If these rules are violated the system will stop with a parity error.

2. SUBTEST SPECIFICATION

2.1 TEST A, Address Test

Test A is an address test, first writing all the addresses within the test area, thereafter only reading and checking for modifications. This is the only subtest that both reads wordswise and bytewise. Only bytewise transfer for external memory.

2.2 TEST B, Bit Selection Test

Test B is a bit selection test, which for each word first writes the least significant bit alone. And then reads it to verify that it is correctly written. Then it is shifted one position towards the most significant bit and read again. This is done until the MSB is reached. Then the test proceeds to the next word and the procedure is repeated, until the whole area is tested. Bytewise transfer for external memory.

2.3 TEST C, Worst Case Complement Test

Test C is a worst case complement test, which only in run no. 1 writes the worst case pattern. The proceding runs are checking that the content is not modified. Can only run in internal memory.

The complement pattern is derived in the following way: When address bit 14 is not equal to address bit 2, the content of the dataword is 0, else it is -1.

2.4 TEST D, Address-Jumping Test

Test D is a test, which jumps in address with increasing distances, until the jump distance is half of the allocated size. It starts with jump distance 1. The pattern is either

1010101010101010 or 0101010101010101

every second time.

The test starts with a reset of all memory cells to zero. Can only run in internal memory.

2.5 TEST E, Move Byte Test

Test E uses "moveb" to move the whole area (last byte is not used) one position. This test gives many memory accesses and may run in external memory, too. Testsize must be at least 32 words.

2.6 TEST F, Move Word Test

Test F uses "moveg" to move blocks of words. Blocklength varying from one to 30. This test will in model 2 use and test the CPU217 prefetcher. Testsize must be at least 32 words.

2.7 TEST G, Long Reliability Test

Test G is a test first writing zeroes in all locations. Each address is read and verified. Then a single 1 is substituted in one bit position, and the altered word is written back in the same location. And finally the word is reread to verify the newly entered 1 is still there. This procedure is repeated until all cell are all ones. The same action is taken with zeroes.

The whole area is writtten and read with a 'moveb' instruction. The last phase of this test is a test of the refresh circuit; this test includes a 3 minutes pause.

Bytewise transfer for external memory.

2.8 TEST H, EPROM Sumcheck

Test H controls the checksum in installed EPROM's.

p002 is first module

p003 is number of modules

p004 gives number of seconds between each run of the test

2.9 TEST I, MEM207/208/209 Functions

This test is used to check that the error detection and error correction functions are working correctly. The test is divided in two phases, in phase one one-bit errors are checked. In phase two, which is only entered if parameter 8 "stop on parity err" is "YES", the detection of multible bit errors are tested. This test will however stop the CPU with a "parity error", and the system must be autoloaded again.

3. TESTOUTPUT

The test has the general output routines for things like "run no" and so on.

When the test has passed the initialization phase, where it gets its buffer, it will write where it starts (byte address) and how large the testbuffer is.

```
--   test area start locations (hex) c0:  80AA..FFFF
--   test area size -1:                   16298
```

(Testing a whole memory module, the size will appear as 32767).

3.1 Operator Directions

The following texts could appear (see also the examples in appendix B):

?operator error: illegal value. Parameter xx given xxxxx set to xxxxx.

Self-explaining. The parameters with limit check is P002, P003, P004, P010 and P011.

"no core in wanted area"

means that the test has not found a buffer within the wanted range. (The test is not run). You can use the 'OPSYS' command 'FREE' to find modules with free areas.

"reserveextmem = x"

means that reservation of external memory failed.

cause 1: area reserved
cause 4: module not installed
cause 6: no core for area descriptor
Other causes are testprogram failures.

"change byte xxxx via debug:"

appears in model 1 if byte 01 of the wanted area = 0. You must use the debugger M command to change the byte to FF.

"? module not installed."

appears in model 2, if reservation of external memory fails.

3.2 Error Output

"data error: error in word"

means that the read data is different from the written. Received and expected specifies the difference.

"moveb: error in word"

means that data read after being moved by 'moveb' is different from the written.

"moveg: error in word"

means that data read after being moved by 'moveg' is different from the written.

"parity error in testbuffer"

means that at least one parity error was detected in the memory, which you are testing. (W 3FE and 3FF hold the address). The test program is reading from memory without the normal CPU-microprogram parity check to prevent the system from stopping, when it meets a parity error in the memory.

"parity error outside testbuffer"

means that the two W registers (W 3FE and 3FF) that hold the parity address were pointing to some other module than the one tested by this incarnation. The address could be in the testbuffer for another incarnation of the MEMTEST, or the address is made by some other program.

"error in syndrome bits"

means that the syndrome bits in the error log register is wrong.

```
"** LEFT bank syndrome    RIGTH bank syndrome "
          ABC    DEFGH            IJK    LMNOP
```

This is the content of the error log register in MEM207/208/209

```
"** logstate err-type bank syndrom
     AB        CDEF    G         HIJKLM"
```

This is the content of the errorlog in a MEM205. For details see the MEM205 General Information.

"checksum error in eprom"

Error in a CRC16 checksum. Maybe caused by unsuccessful reading from the TES module.

"module select error"

More than one module are selected. Received and expected are the module numbers in hex.

4. TURN AROUND TIMES

The specified times are the approximate turn around times per 32K module for each sub-test in the RC3502 computer without any other test running at the same time.

SUBTEST	TURN AROUND TIME
A	30 sec.
B	3 min. 15 sec.
C	30 sec.
D	35 sec.
E	3 min. 25 sec.
F	45 sec.
G	10 min. 45 sec.
H	5 sec.
I	15 sec.

Note that the turn around times may be smaller in later versions of the CPU microprogram or the compiler.

The time for G test of a whole MEM205 in model 2 is 16 minutes.

A. REFERENCES

1. PN: 99 0 00771:
RC3502/2 Operating Guide

2. RCSL No. 30-M329:
RC3502, TOP35, Test Operating System User's Guide

3. RCSL No. 52-AA977: Technical Manual for MEM204

4. RCSL No. 52-AA1182: MEM205 General Information

5. PN: 99 0 00815 MEM206 General Information

B. EXAMPLE OF TESTOUTPUT

```
Select function:
LIST
-- MEM 20X test ---- ver 89.10.13 -- LIST OF PARAMETERS :
p  0  testprogram          :      f
p  1  no of runs           :      1
p  2  module no            :    128  h80
p  3  first addr (K byte)  :      0  h00
p  4  first addr ( byte)   :      0  h00
p  6  datacheck            :    yes
p  7  parity check         :    yes
p 10  test size-1 (K wrd)  :    511
p 11  test size-1 (words)  :   1023
p 12  MEM205/209 RAM start    128
p 49  max error messages   :     10
Select function:
P1=3 P2=H90 P4=H10 P10=3 P12=HA0 P49=2 START
Select function:

-- test area locations  ( hex ) 90:   0010  ..  200f
-- test area size-1                  4095
run no.      1            1989.10.20  11.28.23
********** run no.      1  : **********
moveg : error in word
module no  :   90
byte no    : 9ff2
expected   :       01
received   :       00
********** 1989.10.20  11.28.23 ****
********** run no.      1  : **********
moveg : error in word
module no  :   90
byte no    : 9ff2
expected   :       01
received   :       00
********** 1989.10.20  11.28.26 ****
--  Test terminated.
-- MEM 20X test ---- ver 89.10.13 -- LIST OF ERRORS :
---------- run no.      1  : ----------
     2 of type :moveg : error in word
Total number of errors :      2
---------- 1989.10.20  11.28.38 ----
```

```
Select function:
P0=I
Select function:
LIST
-- MEM 20X test ---- ver 89.10.13 -- LIST OF PARAMETERS :
p  0  testprogram          :      i
p  1  no of runs           :     10
p  2  module no            :    160  ha0
p  6  datacheck            :    yes
p  8  stop on parity err   :     no
p 12  MEM205/209 RAM start    160
p 49  max error messages   :      2
Select function:
P1=3 START
Select function:
!! Warning:   -> This test  MUST  be   running alone.
                 Don't use the console, no DMA cycles.

  ID reg:      19 hex     MEM 209 installed.

 ! check that both yellow LEDS are on
   and that MNT shows weak ligth.
run no.       1            1989.10.20   11.29.13
run no.       2
run no.       3
press  CLEAR ERROR LEDS,  check all off
--  Test terminated.
-- MEM 20X test ---- ver 89.10.13 -- LIST OF ERRORS :
--------------- run no.     10  : ---------------
No errors detected by testprogram.
---------------------- 1989.10.20   11.29.18 ----
Select function:
P8=YES START
Select function:
!! Warning:   -> This test  MUST  be   running alone.
                 Don't use the console, no DMA cycles.

  ID reg:      19 hex     MEM 209 installed.

 ! check that both yellow LEDS are on
   and that MNT shows weak ligth.
run no.       1            1989.10.20   11.29.52
run no.       2
run no.       3
press  CLEAR ERROR LEDS,  check all off
Test for fatal errors.
The 2 red 'FER'  LEDS should be on, and CPU's  'OP' LED  goes
off.
After this the system must be autoloaded
  10 seconds delay .
P  D4:D3F6  LR
*
```

C. STATISTIC COUNTERS

Index	Meaning
8	parity errors outside the testbuffer
9	parity errors in the testbuffer
10	checksum errors in eprom
11	errors during word transfer
12	errors during movebytes
13	errors during moveg
14	errors in left byte
15	errors in right byte
16	module select errors
17	error in syndrome bits

All other counters are not used.