TITLE: STANDARD FLOPPY DISK CTRL.
TECHNICAL MANUAL
CR8047D/010AB/00

DOCUMENT NO : CSD/005/TCM/0041

PREPARED BY : BERTRAM PAÅSKESEN

AUTHORIZED BY: GOTTLOB BORUP

DISTRIBUTION : PRO(3), BBP, PO
File(2)
KFL(2), LU(6)
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ENG/QA	811002	K.C. Kielsen.

ISSUE: 1

DATE: 810126

400-810-1

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		DATE 820329	
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6 REL.CAT. ☐ I ☒ II	7. PROJECT.	8. CONTRACT NO.	9. REF.

10. DOCUMENT TITLE

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CSD/005/FNC/0032 Issue 1	810901	CSD/005/FNC/0032 Issue 2	820413

13. PREPARED BY BERTRAM PAASKESEN	DATE 820329	APPROVED BY	DATE
14. APPROVED BY KARSTEN NIELSEN	DATE 820480	APPROVED BY	DATE
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13. PREPARED BY BERTRAM B. PÅSKESEN	DATE 820109	APPROVED BY	DATE
14. APPROVED BY	DATE	APPROVED BY	DATE
15. AUTHORIZED BY	DATE	APPROVED BY	DATE

16. DISTRIBUTION PRO(2), BBP, KFL(4), File(2)

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	repl	project

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1. INTRODUCTION

This document contains all required information for production and board level maintenance at factory of the Floppy Disk Controller CR8047M, which is a standard CR80M module.

2. CIRR

The release status of the configuration items is defined in the following Configuration Item Release Record.

Single Bus Version: CSD/003/LST/0552
Dual Bus Version: CSD/003/LST/0586

K

CONFIGURATION ITEM RELEASE RECORD

P/N: 4.04169-01 CR NO: CR8047D/010A/00 FLOPPY DISK CONTROLLER

DESIGNER	DOC. NO.	ISSUE	INIT / DATE	PAGE
BBP	CSD/003/LST/0552	4	821103	1 of 3

LINE	DOCUMENT / DRAWING NUMBER	DOCUMENT / DRAWING TITLE		DESIGN RELEASE (1)	ISSUE STATUS ON RELEASE 2	3	4	5	6
1	CSD/005/PSP/0078	PRODUCT SPECIFICATION	ISS	3					
			DATE	820916					
2		TEST SPECIFICATION							
3		TEST PROCEDURE							
4		TEST REPORT							
5	CSD/005/TCM/0041	TECHNICAL MANUAL		1/2 810126					
6		USERS MANUAL							
7		RELIABILITY ANALYSIS							
8		FMECA ANALYSIS							
9		DESIGN ANALYSIS REPORT							
10	CSD/005/FNC/0032	FUNCTIONAL DESCRIPTION		2 820413					
11									
12	3-3028	BLOCK DIAGRAM		1 810910					
13									
14	2-287	MECHANICAL DWG, FRONT PANEL		2 801223					
15	S3-266	SILK SCREEN DWG, FRONT PANEL		1 810105					
16	T2-588	LAYOUT DWG, FRONT PANEL		2 820125					
17									

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CONFIGURATION ITEM RELEASE RECORD

CR8047D/010A/00

P/N: 4.04169-01 CR NO: F. D. CONTROLLER

DESIGNER	DOC. NO.	ISSUE	INIT / DATE	PAGE
BBP	CSD/003/LST/0552	4	821103	2 of 3

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18	4.04169-01	PARTSLIST, MODULE	1 800922					
19		PARTSLIST, FIRMWARE PACKAGE						
20		PARTSLIST, MODULE, BASIC						
21	2-274	ASSEMBLY DWG, MODULE	1 801001					
22								
23		VDD, BASIC FIRMWARE						
24	CSD/005/VDD/0022	VDD, APPLICATION FIRMWARE	1 801016					
25	CSD/005/LST/0009	MICROPROGRAM LISTING	1 810921					
26	1 - 207	BLOCKED SCHEMATIC	1 800815					
27	CSD/005/LST/0010	PAL SOURCE	1 810921					
28	5.04188-00	PCB 1 PARTSLIST, BASIC	1 800513					
29	K2 - 476	ASSEMBLY DWG, BASIC	1 800815					
30		PARTSLIST, APPL. DEFINED						
31		ASSEMBLY DWG, APPL. DEFINED						
32	2 - 281	DRILLING DRAWING	1 800506					
33	476 A B	LAYOUT DRAWING	1 800425					
34	476C	SILK SCREEN DRAWING	1 800815					
35	CSD/005/ECO/0185 -1A	ENGINEERING CHANGE ORDER.	1A 800814					

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			DATE	800819					
37	CSD/005/ECO/0250-1C	ECO		1C 801220					
38	CSD/005/ECO/0537-1D	ECO		1D 820420					
39	CSD/005/ECO/0575-1E	ECO		1E 820611					
40									

DISTRIBUTION:

400-938

CONFIGURATION ITEM RELEASE RECORD

P/N: 4.04196-01 CR NO ST FD CTRL (dual bus) 8047D/010AB/00

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1	CSD/005/PSP/0078	PRODUCT SPECIFICATION	ISS/REV	1	3				
			DATE	810112	820916				
2	CSD/008/TPR/0081	TEST SPECIFICATION			1				
					810701				
3		TEST PROCEDURE							
4	CSD/008/TRP/0100	TEST REPORT			1				
					820118				
5	CSD/005/TCM/0041	TECHNICAL MANUAL		1	1.2				
				810126					
6		USERS MANUAL							
7	CSD/005/RRP/013	RELIABILITY REPORT			1				
					810413				
8		FMECA ANALYSIS							
9		DESIGN ANALYSIS REPORT							
10	CSD/005/FNC/0032	FUNCTIONAL DESCRIPTION		1	2				
				810901	820413				
11	CSD/008/TRP/0097	FAQ TEST PROCEDURE			1				
					820118				
12	3-2843	BLOCK DIAGRAM		1	1				
				810213					
13	CSD/008/TRP/0097	FAQ TEST RAPPORT			1				
					820118				
14	2 - 370	MECHANICAL DWG, FRONT PANEL		2	3				
				801103	820125				
15	S3 - 207/2	SILK SCREEN DWG, FRONT PANEL		2	3				
				801103	820125				
16	T2 - 589	LAYOUT DWG, FRONT PANEL		1	2				
				810112	820215				
17	RELEASE AUTHORIZATION AND APPROVAL		SIGN						
			DATE						

DISTRIBUTION: PRO(5), KN, GB, BBP, KFL(7), KAM, EV, FILE(2), HKJ

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18		PARTSLIST, MODULE							
19		PARTSLIST, FIRMWARE PACKAGE							
20	4.04196-01	PARTSLIST, MODULE, BASIC		0 801209	1 810501				
21	2-274	ASSEMBLY DWG, MODULE			2 820802				
22	CSD/005/LST/0014	MICROPROGRAM LISTNING			1 820111				
23		VDD, BASIC FIRMWARE							
24	CSD/005/VDD/0058	VDD, APPLICATION FIRMWARE			1.1 810427				
25	CSD/005/LST/0013	PAL SOURCE LISTNING			1 810929				
26	1 - 275	BLOCKED SCHEMATIC		1 810115	2 810526				
27									
28	5.04222-00	PCB 1 PARTSLIST, BASIC		0 801209	1 810501				
29	K2-522	ASSEMBLY DWG, BASIC		1 810119	4 820215				
30		PARTSLIST, APPL. DEFINED							
31		ASSEMBLY DWG, APPL. DEFINED							
32	2-502	DRILLING DRAWING		1 810119	4 820215				
33	522 A - B	LAYOUT DRAWING		1 801201	3 810715				
34	522 C	SILK SCREEN DRAWING		1 801201	3 810715				
35	432-3A	ENGINEERING CHANGE ORDER.			3A 810911				

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CONFIGURATION ITEM RELEASE RECORD

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BBP	CSD/003/LST/0586	6	821102	3 of 3

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36	492-3B	ENGINEERING CHANGE ORDER	3B / 811111						
37	527-3C	ENGINEERING CHANGE ORDER	3C / 820318						
38	547-3D	ENGINEERING CHANGE ORDER	3D / 820427						

RELEASE AUTHORIZATION AND APPROVAL

SIGN

DATE

DISTRIBUTION:

400-938

3. PRODUCT SPECIFICATION

CSD/005/PSP/0078

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821209/HMS

Indtil næste plastlomme
trykkes med For- og Bagside.

TITLE: STANDARD FLOPPY DISK CONTROLLER
CR8047M/010XX/00
PRODUCT SPECIFICATION

DOCUMENT NO : CSD/005/PSP/0078

PREPARED BY : BERTRAM PÅSKESEN

AUTHORIZED BY : GOTTLOB BORUP

DISTRIBUTION : BBP, GB, PRO(2), KFL(4), FILE(2)

APPROVED BY:

AUTHORITY	DATE	SIGNATURE
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ISSUE: 3

DATE: 820916

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STANDARD FLOPPY DISK CONTROLLER
CR8047M/010XX/00

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1. SCOPE

This document specifies the operation and Main Bus Interface for ST FD CTRL/010--/00, single or dual bus type.

The modules are both parts of the CR80D Standard Product Line.

The following versions are described:

CR8047D/010AB/00	Dual Main Bus
CR8047D/010A-/00	Single Main Bus

1.1 Applicable Documents

Product specification CR80D
Mainbus
CSD/005/PSP/0033

OEM Manual for Shugart SA 800/801 diskette storage drive.
Service Manual for Shugart SA 850/851 diskette storage drive.

Maintenance manual for Shugart SA 800/801 diskette storage drive.

2. INTRODUCTION

The ST FD CTRL performs the interface between the CR80D computer system and up to 4 floppy disc drives, type SA 800/850.

The dual bus version is designed for use in the high reliable redundant system and the module may be accessed from either main bus A or main bus B (connnector P1 or P2). The module may of course, also be used in a single bus system, if system software is able to handle the bus-switch commands. (See section 4.6), and supply voltages are increased in accordance to specifications (see sec. 4.5).

The drive(s) is (are) connected to the module via P3 and a standard Floppy Disc Adapter (SFA), see figure 2.

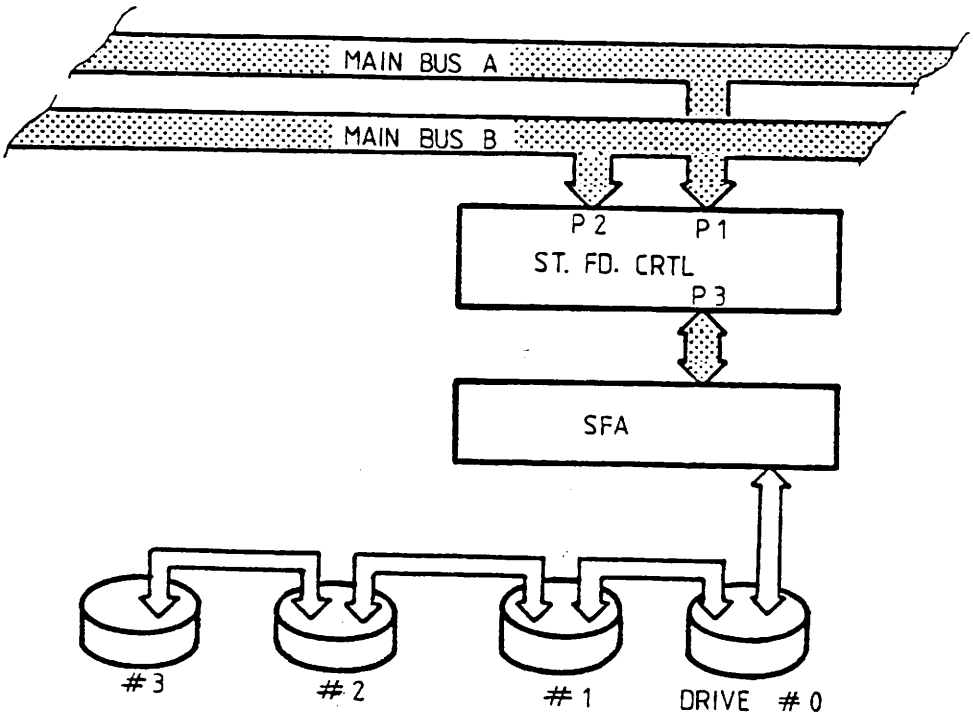


Fig. 2

The single bus version is intended for small system, and connection to the drives is normally performed via the CSA module. See figure 3.

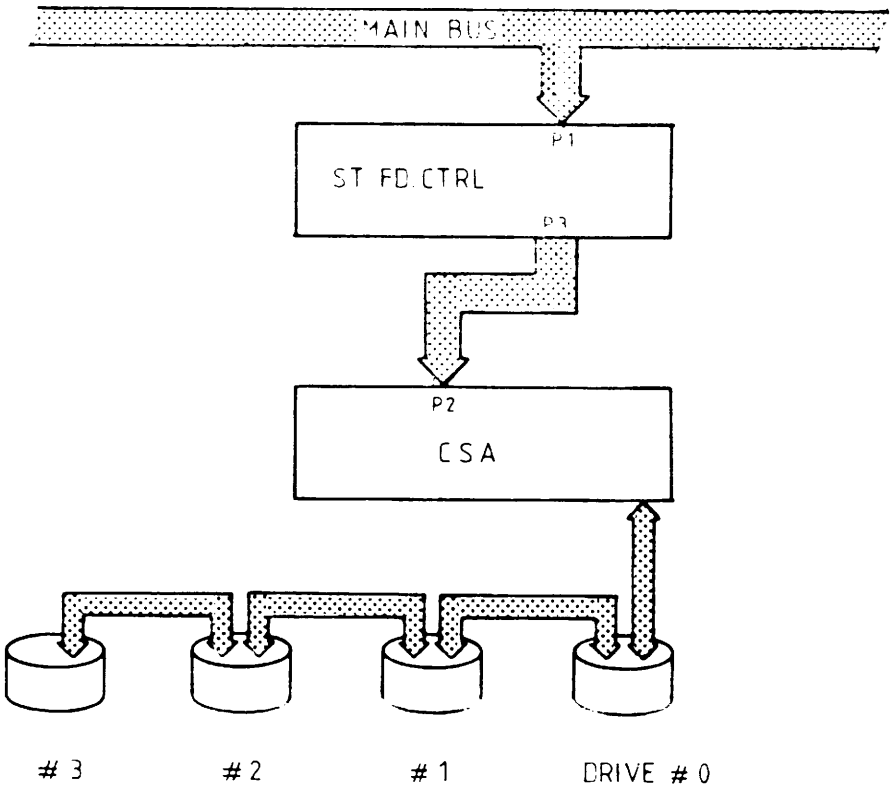


Fig. 3

3. FUNCTIONAL OVERVIEW

The modules perform necessary timing and buffering between CR80D and the Floppy Disc drive.

The maximum buffer length is equal to 1 sector $\approx$ 128 bytes of data.

The drive interfacing hardware is identical on both module versions.

3.1 Dual Bus Version

For use in redundant systems a busswitch is included for dynamical switching between two main buses. The buss-election is issued from the processing unit. Figure 3.1-1 shows the functional block diagram of the module.

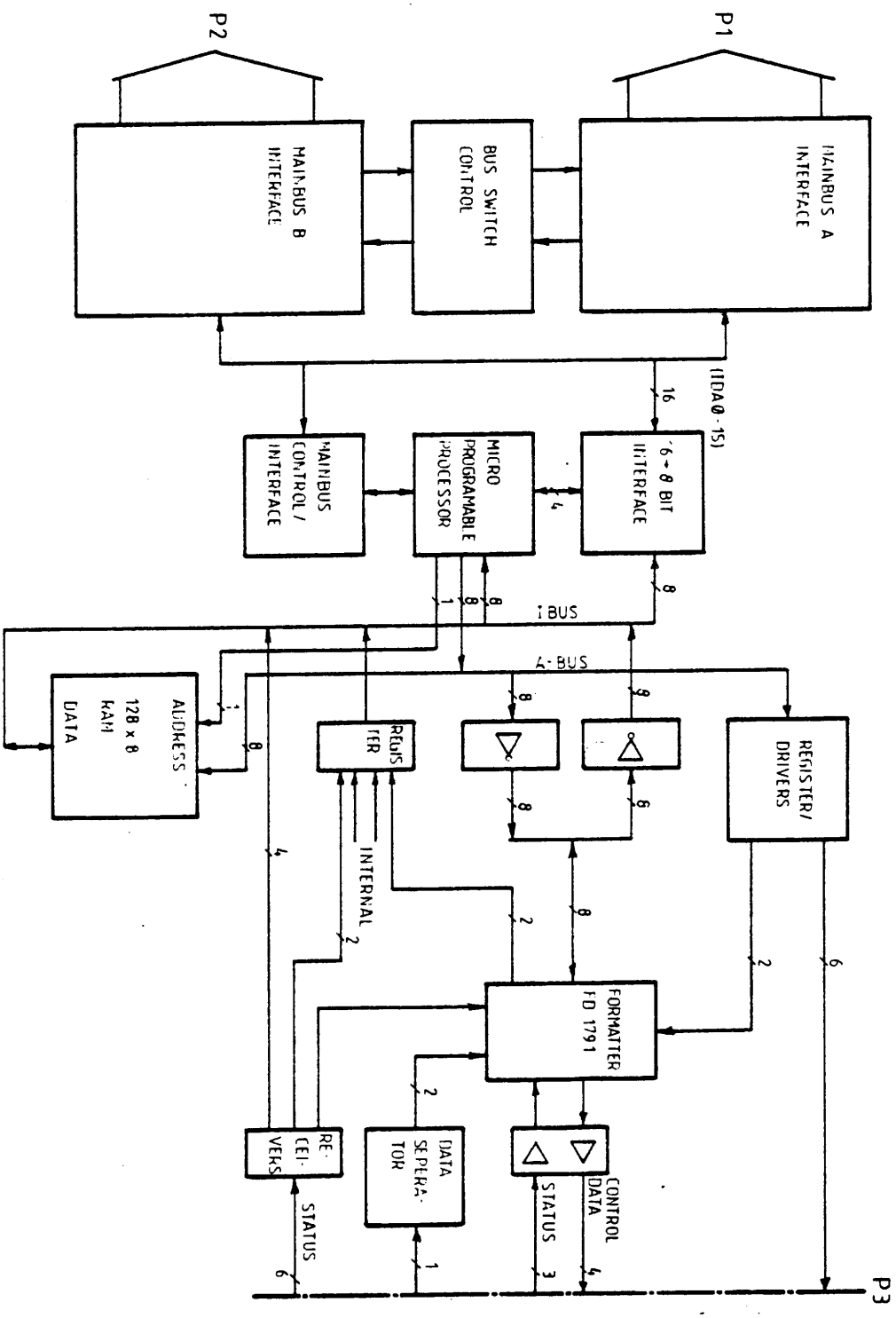


Fig. 1

Figure 3.1-1 BLOCK DIAGRAM

CHRISTIAN ROVSING A/S					
St. F.D. Ctrl. Dual, CR8047D/010AB/00	Scale		Approved	Issue	1
	Date	81-02-12	E	Date	81-02-12
	Drawn	BBP/MZL		Approved	
	Parts no		3-2843		
Block Diagram	Print no		Sheet 1 of 1 sheets		

Parity generating is performed at every CPU RIO operation to the module. Parity check of received data at CPU WIO is implemented. A failed check (Parity Error) will cause:

a) The generation of an interrupt

b) The Parity Error bit in auto status to be set . (See section 4.1.2)

c) If the failed dataword is a part of a "Normal System Command" (see section 4.1.1) the command is ignored. If the data word was particular for the sector buffer, normal actions as described in section 4.1.3 will occur.

A Bus enable command to either bus A or B must always be issued, previous to any command to the controller part (see section 4) of the module.

Further information about busswitching is described in section 4.6.

3.2 Single Bus version

This module does not include the switchable mainbus interface and it will always respond to any valid I/O command.

Parity generating and checking is not performed.

Figure 3.2-1 shows its functional blockdiagram

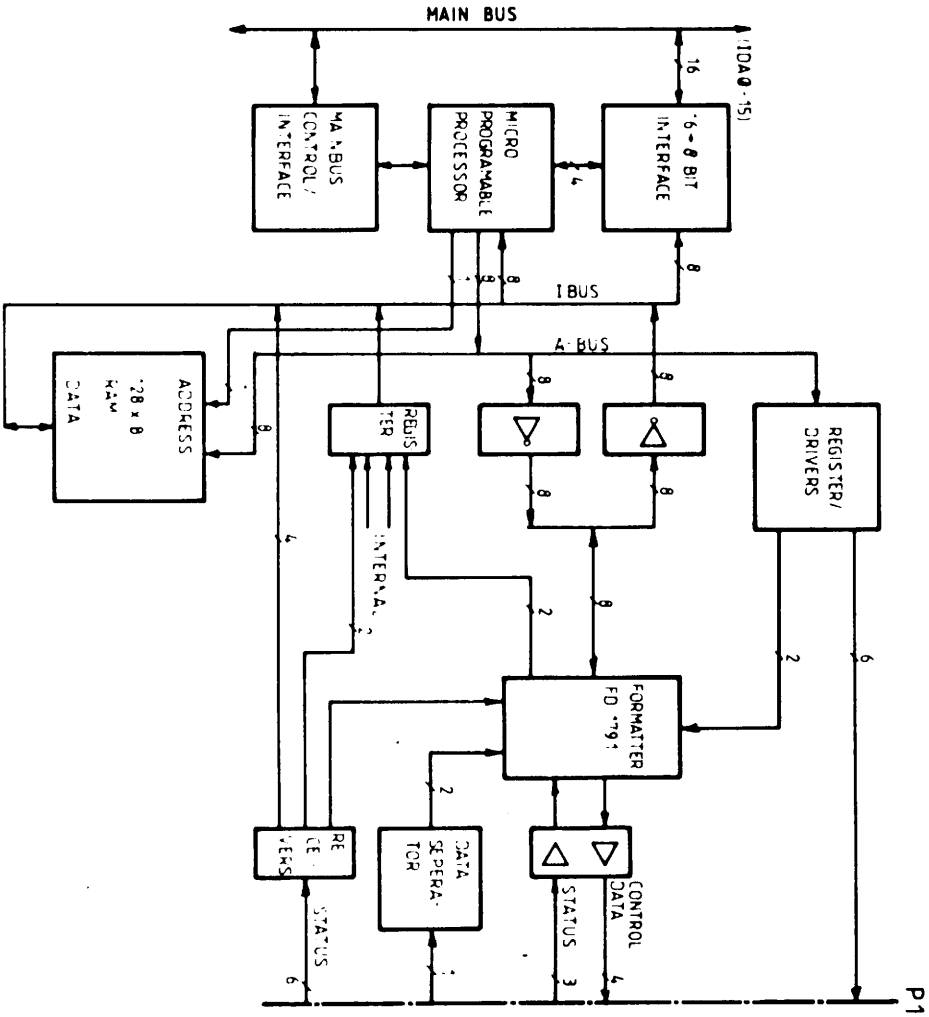


Fig 1

Figure 3.2-1 BLOCK DIAGRAM

CHRISTIAN ROVSING A/S					
Floppy Disk Ctrl., CR 8062	Scale		Approved	Issue 1	
	Date 81-09-20			Date 81-09-20	
	Drawn JKH/MZL			Approved JKH /MZL	
	Parts no		3-3035		
	Print no		Sheet 1 of 1 sheets		

4. SPECIFICATIONS

In this section the detailed specification is given.

4.1 CPU Instructions

The Floppy Disc Controller accepts the follwing instructions:

1) WIO: Write a 16 bit data word

2) RIO: Read a 16 bit data word

In order to use software designed for unmapped system, two straps might be changed. This modification will make the module also to accept:

1) CIO: "Control", i.e. write a command

2) SIO: "Sense", i.e. read auto status

It shall be noted that CIO functionally is equal to a WIO in fact the only thing the modification do is to select address bit 17 instead of bit 7 and addr. bit 15 instead of addr. bit 6.

ACCESS RATE FROM MAINBUS

The internal operation speed is fast enough to ensure proper mainbus service without any limits in software access rate. One exception is the WIO-RIO sequence, which will cause in an mainbus time out, if the access rate is too fast. See table 4.1

INSTRUCTION SEQUENCE	MINIMUM TIME BETWEEN ACCESS
WIO WIO	No limits
RIO WIO	No limits
WIO RIO	4 usec
RIO RIO	No limist

Table 4.1

4.1.1 WIO, Write a System Command

The format of the system commands are shown on the next pages.

Each command has as an integral part the Floppy Disc drive number to which it pertains. This provides the ability to intersperse commmands to different drives.

When a system command is given, transfers between the formatter and the disc drives take place, and it is necessary to wait for the completion of the command.

The completion of the command is indicated in two ways:

1. The additional status changes from BUSY to NOT BUSY

2. An interrupt is generated

SYSTEM COMMANDS:

CPU Instruction: WIO

ADDRESS BITS																FUNCTION
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
X	X	X	X	0	X	X	X	0	0	A	A	A	A	A	A	Normal system command. The command type is specified in the data word.
X	X	X	X	0	X	X	X	0	1	A	A	A	A	A	A	Reset RAM Buffer pointer.

AA Module device address
XX don't care

DATA WORD FOR NORMAL SYSTEM COMMAND

DATA BITS																FUNCTION
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	D	D	X	X	X	X	X	X	X	X	Select drive
0	0	1	0	0	0	D	D	T	T	T	T	T	T	T	T	Seek track
0	1	0	0	0	0	D	D	x	x	x	x	x	x	x	x	Restore head
0	0	0	1	0	S	D	D	R	R	R	R	R	R	R	R	Read initial Record
0	0	0	0	1	S	D	D	R	R	R	R	R	R	R	R	Write initial Record
0	0	1	0	1	S	D	D	R	R	R	R	R	R	R	R	Write deleted record

TT	Track number (0:78)
RR	Record (sector) number (1:26)
S	Discette side (1:0)
DD	Drive number (0:3)
XX	Don't care

Limits of numbers (TT, RR, DD) are specified in brackets

Command definitions follow.

Select

This command performs drive selection and presents the following status (if the status condition exists):

1. DRIVE NOT READY

2. WRITE PROTECT

3. TWO SIDED

The selected drive would not be ready if a discette is not properly installed or the drive is not up to operational speed. WRITE PROTECT status indicates that the discette may only be read. TWO SIDED status indicates that a discette with data tracks on both sides is installed (SA 850 only).

Seek

The track number passed within the SEEK command is located and verified automatically. If the verify does not succeed within 4 revolutions of the discette, a SEEK ERROR status is presented. A successful completion of a seek indicated by track address comparison and CRC check would set SEEK COMPLETE status. A CRC error would set ID DATA CHECK status after four verify attempts. Present track address is maintained for each drive at all time.

Restore

The RESTORE command causes the drive to step out max. 256 times and tests for a TRACK 00 signal. Upon issuing 256 steps, if TRACK 00 fails to be detected, a RECALIBRATE ERROR status is set. When the TRACK 00 signal is detected, a verify is performed as for SEEK.

Read

The READ command is initiated after a SEEK or RESTORE command. The drive orients to the sector number within the command. Data is read from that sector until one of the following occurs:

1. A full sector has been read

2. An error is detected

If the record ID fails to compare without an ID DATA CHECK error after 4 disc revolutions, the READ operation is terminated and an ID NOT FOUND status will be presented.

If the data field CRC check fails, the status DATA CHECK will be presented.

Write

The WRITE command is initiated after a SEEK or RESTORE command. The drive orients to the sector number within the command and the FB data pattern indicating the record address mark is written to precede the record data field. The write operation continues until one of the following occurs:

1. A full sector has been written

2. An error is detected

If the record ID fails to compare without ID DATA CHECK error after 4 disc revolutions, the WRITE operation is terminated and an ID NOT FOUND status is set.

Write Deleted Record

Identical to the WRITE command except that a F8 address mark is written instead of a FB.

4.1.2 RIO, Read Auto Status

When a RIO instruction is performed, the Floppy Disc I/F will put the auto status, the format of which is shown on the next pages, onto the Main Bus data lines.

RIO, Read Additional Status

When bit 7 in auto status is set, AD6 & AD7 are used to find out, which condition caused it.

The format of the additional status is shown on the next pages.

RIO Formats

	ADDRESS																
R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	FUNCTION
0	X	X	X	X	0	X	X	X	1	0	A	A	A	A	A	A	Read Data From Buffer RAM
0	X	X	X	X	0	X	X	X	0	0	A	A	A	A	A	A	Read Auto Status
0	X	X	X	X	0	X	X	X	0	1	A	A	A	A	A	A	Read Additional Status

AA = Modul Device Address
XX = Don't Care

4.1.3 WIO, Write Data

WIO transfers a 16 bit data word into the sector buffer (16 bits times 64 word of RAM). The address of the RAM is automatically incremented after each instruction.

NOTE: Before filling the sector buffer, the RAM Buffer pointer should be reset, by issuing a WIO System Command.

WIO is used before giving a WRITE og WRITE DELETED command.

WIO Formats

	ADDRESS																
R/W	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	FUNCTION
1	X	X	X	X	0	X	X	X	1	0	A	A	A	A	A	A	WRITE DATA TO BUFFER

AA = Modul Device Address
XX = Don't Care

4.1.4 RIO, Read Data

RIO transfers one 16 bit data word from the sector buffer (RAM). The address of the RAM is automatically incremented after each RIO instruction. The readformat is shown on next page.

When RIO is used after a DISC READ command, the sector buffer contains the addressed sector, even if the status bit DATA CHECK or DELETED RECORD was set.

4.1.5 (Reset) RAM Buffer Pointer

WIO (ADDRESS) is used to reset the address of the sector buffer (16 bit times 64 words of RAM). The RESET POINTER instruction should be used before issuing the first WIO instruction while filling the sector buffer.

Note: The address of the sector buffer is automatically reset at the start and at successful termination of either of the commands: READ, WRITE, WRITE DELETED.

AUTOMATIC STATUS ERROR CODE

Bit Position	Description	Definition
0	Seek Complete	Seek command was executed successfully
1	ID DATA CHECK	CRC failed to compare in the ID field
2	PROGRAM ERROR	Invalid command
3		Undefined
4	DATA CHECK	CRC check failed on the data field
5	ID NOT FOUND	Search of the ID field was not successful after 5 revolutions.
6	EQUIPMENT CHECK	Resident Microdiagnostics failed
7	ADD. STATUS NOT ZERO	One or more bits in the additional status (see later) are set
8	WRITE PROTECT	Selected drive is write protected
9		Undefined
10		Undefined
11	DRIVE NOT READY	Selected drive is not ready

AUTOMATIC STATUS ERROR CODE

Bit Position	Description	Definition
12	SEEK ERROR	Upon completion of the SEEK or RESTORE command, the track address does not compare
13	RECALIBRATE ERROR	Track 00 was not detected in response to a RESTORE command
14		Undefined
15	PARITY ERROR	Parity check of received data from Mainbus, failed. Parity error detected.

ADDITIONAL STATUS CODE

Bit Position	Description	Definition
0	DISK CH 0	Disk Change, Drive 0
1	DISK CH 1	Disk Change, Drive 1
2	DISK CH 2	Disk Change, Drive 2
3	DISK CH 3	Disk Change, Drive 3
4	DEL REC	DELETED RECORD, i.e. a F8 AM found during a read operation
5	OVERRUN	HANDSHAKE ERROR, transfer between floppy disk drive and sector buffer failed
6	BUSY	The formatter is executing a command
7	TWO SIDED	The selected drive contains a two sided discette
8-15	UNDEFINED	

K

4.2 Data Format

CR8047D/010AB/00 is designed for IBM soft sectoring formats with following specifications:

Single Density (FM):	128 bytes/sector	(IBM 3740)
Standard Floppy:	26 sectors/track	(1 - 26)
	77 tracks/side	(0 - 76)
	1 or 2 sides/discette	(0 - 1)

4.3 Timing of Operations

Head Loading and Unloading

The head is loaded each time a READ, WRITE or VERIFY is to be executed.

The head is unloaded:

1) When the unit number is changed or

2) When 0.5 sec. has lapsed since the latest reading or writing

In the specifications below, "head load" time is 35 ms if the unit number has been changed or more than 0.5 sec. has lapsed since the latest disc operation. Otherwise "head load" is 0.

SEEK: With VERIFY: 1) no-of-track . track-to-track + settling + latency

or

2) head load, whichever is largest

Drive Type	SA850	SA800
track-to-track	3 ms	10 ms
settling	15 ms	15 ms
latency	<7 ms	<7 ms
arv. SEEK + VERIFY	100 ms	280 ms

RESTORE: Max. 77 track-to-track
Min. 35 ms

READ OR WRITE: Head load + latency + length

Latency:

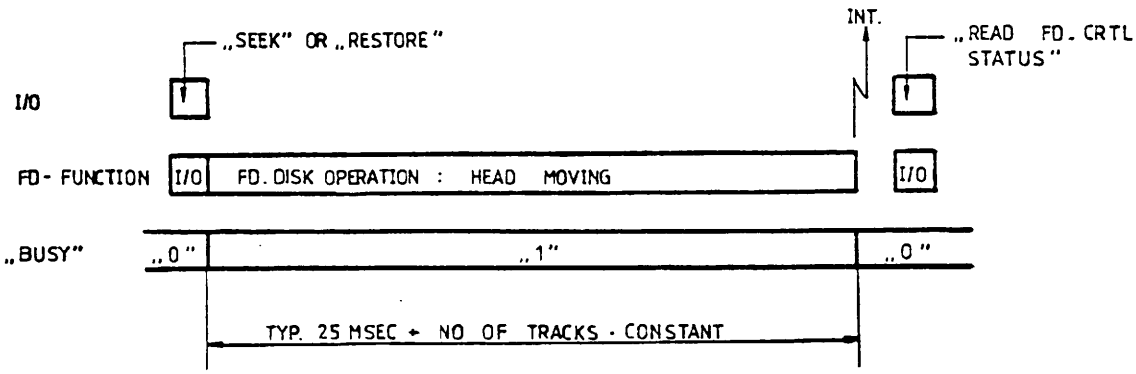
SA850	SA800
<170 ms	<170 ms

Head Load: See text "Head loading and unloading" above.

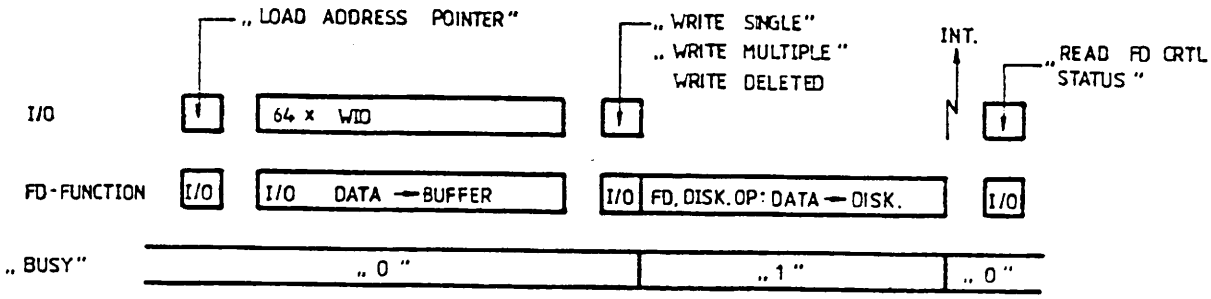
Length (single sector) for SA800/850: 7 ms

The following 3 figures show 3 sequences used in normal operation using interrupt:

Seek or Restore Sequence

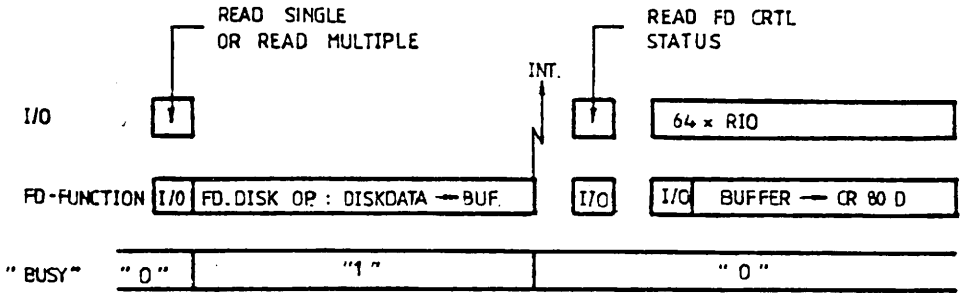


Write Sequence



K

Read Sequence



4.4 Interrupt Conditions

The Floppy Disc I/F generates on interrupt when one or more of the following happens:

a) Its status changes from busy to not busy

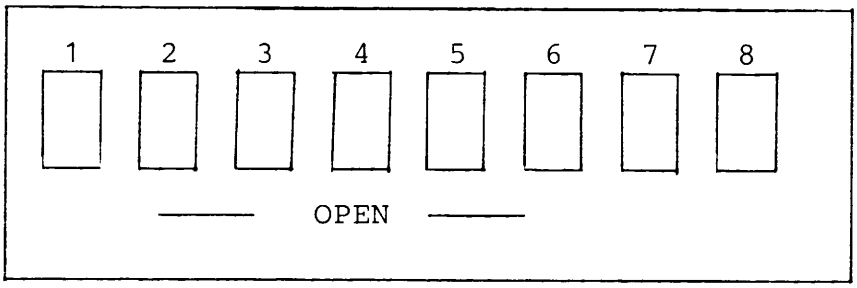
b) When the disc drive door is closed after changing the disc

c) When the controller detects a parity error of received data from Mainbus (During CPU WIO operations)

d) At the completion of the internal test routine (BIT)

Action c), d) is not taken by the single bus version of ST FD CTRL.

The priority and device address are programable by means of S1:



SW 1 - 6 define device address in binary code.
1 is LSB

SW 7 - 8 define interrupt priority in binary code.
7 is LSB

An open switch is equal to a logical one.

4.5 Power Requirements

Dual Bus Version:

+5V Pin No. AB 40 - 41:	4.2A
+12V Pin No. AB 14:	25 mA

The power consumption listed is the total amount, from either the A-BUS or the B-Bus

Single Bus version:

+ 5V Pin No. AB 40 - 41 :	3.2A
+12V Pin No. AB 14	25mA

4.6 Busswitching Commands

These commands can be issued from every address sourcing module during either a WIO or RIO operation. The busswitching can be controlled from the A or B Bus.

Command Format

CPU instruction. WIO, RIO, SIO or CIO

ADDRESS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	FUNCTION
X	X	X	X	1	0	0	X	X	X	A	A	A	A	A	A	Disable module, reset
X	X	X	X	1	0	1	X	X	X	A	A	A	A	A	A	Enable switch, reset

AA = module device address
XX = don't care

Disable Module, reset

By this command the Floppy Disc Controller is disabled from both main buses and the module is reset to a well defined state.

The command will cause the TEST LED to turn on.

Enable Switch, reset

By this command the Floppy Disc Controller is disabled from the other bus, and enabled onto the bus, which is sourcing the command. Furhtermore the command will clear the module. Transfer on the other bus will be destroyed.

Enabling of an already enabled Bus I/F will cause a program clear (PCL) signal to the internal Micro Controller.

NOTE: Any PCL-commands to the module will force Micro Controler to its BIT sequence. (See section 7).

The enable command is internally latched, and thus perform a permanent enable state, until a bus disable command is received or an internal powerfailure is detected.

4.7 Front Panel LEDS

On the front panel five LEDS are mounted.

"POWER" (green) is turned on when the +12V and +5V are turned on. Both power voltages are supervised by power detection circuits.

The LED is on if the V_{CC} (normally 5.0V) is above 4,85V and V_{DD} (normally 12,0) is above 11,7V.

"TEST" (red) is turned on after every Master Clear. The LED is turned off after end of BIT sequence of internal microprogram. (See section 7)

"BUS A" (yellow) indicates that the ST FD CTRL is enabled onto Main Bus A.

"BUS B" (yellow) indicates that the ST FD CTRL is enabled onto Main Bus B.

Note: Both BUS-LEDS are turned off at power up
The BUS-LED's are never active at the same time.

"BUSY" (yellow) is turned on when the ST FD CTRL is busy executing system commands (further information in statusword description)..

NOTE: The single bus version is only equiped with "POWER" and "BUSY" LEDS

4.8 Mechanical Dimensions

The device is a standard 1M CR80D module with 3
3 x 43 pin edge connectors for Main Bus Interface and I/O connections.

Height:	412.6	mm
Width:	17	mm
Length:	304	mm
Weight:	1,1	kg.

5. STRAP OVERVIEW

5.1 Dual Bus Version

Application: Drive: SHUGART SA 800/850
Discette Format IBM 3740

SR1	in position	B	
SR2		B	
SR3	A		
SR4	A		
SR5		B	
SR6		B	
SR7		B	
SR8		B	
SR9		B	
SR10			C
SR11	A		
SR12		B	
SR13		B	
SR14		B	

SR11 must be mounted in position A, when issue 2 or newer firmware (PROM 1768 -XX - 1774-XX) versions are used else mount in pos B.

5.2 Single Bus Version

Application: Drive: SHUGART SA 800/850
Discette Format: IBM 3740

Software: Address bit 6 and 7 used to distinguish command type

SR1	in position	B
SR2		B
SR3	A	
SR4	A	
SR5	A	
SR6	A	
SR7	A	
SR8	A	
SR9		B
SR10	A	
SR11		B
SR12	A	
SR13	A	

5.3 Single Bus Version

Application: Drive: SHUGART SA 800/850
Discette Format: IBM 3740

Software: Address bit 15 and 17 used to distinguish command type. This strapsetting is valid for "old" driver software (AMU and System ONE FD BOOT).

SR1	in position	A	
SR2		A	
SR3		A	
SR4		A	
SR5		A	
SR6		A	
SR7		A	
SR8		A	
SR9			B
SR10		A	
SR11			B
SR12		A	
SR13		A	

6. SCHEMATIC OVERVIEW FOR COMMAND DECODING

CPU INS.	AD7 AD17	AD6 AD15	R/W R/W	Function
SIO	Ø	Ø	Ø	Read Auto Status
CIO	Ø	Ø	1	Write Command
SIO	Ø	1	Ø	Read Additional Status
CIO	Ø	1	1	Clear Pointer
RIO	1	Ø	Ø	Read Data from Buffer
WIO	1	Ø	1	Write Data from Buffer
RIO	1	1	Ø	Reserved
WIO	1	1	1	Reserved

7. BUILD IN TEST (BIT)

This section is only valid for the dual bus version.

After Power-up 3 LED's: POWER, TEST and BUSY on the front panel will turn ON, indicating the following:

A power failure is detected (during power-up), the busswitch is disabled. The module is ready to start its BIT when it receives an "Enable Busswitch Command" (See section 4.6).

When the module is runnning its BIT and if an error is detected it willnot respond to Mainbus access concerning the command (WIO and RIO) described in section 4.1.

The Maximum execution time for BIT is approx. 4,8 sec, and if an interrupt is not received from the module within this time, an error is detected.

An H/W error detected during BIT will force the module to a welldefined state and the Test LED will remain lighting.

If the BIT is completed without any error detected, an interrupt is generated, the status register updated, and Mainbus access is serviced. The BIT sequence will clear the buffer RAM.

The BIT-sequence will also be activated by receiving a PCL. (see section 4.6).

BIT Funtion

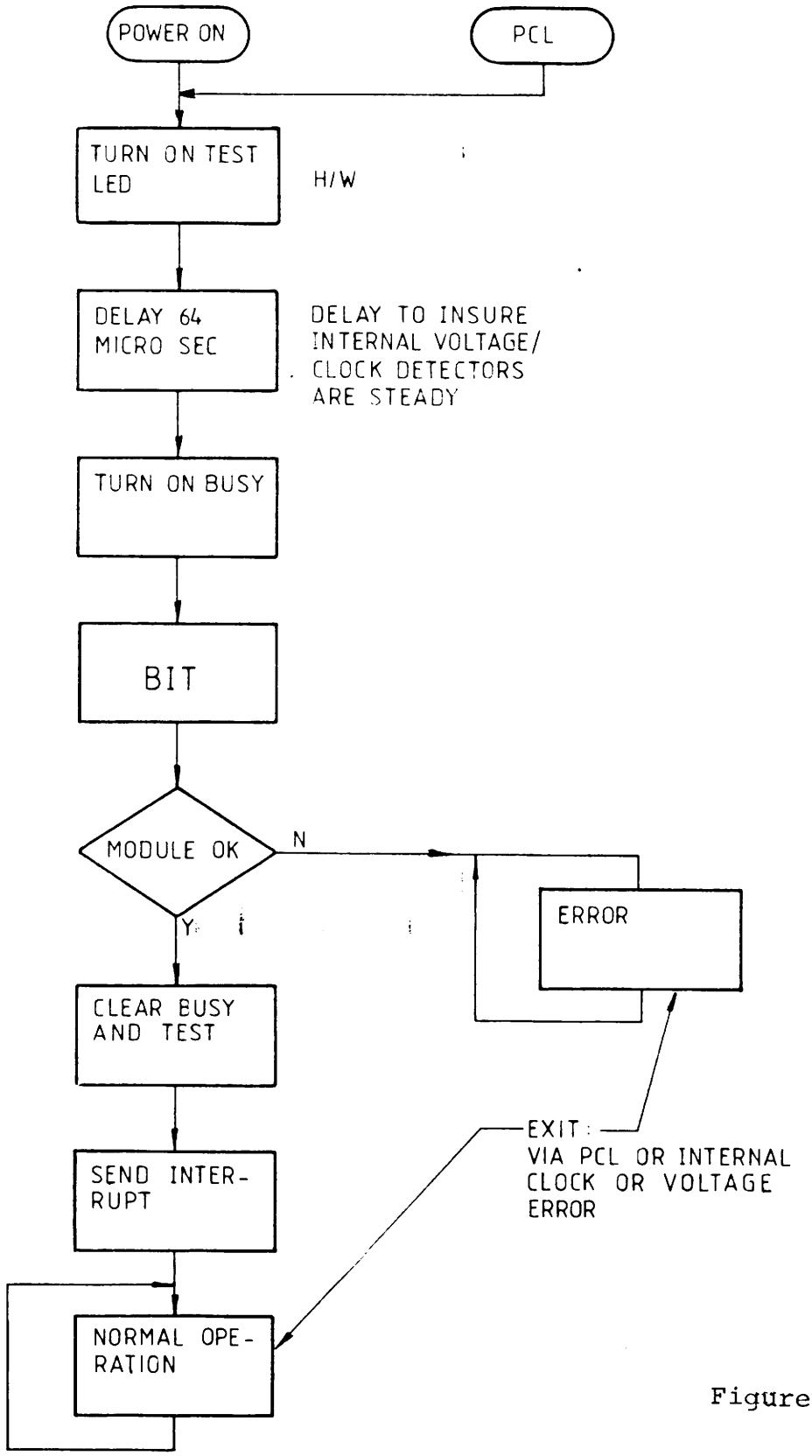


Figure 7-1

4. FUNCTIONAL DESCRIPTION

CSD/005/FNC/0032

K

821209/FM

Indtil næste plastlomme
trykkes med For- og Bagside

TITLE: FUNCTIONAL DESCRIPTION FOR ST.FD.CTRL CR8047M/010XX/00

DOCUMENT NO : CSD/005/FNC/0032

PREPARED BY : BERTRAM B. PAASKESEN

AUTHORIZED BY: JESPER KNUTZEN

DISTRIBUTION : PRO(3), LVN, BBP, FILE(1), KFL(7)

APPROVED BY:

AUTHORITY	DATE	SIGNATURE
EDD/JKZ	820601	

ISSUE: 2

DATE: 820413

400-810-1

FUNCTIONAL DESCRIPTION FOR ST.FD.CTRL	sign/date BBP/820413	page i
	repl	project

PAGE RECORD AND ISSUE LOG.

PAGE	ISSUE 1	2	3	4	5	6	7	8
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100								

ISSUE	DATE	PREPARED BY	APPROVED BY	AUTHORIZED BY
1	810901	BBP	JKZ	JKZ
2	820413	BBP	JKZ	JKZ

LIST OF CONTENTS

CSD/005/FNC/0032
BBP/820413

1. SCOPE

This manual describes the detail function of the Standard Floppy Disc Controller, CR8047M/010XX/00, which is a part of the CR80M product line.

Applicable Documents

1. Product Specification,
   ST. FD. Ctrl. CR8047D/010XX/00
   Doc. NO.: CSD/005/PSP/0078

2. OEM Manual for SHUGART SA800/850

3. Users Manual,
   Micro Assembler MICAS
   Doc. NO.: CSS/0000/USM/0019

4. Blocked Schematic 1 - 275 4 Sheets

2. INTRODUCTION

This document describes the detailed function of the CR8047M/010XX/00 Floppy Disk Controller.

Following versions are described:

CR8047M/010AB/00	Dualized Main Bus I/F
CR8047M/010A-/00	Single Main Bus I/F

The Floppy Disk Controller interfaces the CR80M Computer to max. 4 floppy disk drives.

3. Theory of Operation

Since the ST. FD. CTRL. consists of 3 major functional blocks (see figure 1), the functional description will be devided into 3 sections, one for each functional block.

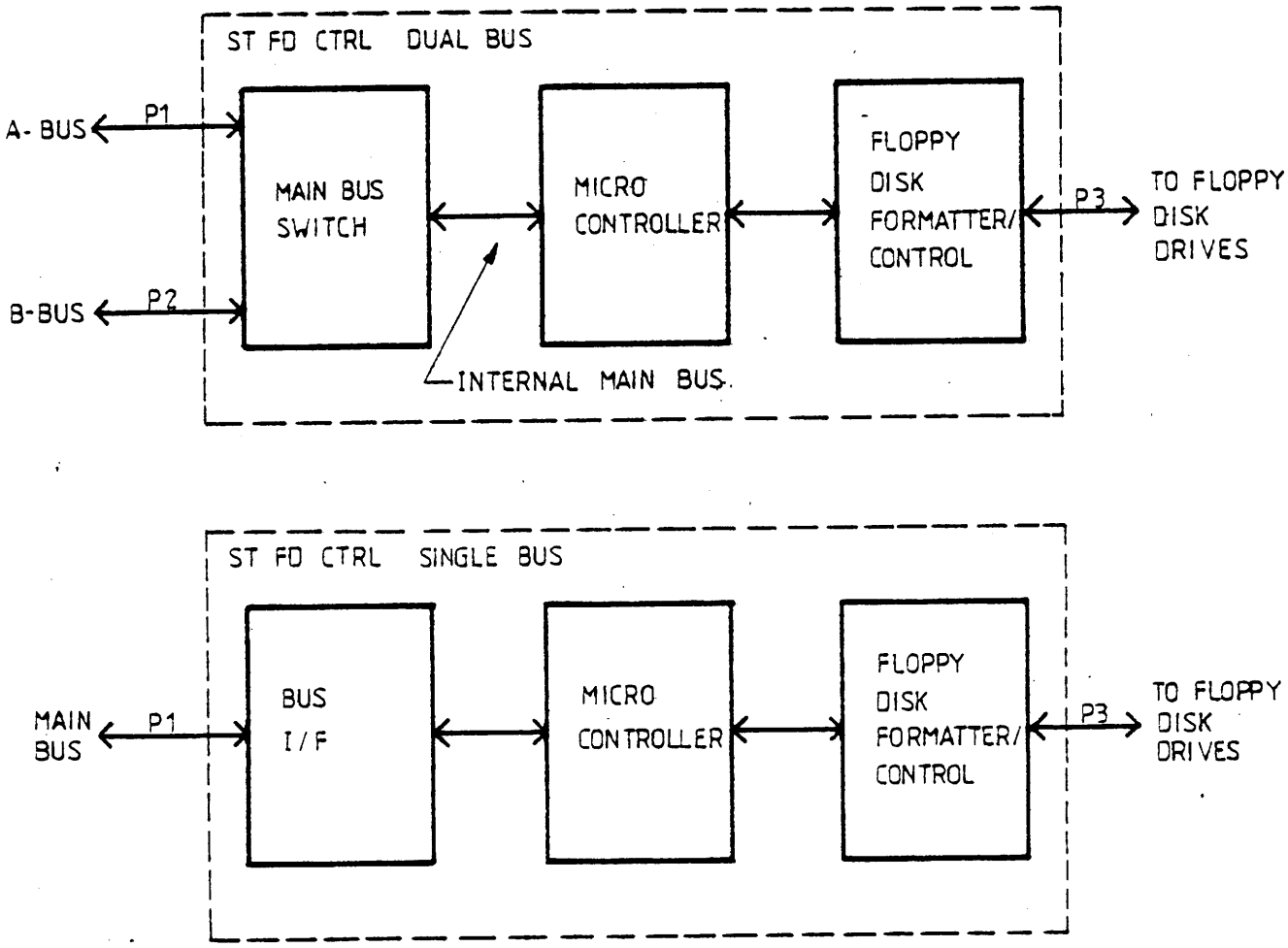
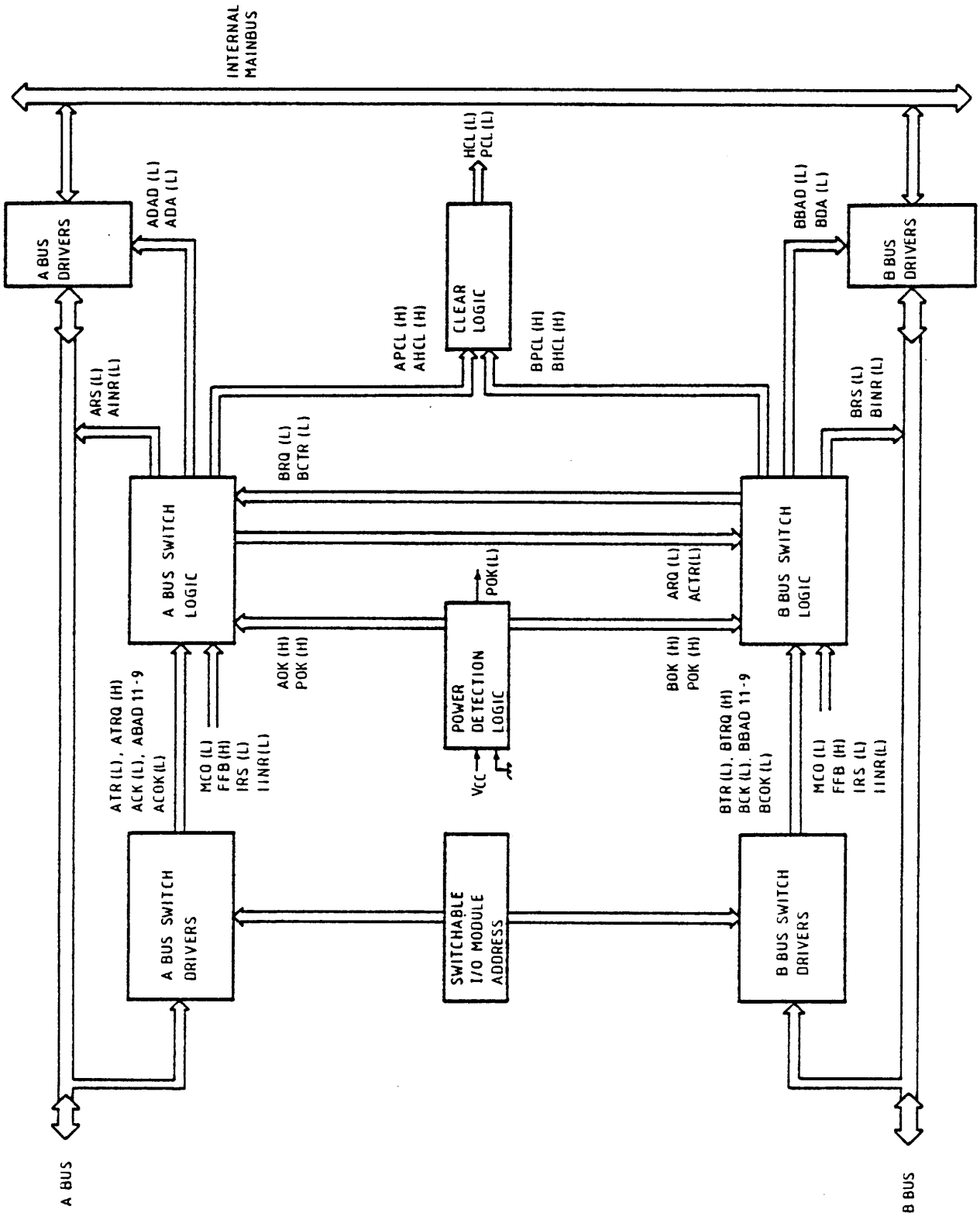


Figure 3-1

3.1 Main Bus Switch

This section is only valid for the dual bus version. Sections 3.1.1-3.1.5 describe the main bus switch, which is used in redundant systems for dynamical switching between the 2 Main Buses. Figure 3.1-1 shows a Block Diagram for the Main Bus switch.



CHRISTIAN ROVSING A/S

Fig. 3.1-1

CR80D Main Bus Switch

Block Diagram

Scale:		Approved	
Date:	81-06-16		
Drawn:	EBJ / AMR		
Parts no:		3-3000	
Print no		Sheet 1 of 1 sheets	

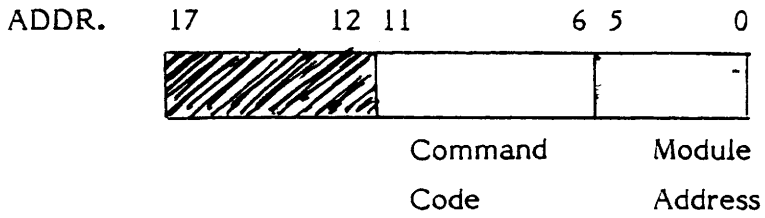
Issue	1
Date:	81-06-16
Approved	EBJ

3.1.1 L-ADR-1 A Bus Driver/Receiver
L-BDR-1 B Bus Driver/Receiver

The interface towards the Main Bus is designed to stay in the high impedance state during power up/down. The receivers/transmitters are disabled until the ST. FD. Ctrl. receives an "Enable and Reset" command as described in section 3.2.1. The control, data and address signals from the 2 Main Buses are gated onto an internal Main Bus with timing specifications in accordance with CR80M Main Bus specifications.

3.1.2 L-ABD-1 A Bus I/O Decoding
L-BBD-1 B Bus I/O Decoding

The ST. FD. Ctrl. accepts the following I/O commands.



Command Code

AD11-6	Function
000XXX	Normal I/O operation, i.e. Read or Write
100XXX	Disable Bus I/F, Reset
101XXX	Enable Bus I/F, Reset

If LS1, LS0 = 00 and address 0-5 match the module address switch setting (L-MADSS-1) the command code is decoded by the programmed PAL CR1590/CR1591.

If the module receives a normal I/O command, the signal I/O(L) is activated during the transfer.

If the module receives a command for the bus switch, CR1590/CR1591 generate the control signal for connecting/disconnecting the internal and external Main Bus. The timing diagrams on fig. 3.1.2-1 and 3.1.2-2 show the handshaking between the A Bus switch logic and B Bus switch logic for swithing between the two buses.

The signal FFB(H) shown on fig. 3.1.2-1 and 3.1.2-2 has no effect for the function of ST. FD. Ctrl. since the signal is tied "0"-level.

To prevent latch up of I/O decoding logic, due to the lack of Main Bus clock, two retrigable one-shots are included as watchdogs. Further these circuits will disable the actual bus I/F if the corresponding external bus disable signal (EABD or EBBD) is activated.

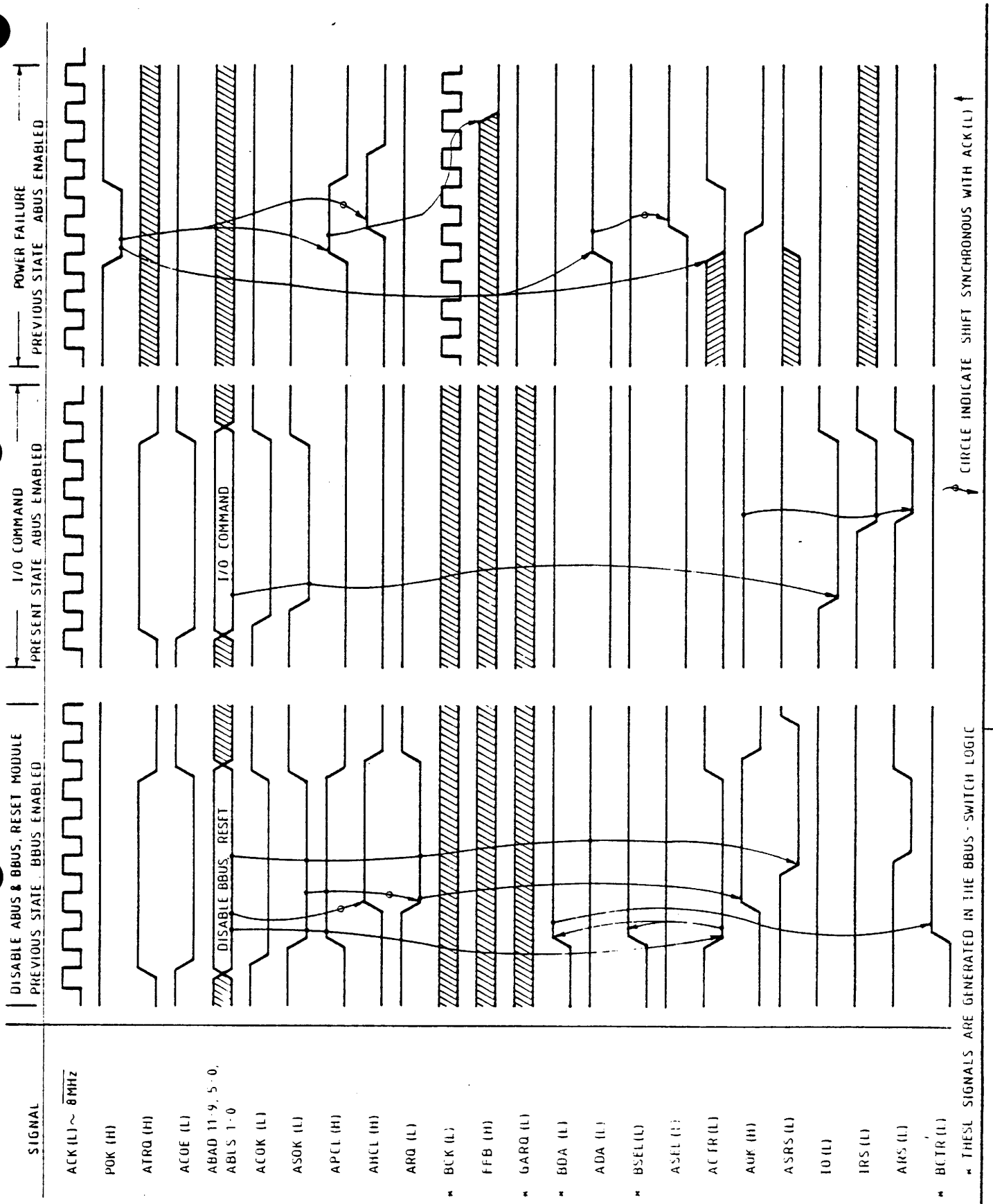


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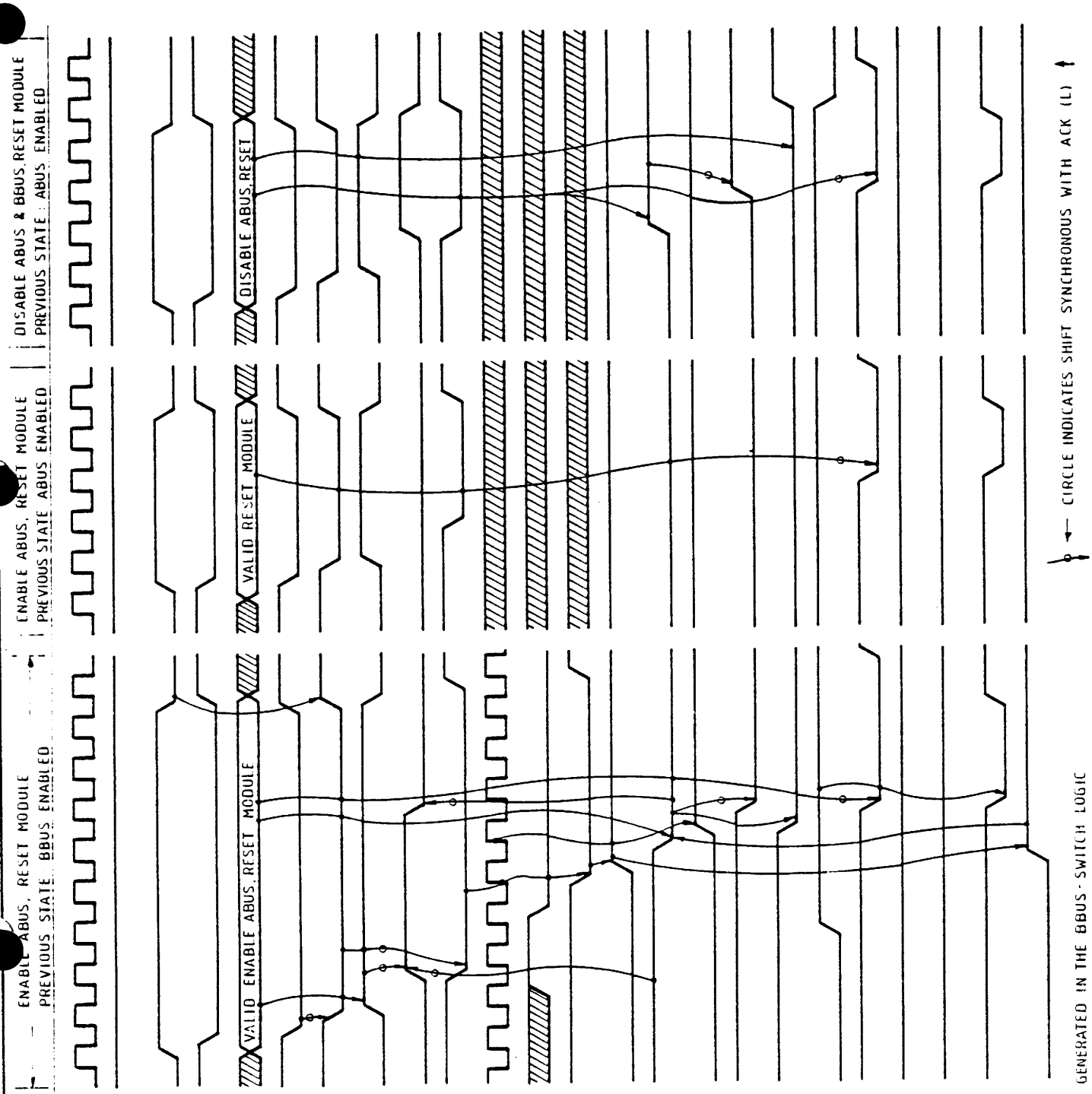
Fig. 3.1.2-1

CR80 Main Bus Switch

Timing Diagram

Scale		Approved	Issue 1
Date	81-07-03		Date 81-07-03
Drawn	EBJ / AMR		Approved EBJ
Parts no		3-2998	
Print no		Sheet 2 of 2 sheets	



CHRISTIAN ROVSING A/S

Fig. 3.1.2-2

CR80 Main Bus Switch

Timing Diagram

Scale		Approved	Issue
Date	81-07-03		Date 81-07-03
Drawn	EBJ / AMR		Approved
Parts no		3-2998	
Print no		Sheet 1 of 2 sheets	

3.1.3 L-ARID-1 Main Bus A Interrupt and Response Driver
L-BRID-1 Main Bus B Interrupt and Response Driver

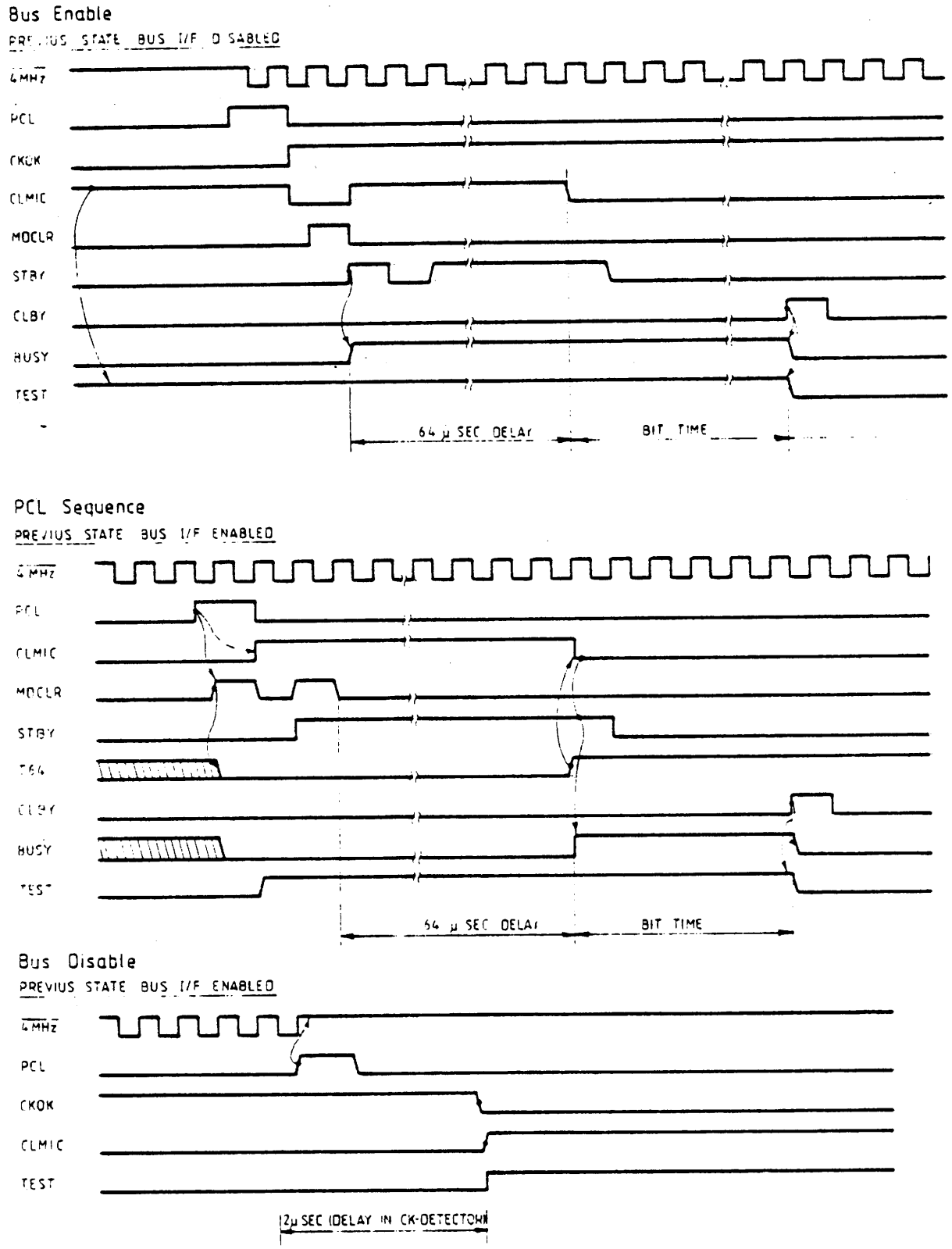
When the module has received an enable command and during a disable command the signal AOK(H)/BOK(H) is set, provided that there is no power failure. This enables the drivers for Response RS(L) and Interrupt Request INR(L). Furthermore the signal is feed to the A Bus/B Bus Indicator led on the front panel.

3.1.4 L-CL- 1 Clear Logic

Two clear signals are generated by the bus switch logic, PCL(L) (Programmed Clear) and HCL(L) (Hard Clear). Programmed clear is activated during all commands to the bus switch and resets the module to a well defined state. Hard clear disables the sending of interrupts immediately, while programmed clear disables the sending of interrupts at the end of an interrupt request cycle.

The signal Master Clear (MC(H)) on the Main Bus is normally not used in the ST. FD. Ctrl. It is possible to enable Master Clear with a strap for test purpose.

Figure 3.1.4-1 shows the Timing Diagram of the Clear situations in the dual bus ST. FD. Ctrl. Figure 3.1.4-2 shows the Block Diagram.



CHRISTIAN ROVSING A/S

Fig. 3.1.4-1

CR 8047 /010 AB/00
Interface Signals between Bus Switch Logic and Main Bus PAL

Scale		Approved	
Date	81-09-24		
Drawn	BBP/MZL		
Parts no		3-3044	
Print no		Sheet 1 of 1 sheets	

Issue	1
Date	81 09 24
Approved	MZL

Clear Logic Block Diagram Dual Bus Version

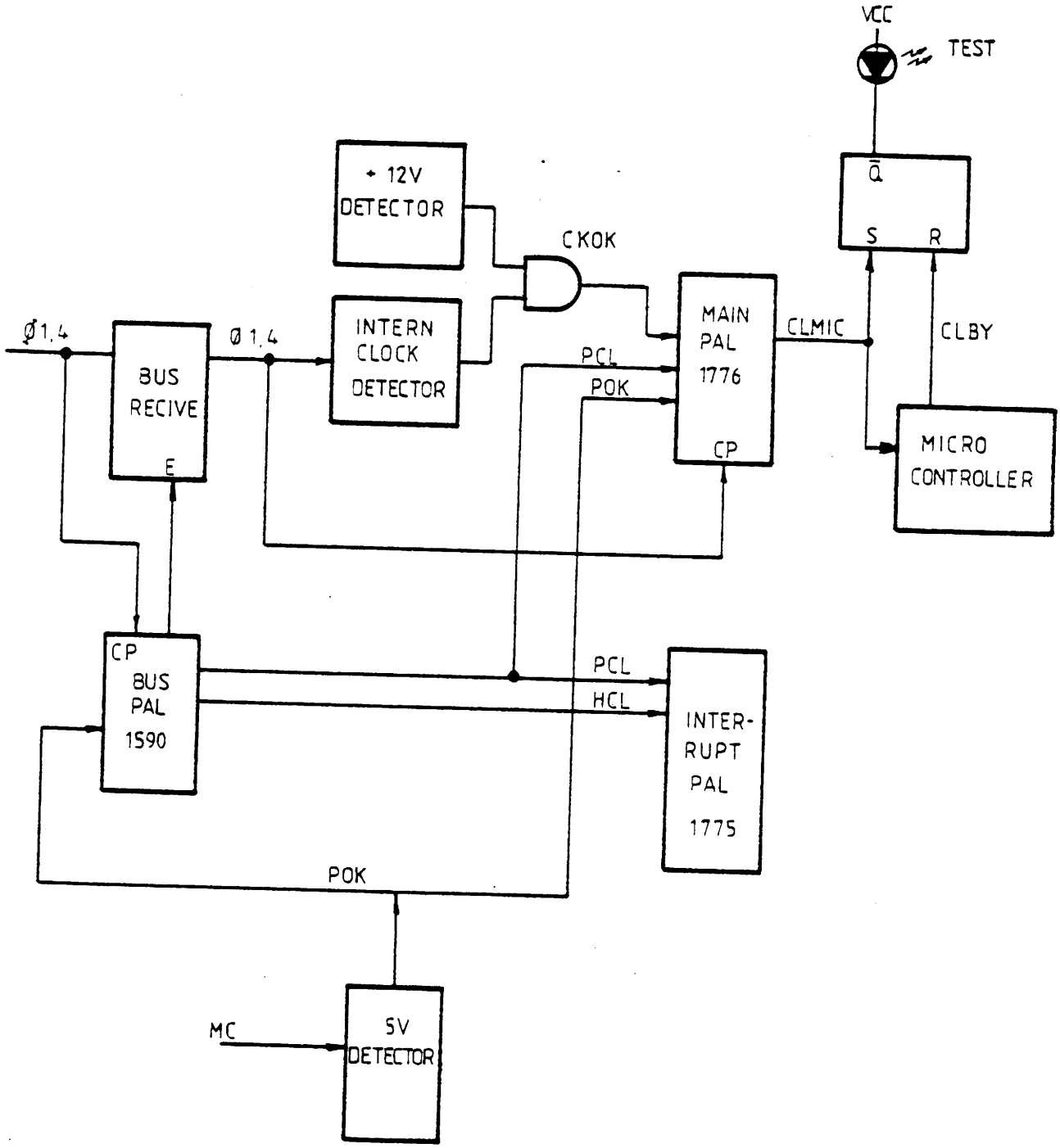


Figure 3.1.4.2

3.1.5 C-PS-1&2 Power Switch
C-VD-1 Voltage Detector

The module receives power from Main Bus A and Main Bus B. In case of a power drop out on one bus, the power switch controls that all power is taken from the other bus, and no power failure occurs.

The power switch includes a current limitting function with fold back. Furhtermore a PTC, R24, mounted on the heat sink for the two power transistors Q2 and Q3 ensures that the voltage regulator is "shut down" if the temperature of the transistors exceeds 100°C.

By means of a delayed ground pin DELGND on the A-Main Bus connector, power is not supplied to the board before all other pins are connected.

The voltage detector supervise V_{CC}, and will in case of voltage drop-out (V_{CC} less than 4.8V), immediately disable both Main Bus interfaces, and cause the issuing of proper clear signals to the controller part of the module.

3.2 Micro-Controller L-MIC-1

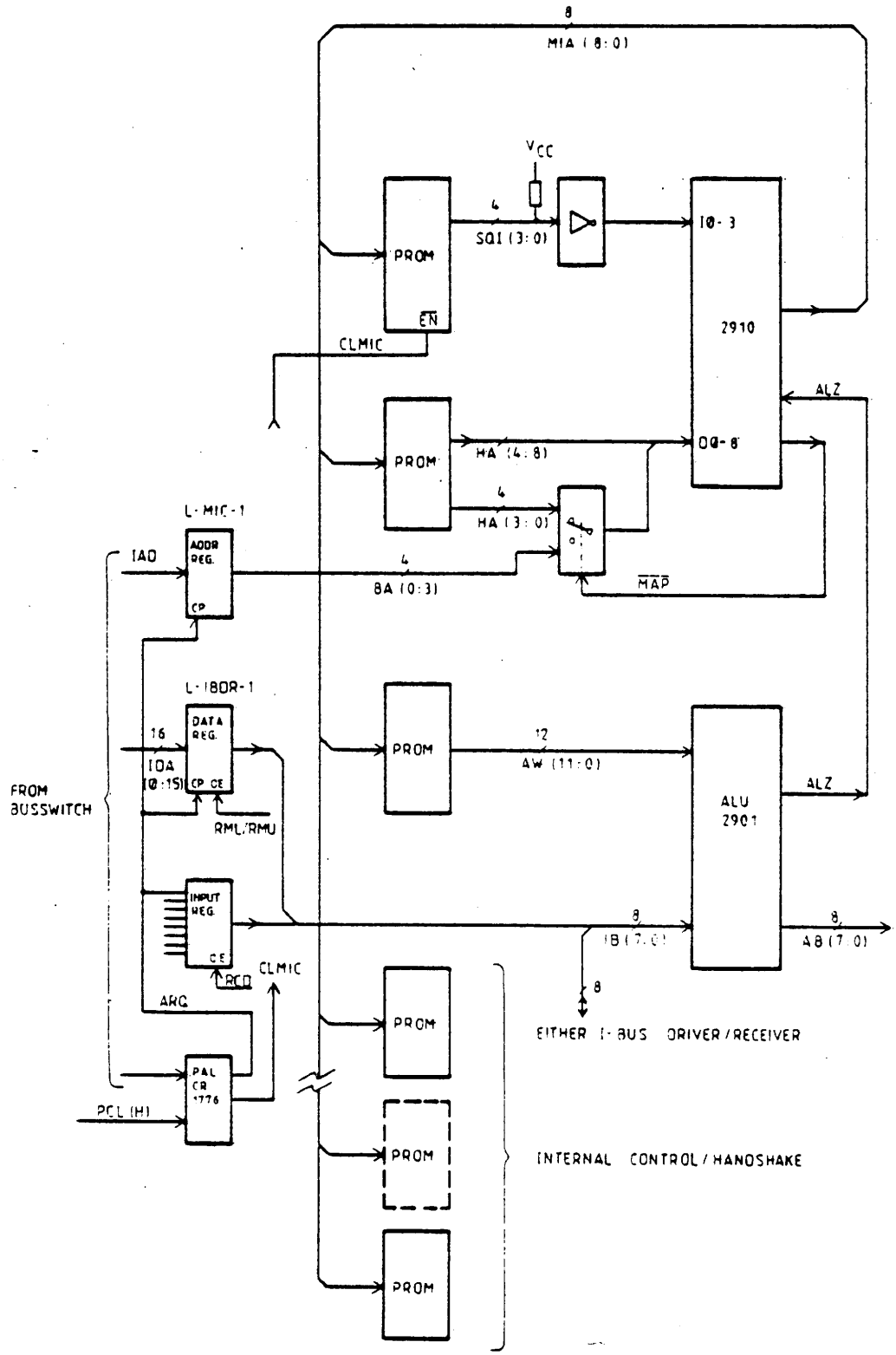
The controller part of the FD. ST. Ctrl. is built around the micro sequencer AM 2910 and the ALU AM2901 (fig. 3.2-1). The micro program is stored in 7 PROMS, which together can deliver a 512 x 56 bits wide micro word. The PROMS get their 9 bit address MIA 8:0 from the 2910. The different bits of the micro PROMS are divided into groups, and the signals AW11:0 are used for controlling the ALU. The ALU consists of 2 4-bit slices, which in parallel acts as an 8 bit ALU. Depending of the control word (AW11:0) the ALU can fetch data from either its internal registers or from the I-Bus (IB7:0). The result from the ALU is outputted on the AB-Bus (AB7-0). A single line ALZ (actually the zero flag) teels the sequencer, if the ALU-result was zero or not ("1"if true).

Some other PROM signals (data bits) are used to control the sequencer, and in this way the 2910 is able to address its own next operation code. And depending of the operation code and the state of the ALZ-signal the 2910 will decide whether to branch or not.

The branch address can be fetched from either the direct address input (Lines SH3:0 and HA8:4) or the 2910's internal registers. The four least significant branch addresses SH3:0 can be chosen between HA3:0 or BA3-0, under control of the sequencer by means of the MAP-signal. - When the micro controller detects a valid CR80M Main Bus access by polling the ARQ signal, it will read the address register (L-ALIR-1), via the selector (LS157), controlled by the MAP line.

And simply decode the system command issued from the CR80M, by means of a multi branching technique, where the 4 LSB's of the jump address is a direct copy of the combination of the SH3:0 lines.

To insure proper initialization of the micro controller a special clear signal, CLMIC is generated by the Main bus logic (PAL CR1776). When a clear condition occurs (see section 3.1.4) the CLMIC synchronously will disable the output of PROM which delivers the instruction to the 2910. Because of the pull-up resistors and the 4 inverters, this disable will force a "Jump to Zero" instruction (0H) to the inputs of the 2910, and in this way gets the micro controller to run its start-up program.



CHRISTIAN POULSEN A/S

Fig. 3.2-1

CR 8047 /010 AB/00
Micro Controller. L-MiC-1

Block Diagram

Scale		Approved	Issue 1
Date	81-09-24		Date 81-09-24
Drawn	BBP/MZL		Approved
Parts no		3-3043	
Print no		Sheet 1 of 1 sheets	

3.2.1 L-IBDR-1 Internal Main Bus Data Receiver

Data from the Internal Main Bus (Int.BUS) to the micro controller are latched on the rising edge of ARQ. The fetched data are transferred to the IBUS under micro control by the signals RML and RMU (Read Main bus Lower byte and Upper)

3.2.2 L-IBDD-1 Internal Main Bus Data Drivers

Data read by the CR80 are clocked to the int. bus, on the positive edge of REL and CPUP. These signals are delayed half a micro cycle compared with LML and LMU from the micro PROMS to ensure data set-up time on IBUS.

The tri-state control (DMD) of the data drives is performed by Main Bus logic (PAL CR1776)

3.2.3 L-MBL-1 Main Bus Logic

The Main Bus logic does perform necessary handshake between the internal Main Bus and the micro controller. Because the main logic is different for the two controller versions, 2 explanations of operation will follow.

3.2.3.1 Single Bus Version
Read Cycle

A read cycle starts when ITRQ goes high and R/W is low, and the device is ready (ACC(L) = 1 and ARQ = 0).

ACC(L) = 1 will synchronous enable the address comparator, and make the system able to recognize a valid CPU Access.

A positive recognize will synchronously set the ARQ line (which clocks the Main Bus receivers). Simultaneously the DMD, ACC(L) and RWI goes low and ARQ high. ARQ high will start internal micro controller action.

When the micro controller has completed its operation, it terminates by sending a SRL signal (SRL = gated LML)

The Main Bus logic interpret SRL as a completion signal for the Main Bus operation and issues the response signal. (See figure 3.2.3.1-1)

3.2.3.2 Write Cycle

This is performed in the same way as the read, except RWI goes high, and DMD remains high.

Due to the ability of the controller to latch data written by the CR80, it will send a response signal faster than in case of CPU reads. (See figure 3.2.3.1-1)

3.2.3.3 Dual Bus Version
CPU Access Cycle (RIO and WIO)

This section is only valid for dual version of the ST. FD. Ctrl.

A read cycle starts when IO(L) goes active (See Timing Diagram 2.3 in bus switch section) and IR/W is low, and the device is ready (ACC(L) = 1 and ARQ = 0)

A write cycle starts on the same conditions a read, but IR/W is high, and the device is ready.

The timing of the cycles is shown on figure 3.13.

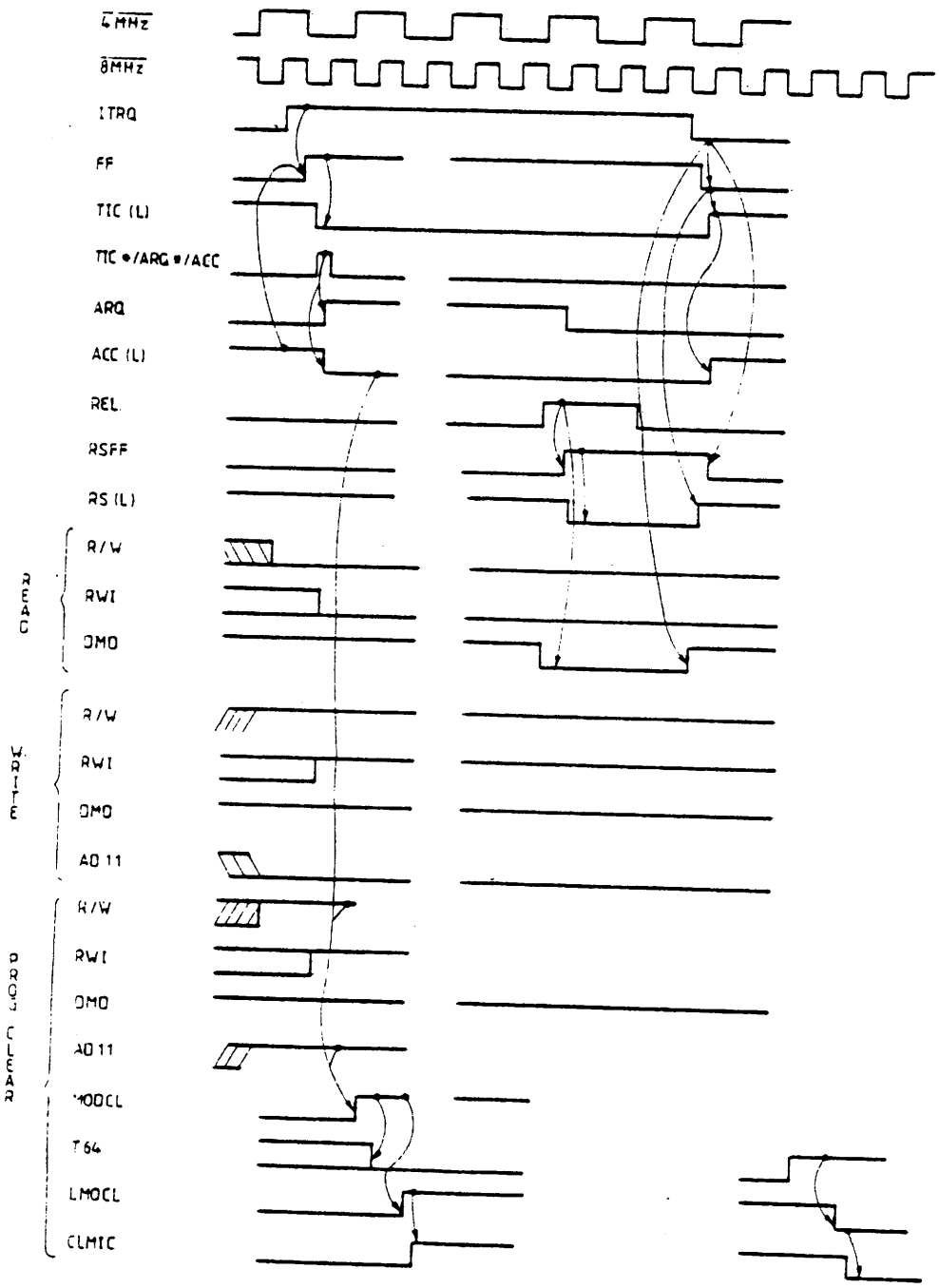


Figure 3.2.3.1-1

3.2.3.4 Clear Conditions

A CPU WIO-instruction with address bit 11 high will cause the Single bus STFD CTRL to be cleared. The clearing will force the mainbus logic to issue a RS immidiately after the reception of the command. The interrupt circuit will remain sending (if any previous request from the Micro Controller) until succesfully serviced. See timing figure 3.2.3.1-1 The internal voltage and clock detectors and the MC signal from the main, are also able to clear the module. This clearing treat interrupts sendings, in the same way as descriped formerly.
The dual bus version handles 2 different clear situations as explained in section 3.1.4.

3.2.3.5 L-TIM-1 TIMER

The timer delivers a signal T64 to the main bus logic 32 micro sec. after clear signal MODCL from the main bus logic. The T64 signal determines the length of the CLMIC signal when it clears the microprogram after a CPU-WI0 instruction with AD 11(PCL) high, see timing diagram 3.2.3.1-1. The TIMER signal from the timer will change a bit in the input register every 128 us and is used as timereferende for timedepending operations in microprogram execution.

3.2.3.6 L-RAM-1 Buffer RAM

The purpose of the RAM circuit is to establish a buffer storage between the CR80 and the floppy disc read/write mechanism. Figure 3.2.3.6-1 shows the timing diagram for RAM operation. The data patches for the different operations are shown in section 3.2.3.7.

When data is moved from RAM-buffer to the floppy disc formatter (FD1791), it is necessary to use a time multiplexing technique, since both data and RAM address is transferred on the AB-BUS.

The RAM circuit is prepared for future expansion of buffersize.

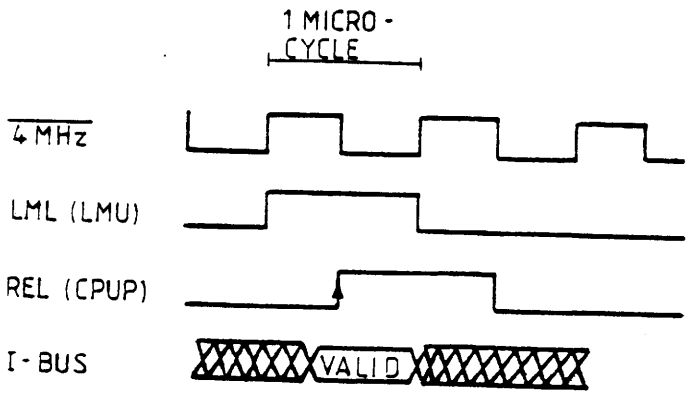


Figure 3.2.3.6-1

3.2.3.7 Data Patch at Different STFD CTRL Operations.

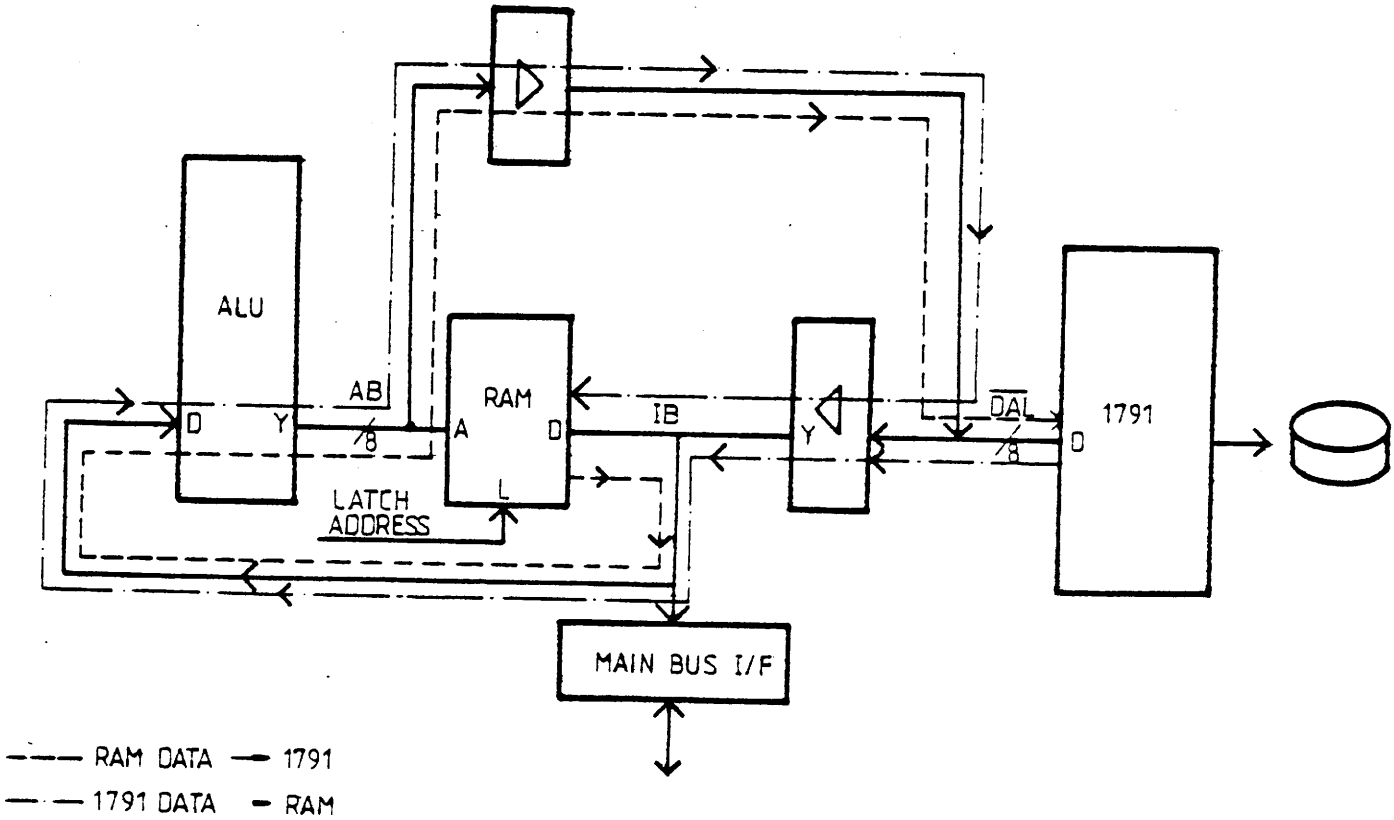


Figure 3.2.3.7-1

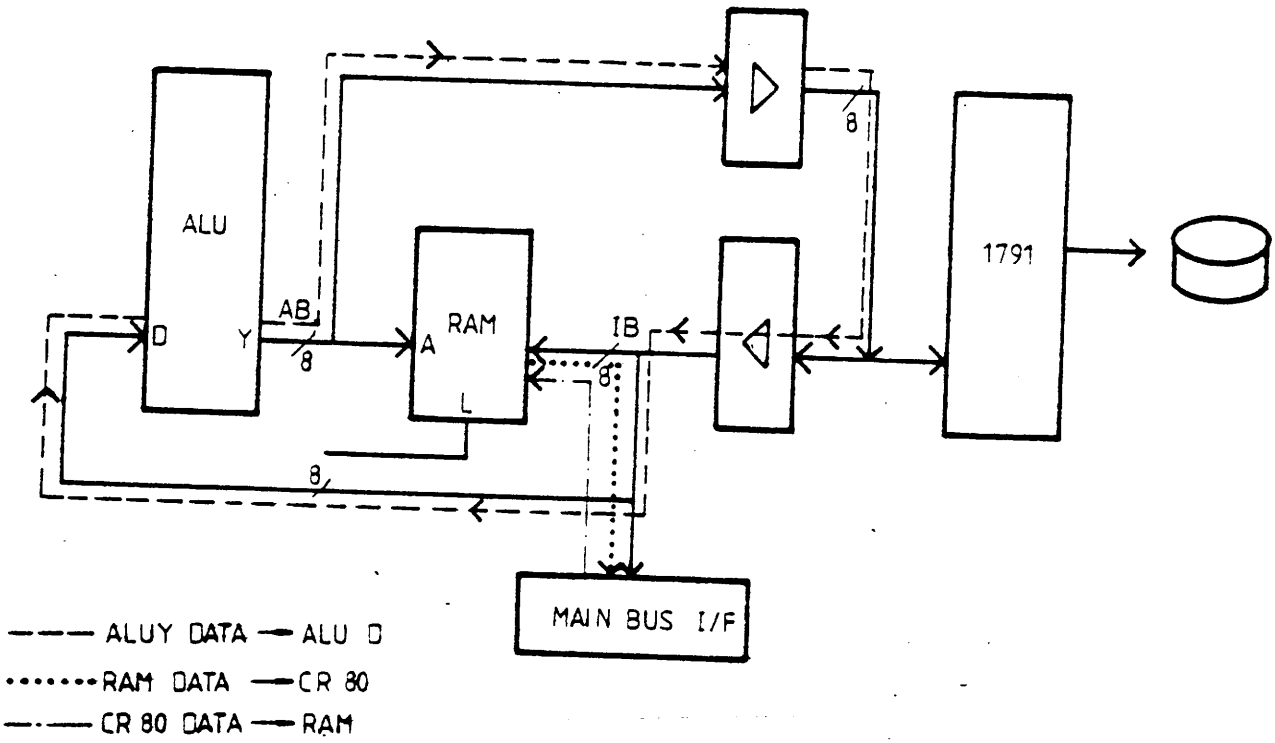


Figure 3.2.3.7-2

3.2.3.8 Interrupt sending logic dual bus version

The detail function of this circuit is given in accordance to the detailed block schematic fig. 2.3.8-1.
The Micro Controller is able to control the interrupt sending in two ways:

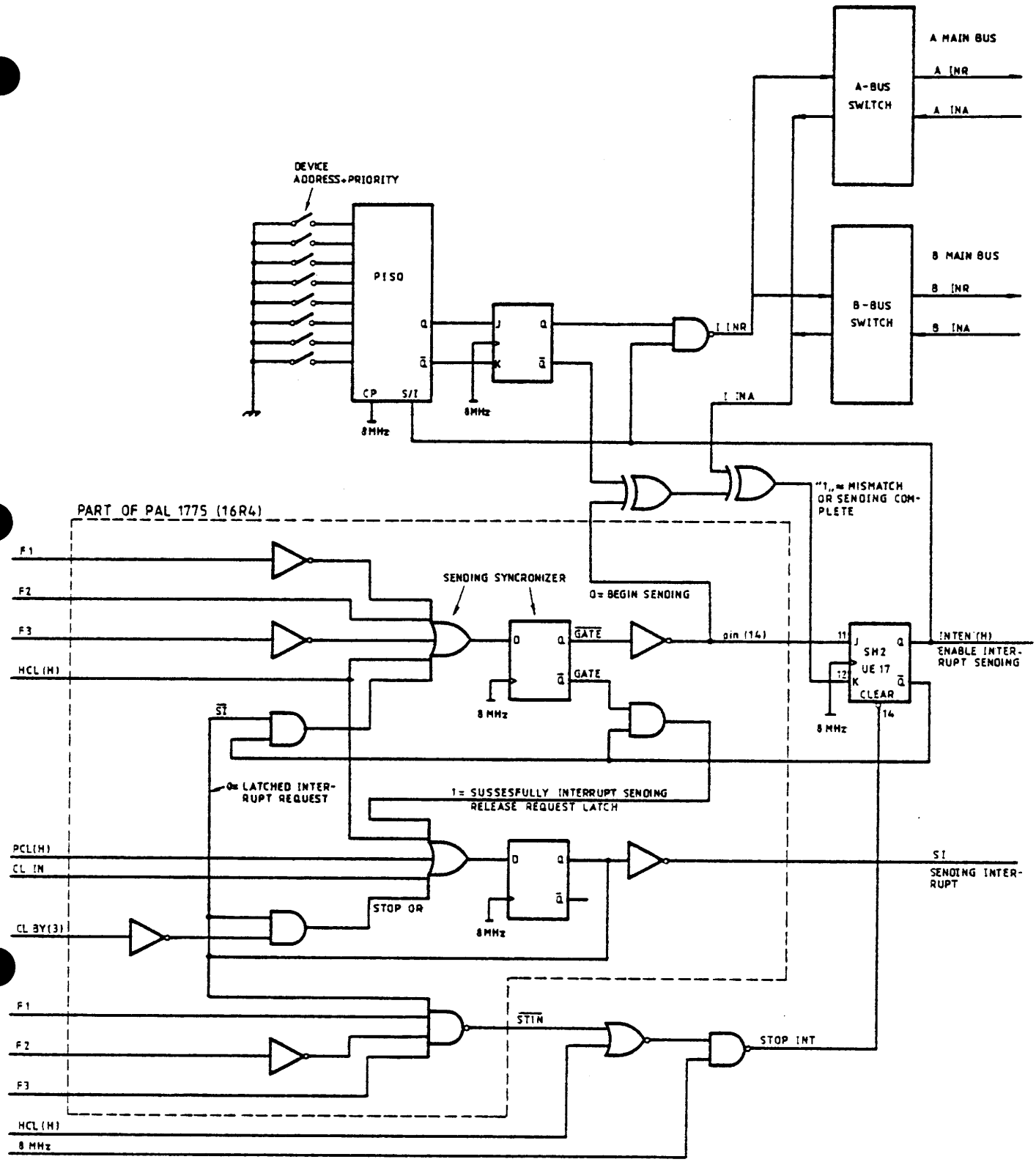
a) The CLBY signal is the interrupt requesting signal. The CLBY signal is an 250 nsec puls from the Micro Controller, and is latched by the interrupt logic, if no interrupt clear signals is present.

b) The CLIN *) is the interrupt clear signal. This signal will release the interrupt request latch. An already sending interrupt will continue the present 1 MHz cycle, but don't retry if mismatch.

The bolean expressions of the interrupt logic is shown in firmware description section.

Figure 3.2.3.8-2 shows the timing diagram.

*) This signal is shorted to PCL(H) signal in ST. FD. CTRL's equipped with issue 3 or newer firmware versions.



STIN = Time conditional disable of sending.
CLIN = Unconditional interrupt request clear. (by micro control).
PCL = ——— " ——— (by system software control). } Pending interrupts will be completed.
HCL = ——— " ——— (——— " ———). Immediately shut-down of interrupt sending.
CLBY = Interrupt requesting signal

Figure

3.2.3.8-1

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CR8047 /010AB/00
Interrupt logic detailed

Scale:		Approved:		Issue	1
Date:	81-09-24	E		Date:	81-09-24
Drawn:	BBP/MM			Approved	
Parts no:		3-3045			
Print no:		Sheet of sheets			

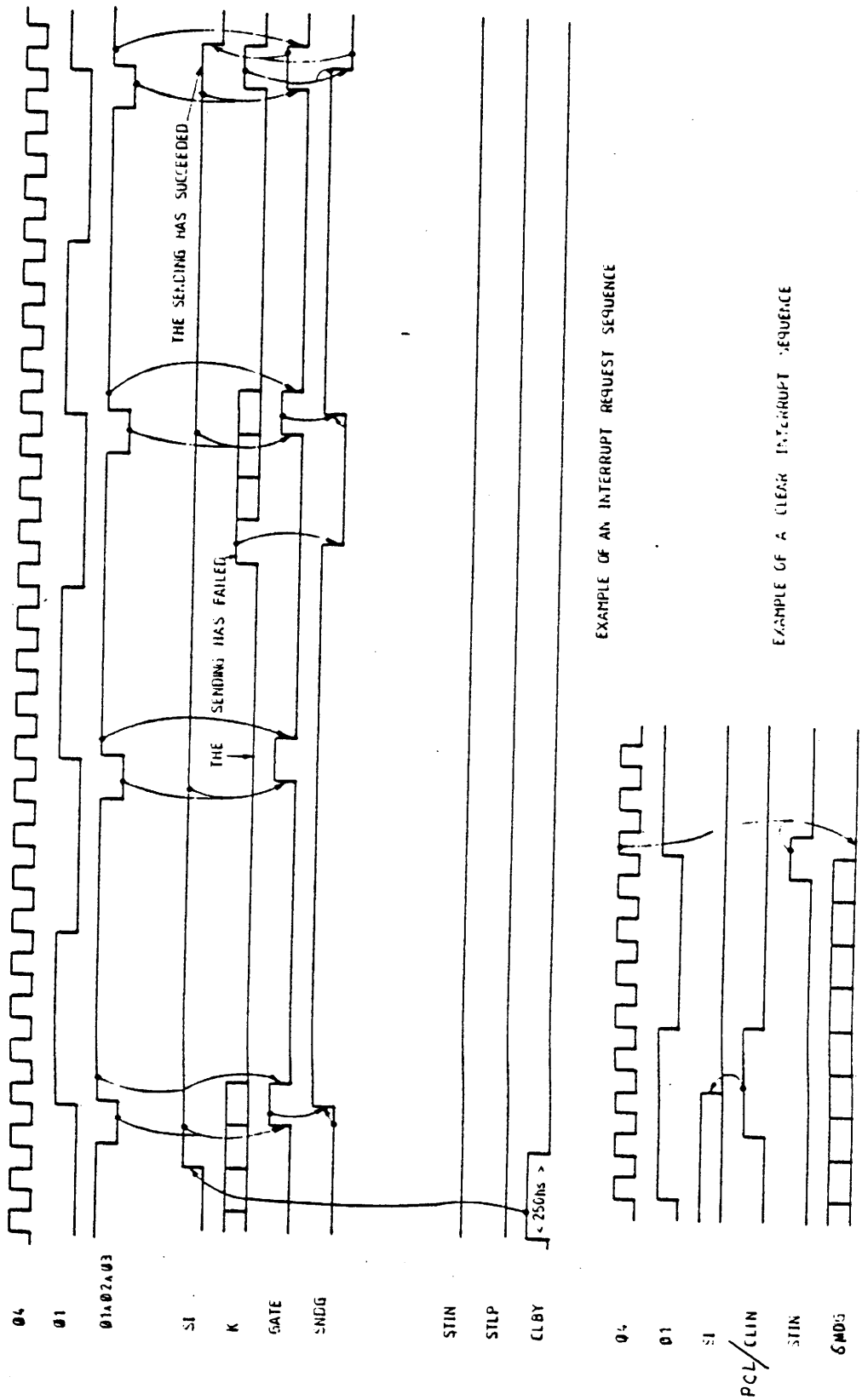
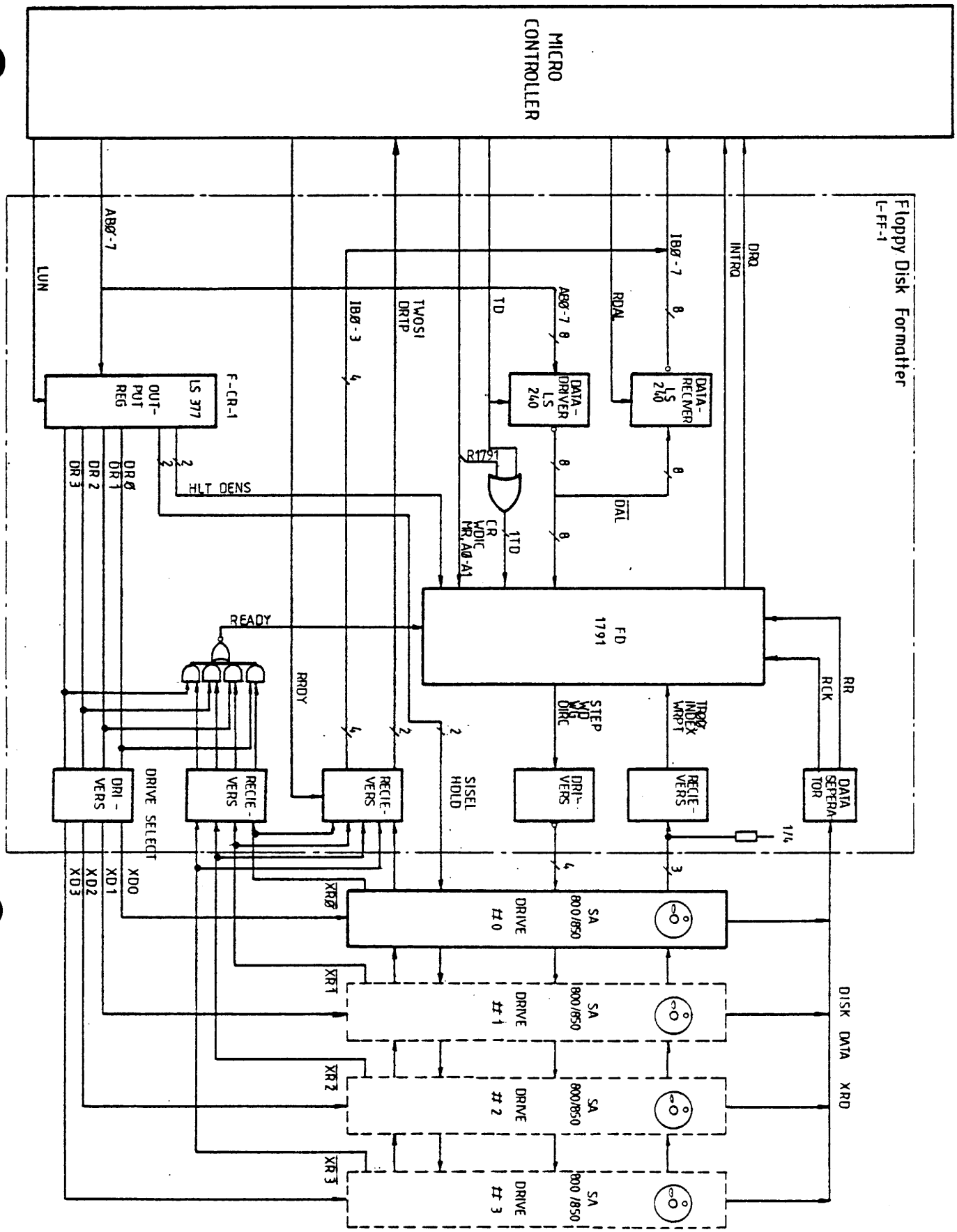


Figure 3.2.3.8-2

3.3 L-FF-1 : Floppy disc formatter.

The circuit is shown on sheet 4 of the blocked schematic.

The formatter function is build around the LSI-divice FD 1791, which perform all the control and handshake to a standard OEM-Floppy disc drive. Detailed information about FD 1791 is shown in appendix A. In the Floppy disc controller module, the FD 1791 works as, what you might call, a subcontroller, to the micro controller (L-MIC-1). The signals to and from the FD1791 can be divided into three groups. One group for control and data transfer between the Micro Controller and the formatter chip. The second group of signals are control and data lines between FD1791 and the Floppy drive(s). The third group are controllines between the micro-controller and the floppy drive(s). The second and third group are feed and received via drivers and receivers. See Figure 3.3-1 (Block diagram)



~~FIG. 4.7~~

CHRISTIAN ROVSING A/S

Fig. 3.3-1

ST FD CNTL CR 8047 /010AB/00

Floppy Disk Formatter

Block Diagram

Scale:	—	Approved	
Date:	81-09-23		
Drawn:	BBP / LLA		
Parts no:		3-3041	
Print no:		Sheet 1 of 1 sheets	

Issue	1
Date	81-09-23
Approved	BB/LL

3.3.1 Signal Description

The following description is an explanation of the function and purpose, of the different signals within the Floppy disc formatter part of the ST.FD. CTRL.

RD: Read data. Data input direct from drive. The signal is input to the dataseperator.

RR: Raw Read. Data input signal equal to RD from drive, but syncronized to the system clock. The signal is an output signal from the data seperator, and consist of pulses which have a negativ edge, for each recorded flux transition.

RCK: Read Clock. A nominal square-ware clock signal derived from the data streen. The phase is relativ to RR (see timing diagram fig. 3.3.2.1), and is important, but polarity is not.

TR00: Track 00. Signal derived from the selected drive, indicates that read/write head is in position, track zero.

Index: Index. Signal derived form the selected drive. A pulse indicates when the indexhole is encountered on the discette.

WRPT: Write protected: Signal derived form the selected drive. The signal terminated every write command to the drive, and inform the Micro Controller and formatter about the protecting.

SISEL: Side Select. Output signal from the Micro Controller, inform the selected drive, which side on the diskette the controller want to access.
Logical 0 is equal to side 0.
Logical 1 is equal to side 1.

HDLD: Head Load. Output signal from the Micro Controller The signal will force the read/write head against the media.

STEP: STEP. Output from the FD1791, each pulse will move the stepper motor in the drive one stroke.

DIRC: Direction. Output to the floppy drive, to control the direction of the movement of the read/write head.
Logical "1" will move head against track 76
Logical "0" will move head against track 00

WG: Write gate. Output signal to the floppy drive. The signal is made valid before writing on the discette is performed, enable writing logic in selected drive.

WD: Write Data. A composite clock and data pattern to the floppy drive. The controller sends write data stream fast enough to maintain synchronization with the rotational speed of the diskette.

XR

(0-3): Ready from diskette drives. The signals indicates that drive electronics are ready to read or write. The signals are received by the formatter and the Micro Controller.

READY: Ready. Input to the FD1791, inform the formatter about the state of XR-lines. The specific one XR-signal is selected by the corresponding DR-signal. The ready line is High if all DR-signals are zero.

DR

(0-3): Drive select. These signals are issued by the Micro Controller, which selects one of the drives a time. The DR also control the Ready-selector, so that only the corrending Ready signal is send to the formatter.

HLT: Head Load Timing. Input to the FD1791 from the Micro Controller.
The signal tells the formatter, that the HDLD-signal already is sent to floppy drive and the head load time is expired, and read/write head is stable against media. Head load time is determined by drive type. (difference in mechanical delay).

DENS: Density: Input to the formatter from the Micro Controller. The signal select single or double density operation of the diskette formatting. (MF or MFM).

Note: The signal is optional for future design. The date-seperator and firmware of the CR8047M/010XX/00 is not able to handle MFM operation and only single density formatting is performed. The DENS line is tied to "1"-level.

DAL (0-7): Data Bus: These signal-lines are a bidirectional databus between the Micro Controller and formatter chip. The bus signals are inverted data.

DRQ: Data Request: Signal from FD 1791 to Micro Controller. It indicates that the dataregister contains data to the Micro Controller when the FD1791 reads data from the diskette. In write mode DRQ indicates an empty dataregister. The DRQ-signal is reset when serviced by the Micro Controller.

INTRQ: Interrupt request: The signal is issued by th FD1791 to the Micro Controller. It is set at the complition of any command. INTRQ is reset when the Micro Controller reads the status register or loads the commands register in order to start a new task.

A0-A1: Address signals Input sipnal to the FD1791 from the Micro Controller, is used to seperate between the different internal registers in the FD1791.

WDIC: Write delayed to 1791. Signal from the Micro Controller to the FD1791. WDiC is used to enable writing to the formatter. The signal is delayed 125 nsec to ensure enough set-up time on the AØ-A1 lines before enabling the 1791's write logic. A write operation from the Micro Controller is performed with the data-driver (F-DD-1). The datadriver is enabled synchronious to the microclock. (4 MHz)

R1791: Read from 1791: Control signal to the formatter chip from the micro controller. Issued when the microcontroller wants to read data or status from the FD1791. To ensure proper Set-Up time of the address lines A0-A1 is the RE (READ ENABLE) line to the FD1791 delayed 125 nsec. The delayed controlsignals is named TD.

TD: Transfer Delayed: Signal used, when the Micro Controller wants to read from the FD1791 (see R1791). The signal do also control enable lines ($\overline{1G}$ and $\overline{2G}$) of the data driver (F-DD-1). This will prevent against collision between output drivers of the FD1791 and the datadriver.

MR: Master Reset: Input signal to the FD1791 from the Micro Controller. The signal resets the chip and load Hex 03 into the command register. Because of this loading the FD1791 will execute a restore operation when the MR goes high, regardless of the state of the READY input. Also Hex 01 is loaded into the sector register.

3.3.2 L-DSEP-1 Data Seperator

The job of this circuit is to decompose the read data (RD) from floppy drive(s), to 2 signals Raw Read (RR) and Read Clock (RCK). See sec. 3.3.1
Figure 3.3.2-1 shows the timing diagram.

Data Stream from disc.

Example with DATA = D2

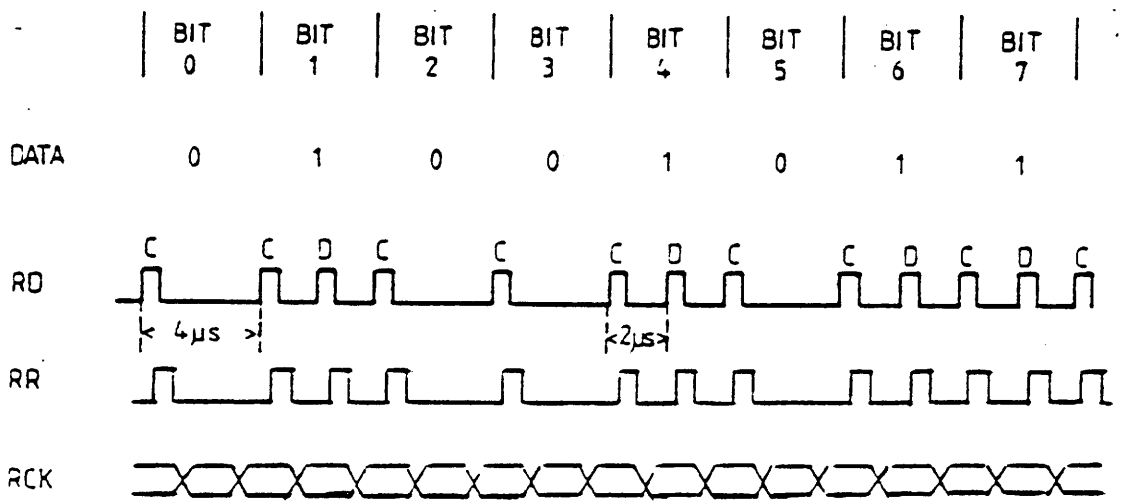


Figure 3.3.2-1

3.3.3 F-DR-1: Data Receiver
F-DR-1: Datadriver

Buffers which interface the FD 1791 and the Micro Controller. Further the buffers perform datatransfer from AB-BUS to IBUS under micro control. See section 3.2.3.7

3.3.4 F-CR-1: Command register

This register is an dedicated output port used by the Micro Controller to output different controlsignals to the drive(s), FD 1791 and DR-mux.

3.3.5 L-PAR-1 : Parity logic.

This paragraph is only valid for the dual bus STFD CRTL. The parity logic does perform parity bit generation of the dataword read by CR80 during RIO operation. The circuit does also perform parity check of received data, during CPU WIO operations. The output of the parity checker is feed to the IBUS, when the Micro Controller shakes the RRDY-line.

4. Signal specifications

The electrical specifications are provided for the 3 connectors on the module, fig 4.1-1, 4.1-2, 4.2-2, shows the pin lay-out.

General about mainbus signal

For use in redundant channel crates the CR8047M/010-AB/00 is equiped with dualized mainbus interface. The interface is functional and fysical identical, the only exception is the ground connection to the +12V bus-switch, which is only connected to Mainbus A (plug 1) terminal. B39. The terminal is shorter as the others, giving a automatic disable of the two mainbus infaces, to prevent against harzardeous busaccess, when the module fysical is removed or inserted in the crate, while the computer is running.

The main bus I/F of the single bus version CR8047M/010A-/00 is identical to Main Bus A I/F of the dual bus version, except pin B39 which is a normaly ground connection.

In the following section, only one mainbus I/F (BUS A) will be specified.

4.1 Main bus signal specification.

Power Consumption:

Dual bus version:	+ 5V	4,2A
	+12V	25 mA
Single bus version:	+ 5V	3,2A
	+12V	25 mA

Response time:	t_{rs} read	<	2,8 usec
	t_{rs} write	<	650,- nsec
*)	t_{rs} busswitch command	<	400,- nsec

*) only for dual bus version

Signal lines.

The levels for all the mainbus signals are normal TTL-logic levels ie:

High level: $2,0 < V_H < 5,0V$

$0V < V_L < 0,8V$

The following subsection will specify the Main Bus load caused by the modules input lines.

Signal sinking lines.

			I_{IL}	I_{IH}
(A) (B)	DA 0-15, UP, LP	:	-200 uA	80 uA
(A) (B)	AD 0-8,11,17,15	:	-200 uA	80 uA
(A) (B)	AD 9-10	:	- 40 uA	160 uA
(A) (B)	LSØ-1	:	-400 uA	40 uA
(A) (B)	R/W	:	-200 uA	20 uA
(A) (B)	TRQ	:	-800 uA	100 uA
(A) (B)	AE	:	-400 ua	50 uA
(A) (B)	INA	:	-400 uA	50 uA
(A) (B)	MC	:	-400 uA	80 uA
(A) (B)	Ø1 (1MHZ)	:	-400 uA	50 uA
(A) (B)	Ø1 (8MHz)	:	-1,2 uA	150 uA

Signal sourcing lines.

I_{OL} @ U_O = 0.4 V	(A) (B) DA 0-15, UP, LP:	-16 mA
I_{OH} @ U_O = 2.4 V	(A) (B) DA 0-15, UP, LP:	8 mA
I_O Tri-state	(A) (B) DA 0-15, UP, LP:	+/-200 uA

I_{OL} @ U_O = 0.4V	(A) (B) RS, INR:	- 40 mA
I_{IH}	during off (open collector output):	-250 uA

Main Bus Connector P1

A-BUS

Rear View

	B		A	
	gnd	43	gnd	
	gnd	42	gnd	
	A5V	41	A5V	
	A5V	40	A5V	
*)Delay ——>	gnd	39		
(delaygnd)	gnd	38	AØ2	
	gnd	37	AAE(L) *1)	
		36		
	gnd	35	AØ1	
	gnd	34	AR/W(L/H)	
	gnd	33	AINR(L)	
	gnd	32	AINA(H)	
	gnd	31	ATRQ(L)	
	gnd	30	ARS(L)	
	AMC(H)	29		
	ALP	28	AUP	
	gnd	27	gnd	
	ALS1	26	ALS0	
	17	25		
	15	24		
		23		
	11	22	10	
	9	21	8	
ADDRESS (ADD)	gnd	20	gnd	ADDRESS (AAD)
	7	19	6	
	5	18	4	
	3	17	2	
	1	16	0	
	gnd	15	gnd	
	+12VA	14	+12VA	
	gnd	13	gnd	
		12		
		11		
	gnd	10	gnd	
	15	9	14	
	13	8	12	
	11	7	10	
	9	6	8	
	7	5	6	
DATA(ADA)	5	4	4	DATA (ADA)
	3	3	2	
	1	2	0	
	gnd	1	gnd	

Figure 4.1-1 cont.

*) Normal ground connection on the single bus version

*1) Do not effect operation of single bus version

Main Bus Connector P2

B-BUS

(Only valid for the dual bus version)

Rear View

	B		A	
	gnd	43	gnd	
	gnd	42	gnd	
	B5V	41	B5V	
	B5V	40	B5V	
	gnd	39	gnd	
	gnd	38	BØ2	
	gnd	37	BAE(L)	
		36		
	gnd	35	BØ1	
	gnd	34	BR/W(L/H)	
	gnd	33	BINR(L)	
	gnd	32	BINA(H)	
	gnd	31	BTRQ(L)	
	gnd	30	BRS(L)	
	BMC(H)	29		
	BLP	28	BUP	
	gnd	27	gnd	
	BLS1	26	BLS0	
	17	25		
	15	24		
		23		
	11	22	10	
	9	21	8	
ADDRESS (BDD)	gnd	20	gnd	ADDRESS (BAD)
	7	19	6	
	5	18	4	
	3	17	2	
	1	16	0	
	gnd	15	gnd	
	+12VB	14	+12VB	
	gnd	13	gnd	
		12		
		11		
	gnd	10	gnd	
	15	9	14	
	13	8	12	
	11	7	10	
	9	6	8	
	7	5	6	
DATA (BDA)	5	4	4	DATA (BDA)
	3	3	2	
	1	2	0	
	gnd	1	gnd	

Figure 4.1-2

4.2 I/O Signal specification.

The signal lines are connected to perifical devices via P3. Further P3 is used for external disable of the 2 mainbuses, when the module is connected to the computer watchdog.

Generel about I/O signal.

An "X"-letter is used as prefix for the signal names, indicating a "Perifical signal": The input lines are pulled-up to Vcc-0,7V using 2K2 ohms resistors.
Out-put signals are driven by open collector drivers (Normally 5438 TTL-gate), without pull-up.

Input Signals:

	I_{IL} $U_{IL=0.4V}$	I_{IH} $U_{IH} = 2.7V$
XR0 - XR3:	-2.4 mA	- 680 uA
XTZ, XIN, XWP:	-2.2 mA	- 700 uA
XTS, XDT, XRD:	-2.2 mA	- 700 uA

Output Signals:

	I_{OL} $U_{OL} = 0.4V$	IO_{OFF}
XD0 - XD3	38 mA	250 uA
XWD, XSS, XHL	38 mA	250 uA
XWG, XDIR, XST	38 mA	250 uA

WATCHDOG SIGNALS

Only valid for the dual bus version.

EABD(L)

EAD (L)

This signal will while active prevent against access from the A-BUS.

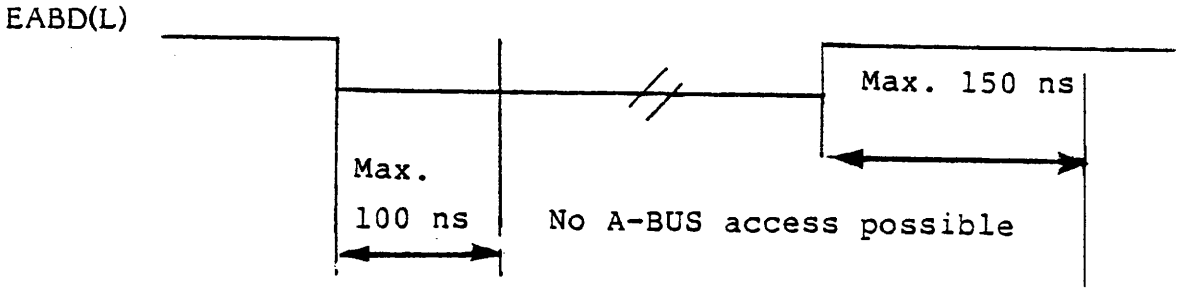


Figure 4.2-1

EBBD(L)

This signal has the same function on the B-BUS as EABD(L) has on the A-BUS.

A SEL (L)

This signal indicate when the A-BUS is enabled. During bus switch commands from the A-BUS, the signal can go low even if the A-BUS is not enabled (the response driver must shortly be enabled to insure Main Bus handshake).

B SEL (L)

This signal indicates when the B-BUS is enabled. During bus switch commands from the B-BUS the signal can go low even if the B-BUS is not enabled.

I/O-Connector P3

Rear View

B		A	
	43		
	42		
gnd	41	gnd	
	40	EABD(L)	
ASEL(L)	39	EBBD(L)	
BSEL(L)	38	gnd	*)
gnd	37	gnd	
	36		
	35		
	34		
	33		
	32		
	31		
	30		
	29		
	28		
	27		
	26		
	25		
XRD	24		
XWP	23		
XTZ	22		
XWG	21		
XWD	20		
XST	19		
XDIR	18		
XD3	17		
XD2	16		
XD1	15		
XD0	14	gnd	
	13		
XRO	12		
XIN	11		
XHL	10		
gnd	9		
XSS	8		
gnd	7		
XTS	6		
XR1	5		
XR2	4		
XR3	3		
XDT	2		
	1		

*) Not valid for the single bus version

Figure 4.2-2

5. INSTALLATION

This section describes the strap and switch setting of the ST. FD. Ctrl.

The SR identification numbers mentioned are valid for the dual bus version Hardware. Section 6.1 shows a cross reference list to the single bus version.

5.1 Module Device Address:

8 switches in position S1 select the modules, I/O Address and interrupt priority

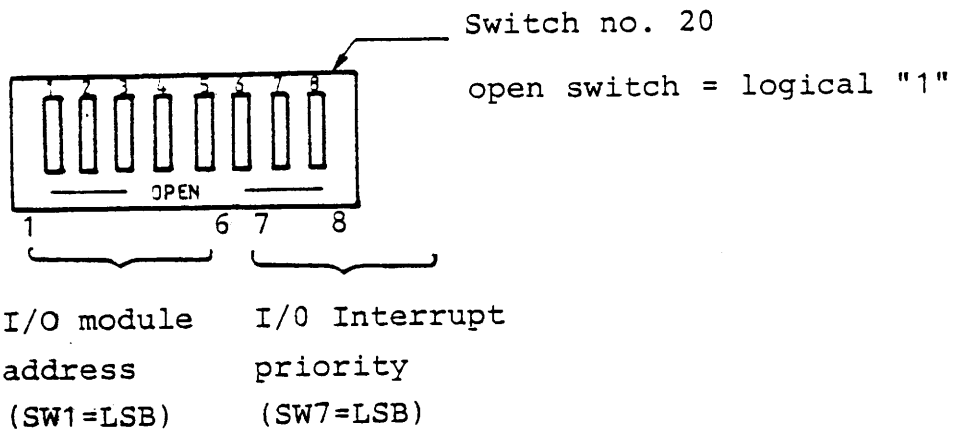


Figure 5.1-1

5.2 Straps

SR1 located near UD7, might be used to introduce a permanent disable of A-Main Bus interface. The strap will in pos. A make it impossible for the module to recognize its own module address, and because of that never issue a response to the address sourcing device.

SR1 in pos. A	Disable A-BUS response
SR1 in pos. B	Enable A-BUS compare

SR2 located near UD213, same function as SR1, but related to B-Main Bus.

SR2 in pos. A	Disable B-BUS response
SR2 in pos. B	Enable B-BUS compare

SR3 located near UD31.
The strap might be used to make them Micro Controller to accept different formats of system command (issued from CR80M system software), as command for same function. Commands definition in document ref. 1. See fig. 6.1.

SR3 in pos. A	Select AD7
SR3 in pos. b	Select AD17

SR4 located near UD31.

Same function as SR3, but select between AD6 and AD15, see fig. 6.1

SR4 in pos. A	select AD6
SR4 in pos. B	select AD15

SR5 located near UD31

Same function as SR3, but select between AD8 and R/W, see fig. 6.1

SR5 in pos. A	select AD9
SR5 in pos. B	select R/W

SR6 located near UD31

Same function as SR3, but select between AD9 and Logical "0". See fig. 6.1

SR6 in pos. A	select AD9
SR6 in pos. B	select "0"

SR10 located near Q2 and Q3

The strap might be used to enable hard master clear, controlled from Main Bus pin B29.

SR10 in pos. A	Hard MC from Main Bus
SR10 in pos. C	Hard MC disabled
SR10 in pos. B	Hard MC disabled from Main Bus, but external hard clear might be issued from test equipment during hardware test to the B terminal of SR10

SR11 located near UD30

The strap is set in different position in accordance to promsize

SR11 in pos. A for. 27S35 (1024X8 bit)
SR11 in pos. B for. 27S25 (512X8 bit)

SR13-SR14 located near UD33

The two straps are used to extend size and number of RAM Buffer. Normally when used, as sector buffer for. 128 bytes (IBM 3740) the straps must be in pos. B.

SR 13	SR 14	Buffer Size	
B	B	128 bytes	Buffer 1
B	A	256 bytes	
A	B	128 bytes	Buffer 2
A	A	256 bytes	

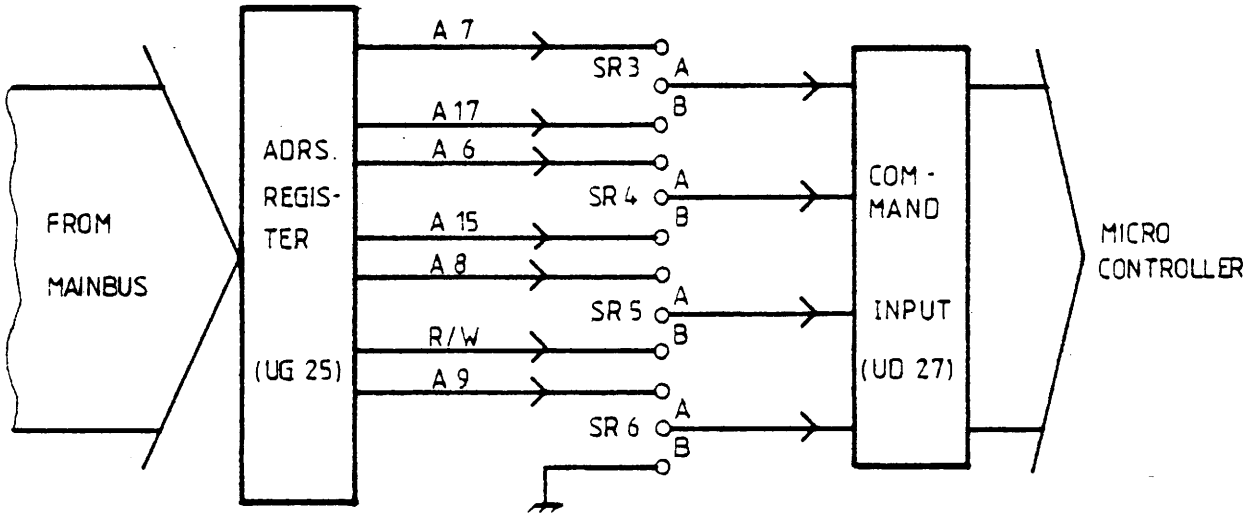


Figure 5.2-1
Command Format Strap Area

SR7 located near UC41
SR8 located near UD43 — For drive type
SR9 located near UD43 — programming
SR12 located near UA45

The 4 straps just mentioned are used for set-up in accordance with the type of floppy drive (normal 8" or mini 5 1/4").

Drive	Normal 7"		Mini 5 1/4"	
SR NO.	A	B	A	B
7		X	X	
8		X	X	
9		X	X	
12		X	X	

NOTE: The micro program must also be changed, when changing drive type.

5.1 Strap Number Cross Reference

Single Bus Version Straps Identification		Dual Bus Version Straps Indification
SR1	equal to	SR4
SR2	equal to	SR3
SR3	equal to	SR5
SR4	equal to	SR6
SR5	equal to	SR14
SR6	equal to	SR13
SR7	equal to	SR9
SR8	equal to	NO
SR9	equal to	NO
SR10	equal to	SR8
SR11	equal to	NO
SR12	equal to	SR7
SR13	equal to	SR12

NO means no equivalent strap.

SR8 in pos. B disables WD to drive

SR4 in pos. B removes gating between WD from FD1791 and WRPT

SR11 in pos. B in applications with 8 inc. drives

SR11 in pos. A in applications with 5 1/4 inc.drives.

APPENDIX A

FD 179X-02 Floppy Disk Formatter/Controller
Application Notes (24 pages)

WESTERN DIGITAL
CORPORATION

FD 179X-02 Floppy Disk Formatter/Controller Family

MAY 1980

FEATURES

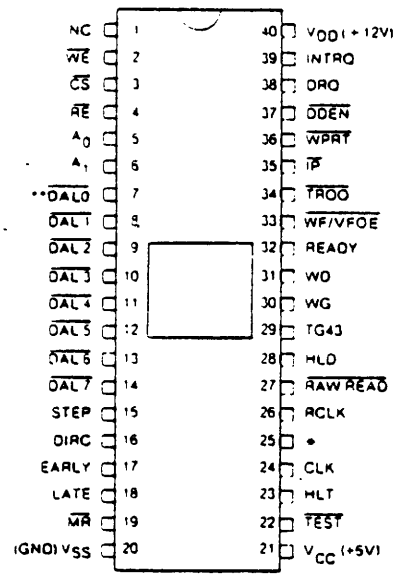
- TWO VFO CONTROL SIGNALS
- SOFT SECTOR FORMAT COMPATIBILITY
- AUTOMATIC TRACK SEEK WITH VERIFICATION
- ACCOMMODATES SINGLE AND DOUBLE DENSITY FORMATS
  - IBM 3740 Single Density (FM)
  - IBM System 34 Double Density (MFM)
- READ MODE
  - Single/Multiple Sector Read with Automatic Search or Entire Track Read
  - Selectable 128 Byte or Variable length Sector
- WRITE MODE
  - Single/Multiple Sector Write with Automatic Sector Search
  - Entire Track Write for Diskette Formatting
- SYSTEM COMPATIBILITY
  - Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and Status
  - DMA or Programmed Data Transfers
  - All Inputs and Outputs are TTL Compatible
  - On-Chip Track and Sector Registers/Comprehensive Status Information
- PROGRAMMABLE CONTROLS
  - Selectable Track to Track Stepping Time
  - Side Select Compare
- WRITE PRECOMPENSATION
- WINDOW EXTENSION
- INCORPORATES ENCODING/DECODING AND ADDRESS MARK CIRCUITRY
- FD1792/4 IS SINGLE DENSITY ONLY
- FD1795/7 HAS A SIDE SELECT OUTPUT

179X-02 FAMILY CHARACTERISTICS

FEATURES	1791	1793	1795	1797
Single Density (FM)	X	X	X	X
Double Density (MFM)	X	X	X	X
True Data Bus		X		X
Inverted Data Bus	X		X	
Write Precomp	X	X	X	X
Side Selection Output			X	X

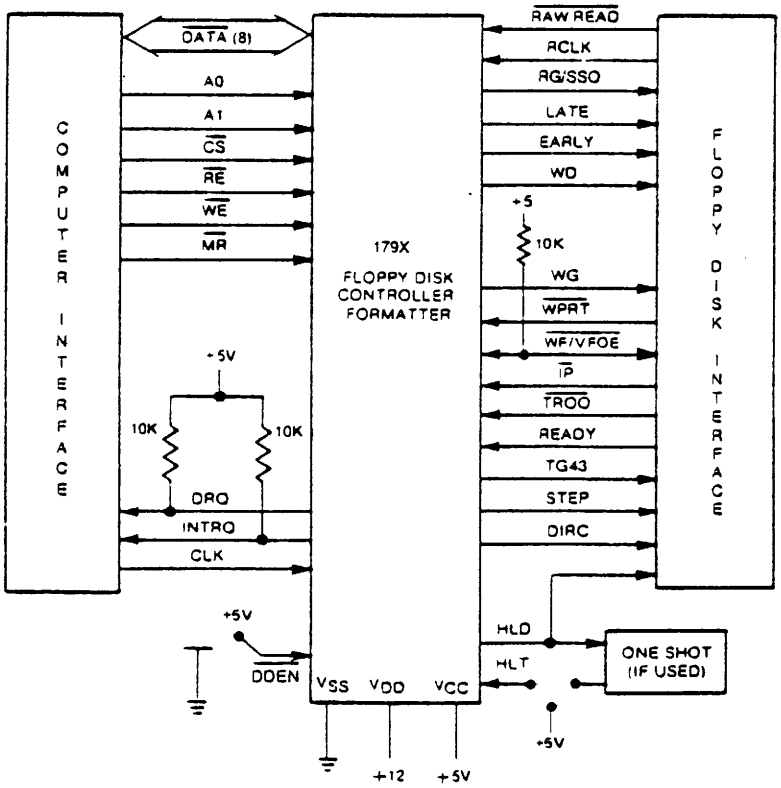
APPLICATIONS

FLOPPY DISK DRIVE INTERFACE
SINGLE OR MULTIPLE DRIVE CONTROLLER/ FORMATTER
NEW MINI-FLOPPY CONTROLLER



*1791/3 = RG 1795/7 = SSO
**1793/7 TRUE BUS

PIN CONNECTIONS



FD179X SYSTEM BLOCK DIAGRAM

GENERAL DESCRIPTION

The FD179X are MOS LSI devices which perform the functions of a Floppy Disk Formatter/Controller in a single chip implementation. The FD179X, which can be considered the end result of both the FD1771 and FD1781 designs, is IBM 3740 compatible in single density mode (FM) and System 34 compatible in Double Density Mode (MFM). The FD179X contains all the features of its predecessor the FD1771, plus the added features necessary to read/write and format a double density diskette. These include address mark detection, FM and MFM encode and decode logic, window extension, and write precompensation. In order to maintain compatibility, the FD1771, FD1781, and FD179X designs were made as close as possible with the computer interface, instruction set, and I/O registers being identical. Also, head load control is identical. In each case, the actual pin assignments vary by only a few pins from any one to another.

The processor interface consists of an 8-bit bidirectional bus for data, status, and control word transfers. The FD179X is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD179X is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs. The 1793 is identical to the 1791 except the DAL lines are TRUE for systems that utilize true data busses.

The 1795/7 has a side select output for controlling double sided drives, and the 1792 and 1794 are "Single Density Only" versions of the 1791 and 1793. On these devices, DDEN must be left open.

PIN OUTS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	NO CONNECTION	NC	Pin 1 is internally connected to a back bias generator and must be left open by the user.
19	$\overline{\text{MASTER RESET}}$	$\overline{MR}$	A logic low on this input resets the device and loads HEX 03 into the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a RESTORE Command is executed, regardless of the state of the Ready signal from the drive. Also, HEX 01 is loaded into sector register.
20	POWER SUPPLIES	V_{SS}	Ground
21		V_{CC}	+5V ±5%
40		V_{DD}	+12V ±5%
COMPUTER INTERFACE:			
2	$\overline{\text{WRITE ENABLE}}$	$\overline{WE}$	A logic low on this input gates data on the DAL into the selected register when $\overline{CS}$ is low.
3	$\overline{\text{CHIP SELECT}}$	$\overline{CS}$	A logic low on this input selects the chip and enables computer communication with the device.
4	$\overline{\text{READ ENABLE}}$	$\overline{RE}$	A logic low on this input controls the placement of data from a selected register on the DAL when $\overline{CS}$ is low.
5,6	REGISTER SELECT LINES	A0, A1	These inputs select the register to receive/transfer data on the DAL lines under $\overline{RE}$ and $\overline{WE}$ control: A1 A0 $\overline{RE}$ $\overline{WE}$ 0 0 Status Reg Command Reg 0 1 Track Reg Track Reg 1 0 Sector Reg Sector Reg 1 1 Data Reg Data Reg
7-14	$\overline{\text{DATA ACCESS LINES}}$	$\overline{DAL0}$-$\overline{DAL7}$	Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is receiver enabled by $\overline{WE}$ or transmitter enabled by $\overline{RE}$.
24	CLOCK	CLK	This input requires a free-running square wave clock for internal timing reference, 2 MHz for 8" drives, 1 MHz for mini-drives.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
38	DATA REQUEST	DRQ	This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operations, respectively. Use 10K pull-up resistor to +5.
39	INTERRUPT REQUEST	INTRQ	This open drain output is set at the completion of any command and is reset when the STATUS register is read or the command register is written to. Use 10K pull-up resistor to +5.
FLOPPY DISK INTERFACE:			
15	STEP	STEP	The step output contains a pulse for each step.
16	DIRECTION	DIRC	Direction Output is active high when stepping in, active low when stepping out.
17	EARLY	EARLY	Indicates that the WRITE DATA pulse occurring while Early is active (high) should be shifted early for write precompensation.
18	LATE	LATE	Indicates that the write data pulse occurring while Late is active (high) should be shifted late for write precompensation.
22	$\overline{\text{TEST}}$	$\overline{\text{TEST}}$	This input is used for testing purposes only and should be tied to +5V or left open by the user unless interfacing to voice coil actuated motors.
23	HEAD LOAD TIMING	HLT	When a logic high is found on the HLT input the head is assumed to be engaged.
25	READ GATE (1791/3)	RG	A high level on this output indicates to the data separator circuitry that a field of zeros (or ones) has been encountered, and is used for synchronization.
25	SIDE SELECT OUTPUT (1795, 1797)	SSO	The logic level of the Side Select Output is directly controlled by the 'S' flag in Type II or III commands. When S = 1, SSO is set to a logic 1. When S = 0, SSO is set to a logic 0. The Side Select Output is only updated at the beginning of a Type II or III command. It is forced to a logic 0 upon a MASTER RESET condition.
26	READ CLOCK	RCLK	A nominal square-wave clock signal derived from the data stream must be provided to this input. Phasing (i.e. RCLK transitions) relative to RAW READ is important but polarity (RCLK high or low) is not.
27	$\overline{\text{RAW READ}}$	$\overline{\text{RAW READ}}$	The data input signal directly from the drive. This input shall be a negative pulse for each recorded flux transition.
28	HEAD LOAD	HLD	The HLD output controls the loading of the Read-Write head against the media.
29	TRACK GREATER THAN 43	TG43	This output informs the drive that the Read/Write head is positioned between tracks 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	This output is made valid before writing is to be performed on the diskette.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
31	WRITE DATA	WD	A 250 ns (MFM) or 500 ns (FM) pulse per flux transition. WD contains the unique Address marks as well as data and clock in both FM and MFM formats.
32	READY	READY	This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. Type I operations are performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.
33	$\overline{\text{WRITE FAULT}}$ / VFO ENABLE	$\overline{\text{WF}}$/$\overline{\text{VFOE}}$	This is a bi-directional signal used to signify writing faults at the drive, and to enable the external PLO data separator. When WG = 1, Pin 33 functions as a WF input. If WF = 0, any write command will immediately be terminated. When WG = 0, Pin 33 functions as a VFOE output. VFOE will go low during a read operation after the head has loaded and settled (HLT = 1). On the 1795/7, it will remain low until the last bit of the second CRC byte in the ID field. VFOE will then go high until 8 bytes (MFM) or 4 bytes (FM) before the Address Mark. It will then go active until the last bit of the second CRC byte of the Data Field. On the 1791/3, VFOE will remain low until the end of the Data Field.
34	$\overline{\text{TRACK 00}}$	$\overline{\text{TR00}}$	This input informs the FD179X that the Read/Write head is positioned over Track 00.
35	$\overline{\text{INDEX PULSE}}$	$\overline{\text{IP}}$	This input informs the FD179X when the index hole is encountered on the diskette.
36	$\overline{\text{WRITE PROTECT}}$	$\overline{\text{WPRT}}$	This input is sampled whenever a Write Command is received. A logic low terminates the command and sets the Write Protect Status bit.
37	$\overline{\text{DOUBLE DENSITY}}$	$\overline{\text{DDEN}}$	This pin selects either single or double density operation. When $\overline{\text{DDEN}}$ = 0, double density is selected. When $\overline{\text{DDEN}}$ = 1, single density is selected. This line must be left open on the 1792/4

ORGANIZATION

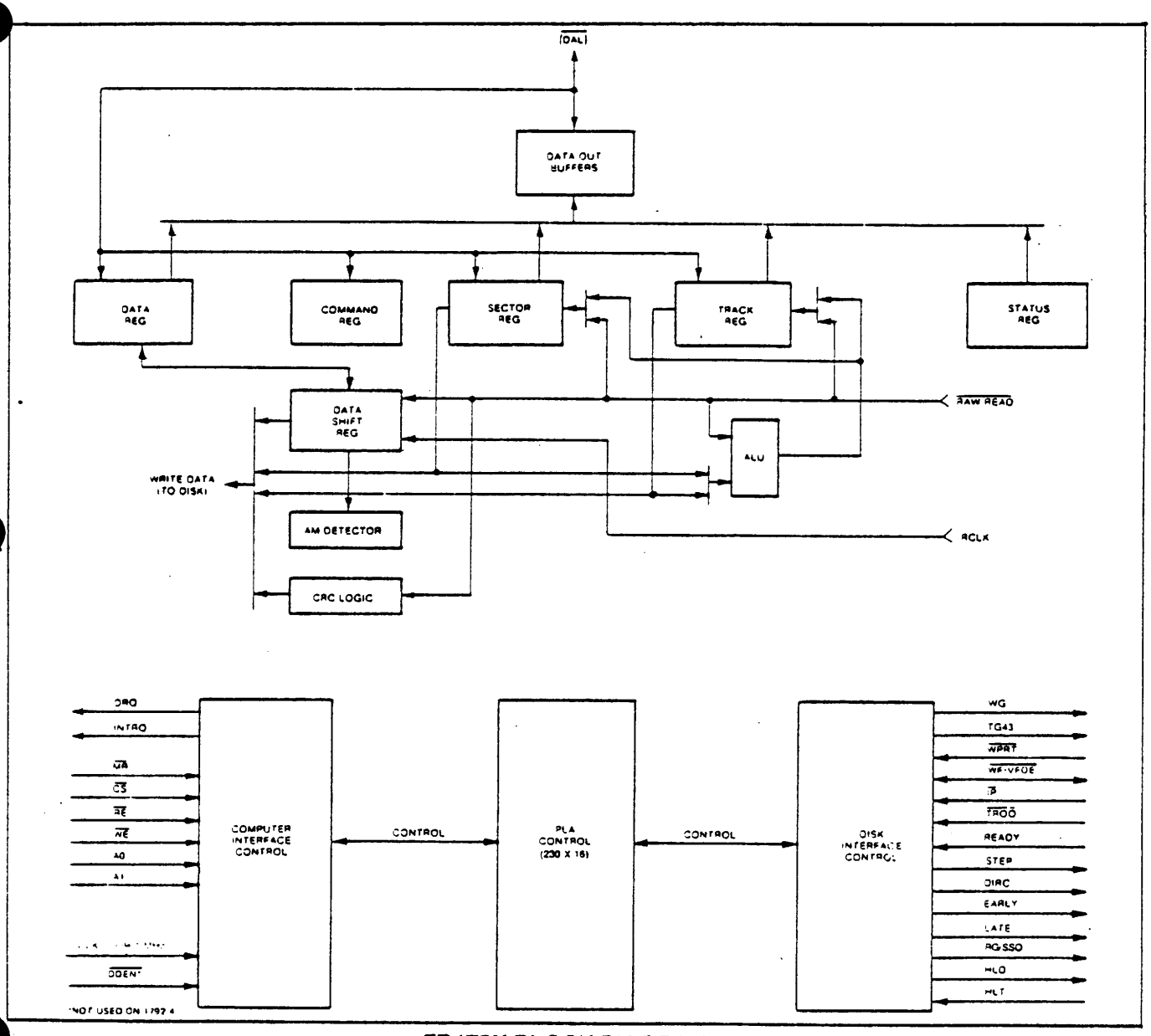
The Floppy Disk Formatter block diagram is illustrated on page 5. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register—This 8-bit register assembles serial data from the Read Data input ($\overline{\text{RAW READ}}$) during Read operations and transfers serial data to the Write Data output during Write operations.

Data Register—This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register is loaded from the DAL and gated onto the DAL under processor control.

Track Register—This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when the device is busy.



FD179X BLOCK DIAGRAM

Sector Register (SR)—This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR)—This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the new command is a force interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR)—This 8-bit register holds device Status information. The meaning of the Status bits is a function of the type of command previously executed. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic—This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is: $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU)—The ALU is a serial comparator, incrementer, and decrementer and is used for register modification and comparisons with the disk recorded ID field.

Timing and Control—All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from an external crystal clock.

The FD1791/3 has two different modes of operation according to the state of $\overline{DDEN}$. When $\overline{DDEN} = 0$ double density (MFM) is assumed. When $\overline{DDEN} = 1$, single density (FM) is assumed.

AM Detector—The address mark detector detects ID, data and index address marks during read and write operations.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines ($\overline{DAL}$) and associated control signals. The $\overline{DAL}$ are used to transfer Data, Status, and Control words out of, or into the FD179X. The $\overline{DAL}$ are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable ($\overline{RE}$) are active (low logic state) or act as input receivers when $\overline{CS}$ and Write Enable ($\overline{WE}$) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and $\overline{CS}$ is made low. The address bits A1 and A0, combined with the signals $\overline{RE}$ during a Read operation or $\overline{WE}$ during a Write operation are interpreted as selecting the following registers:

A1-A0	READ ($\overline{RE}$)	WRITE ($\overline{WE}$)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD179X and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

At the completion of every command an INTRQ is generated. INTRQ is reset by either reading the status register or by loading the command register with a new command. In addition, INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The 179X has two modes of operation according to the state of $\overline{DDEN}$ (Pin 37). When $\overline{DDEN}$ = 1, single density is selected. In either case, the CLK input (Pin 24) is at 2 MHz. However, when interfacing with the mini-floppy, the CLK input is set at 1 MHz for both single density and double density. When the clock is at 2 MHz, the stepping rates of 3, 6, 10, and 15 ms are obtainable. When CLK equals 1 MHz these times are doubled.

HEAD POSITIONING

Five commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the r field in bits 1 and 0 of the command word. After the last directional step an additional 15 milliseconds of head settling time takes place if the Verify flag is set in Type I commands. Note that this time doubles to 30 ms for a 1 MHz clock. If $\overline{TEST}$ = 0, there is zero settling time. There is also a 15 ms head settling time if the E flag is set in any Type II or III command.

The rates (shown in Table 1) can be applied to a Step-Direction Motor through the device interface.

Step—A 2 μs (MFM) or 4 μs (FM) pulse is provided as an output to the drive. For every step pulse issued, the drive moves one track location in a direction determined by the direction output.

Direction (DIRC)—The Direction signal is active high when stepping in and low when stepping out. The Direction signal is valid 12 μs before the first stepping pulse is generated.

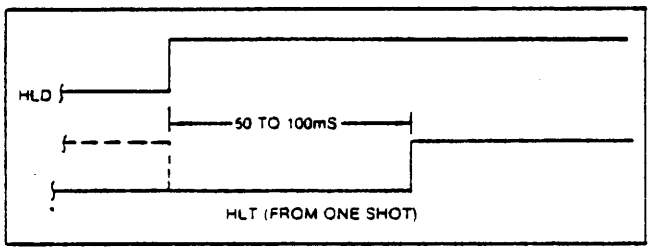
When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 (V = 1) in the command word to a logic 1. The verification operation begins at the end of the 15 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track Register. If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete and an INTRQ is generated with no errors. The FD179X must find an ID field with correct track number and correct CRC within 5 revolutions of the media; otherwise the seek error is set and an INTRQ is generated.

Table 1. STEPPING RATES

CLK	2 MHz	2 MHz	1 MHz	1 MHz	2 MHz	1 MHz
$\overline{DDEN}$	0	1	0	1	x	x
R1 R0	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=1	$\overline{TEST}$=0	$\overline{TEST}$=0
0 0	3 ms	3 ms	6 ms	6 ms	184μs	368μs
0 1	6 ms	6 ms	12 ms	12 ms	190μs	380μs
1 0	10 ms	10 ms	20 ms	20 ms	198μs	396μs
1 1	15 ms	15 ms	30 ms	30 ms	208μs	416μs

The Head Load (HLD) output controls the movement of the read/write head against the media. HLD is activated at the beginning of a Type I command if the h flag is set (h = 1), at the end of the Type I command if the verify flag (V = 1), or upon receipt of any Type II or III command. Once HLD is active it remains active until either a Type I command is received with (h = 0 and V = 0); or if the FD179X is in an idle state (non-busy) and 15 index pulses have occurred.

Head Load Timing (HLT) is an input to the FD179X which is used for the head engage time. When HLT = 1, the FD179X assumes the head is completely engaged. The head engage time is typically 30 to 100 ms depending on drive. The low to high transition on HLD is typically used to fire a one shot. The output of the one shot is then used for HLT and supplied as an input to the FD179X.



HEAD LOAD TIMING

When both HLD and HLT are true, the FD179X will then read from or write to the media. The "and" of HLD and HLT appears as a status bit in Type I status.

In summary for the Type I commands: if h = 0 and V = 0, HLD is reset. If h = 1 and V = 0, HLD is set at the beginning of the command and HLT is not sampled nor is there an internal 15 ms delay. If h = 0 and V = 1, HLD is set near the end of the command, an internal 15 ms occurs, and the FD179X waits for HLT to be true. If h = 1 and V = 1, HLD is set at the beginning of the command. Near the end of the command, after all the steps have been issued, an internal 15 ms delay occurs and the FD179X then waits for HLT to occur.

For Type II and III commands with E flag off, HLD is made active and HLT is sampled until true. With E flag on, HLD is made active, an internal 15 ms delay occurs and then HLT is sampled until true.

DISK READ OPERATIONS

Sector lengths of 128, 256, 512 or 1024 are obtainable in either FM or MFM formats. For FM, $\overline{DDEN}$ should be placed to logical "1." For MFM formats, $\overline{DDEN}$ should be placed to a logical "0." Sector lengths are determined at format time by a special byte in the "ID" field. If this Sector length byte in the ID field is zero, then the sector length is 128 bytes. If 01 then 256 bytes. If 02, then 512 bytes. If 03, then the sector length is 1024 bytes. The number of sectors per track as far as the FD179X is concerned can be from 1 to 255 sectors. The number of tracks as far as the FD179X is concerned is from 0 to 255 tracks. For IBM 3740 compatibility, sector lengths are 128 bytes with 26 sectors per track. For System 34 compatibility (MFM), sector lengths are 256 bytes/sector with 26 sectors/track; or lengths of 1024 bytes/sector with 8 sectors/track. (See Sector Length Table.)

For read operations, the FD179X requires $\overline{RAW\ READ}$ Data (Pin 27) signal which is a 250 ns pulse for flux transition and a Read clock (RCLK) signal to indicate flux transition spacings. The RCLK (Pin 26) signal is provided by some drives but if not it may be derived externally by Phase lock loops, one shots, or counter techniques. In addition, a Read Gate Signal is provided as an output (Pin 25) which can be used to inform phase lock loops when to acquire synchronization. When reading from the media in FM. RG is made true when 2 bytes of zeroes are detected. The FD179X must find an address mark within the next 10 bytes; otherwise RG is reset and the search for 2 bytes of zeroes begins all over again. If an address mark is found within 10 bytes, RG remains true as long as the FD179X is deriving any useful information from the data stream. Similarly for MFM, RG is made active when 4 bytes of "00" or "FF" are detected. The FD179X must find an address mark within the next 16 bytes, otherwise RG is reset and search resumes.

During read operations (WG = 0), the $\overline{VFOE}$ (Pin 33) is provided for phase lock loop synchronization. $\overline{VFOE}$ will go active when:

a) Both HLT and HLD are True
b) Settling Time, if programmed, has expired
c) The 179X is inspecting data off the disk

If $\overline{WF}/\overline{VFOE}$ is not used, leave open or tie to a 10K resistor to +5.

DISK WRITE OPERATION

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD179X before the Write Gate signal can be activated.

Writing is inhibited when the $\overline{Write\ Protect}$ input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD179X terminates the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive..

For write operations, the FD179X provides Write Gate (Pin 30) and Write Data (Pin 31) outputs. Write data consists of a series of 500 ns pulses in FM ($\overline{DDEN}$ = 1) and 250 ns pulses in MFM ($\overline{DDEN}$ = 0). Write Data provides the unique address marks in both formats.

Also during write, two additional signals are provided for write precompensation. These are EARLY (Pin 17) and LATE (Pin 18). EARLY is active true when the WD pulse appearing on (Pin 30) is to be written early. LATE is active true when the WD pulse is to be written LATE. If both EARLY and LATE are low when the WD pulse is present, the WD pulse is to be written at nominal. Since write precompensation values vary from disk manufacturer to disk manufacturer, the actual value is determined by several one shots or delay lines which are located external to the FD179X. The write precompensation signals EARLY and LATE are valid for the duration of WD in both FM and MFM formats.

- Whenever a Read or Write command (Type II or III) is received the FD179X samples the Ready input. If this input is logic low the command is not executed and an interrupt is generated. All Type I commands are performed regardless of the state of the Ready input. Also, whenever a Type II or III command is received, the TG43 signal output is updated.

COMMAND DESCRIPTION

The FD179X will accept eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in Table 2.

Table 2. COMMAND SUMMARY

		BITS							
TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r_1	r_0
I	Seek	0	0	0	1	h	V	r_1	r_0
I	Step	0	0	1	u	h	V	r_1	r_0
I	Step In	0	1	0	u	h	V	r_1	r_0
I	Step Out	0	1	1	u	h	V	r_1	r_0
II	Read Sector	1	0	0	m	F_2	E	F_1	0
II	Write Sector	1	0	1	m	F_2	E	F_1	a_0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrrupt	1	1	0	1	I_3	I_2	I_1	I_0

Note: Bits shown in TRUE form.

Table 3. FLAG SUMMARY

TYPE I COMMANDS

h = Head Load Flag (Bit 3)

h = 1, Load head at beginning
h = 0, Unload head at beginning

V = Verify flag (Bit 2)

V = 1, Verify on destination track
V = 0, No verify

r_1r_0 = Stepping motor rate (Bits 1-0)

Refer to Table 1 for rate summary

u = Update flag (Bit 4)

u = 1, Update Track register
u = 0, No update

Table 4. FLAG SUMMARY

TYPE II & III COMMANDS

m = Multiple Record flag (Bit 4)

m = 0, Single Record
m = 1, Multiple Records

a_0 = Data Address Mark (Bit 0)

a_0 = 0, FB (Data Mark)
a_0 = 1, F8 (Deleted Data Mark)

E = 15 ms Delay (2MHz)

E = 1, 15 ms delay
E = 0, no 15 ms delay

(F_2) S = Side Select Flag (1791/3 only)

S = 0, Compare for Side 0
S = 1, Compare for Side 1

(F_1) C = Side Compare Flag (1791/3 only)

C = 0, disable side select compare
C = 1, enable side select compare

(F_1) S = Side Select Flag

(Bit 1, 1795/7 only)

S = 0 Update SSO to 0
S = 1 Update SSO to 1

(F_2) b = Sector Length Flag

(Bit 3, 1975/7 only)

	Sector Length Field			
	00	01	10	11
b = 0	256	512	1024	128
b = 1	128	256	512	1024

Table 5. FLAG SUMMARY

TYPE IV COMMAND

Ii = Interrupt Condition flags (Bits 3-0)

I0 = 1, Not-Ready to Ready Transition
I1 = 1, Ready to Not-Ready Transition
I2 = 1, Index Pulse
I3 = 1, Immediate Interrupt
I_3 -I_0 = 0, Terminate with no Interrupt

TYPE I COMMANDS

The Type I Commands include the Restore, Seek, Step, Step-In, and Step-Out commands. Each of the Type I Commands contains a rate field (r_0r_1), which determines the stepping motor rate as defined in Table 1.

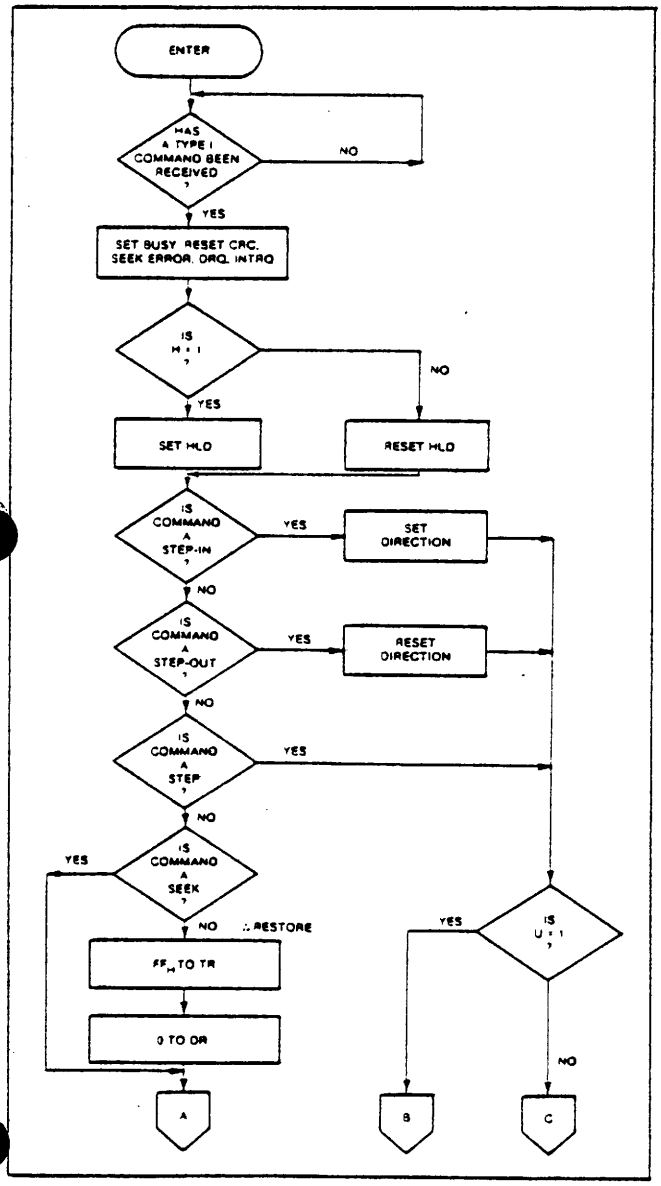
The Type I Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h = 1, the head is loaded at the beginning of the command (HLD output is made active). If h = 0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD179X receives a command that specifically disengages the head. If the FD179X is idle (busy = 0) for 15 revolutions of the disk, the head will be automatically disengaged (HLD made inactive).

The Type I Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V = 1, a verification is performed, if V = 0, no verification is performed.

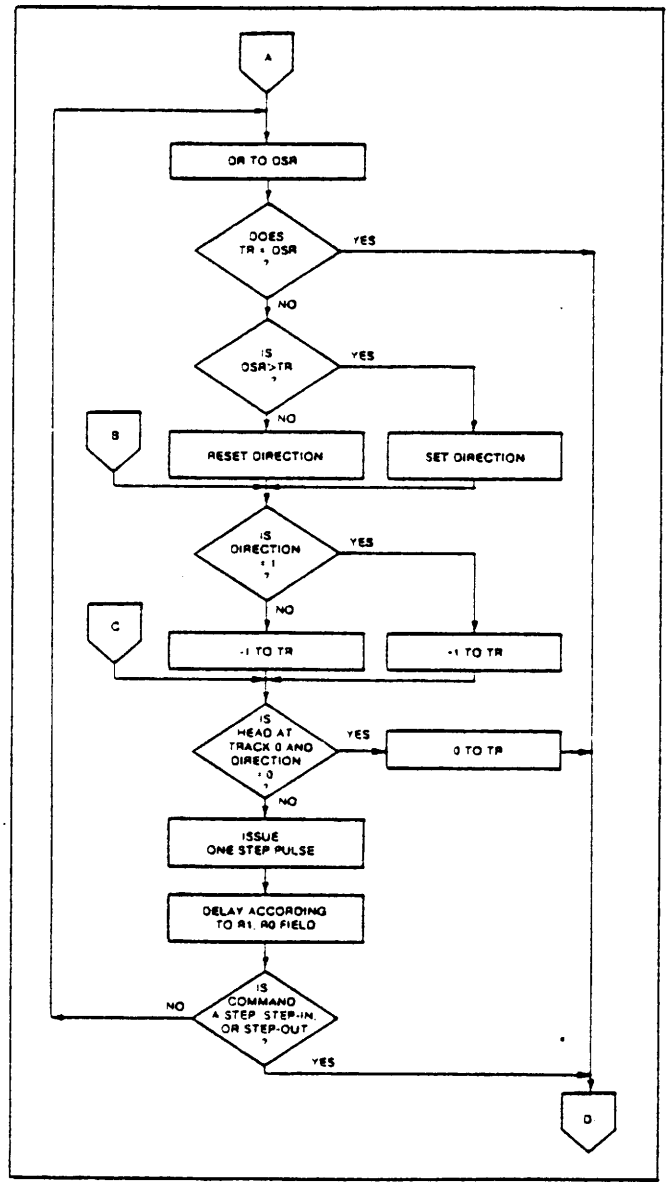
During verification, the head is loaded and after an internal 15 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the Busy status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, and Seek Error Status bit (Status bit 4) is set and the Busy status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after four revolutions of the disk, the FD179X terminates the operation and sends an interrupt, (INTRQ).

The Step, Step-In, and Step-Out commands contain an Update flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

On the 1795/7 devices, the SSO output is not affected during Type 1 commands, and an internal side compare does not take place when the (V) Verify Flag is on.



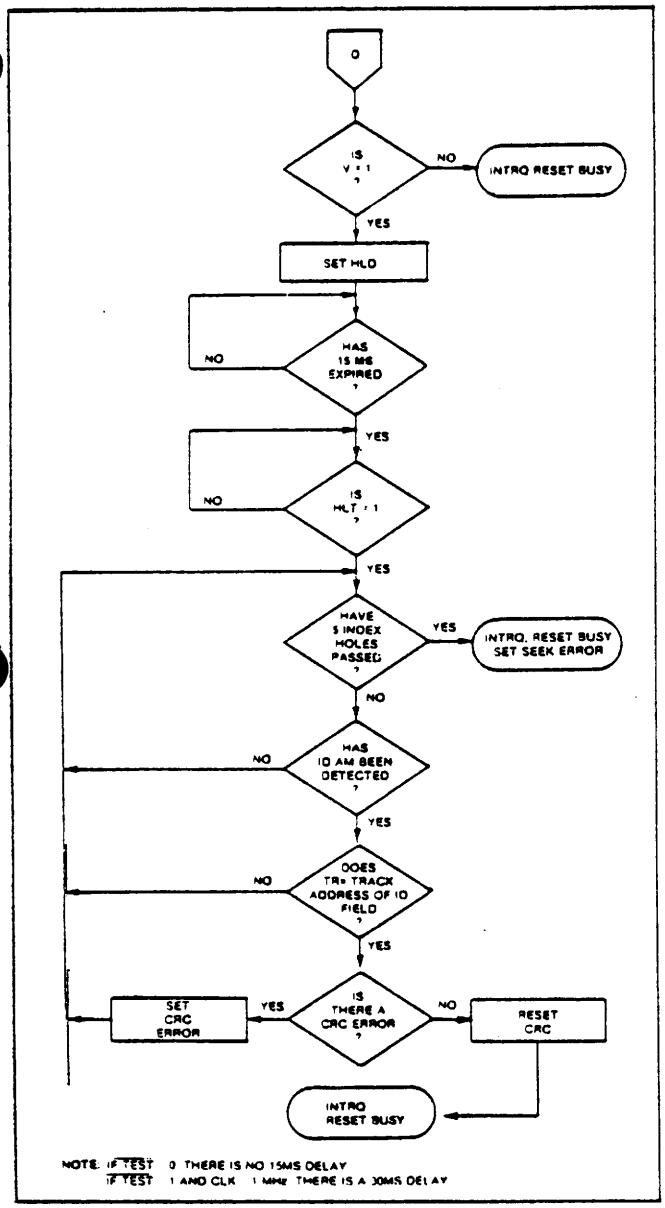
TYPE I COMMAND FLOW



TYPE I COMMAND FLOW

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{TR00}$) input is sampled. If $\overline{TR00}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{TR00}$ is not active low, stepping pulses (pins 15 to 16) at a rate specified by the r_1r_0 field are issued until the $\overline{TR00}$ input is activated. At this time the Track Register is loaded with zeroes and an interrupt is generated. If the $\overline{TR00}$ input does not go active low after 255 stepping pulses, the FD179X terminates operation, interrupts, and sets the Seek error status bit. A verification operation takes place if the V flag is set. The h bit allows the head to be loaded at the start of command. Note that the Restore command is executed when $\overline{MR}$ goes from an active to an inactive state.



TYPE I COMMAND FLOW

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD179X will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD179X issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-IN

Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

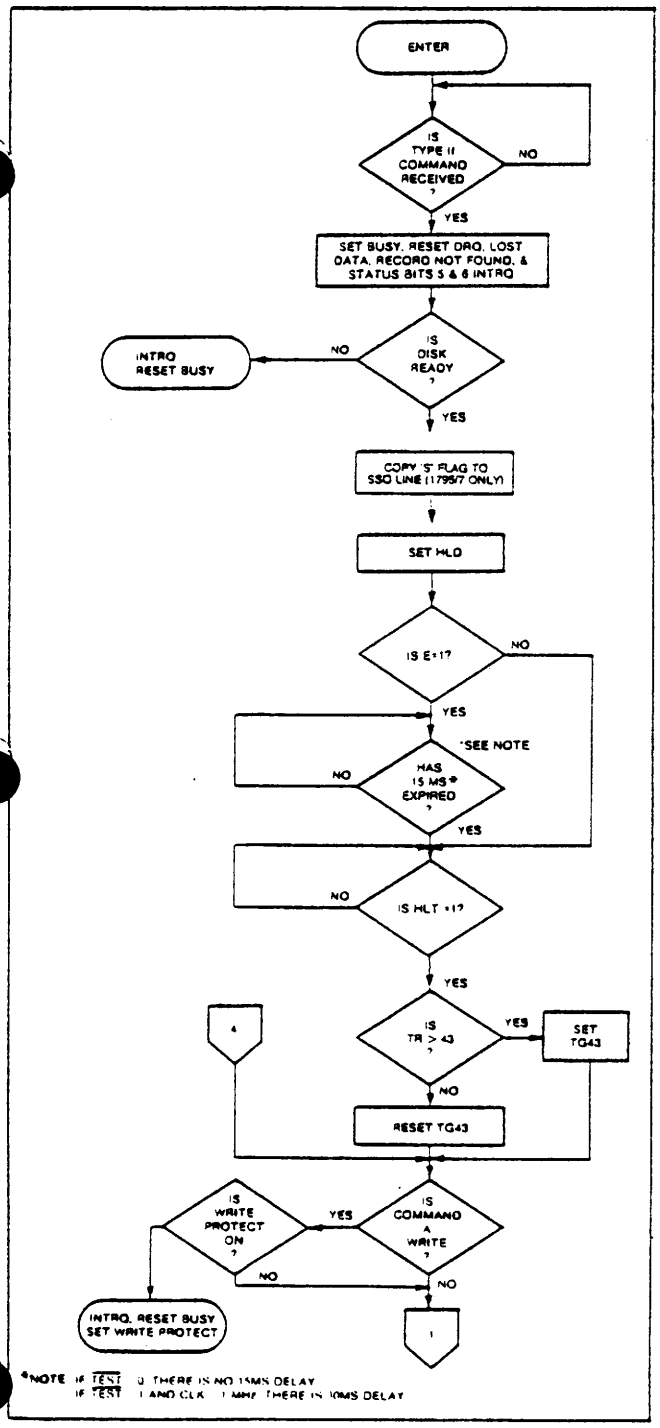
Upon receipt of this command, the FD179X issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands are the Read Sector and Write Sector commands. Prior to loading the Type II Command into the Command Register, the computer must load the Sector Register with the desired sector number. Upon receipt of the Type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 15 msec delay. If the E flag is 0, the head is loaded and HLT sampled with no 15 msec delay. The ID field and Data Field format are shown on page 13.

When an ID field is located on the disk, the FD179X compares the Track Number on the ID field with the Track Register. If there is not a match, the next en-

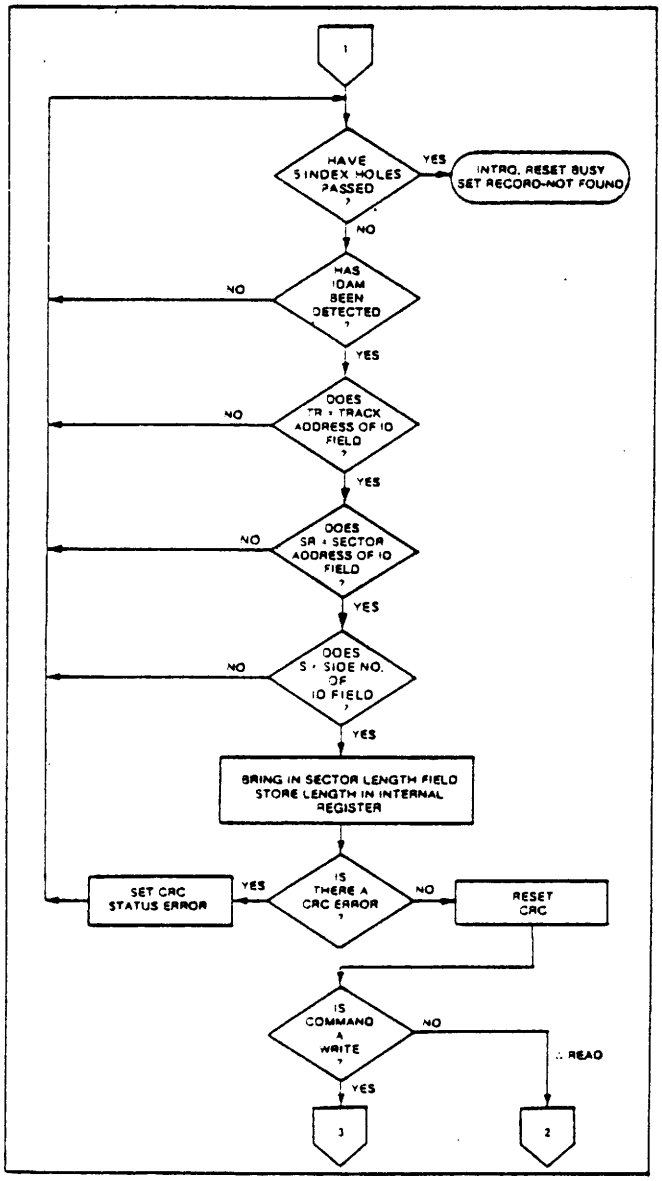
countered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD179X must find an ID field with a Track number, Sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.



TYPE II COMMAND

Sector Length Table	
Sector Length Field (hex)	Number of Bytes in Sector (decimal)
00	128
01	256
02	512
03	1024

Each of the Type II Commands contains an (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and an interrupt is generated at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD179X will continue to read or write multiple records and update the sector register until the sector regis-



TYPE II COMMAND

ter exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the Command Register, which terminates the command and generates an interrupt.

If the Sector Register exceeds the number of sectors on the track, the Record-Not-Found status bit will be set.

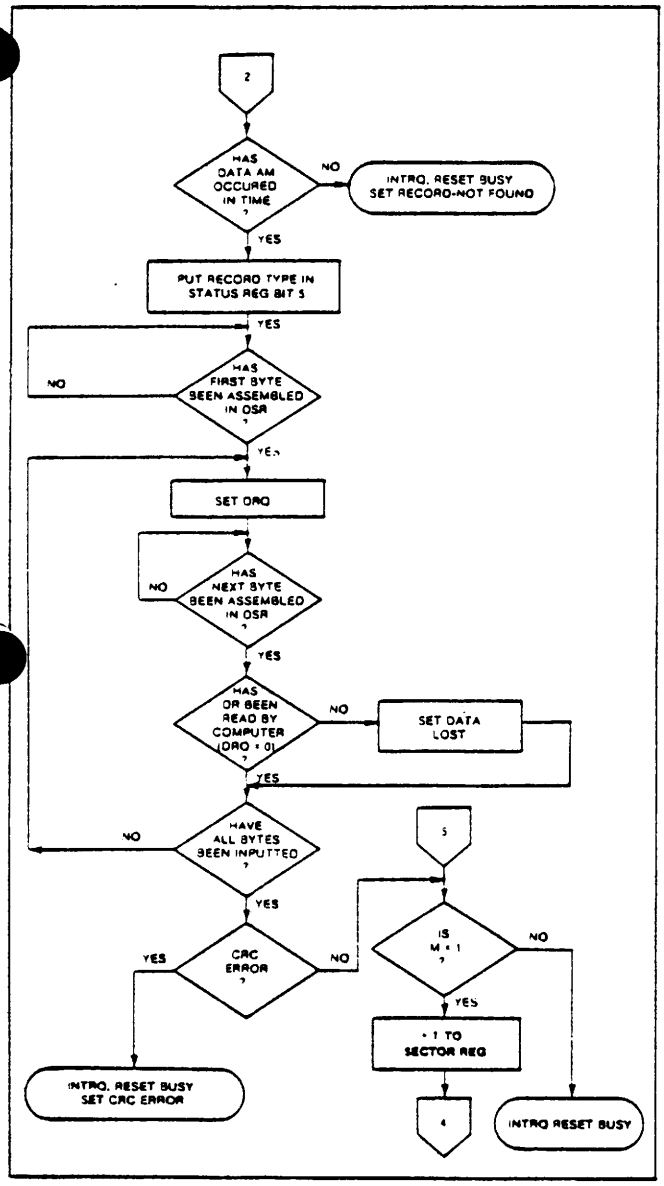
The Type II commands also contain side select compare flags. When C = 0, no side comparison is made. When C = 1, the LSB of the side number is read off the ID Field of the disk and compared with the contents of the (S) flag. If the S flag compares with the side number recorded in the ID field, the 179X continues with the ID search. If a comparison is not made within 5 index pulses, the interrupt line is made active and the Record-Not-Found status bit is set.

The 1795/7 READ SECTOR and WRITE SECTOR commands include a 'b' flag. The 'b' flag, in conjunction with the sector length byte of the ID Field, allows different byte lengths to be implemented in each sector. For IBM compatability, the 'b' flag should be set to a one. The 's' flag allows direct control over the SSO Line (Pin 25) and is set or reset at the beginning of the command, dependent upon the value of this flag.

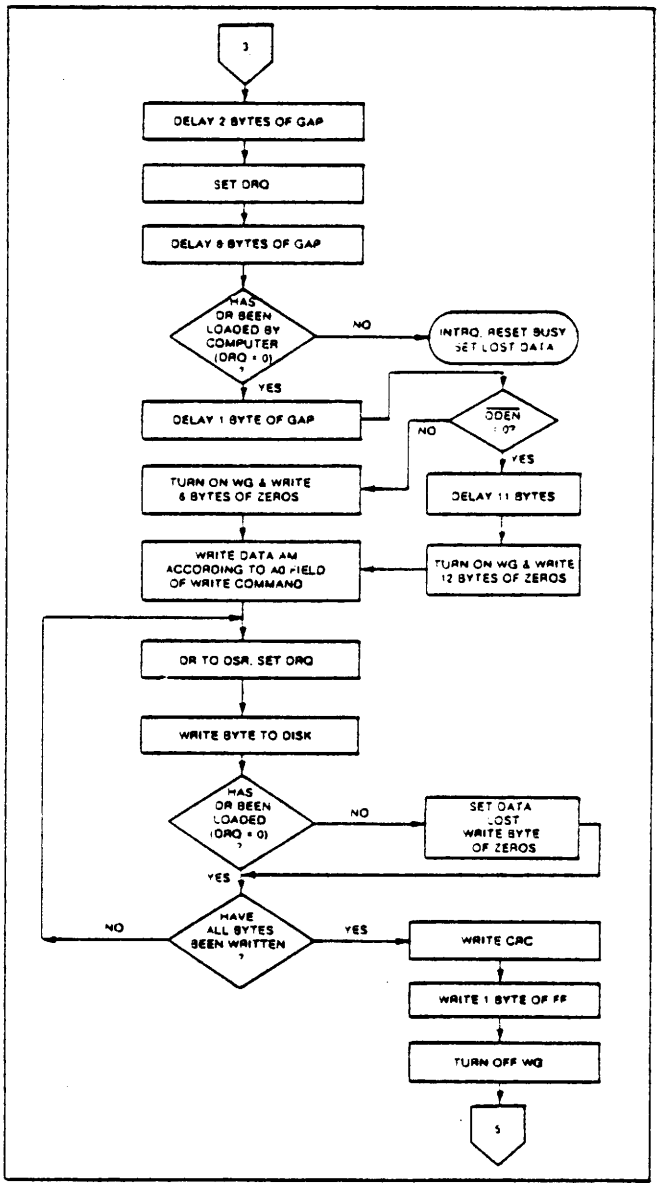
READ SECTOR

Upon receipt of the Read Sector command, the head is loaded, the Busy status bit set, and when an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit is set and the operation is terminated.

When the first character or byte of the data field has been shifted through the DSR, it is transferred to the DR, and DRQ is generated. When the next byte is accumulated in the DSR, it is transferred to the DR and another DRQ is generated. If the Computer has not read the previous contents of the DR before a new character is transferred that character is lost and



TYPE II COMMAND



TYPE II COMMAND

the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set, and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bit 5) as shown below:

STATUS BIT 5	
1	Deleted Data Mark
0	Data Mark

WRITE SECTOR

Upon receipt of the Write Sector command, the head is loaded (HLD active) and the Busy status bit is set. When an ID field is encountered that has the correct track number, correct sector number, correct side number, and correct CRC, a DRQ is generated. The FD179X counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the DR has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, the WG is made active and six bytes of zeros in single density and 12 bytes in double density are then written on the disk. At this time the Data Address Mark is then written on the disk as determined by the a_0 field of the command as shown below:

a_0	Data Address Mark (Bit 0)
1	Deleted Data Mark
0	Data Mark

The FD179X then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing the Lost Data Status Bit is set and a byte of zeros is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the Busy Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	SIDE NUMBER	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD179X checks for validity and the CRC error status bit is set if there is a CRC error. The Track Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the Busy Status is reset.

READ TRACK

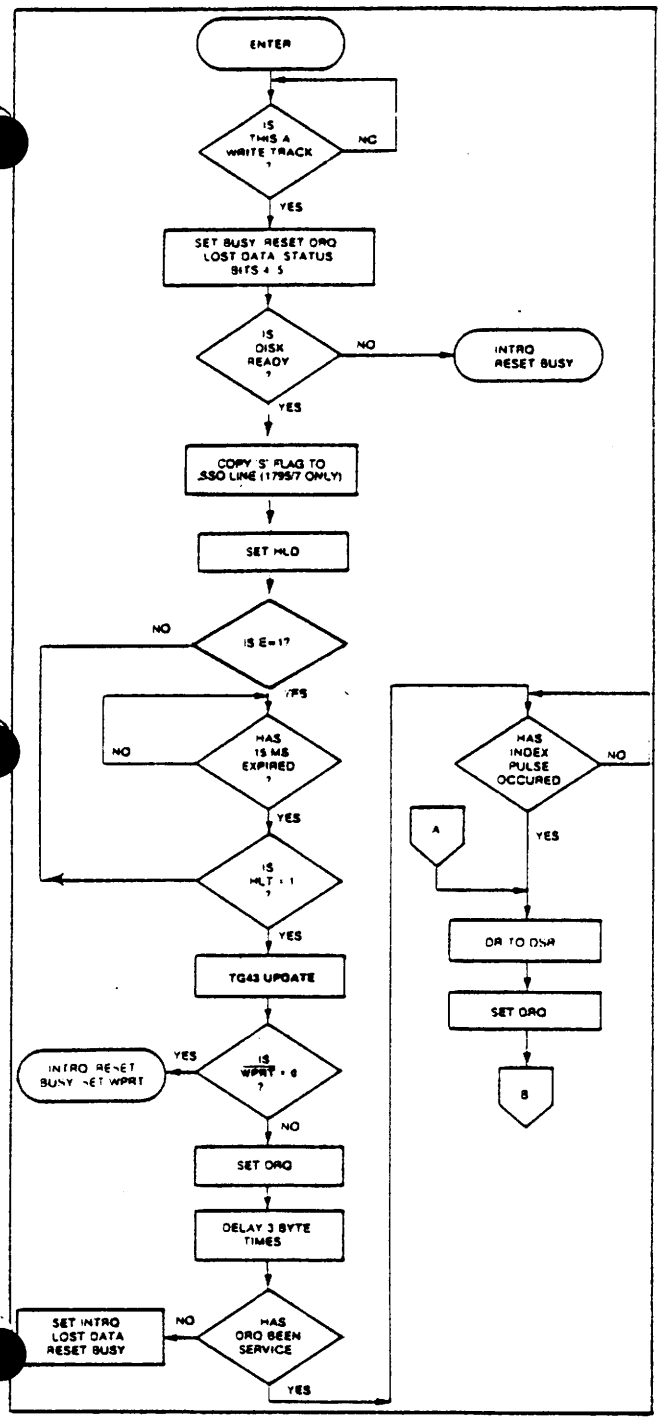
Upon receipt of the Read Track command, the head is loaded and the Busy Status bit is set. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. RG is not activated during the Read Track Command. An internal side compare is not performed during a Read Track.

WRITE TRACK

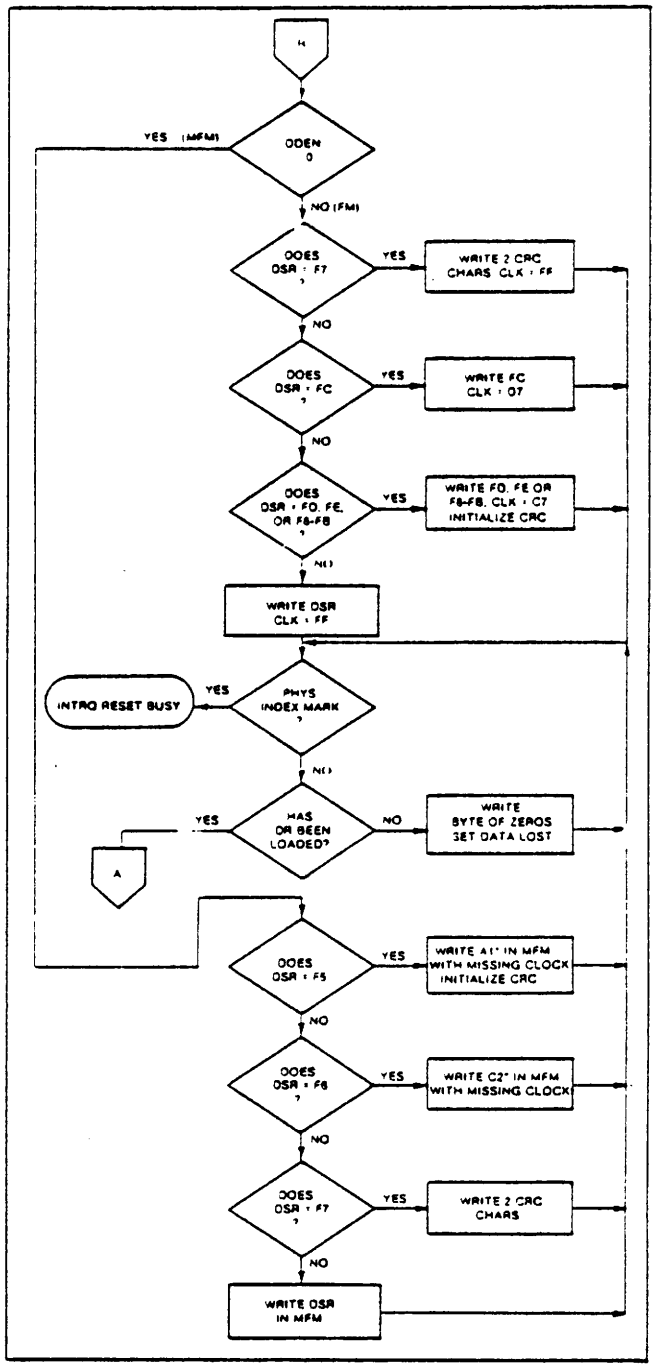
Upon receipt of the Write Track command, the head is loaded and the Busy Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the Interrupt is activated. If a byte is not present in the DR when needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be transferred from the DR to the DSR in FM or by receipt of F5 in MFM.

GAP III	ID AM	TRACK NUMBER	SIDE NUMBER	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP II	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD										DATA FIELD		

In MFM only; IDAM and DATA AM are preceded by three bytes of A1 with clock transition between bits 4 and 5 missing.



TYPE III COMMAND WRITE TRACK



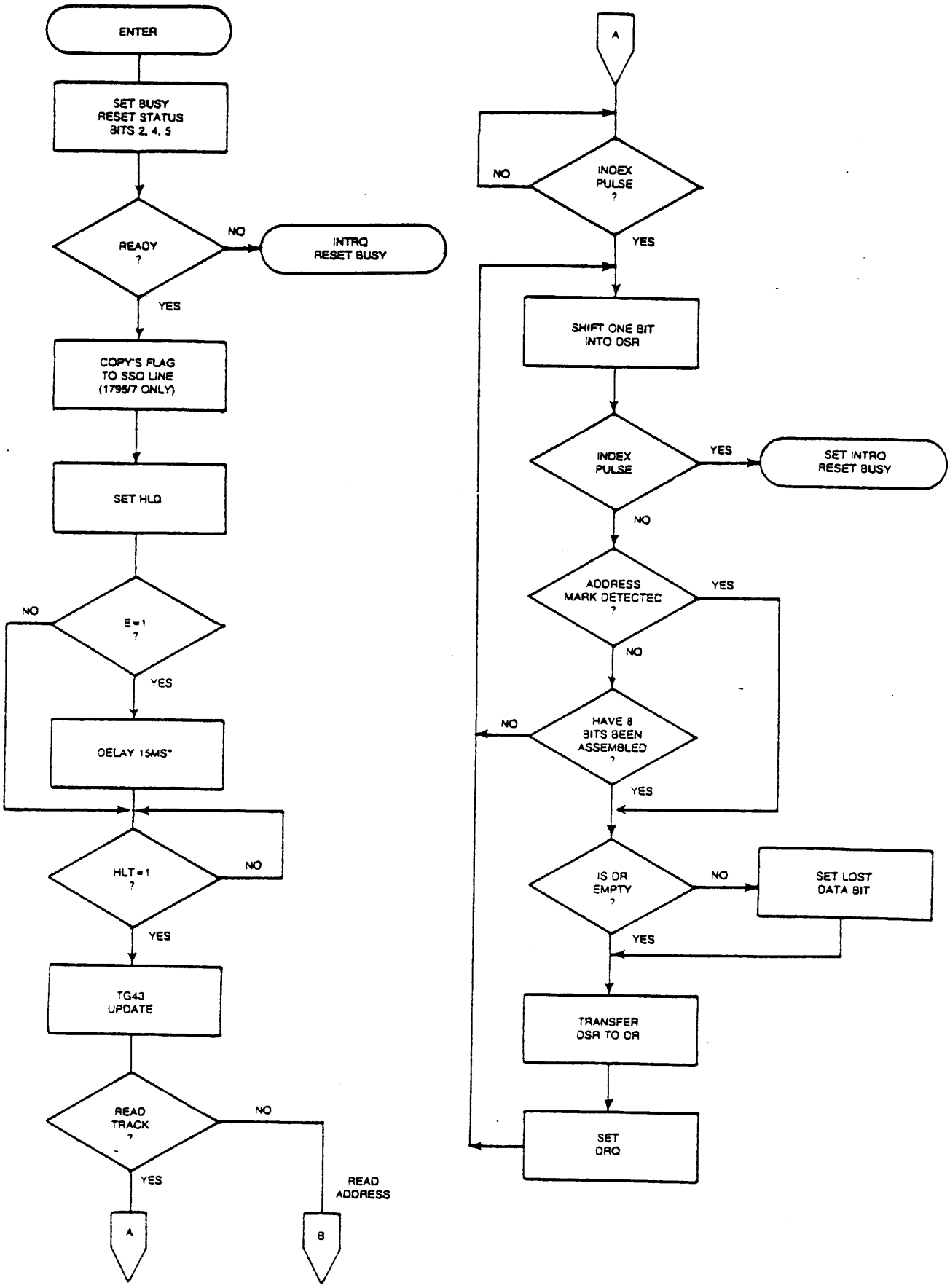
TYPE III COMMAND WRITE TRACK

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN IN DR (HEX)	FD179X INTERPRETATION IN FM ($\overline{DDEN}$ = 1)	FD1791/3 INTERPRETATION IN MFM ($\overline{DDEN}$ = 0)
00 thru F4	Write 00 thru F4 with CLK = FF	Write 00 thru F4, in MFM
F5	Not Allowed	Write A1* in MFM, Preset CRC
F6	Not Allowed	Write C2** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk = C7, Preset CRC	Write F8 thru FB, in MFM
FC	Write FC with Clk = D7	Write FC in MFM
FD	Write FD with Clk = FF	Write FD in MFM
FE	Write FE, Clk = C7, Preset CRC	Write FE in MFM
FF	Write FF with Clk = FF	Write FF in MFM

*Missing clock transition between bits 4 and 5

**Missing clock transition between bits 3 & 4

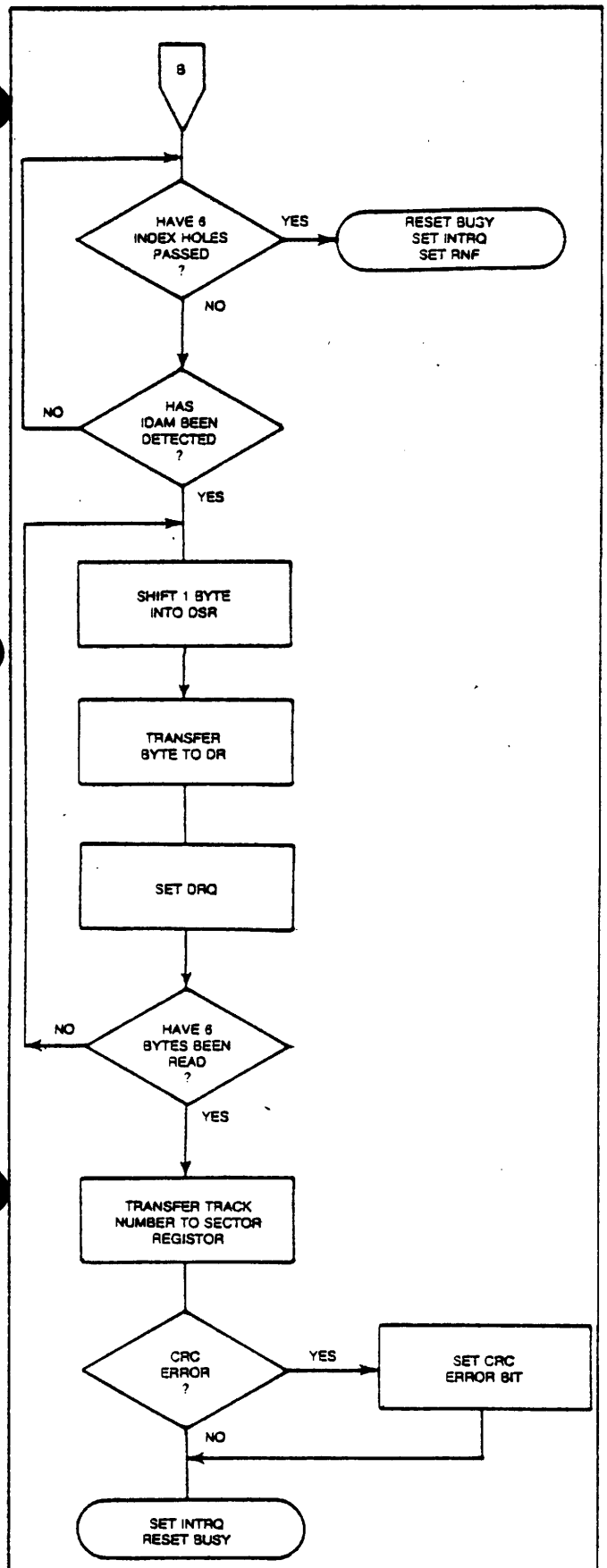


*If TEST = ϕ NO DELAY

If TEST = 1 and CLK = 1 MHZ, 30 MS DELAY

TYPE III COMMAND

Read Track/Address



TYPE III COMMAND

Read Track/Address

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt (requires reset, see Note)

NOTE: If $I_0 - I_3 = 0$, there is no interrupt generated but the current command is terminated and busy is reset. *This is the only command that will enable the immediate interrupt to clear on a subsequent Load Command Register or Read Status Register.*

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the Busy Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the Busy status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the Busy Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under Formatting the disk is accomplished by positioning the R/W head over the desired track number and issuing the Write Track command. Upon receipt of the Write Track command, the FD179X raises the Data Request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a normal clock pattern. However, if the FD179X detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, in FM an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks may be formatted in IBM 3740 or System 34 formats with sector lengths of 128, 256, 512, or 1024 bytes.

IBM 3740 FORMAT—128 BYTES/SECTOR

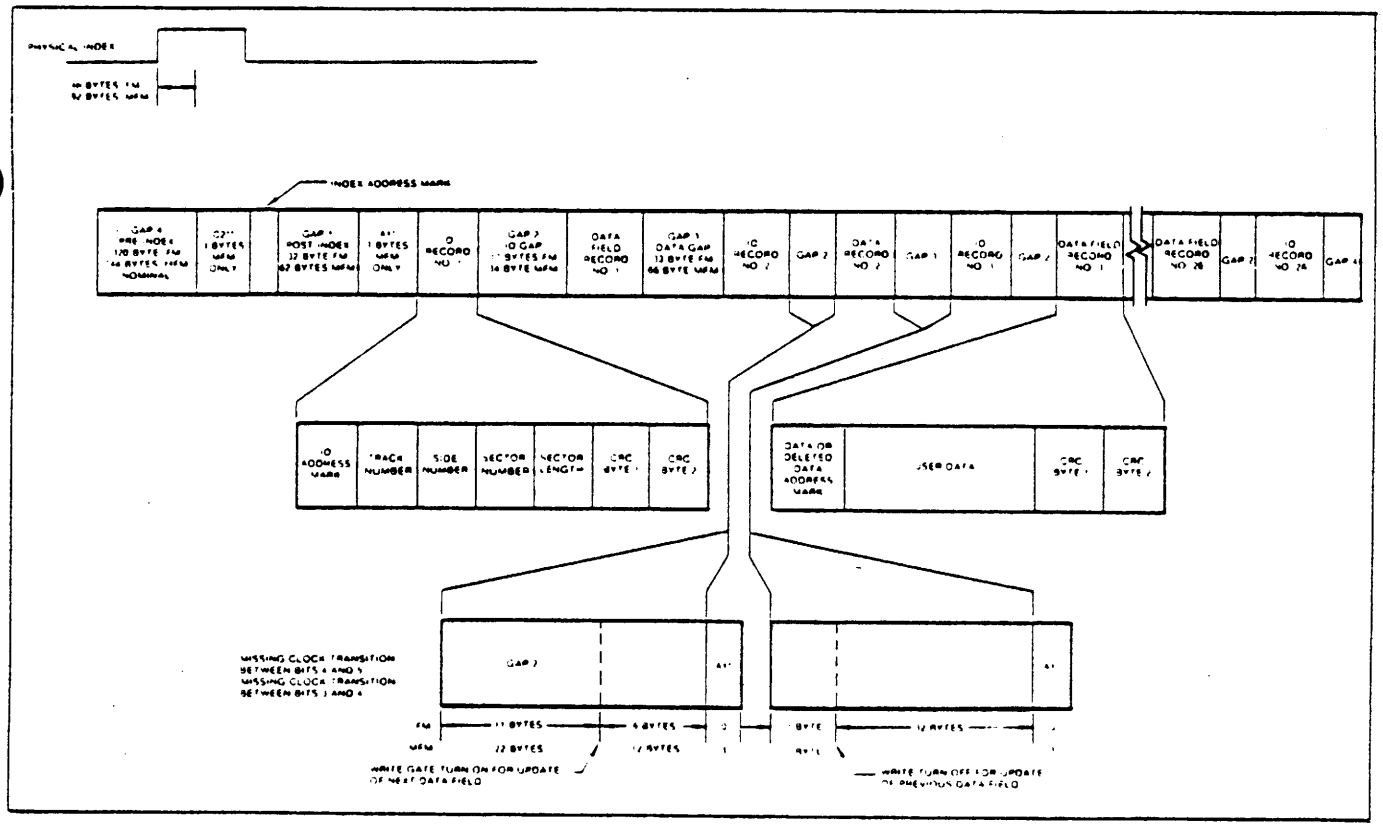
Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
40	FF (or 00)[1]
6	00
1	FC (Index Mark)
26	FF (or 00)
6	00
1	FE (ID Address Mark)
1	Track Number
1	Side Number (00 or 01)
1	Sector Number (1 thru 1A)
1	00
1	F7 (2 CRC's written)
11	FF (or 00)
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	FF (or 00)
247**	FF (or 00)

*Write bracketed field 26 times

**Continue writing until FD179X interrupts out. Approx. 247 bytes.

1-Optional '00' on 1795/7 only.



IBM TRACK FORMAT

IBM SYSTEM 34 FORMAT-256 BYTES/SECTOR

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

NUMBER OF BYTES	HEX VALUE OF BYTE WRITTEN
80	4E
12	00
3	F6
1	FC (Index Mark)
50*	4E
12	00
3	F5
1	FE (ID Address Mark)
1	Track Number (0 thru 4C)
1	Side Number (0 or 1)
1	Sector Number (1 thru 1A)
1	01
1	F7 (2 CRCs written)
22	4E
12	00
3	F5
1	FB (Data Address Mark)
256	DATA
1	F7 (2 CRCs written)
54	4E
598**	4E

* Write bracketed field 26 times
**Continue writing until FD179X interrupts out. Approx. 598 bytes.

1. NON-IBM FORMATS

Variations in the IBM format are possible to a limited extent if the following requirements are met: sector size must be a choice of 128, 256, 512, or 1024 bytes; gap size must be according to the following table. Note that the Index Mark is not required by the 179X. The minimum gap sizes shown are that which is required by the 179X, with PLL lock-up time, motor speed variation, etc., adding additional bytes.

	FM	MFM
Gap I	16 bytes FF	32 bytes 4E
Gap II	11 bytes FF	22 bytes 4E
*	6 bytes 00	12 bytes 00 3 bytes A1
Gap III	10 bytes FF	24 bytes 4E 3 bytes A1
**	4 bytes 00	8 bytes 00
Gap IV	16 bytes FF	16 bytes 4E

*Byte counts must be exact.
**Byte counts are minimum, except exactly 3 bytes of A1 must be written.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground) =15 to −0.3V
Max. Voltage to Any Input With Respect to V_{SS} =15 to −0.3V
Operating Temperature 0°C to 70°C
Storage Temperature −55°C to +125°C

I_{DD} = ID ma Nominal V_{CC} = 35 ma Nominal

OPERATING CHARACTERISTICS (DC)

TA = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = OV, V_{CC} = + 5V ± .25V

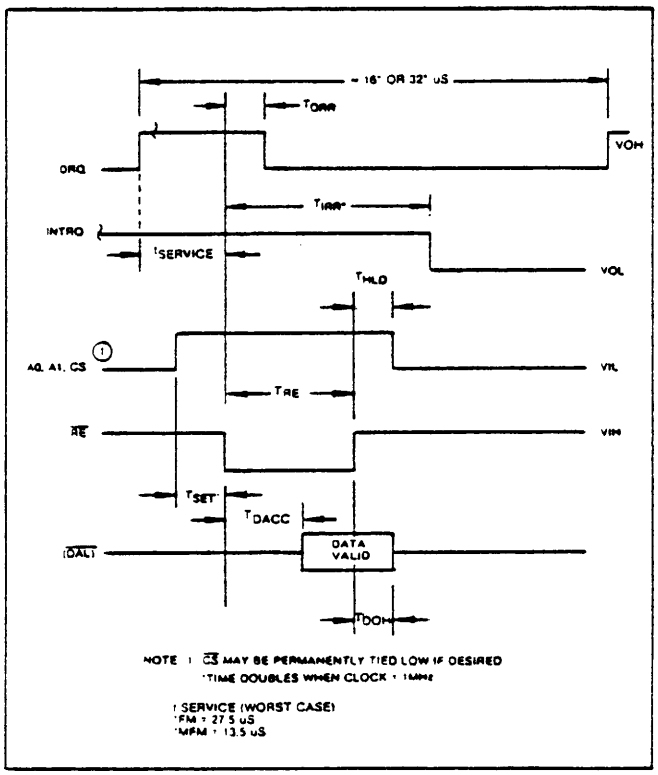
SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
I_{IL}	Input Leakage		10	μA	$V_{IN} = V_{DD}$
I_{OL}	Output Leakage		10	μA	$V_{OUT} = V_{DD}$
V_{IH}	Input High Voltage	2.6		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.8		V	$I_O = -100\ \mu A$
V_{OL}	Output Low Voltage		0.45	V	$I_O = 1.6$ mA
P_D	Power Dissipation		0.5	W	

TIMING CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = + 12V ± .6V, V_{SS} = 0V, V_{CC} = +5V ± .25V

READ ENABLE TIMING

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{RE}$	50	-		nsec	
THLD	Hold ADDR & CS from $\overline{RE}$	10			nsec	
TRE	$\overline{RE}$ Pulse Width	400			nsec	C_L = 50 pf
TDRR	DRQ Reset from $\overline{RE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{RE}$		500	3000	nsec	See Note 5
TDACC	Data Access from $\overline{RE}$			350	nsec	C_L = 50 pf
TDOH	Data Hold From $\overline{RE}$	50		150	nsec	C_L = 50 pf



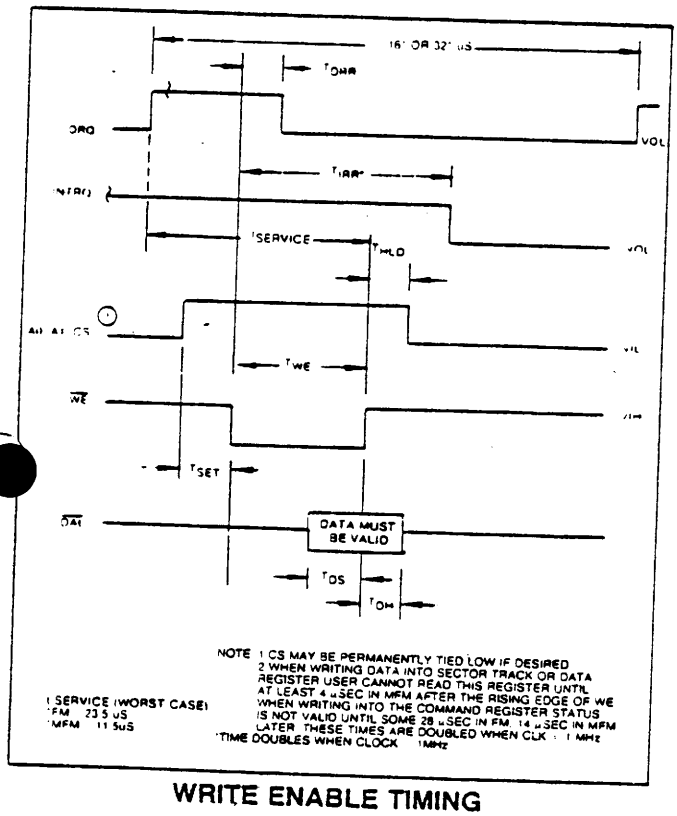
READ ENABLE TIMING

WRITE ENABLE TIMING

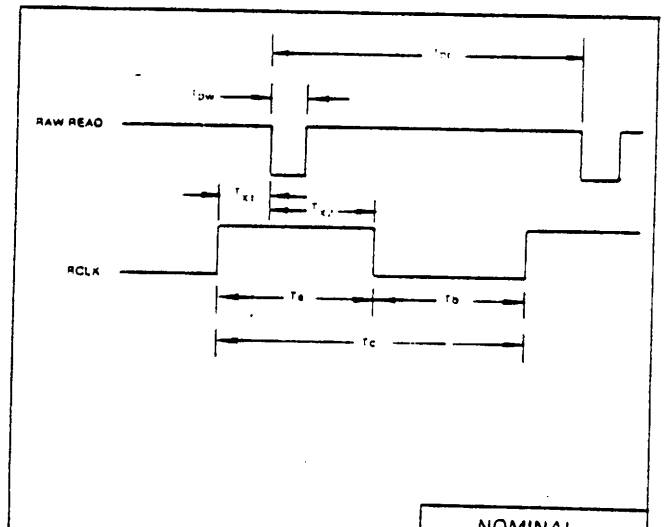
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	50			nsec	
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$		400	500	nsec	
TIRR	INTRQ Reset from $\overline{WE}$		500	3000	nsec	See Note 5
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	70			nsec	

INPUT DATA TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Tpw	$\overline{Raw\ Read}$ Pulse Width	100	200		nsec	See Note 1
tbc	$\overline{Raw\ Read}$ Cycle Time		1500		nsec	1800 ns @ 70°C
Tc	RCLK Cycle Time		1500		nsec	1800 ns @ 70°C
T_{X1}	RCLK hold to $\overline{Raw\ Read}$	40			nsec	See Note 1
T_{X2}	$\overline{Raw\ Read}$ hold to RCLK	40			nsec	



WRITE ENABLE TIMING

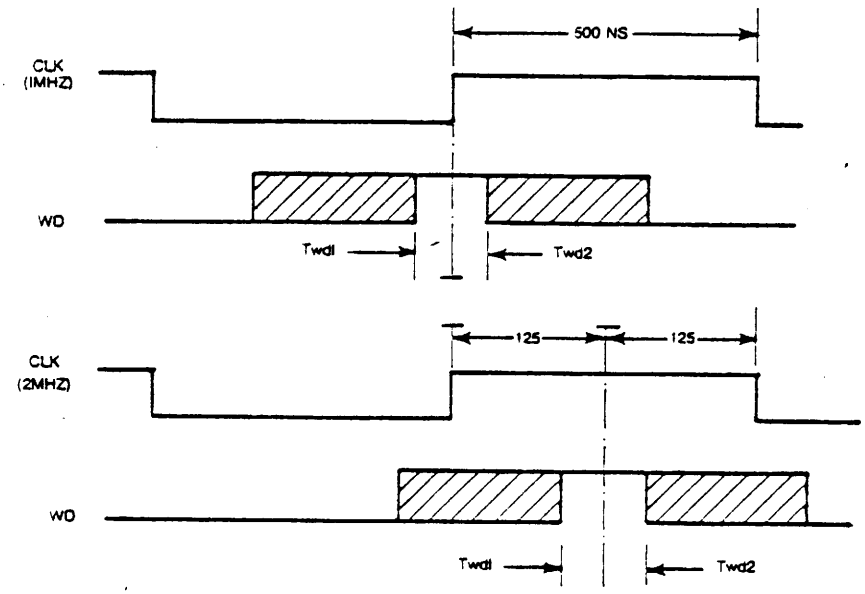


DISKETTE	MODE	$\overline{DDEN}$	CLK	NOMINAL T_a	NOMINAL T_b	NOMINAL T_c
8"	MFM	0	2 MHz	1 µs	1 µs	2 µs
8"	FM	1	2 MHz	2 µs	2µs	4 µs
5"	MFM	0	1 MHz	2 µs	2µs	4 µs
5"	FM	1	1 MHz	4 µs	4 µs	8 µs

INPUT DATA TIMING

WRITE DATA TIMING: (ALL TIMES DOUBLE WHEN CLK = 1 MHz)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Twp	Write Data Pulse Width	450	500	550	nsec	FM
		150	200	250	nsec	MFM
Twg	Write Gate to Write Data		2		µsec	FM
			1		µsec	MFM
Tbc	Write data cycle Time		2,3, or 4		µsec	±CLK Error
Ts	Early (Late) to Write Data	125			nsec	MFM
Th	Early (Late) From Write Data	125			nsec	MFM
Twf	Write Gate off from WD		2		µsec	FM
			1		µsec	MFM
Twd1	WD Valid to Clk	100			nsec	CLK=1 MHZ
		50			nsec	CLK=2 MHZ
Twd2	WD Valid after CLK	100			nsec	CLK=1 MHZ
		30			nsec	CLK=2 MHZ



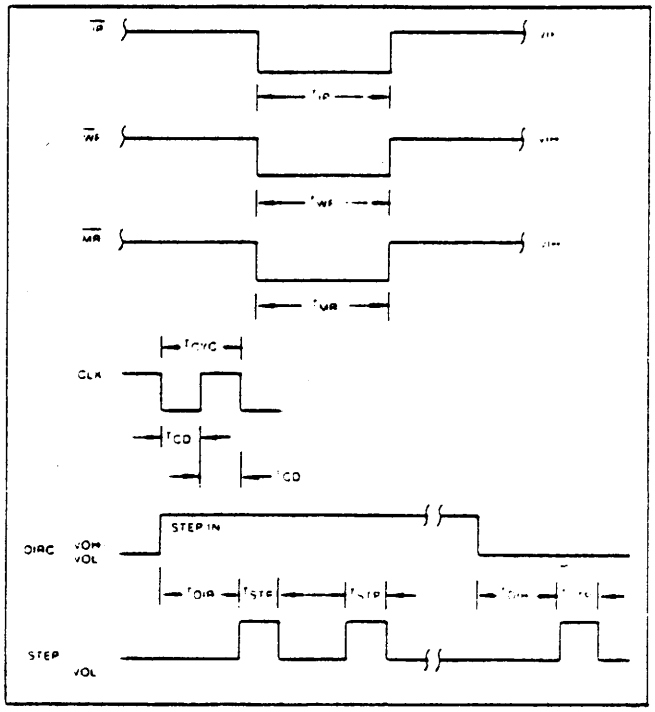
WRITE DATA/CLOCK RELATIONSHIP

($\overline{DDEN}$= 0)

WRITE DATA TIMING

MISCELLANEOUS TIMING:

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
TCD_1	Clock Duty (low)	230	250	20000	nsec	
TCD_2	Clock Duty (high)	200	250	20000	nsec	
TSTP	Step Pulse Output	2 or 4			µsec	See Note 5
TDIR	Dir Setup to Step		12		µsec	± CLK ERROR
TMR	Master Reset Pulse Width	50			µsec	
TIP	Index Pulse Width	10			µsec	See Note 5
TWF	Write Fault Pulse Width	10			µsec	



MISCELLANEOUS TIMING

NOTES:

1. Pulse width on RAW READ (Pin 27) is normally 100-300 ns. However, pulse may be any width if pulse is entirely within window. If pulse occurs in both windows, then pulse width must be less than 300 ns for MFM at CLK = 2 MHz and 600 ns for FM at 2 MHz. Times double for 1 MHz.
2. A PPL Data Separator is recommended for 8" MFM.
3. tbc should be 2 µs, nominal in MFM and 4 µs nominal in FM. Times double when CLK = 1 MHz.
4. RCLK may be high or low during RAW READ (Polarity is unimportant).
5. Times double when clock = 1 MHz.

Table 6. STATUS REGISTER SUMMARY

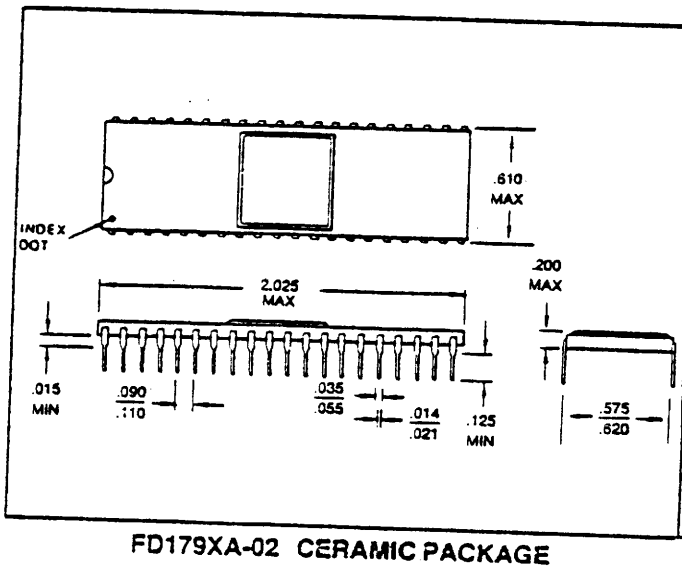
BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ SECTOR	READ TRACK	WRITE SECTOR	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	0	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD LOADED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	RNF	RNF	0	RNF	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

STATUS FOR TYPE I COMMANDS

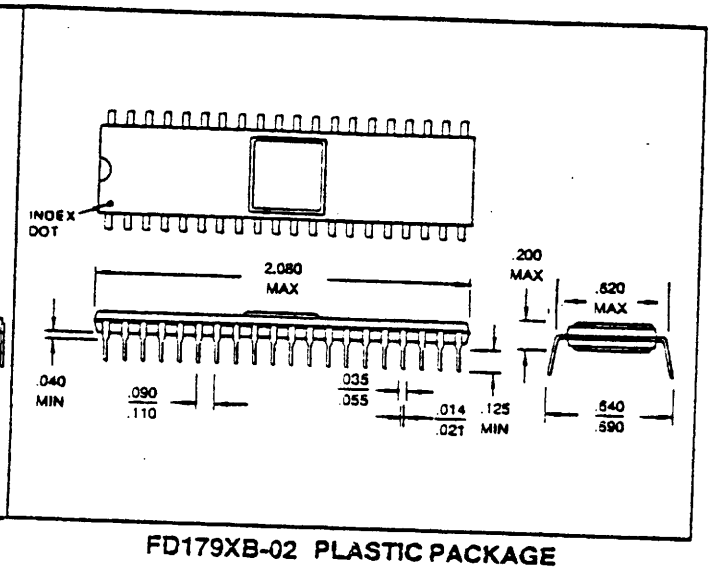
BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the Ready input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of $\overline{WRPT}$ input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	CRC encountered in ID field.
S2 TRACK 00	When set, indicates Read/Write head is positioned to Track 0. This bit is an inverted copy of the $\overline{TR00}$ input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the $\overline{IP}$ input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS FOR TYPE II AND III COMMANDS

BIT NAME	MEANING
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the Ready input and 'ored' with MR. The Type II and III Commands will not execute unless the drive is ready.
S6 WRITE PROTECT	On Read Record: Not Used. On Read Track: Not Used. On any Write: It indicates a Write Protect. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the record-type code from data field address mark. 1 = Deleted Data Mark. 0 = Data Mark. On any Write: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND (RNF)	When set, it indicates that the desired track, sector, or side were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read Operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.



FD179XA-02 CERAMIC PACKAGE



FD179XB-02 PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

WESTERN DIGITAL CORPORATION
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NEWPORT BEACH, CA 92663 (714) 557-3550, TWX 910-595-1139

5. FIRMWARE

This section contains listnings and descriptions of the firmware in the 2 versions of the ST. FD. CTRL.

K

5.1 Microprogram of CR804D/010AB/00

CSD/005/LST/0014

K

TITLE: MICROPROGRAM SOURCE LISTNING
FOR ST. FD. CTRL. 8047M/010AB/00

DOCUMENT NO : CSD/005/LST/0014

PREPARED BY : BERTRAM PAASKESEN

AUTHORIZED BY: GOTTLOB BORUP

DISTRIBUTION : GB, BBP, File(2), PRO(2)

APPROVED BY:

AUTHORITY	DATE	SIGNATURE
ENG/QA-KN		

ISSUE: 1

DATE: 820111

400-810-1

MICROPROGRAM SOURCE LISTNING FOR ST. FD. CTRL. CR8047M/010AB/00	sign/date BBP/820111	page i
	repl	project

PAGE RECORD AND ISSUE LOG.

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ISSUE	DATE	PREPARED BY	APPROVED BY	AUTHORIZED BY
1	820111	BBP	KN	GB

A

CONTENTS

APPLICABLE DOCUMENTS

CR80 AMOS TOS	CSS/380/USM/0026
CR80 AMOS CMI	CSS/381/USM/0037
CR80 AMOS EDITOR	CSS/102/USM/0021
MICAS MICROASSEMBLER	CSS/006/USM/0019
CR80 AMOS COPY	CSS/110/USM/0032

MICRO PROGRAM SOURCE LISTNING FOR ST. FD. CTRL. CR8047M/010AB/00	sign/date BBP/820111	page 1
	replace	project

1. INTRODUCTION

This document contains descriptions of source-, command- and object files concerning the micro-firmware included in the Dual Bus Floppy Disk Controller (CR8047M/010AB/00.

The Firmware allows the ST. FD. CTRL. to interface SHUGART SA 800/850 Floppy Disk Drives as described in:

CSD/005/PSP/0078

The PROM's which contain the microprogram, are described in CSD/005/VDD/0058.

2. STRUCTURE OF MICROPROGRAM DEVELOPMENT PHASE

The microprogram coding and assembly is performed by an AMOS development system, and the following explanation requires a basical knowledge about AMOS at user level.

Four different programs are called in the sequence shown in fig. 1. Each program uses a number of files which contain source-, object- and print code, List 1 shows the files concerned. These files are stored on harddisk in the following directory:

∂*CRP0004*USERS.D*HCL.D*BBP.D*CR8047DAB.D

A back-up issue of the files is stored on floppy disk in the following directory:

∂*CRD2192

For the sake of convenience a special commandfile (a DO-type) called:

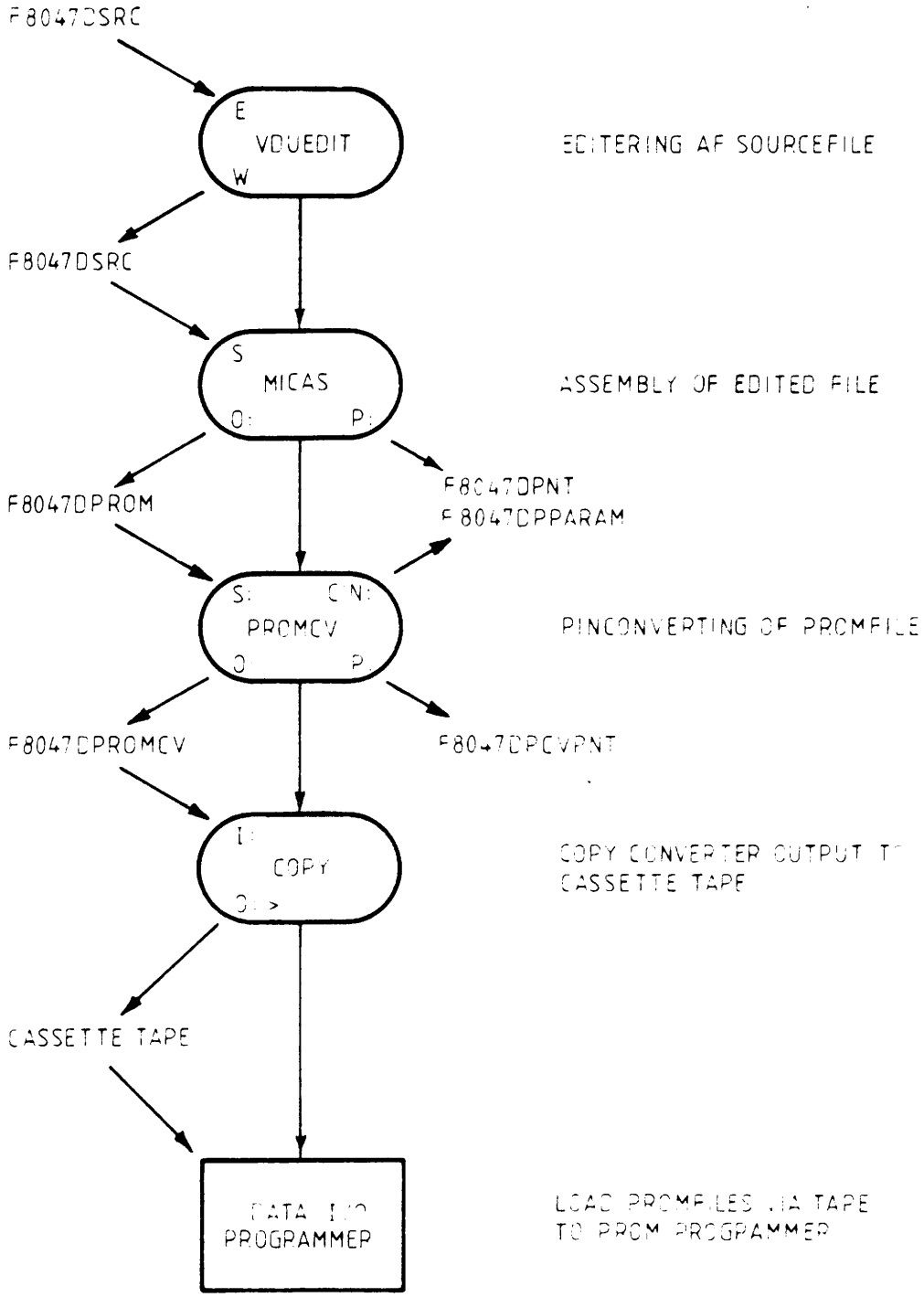
----CR8047DAB.D*DOMICASPROMCV

are generated and a call of this file, does automatic perform the MICAS, PROMCV sequence, and deliver prober output files for copy. F8047DPNT and F8047DPCVPNT are printed out as hard copy.

```
*****************************************************************
*
* FILE: SDMACCO-FILE*CPPCCC4*LSEPS.D*HCL.D*BBP.D*CR8047DAB.D*TEMP
*
* DATE: 80:01:15
*
* TIME: 14:28:24
*
*****************************************************************
```

NAME	TYPE	SIZE	ALLOCATED	AREASIZE
F8047DSRC	RANDOM	63601	125	1
F8047DPROM	RANDOM	22370	44	1
F8047DPNT	RANDOM	0	0	4
F8047DPROMOV	RANDOM	22430	44	1
F8047DPOVPNT	RANDOM	0	0	4
F8047DPPARAM	RANDOM	250	1	1
DOMIDASPROMOV	RANDOM	152	1	1
BESKRIVELSE	RANDOM	656	2	1
TEMP	RANDOM	0	0	1

MICROPROGRAM SOURCE LISTNING FOR ST. FD. CTRL. CR8047M/010AB/00	sign/date BBP/820111	page 4
	replace	project



F 3 :

3. LISTNING OF SOURCEFILE

The following section shows file: F8047SRC generated by MICAS, (actual the first part of F8047PNT).

K

```
                    ---------------------------
                    MICAS MICRO ASSEMBLER V800123
                    ---------------------------

0000            WORDLENGTH=56 ,
0000             PROMWIDTH=8 ,
0000            JUMPDED=1 ,
0000            PROMLENGTH=1024
0000
0000            .
0000
0000             1  5 10   0 ,
0000             2 24 8   0 ,
0000             3  0 1   0 ,
0000             4  14 1   0 ,
0000             5  1 4   1 ,
0000             6 15 2   1 ,
0000             7 17 2   0 ,
0000             8 19 3   0 ,
0000             9 22 2   1 ,
0000            10 32 1   0 ,
0000            11 33 3   0 ,
0000            12 36 4   0 ,
0000            13 40 7 125 ,
0000            14 47 1   1 ,
0000            15 48 1   1 ,
0000            16 49 1   1 ,
0000            17 50 1   1 ,
0000            18 51 1   1 ,
0000            19 52 2   0 ,
0000            20 54 2   2 ,
0000            .
0000
0000
0000             UNC=1,3
0000             CLIN=1,4
0000             JZ=15,5
0000             CJS=14,5
0000             JMP=13,5
0000             CJP=12,5
0000             PCLC=11,5
0000             JRP=8,5
0000             RFCT=7,5
0000             RPCT=6,5
0000             CRET=5,5
```

```
0000            CJPP=4,5
0000            LDCT=3,5
0000            ENLD=2,5
0000            TWB=0,5
0000
0000            CLBY=0,6
0000            STBY=3,6
0000
0000            STCM=0,7
0000            TRK=1,7
0000            SCT=2,7
0000            DAT=3,7
0000
0000            AQ=0,8
0000            AB=1,8
0000            ZQ=2,8
0000            ZA=4,8
0000            DA=5,8
0000            DQ=6,8
0000            DZ=7,8
0000
0000            Q=0,9
0000            BA=2,9
0000            B=3,9
0000
0000            C=1,10
0000
0000            ADD=0,11
0000            SUB=1,11
0000            BUS=2,11
0000             OR=3,11
0000            AND=4,11
0000            IAN=5,11
0000            EXO=6,11
0000            EXN=7,11
0000
0000            A0=0,12
0000            A1=1,12
0000            A2=2,12
0000            A3=3,12
0000            A4=4,12
0000            A5=5,12
0000            A6=6,12
0000            A7=7,12
0000            A8=8,12
0000            A9=9,12
0000            A10=10,12
0000            A11=11,12
```

```
0000            A12=12,12
0000            A13=13,12
0000            A14=14,12
0000            A15=15,12
0000
0000            COND=126,13
0000            RDY=123,13
0000            RAM=119,13
0000            RL=111,13
0000            RU=95,13
0000            DAL=63,13
0000            NIB=127,13
0000
0000            RIC=0,14
0000            UPBY=0,15
0000            UNIT=0,16
0000            WIC=0,17
0000            LATCH=0,18
0000            WRA=1,19
0000            DU=2,19
0000            DL=3,20
0000            HR=0,20
0000            BIT1=#3FF,1
0000            .
```

```
0000
0000
0000
0000            ;ST FD CTRL CR8047D/010AB/01 ;.
0000            ;FIRMWARE VERSION 811130/BBP ;.
0000            ;BUILD-IN-TEST IMPLEMENTED ;.
0000            ;UPDATED LAST: 820116.
0000          ;.
0000        BIT:   UNC CJP T2910                    STBY MR          ;SET BUSY MR1791  ;.
0001               JZ                               STBY MR          ;2910 ERROR  ;.
0002               UNC CJS BIT1                     STBY MR          ;TRY RESET CMD  ;.
0003          ;.
0003          ;.
0003        E2910: UNC CJP LOC                     STBY MR ;.
0004
0004        E2901:  UNC CJP LOC                     STBY MR ;.
0005          ;.
0005        EIBUS: UNC CJP LOC                     STBY MR ;.
0006          ;.
0006        EABBUS: UNC CJP LOC                     STBY MR ;.
0007          ;.
0007        ERAM:   UNC CJP LOC                     STBY MR ;.
0008          ;.
0008        ETIMER: UNC CJP LOC                     STBY MR ;.
0009          ;.
0009        E1791:  UNC CJP LOC                     STBY MR ;.
000A          ;.
000A          ;.
000A               ;******   2901 TEST SUBROUTINES ****** ;.
000A        T29011:          AND ZA AO              B MR             ;AO_00 Y=RESULT Z=1 ;.
000B                        BUS ZA AO               B MR             ;AO_#FF Y=RESULT Z=0 ;.
000C               CJP E2910        AND ZA AO       B MR             ;Z=1 ;.
000D               CRET             BUS ZA AO       B MR             ;Z=0 TEST CRET ;.
000E               UNC CJP E2910                      MR    ;RETURN TO MAIN PROGRAM ;.
000F          ;.
000F          ;.
000F          ;.
000F               ;*****   2910 TEST SUBROUTINES ****** ;.
000F          ;.
000F        T29101: UNC CRET                          MR ;.
0010               UNC E2910                         MR ;.
0011          ;.
0011        T29102: UNC CJS T29103                    MR ;.
0012               UNC CJP E2910                     MR ;.
0013          ;.
0013        T29103: UNC CJP T29104                    MR ;.
0014               UNC CJP E2910                     MR    ;COME HERE IF JPP DEFECT ;.
```

```
0015          ;.
0015        T29104: UNC CRET                                MR    ;RETURN TO T2910 IF POP OK ;.
0016                                                              ;ELSE RETURN TO T29102+1 ;.
0016        T29105: CJS E2910        AND ZA A0        B MR ;.
0017                CJS T29103       BUS ZA A0        B MR    ;CALL IF OK ;.
0018                UNC CJP E2910                       MR    ;ELSE GOTO ERROR LOOP ;.
0019          ;.
0019        T29107: UNC CJS T29103                      MR    ;PUSH T29107+1 TO STACK ;.
001A                UNC CJP E2910                       MR    ;COME IF POP ERROR ;.
0018          ;.
0018        T29108:                  AND ZA A0        B MR    ;CLEAR REG 0 ;.
001C                CJPP T29109      BUS ZA A0        B MR    ;FORCE THE JUMP CONDITION ;.
001D                UNC CJP E2910                       MR    ;ERROR EXIT ;.
001E          ;.
001E        T29109: UNC CRET                            MR    ;RETURN TO MAINLOOP IF POP ;.
001F                                                              ;WAS OK,ELSE RET TO T29107+1 ;.
001F          ;.
001F        T2910A: LDCT T29108                         MR    ;REG_JUMP ENTRY ;.
0020                JRP              AND ZA A0        B MR    ;JUMP TO LOC T29108 ;.
0021               UNC CJP E2910                        MR    ;.
0022          ;.
0022        T29108: UNC CRET                            MR    ;COME HERE IF LDCT&JRP WASS ;.
0023                                                              ;OK ;.
0023          ;.
0023          ;.
0023        T2910C: LDCT 1(#FF)      AND ZA  A0       B MR    ;LOAD COUNTER R0_0 ;.
0024                RPCT LOC         SUB ZA A0        B MR    ;DECREMENT COUNTER ;.
0025                CJP E2910        OR  ZA A0          MR    ;.
0026                UNC CRET                            MR    ;COME IF CNT=R0 ;.
0027        T2910D: UNC PCLC 1(#FF) AND ZA A0         B MR    ;LOAD COUNTER+STACK ;.
0028                RPCT             SUB ZA A0        B MR    ;DCR COUNTER A0_A0+1 ;.
0029                CJP E2910        OR ZA A0           MR    ;.
002A                UNC CRET                            MR ;.
002B          ;.
002B                ;*****   1791 TEST SUBROUTIN   *****
002B                 ENTRY:  R10= PREVIOUS STATE
002B                 EXIT:   R9 = CURRENT STATE OF INPUT REGISTER
002B                         R10= LAST STATE OF STPU
002B                         R1 DESTROED.
002B
002B        W1STPU:                  AND ZA A1        B       ;CLEAR COUNT REG.
002C        W1ST:   LDCT 1(#20)      OR  DZ A8 COND   B       ;READ INPUT REG.
002D                     2(#40)      AND DA A8        Q       ;MASK STPU BIT.
002E                CRET             IAN AQ A10               ;RETURN IF POS EDGE.
002F                RPCT W1ST        OR  ZQ A10       B       ;UPDATE STATE REG.
0030                               C ADD ZA A1        B       ;INCREMENT LOOP CNT.
0031                CJP W1ST         OR  ZA A1                ;LOOP MAX 10 MSEC.
0032           UNC  CJP E1791                                 ;THEN GIVE UP.
```

```
0033
0033                ;*****   2910 TEST MAINLOOP ***** ;.
0033          ;.
0033          T2910:  UNC CJS T29101                      MR    ;TEST CALL/RET ;.
0034                UNC CJS T29102                      MR    ;TEST JPP ;.
0035          ;.
0035                ;THE FOLLOWING 2901 TEST MUST BE PERFORMED BEFORE ;.
0035                ;TEST OF 2910 CONDITIONAL JUMP FACILITIES  ;.
0035          ;.
0035                UNC CJS T29011                      MR     ;TEST ZERO FLAG ON ;.
0036                                                           ;JUMPS/RET ;.
0036                UNC CJS T29105                      MR    ;TEST CJS ;.
0037                UNC CJS T29107                      MR    ;TEST CJPP ;.
0038                UNC CJS T2910A                      MR    ;TEST LDCT ;.
0039                UNC CJS T2910C                      MR    ;TEST RPCT/DCR ALU REG 0 ;.
003A                UNC CJS T2910D                      MR    ;TEST RFCT ;.
0038          ;.
0038                ;***** TEST 2901 LOGICAL FUNCTIONS ***** ;.
0038          ;.
0038          A29010: LDCT 1(#0E)      AND ZA A1        B MR    ;LOAD CNTR CLEAR REG 1 ;.
003C                RPCT LOC       C ADD ZA A1        B MR    ;PRESET REG 1 TO #0F ;.
003D                CJP A29011       OR ZA  A1          MR    ;IS REG 1 =I 0 ;.
003E                UNC CJP E2901                       MR    ;NO ;.
003F          ;.
003F          A29011:                 OR  ZA A1        Q MR ;.
0040                                  OR  ZQ A0        B MR    ;COPY R1 TO R0 ;.
0041                LDCT 1(#EF)       AND ZA A2        B MR    ;PRESET A2 TO #F0 ;.
0042                RPCT LOC       C ADD ZA A2        B MR ;.
0043                CJP A29012        OR  ZA A2          MR    ;TEST RESULT ;.
0044                UNC CJP E2901                       MR.
0045          ;.
0045          A29012:                 OR  ZA A2        Q MR ;.
0046                                  OR  ZQ A3        B MR    ;COPY R2 TO R3 ;.
0047                                  ADD AQ A0        Q MR    ;TEST ADD ;.
0048                CJP E2901      C ADD ZQ              MR    ;RESULT=0 IF OK ;.
0049                                  OR  ZA A3        Q MR    ;Q=F0 ;.
0044                                  OR  AQ A0        Q MR    ;COMPUTE F0-OR-0F ;.
0043                CJP E2901      C ADD ZQ              MR    ;TEST RESULT (0 IF OK) ;.
004C                                  OR  ZA A3        Q MR    ;Q=F0 ;.
004D                                  IAN AQ A0        Q MR    ;TEST IAN (0 IF OK) ;.
004E                                  ADD AQ A1        Q MR ;.
004F                CJP E2901      C ADD ZQ              MR    ;END OF MSNYBBLE TEST ;.
0050                                  OR  ZA A1        Q MR    ;Q=0F ;.
0051                                  IAN AQ A3        Q MR    ;Q=0F IF OK ;.
0052                                  ADD AQ A2        Q MR    ;Q=FF IF OK ;.
0053                CJP E2901      C ADD ZQ              MR    ;END OF LSNYBBLE TEST ;.
0054          ;.
0054                ;***** XOR TEST ***** ;.
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0054            ;.
0054                  LDCT 1(#54)      AND ZA A4        B MR ;.
0055                  RPCT LDC       C ADD ZA A4        B MR     ;PRESET R4 TO #55 ;.
0056                                   EXO AQ A4        Q MR     ;Q=55 IF OK ;.
0057                                   AND ZA A5        B MR ;.
0058                                   SUB ZA A5        B MR     ;R5=FF ;.
0059                                   EXO AQ A5        B MR     ;R5=#AA IF OK ;.
005A                                   ADD AQ A5        Q MR     ;Q=00 IF OK ;.
005B                  CJP E2901      C ADD ZQ           Q MR ;.
005C            ;.
005C                  ;***** XNOR TEST ***** ;.
005C            ;.
005C                                   EXN AQ A5        Q MR     ;Q=55 IF OK ;.
005D                  CJP E2901        EXN AQ A5        Q MR     ;Q=00 IF OK ;.
005E            ;.
005E                  ;****** TEST Q-REG ****** ;.
005E          T29012:                   AND ZA A0        B MR ;.
005F                                   AND ZQ           Q MR     ;CREAR RO & QREG ;.
0060                  CJP E2901        OR  AQ A0          MR ;.
0061                                   SUB ZA A0        B MR     ;A0_#FF ;.
0062                  CJP T29013       OR  ZA A0        Q MR ;.
0063             UNC CJP E2910                            MR     ;.
0064          T29013: CJP E2901      C SUB AQ A0          MR     ;JUMP IF ERROR ;.
0065            ;.
0065                  ;****** TEST GENERAL PURPOSE REGISTERS ****** ;.
0065            ;.
0065                  LDCT 1(#FF)      AND ZA A0        B MR ;.
0066                                   AND ZQ           Q MR     ;CLEAR RO & QREG ;.
0067          T29014:                C ADD ZA A0        B MR     ;TEST INCREMENT INSTRUCTION ;.
0068                                 C ADD ZQ           Q MR     ;  --"-- ON QREG ;.
0069                  CJP E2901      C SUB AQ A0            MR ;.
006A                  RPCT T29014                         MR     ;REPEAT TEST ON ALL REG S ;.
006B                  LDCT 1(#FF)    AND ZA A1        B MR ;.
006C          T29015:                C ADD ZA A1        B MR     ;A1_A1+1 ;.
006D                                 C ADD ZQ           Q MR     ;Q_Q+1 ;.
006E                  CJP E2901      C SUB AQ A1            MR ;.
006F                  RPCT T29015                         MR     ;TRY ALL BINARY COMBINATIONS ;.
0070                                                              ;ON EVERY OF THE 2901 REG ;.
0070                  LDCT 1(#FF)    AND ZA A2        B MR     ;TEST REG 2 ;.
0071          T29016:                C ADD ZA A2        B MR ;.
0072                                 C ADD ZQ           Q MR ;.
0073                  CJP E2901      C SUB AQ A2          MR ;.
0074                  RPCT T29016                       MR.
0075            ;.
0075                  LDCT 1(#FF)    AND ZA A3        B MR     ;TEST REG 3 ;.
0076          T29017:                C ADD ZA A3        B MR ;.
0077                                 C ADD ZQ           Q MR ;.
0078                  CJP E2901      C SUB AQ A3          MR ;.
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0079                RPCT T29017                          MR       ;.
007A                LDCT 1(#FF)    AND ZA A4        B MR     ;TEST REG 4 ;.
007B        T29018:                  C ADD ZA A4        B MR ;.
007C                               C ADD ZQ          Q MR ;.
007D                CJP E2901      C SUB AQ A4          MR ;.
007E                RPCT T29018                         MR       ;.
007F         ;.
007F                LDCT 1(#FF)    AND ZA A5        B MR     ;TEST REG 3 ;.
0080        T29019:                  C ADD ZA A5        B MR ;.
0081                               C ADD ZQ          Q MR ;.
0082                CJP E2901      C SUB AQ A5          MR ;.
0083                RPCT T29019                         MR       ;.
0084         ;.
0084                LDCT 1(#FF)    AND ZA A6        B MR     ;TEST REG 6 ;.
0085        T2901A:                C ADD ZA A6        B MR ;.
0086                               C ADD ZQ          Q MR ;.
0087                CJP E2901      C SUB AQ A6          MR ;.
0088                RPCT T2901A                         MR.
0089         ;.
008A                LDCT 1(#FF)    AND ZA A7        B MR     ;TES  REG 7 ;.
008A        T2901B:                C ADD ZA A7        B MR ;.
008B                               C ADD ZQ          Q MR ;.
008C                CJP E2901      C SUB AQ A7          MR ;.
008D                RPCT T2901B                         MR.
008E         ;.
008E                LDCT 1(#FF)    AND ZA A8        B MR     ;TEST REG 8 ;.
008F        T2901C:                C ADD ZA A8        B MR ;.
0090                               C ADD ZQ          Q MR ;.
0091                CJP E2901      C SUB AQ A8          MR ;.
0092                RPCT T2901C                         MR.
0093         ;.
0093                LDCT 1(#FF)    AND ZA A9        B MR     ;TEST REG 9 ;.
0094        T2901D:                C ADD ZA A9        B MR ;.
0095                               C ADD ZQ          Q MR ;.
0096                CJP E2901      C SUB AQ A9          MR ;.
0097                RPCT T2901D                         MR.
0098         ;.
0098                LDCT 1(#FF)    AND ZA A10       B MR     ;TEST REG 10 ;.
0099        T2901E:                C ADD ZA A10       B MR ;.
009A                               C ADD ZQ          Q MR ;.
009B                CJP E2901      C SUB AQ A10         MR ;.
009C                RPCT T2901E                         MR.
009D         ;.
009D                LDCT 1(#FF)    AND ZA A11       B MR     ;TEST REG 11 ;.
009E        T2901F:                C ADD ZA A11       B MR ;.
009F                               C ADD ZQ          Q MR ;.
00A0                CJP E2901      C SUB AQ A11         MR ;.
00A1                RPCT T2901F                         MR.
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00A2            ;.
00A2                  LDCT 1(#FF)    AND ZA A12      B MR    ;TEST REG 12 ;.
00A3            T29020:              C ADD ZA A12      B MR    ;TEST REG 12 ;.
00A4                                 C ADD ZQ          Q MR ;.
00A5                  CJP E2901      C SUB AQ A12        MR ;.
00A6                  RPCT T29020                        MR.
00A7            ;.
00A7                  LDCT 1(#FF)    AND ZA A13      B MR    ;TEST REG 13 ;.
00A8            T29021:              C ADD ZA A13      B MR ;.
00A9                                 C ADD ZQ          Q MR ;.
00AA                  CJP E2901      C SUB AQ A13        MR ;.
00AB                  RPCT T29021                        MR.
00AC            ;.
00AC                  LDCT 1(#FF)    AND ZA A14      B MR    ;TEST REG 14 ;.
00AD            T29022:              C ADD ZA A14      B MR ;.
00AE                                 C ADD ZQ          Q MR ;.
00AF                  CJP E2901      C SUB AQ A14        MR ;.
00B0                  RPCT T29022                        MR.
00B1            ;.
00B1                  LDCT 1(#FF)    AND ZA A15      B MR    ;TEST REG 15 ;.
00B2            T29023:              C ADD ZA A15      B MR ;.
00B3                                 C ADD ZQ          Q MR ;.
00B4                  CJP E2901      C SUB AQ A15        MR ;.
00B5                  RPCT T29023                        MR.
00B6            ;.
00B6                  ;****** TEST IBUS ****** ;.
00B6            ;.
00B6                                   AND ZA A0       B MR    ;A0=0 ;.
00B7                                 C ADD ZQ          Q MR ;.
00B8                                   OR  ZQ A1       B MR    ;A1=1 ;.
00B9                                   ADD AQ A1       Q MR ;.
00BA                                   OR  ZQ A2       B MR    ;A2=2 ;.
00BB                                   ADD AQ A2       Q MR ;.
00BC                                   OR  ZQ A3       B MR    ;A3=4 ;.
00BD                                   ADD AQ A3       Q MR ;.
00BE                                   OR  ZQ A4       B MR    ;A4=8 ;.
00BF                                   ADD AQ A4       Q MR ;.
00C0                                   OR  ZQ A5       B MR    ;A5=#10 ;.
00C1                                   ADD AQ A5       Q MR ;.
00C2                                   OR  ZQ A6       B MR    ;A6=#20 ;.
00C3                                   ADD AQ A6       Q MR ;.
00C4                                   OR  ZQ A7       B MR    ;A7=#40 ;.
00C5                                   ADD AQ A7       Q MR ;.
00C6                                   OR  ZQ A8       B MR    ;A8=#80 ;.
00C7                  CJP EIBUS 2(#00) EXO DA A0         MR    ;ZERO=1 IF OK ;.
00C8                  CJP EIBUS 2(#01) EXO DA A1         MR ;.
00C9                  CJP EIBUS 2(#02) EXO DA A2         MR ;.
00CA                  CJP EIBUS 2(#04) EXO DA A3         MR ;.
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00C5                CJP EIBUS 2(#08) EXO DA A4          MR ;.
00CC                CJP EIBUS 2(#10) EXO DA A5          MR ;.
00CD                CJP EIBUS 2(#20) EXO DA A6          MR ;.
00CE                CJP EIBUS 2(#40) EXO DA A7          MR ;.
00CF                CJP EIBUS 2(#80) EXO DA A8          MR ;.
00D0                                 AND ZA A9        B MR ;.
00D1                                 SUB ZA A9        B MR    ;REG 9=#FF TEST 8 LINES ;.
00D2                CJP EIBUS 2(#FF) EXO DA A9          MR ;.
00D3          ;.
00D3                ;****** TEST ABBUS ****** ;.
00D3          ;.
00D3                                         A0 BA DAL MR    ;RAM DATA TO ABBUS ;.
00D4                CJP EABBUS       EXO DA  A0 BA DAL MR    ;TEST IBUS=ABBUS ? ;.
00D5                                         A1 BA DAL MR    ;TRY ANOTHER BIT PATTERN ;.
00D6                CJP EABBUS       EXO DA  A1 BA DAL MR ;.
00D7                                         A2 BA DAL MR ;.
00D8                CJP EABBUS       EXO DA  A2 BA DAL MR ;.
00D9                                         A3 BA DAL MR ;.
00DA                CJP EABBUS       EXO DA  A3 BA DAL MR ;.
00DB                                         A4 BA DAL MR ;.
00DC                CJP EABBUS       EXO DA  A4 BA DAL MR ;.
00DD                                         A5 BA DAL MR ;.
00DE                CJP EABBUS       EXO DA  A5 BA DAL MR ;.
00DF                                         A6 BA DAL MR ;.
00E0                CJP EABBUS       EXO DA  A6 BA DAL MR ;.
00E1                                         A7 BA DAL MR ;.
00E2                CJP EABBUS       EXO DA  A7 BA DAL MR ;.
00E3                                         A8 BA DAL MR ;.
00E4                CJP EABBUS       EXO DA  A8 BA DAL MR ;.
00E5                                         A9 BA DAL MR ;.
00E6                CJP EABBUS       EXO DA  A9 BA DAL MR ;.
00E7          ;.
00E7                ;****** CLEAR COMMAND REGISTER ****** ;.
00E7          ;.
00E7                                 AND DZ  UNIT       MR    ;UNIT=00000000B ;.
00E8          ;.
00E8                ;****** TEST BUFFER RAM ****** ;.
00E8          ;.
00E8          TRAM:          2(#55)  OR  DZ A14       B MR    ;REG 14 =#55 ;.
00E9                         2(#AA)  OR  DZ A13       B MR    ;REG 13 =#AA ;.
00EA          TRAM3: LDCT    1(#7F)  AND ZA A15       B MR    ;CLEAR ADDRESS POINTER ;.
00EB          TRAM1:                 OR  ZA A15         MR    ;PASS ADDRESS TO ABBUS ;.
00EC                         2(#55)  OR  ZA A15 WRA      MR    ;WRITE ENABLE LOW ;.
00ED                         2(#55)  OR  ZA A15            MR   ;.
00EE                                 OR   ZA A15 UPBY        MR    ;ADDRESS+1 OUT ;.
00EF                         2(#AA)  OR   ZA A15 UPBY WRA     MR    ;WRITE NEXT PATTERN ;.
00F0            RPCT TRAM1   2(#AA) C ADD ZA A15 UPBY BA     MR    ;INCREMENT ADDRESS ;.
00F1          ;.
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00F1                ;****** TEST RAM CONTENS ****** ;.
00F1          ;.
00F1                LDCT    1(#7F)  AND ZA A15       B MR    ;CLEAR POINTER ;.
00F2          TRAM2:                OR  ZA A15 RAM LATCH  MR    ;LATCH LOWER ADDRESS.
00F3                CJP ERAM        EXO DA A14 RAM LATCH MR ;.
00F4                                           RAM        MR ;.
00F5                                OR ZA A15 RAM UPBY LATCH MR ;LATCH UPPER ADDRESS.
00F6                CJP ERAM        EXO DA A13 RAM LATCH MR ;.
00F7                RPCT TRAM2    C ADD ZA A15 NIB     B MR  ;INCREMENT ADDRESS
00F7          ;.
00F8          ;.
00F8                ;****** TEST H/W TIMER (256 MICROSEC ) ****** ;.
00F8          ;.
00F8          TTIMER:                                            ;.
00F8                LDCT    1(#95)  OR DZ COND       Q MR    ;LOAD TIMEOUT COUNTER ;.
00F9                        2(#80)  AND DQ A12       B MR ;.
00FA          TIME1:                  OR  DZ COND      Q MR ;.
00FB                        2(#80)  AND DQ           Q MR    ;TEST TIMER BIT ;.
00FC                CJP TEDGE       EXO AQ A12         MR ;.
00FD                RPCT TIME1                          MR    ;LOOP IN MAX 150 MICROSEC ;.
00FE                 UNC CJP ETIMER                     MR ;.
00FF          ;.
00FF          TEDGE: LDCT    1(#95)  OR  ZQ A12       B MR ;.
0100                                AND ZA A11       B MR    ;CLEAR REG.
0101          TIM2:                 OR DZ COND       Q MR ;.
0102                        2(#80) AND DQ            Q MR ;.
0103                CJP TEDGE1      EXO AQ A12         MR ;.
0104                RPCT TIM2     C ADD ZA A11       B MR ;REG11=REG11+1.
0105                UNC CJP ETIMER                     MR ;.
0106          ;.
0106          TEDGE1:               OR  ZQ A12       B MR    ;UPDATE REG 12 ;.
0107                        2(#57) C SUS DA A11       Q MR ;.
0108             CJP TEDGE3 2(#80)  AND DQ             MR ;.
0109             UNC CJP ETIMER                        MR.
010A          TEDGE3:       2(#87) C SUB DA A11         MR    ;TEST LOWER AND UPPER LIMIT ;.
010B             CJP TIM3A  2(#80)  AND DQ             MR    ;JUMP IF GRETHER THAN UPPER ;.
010C             UNC CJP ETIMER                        MR.
010D          ;.
010D          TIM3A: LDCT    1(#95)  AND DZ A11       B MR    ;CLEAR TIMER ;.
010E          TIM3:                 OR  DZ COND      Q MR ;.
010F                        2(#80)  AND DQ           Q MR ;.
0110                CJP TEDGE2      EXO AQ A12         MR ;.
0111                RPCT TIM3     C ADD ZA A11       B MR    ;INCREMENT TIMER REG.
0112                UNC CJP ETIMER                     MR ;.
0113          ;.
0113          TEDGE2:               OR  ZQ A12       B MR    ;UPDATE R12 ;.
0114                        2(#57) C SUS DA A11       Q MR    ;#57 = LOWER LIMIT ;.
0115             CJP TEDGE4 2(#80)  AND DQ             MR    ;TEST SIGNBIT ;.
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011b            UNC CJP ETIMER                          MR.
0117         TEDGE4:        2(#87) C SUB DA A11      Q MR    ;#87 = UPPER LIMIT ;.
0118            CJP TARSTO 2(#80)   AND DQ            MR    ;JUMP TO ERROR IF NOT OVERFLOW ;.
0119            UNC CJP ETIMER                        MR.
011A          ;.
011A          ;.
011A                ;****** TEST 1791 ******* ;.
011A                ;TEST AUTO RESTORE FACILITIES OF 1791 ;.
011A          ;.
011A         TARSTO:                AND ZA A7        B MR    ;CLEAR INTERRUPT STATE REG ;.
011B                                AND ZA A8        B MR    ;CLEAR PORTSAVE AREA ;.
011C                                AND ZA A9        B MR    ;CLEAR COUNT REG ;.
011D                                AND ZA A10       B MR    ;CLEAR STPU STATE REG ;.
011E                                AND ZA A11       B MR    ;CLEAR TIMER PERIOD REG.
011F                                AND ZA A12       B MR    ;CLEAR TIMER NUMBER REG ;.
0120                                AND ZA A14       B MR    ;CLEAR TIMER COUNTER.
0121                LOCT   1(#28)   AND ZA A13       B MR    ;.
0122                RPCT LOC                                 ;.
0123                                         RIC STCM        ;.
0124            UNC  CJS W1STPU              RIC STCM        ;DUMMY READ STATUS (CLEAR INTRQ) WAIT
0125         STPU2: LOCT   1(#10)   OR  ZQ A10       B       ;.
0126                RPCT LOC           STBY                  ;WAIT 1 STEPPULS TIME.
0127         ROCOND:                OR  OZ A8 COND     B    ;SAVE PORT PICTURE I R8 ;.
0128                        2(#40)  AND DA A8        Q       ;TEST STPU BIT ;.
0129             CJP PSSTPU         IAN AQ A10               ;JUMP IF POS EDGE ;.
012A                                OR  ZQ A10        B              ;UPDATE STPU STATE REG ;.
012B          ;.
012B         TIMTST:        2(#80)  AND DA A8        Q       ;TEST TIMER BIT ;.
012C             CJP PSTIM          IAN AQ A13               ;JUMP IF POS EDGE ;.
012D                                OR  ZQ A13        B              ;UPDATE STATE REG ;.
012E          ;.
012E         INTTST:        2(#02)  AND DA A8        Q       ;TEST INTRQ BIT ;.
012F             CJP PSINT          IAN AQ A7 ;.
0130          UNC CJP ROCOND        OR  ZQ A7        B       ;UPDATE INT STATE REG ;.
0131          ;.
0131         PSINT: UNC CJP E1791 ;.
0132          ;.
0132         PSSTPU: LOCT   1(#10) ;.
0133                 RPCT LOC ;.
0134                                OR  ZQ A10 STBY  B       ;WAIT 4 MICROSEC (TSTPU) ;.
0135                        2(#35) C BUS DA A14      Q ;.
0136             CJP ULTST 2(#80)   AND DQ                   ;TEST SIGNBIT ;.
0137             UNC CJP E1791.
0138         ULTST:         2(#40) C SUB DA A14      Q       ;TEST UPPER LIMIT ;.
0139             CJP PSTP1 2(#80)   AND DQ ;.
013A             UNC CJP E1791.
013B         PSTP1:                 AND ZA A14        B ;.
013C                              C ADD ZA A9         B       ;INCREMENT STPU COUNTER ;.
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013D            CJP TIMTST 2(#FE) C SUB DA A9 ;.
013E            CJP E1791  2(#3A) C SUB DA A12                ;TEST TIMER MS-BYTE ;.
013F            UNC CJP INTRQ ;.
0140          ;.
0140        PSTIM:                  OR  ZQ A13        B       ;UPDATE TIMER STATE REG ;.
0141                              C ADD ZA A14        B       ;INCREMENT PERIOD CNT ;.
0142                              C ADD ZA A11        B       ;INCREMENT LS-TIMER CNT ;.
0143            CJP INTTST 2(#FF) C SUB DA A11                ;TEST LOWER TIMER BYTE ;.
0144                              C ADD ZA A12        B ;.
0145            CJP INTTST 2(#3B) C SUB DA A12                ;TEST UPPER TIMER BYTE ;.
0146            CJP E1791  2(#FE) C SUB DA A9                 ;TEST STPU CNT ;.
0147        INTRQ:                  AND ZA A6         B       ;CLEAR LOOP COUNTER.
0148        INTWT: LOCT 1(#138)   C ADD ZA A6         B       ;INCREMENT LOOP COUNTER.
0149               RPCT LOC         OR  DA A8 COND    B       ;READ INPUT REGISTER.
014A            CJP INTOK  2(#02)   AND DA A8                 ;TEST INTRQ FROM 1791 ;.
014B               CJP INTWT        OR  ZA A6                 ;LOOP UNTILL R6=00.
014C            UNC CJP E1791                                     ;.
014D        INTOK:                              RIC STCM ;.
014E                                OR  DZ      RIC STCM      ;READ STATUS FROM 1791 ;.
014F            CJP TTKSD  2(#10)   AND DQ            Q       ;TEST SEEK ERROR BIT ;.
0150            UNC CJP E1791                                           ;.
0151          ;.
0151               ;****** TEST TRACK - SECTOR - DATA REGISTERS ****** ;.
0151        TTKSD:
0151                                AND ZA A0         B       ;CLEAR COUNT REG.
0152        TKLOOP:                             WIC TRK ;.
0153                                            WIC TRK ;.
0154                                OR  ZA A0 WIC TRK         ;WRITE <A0> TO TRACK REG ;.
0155                LOCT 1(#28)     OR  ZA A0     TRK.
0156                RPCT LOC                                  ;WAIT 10 MICROSEC.
0157                                            RIC TRK ;.
0158                                            RIC TRK ;.
0159            CJP E1791           EXD DA A0 RIC TRK DAL     ;READ BACK AND COMPARE ;.
015A                              C ADD ZA A0 NIB TRK B       ;NEXT TRACK COMBINATION ;.
015B            CJP TKLOOP          OR  ZA A0                 ;LOOP UNTILL R0=0.
015C        SCLOOP:                             WIC SCT ;.
015D                                            WIC SCT ;.
015E                                OR  ZA A0 WIC SCT         ;WRITE <A0> TO SECTOR REG ;.
015F                LOCT 1(#28)     OR  ZA A0     SCT.
0160                RPCT LOC                                  ;WAIT 10 MICROSEC.
0161                                            RIC SCT ;.
0162                                            RIC SCT ;.
0163            CJP E1791           EXD DA A0 RIC SCT DAL     ;READ BACK AND COMPARE ;.
0164                              C ADD ZA A0 NIB SCT B       ;NEXT SECTOR COMBINATION ;.
0165            CJP SCLOOP          OR  ZA A0                 ;LOOP UNTILL R0=00.
0166        DTLOOP:                             WIC DAT ;.
0167                                            WIC DAT ;.
0168                                OR  ZA A0 WIC DAT         ;WRITE <A0> TO DATA REG ;.
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0169                LDCT 1(#28)     OR  ZA A0      DAT.
016A                RPCT LOC                                   ;WAIT 10 MICROSEC.
016B                                          RIC DAT ;.
016C                                          RIC DAT ;.
016D          CJP E1791             EXO DA A0 RIC DAT DAL      ;READ BACK AND COMPARE ;.
016E                              C ADD ZA A0 NIB DAT B        ;NEXT DATA COMBINATION ;.
016F          CJP DTLOOP            OR  ZA A0                  ;LOOP UNTILL RQ=00.
0170        ;.
0170              ;****** TEST HEAD LOAD TIMER FUNCTION ****** ;.
0170        ;.
0170                                          WIC TRK.
0171                      2(#4C)  OR  DZ      WIC TRK.
0172                      2(#4C)  OR  DZ          TRK.
0173                      2(#70)  OR  DZ      WIC STCM       ;ONE STEPOUT CMD ;.
0174          LDCT 1(#70) 2(#70)  OR  DZ      WIC STCM       ;"H","U","V" SET ;.
0175          RPCT LOC    2(#70)  OR  DZ          STCM       ;WAIT 28 MICROSEC.
0176                      2(#40)  OR  DZ      UNIT           ;SET HLT ;.
0177          UNC CJS W1STPU      AND ZA A10        B        ;WAIT UNTILL 1ST STPU.
0178          LDCT        1(#10) ;.
0179          RPCT LOC                                         ;WAIT 4 MICROSEC ;.
017A                                          RIC STCM STBY ;CLEAR STPU LATCH ;.
017B                                          RIC STCM ;.
017C                              OR DZ       RIC STCM DAL Q ;READ STATUS ;.
017D                                          NIB STCM ;.
017E          CJP RDTRK  2(#20)   AND DQ      RIC TRK        ;TEST HLD*HLT ;.
017F          UNC CJP E1791                                    ;ERRQR EXIT IF NOT TRUE.
0180        RDTRK:                             RIC TRK ;.
0181                              OR DZ       RIC TRK DAL Q ;READ TRACK REG ;.
0182          CJP E1791  2(#48)   EXO DQ      NIB TRK        ;TEST AUTO DCR OF TRACK REG ;.
0183                                          WIC STCM ;.
0184                                          WIC STCM ;.
0185                      2(#D0)  OR  DZ      WIC STCM       ;SEND FORCE INTERRUPT ;.
0186          LDCT 1(#70) 2(#D0)  OR  DZ          STCM.
0187          RPCT LOC                                         ;WAIT 28 MICROSEC ;.
0188                                          RIC STCM ;.
0189                                          RIC STCM ;.
018A                              OR  DZ      RIC STCM DAL Q ;READ STATUS FROM 1791 ;.
018B                                          NIB STCM ;.
018C          CJP E1791  2(#01)   AND DQ                       ;TEST BUSY CLEARING ;.
018D        ;.
018D        ;.
018D              ;****** CLEAR RAM ****** ;.
018D        ;.
018D          LDCT       1(#7F)   AND ZA A15        B ;.
018E        RAMCL:                OR  ZA A15                 ;ADDRESS OUT ;.
018F                     2(#00)   OR  ZA A15 WRA            ;WRITE ZERO TO RAM ;.
0190                     2(#00)   OR  ZA A15.
0191                              OR  ZA A15 UPBY.
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0192                    2(#00)    OR  ZA A15 UPBY WRA      ;CLEAR UPPER BYTE.
0193          RPCT RAMCL 2(#00) C ADD ZA A15 UPBY  BA      ;INCREMENT ADDRESS ;.
0194        ;.
0194             ;******   END OF BUILD IN TEST (BIT)   ****** ;.
0194        ;.
0194        ;.
0194        ;.
0194        ;.
0194        ;.
0194        ;.
0194                         AND DZ A12          B  STBY ;.
0195                         2(1) OR DZ A15      B              ;PRESET ARQ BITMASK ;.
0196                         2(#80) OR DZ A7     B            ;   ;.
0197                         2(#40) OR DZ A5     B WIC        ;   ;.
0198                         2(#00) OR DZ        WIC          ;   ;.
0199                         2(#00) OR DZ                     ;   ;.
019A          UNC PCLC 1(34) AND DZ A8           B            ;   ;.
019B              RFCT       AND ZA A11          B            ;   ;.
019C                         2(#F0) OR DZ A4     B            ;   ;.
0190          UNC CJS GETSTA 2(128) OR DZ A0     B            ; HEAD POS UNKNOWN   ;.
019E              CJP LOCM1  2(1) AND DQ                      ;   ;.
019F                         2(128) OR DZ A1     B            ; HEAD POS UNKNOWN   ;.
01A0                         2(128) OR DZ A2     B            ; HEAD POS UNKNOWN   ;.
01A1                         2(128) OR DZ A3     B            ; HEAD POS UNKNOWN   ;.
01A2                         2(#7F) AND DA A7    B            ;   ;.
01A3                         AND DZ A5           B CLBY       ;   SEND BIT END INTERRUPT.
01A4
01A4             ;********    READY TO PERFORM COMMANDS   **********.
01A4
01A4        NODEC: ;.
01A4              CJS SVMBO  COND AND DA A15                  ;   ;.
01A5              LOCT 1(77)                                  ;   ;.
01A6              CJS SVMBO  COND AND DA A15                  ;   ;.
01A7              RPCT LOCM1 COND EXO DA A10     Q            ;   ;.
01A8              CJP NODEC  2(#80) AND DQ                    ; TEST TIMER   ;.
01A9                         2(#80) EXO DA A10   B            ; CHANGE OLD TIMER   ;.
01AA              CJS SVMBO  COND AND DA A15                  ;   ;.
01AB              CJP NODEC  SUB ZA A9           B            ; DECR LOWER TIMER   ;.
01AC                         SUB ZA A10          B            ; DECR UPPER TIMER   ;.
01AD              CJP NODES  2(#7F) AND DA A10                ; UPPER = 0?   ;.
01AE              CJS SVMBO  COND AND DA A15                  ;   ;.
01AF                         2(#9F) AND DA A11   B            ;   ;.
0180                         AND DZ              UNIT         ;   ;.
0181        NODES: ;.
0181              CJS SVMBO  COND AND DA A15                  ;   ;.
0182                         RDY OR DZ           Q            ;   ;.
0183                         2(#F0) OR DQ A14    B            ; STORE NEW RDY3:0   ;.
0184              CJS SVMBO  COND AND DA A15                  ;   ;.
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                CJP CHINT     IAN AQ A4              Q          ; DISK CHANGE ?   ;.
0185
0186        STNEW: ;.
                              A14 OR ZA              Q          ; NEW   ;.
0186                          OR ZQ A4               B          ; OLD:=NEW   ;.
0187
0188            CJS SVMBO     COND AND DA A15                   ;   ;.
0189                                                            ;   ;.
0189      UNC CJP NODEC
018A
018A        CHINT: ;.
018A            CJS SVMBO     COND AND DA A15                   ;   ;.
018B                          2(#80) OR DA A7        B          ;   ;.
018C      UNC CJP STNEW       OR AQ A5               B CLBY     ; DISK CHANGE INTERRUPT   ;.
018D
018D        START: ;.
018D                          RU OR DZ A14           B DL STBY  ;   ;.
018E                          2(#40) OR DA A5        B          ;   ;.
018F                          2(#E) AND DA A5        Q          ;   ;.
01C0            CJS SVMB3     COND AND DA A15                   ;   ;.
01C1                          ADD ZQ A10             B          ;   ;.
01C2      UNC CJS DGTSTA      2(#80) OR DA A7        B          ;   ;.
01C3
01C3            CJS SVMB3     COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
01C4            CJP NOTO      2(3) AND DA A14                   ;   ;.
01C5                          AQ OR ZA               Q          ;   ;.
01C6      UNC CJP LDNEU       2(1) OR DZ A9          B          ; DECODED NEW UNIT   ;.
01C7
01C7        NOTO: ;.
01C7            CJS SVMB3     COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
01C8            CJP UN2OR3    2(2) AND DA A14                   ;   ;.
01C9                          A1 OR ZA               Q          ;   ;.
01CA      UNC CJP LDNEU       2(2) OR DZ A9          B          ;   ;.
01CB
01CB        UN2OR3: ;.
01CB            CJS SVMB3     COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
01CC            CJP UN3       2(1) AND DA A14                   ;   ;.
01CD                          A2 OR ZA               Q          ;   ;.
01CE      UNC CJP LDNEU       2(8) OR DZ A9          B          ;   ;.
01CF
01CF        UN3: ;.
01CF                          A3 OR ZA               Q          ;   ;.
01D0      UNC CJP LDNEU       2(16) OR DZ A9         B          ;   ;.
01D1
01D1        LDNEU: ;.
01D1            CJS SVMB3     COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
01D2                                                 TRK WIC    ;   ;.
01D3                          OR ZQ                     TRK WIC ;   ;.
01D4                          OR ZQ                  TRK        ;   ;.
01D5            CJS SVMB3     COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
01D6                          2(#80) AND DQ A13      B          ; R13 NOT ZERO MEANS
01D6                                                              TRK UNDEFINED   ;.
01D7                          A9 OR ZA               Q          ;   ;.
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01D8                CJS SVMB3    COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
01D9                CJP SAMEUN   A11 AND AQ                       ;   ;.
01DA                             OR ZQ A11          B             ; NEW UNIT   ;.
01DB          SAMEUN: ;.
01DB                             OR ZA A13          Q             ;SAVE R13 IN Q REG.
01DC                CJS SVMB3    COND AND DA A15                  ; REQUEST FROM MAINBUS.
01DD                             OR ZQ A9           B             ;UNDEF TO R9.
01DE                CJP ILLCOM   2(#80) AND DA A14                ;NO DOUBLLE DENS IN THIS FIRMWA
01DF                             2(#84) AND DA A14  Q             ; DENS/SIDE   ;.
01E0                CJS SVMB3    COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
01E1                             2(128) EXO DQ      Q             ; /DENS/SIDE   ;.
01E2                             2(#78) AND DA A11  B             ;   ;.
01E3                             A11 OR AQ          B             ; SET DENS/SIDE I REG11   ;.
01E4                CJS SVMB3    COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
01E5           ;.
01E5                CJP NSELEC   2(#78) AND DA A14                ;   ;.
01E6           ;.
01E6          ;OPERATION "SELECT"   ;.
01E6           ;.
01E6                             2(#F8) AND DA A11  UNIT          ;   ;.
01E7                CJS SVMB3    COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
01E8                                                STCM WIC      ;   ;.
01E9                             2(#00) OR DZ       STCM WIC      ;   ;.
01EA             UNC PCLC 1(16)  2(#00) OR DZ       STCM          ;   ;.
01EB                CJS SVMB3    COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
01EC                RFCT                                          ; DELAY FROM LOAD COMMAND
01EC                                                               TO READ STATUS   ;.
01ED             UNC CJS GETSTA                     ;   ;.
01EE                CJS AUTO6    2(1) AND DQ                      ;   ;.
01EF                CJS AUTO11   2(#80) AND DQ                    ;   ;.
01F0                CJS SVMB3    COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
01F1                CJS AUTO8    2(#40) AND DQ                    ;   ;.
01F2                             2(#4F) AND DA A5   B             ;   ;.
01F3                             COND OR DZ         Q             ;   ;.
01F4                CJS SVMB3    COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
01F5                CJS ADDI7    2(#10) AND DQ                    ;   ;.
01F6             UNC CJP COMSLT                                   ;   ;.
01F7           ;.
01F7          NSELEC: ;.
01F7             UNC CJS CHKRDY                                   ;   ;.
01F8             UNC CJS CHKWAS  A10 IAN AQ         Q             ;   ;.
01F9                CJS SVMB3    COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
01FA                CJP REAWRI   2(#18) AND DA A14                ;   ;.
01FB                CJP RESTOR   2(#53 AND DA A14                 ;   ;.
01FC                CJS SVMB3    COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
01FD           ;.
01FD          ; OPERATION "SEEK"   ;.
01FD           ;.
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01FD            CJP SEER      2(128) AND DA A6                  ;   ;.
01FE                          2(#33) ADD DA A6     Q            ;   ;.
01FF            CJS SVMB3     COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
0200            CJP SEER      2(128) AND DQ                     ;   ;.
0201            CJS EXECRS    A9 ADD ZA                         ; EXECUTE A RESTORE,
0201                                                              IF TRACK IS UNDEFINED   ;.
0202       UNC CJS TRKDIF     2(#FB) AND DA A11    UNIT         ;   ;.
0203     NOLOAD: ;.
0203            CJS SVMB3     COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
0204                          COND OR DZ A13       B            ;8047D MOD  ;.
0205            CJP TP850U    2(8) AND DA A13                   ;                  *******  ;.
0206                          2(5)  ADD DQ         Q            ;                  *******  ;.
0207     TESTUN: ;.
0207            CJP UNLOAD    2(#80) AND DQ                     ;   ;.
0208     TESTSI: ;.
0208            CJS SVMB3     COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
0209                          COND OR DZ A13 B                  ;8047D MOD  ;.
020A            CJP TWOSI     2(#10) AND DA A13                 ;   ;.
020B            CJP INVSI     2(4) AND DA A11                   ;   ;.
020C     TWOSI: ;.
020C       UNC CJP LDNWTK     A11 OR ZA            UNIT         ;   ;.
020D     TP850U:                                                ;                  *******  ;.
020D       UNC CJP TESTUN     2(16) ADD DQ         Q            ;                 *********  ;.
020E     UNLOAD: ;.
020E            CJS SVMB3     COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
020F       UNC CJP TESTSI     2(#9F) AND DA A11    B            ;   ;.
0210      ;.
0210     LDNWTK: ;.
0210            CJS SVMB3     COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
0211                                               DAT WIC      ;   ;.
0212                          A6 OR ZA             DAT WIC      ;   ;.
0213                          A6 OR ZA             DAT          ;   ;.
0214            CJS SVMB3     COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
0215       UNC CJS WASIDE                                        ;   ;.
0216            CJS SVMB3     COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
0217                          COND OR DZ A13 B                  ;8047D MOD  ;.
0218            CJP TP850S    2(8) AND DA A13      STCM WIC     ;   ;.
0219                          2(#1E) OR DZ         STCM WIC     ;                  *******  ;.
021A       UNC CJP SECMLD     2(#1E) OR DZ         STCM         ;   ;.
021B     TP850S:                                                ;                  *******  ;.
021B                          2(#1C) OR DZ         STCM WIC     ;   ;.
021C                          2(#1C) OR DZ         STCM         ;                  *******  ;.
021D     SECMLD: ;.
021D            CJS SVMB3     COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
021E            CJP HLDON     2(#20) AND DA A11                 ;   ;.
021F            LOCT 1(100)                                     ;   ;.
0220     WAHOLD: ;.
0220            CJS SVMB3     COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
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0221                          COND OR DZ          Q          ;   ;.
0222                CJP STEPPU  2(#40) AND DQ                ;   ;.
0223                CJP SEEKOV  2(2) AND DQ                  ;   ;.
0224                CJS SVMB3   COND AND DA A15              ; REQUEST FROM MAINBUS ?   ;.
0225                            A10 EXN AQ          Q        ;   ;.
0226                CJP WAHOLD  2(#80) AND DQ                ;   ;.
0227                RPCT WAHOLD 2(#80) EXO DA A10   B        ;   ;.
0228                CJS SVMB3   COND AND DA A15              ; REQUEST FROM MAINBUS ?   ;.
0229                            2(#34) AND DA A7    B        ;   ;.
022A                            2(#C0) OR DA A7     B        ;   ;.
022B            UNC CJP ABEND   AND DZ A3           B        ;   ;.
022C                CJS SVMB3   COND AND DA A15              ; REQUEST FROM MAINBUS ?   ;.
022D          ;.
022D         STEPPU: ;.
022D            UNC CJS TRKDIF                               ;   ;.
022E                CJS SVMB3   COND AND DA A15              ;   ;.
022F                            A11 OR ZA           UNIT     ;   ;.
0230            UNC CJS CHKRDY                               ;   ;.
0231            UNC CJS UPDCHG                               ;   ;.
0232                CJS SVMB3   COND AND DA A15              ;   ;.
0233            UNC CJP SECMLD                               ;   ;.
0234          ;.
0234         HLDON: ;.
0234            UNC CJS DELHLT                               ;   ;.
0235         SEEKOV: ;.
0235            UNC CJS GETSTA                               ;   ;.
0236                            2(#4F) AND DA A5    B        ;   ;.
0237                CJS AUTO6   2(1) AND DQ                  ;   ;.
0238                CJS SVMB3   COND AND DA A15              ; REQUEST FROM MAINBUS ?   ;.
0239                CJS AUTO1   2(8) AND DQ                  ;   ;.
023A                CJS AUTO12  2(#10) AND DQ                ;   ;.
023B                CJS AUTO11  2(#30) AND DQ                ;   ;.
023C                CJS SVMB3   COND AND DA A15              ; REQUEST FROM MAINBUS ?   ;.
023D                            2(1) OR DA A7       B        ;   ;.
023E                CJS SENOCP  2(#42) AND DA A7             ;   ;.
023F                CJS SENOCP  2(#18) AND DA A8             ;   ;.
0240                CJS SVMB3   COND AND DA A15              ; REQUEST FROM MAINBUS ?   ;.
0241            UNC CJP COMSLT                               ;   ;.
0242          ;.
0242          ; OPERATION " RESTORE"   ;.
0242         RESTOR: ;.
0242                CJS SVMB3   COND AND DA A15              ; REQUEST FROM MAINBUS ?   ;.
0243                CJP ILLCOM  2(#38) AND DA A14            ;   ;.
0244            UNC CJS EXECRS                               ;   ;.
0245            UNC CJP COMSLT                               ;   ;.
0246          ;.
0246          ; OPERATION "READ" OR "WRITE"   ;.
0246         READWRI: ;.
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0246            CJS CHKREA   2(#50) AND DA A14                 ;   ;.
0247            CJS SVMB4    COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
0248                         2(#F8) AND DA A11   UNIT SCT WIC  ;   ;.
0249                         A6 OR ZA            SCT WIC       ;   ;.
024A                         A6 OR ZA            SCT           ;   ;.
024B            CJS SVMB4    COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
024C                         COND OR DZ          Q             ;   ;.
024D            CJP TWOSRW   2(#10) AND DQ                     ;   ;.
024E            CJP INVSRW   2(4) AND DA A11                   ;   ;.
024F      TWOSRW: ;.
024F            CJS SVMB4    COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
0250        UNC CJS WASIDE   A11 OR DA 2(#20)    B UNIT        ;   ;.
0251            CJS SVMB4    COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
0252                         2(#80) OR DZ        Q             ;   ;.
0253            CJP RWCM     2(#10) AND DA A14                 ;   ;.
0254                         2(#21) OR DQ        Q             ;   ;.
0255            CJS SVMB4    COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
0256            CJP RWCM     2(#20) AND DA A14                 ;   ;.
0257                         2(#FE) AND DQ       Q             ;   ;.
0258      RWCM: ;.
0258            CJS SVMB4    COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
0259                         AND DZ A12          B STCM WIC    ;   ;.
025A                         OR ZQ               STCM WIC      ;   ;.
025B                         OR ZQ               STCM          ;   ;.
025C            CJS SVMB4    COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
025D        UNC CJS WRIUPP   2(1) OR DZ A9       B             ;   ;.
025E      RWCMLD: ;.
025E            CJS SVMB4    COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
025F            LDCT 1(275)                                    ;   ;.
0260      WAITIN: ;.
0260                         COND OR DZ          Q             ;   ;.
0261            CJS SVMB4    COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
0262            CJS DRQSRV   2(4) AND DQ                       ;   ;.
0263            CJS SVMB4    COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
0264            CJP RWOVER   2(2) AND DQ                       ;   ;.
0265                         A10 EXN AQ          Q             ;   ;.
0266            CJS SVMB4    COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
0267            CJP WAITIN   2(#80) AND DQ                     ;   ;.
0268            RPCT WAITIN  2(#80) EXO DA A10   B             ;   ;.
0269      ;.
0269            LDCT INVSRW  COND OR DZ          Q             ;   ;.
026A      ;.
026A            CJS SVMB4    COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
026B            CJS DRQSRV   2(4) AND DQ                       ;   ;.
026C            CJS SVMB4    COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
026D        UNC CJS UPDCHG   2(#40) OR DA A11    B UNIT        ;   ;.
026E            CJS SVMB4    COND AND DA A15                   ; REQUEST FROM MAINBUS ?   ;.
026F                         COND OR DZ          Q             ;   ;.
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0270                CJS DRQSRV    2(4) AND DQ                        ;   ;.
0271                CJS SVMB4     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
0272            UNC CJS CHKRDY    2(#7F) AND DA A10    B             ;   ;.
0273                JRP  RWCMLD   A10 SUB ZA           B             ;   ;.
0274             ;.
0274          RWOVER: ;.
0274            UNC CJS GETSTA    AND DZ A12           B             ;   ;.
0275                CJS AUTD6     2(1) AND DQ                        ;   ;.
0276                CJS AUTD11    2(#80) AND DQ                      ;   ;.
0277                CJS SVMB4     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
0278                CJS AUTD8     2(#40) AND DQ                      ;   ;.
0279                CJS AUTD5     2(#10) AND DQ                      ;   ;.
027A                CJS SVMB4     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
027B                CJS CRCERR    2(8) AND DQ                        ;   ;.
027C                              2(#4F) AND DA A5     B             ;   ;.
027D                CJS ADDI4     2(#20) AND DQ                      ;   ;.
027E                CJS SVMB4     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
027F                CJS ADDI5     2(4) AND DQ                        ;   ;.
0280            UNC CJP COMSLT                                       ;   ;.
0281             ;.
0281          SEER: ;.
0281                              2(#84) AND DA A7     B             ;   ;.
0282                              2(#10) OR DZ A8      B             ;   ;.
0283                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
0284            UNC CJP COMSLT    2(#4F) AND DA A5     B             ;   ;.
0285             ;.
0285          INVSI: ;.
0285                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
0286                              2(#84) AND DA A7     B             ;   ;.
0287                              2(#10) OR DZ A8      B             ;   ;.
0288          ABEND: ;.
0288                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
0289            UNC CJS CHKRDY    2(#4F) AND DA A5     B             ;   ;.
028A          ABP2: ;.
028A                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
028B                                                   WIC           ;   ;.
028C                              2(#00) OR DZ         WIC           ;   ;.
028D            UNC CJS DGTSTA    2(#00) OR DZ                       ;   ;.
028E                CJP LOCM1     2(1) AND DQ                        ;   ;.
028F            UNC CJP COMSLT                                       ;   ;.
0290          INVSRW: ;.
0290                CJS SVMB4     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
0291                              2(#80) AND DA A8     B       ;CLEAR AUTO STATUS EXCEPT PE ;.
0292                              2(#84) AND DA A7     B             ;   ;.
0293            UNC CJP ABEND     2(#20) OR DZ A7      B             ;   ;.
0294             ;.
0294             ;.
0294          ILLCOM: ;.
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0294                            2(#80) AND DA A8     B      ;CLEAR AUTO STATUS EXCEPT PE  ;.
0295                            2(#84) AND DA A7     B              ;   ;.
0296                 CJS SVMB3  COND AND DA A15                     ; REQUEST FROM MAINBUS ?   ;.
0297                            2(4) OR DZ A7        B              ;   ;.
0298                            2(#4F) AND DA A5     B              ;   ;.
0299          ;.
0299        COMSLT: ;.
0299                 CJS SVMB3  COND AND DA A15                     ; REQUEST FROM MAINBUS ?   ;.
029A                            TRK RIC                            ;   ;.
029B                            TRK RIC                            ;   ;.
029C                            TRK RIC DAL OR DZ    Q             ;   ;.
029D                 CJS SVMB3  TRK COND AND DA A15                 ;   ;.
029E                 CJP SAUN0  2(1) AND DA A11                     ;   ;.
029F                 CJP SAUN1  2(2) AND DA A11                     ;   ;.
02A0                 CJS SVMB3  COND AND DA A15                     ; REQUEST FROM MAINBUS ?   ;.
02A1                 CJP SAUN2  2(8) AND DA A11                     ;   ;.
02A2                 CJP SAUN3  2(16) AND DA A11                    ;   ;.
02A3          ;.
02A3        FENEU: ;.
02A3                 CJS SVMB3  COND AND DA A15                     ; REQUEST FROM MAINBUS ?   ;.
02A4                 CJP ADDNZ  2(#BF) AND DA A5     B   CLBY       ;   ;.
02A5                            2(#7F) AND DA A7     B              ;   ;.
02A6        ADDNZ: ;.
02A6           UNC ENLD                                            ;   ;.
02A7                 CJS SVMB3  COND AND DA A15                     ; REQUEST FROM MAINBUS ?   ;.
02A8           UNC ENLD                                            ;   ;.
02A9           UNC ENLD                                            ;   ;.
02AA           UNC ENLD         2(15) OR DZ A10     B              ;   ;.
02AB                 CJS SVMB0  COND AND DA A15                     ;   ;.
02AC           UNC CJP NODEC    AND DZ A9           B              ;   ;.
02AD          ;.
02AD        SAUN0: ;.
02AD           UNC CJP FENEU    OR ZQ A0            B              ;   ;.
02AE        SAUN1: ;.
02AE           UNC CJP FENEU    OR ZQ A1            B              ;   ;.
02AF        SAUN2: ;.
02AF           UNC CJP FENEU    OR ZQ A2            B              ;   ;.
02B0        SAUN3: ;.
02B0           UNC CJP FENEU    OR ZQ A3            B              ;   ;.
02B1          ;.
02B1        ;*************************************************<   ;.
02B1          ;.
02B1          ;.
02B1        DGTSTA: ;.
02B1                 CJS SVMB3  COND AND DA A15                     ; REQUEST FROM MAINBUS ?   ;.
02B2                            RIC                                ;   ;.
02B3                            RIC                                ;   ;.
02B4                            RIC DAL OR DZ        Q             ;   ;.
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0285                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
0286             UNC CRET                                            ;   ;.
0287           ;.
0287           ; SUBROUTINE "GETSTATUS"   ;.
0287           GETSTA: ;.
0287                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
0288                              2(#84) AND DA A7     B STCM RIC    ;   ;.
0289                              AND DZ A8            B STCM RIC    ;   ;.
028A                              DAL OR DZ            Q STCM RIC ;   ;.
028B                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
028C             UNC CRET                                            ;   ;.
028D           ;.
028D           ; SUBROUTINE "EXECUTE A RESTORE OPERATION"   ;.
028D           EXECRS:                                               ;   ;.
028D             UNC CJS UPDCHG   2(#98) AND DA A11    B UNIT        ;   ;.
028E                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
028F             UNC CJS WASIDE                                      ;   ;.
02C0                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
02C1                              COND OR DZ A13       B             ;   ;.
02C2                CJP TP35OR    2(8) AND DA A13      STCM WIC      ;                  *******  ;.
02C3                              2(#E) OR DZ          STCM WIC      ;   ;.
02C4             UNC CJP RSCMLD   2(#E) OR DZ          STCM          ;   ;.
02C5           TP35OR:                                               ;                  *******  ;.
02C5                              2(#C) OR DZ          STCM WIC      ;   ;.
02C6                              2(#C) OR DZ          STCM          ;   ;.
02C7           RSCMLD: ;.
02C7                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
02C8                LOCT 1(100)                                      ;   ;.
02C9           WANOST: ;.
02C9                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
02CA                              COND OR DZ           Q             ;   ;.
02CB                CJP STEPRS    2(#40) AND DQ                      ;   ;.
02CC                CJP RESTOV    2(2) AND DQ                        ;   ;.
02CD                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
02CE                              A10 EXN AQ           Q             ;   ;.
02CF             CJP WANOST       2(#80) AND DQ                      ;   ;.
02D0                RPCT WANOST   2(#80) EXO DA A10    B             ;   ;.
02D1                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
02D2                              2(#20) OR DA A11     B UNIT        ;   ;.
02D3             UNC CJS DELHLT                                      ;   ;.
02D4           RESTOV: ;.
02D4             UNC CJS GETSTA                                      ;   ;.
02D5                              2(#4F) AND DA A5     B             ;   ;.
02D6                CJS AUTO6     2(1) AND DQ                        ;   ;.
02D7                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
02D8                CJS AUTO1     2(8) AND DQ                        ;   ;.
02D9                CJS AUTO11    2(#80) AND DQ                      ;   ;.
02DA                CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ?   ;.
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02D6                CJS RESTER    2(#10) AND DQ                    ;   ;.
02DC                CJPP COMSLT   2(#78) AND DA A7                 ;   ;.
02DD                CJPP COMSLT   A8 ADD ZA                        ;   ;.
02DE                CJS SVMB3     COND AND DA A15                  ;   ;.
02DF             UNC CRET                                          ;   ;.
02E0           ;.
02E0          STEPRS: ;.
02E0                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
02E1             UNC CJS CHKRDY                                    ;   ;.
02E2             UNC CJS UPDCHG                                    ;   ;.
02E3                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
02E4             UNC CJP RSCMLD                                    ;   ;.
02E5           ;.
02E5           ;.
02E5          ; SUBROUTINES FOR SETTING STATUSBITS   ;.
02E5          SENOCP: ;.
02E5                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
02E6             UNC CRET         2(#FE) AND DA A7     B           ;   ;.
02E7          AUTO1: ;.
02E7                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
02E8             UNC CRET         2(2) OR DA A7        B           ;   ;.
02E9          CRCERR: ;.
02E9                CJP AUTO1     2(#10) AND DQ                    ;   ;.
02EA                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
02EB             UNC CRET         2(#10) OR DA A7      B           ;   ;.
02EC          AUTO5: ;.
02EC                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
02ED             UNC CRET         2(#20) OR DA A7      B           ;   ;.
02EE          AUTO6: ;.
02EE                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
02EF             UNC CRET         2(#40) OR DA A7      B           ;   ;.
02F0          AUTO8: ;.
02F0                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
02F1             UNC CRET         2(1) OR DA A8        B           ;   ;.
02F2          AUTO11: ;.
02F2                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
02F3             UNC CRET         2(8)   OR DA A8      B           ;   ;.
02F4          AUTO12: ;.
02F4                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
02F5             UNC CRET         2(#10) OR DA A8      B           ;   ;.
02F6          RESTER: ;.
02F6                CJP AUTO12    2(4) AND DQ                      ;   ;.
02F7                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
02F8             UNC CRET         2(#20) OR DA A8      B           ;   ;.
02F9           ;.
02F9          ADDI4: ;.
02F9                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
02FA             UNC CRET         2(#10) OR DA A5      B           ;   ;.
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02FB            ADDIS: ;.
02FB                   CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
02FC               UNC CRET          2(#20) OR DA A5      B           ;   ;.
02FD            ADDIF: ;.
02FD                   CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
02FE               UNC CRET          2(#30) OR DA A5      B           ;   ;.
02FF             ;.
02FF            ; SUBROUTINE "CALCULATE TRACK DIFFERENCE"   ;.
02FF            TRKDIF: ;.
02FF                   CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
0300                                                      TRK RIC     ;   ;.
0301                                                      TRK RIC     ;   ;.
0302                                 DAL C SUB DA A6      Q TRK RIC   ;   ;.
0303                   CJS SVMB3     COND AND DA A15      TRK         ;   ;.
0304                   CJP NEGATI 2(#80) AND DQ                       ;   ;.
0305                                 C BUS ZQ             Q           ;   ;.
0306            NEGATI: ;.
0306                   CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
0307                                 COND OR DZ A13       B           ;   ;.
0308                   CJP TP85OL    2(3) AND DA A13                  ;                  *******  ;.
0309                                 2(2) ADD DQ          Q           ;                  *******  ;.
030A            TESTLD: ;.
030A                   CRET          2(#80) AND DQ                    ;   ;.
030B                   CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
030C               UNC CRET          2(#20) OR DA A11     B           ;   ;.
030D            TP85OL: ;.
030D               UNC CJP TESTLD    2(7) ADD DQ          Q           ;                     *****  ;.
030E             ;.
030E            ; SUBROUTINE "DELAY HLT"   ;.
030E            DELHLT: ;.
030E                   LOCT 1(275)                                    ;   ;.
030F            WAHLT: ;.
030F                   CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
0310                                 COND OR DZ           Q           ;   ;.
0311                   CRET          2(2) AND DQ                      ;   ;.
0312                                 A10 EXN AQ           Q           ;   ;.
0313                   CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
0314                   CJP WAHLT     2(#80) AND DQ                    ;   ;.
0315               UNC CJS CHKRDY    2(#80) EXD DA A10    B           ;   ;.
0316                   CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
0317                   RPCT WAHLT                                     ;   ;.
0318                   CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
0319               UNC CJS UPDCHG    2(#40) OR DA A11     B UNIT      ;   ;.
031A                   CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
031B               UNC CJP DELHLT                                     ;   ;.
031C             ;.
031C            ; SUBROUTINE "UPDATE CHANGE BITS"   ;.
031C            UPDCHG: ;.
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031C                            RDY OR DZ           Q           ;   ;.
031D                CJS SVMB3   COND AND DA A15                 ; REQUEST FROM MAINBUS ?   ;.
031E                            Z(#F0) OR DQ A13    B           ;   ;.
031F                CJP CHINT3  A4 IAN AQ           Q           ;   ;.
0320            STNEW3: ;.
0320                            A13 OR ZA           Q STBY      ;   ;.
0321                CJS SVMB3   COND AND DA A15                 ; REQUEST FROM MAINBUS ?   ;.
0322            UNC CRET        OR ZQ A4            B           ;   ;.
0323            CHINT3: ;.
0323                            OR AQ A5            B CLBY      ;   ;.
0324            UNC CJP STNEW3  Z(#80) OR DA A7     B           ;   ;.
0325             ;.
0325            ; SUBROUTINE "CHECK READY"   ;.
0325            CHKRDY: ;.
0325                CJP MSKRDY  Z(1) AND DA A11     Q           ;   ;.
0326                CJS SVMB3   COND AND DA A15                 ; REQUEST FROM MAINBUS ?   ;.
0327                CJP MSKRDY  Z(2) AND DA A11     Q           ;   ;.
0328                CJP RDYZ    Z(3) AND DA A11                 ;   ;.
0329            UNC CJP MSKRDY  Z(8) OR DZ          Q           ;   ;.
032A            RDYZ: ;.
032A                            Z(4) OR DZ          Q           ;   ;.
032B            MSKRDY: ;.
032B                CJS SVMB3   COND AND DA A15                 ; REQUEST FROM MAINBUS ?   ;.
032C                            RDY OR DZ A13       B           ;   ;.
032D                CRET        A13 AND AQ          Q           ;   ;.
032E                            Z(#84) AND DA A7    B           ;   ;.
032F            NOTRDY: ;.
032F                CJS SVMB3   COND AND DA A15                 ; REQUEST FROM MAINBUS ?   ;.
0330            UNC CJPP ASP2   Z(8) OR DZ A8       B           ;   ;.
0331             ;.
0331             ; SUBROUTINE "CHECK WAS READY",
0331               CHECKS THAT DRIVE WAS READY AND NOT IN DISK CHANGE STATUS, WHEN CURRENT
0331               OPERATION WAS REQUESTED   ;.
0331            CHKWAS: ;.
0331                CJS SVMB3   COND AND DA A15                 ; REQUEST FROM MAINBUS ?   ;.
0332                            Z(63) ADD DZ A10    B           ;   ;.
0333          UNC   CRET        A4 AND AQ                       ;   ;.
0334            UNC CJP  NOTRDY Z(#84) AND DA A7    B           ;   ;.
0335             ;.
0335            ; SUBROUTINE "CHECK READ COMMAND"   ;.
0335            CHKREA: ;.
0335                CJS SVMB4   COND AND DA A15                 ; REQUEST FROM MAINBUS ?   ;.
0336                CJP ILLCOM  Z(#63) AND DA A14               ;   ;.
0337            UNC CRET                                        ;   ;.
0338             ;.
0338            ; SUBROUTINE " WAITE SIDE SELECTION"   ;.
0338            WASIDE: ;.
0338                            Z(#80) OR DZ        Q           ;   ;.
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MICRO PROGRAM SOURCE LISTNING
FOR ST. FD. CTRL. CR8047M/010AB/00

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033B            CJP TIM1      COND AND DQ                      ;   ;.
033A            CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
0339            CJP LOCM1     COND IAN DQ                      ;   ;.
033C            CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
033D            CJP LOCM1     COND AND DQ                      ;   ;.
033E         UNC CRET                                          ;   ;.
033F      TIM1: ;.
033F            CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
0340            CJP LOCM1     COND AND DQ                      ;   ;.
0341            CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
0342            CJP LOCM1     COND IAN DQ                      ;   ;.
0343         UNC CRET                                          ;   ;.
0344       ;.
0344      ; SUBROUTINE "DRQ-SERVICE "   ;.
0344      DRQSRV: ;.
0344            CJP WRIDAT    2(9) AND DA A14                  ;   ;.
0345            CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
0346                          2(63) OR DA A10      B DAT RIC   ;   ;.
0347                                               DAT RIC     ;   ;.
0348                          DAL EXN DZ A6        B DAT RIC   ;   ;.
0349            CJS SVMB4     COND AND DA A15      DAT         ;   ;.
034A            CJP REALOW    2(1) EXO DA A9       B           ;   ;.
0349            CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
034C         UNC CJP COMREA   UPBY A12 ADD ZA      BA LATCH    ;   ;.
034D      REALOW: ;.
034D            CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
034E                          A12 C ADD ZA         BA LATCH    ;   ;.
034F      COMREA: ;.
034F                          OR ZA DAL A6         BA LATCH WRA ;   ;.
0350         UNC CRET         OR ZA DAL A6         BA LATCH    ;   ;.
0351      WRIDAT: ;.
0351            CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
0352                          2(63) OR DA A10      B DAT WIC   ;   ;.
0353                          A6 OR ZA             BA DAT WIC  ;   ;.
0354                          A6 OR ZA             BA DAT      ;   ;.
0355            CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
0356            CJP WRIUPP    2(1) EXO DA A9       B           ;   ;.
0357      WRILOW: ;.
0357            CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
0358         UNC CJP COMWRI   A12 C ADD ZA         BA LATCH RAM ;   ;.
0359      WRIUPP: ;.
0359            CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ?   ;.
035A                          UPBY A12 ADD ZA      BA LATCH RAM ;   ;.
035B      COMWRI: ;.
035B                         EXN DZ A6             B LATCH RAM  ;   ;.
035C         UNC CRET         NIB                              ;   ;.
035D       ;.
035D      ;*****************************************************<  ;.
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035D            ;.
035D          RAUTO: ;.
035D                          A7 OR ZA DAL        DL          ;   ;.
035E                         2(#F3) AND DA A7     B           ;   ;.
035F             UNC CRET    2(#7F) AND DA A8     B      ;RESET PROGRAM ERROR &PE ;.
0360          RADDI: ;.
0360             CRET         2(#F0) AND DA A5     B           ;   ;.
0361             UNC CRET     2(#7F) AND DA A7     B           ;   ;.
0362          RBUFF: ;.
0362                          UPBY A12 ADD ZA RAM BA     DU    ;   ;.
0363             UNC CRET     A12 C ADD ZA RAM     BA DL       ;   ;.
0364            ;.
0364          WBUFF: ;.
0364             CJP WBUFF1   AND DA A13 RDY LATCH        ;TEST H/W SIGNAL PAROK.
0365                          ADD ZA A12 RU BA WRA.
0366                        C ADD ZA A12 RL BA             ;READ DATA FROM MAINBUS.
0367          PERROR: ;.
0367             UNC CRET     2(#80) OR DA A8  DL B CLBY ;SEND PE INTERRUPT SET PE INAUTO STATUS ;
0368          WBUFF1:         ADD ZA A12 RU BA WRA.
0369             UNC CRET   C ADD ZA A12 RL BA DL         ;READ MAINBUS DATA RELEASE ARQ.
036A            ;.
036A          XSTART: ;.
036A                          2(#80) OR DZ A13     B      ;BITMASK TO W13 ;.
036B             CJP XSTART1  AND DA A13 RDY              ;TEST H/W SIGNAL PAROK ;.
036C             UNC CJP PERROR.
036D          XSTART1:
036D             UNC CJPP START  RL OR DZ A6          B   ;READ LOWER COMMAND BYTE ;.
036E            ;.
036E          PTST: ;.
036E                          2(#80) OR DZ A13     B      ;BITMASK TO W13 ;.
036F             CJP PTST1    AND DA A13 RDY              ;TEST H/W SIGNAL PAROK ;.
0370             UNC CJP PERROR.
0371          PTST1:
0371             UNC CRET     AND DZ A12           B DL   ;CLEAR POINTER SEND RS ;.
0372            ;.
0372          IPTST: ;.
0372                          2(#80) OR DZ A13     B      ;BITMASK TO W13 ;.
0373             CJP IPTST1   AND DA A13 RDY              ;TEST H/W SIGNAL PAROK ;.
0374             UNC CJP PERROR.
0375          IPTST1:
0375             UNC CRET     2(#04) OR DA A7      B DL   ;SET INVALID COMMAND IN AUTOSTATUS ;.
0376            ;.
0376          SVMB0: ;.
0376             JMP BRNCH0   UPBY A12 ADD ZA      BA LATCH    ;   ;.
0377            ;.
0377          SVMB4: ;.
0377          SVMB3: ;.
0377             JMP BRNCH3   UPBY A12 ADD ZA      BA LATCH    ;   ;.
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0378          ;.
0379          ;*************************************************************  ;.
0379            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
0379            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
037A            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
037B            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
037C            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
037D            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
037E            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
037F            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
0380          ;*************************************************************  ;.
0380          ;.
0380        BRNCH0: ;.
0380            UNC CJP RAUTO     A8 OR ZA DAL        DU          ;   ;.
0381            UNC CJP RADDI     A5 OR ZA DAL        DL          ;   ;.
0382            UNC CJP RBUFF     UPBY A12 ADD ZA RAM BA          ;   ;.
0383            UNC CJP RBUFF     UPBY A12 ADD ZA RAM BA          ;   ;.
0384            UNC CJP XSTART    2(#7F) AND DA A8    B           ;CLEAR PE FLAG ;.
0385            UNC CJP PTST      2(#7F) AND DA A8    B           ;CLEAR PE FLAG ;.
0386            UNC CJP WBUFF 2(#80) OR DZ A13 LATCH B            ;BITMASK TO REG 13.
0387            UNC CJP WBUFF 2(#80) OR DZ A13 LATCH B            ;BITMASK TO REG 13.
0388          ;.
0386          ;*************************************************************  ;.
0388            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
0389            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
038A            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
038B            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
038C            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
038D            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
038E            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
038F            5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ;   ;.
0390          ;*************************************************************  ;.
0390          ;.
0390        BRNCH3: ;.
0390            UNC CJP RAUTO     A3 OR ZA DAL        DU          ;   ;.
0391            UNC CJP RADDI     A5 OR ZA DAL        DL          ;   ;.
0392            UNC CJP RBUFF     UPBY A12 ADD ZA RAM BA          ;   ;.
0393            UNC CJP RBUFF     UPBY A12 ADD ZA RAM BA          ;   ;.
0394            UNC CJP IPTST     2(#80) OR DA A13    B           ;BITMASK TO W13 ;.
0395            UNC CJP PTST      2(#7F) AND DA A8    B           ;CLEAR PE FLAG ;.
0396            UNC CJP WBUFF 2(#80) OR DZ A13 LATCH B            ;BITMASK TO REG 13.
0397            UNC CJP WBUFF 2(#80) OR DZ A13 LATCH B            ;BITMASK TO REG 13.
0398          ;.
0398
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5.2 PAL'S of CR8047D/010AB/00

CSD/005/LST/0013

K

TITLE: PAL Source for
Floppy Disk Ctrl. CR8047D/010AB/00

DOCUMENT NO : CSD/005/LST/0013

PREPARED BY : BERTRAM PAASKESEN

AUTHORIZED BY: GOTTLOB BORUP

DISTRIBUTION : BBP, FILE (2)

APPROVED BY:

AUTHORITY	DATE	SIGNATURE
ENG/QA	811002	Karl. Nielsen

ISSUE: 1

DATE: 810929

400-810-1

PAL Source for Floppy Disk Ctrl. CR8047D/010AB/00	sign/date BBP/810929	page i
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PAGE RECORD AND ISSUE LOG.

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PAL Source for Floppy Disk Ctrl. CR8047D/010AB/00	sign/date BBP/810929	page 1
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PAL Description:

This description is in accordance with the format used in

SD 20/24 PAL DEVELOPMENT SYSTEM
STRUCTURED DESIGN, INCORPORATED

The source code is situated on CR/T/0150.

The PAL's are used in the FLOPPY DISK CTRL. CR8047 as described in the Functional Description CSD/005/FNC/0032.

The PAL's are also described in CSD/005/VDD/0058.

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PAL Source for Floppy Disk Ctrl. CR8047D/010AB/00	sign/date BBP/810929	page 2
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     PAL16R6
     CR1776-01 810926 BBP

     /8MHZ TIC IRW CKOK PCL POK T64 SREL ITRQ GND
     /OE CLMIC RSFF ARQ RWI MODCL /LMOCL /ACC /DMD VCC

     IF(VCC)/DMD=POK*CKOK*TIC*SREL*ITRQ*/RWI
                +POK*CKOK*TIC*ACC
                +POK*CKOK*RSFF
                +POK*CKOK*/ACC*PCL

          LMOCL:=POK*CKOK*MODCL
                 +POK*CKOK*LMOCL*/T64

         /MODCL:=/CKOK+/POK+/ACC+/PCL*/MODCL

          /RWI:=/ACC*/ARQ*TIC*/IRW
                +ACC*/RWI+ARQ*/RWI+/TIC*/RWI


          /ARQ:=ARQ*SREL+ACC*/ARQ+/TIC*/ARQ+CLMIC

         /RSFF:=/ITRQ+/TIC+/ACC+/POK+/RWI*/SREL*/RSFF+/CKOK

     IF(VCC)/CLMIC=POK+CKOK+/LMOCL


     DESCRIPTION: MAINBUS PAL FOR DUALBUS ST.FD.CTRL

>ASSEMBLE

PASS
```

K

PAL Source for Floppy Disk Ctrl. CR8047D/010AB/00	sign/date BBP/810929	page 3
	replace	project

```
>XPLOT
#A

#P00 ---- ---- ---- ---- ---- ---- ---- ----
  01 X--- ---- X--- ---- X--X ---- X--- X---
  02 X--- ---X X--- ---- X--- ---- ---- ----
  03 ---- ---- X--- ---- X--- ---- --X- ----
  04 ---- --X- X--- X--- X--- ---- ---- ----
  05 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  06 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  07 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

  08 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  09 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  10 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  11 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  12 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  13 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  14 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  15 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

  16 ---- ---- X--- --X- X--- ---- ---- ----
  17 ---- ---- X--X ---- X--- -X-- ---- ----
  18 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  19 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  20 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  21 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  22 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  23 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

  24 ---- ---- -X-- ---- ---- ---- ---- ----
  25 ---- ---- ---- ---- -X-- ---- ---- ----
  26 ---- --X- ---- ---- ---- ---- ---- ----
  27 ---- ---- ---- -X-X ---- ---- ---- ----
  28 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  29 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  30 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  31 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
```

Cont.

K

PAL Source for Floppy Disk Ctrl. CR8047D/010AB/00	sign/date BBP/810929	page 4
	replace	project

```
32 X--- -XX- ---- ---- ---- ---X ---- ----
33 ---- ---X ---- ---- ---X ---- ---- ----
34 ---- ---- ---- ---- ---X --X- ---- ----
35 -X-- ---- ---- ---- ---X ---- ---- ----
36 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
37 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
38 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
39 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

40 ---- ---- ---- ---- ---- --X- X--- ----
41 ---- ---X ---- ---- ---- ---X ---- ----
42 -X-- ---- ---- ---- ---- ---X ---- ----
43 ---- ---- ---- ---- ---- ---- ---- --X-
44 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
45 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
46 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
47 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

48 ---- ---- ---- ---- ---- ---- ---- -X--
49 -X-- ---- ---- ---- ---- ---- ---- ----
50 ---- --X- ---- ---- ---- ---- ---- ----
51 ---- ---- ---- ---- -X-- ---- ---- ----
52 ---- ---- ---- ---- ---X ---- -X-X ----
53 ---- ---- -X-- ---- ---- ---- ---- ----
54 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
55 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

56 ---- ---- ---- ---- ---- ---- ---- ----
57 ---- ---- ---- ---- X--- ---- ---- ----
58 ---- ---- X--- ---- ---- ---- ---- ----
59 ---- ---- --X- ---- ---- ---- ---- ----
60 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
61 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
62 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
63 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
```

K

PAL Source for Floppy Disk Ctrl. CR8047D/010AB/00	sign/date BBP/810929	page 5
	replace	project

```
PAL16R4
   1775-1 BBP 810924
    /8MHZ BST CLBY STBY CLIN PCL F1 F3 F2 GND
/OE BUSY STPU GATE /STIN SI /ENDP INTEM HCL VCC

/SI:=CLIN+GATE*/INTEM+/CLBY*/SI+HCL+PCL
    /GATE:=/F1+F2+/F3+/SI*/INTEM+HCL
STIN:=/SI*F1*/F2*F3
IF(VCC)BUSY=STBY+/CLBY*BUSY
IF(VCC)/STPU=STBY+/BST*/STPU
ENDP:=F1*/F2*F3+F1*ENDP
DESCRIPTION:INTERRUPTPAL FOR DUAL BUS ST.FD.STRL


>ASSEMBLE


PASS
```

K

```
>XPLOT
#A

#P00 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  01 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  02 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  03 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  04 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  05 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  06 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  07 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

  08 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  09 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  10 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  11 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  12 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  13 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  14 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  15 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

  16 ---- ---- ---- ---- ---- X--- X--- -X--
  17 ---- ---- ---X ---- ---- X--- ---- ----
  18 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  19 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  20 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  21 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  22 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  23 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

  24 ---- ---- ---- X--- ---- ---- ---- ----
  25 ---- ---X ---- ---- ---- --X- ---- ----
  26 ---- -X-- ---- ---X ---- ---- ---- ----
  27 --X- ---- ---- ---- ---- ---- ---- ----
  28 ---- ---- ---- ---- X--- ---- ---- ----
  29 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  30 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
  31 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
```

Cont.

K

PAL Source for Floppy Disk Ctrl. CR8047D/010AB/00	sign/date BBP/810929	page 7
	replace	project

```
32 ---- ---- ---- ---X ---- X--- X--- -X--
33 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
34 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
35 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
36 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
37 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
38 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
39 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

40 ---- ---- ---- ---- ---- -X-- ---- ----
41 ---- ---- ---- ---- ---- ---- ---- X---
42 ---- ---- ---- ---- ---- ---- -X-- ----
43 ---- ---X ---- ---X ---- ---- ---- ----
44 --X- ---- ---- ---- ---- ---- ---- ----
45 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
46 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
47 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

48 ---- ---- ---- ---- ---- ---- ---- ----
49 ---- ---- X--- ---- ---- ---- ---- ----
50 -X-- ---- ---- ---- ---- ---- ---X ----
51 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
52 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
53 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
54 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
55 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

56 ---- ---- ---- ---- ---- ---- ---- ----
57 ---- ---- X--- ---- ---- ---- ---- ----
58 ---- -X-- ---- ---- ---- ---- ---- --X-
59 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
60 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
61 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
62 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
63 XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
```

K

5.3 Microprogram of CR8047D/010A-/00

CSD/005/LST/0009

K

TITLE: MICROPROGRAM FOR
FLOPPY DISC CTRL CR8062 & CR8047D/010A-/00

DOCUMENT NO : CSD/005/LST/0009

PREPARED BY : JOHANNES K. HANSEN

AUTHORIZED BY: GOTTLOB BORUP

DISTRIBUTION : BBP, JKH, FILE (2), GB

APPROVED BY:

AUTHORITY	DATE	SIGNATURE
ENG Manager	81.7 23	
ENG/QA	811002	N. Nielsen.

ISSUE: 1

DATE: 810921

400-810-1

MICROPROGRAM FOR FLOPPY DISC CTRL CR8062 & CR8047D/010A-/00	sign/date JKH/810921	page i
	repl	project

PAGE RECORD AND ISSUE LOG.

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ISSUE	DATE	PREPARED BY	APPROVED BY	AUTHORIZED BY
1	810921	JKH	KN	GB

A

Microprogram list

This list can be used as source for MICAS (CSS/006/USM/0019) except for left column hex numbers, which not should be used. The source are situated on CR/D/1879-a *HCLAM01* FLOPSRC.

This microprogram allow the Floppy Disc Controller to interface to Shugart SA 800/850 drives as described in CSD/005/PSP/0019 (CR8062) and CSD/005/PSP/0078 (CR8047D/010A-/00)

The PROM's which contains the microprogram, are described in CSD/005/VDD/0022.

```
                    ----------------------------
                    MICAS MICRO ASSEMBLER V800123
                    ----------------------------

0000          WORDLENGTH=56 ,
0000           PROMWIDTH=8 ,
0000          JUMPDED=1 ,
0000          PROMFILL=0
0000
0000          .
0000
0000           1  6 9   0 ,
0000           2 24 8   0 ,
0000           3  0 1   0 ,
0000           4  1 1   0 ,
0000           5  2 4   1 ,
0000           6 15 2   0 ,
0000           7 17 2   0 ,
0000           8 19 3   0 ,
0000           9 22 2   1 ,
0000          10 32 1   0 ,
0000          11 33 3   0 ,
0000          12 36 4   0 ,
0000          13 40 7 125 ,
0000          14 47 1   1 ,
0000          15 48 1   1 ,
0000          16 49 1   1 ,
0000          17 50 1   1 ,
0000          18 51 1   1 ,
0000          19 52 2   0 ,
0000          20 54 2   2 ,
0000          .
0000
```

```
0000
0000          UNC=1,3
0000          CLIN=1,4
0000          JZ=15,5
0000          CJS=14,5
0000          JMP=13,5
0000          CJP=12,5
0000          PCLC=11,5
0000          JRP=8,5
0000          RFCT=7,5
0000          RPCT=6,5
0000          CRET=5,5


0000          CJPP=4,5
0000          LDCT=3,5
0000          ENLO=2,5
0000          TWB=0,5
0000
0000          CLBY=1,6
0000          STBY=2,6
0000
0000          STCM=0,7
0000          TRK=1,7
0000          SCT=2,7
0000          DAT=3,7
0000
0000          AQ=0,8
0000          AB=1,8
0000          ZQ=2,8
0000          ZA=4,8
0000          DA=5,8
0000          DQ=6,8
0000          DZ=7,8
0000
0000          Q=0,9
0000          BA=2,9
0000          B=3,9
0000
```

```
0000          C=1,10
0000
0000          ADD=0,11
0000          SUB=1,11
0000          BUS=2,11
0000           OR=3,11
0000          AND=4,11
0000          IAN=5,11
0000          EXO=6,11
0000          EXN=7,11
0000
0000          A0=0,12
0000          A1=1,12
0000          A2=2,12
0000          A3=3,12
0000          A4=4,12
0000          A5=5,12
0000          A6=6,12
0000          A7=7,12
0000          A8=8,12
0000          A9=9,12
0000          A10=10,12
0000          A11=11,12


0000          A12=12,12
0000          A13=13,12
0000          A14=14,12
0000          A15=15,12
0000
0000          COND=126,13
0000          RDY=123,13
0000          RAM=119,13
0000          RL=111,13
0000          RU=95,13
0000          DAL=63,13
0000          NIB=127,13
0000
```

```
0000          RIC=0,14
0000          UPBY=0,15
0000          UNIT=0,16
0000          WIC=0,17
0000          LATCH=0,18
0000          WRA=1,19
0000          DU=2,19
0000          DL=3,20
0000          MR=0,20
0000        .

0000        ;     PROMREV-1.
0000                          AND DZ A12          B STBY UNIT MR CLIN ; .
0001                          2(1) OR DZ A15      B              ; .
0002                          2(#30) OR DZ A7     B              ; .
0003                          2(#40) OR DZ A5     B WIC          ; .
0004                          2(#D0) OR DZ        WIC            ; .
0005                          2(#D0) OR DZ                       ; .
0006          UNC PCLC 1(34)  AND DZ A8           B              ; .
0007              CJS SVM33   COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0008              RFCT        AND ZA A11          B              ; .
0009                          2(#F0) OR DZ A4     B              ; .
000A          UNC CJS GETSTA  2(128) OR DZ A0     B              ; HEAD POS UNKNOWN .
000B              CJP LOCM1   2(1) AND DQ                        ; .
000C                          2(128) OR DZ A1     B              ; HEAD POS UNKNOWN .
000D                          2(128) OR DZ A2     B              ; HEAD POS UNKNOWN .
000E              CJS SVM33   COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
000F                          2(128) OR DZ A3     B              ; HEAD POS UNKNOWN .
0010                          2(#7F) AND DA A7    B              ; .
0011                          AND DZ A5           B CLBY         ; .
0012
```

```
0012            NODEC:
0012                    CJS SVMBO     COND AND DA A15                  ; .
0013                    LDCT 1(77)                                     ; .
0014                    CJS SVMBO     COND AND DA A15                  ; .
0015                    RPCT LOCM1    COND EXO DA A10      Q           ; .
0016                    CJP NODEC     2(#80) AND DQ                    ; TEST TIMER .
0017                                  2(#80) EXO DA A10    B           ; CHANGE OLD TIMER .
0018                    CJS SVMBO     COND AND DA A15                  ; .
0019                    CJP NODEC     SUB ZA A9            B           ; DECR LOWER TIMER .
001A                                  SUB ZA A10           B           ; DECR UPPER TIMER .
001B                    CJP NODES     2(#7F) AND DA A10                ; UPPER = 0? .
001C                    CJS SVMBO     COND AND DA A15                  ; .
001D                                  2(#9F) AND DA A11    B           ; .
001E                                  AND DZ               UNIT        ; .
001F            NODES:
001F                    CJS SVMBO     COND AND DA A15                  ; .
0020                                  RDY OR DZ            Q           ; .
0021                                  2(#F0) OR DQ A13     B           ; STORE NEW RDY3:0 .
0022                    CJS SVMBO     COND AND DA A15                  ; .
0023                    CJP CHINT     IAN AQ A4            Q           ; DISK CHANGE ? .
0024            STNEW:
0024                                  A13 OR ZA            Q           ; NEW .
0025                                  OR ZQ A4             B           ; OLD:=NEW .
0026                    CJS SVMBO     COND AND DA A15                  ; .
0027                UNC CJP NODEC                                      ; .
0028
0029            CHINT:


0028                    CJS SVMBO     COND AND DA A15                  ; .
0029                                  2(#80) OR DA A7      B           ; .
002A                UNC CJP STNEW     OR AQ A5             B CLBY      ; DISK CHANGE INTERRUPT .
002B
```

MICROPROGRAM FOR FLOPPY DISC CTRL
CR8062 & CR8047D/010A-/00

CSD/005/LST/0009

sign/date JKH/810921

page 6

replace

project

```
0028  ;*****************************************************************.
0028  START:
0028                        RU OR DZ A14          B DL STBY     ; .
002C                        2(#40) OR DA A5       B             ; .
002D                        2(#F) AND DA A5       Q             ; .
002E        CJS SVMB3       COND AND DA A15                     ; .
002F                        ADD ZQ A10            B             ; .
0030    UNC CJS OGTSTA      2(#80) OR DA A7       B             ; .
0031
0031        CJS SVMB3       COND AND DA A15                     ; REQUEST FROM MAINBUS ? .
0032        CJP NOTO        2(3) AND DA A14                     ; .
0033                        A0 OR ZA              Q             ; .
0034    UNC CJP LDNEU       2(1) OR DZ A13        B             ; DECODED NEW UNIT .
0035  NOTO:
0035        CJS SVMB3       COND AND DA A15                     ; REQUEST FROM MAINBUS ? .
0036        CJP UN2OR3      2(2) AND DA A14                     ; .
0037                        A1 OR ZA              Q             ; .
0038    UNC CJP LDNEU       2(2) OR DZ A13        B             ; .
0039  UN2OR3:
0039        CJS SVMB3       COND AND DA A15                     ; REQUEST FROM MAINBUS ? .
003A        CJP UN3         2(1) AND DA A14                     ; .
003B                        A2 OR ZA              Q             ; .
003C    UNC CJP LDNEU       2(8) OR DZ A13        B             ; .
003D  UN3:
003D                        A3 OR ZA              Q             ; .
003E    UNC CJP LDNEU       2(16) OR DZ A13       B             ; .
003F
003F  LDNEU:
003F        CJS SVMB3       COND AND DA A15                     ; REQUEST FROM MAINBUS ? .
0040                                              TRK WIC       ; .
0041                        OR ZQ                 TRK WIC       ; .
0042                        OR ZQ                 TRK           ; .
0043        CJS SVMB3       COND AND DA A15                     ; REQUEST FROM MAINBUS ? .
0044                        2(#80) AND DQ A9      B             ; R9 NOT ZERO MEANS
0044                                                              TRK UNDEFINED .
0045                        A13 OR ZA             Q             ; .
0046        CJS SVMB3       COND AND DA A15                     ; REQUEST FROM MAINBUS ? .
0047        CJP SAMEUN      A11 AND AQ                          ; .
0048                        OR ZQ A11             B             ; NEW UNIT .
0049  SAMEUN:
0049                        2(#84) AND DA A14     Q             ; DENS/SIDE .
004A        CJS SVM33       COND AND DA A15                     ; REQUEST FROM MAINBUS ? .
004B                        2(123) EXO DQ         Q             ; /DENS/SIDE .
```

```
004C                          2 (#7B) AND DA A11    B              ;.
004D                          A11 OR AQ             B              ; SET DENS,SIDE I REG11 .
004E          CJS SVMB3       COND AND DA A15                      ; REQUEST FROM MAINBUS ? .
004F
004F          CJP NSELEC      2(#78) AND DA A14                    ; .
0050
0050     ;OPERATION "SELECT" .
0050
0050                          2(#FB) AND DA A11     UNIT           ; .
0051          CJS SVMB3       COND AND DA A15                      ; REQUEST FROM MAINBUS ? .
0052                                                STCM WIC       ; .
0053                          2(#D0) OR DZ          STCM WIC       ; .
0054      UNC PCLC 1(16)      2(#D0) OR DZ          STCM           ; .
0055          CJS SVMB3       COND AND DA A15                      ; REQUEST FROM MAINBUS ? .
0056          RFCT                                                 ; DELAY FROM LOAD COMMAND
0056                                                                 TO READ STATUS .
0057      UNC CJS GETSTA                            ; .
0058          CJS AUTO6       2(1) AND DQ                          ; .
0059          CJS AUTO11      2(#80) AND DQ                        ; .
005A          CJS SVMB3       COND AND DA A15                      ; REQUEST FROM MAINBUS ? .
005B          CJS AUTO8       2(#40) AND DQ                        ; .
005C                          2(#4F) AND DA A5      B              ; .
005D                          COND OR DZ            Q              ; .
005E          CJS SVMB3       COND AND DA A15                      ; REQUEST FROM MAINBUS ? .
005F          CJS ADDI7       2(#10) AND DQ                        ; .
0060      UNC CJP COMSLT                                           ; .
0061
0061     NSELEC:
0061      UNC CJS CHKRDY                                           ; .
0062      UNC CJS CHKWAS      A10 IAN AQ            Q              ; .
0063          CJS SVMB3       COND AND DA A15                      ; REQUEST FROM MAINBUS ? .
0064          CJP REAWRI      2(#18) AND DA A14                    ; .
0065          CJP RESTOR      2(#58 AND DA A14                     ; .
0066          CJS SVMB3       COND AND DA A15                      ; REQUEST FROM MAINBUS ? .
0067
0067     ; OPERATION "SEEK" .
0067
0067          CJP SEER        2(128) AND DA A6                     ; .
0068                          2(#33) ADD DA A6      Q              ; .
0069          CJS SVMB3       COND AND DA A15                      ; REQUEST FROM MAINBUS ? .
006A          CJP SEER        2(128) AND DQ                        ; .
006B          CJS EXECRS      A9 ADD ZA                            ; EXECUTE A RESTORE,
006B                                                                 IF TRACK IS UNDEFINED .
```

```
006C          UNC CJS TRKDIF   2(#FB) AND DA A11   UNIT        ; .
006D       NOLOAD:
006D              CJS SVMB3    COND AND DA A15                 ; REQUEST FROM MAINBUS ? .
006E              CJP TP350U   2(8) AND DA A13                 ;                  *******.
006F                           2(5)  ADD DQ        Q           ;                  *******.
0070       TESTUN:


0070              CJP UNLOAD   2(#80) AND DQ                   ; .
0071       TESTSI:
0071              CJS SVMB3    COND AND DA A15                 ; REQUEST FROM MAINBUS ? .
0072              CJP TWOSI    2(#10) AND DA A13               ; .
0073              CJP INVSI    2(4) AND DA A11                 ; .
0074       TWOSI:
0074          UNC CJP LDNWTK   A11 OR ZA           UNIT        ; .
0075       TP850U:                                             ;                  *******.
0075          UNC CJP TESTUN   2(16) ADD DQ        Q           ;                 *********.
0076       UNLOAD:
0076              CJS SVMB3    COND AND DA A15                 ; REQUEST FROM MAINBUS ? .
0077          UNC CJP TESTSI   2(#9F) AND DA A11   B           ; .
0078
0078       LDNWTK:
0078              CJS SVMB3    COND AND DA A15                 ; REQUEST FROM MAINBUS ? .
0079                                              DAT WIC      ; .
007A                           A6 OR ZA           DAT WIC      ; .
007B                           A6 OR ZA           DAT          ; .
007C              CJS SVMB3    COND AND DA A15                 ; REQUEST FROM MAINBUS ? .
007D          UNC CJS WASIDE                                   ; .
007E              CJS SVMB3    COND AND DA A15                 ; REQUEST FROM MAINBUS ? .
007F              CJP TP850S   2(8) AND DA A13     STCM WIC    ; .
0080                           2(#1E) OR DZ        STCM WIC    ;                  *******.
0081          UNC CJP SECMLD   2(#1E) OR DZ        STCM        ; .
0082       TP850S:                                             ;                  *******.
0082                           2(#1C) OR DZ        STCM WIC    ; .
0083                           2(#1C) OR DZ        STCM        ;                  *******.
0084       SECMLD:
0084              CJS SVMB3    COND AND DA A15                 ; REQUEST FROM MAINBUS ? .
0085              CJP HLDON    2(#20) AND DA A11               ; .
0086              LDCT 1(100)                                  ; .
```

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0087          WAHDLD:
0087                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
0088                              COND OR DZ          Q            ; .
0089                CJP STEPPU    2(#40) AND DQ                    ; .
008A                CJP SEEKOV    2(2) AND DQ                      ; .
008B                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
008C                              A10 EXN AQ          Q            ; .
008D                CJP WAHDLD    2(#80) AND DQ                    ; .
008E                RPCT WAHDLD   2(#80) EXO DA A10   B            ; .
008F                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
0090                              2(#84) AND DA A7    B            ; .
0091                              2(#C0) OR DA A7     B            ; .
0092             UNC CJP ABEND    AND DZ A8           B            ; .
0093                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
0094
0094          STEPPU:
0094             UNC CJS TRKDIF                                    ; .


0095                CJS SVMB3     COND AND DA A15                  ; .
0096                              A11 OR ZA           UNIT         ; .
0097             UNC CJS CHKRDY                                    ; .
0098             UNC CJS UPDCHG                                    ; .
0099                CJS SVMB3     COND AND DA A15                  ; .
009A             UNC CJP SECMLD                                    ; .
009B
009B          HLDON:
009B             UNC CJS DELHLT                                    ; .
009C          SEEKOV:
009C             UNC CJS GETSTA                                    ; .
009D                              2(#4F) AND DA A5    B            ; .
009E                CJS AUTO6     2(1) AND DQ                      ; .
009F                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00A0                CJS AUTO1     2(3) AND DQ                      ; .
00A1                CJS AUTO12    2(#10) AND DQ                    ; .
00A2                CJS AUTO11    2(#80) AND DQ                    ; .
00A3                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00A4                              2(1) OR DA A7       B            ; .
00A5                CJS SENDCP    2(#42) AND DA A7                 ; .
00A6                CJS SENDCP    2(#18) AND DA A8                 ; .
00A7                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00A8             UNC CJP COMSLT                                    ; .
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00A9
00A9          ; OPERATION " RESTORE" .
00A9        RESTOR:
00A9              CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00AA              CJP ILLCOM    2(#38) AND DA A14                ; .
00AB          UNC CJS EXECRS                                     ; .
00AC          UNC CJP COMSLT                                     ; .
00AD
00AD          ; OPERATION "READ" OR "WRITE" .
00AD        REAWRI:
00AD              CJS CHKREA    2(#50) AND DA A14                ; .
00AE              CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00AF                            2(#FB) AND DA A11   UNIT SCT WIC ; .
00B0                            A6 OR ZA            SCT WIC      ; .
00B1                            A6 OR ZA            SCT          ; .
00B2              CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00B3                            COND OR DZ          Q            ; .
00B4              CJP TWOSRW    2(#10) AND DQ                    ; .
00B5              CJP INVSRW    2(4) AND DA A11                  ; .
00B6        TWOSRW:
00B6              CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00B7          UNC CJS WASIDE    A11 OR DA 2(#20)    B UNIT       ; .
00B8              CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00B9                            2(#80) OR DZ        Q            ; .
00BA              CJP RWCM      2(#10) AND DA A14                ; .


00BB                            2(#21) OR DQ        Q            ; .
00BC              CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00BD              CJP RWCM      2(#20) AND DA A14                ; .
00BE                            2(#FE) AND DQ       Q            ; .
00BF        RWCM:
00BF              CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00C0                            AND DZ A12          B STCM WIC   ; .
00C1                            OR ZQ               STCM WIC     ; .
00C2                            OR ZQ               STCM         ; .
00C3              CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00C4          UNC CJS WRIUPP    2(1) OR DZ A9       B            ; .
00C5        RWCMLD:
00C5              CJS SVMB4     COND AND DA A15,                 ; REQUEST FROM MAINBUS ? .
00C6              LDCT 1(275)                                    ; .
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00C7    WAITIN:
00C7                        COND OR DZ          Q          ; .
00C8        CJS SVMB4       COND AND DA A15                ; REQUEST FROM MAINBUS ? .
00C9        CJS DRQSRV      2(4) AND DQ                    ; .
00CA        CJS SVMB4       COND AND DA A15                ; REQUEST FROM MAINBUS ? .
00CB        CJP RWOVER      2(2) AND DQ                    ; .
00CC                        A10 EXN AQ          Q          ; .
00CD        CJS SVMB4       COND AND DA A15                ; REQUEST FROM MAINBUS ? .
00CE        CJP WAITIN      2(#80) AND DQ                  ; .
00CF        RPCT WAITIN     2(#80) EXO DA A10   B          ; .
00D0
00D0        LDCT INVSRW     COND OR DZ          Q          ; .
00D1
00D1        CJS SVMB4       COND AND DA A15                ; REQUEST FROM MAINBUS ? .
00D2        CJS DRQSRV      2(4) AND DQ                    ; .
00D3        CJS SVMB4       COND AND DA A15                ; REQUEST FROM MAINBUS ? .
00D4    UNC CJS UPDCHG      2(#40) OR DA A11    B UNIT     ; .
00D5        CJS SVMB4       COND AND DA A15                ; REQUEST FROM MAINBUS ? .
00D6                        COND OR DZ          Q          ; .
00D7        CJS DRQSRV      2(4) AND DQ                    ; .
00D8        CJS SVMB4       COND AND DA A15                ; REQUEST FROM MAINBUS ? .
00D9    UNC CJS CHKRDY      2(#7F) AND DA A10   B          ; .
00DA        JRP RWCMLD      A10 SUB ZA          B          ; .
00DB
00DB    RWOVER:
00DB    UNC CJS GETSTA      AND DZ A12          B          ; .
00DC        CJS AUTO6       2(1) AND DQ                    ; .
00DD        CJS AUTO11      2(#30) AND DQ                  ; .
00DE        CJS SVMB4       COND AND DA A15                ; REQUEST FROM MAINBUS ? .
00DF        CJS AUTO3       2(#40) AND DQ                  ; .
00E0        CJS AUTO5       2(#10) AND DQ                  ; .
00E1        CJS SVMB4       COND AND DA A15                ; REQUEST FROM MAINBUS ? .
00E2        CJS CRCERR      2(3) AND DQ                    ; .
00E3                        2(#4F) AND DA A5    B          ; .
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00E4                CJS ADDI4     2(#20) AND DQ                    ; .
00E5                CJS SVMB4     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00E6                CJS ADDI5     2(4) AND DQ                      ; .
00E7             UNC CJP COMSLT                                    ; .
00E8
00E8          SEER:
00E8                              2(#84) AND DA A7     B           ; .
00E9                              2(#10) OR DZ A8      B           ; .
00EA                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00EB             UNC CJP COMSLT   2(#4F) AND DA A5     B           ; .
00EC
00EC          INVSI:
00EC                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00ED                              2(#84) AND DA A7     B           ; .
00EE                              2(#10) OR DZ A8      B           ; .
00EF          ABEND:
00EF                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00F0             UNC CJS CHKRDY   2(#4F) AND DA A5     B           ; .
00F1          ABP2:
00F1                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00F2                                                  WIC         ; .
00F3                              2(#DO) OR DZ         WIC         ; .
00F4             UNC CJS OGTSTA   2(#DO) OR DZ                     ; .
00F5                CJP LOCM1     2(1) AND DQ                      ; .
00F6             UNC CJP COMSLT                                    ; .
00F7          INVSRW:
00F7                CJS SVME4     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00F8                              AND DZ A8            B           ; .
00F9                              2(#84) AND DA A7     B           ; .
00FA             UNC CJP ABEND    2(#20) OR DZ A7      B           ; .
00FB
00FB
00FB          ILLCOM:
00FB                              AND DZ A8            B           ; .
00FC                              2(#84) AND DA A7     B           ; .
00FD                CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
00FE                              2(4) OR DZ A7        B           ; .
00FF                              2(#4F) AND DA A5     B           ; .
0100
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0100            COMSLT:
0100                  CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0101                                TRK RIC                            ; .
0102                                TRK RIC                            ; .
0103                                TRK RIC DAL OR DZ    Q             ; .
0104                  CJS SVMB3     TRK COND AND DA A15                ; .
0105                  CJP SAUN0     2(1) AND DA A11                    ; .
0106                  CJP SAUN1     2(2) AND DA A11                    ; .
0107                  CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .


0108                  CJP SAUN2     2(8) AND DA A11                    ; .
0109                  CJP SAUN3     2(16) AND DA A11                   ; .
010A
010A            FENEU:
010A                  CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
010B                  CJP ADDNZ     2(#BF) AND DA A5     B    CLBY    ; .
010C                                2(#7F) AND DA A7     B CLBY       ; .
010D            ADDNZ:
010D               UNC ENLO                                            ; .
010E                  CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
010F               UNC ENLO                                            ; .
0110               UNC ENLO                                            ; .
0111               UNC ENLO         2(15) OR DZ A10      B             ; .
0112                  CJS SVMBO     COND AND DA A15                    ; .
0113               UNC CJP NODEC    AND DZ A9            B             ; .
0114
0114            SAUN0:
0114               UNC CJP FENEU    OR ZQ A0             B             ; .
0115            SAUN1:
0115               UNC CJP FENEU    OR ZQ A1             B             ; .
0116            SAUN2:
0116               UNC CJP FENEU    OR ZQ A2             B             ; .
0117            SAUN3:
0117               UNC CJP FENEU    OR ZQ A3             B             ; .
0118
0118            ;*****************************************************<.
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0118
0118
0118        DGTSTA:
0118              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0119                            RIC                                ; .
011A                            RIC                                ; .
011B                            RIC DAL OR DZ        Q             ; .
011C              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
011D         UNC CRET                                              ; .
011E
011E        ; SUBROUTINE "GETSTATUS" .
011E        GETSTA:
011E              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
011F                            2(#34) AND DA A7     B STCM RIC    ; .
0120                            AND DZ A8            B STCM RIC    ; .
0121                            DAL OR DZ            Q STCM RIC ; .
0122              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0123         UNC CRET                                              ; .
0124
0124         ; SUBROUTINE "EXECUTE A RESTORE OPERATION" .
0124        EXECRS:                                                ; .
0124         UNC CJS UPDCHG     2(#9B) AND DA A11    B UNIT        ; .


0125              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0126         UNC CJS WASIDE                                        ; .
0127              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0128                            COND OR DZ A13       B             ; .
0129              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
012A              CJP TP85OR    2(8) AND DA A13      STCM WIC      ;                       *******.
012B                            2(#E) OR DZ          STCM WIC      ; .
012C         UNC CJP RSCMLD     2(#E) OR DZ          STCM          ; .
012D        TP85OR:                                                ;                       *******.
012D                            2(#C) OR DZ          STCM WIC      ; .
012E                            2(#C) OR DZ          STCM          ; .
012F        RSCMLD:
012F              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0130              LDCT 1(100)                                      ; .
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0131        WANOST:
0131              CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
0132                            COND OR DZ          Q            ; .
0133              CJP STEPRS    2(#40) AND DQ                    ; .
0134              CJP RESTOV    2(2) AND DQ                      ; .
0135              CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
0136                            A10 EXN AQ          Q            ; .
0137         CJP WANOST         2(#80) AND DQ                    ; .
0138              RPCT WANOST   2(#80) EXO DA A10   B            ; .
0139              CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
013A                            2(#20) OR DA A11    B UNIT       ; .
013B         UNC CJS DELHLT                                      ; .
013C        RESTOV:
013C         UNC CJS GETSTA                                      ; .
013D                            2(#4F) AND DA A5    B            ; .
013E              CJS AUTO6     2(1) AND DQ                      ; .
013F              CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
0140              CJS AUTO1     2(3) AND DQ                      ; .
0141              CJS AUTO11    2(#80) AND DQ                    ; .
0142              CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
0143              CJS RESTER    2(#10) AND DQ                    ; .
0144              CJPP COMSLT   2(#73) AND DA A7                 ; .
0145              CJPP COMSLT   A8 ADD ZA                        ; .
0146              CJS SVMB3     COND AND DA A15                  ; .
0147         UNC CRET                                            ; .
0148
0148        STEPRS:
0148              CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
0149         UNC CJS CHKRDY                                      ; .
014A         UNC CJS UPDCHG                                      ; .
014B              CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
014C         UNC CJP RSCMLD                                      ; .
014D
014D
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014D    ; SUBROUTINES FOR SETTING STATUSBITS .
014D    SENDCP:
014D            CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
014E       UNC  CRET          2(#FE) AND DA A7      B            ; .
014F    AUTO1:
014F            CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0150       UNC  CRET          2(2) OR DA A7         B            ; .
0151    CRCERR:
0151            CJP AUTO1     2(#10) AND DQ                      ; .
0152            CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0153       UNC  CRET          2(#10) OR DA A7       B            ; .
0154    AUTO5:
0154            CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0155       UNC  CRET          2(#20) OR DA A7       B            ; .
0156    AUTO6:
0156            CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0157       UNC  CRET          2(#40) OR DA A7       B            ; .
0158    AUTO8:
0158            CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0159       UNC  CRET          2(1) OR DA A8         B            ; .
015A    AUTO11:
015A            CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
015B       UNC  CRET          2(8)   OR DA A8       B            ; .
015C    AUTO12:
015C            CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
015D       UNC  CRET          2(#10) OR DA A8       B            ; .
015E    RESTER:
015E            CJP AUTO12    2(4) AND DQ                        ; .
015F            CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0160       UNC  CRET          2(#20) OR DA A8       B            ; .
0161
0161    ADDI4:
0161            CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0162       UNC  CRET          2(#10) OR DA A5       B            ; .
0163    ADDI5:
0163            CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0164       UNC  CRET          2(#20) OR DA A5       B            ; .
0165    ADDI7:
0165            CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0166       UNC  CRET          2(#80) OR DA A5       B            ; .
```

```
0167
0167        ; SUBROUTINE "CALCULATE TRACK DIFFERENCE" .
0167        TRKDIF:
0167              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0168                                           TRK RIC             ; .
0169                                           TRK RIC             ; .
016A                            DAL C SUB DA A6    Q TRK RIC       ; .
016B              CJS SVMB3     COND AND DA A15    TRK             ; .

016C              CJP NEGATI 2(#80) AND DQ                         ; .
016D                            C BUS ZQ           Q               ; .
016E        NEGATI:
016E              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
016F                            COND OR DZ A13     B               ; .
0170              CJP TP850L    2(8) AND DA A13                    ;                    *******.
0171                            2(2) ADD DQ        Q               ;                    *******.
0172        TESTLD:
0172              CRET          2(#80) AND DQ                      ; .
0173              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0174          UNC CRET          2(#20) OR DA A11   B               ; .
0175        TP850L:
0175          UNC CJP TESTLD    2(7) ADD DQ        Q               ;                     *****.
0176
0176        ; SUBROUTINE "DELAY HLT" .
0176        DELHLT:
0176              LDCT 1(275)                                       ; .
0177        WAHLT:
0177              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0178                            COND OR DZ         Q               ; .
0179              CRET          2(2) AND DQ                        ; .
017A                            A10 EXN AQ         Q               ; .
017B              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
017C              CJP WAHLT     2(#80) AND DQ                      ; .
017D          UNC CJS CHKRDY    2(#80) EXO DA A10  B               ; .
017E              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
017F              RPCT WAHLT                                       ; .
0180              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0181          UNC CJS UPDCHG    2(#40) OR DA A11   B UNIT          ; .
0182              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
0183          UNC CJP DELHLT                                       ; .
```

```
0184
0184    ; SUBROUTINE "UPDATE CHANGE BITS" .
0184    UPDCHG:
0184          CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
0185                        RDY OR DZ            Q           ; .
0186                        2(#F0) OR DQ A13     B           ; .
0187          CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
0188          CJP CHINT3    A4 IAN AQ            Q           ; .
0189    STNEW3:
0189                        A13 OR ZA            Q STBY      ; .
018A       UNC CRET         OR ZQ A4             B           ; .
018B    CHINT3:
018B          CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
018C                        OR AQ A5             B CLBY      ; .
018D       UNC CJP STNEW3   2(#80) OR DA A7      B           ; .
018E
018E    ; SUBROUTINE "CHECK READY" .


018E    CHKRDY:
018E          CJP MSKRDY    2(1) AND DA A11      Q           ; .
018F          CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
0190          CJP MSKRDY    2(2) AND DA A11      Q           ; .
0191          CJP RDY2      2(8) AND DA A11                  ; .
0192       UNC CJP MSKRDY   2(8) OR DZ            Q           ; .
0193    RDY2:
0193                        2(4) OR DZ           Q           ; .
0194    MSKRDY:
0194          CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
0195                        RDY OR DZ A13        B           ; .
0196          CRET          A13 AND AQ           Q           ; .
0197                        2(#84) AND DA A7     B           ; .
0198    NOTRDY:
0198          CJS SVMB3     COND AND DA A15                  ; REQUEST FROM MAINBUS ? .
0199       UNC CJPP ABP2    2(8) OR DZ A8        B           ; .
019A
019A    ; SUBROUTINE "CHECK WAS READY",
019A      CHECKS THAT DRIVE WAS READY AND NOT IN DISK CHANGE STATUS, WHEN CURRENT
019A      OPERATION WAS REQUESTED .
```

```
019A        CHKWAS:
019A              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
019B                            2(63) ADD DZ A10     B             ; .
019C        UNC   CRET          A4 AND AQ                          ; .
019D        UNC CJP   NOTRDY    2(#84) AND DA A7     B             ; .
019E
019E        ; SUBROUTINE "CHECK READ COMMAND" .
019E        CHKREA:
019E              CJS SVMB4     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
019F              CJP ILLCOM    2(#68) AND DA A14                  ; .
01A0        UNC CRET                                               ; .
01A1
01A1        ; SUBROUTINE " WAITE SIDE SELECTION" .
01A1        WASIDE:
01A1                            2(#80) OR DZ         Q             ; .
01A2              CJP TIM1      COND AND DQ                        ; .
01A3              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
01A4              CJP LOCM1     COND IAN DQ                        ; .
01A5              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
01A6              CJP LOCM1     COND AND DQ                        ; .
01A7        UNC CRET                                               ; .
01A8        TIM1:
01A8              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
01A9              CJP LOCM1     COND AND DQ                        ; .
01AA              CJS SVMB3     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
01AB              CJP LOCM1     COND IAN DQ                        ; .
01AC        UNC CRET                                               ; .
01AD


01AD        ; SUBROUTINE "DRQ-SERVICE " .
01AD        DRQSRV:
01AD              CJP WRIDAT    2(8) AND DA A14                    ; .
01AE              CJS SVMB4     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
01AF                            2(63) OR DA A10      B DAT RIC     ; .
01B0                                                 DAT RIC       ; .
01B1                            DAL EXN DZ A6        B DAT RIC     ; .
01B2              CJS SVMB4     COND AND DA A15      DAT           ; .
01B3              CJP REALOW    2(1) EXO DA A9       B             ; .
01B4              CJS SVMB4     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
01B5        UNC CJP COMREA      UPBY A12 ADD ZA      BA LATCH      ; .
01B6        REALOW:
```

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01B6            CJS SVMB4     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
01B7                          A12 C ADD ZA          BA LATCH     ; .
01B8        COMREA:
01B8                          OR ZA DAL A6          BA LATCH WRA ; .
01B9           UNC CRET       OR ZA DAL A6          BA LATCH     ; .
01BA        WRIDAT:
01BA            CJS SVMB4     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
01BB                          2(63) OR DA A10       B DAT WIC    ; .
01BC                          A6 OR ZA              BA DAT WIC   ; .
01BD                          A6 OR ZA              BA DAT       ; .
01BE            CJS SVMB4     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
01BF            CJP WRIUPP    2(1) EXO DA A9        B            ; .
01C0        WRILOW:
01C0            CJS SVMB4     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
01C1       UNC CJP COMWRI     A12 C ADD ZA          BA LATCH RAM ; .
01C2        WRIUPP:
01C2            CJS SVMB4     COND AND DA A15                    ; REQUEST FROM MAINBUS ? .
01C3                          UPBY A12 ADD ZA       BA LATCH RAM ; .
01C4        COMWRI:
01C4                          EXN DZ A6             B LATCH RAM  ; .
01C5           UNC CRET       NIB                                ; .
01C6
01C6        ;*****************************************************<.
01C6
01C6        RAUTO:
01C6                          A7 OR ZA DAL          DL           ; .
01C7           UNC CRET       2(#FB) AND DA A7      B            ; .
01C8        RADDI:
01C8            CRET          2(#F0) AND DA A5      B            ; .
01C9           UNC CRET       2(#7F) AND DA A7      B            ; .
01CA        RBUFF:
01CA                          UPBY A12 ADD ZA RAM BA      DU     ; .
01CB           UNC CRET       A12 C ADD ZA RAM      BA DL        ; .
01CC
01CC        WBUFF:
01CC           UNC CRET       C ADD ZA A12 RL       BA DL        ; .


01CD
01CD        SVMBO:
01CD            JMP BRNCHO    UPBY A12 ADD ZA       BA LATCH     ; .
```

MICROPROGRAM FOR FLOPPY DISC CTRL
CR8062 & CR8047D/010A-/00

CSD/005/LST/0009
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```
01CE
01CE        SVMB4:
01CE        SVMB3:
01CE              JMP BRNCH3   UPBY A12 ADD ZA     BA LATCH     ; .
01CF
01CF
01CF         ;*****************************************************************.
01CF           5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ; .
01D0         ;*****************************************************************.
01D0
01D0        BRNCH0:
01D0           UNC CJP RAUTO     A8 OR ZA DAL          DU            ; .
01D1           UNC CJP RADDI     A5 OR ZA DAL          DL            ; .
01D2           UNC CJP RBUFF     UPBY A12 ADD ZA RAM BA              ; .
01D3           UNC CJP RBUFF     UPBY A12 ADD ZA RAM BA              ; .
01D4           UNC CJPP START    RL OR DZ A6           B             ; .
01D5           UNC CRET          AND DZ A12            B DL          ; .
01D6           UNC CJP WBUFF     ADD ZA A12 RU         BA WRA        ; .
01D7           UNC CJP WBUFF     ADD ZA A12 RU         BA WRA        ; .
01D8
01D8         ;*****************************************************************.
01D8           5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ; .
01D9           5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ; .
01DA           5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ; .
01DB           5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ; .
01DC           5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ; .
01DD           5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ; .
01DE           5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ; .
01DF           5(0) 9(0) 13(0) 14(0) 15(0) 16(0) 17(0) 18(0) 20(0) ; .
01E0         ;*****************************************************************.
01E0
01E0        BRNCH3:
01E0           UNC CJP RAUTO     A8 OR ZA DAL          DU            ; .
01E1           UNC CJP RADDI     A5 OR ZA DAL          DL            ; .
01E2           UNC CJP RBUFF     UPBY A12 ADD ZA RAM BA              ; .
01E3           UNC CJP RBUFF     UPBY A12 ADD ZA RAM BA              ; .
01E4           UNC CRET          2(4) OR DA A7         B DL          ; .
01E5           UNC CRET          AND DZ A12            B DL          ; .
01E6           UNC CJP WBUFF     ADD ZA A12 RU         BA WRA        ; .
01E7           UNC CJP WBUFF     ADD ZA A12 RU         BA WRA        ; .
01E8
01E8
```

5.4 PAL's of CR8047D/010A-/00

CSD/005/LST/0010

K

TITLE: PAL SOURCE FOR FLOPPY DISK CTRL. CR8062 & CR8047D/010A-/00

DOCUMENT NO: CSD/005/LST/0010

PREPARED BY: JOHANNES KRUSE HANSEN

APPROVED BY: KARSTEN NIELSEN

AUTHORIZED BY: GOTTLOB BORUP

DISTRIBUTION: BBP, JKH, File(2)

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DATE:	810921							

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PAL SOURCE FOR FLOPPY DISK CTRL. CR8062 & CR8047D/010A-/00	sign/date JKH/810921	page i
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PAL SOURCE FOR FLOPPY DISK CTRL. CR8062 & CR8047D/010A-/00	sign/date JKH/810921	page 1
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PAL Description:

This discription is in accordance with the format used in

SD 20/24 PAL DEVELOPMENT SYSTEM
STRUCTURED DESIGN, INCORPORATED

The source code is situated on CR/T/0116.

The PAL's are used in the FLOPPY DISK CTRL. CR8062 as described in the Functional Description CSD/005/FNC/0031 and in CR8047D/010A-/00.

The PAL's are also described in CSD/005/VDD/0022.

PAL SOURCE FOR FLOPPY DISK CTRL. CR8062 & CR8047D/010A-/00	sign/date JKH/810921	page 2
	replace	project

```
PAL16R6
     CR1505-1 JKH/790924
     FDC,UA5

     /8MHZ /TIC /RW /IMC AD11 INCL T64 PEL ITRQ GND
     /OE CLMIC RSFF ARQ RWI MODCL /LMOCL /ACC DMD VCC


     IF(VCC)/DMD:=/INCL*/IMC*TIC*REL*ITRQ*/RWI +
                    /INCL*/IMC*TIC*ITRQ*/DMD*/RWI

        ACC:=/INCL*/IMC*/ACC*/ARQ*TIC +
             /INCL*/IMC*TIC*ACC +
             /INCL*/IMC*RSFF +
             /INCL*/IMC*/ACC*AD11*TIC*RW


      LMOCL:= /INCL*/IMC*MODCL + /INCL*/IMC*LMOCL*/T64

     /MODCL:= IMC + INCL + /ACC + /TIC*/MODCL + /RW*/MODCL + /AD11*/MODCL

       /RWI:= /ACC*/ARQ*TIC*/RW + ACC*/RWI + ARQ*/RWI + /TIC*/RWI

       /ARQ:= ARQ*PEL + ACC*/ARQ + /ARQ*/TIC + CLMIC

      /RSFF:= /ITRQ + /TIC + /ACC + /RWI*/PEL*/RSFF + INCL + IMC

     IF(VCC) /CLMIC:=/INCL*/IMC*/LMOCL


     DESCRIPTION: MAINBUS PAL FOR FLOPPY DISK CTRL

>ASSEMBLE
```

PAL SOURCE FOR FLOPPY DISK CTRL. CR8062 & CR8047D/010A-/00	sign/date JKH/810921	page 3
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DESCRIPTION: MAINBUS PAL FOR FLOPPY DISK CTRL

```
>ASSEMBLE

PASS
>XPLOT
:P

 00 ---- ---- ---- ---- ---- ---- ---- ----
 01 -X-- ---- X--- ---- -X-X ---- X--- X---
 02 -X-X ---- X--- ---- -X-X ---- ---- X---

 08 -X-- --X- X--- ---- -X-- ---X ---- ----
 09 -X-- ---X X--- ---- -X-- ---- ---- ----
 10 ---- ---- X--- ---- -X-- ---- --X- ----
 11 -X-- -XX- X--- X--- -X-- ---- ---- ----

 16 ---- ---- X--- --X- -X-- ---- ---- ----
 17 ---- ---- X--X ---- -X-- -X-- ---- ----

 24 ---- ---- -X-- ---- ---- ---- ---- ----
 25 ---- ---- ---- ---- X--- ---- ---- ----
 26 ---- --X- ---- ---- ---- ---- ---- ----
 27 X--- ---- ---- ---X ---- ---- ---- ----
 28 ---- X--- ---- ---X ---- ---- ---- ----
 29 ---- ---- ---- -X-X ---- ---- ---- ----

 32 -X-- X-X- ---- ---- ---- ---X ---- ----
 33 ---- ---X ---- ---- ---X ---- ---- ----
 34 ---- ---- ---- ---- ---X --X- ---- ----
 35 X--- ---- ---- ---- ---X ---- ---- ----

 40 ---- ---- ---- ---- ---- --X- X--- ----
 41 ---- ---X ---- ---- ---- ---X ---- ----
 42 X--- ---- ---- ---- ---- ---X ---- ----
 43 ---- ---- ---- ---- ---- ---- ---- --X-

 48 ---- ---- ---- ---- ---- ---- ---- -X--
 49 X--- ---- ---- ---- ---- ---- ---- ----
 50 ---- --X- ---- ---- ---- ---- ---- ----
 51 ---- ---- ---- ---- ---X ---- -X-X ----
 52 ---- ---- ---- ---- X--- ---- ---- ----
 53 ---- ---- -X-- ---- ---- ---- ---- ----

 56 ---- ---- ---- ---- ---- ---- ---- ----
 57 ---- ---- X-X- ---- -X-- ---- ---- ----
```

PAL SOURCE FOR FLOPPY DISK CTRL. CR8062 & CR8047D/010A-/00	sign/date JKH/810921	page 4
	replace	project

```
PRINT
PAL16R4
     CR1504-1 JKH/790924
     FDC,UB1

     /8MHZ /F3 /F2 /F1 CLBY STBY CLIN INCL BST GND
     /OE STPU /BUSY /STIN SI INFF GATE SNDG NC VCC

     /GATE:= F1 + F2 + F3 + /SI*/SNDG

     /SI:= CLIN + GATE*/SNDG + /CLBY*/SI

      STIN:= /SI*/F1*/F2*/F3

     IF(VCC) BUSY:= STBY + /CLBY*BUSY

     IF(VCC) /STPU:= STBY + /BST*/STPU


     DESCRIPTION: INTERRUPTPAL FOR FLOPPY DISK CTRL.

>%PLOT
:P

  16 ---- ---- -%-- ---- ---- ---- ---- ----
  17 ---- -%-- ---- ---- ---- ---- ---- ----
  18 -%-- ---- ---- ---- ---- ---- ---- ----
  19 ---- ---%  ---- ---- ---%  ---- ---- ----

  32 ---- ---- ---- ---- ---- %--- ---- ----
  33 ---- ---%  --%- ---- ---- ---- ---- ----
  34 ---- ---- ---- -%-- ---%  ---- ---- ----

  40 %--- %--- %--- ---- ---%  ---- ---- ----

  48 ---- ---- ---- ---- ---- ---- ---- ----
  49 ---- ---- ---- ---- %--- ---- ---- ----
  50 ---- ---- ---- -%-- ---- ---- ---%  ----

  56 ---- ---- ---- ---- ---- ---- ---- ----
  57 ---- ---- ---- ---- %--- ---- ---- ----
  58 ---- ---- ---- ---- ---- ---- ---- -%-%

>
```

PAL SOURCE FOR FLOPPY DISK CTRL. CR8062 & CR8047D/010A-/00	sign/date JKH/810921	page 5
	replace	project

```
PRINT
PAL16R4
     CR1504-2 JKH/790924
     FDC,UB1

     /8MHZ /F3 /F2 /F1 CLBY STBY CLIN INCL BST GND
     /OE STPU /BUSY /STIN SI INFF GATE SNDG NC VCC

     /GATE:= F1 + F2 + F3 + /SI*/SNDG

     /INFF:= F3*/NC + /F3*/INFF
     /SI:= CLIN + GATE*/SNDG + /CLBY*/SI

      STIN:= /SI*/F1*/F2*/F3

     IF(VCC) BUSY:= STBY + /CLBY*BUSY

     IF(VCC) /STPU:= STBY + /BST*/STPU


     DESCRIPTION: INTERRUPTPAL FOR FLOPPY DISK CTRL.


>%PLOT
*P

 16 ---- ---- -%-- ---- ---- ---- ---- ----
 17 ---- -%-- ---- ---- ---- ---- ---- ----
 18 -%-- ---- ---- ---- ---- ---- ---- ----
 19 ---- ---% ---- ---- ---% ---- ---- ----

 24 -%-% ---- ---- ---- ---- ---- ---- ----
 25 %--- ---- ---- ---% ---- ---- ---- ----

 32 ---- ---- ---- ---- ---- %--- ---- ----
 33 ---- ---% --%- ---- ---- ---- ---- ----
 34 ---- ---- ---- -%-- ---% ---- ---- ----

 40 %--- %--- %--- ---- ---% ---- ---- ----

 48 ---- ---- ---- ---- ---- ---- ---- ----
 49 ---- ---- ---- ---- %--- ---- ---- ----
 50 ---- ---- ---- -%-- ---- ---- ---% ----

 56 ---- ---- ---- ---- ---- ---- ---- ----
 57 ---- ---- ---- ---- %--- ---- ---- ----
 58 ---- ---- ---- ---- ---- ---- ---- -%-%

>
```

6. VERSION DESCRIPTION DOCUMENTS

Dual Bus Version: CSD/005/VDD/0058

Single Bus Version: CSD/005/VDD/ (TBS)

K

TITLE: VERSION DESCRIPTION DOCUMENT FOR FIRMWARE

DOCUMENT NO: CSD/005/VDD/0058

Module: Dual Bus Floppy Disc Controller
Module P/N: 4.04196-o1
Module CR NO.: CR8047M/010AB/00

PREPARED BY: BERTRAM PAASKESEN

APPROVED BY: GOTTLOB BORUP

AUTHORIZED BY: GOTTLOB BORUP

DISTRIBUTION: BBP, GB, PRO(1), TCM, FILE(2)

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CHRISTIAN ROVSING A/S	DOCUMENT CHANGE NOTICE	1. SHEET 1 OF 1	
		DATE 820111	
2. CDC NO.	3. DOCUMENT NO. CSD/005/VDD/0058	4. ISSUE 1	5. DCN NO. 1
6 REL.CAT. ☐ I ☒ II	7. PROJECT.	8. CONTRACT NO.	9. REF. ECO 492

10. DOCUMENT TITLE
VDD for CR8047M/010AB/00

THE DOCUMENT IDENTIFIED IN BLOCKS 3 AND 4 HAS BEEN CHANGED AS SHOWN IN BLOCK 11. THE CHANGED PAGES AUTHORIZED BY THIS DCN ARE ATTACHED. ALL CHANGES AUTHORIZED THROUGH DCN's CONSTITUTE TOGETHER WITH THE ORIGINAL ISSUE SHOWN IN BLOCK 4 THE CURRENT VERSION OF THE DOCUMENT.

11. DOCUMENT CHANGE

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13. PREPARED BY BERTRAM PÅSKESEN	DATE 820111	APPROVED BY	DATE
14. APPROVED BY GOTTLOB BORUP	DATE	APPROVED BY	DATE
15. AUTHORIZED BY GOTTLOB BORUP	DATE	APPROVED BY	DATE

16. DISTRIBUTION GB, BBP, PRO (1), File(2), KFL(4), RA.

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1. SCOPE/IDENTIFICATION

This version description document identifies the content, configuration and related management information for FIRMWARE used in the CR module described on the front page. The configuration management copy of the released FIRMWARE is identified in "Firmware Configuration Data Item List".

FIRMWARE is in this document used as synonym for any Programmed Chip.

1.1 APPLICABLE DOCUMENT

Configuration Control of Firmware
CSD/003/PLN/0002

Version Description Document for Basic Firmware.

K

1.2 INTENDED USE

CR1590-1591	These PAL's 16R4 are used to control the bus switching facilities of the modul.
CR1775	This PAL 16R4 is used to control the interrupt generation, and clock synchronization.
CR1776	This PAL 16R4 interfaces the micro controller to the internal Main Bus.
CR1768-1774	These PROM's 27S25 contain the micro program for the CR8047M/Ø1ØAB/ØØ.

400-769

FIRMWARE CONFIGURATION DATA ITEM LIST

PROGRAMME/PROJECT:
HARDWARE SYSTEM/CONFIGURATION APPLIED FOR TEST/DEMO:

MODULE: ST. FD.CTRL

CR no: 8047M/010AB/00 P/N: 4.04196-01

PROM no. - rev.	DATE (generated)	CASSETTE/DISK designation	CR FIRMWARE Part Number	TEST / DEMO no. and date	SUM check
1768-3	820115	CR/T/0150	5.91768-01	820115	6B65
1769-3	820115	CR/T/0150	5.91769-01	820115	C068
1770-3	820115	CR/T/0150	5.91770-01	820115	05D5
1771-3	820115	CR/T/0150	5.91771-01	820115	3CD7
1772-3	820115	CR/T/0150	5.91772-01	820115	BA11
1773-3	820115	CR/T/0150	5.91773-01	820115	FA56
1774-3	820115	CR/T/0150	5.91774-01	820115	D6BC
1775-2	820112	CR/T/0150	5.91775-01	820115	0B60
1776-1	810505	CR/T/0150	5.91776-01	820115	0C20
1590-01	801211	CR/T/0150	5.91590-01	820115	0988
1591-01	801211	CR/T/1050	5.91591-01	820115	0988

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7. PARTS LISTS

Dual Bus Version:

Parts List, Module Basic:	4.04196-01
Parts List, PCB Basic :	5.04222-00

Single Bus Version:

Parts List, Module Basic:	4.04169-01
Parts List, PCB Basic:	5.04188-00

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CHRISTIAN ROVSING A/S

PARTS LIST
STYKLISTE

Floppy Disk Controller
CR8047D/010AB/00

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Sign. : BBP
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PARTS LIST FOR :
STYKLISTE FOR : 4.04196-01

NEXT HIGHER ASSY:
UNDERPART 1 :

SYSTEM :

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO.	MANUFACT CODE	CR. STOCK NO. CR. LAGER NR.	TOTAL QTY
	FLOPPY DISK CTRL PCB ASSY	K2 - 522		5.04222-00	1
	" " " FRONT PANEL	2-370		5.39246-02	1
	Front modul Mech. kit			5.31705-00	1
	Assembly dwg.	2-274			
	Front panel lay-out dwg.	T2-589			
	" " silkscreen dwg.	S3-207/2			
	" " Drilling dwg.	2-370			

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CHRISTIAN ROVSING A/S	PARTS LIST STYKLISTE	Floppy Disk Controller CR 8047D/010AB/00	Date / Dato : 810501 Issue / Udgave : 1 Sign. : BBP Sheet / Blad 1 of / af 12 sheets / blade

PARTS LIST FOR: STYKLISTE FOR: 5.04222-00	NEXT HIGHER ASSY: UNDERPART 1 : 4.04196-01	SYSTEM:

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO.	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR.	TOTAL QTY
1	Floppy Disk controller PCB	522-1		6.04228-01	
2	Power bus bar 6 pin			6.04701-02	4
3	" " " 14 pin			6.04701-01	2
4	" " " 22 pin			6.04701-00	8
5	Heat sink for Q2 and Q4	4-1025		7.18700-00	1
6	Spacer for Item 5			6.48407-04	2
7	Heat sink for Q1	FGK 5G5		6.18702-00	1
8	socket 24 pin 3 modul Dil. for UG26 — UG38				7
9	socket 40 pin Dil 6M for UE40			6.48301-10	1
10	Jumper 2 pol (Cambion)			6.25500-00	14
11	wire wrap pin SR1-14			6.39901-01	43
12	Ficture for LED			6.19700-00	5
13	spacer for transistors TO-18			6.48401-03	3
14	spacer for transistors TO-39			6.48402-03	1
15	Power Strap SR15-16				2
16	Socket 20 pin 3 modul Dil U				4
17	Screw M2.5 x 8 Phx				4
18	Schnorr Washer S2.5				4
19	Cover for S1			6.49102-03	1
20	Bracket			7.18702-00	1

CHRISTIAN ROVSING A/S

PARTS LIST
STYKLISTE

Floppy Disk Controller
CR8047D/010AB/00

Date / Dato : 810501
Issue / Udgave : 1
Sign. : BBP
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PARTS LIST FOR :
STYKLISTE FOR : 5.042222-00

NEXT HIGHER ASSY:
UNDERPART 1 : 4.04196-01

SYSTEM :

REF.	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO.	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR.	TOTAL QTY
21	Washer 2.5mm.				4
22	Nut M2.5				4
23	stand off pin			6.39901-00	4

CHRISTIAN ROVSING A/S

PARTS LIST
STYKLISTE

Floppy Disk Controller

CR 8047D/010AB/00

Date / Dato : 810501
Issue / Udgave : 1
Sign. : BBP
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PARTS LIST FOR :
STYKLISTE FOR : 5.04222-00

NEXT HIGHER ASSY :
UNDERPART I : 4.04196-01

SYSTEM :

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR.	TOTAL QTY
UA1	Octal Buffer inv.	54S240		6.32207-02	2
UA3	" " non inv.	54S244		6.32313-02	2
UA5	Bus Transceivers	AM2947		6.32477-02	12
UA7	" "	AM2947		6.32477-02	1
UA9	Tripple NAND	S10		6.32119-02	2
UA11	" "	S10		6.32119-02	
UA13	Bus Transceiver	AM2947		6.32477-02	
UA17	Octal Buffer	S240		6.32207-02	
UA19	" " Non inv.	S244		6.32313-02	
UA21	Bus Transceiver	AM2947		6.32477-02	
UA23	" "	AM2947		6.32477-02	
UA25	2 input AND	LS08		6.32115-02	
UA27	Parity checker/generator	82S62		6.32273-02	2
UA29	Bus Transceiver	AM2947		6.32477-02	
UA31	Octal register	S374		6.32297-02	2
UA33	" "	LS374		6.32290-02	3
UA37	2-input AND Driver	N38		6.32279-02	3
UA39	2-input NAND Driver	N38		6.32279-02	
UA41	" " " "	N38		6.32279-02	
UA43	Octal Buffer	LS240		6.32287-02	1
UA45	" " non inv.	LS241		6.32288-02	1

CHRISTIAN ROVSING A/S	PARTS LIST STYKLISTE	Floppy Disk Controller CR 8047D/010AB/00	Date / Dato : 810501 Issue / Udgave : 1 Sign. : BBP Sheet / Blad 4 of / af 12 sheets / blade

PARTS LIST FOR : STYKLISTE FOR : 5.04222-00	NEXT HIGHER ASSY : UNDERPART 1 : 4.04196-01	SYSTEM :

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR	TOTAL QTY
UC1	AND-NOR	S51		6.32143-02	2
UC3	Bus Transceiver	AM2947		6.32477-02	
UC5	Octal bus driver	LS244		6.32373-02	2
UC7	Bus Transceiver	AM2947		6.32477-02	
UC9	dual Retrigable one-shot	LS123		6.32431-02	
UC13	Bus Transceiver	AM2947		6.32477-02	
UC17	AND-NOR	S51		6.32143-02	
UC19	Bus Transceiver	AM2947		6.32477-02	
UC21	Octal bus driver	LS244		5.32273-02	
UC23	Bus Transceiver	AM2947		6.32477-02	
UC25	Octal D-FF	LS377		6.32250-02	2
UC27	Parity-checker/generator	82562		6.32273-02	
UC29	Bus Transceiver	AM2947		6.32477-02	
UC31	Octal D-FF 3-state	S374		6.32297-02	
UC33	" " "	LS374		6.32290-02	
UC35	2-input NOR	LS02		6.32105-02	
UC37	2-input XOR	LS86		6.32153-02	
UC41	9-input AOI-gate	LS54		6.32144-02	
UC43	dual JK	LS112		6.32157-02	

CHRISTIAN ROVSING A/S

PARTS LIST
STYKLISTE

Floppy Disk Controller

CR 8047D/010AB/00

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PARTS LIST FOR :
STYKLISTE FOR : 5.04222-00

NEXT HIGHER ASSY:
UNDERPART 1 : 4.04196-01

SYSTEM :

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR	TOTAL QTY
UD1	PAL (6.32410-02)	CR 1590		5.91590-01	1
UD3	Dual D-FF	LS74		6.32148-02	4
UD5	Dual input NAND driver	S38		6.32141-02	2
UD7	Address comparator	25LS2521		6.32323-02	2
UD9	2-input NAND Driver	LS38		6.32286-02	2
UD13	PISO Shift-register	LS165		6.32416-02	1
UD17	PAL (6.32410-02)	CR1591		5.91591-01	1
UD19	Dual D-FF	LS74		6.32148-02	
UD21	2-input NANS Driver	S38		6.32141-02	
UD23	Address comparator	25LS2521		6.32323-02	
UD25	Quad 3-state buffer	LS125		6.32404-02	1
UD27	Selector	LS157		6.32178-02	1
UD31	Hex D-FF	LS174		6.32197-02	1
UD33	1Kx8 SRAM NB! LATCH TYPE	MK4118-3		6.32239-02	1
UD37	Octal D-FF	LS374		6.32290-02	
UD39	Octal D-FF	LS377		6.32250-02	
UD41	Dual IK-FF	LD112		6.32157-02	
UD43	Counter	LS163		6.32187-02	1

CHRISTIAN ROVSING A/S

PARTS LIST
STYKLISTE

Floppy Disk Controller

CR 8047D/010AB/00

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PARTS LIST FOR :
STYKLISTE FOR : 5.04222-00

NEXT HIGHER ASSY :
UNDERPART 1 : 4.04196-01

SYSTEM :

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR	TOTAL QTY
UE9	Voltage comparator	8212		6.32314-02	2
UE11	Quad NPN TRANSISTOR	MHQ4013		6.32486-02	1
UE13	" PNP "	MHQ3467		6.32487-02	1
UE23	Dual D-FF	LS74		6.32148-02	
UE17	Dual IK-FF	S112		6.32158-02	
UE19	PAL 16R4 (6.32410-02)	CR1775-01		5.91775-00	1
UE21	Dual IK-FF	S112		6.32158-02	3
UE25	Hex inverter	LS04		6.32112-07	1
UE27	Micro Sequenzer	2910		6.32369-02	1
UE30	ALU	2901		6.32368-02	2
UE33	ALU	2901		6.32368-01	
UE36	Octal buffer inv.	LS240		6.32287-02	
UE38	Octal buffer inv.	LS240		6.32287-02	
UE40	Floppy Disk formatter	FD1791		6.32438-02	1
UF17	PAL 16R6 (6.32411-02)	CR1776-01		5.91775-00	1
UF19	Quad XOR	S86		6.32154-02	1
UF21	Quad NOR	S02		6.32106-02	1
UF23	Schmidt-NAND	LS132		6.32159-02	2
UF43	Dual D-FF	LS74		6.32148-02	

CHRISTIAN ROVSING A/S

PARTS LIST
STYKLISTE

Floppy Disk Controller

CR 8047D/010AB/00

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PARTS LIST FOR :
STYKLISTE FOR : 5.04222-00

NEXT HIGHER ASSY :
UNDERPART 1 : 4.04196-01

SYSTEM :

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR.	TOTAL QTY
UG7	Voltage regulator	SG 1532		6.32484-02	1
UG27	PROM (6.32394-02)	27S25	CR1768-01	5.91768-01	1
UG29	" (6.32394-02)	27S25	CR1769-01	5.91769-01	1
UG31	" (6.32394-02)	27S25	CR1770-01	5.91770-01	1
UG33	" (6.32394-02)	27S25	CR1771-01	5.91771-01	1
UG35	" (6.32394-02)	27S25	CR1772-01	5.91772-01	1
UG37	" (6.32394-02)	27S25	CR1773-01	5.91773-01	1
UG39	" (6.32394-02)	27S25	CR1774-01	5.91774-01	1
UG11	Voltage comparator	8212		6.32314-02	
UG13	Schmidt NAND	LS132		6.32159-02	
UG15	Quad NAND driver	LS38		6.32286-02	
UG17	Dual IK-FF	S112		6.32158-02	
UG19	Quad NAND	S00		6.32103-02	1
UG21	Counter	LS393		6.32435-02	1

CHRISTIAN ROVSING A/S	PARTS LIST STYKLISTE	Floppy Disk Controller CR 8047D/010AB/00	Date / Dato : 810501 Issue / Udgave : 1 Sign. : BBP Sheet / Blad 8 of / af 12 sheets / blade

PARTS LIST FOR : STYKLISTE FOR : 5.04222-00	NEXT HIGHER ASSY : UNDERPART 1 : 4.04196-01	SYSTEM :

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR	TOTAL QTY
R1-R8	Carbon resistor 2K2 0,125W 5 % 3M			6.44710-36	19
R9-R11	Resitor wire wund 8R2 2W 5 % 12M			6.44749-02	3
R12-R13	" " " OR016 4W 5 % 12M			6.44749-01	2
R14-R17	" Carbon 150R 0,125W 5 % 3M			6.44710-22	14
R18-R19	" " 1K 0,125W			6.44710-32	23
R20	" " 15R			6.44710-10	1
R21	" MF 1K00 0,125 1 % 6M			6.44731-25	1
R22	" " 1K47 0,125 6M			6.44731-41	1
R23	Carbon resistor TBD				
	NTC "				
R25	Carbon resistor "				
R26	" " 680R 0,125W 5 % 3M			6.44710-30	1
R27	" " 4K7 0,125W 5 % 3M			6.44710-40	4
R28	" " 2K2 0,125W 5 % 3M			6.44710-36	
R29	" " 270K 0,125W 5 % 3M			6.44710-61	1
R30	" " 4K7 0,125W 5 % 3M			6.44710-40	
R31	" " 2K2 0,125W 5 % 3M			6.44710-36	
R32-R33	" " 4K7 0,125W 5 % 3M			6.44710-40	
R34	" " 330R 0,125W 5 % 3M			6.44710-26	1
R35	" " 390R 0,125W 5 % 3M			6.44710-27	1
R36	" " 2K2 0,125W 5 % 3M			6.44710-35	
R37	" " 18K 0,125W 5 % 3M			6.44710-47	1

CHRISTIAN ROVSING A/S	PARTS LIST STYKLISTE	Floppy Disk Controller CR 8047D/010AB/00	Date / Dato : 810501 Issue / Udgave : 1 Sign. : BBP Sheet / Blad 9 of / af 12 sheets / blade

PARTS LIST FOR: STYKLISTE FOR: 5.04222-00	NEXT HIGHER ASSY: UNDERPART 1 : 4.04196-01	SYSTEM:

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO.	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR.	TOTAL QTY
R38	Resistor Carbon film 470K 0,125W 5 % 3M			6.44710-64	1
R39	" " " 1K 0,125W 5 % 3M			6,44710-32	
R40	" " " 4K7 0,125W 5 % 3M			6.44710-40	
R41	" " " 120R 0,125W 5 % 3M			6.44710-21	1
R42-R44	" " " 2K2 0,125W 5 % 3M			6.44710-36	
R45-R47	" " " 100R 0,125W 5 % 3M			6.44710-20	1
R48	" " " 470R 0,125W 5 % 3M			6.44710-28	1
R49	" " " 1KΩ 0,125W 5 % 3M			6.44710-32	
R50	Potentiometer 5KΩ TO5			6.44767-02	2
R51	" 5KΩ TO5			6.44767-02	
R53	Resistor carbon film 330Ω 0,5W 5 % 5M			6.44727-26	1
R52	" " " 47R 0,125W 5 % 3M			6.44710-16	1
R54	" " " 3K9 0,125W 5 % 3M			6.44710-39	1
R55	" " " 1R5 0,125W 5 % 3M			6.44710-83	2
R56	" " " 4R7 0,125W 5 % 3M			6.44710-04	1
R57-58	" " " 1R5 0,125W 5 % 3M			6.44710-83	
R59-60	" " " 12K 0,125W 5 % 3M			6.44710-45	2
R61	" " " 1K 0,125W 5 % 3M			6.44710-32	
R62-65	" " " 2K2 0,125W 5 % 3M			6.44710-36	
R66-73	" " " 1K 0,125W 5 % 3M			6.44710-32	
R74-83	" " " 150R 0,125W 5 % 3M			6.44710-22	
R84-85	" " " 1K 0,125W 5 % 3M			6.44710-32	

CHRISTIAN ROVSING A/S

PARTS LIST
STYKLISTE

Floppy Disk Controller

CR 8047D/010AB/00

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PARTS LIST FOR :
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NEXT HIGHER ASSY :
UNDERPART 1 : 4.04196-01

SYSTEM :

REF	DESCRIPTION BESKRIVELSE					MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR	TOTAL QTY
R86-87	Resistor carbon film	10K	0,125W	5 %	3M			6.44710-44	2
R88	" " "	1K	0,125W	5 %	3M			6.44710-32	
R89	" " "	10K	0,125W	5 %	3M			6.44710-44	
R90-91	" " "	1K	0,125W	5 %	3M			6.44710-32	
R92	Resistor Thick film	2K2	0,2W	2 %	Sil			6.44751-24	1
R93	" carbon "	2K2	0,125W	5 %	3M			6,44710-36	
R94	" " "	1KΩ	0,125W	5 %	3M			6.44710-32	
R95	" " "	2K2	0,125W	5 %	3M			6.44710-36	
R96	" " "	1K	0,125W	5 %	3M			6.44710-32	
R97	" " "	1K	0,125W	5 %	3M			6.44710-32	
R98	" " "	1K	0,125W	5 %	3M			6.44710-32	
R99	" " "	1K	0,125W	5 %	3M			6.44710-32	
R100	" " "	1K	0,125W	5 %	3M			6.44710-32	
R101	" " "	2K2	0,125W	5 %	3M			6.44710-24	
R102	" " "	2K2	0,125W	5 %	3M			6.44710-24	
R103	RESISTOR CARBON FILM	10R	0,125W	5 %	3M			6.44710-08	2
R104	RESISTOR CARBON FILM	56R	0,125W	5 %	3M			6.44710-17	2
R105	RESISTOR CARBON FILM	10R	0,125W	5 %	3M			6.44710-08	
R106	RESISTOR CARBON FILM	56R	0,125W	5 %	3M			6.44710-17	
R107	RESISTOR CARBON FILM	4R7	0,25W	5 %	5M			6.44720-04	2
R108	RESISTOR CARBON FILM	4R7	0,25W	5 %	5M			6.44720-04	
R109-115	RESISTOR CARBON FILM	2K2	0,125W	5 %	3M			6.44710-24	

CHRISTIAN ROVSING A/S

PARTS LIST
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Floppy Disk Controller

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PARTS LIST FOR :
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NEXT HIGHER ASSY
UNDERPART 1 : 4.04196-01

SYSTEM :

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR LAGER NR.	TOTAL QTY
C20-88	Capacitor ceramic 22nF 50V 20 % 3M			6.05313-02	63
C1-C9	Capacitor tantalium 4µ7 35V 10 % 9M			6.0524-37	9
C10	" ceramic 2,7nF 50V 20 % 2M			6.05313-02	2
C12	" " 2,7nF 50V 20 % 2M			6.05313-02	
C13-15	" " 1nF 50V 20 % 2M			6.05318-25	2
C89-C90	" " 100pF 50V 20 % 3M			6.05310-19	2
C11	" " 100nF 50V 20 % 3M			6.05311-30	1
DS1	LED GREEN			6.08790-01	1
DS2	LED RED			6.08790-02	
DS3	LED Yellow	CQY-97		6.08790-03	3
DS4	LED Yellow			6.08790-03	
DS5	LED Yellow			6.08790-03	
S1	Switch 8 bil Dil			6.49101-01	1

CHRISTIAN ROVSING A/S

PARTS LIST
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Floppy Disk Controller

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NEXT HIGHER ASSY :
UNDERPART 1 : 4.04196-01

SYSTEM :

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR	TOTAL QTY
Q5	Transistor NPN TO-18	2N2222A		6.51210-00	2
Q6	" " TO-18	2N2222A		6.51210-00	
Q7	TRANSITOR NPN TO-39	2N2219		6.51212-00	2
Q8	TRANSITOR NPN TO-39	2N2219		6.51212-00	
Q4	Transistor PNP TO-18	2N2907		6.51211-00	1
Q1	" NPN TO-39	BLY68		6.51241-00	1
Q2	" PNP TO-3	2N6377		6.51240-00	2
Q3	" PNP TO-3	2N6377		6.51240-00	
CR8	Diode NB' 5M	1N4148		6.08701-00	1
CR9	"	1N5614		6.03705-00	2
CR10	"	1N5614		6.08705	
CR1	" VSK 120	1N5817		6.08708-00	4
CR2	" VSK 120	1N5817		6.08708-00	
CR4	" VSK 120	1N5817		6.08708-00	
CR5	" VSK 120	1N5817		6.08708-00	
CR3	"	1N4148		6.08701-00	5
CR6	"	1N4148		6.08701-00	
CR7	"	1N4148		6.08701-00	
VR1	Zener Diode 9V1 400mW 5 %			6.08760-16	1
CR11	DIODE	1N4148		6.08701-00	
CR12	DIODE	1N4148		6.08701-00	

CHRISTIAN ROVSING A/S	PARTS LIST STYKLISTE	F.D. CONTROLLER CR8047 D/ 010A-/00	Date / Dato : 800922 Issue / Udgave : 1 Sign. : TLJ Sheet 1 of 1 sheets Blad 1 af 1 blade

PARTS LIST FOR :
STYKLISTE FOR : 4.04169-01

NEXT HIGHER ASSY :
UNDERPART 1 :

SYSTEM :

REF.	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO.	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR.	TOTAL QTY
	FDC BASIC PCB ASSY 476 - 1			5.04188-00	1
	FDC FRONT PANEL	2 - 370		5.39247-02	1
	BUSHING	4 - 1013		7.04701-00	2
	FINGERSCREW	4 - 1014		7.47102-00	2
	SIDE RAIL *			6.02701-00	1
	SIDE RAIL *			6.02701-00	1
	REAR SUSPENSION BAR	2 - 273		7.02711-00	1
	MOULDING	4 - 1018		7.32704-01	6
	SCREW 2.5MG x 6, CROSS RECESS				8
	SCREW 2.5MG x 5, C.H.				11
	WASHER				11
	FRONT PANEL SILKSCREEN	S3 - 207			
	ASSEMBLY DRAWING	2 - 274			
	* NOTE THE EDGE SHAPING				
	SHOWN IN DRAWING NO. 2 - 274				

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CHRISTIAN ROVSING A/S

PARTS LIST
STYKLISTE

F.D. CONTR. BOARD ASSY.
SINGLE BUS

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PARTS LIST FOR :
STYKLISTE FOR : 50418800

NEXT HIGHER ASSY : CR8047D/010A-/00
UNDERPART 1 : 40416901

SYSTEM :

REF.	DESCRIPTION / BESKRIVELSE	MANUFACTURERS PART NO / LEVERANDØRS PART NO.	MANUFACT. CODE	CR. STOCK NO. / CR. LAGER NR.	TOTAL QTY
1	Printed Circuit Board	476		604188XX	1
2	Stand. off pins for F1 og F2			63990100	4
3	Power Bus BAR			60470100	5
XUA1	Socket 20 pin DIL 3M			64830105	2
XUB1	Socket 20 pin DIL 3M				
XUE16	Socket 40 pin DIL 6M			64830110	1
XUG1	Socket 22 pin DIL 4M			64830106	7
XUG3	Socket 22 pin DIL 4M				
XUG5	Socket 22 pin DIL 4M				
XUG7	Socket 22 pin DIL 4M				
XUG9	Socket 22 pin DIL 4M				
XUG11	Socket 22 pin DIL 4M				
XUG13	Socket 22 pin DIL 4M				

CHRISTIAN ROVSING A/S

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F.D. CONTR. BOARD ASSY.
SINGLE BUS

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PARTS LIST FOR:
STYKLISTE FOR: 50418800

NEXT HIGHER ASSY: CR8047D/010A-/00
UNDERPART 1 : 40416901

SYSTEM:

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR.	TOTAL QTY
UA1	Octal Buffer 3 state	S 244		63321302	1
3	Octal Inverter Buffer 3 state	S 240		63220702	1
5	PAL CR	PAL 16R6		63241102	1
7	Octal D Flip Flop	LS 377		63225002	2
9		LS 2521		63232302	1
11	OCTAL D Flip Flop	S 374		63229702	2
13		S 374			
15	OCTAL Inverter Buffer 3 state	LS 240		63228702	3
17	Octal Buffer 3 state	LS 241		63228802	1
19	Quad. 2 input Nand. Buffer	38		63227902	3
21	4 Wide 2 & 3 Input And or Invert	LS 54		63214402	1
UB1	PAL CR	PAL 16R4		63241002	1
3	Quad 2 input Nand Buffer	S 38		63214102	1
5	Dual JK Flip Flop	S 112		63215802	1
7	Quad 2 input Exclusive or	S 86		63215402	1
9	8 input Multiplexer	S 151		63217002	1
11	Octal D Flip Flop	LS 374		63229002	3
13		LS 374			
15		LS 374			
17		38			
19	Dual JK Flip Flop	LS 112		63215702	2

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CHRISTIAN ROVSING A/S

PARTS LIST
STYKLISTE

F.D. CONTR. BOARD ASSY.
SINGLE BUS

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PARTS LIST FOR:
STYKLISTE FOR: 50418800

NEXT HIGHER ASSY: CR1047D/010A-/00
UNDERPART 1 : 40 16901

SYSTEM:

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR.	TOTAL QTY
UB21		38			
UC 3	Hex Inverter Schmitt Trigger	LS 14		632125-02	1
5	Hex Inverter	06		63222402	1
7	Dual Binary Ripple Counter	LS 393		63243502	1
12	RAM 1024x8	MK4118		63239602	1
15	Quad 2 Input NOR	LS 02		63210502	1
17	Synchronous 4 bit Binary Counter	LS 163		63218702	1
19		LS 377			
21	Dual D Flip Flop	LS 74		63214802	1
UD 3	Quad 2 to 1 Multiplexer	LS 157		63217802	1
5	Quad 2 Input Nand	S 00		63210302	1
11	Voltage Comparator	ICL8212		63231402	2
13		ICL8212			
15	Hex D Flip Flop	LS 174		63219702	1
17		LS 112			
UE 1	Hex Inverter	LS 04		63211207	1
3	Controller	Am 2910		63236902	1
6	4 Bit Slice	Am 2901		63236802	2

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CHRISTIAN ROVSING A/S

PARTS LIST
STYKLISTE

F.D. CONTR. BOAID ASSY.
SINGLE BUS

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PARTS LIST FOR:
STYKLISTE FOR: 50418800

NEXT HIGHER ASSY: CR8047D/010A-/00
UNDERPART 1 : 40-16901

SYSTEM:

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR.	TOTAL QTY
UE 9	4 Bit Slice	Am 2901			
12		LS 240			
14		LS 240			
16	Floppy Disc Controller	FD 1791			1
19	Quad 2 Input Nand	LS 00		63210202	1
21	Dual D Flip Flop	S 74		63214902	1
UF21	4 Bit Shift Register	LS 195			1
UG 1	PROM	27S27		63237002	7
3	PROM	27S27			
5	PROM	27S27			
7	PROM	27S27			
9	PROM	27S27			
11	PROM	27S27			
13	PROM	27S27			
21	Quad 2 Input Exclusive or	LS 86		63215302	1

400 - 716

CHRISTIAN ROVSING A/S

PARTS LIST
STYKLISTE

F.D. CONTR. BOARD ASSY.
SINGLE BUS

Date / Dato 800513
Issue / Udgave 1
Sign. : EC
Sheet / Blad 5 of / af 7 sheets / blade

PARTS LIST FOR:
STYKLISTE FOR: 50418800

NEXT HIGHER ASSY: CR8047D/010A-/00
UNDERPART 1 : 40416901

SYSTEM:

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR.	TOTAL QTY
R1	2,2K SIL			64475124	1
R2-R8	1K 1/8W			64471032	12
R9	10K TRIMPOT				1
R10	5K TRIMPOT			64476009	1
R11	18K 1/8W			64471047	1
R12	470K 1/8W			64471064	2
R13	2,2K 1/8W			64471036	4
R14-R15	4,7K 1/8W			64471040	3
R16	470K 1/8W				
R17	2,2K 1/8W				1
R18	2,7K 1/8W			64471037	3
R19	10K 1/8W			64471044	1
R21	27K 1/8W			64471049	1
R22	470K 1/8W			64471028	
R23	2,2K 1/8W				
R24	1K 1/8W				
R25	2,2K 1/8W				
R26-R29	12K 1/8W			64471045	4
R30-R39	150 1/8W			64472522	11
R40-R42	1K 1/8W				
R43-R44	10K 1/8W				
R45-	1K 1/8W				

CHRISTIAN ROVSING A/S

PARTS LIST
STYKLISTE

F.D. CONTR. BOARD ASSY.
SINGLE BUS

Date / Dato 800513
Issue / Udgave 1
Sign. : EC
Sheet 6 of 7 sheets
Blad af blade

PARTS LIST FOR:
STYKLISTE FOR: 50418800

NEXT HIGHER ASSY: CR8047D/010A-/00
UNDERPART 1 : 40416901

SYSTEM:

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR LAGER NR.	TOTAL QTY
R46	4,7K 1/8W				
R47	120 1/4W			64472521	1
R48	150 1/4W				
S1	SWITCH 8 Pole DIL			64910103	1
XS1	SWITCH COVER			64910203	1
DS1	LED GREEN	CQY 95		60879001	1
DS2	LED RED	CQY 54-2		60879002	1
CR1	DIODE	1N5614			2
CR2	DIODE	1N5614			
CR3	DIODE	1N4148		60870100	1
VR1	ZENER DIODE 9,1V	BZX55C-9V1		60876016	1

CHRISTIAN ROVSING A/S

PARTS LIST
STYKLISTE

F.D. CONTR. BOARD ASSY.
SINGLE BUS

Date / Dato 800513
Issue / Udgave 1
Sign. : EC
Sheet / Blad 7 of / af 7 sheets / blade

PARTS LIST FOR:
STYKLISTE FOR: 50418800

NEXT HIGHER ASSY: CR8047D/010A-/00
UNDERPART 1 : 40416901

SYSTEM:

REF	DESCRIPTION BESKRIVELSE	MANUFACTURERS PART NO LEVERANDØRS PART NO	MANUFACT. CODE	CR. STOCK NO. CR. LAGER NR.	TOTAL QTY
C1-C2	2,7 nF Ceramic			60531045	2
C3	100 nF Ceramic			60531130	2
C4-C7	1 nF Ceramic			60531037	4
C8	100 nF Ceramic				
C9	4,7 uF 50V Tantal			60532537	1
C10-C13	4,7 uF 10V Tantal			60532137	4
C14-C62	22 nF Ceramic			60531302	48
Q1		2N3700		65121500	4
Q2		2N2907		65121100	1
Q3-Q5		2N3700			
F1	FUSE 10A	PICO		61510110	1
F2	FUSE 0,5A	PICO		61510101	1

400-716

8. DRAWINGS

Front Panel Layouts:

Dual Bus Version	T2-589
Single Bus Version	T2-588

Dual Bus Version:

Blocked Schematic:	1-275
Assembly Drawing Basic PCB:	K2-522

Single Bus Version:

Blocked Schematic:	1-207
Assembly Dwg. basic PCB:	K2-476

Assembly Drawing Module	2-274

DO NOT SCALE

CHRISTIAN ROVSING A/S

ST FD CTRL CR 8047 /010AB/00	Scale		Approved	Issue	1	2	
	Date	81-01-12	E	Date	81-01-12	82-02-15	
	Drawn	BBP/JFL		Approved		JFL	
Front panel	Parts no	5-39240-02	T2-589				
Lay-out	Print no		Sheet 1 of 1 sheets				

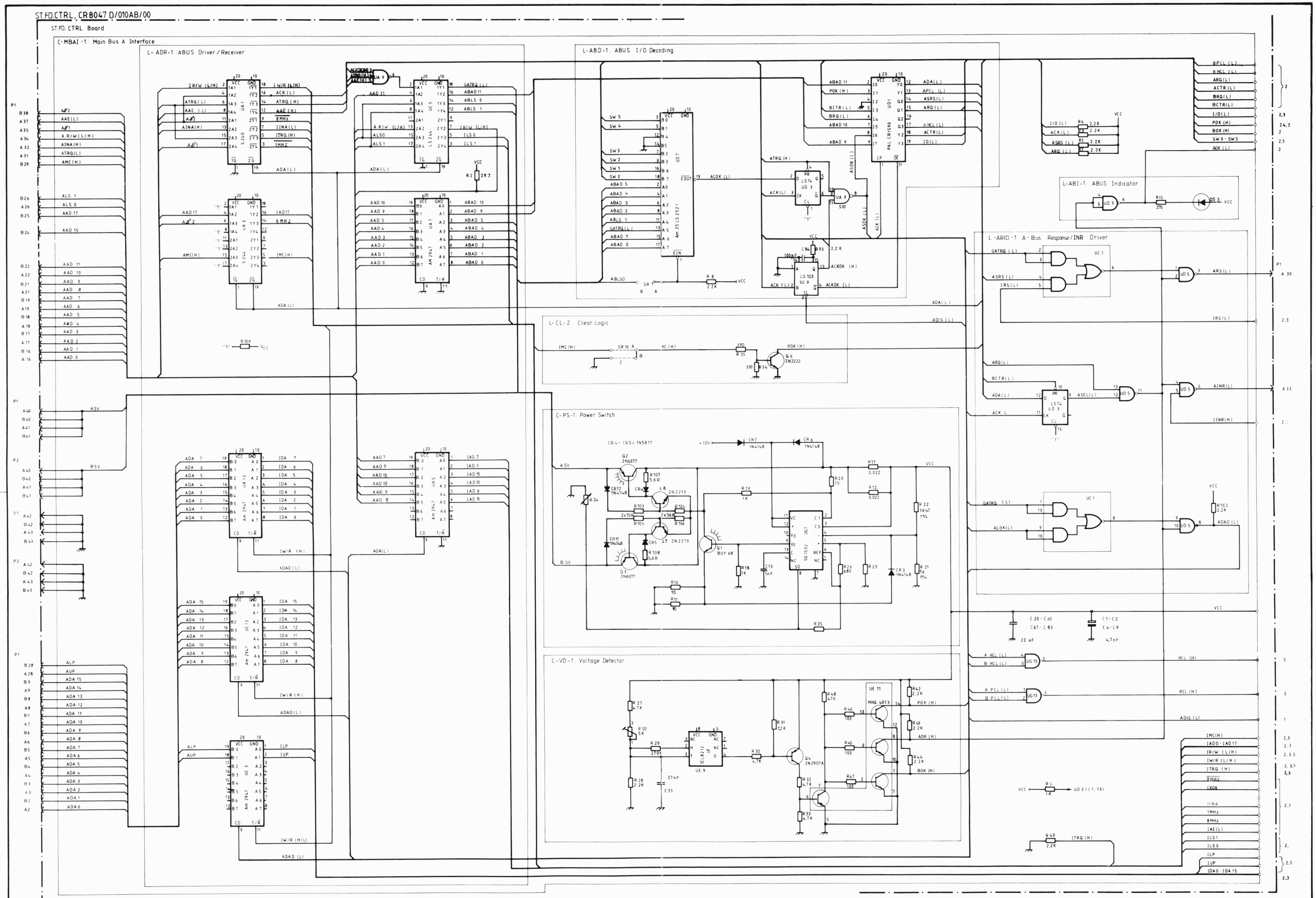
DO NOT SCALE

CHRISTIAN ROVSING A/S

Floppy Disk CTRL,CR8047 /010A-00 Front Panel	Scale		Approved		Issue	1	2
	Date	81-01-06	E		Date	81-01-06	82-01-25
	Drawn	BBP/ MZL			Approved	BD	BP/MZL
	Parts no		T2-588				
Lay-Out	Print no		Sheet 1 of 1 sheets				

ST.FD.CTRL., CR8047 D/010AB/00

ST.FD. CTRL Board



CHRISTIAN ROVSING A/S

ST. FD. CTRL. CR 8047D / 010 AB/00
Floppy CTRL Board
Main Bus A Interface
Blocked Schematic

Scale		Approved	
Date	81-01-15	E	
Drawn	BBP/JFL		
Parts no		1 - 275	
Print no	522	Sheet 1 of 4 sheets	

Issue	1	2
Date	81-01-15	81-05-26
Approved	BBP	BBP/JFL

LU/821030

ST.FD CTRL, CR8047 D/010AB/00

ST.FD CTRL Board

C-MBBI-1: Main Bus B Interface

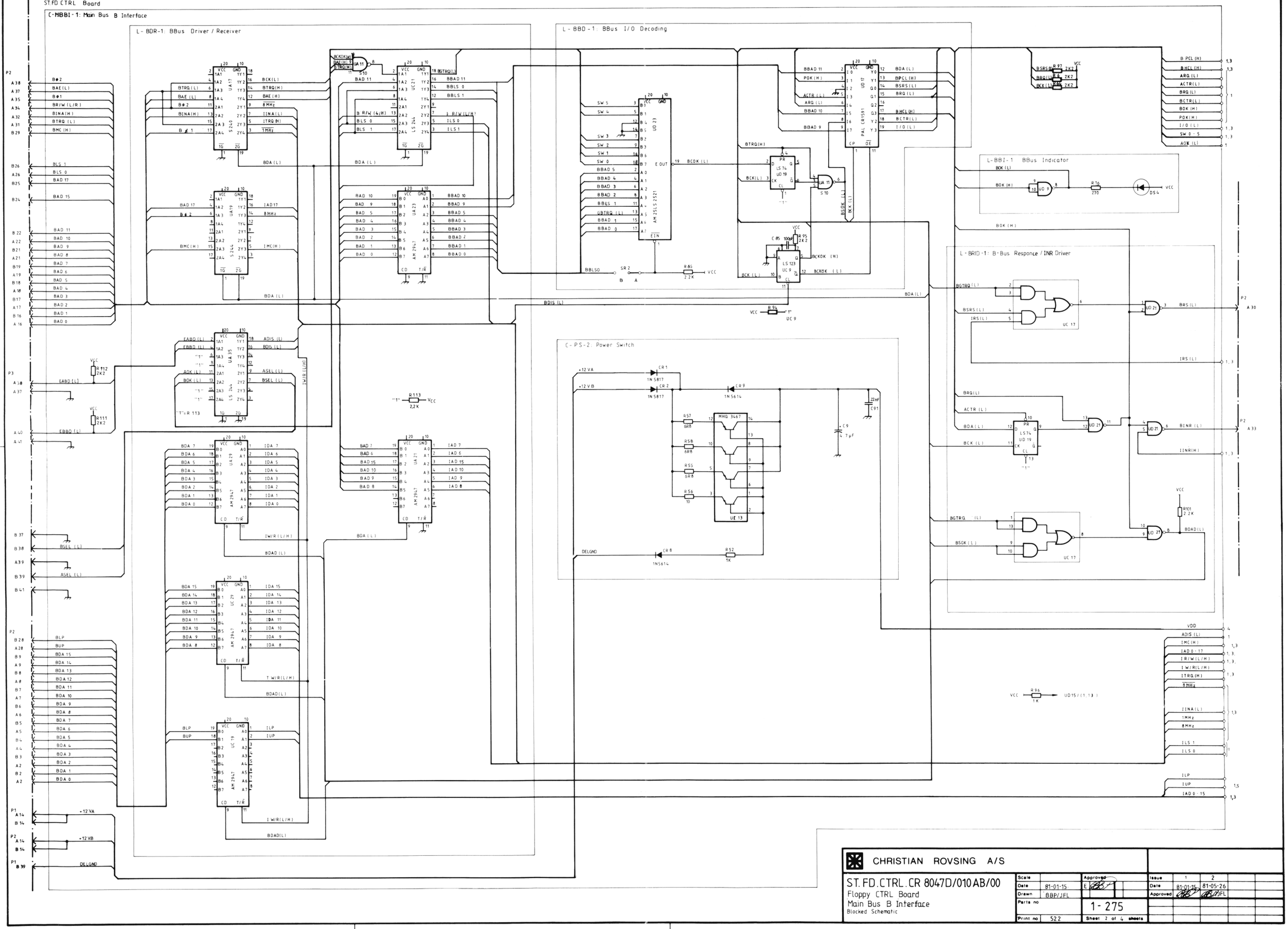
L-BDR-1: BBus Driver / Receiver

L-BBD-1: BBus I/O Decoding

L-BBI-1 BBus Indicator

L-BRID-1: B-Bus Responce / INR Driver

C-PS-2: Power Switch



CHRISTIAN ROVSING A/S

ST.FD.CTRL.CR 8047D/010AB/00
Floppy CTRL Board
Main Bus B Interface
Blocked Schematic

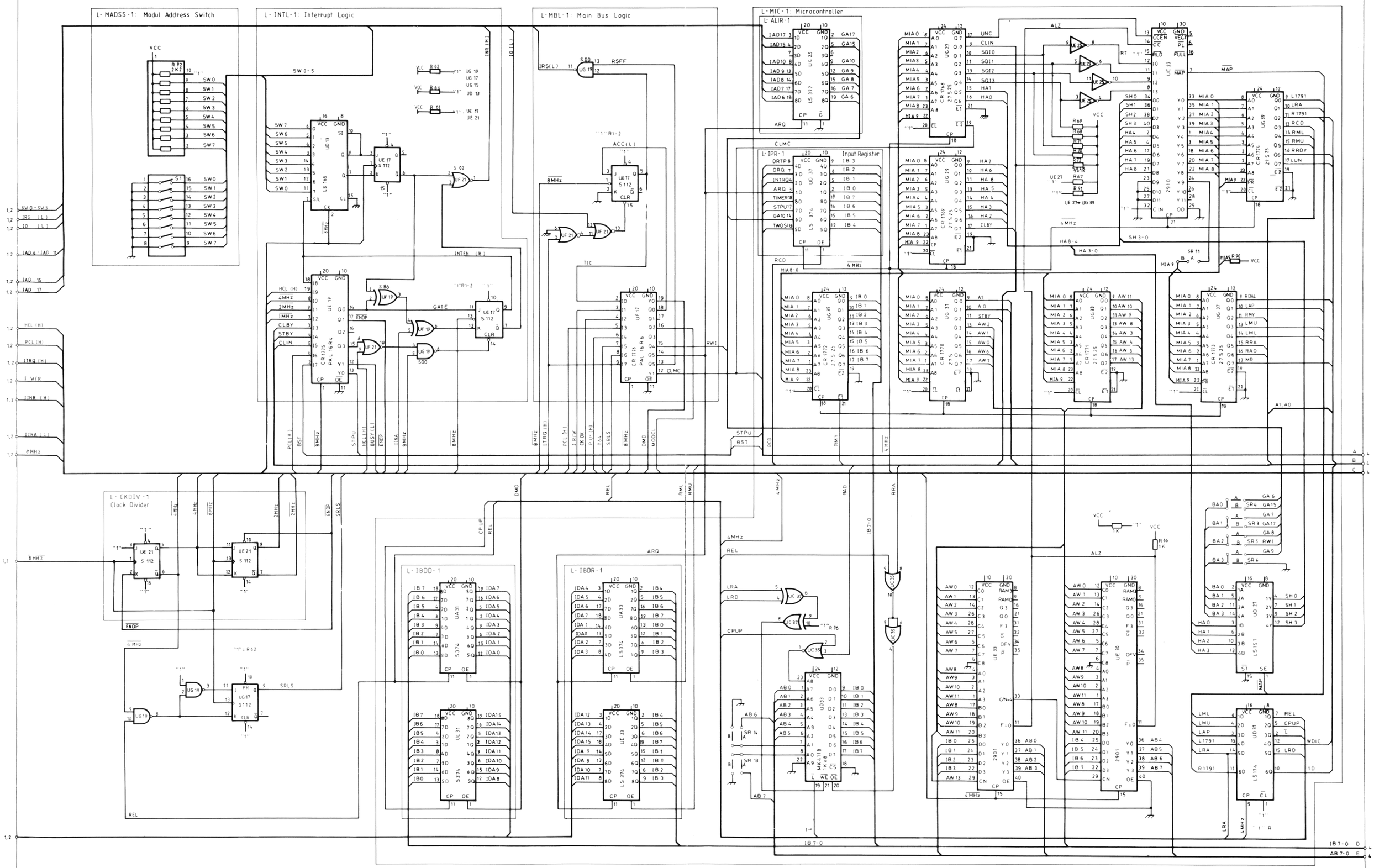
Scale		Approved	
Date	81-01-15	E	
Drawn	BBP/JFL		
Parts no		1-275	
Print no	522	Sheet 2 of 4 sheets	

Issue	1	2	
Date	81-01-15	81-05-26	
Approved		JFL	

LU/821030

ST. FD. CTRL., CR 8047D / 010AB/00

ST. FD. CTRL. Board



CHRISTIAN ROVSING A/S

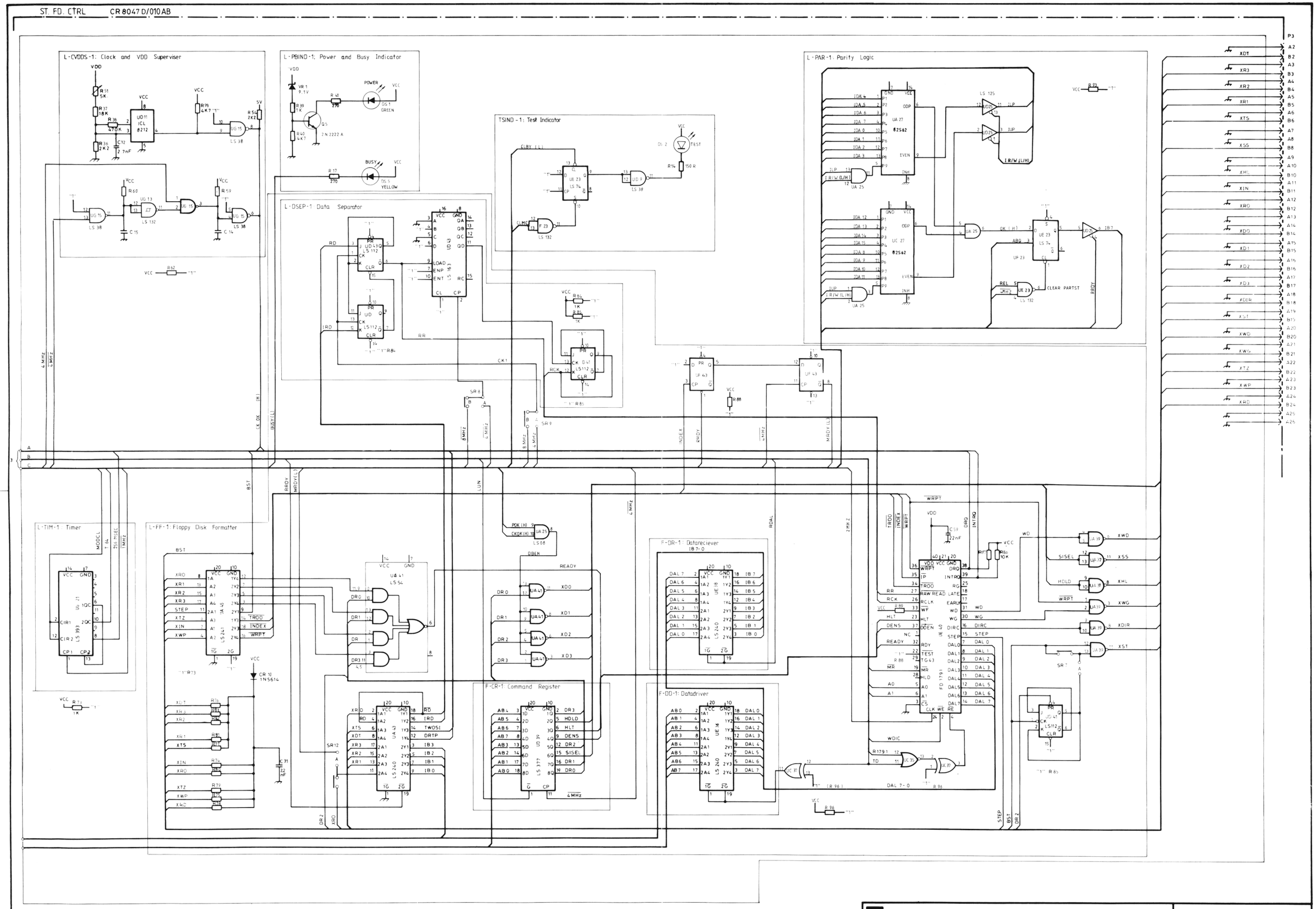
ST. FD. CTRL. CR 8047D / 010 AB / 00

Floppy Disk Controller

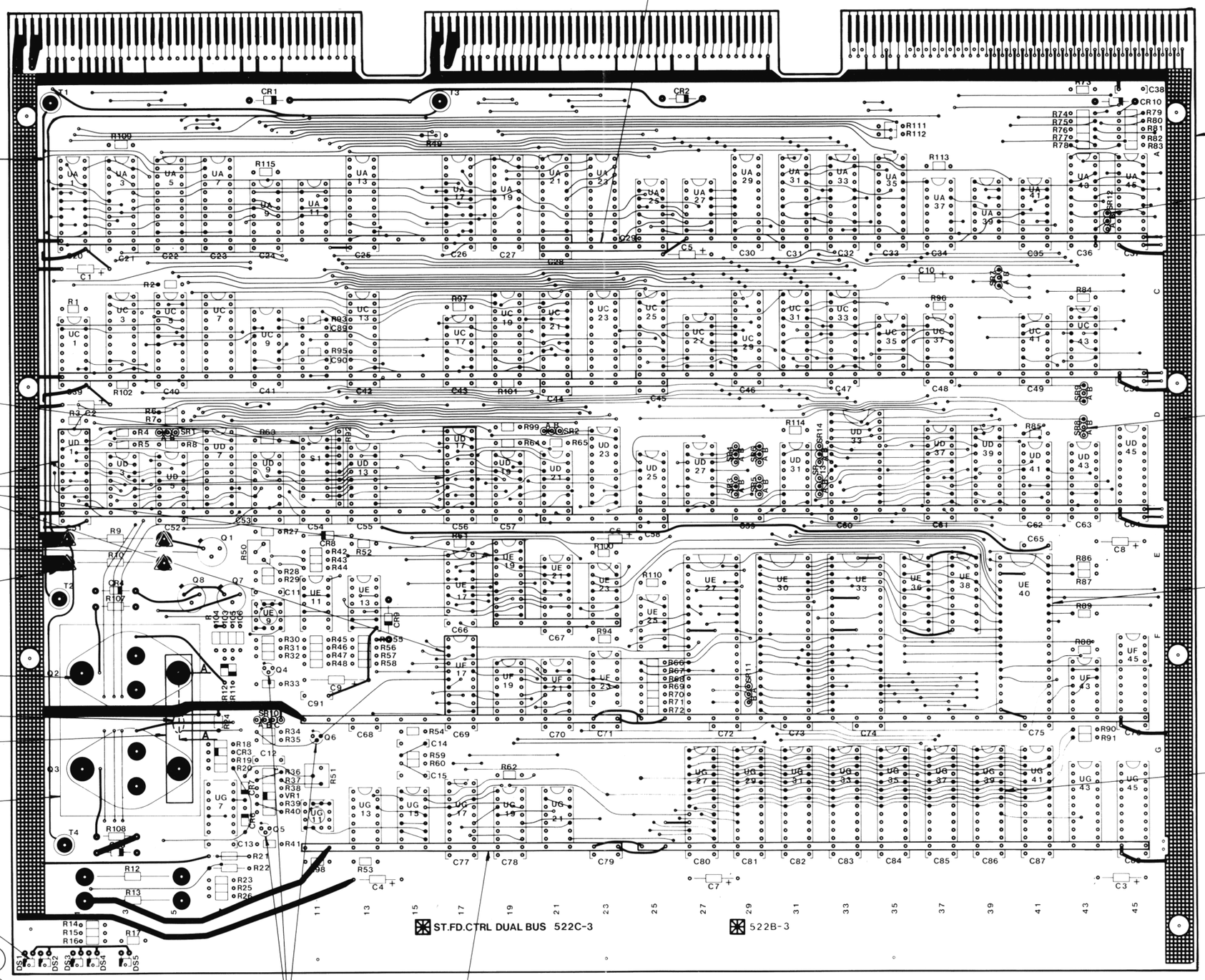
Blocked Schematic

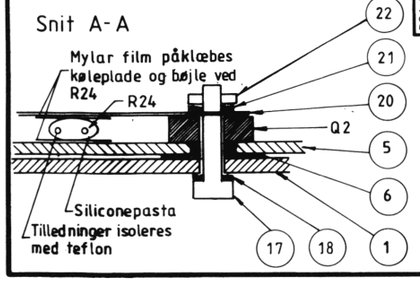
Scale		Approved	Issue 1 / 2
Date	81-01-15	E	Date 81-01-15 / 81-05-26
Drawn	BBP/JFL		Approved MZL
Parts no		1 - 275	
Print no	522	Sheet 3 of 4 sheets	

LU/821030


L-CVDDS-1: Clock and VDD Superviser
L-PBIND-1: Power and Busy Indicator
TSIND-1: Test Indicator
L-PAR-1: Parity Logic
L-DSEP-1: Data Separator
L-TIM-1: Timer
L-FF-1: Floppy Disk Formatter
F-DR-1: Datareciever
F-CR-1: Command Register
F-DD-1: Datadriver
CHRISTIAN ROVSING A/S
ST. FD. CTRL. CR 8047D/010 AB/00
Formatter/Drive Interface
Blocked Schematic
Scale
Date 81-01-15
Drawn BBP/JFL
Parts no
Print no 522
Approved
1-275
Sheet 4 of 4 sheets
Issue 1 2
Date 81-01-15 81-05-26
Approved JFL

LU/821030





Fotomal mellem pasmærker 375,3

CHRISTIAN ROVSING A/S

ST. FD. CTRL DUAL BUS, CR8047 / 010AB/00

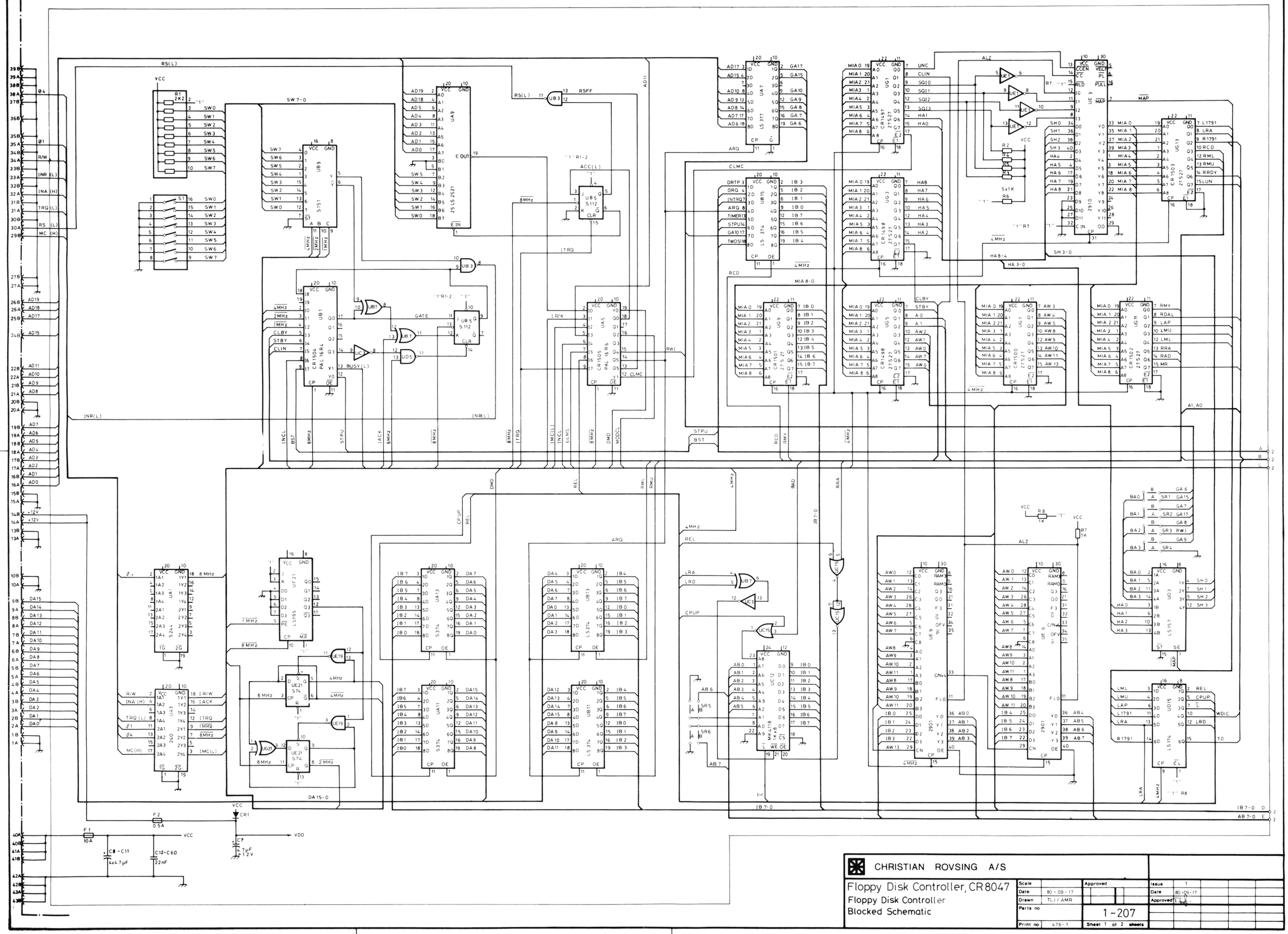
ST. FD. Ctrl. Dual Bus Board

Assembly Dwg.

Scale	1:1	Approved		Issue	1	2	3 / 4
Date	81-07-17	E		Date	81-07-21		81-07-17 / 82-02-15
Drawn	BBP/MM			Approved	BBP/LLA		MM / GFL
Parts no	5.04222-03	K2-522					
Print no	522-3	Sheet 1 of 1 sheets					

LU/821030

Floppy Disk Controller, CR8047D



CHRISTIAN ROVSING A/S

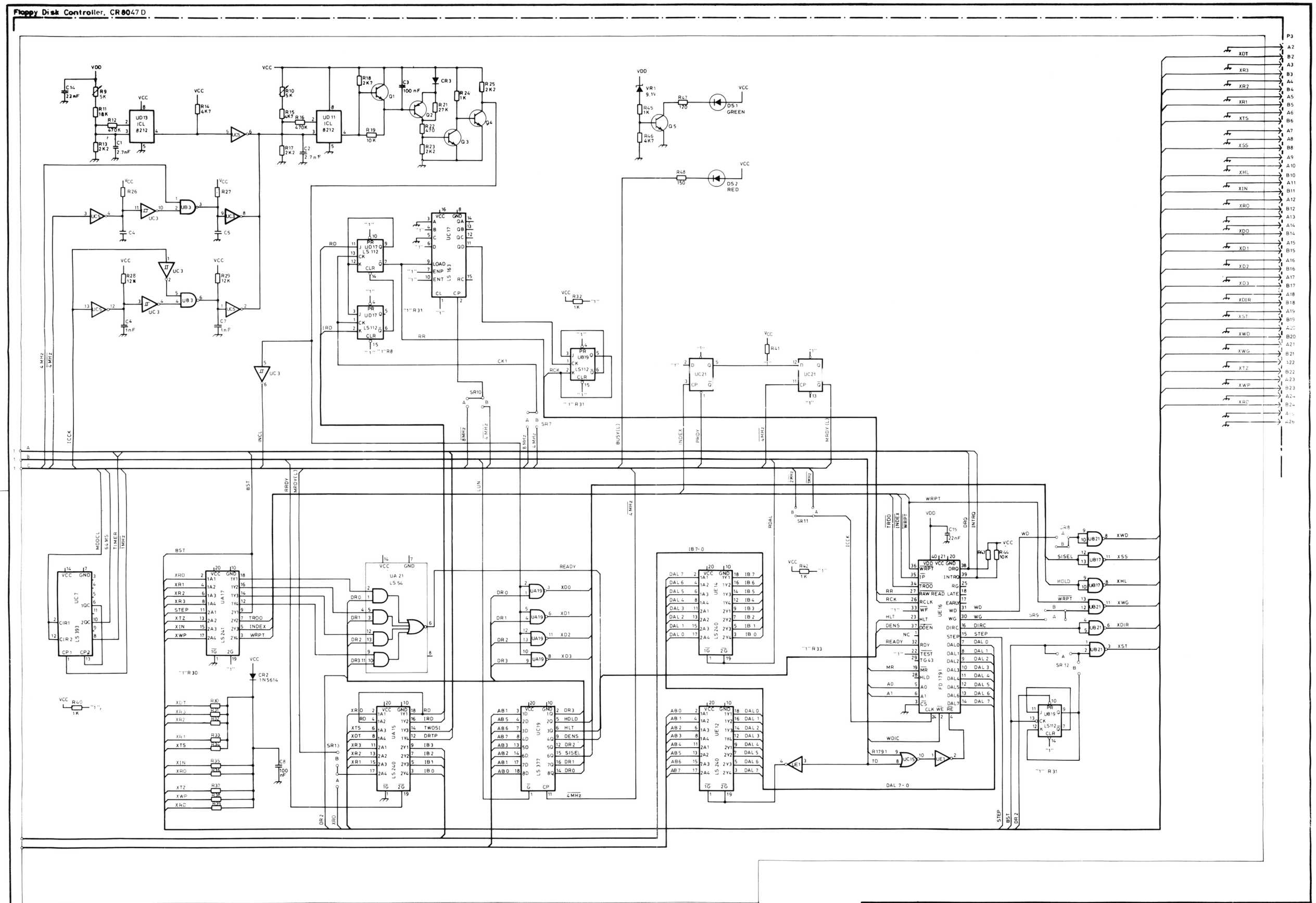
Floppy Disk Controller, CR8047
Floppy Disk Controller
Blocked Schematic

Scale		Approved	
Date	80-09-17		
Drawn	TLJ / AMR		
Parts no		1-207	
Print no	476-1	Sheet 1 of 2 sheets	

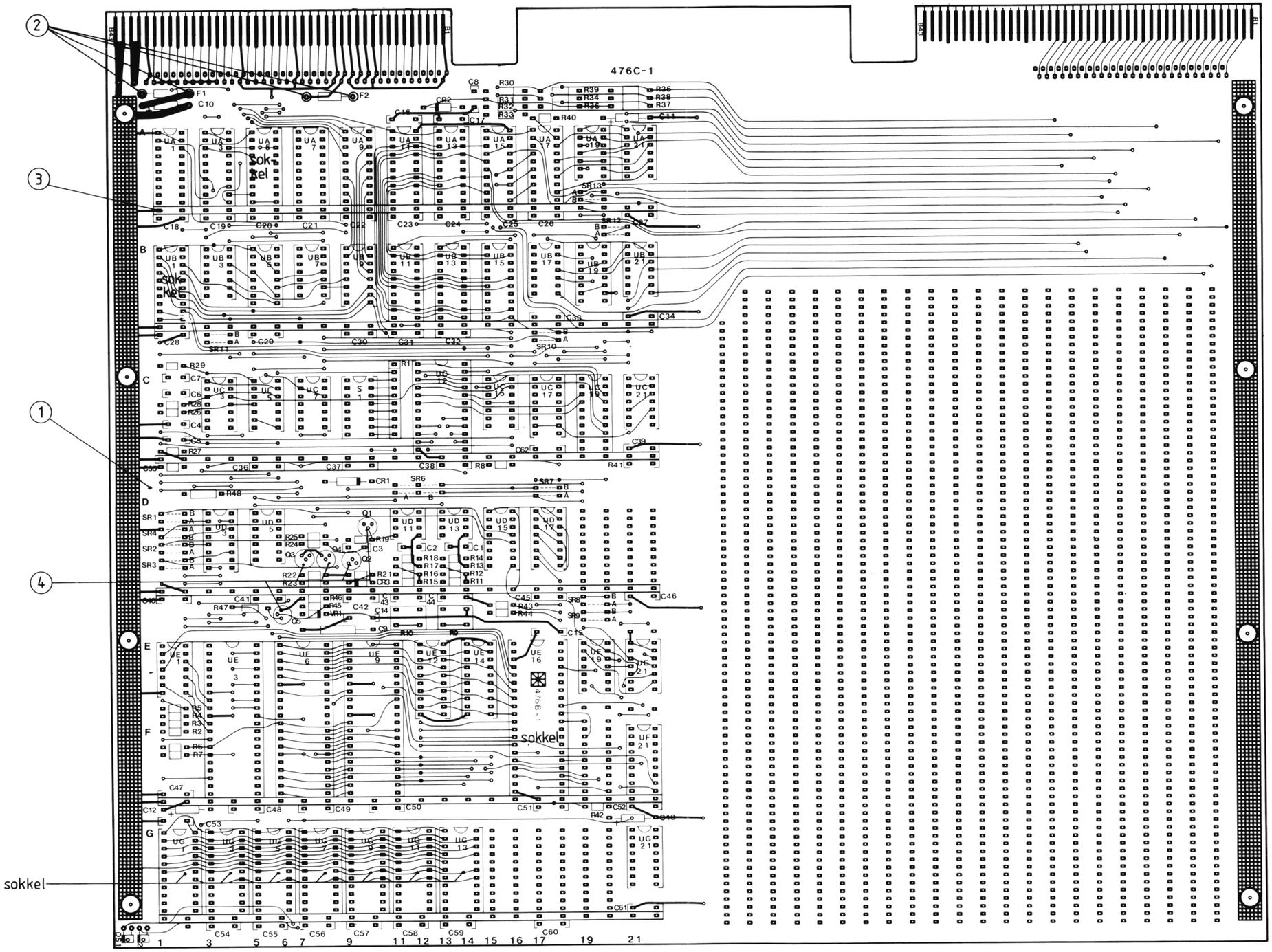
Issue	1
Date	80-09-17
Approved	

LU/821030

Floppy Disk Controller, CR8047 D



LU/821030



CHRISTIAN ROVSING A/S

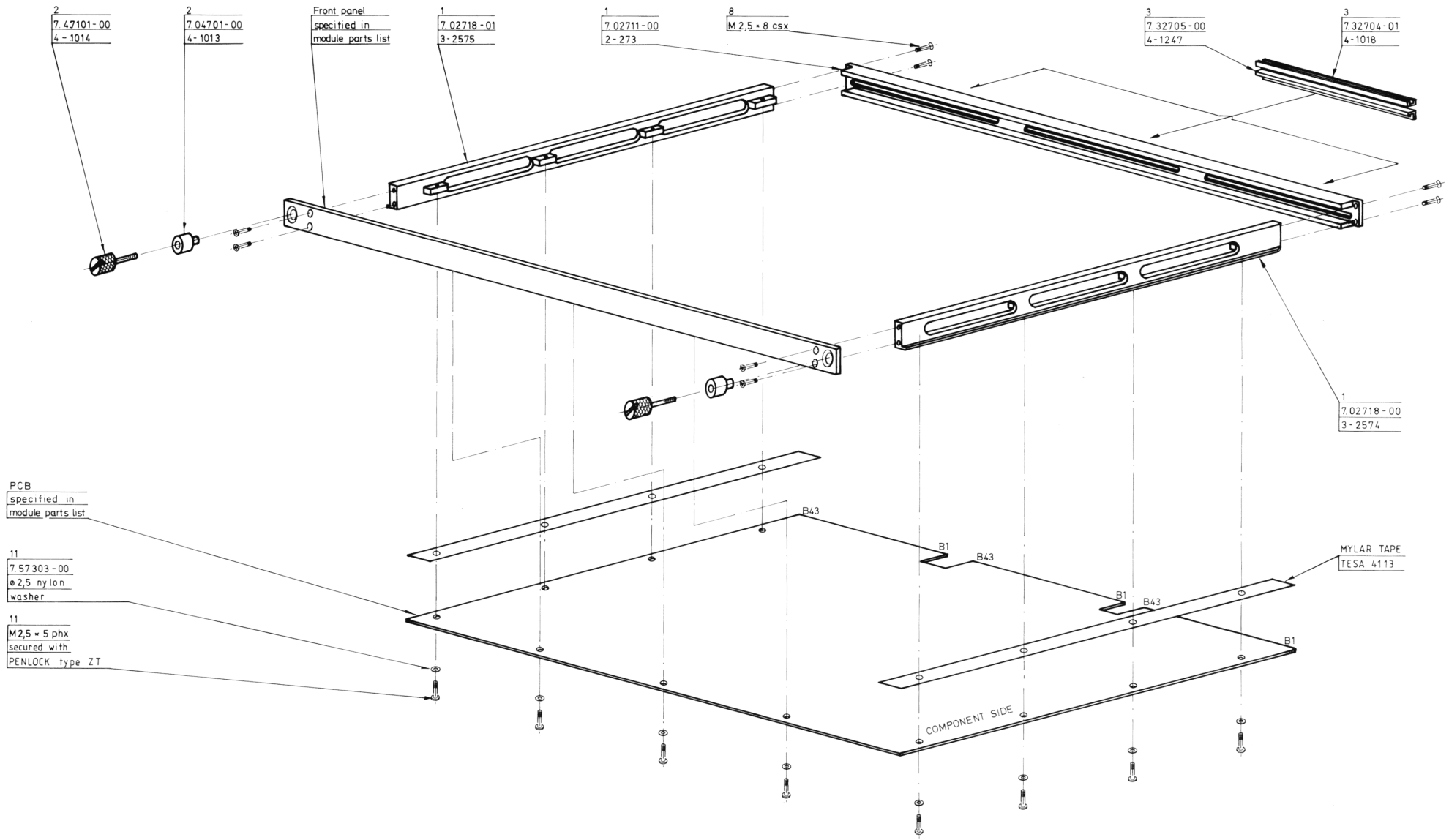
Floppy Disk Controller, CR8047
FDC Board

Assembly Dwg.

Scale	1 : 1	Approved	
Date	80-09-11	E	
Drawn	TLJ/MM		
Parts no		K2 - 476	
Print no	476-1	Sheet 1 of 1 sheets	

Issue	1
Date	80-09-11
Approved	TRG

LU/821030



CHRISTIAN ROVSING A/S

Front PCB module
Mechanics

General assembly drawing

Scale		Approved		Issue	1 / 2
Date	80 05 28			Date	81 03 25 / 82-08-02
Drawn	BST / MS			Approved	BH / BSt /MZL
Parts no	5.31705 -00	2-274			
Print no		Sheet 1 of 1 sheets			

LU/821030