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IML501
Reference Manual

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Abstract:

This publication is a reference manual of an Image Load Module designed for the RC850 display unit.

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1. IML501 DESCRIPTION 1.

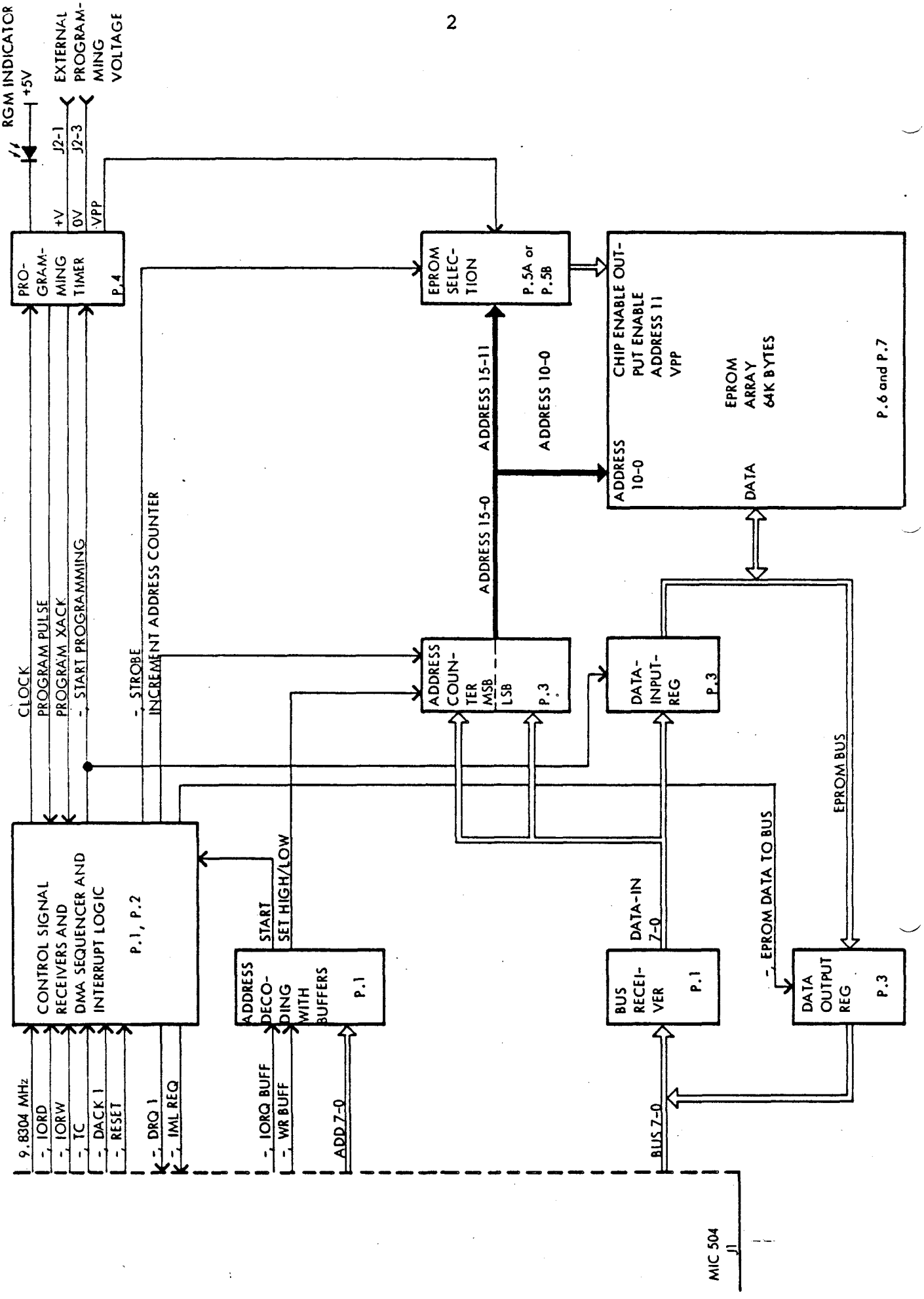
The IMage Load module contains 64K byte of EPROM memory (UV erasable prom memory), and connects to MIC504 via JACK 1.

The IML501 is intended for use in the RC855 stand-alone Display Terminal. In the stand-alone version there are no down-load possibilities from external sources (e.g. floppy-disc or transmission lines), instead IML501 is used. During power-up software in IML501 is moved to Display Terminal ram memory by means of a bootstrap located on MIC504 printed circuit board.

The EPROM's located on the IML module may be programmed while located on the printed circuit board, if an external programming voltage is connected to JACK 2.

IML501 contains a 16-bits address counter, which is loaded with the start address of the EPROM memory. 2 standard I/O instructions (OUT <dev.no.>) are used to load LS-byte and the MS-byte of this address counter. Once the start address is loaded, the transfer to/from Display Terminal ram memory is started by means of a third I/O instruction.

Transfer to/from ram memory is executed using DMA-controller channel 1, which must be initialized with a ram memory start address and a byte count. When IML501 is started the transfer of information between the EPROM's and the ram memory takes place without the engagement of the Z80 processor. The transfer continues until byte count is zero, at that time the Z80 software is interrupted via CTC channel 3.



81.09.09 VH 81.09.09 ABP

2. HOW TO PROGRAM EPROM'S ON IML501 2.

EPROM's on IML501 may be programmed while located on the printed circuit board. An external programming voltage is needed to do this. The programming voltage connects to JACK 2:

External programming voltage for PCB's mounted with 2532/2732 EPROM's is 26V $\pm$ 0V5.
POW206 with CBL700 may be used.

External programming voltage for PCB's mounted with 2732A EPROM's is 22V $\pm$ 0V2.
POW206 with CBL700 may be used.

CAUTION: PROGRAMMING MUST ONLY TAKE PLACE UNDER THE ASSISTANCE OF AUTHORIZED SERVICE PERSONNEL, SINCE IT IS NECESSARY TO HAVE THE DISPLAY TERMINAL COVER REMOVED DURING PROGRAMMING.

2.1 Strapping Possibilities 2.1

EPROM module is designed to use three types of EPROM's:

- TEXAS 2532 or equivalent
- INTEL 2732/2732A or equivalent

INTEL and TEXAS types are, however, not completely pin compatible, so 5 strap positions have been introduced, Pos. 25, Pos. 26, Pos. 27, Pos. 28, and Pos. 29.

Strapping is executed by means of three strap-platforms and two IC's (74LS138), which are mounted as indicated in fig. 2.1. See also fig. 2.2.

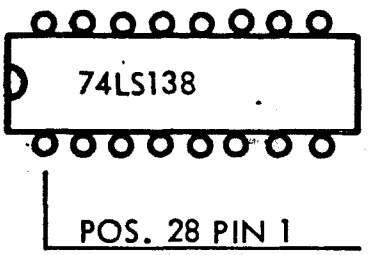
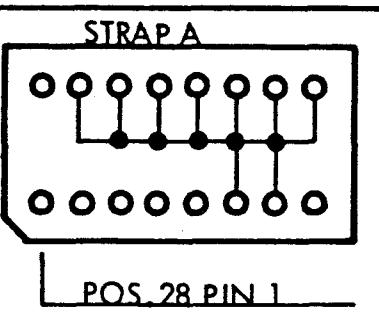
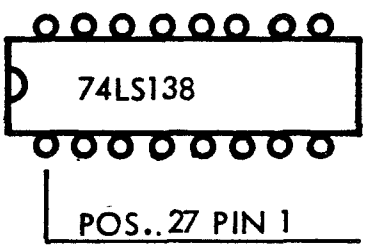
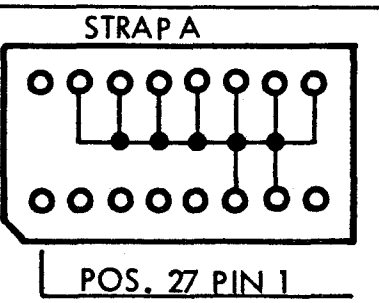
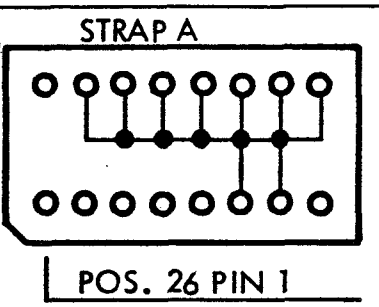
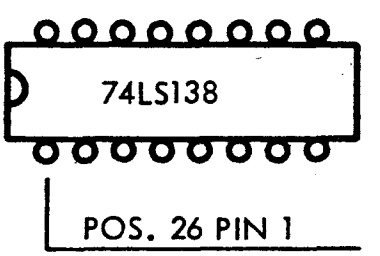
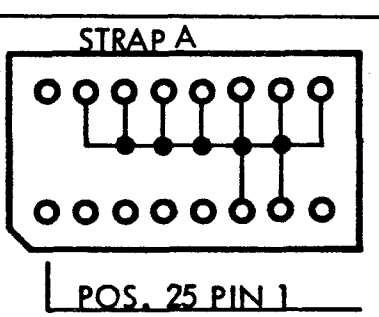
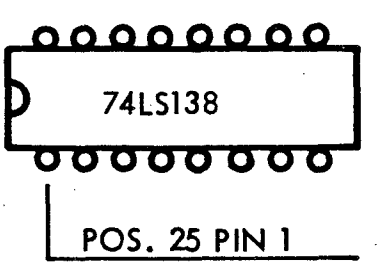
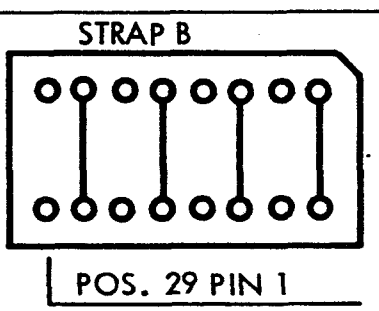
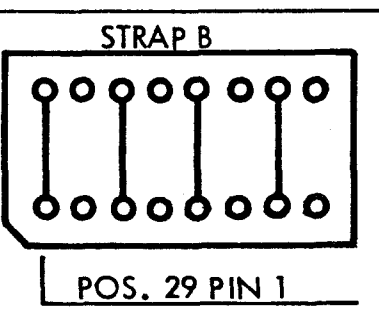
STRAP POSITION	PROGRAM, VERIFY AND READ 2532	PROGRAM, VERIFY AND READ 2732/2732A
28		
27		
26		
25		
29		

Fig. 2.1

IML 501 Straps

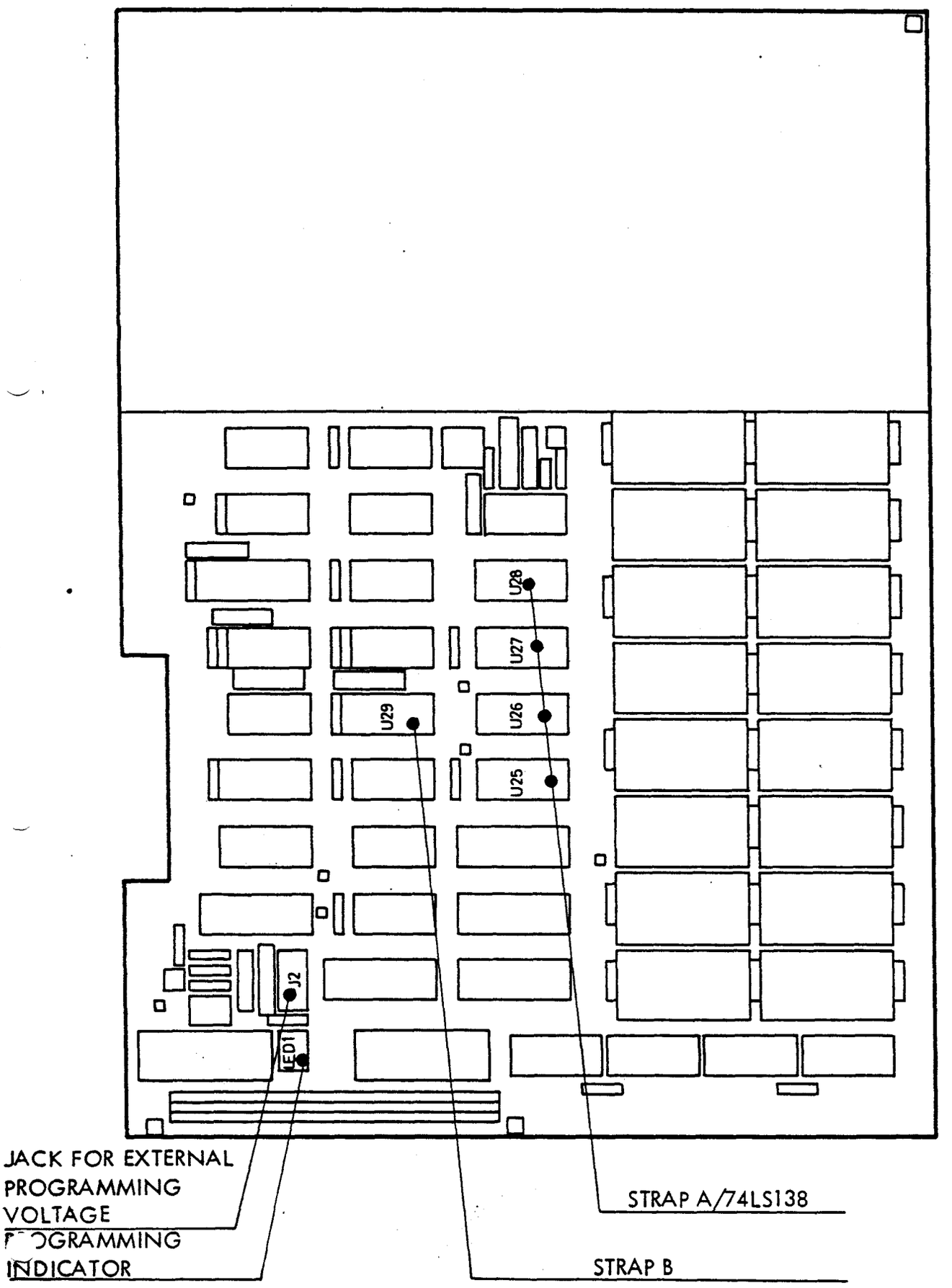


Fig. 2.2
IML501 LAYOUT

To change strapping from one EPROM type to another, do as follows:

1. Turn the 16-pins strap-platform B in POS. 29 180 degrees.

2. Interchange strap-platforms A by IC's 74LS138.

CAUTION: IT IS EMPHASIZED THAT DAMAGE OCCURS TO THE EPROM'S AND THE IC'S 74LS138 IF THE STRAPPING DOES NOT CORRESPOND TO THE EPROM'S USED.

2.2 Programming Procedure

Following general procedure is recommended when programming the EPROM module:

1. Install the required number of EPROM's in the EPROM sockets. Refer to fig. 2.2.

   Be careful not to bend EPROM pins while mounting EPROM's. When EPROM's have been installed, check that no pins are bent.

2. Check that straps for EPROM's correspond to the EPROM type used. Fig. 2.1.

3. Turn Display Unit power off.

4. Install IML501 in the Display Unit.

5. Turn Display Unit power on.

CAUTION: DO NOT TURN DISPLAY POWER ON AND OFF WHILE THE EXTERNAL PROGRAMMING VOLTAGE IS CONNECTED TO JACK 2.

To avoid unintentional programming of the EPROM's the external programming voltage should not be connected to IML501 until application software, which is going to be programmed into the EPROM's, and suitable programming software has been loaded.

6. Connect external programming voltage to IML501 JACK 2. PGM indicator should now be illuminated.

CAUTION: EXTERNAL PROGRAMMING VOLTAGE FOR PCB'S MOUNTED WITH 2532/2732 EPROM'S IS 26V $\pm$ 0V5. POW206 WITH CBL700 MAY BE USED FOR PROGRAMMING. REMEMBER TO PLACE THE POW206 SWITCH IN POSITION + 26V.

EXTERNAL PROGRAMMING VOLTAGE FOR PCB'S MOUNTED WITH 2732A EPROM'S IS 22V $\pm$ 0V2. POW206 WITH CBL700 MAY BE USED FOR PROGRAMMING. REMEMBER TO PLACE THE POW206 IN POSITION + 22V.

7. Start programming software. PGM indicator should now begin to gleam.

When programming is finished the PGM indicator will no longer gleam.

8. Disconnect external programming voltage immediately after the programming is finished.

It is recommended that the programming software verifies the EPROM contents for all "1"'s before the programming is initiated.

Immediately following the programming of one cell the programming software should verify that the programming was successful, if not the cell should be re-programmed. If the programming is not successful after three attempts to re-program the EPROM in question is probably defect.

When programming of the required EPROM area is finished the EPROM contents should be compared with the contents of the original data area to verify correct programming.

3. HOW TO USE IML501 3.

IML501 utilizes three I/O device numbers, the function of which is listed in the table below.

Device Number	Instr.	Function
38_H	OUT <38>	This instruction terminates all IML501 activity and places IML501 in a well defined state. Besides this the IML501 address counter most significant byte is loaded. ADDRESS REG. (MSB) := BUS (7:0). Bit 7 is most significant bit.
39_H	OUT <39>	ADDRESS REG. (LSB) := BUS (7:0).
$3A_H$	OUT <3A>	Start DMA transfers on DMA channel 1.

Programming Example

After initialization of the CTC and the DMA the following should be performed, notice that low byte must be loaded first:

```
lda 'low byte' ; low byte in register A
out 39H        ; set low byte in IML501 address counter
lda 'high byte'; high byte in register A
out 38H        ; set high byte in IML501 address counter,
                 and clear IML501
out 3AH        ; start DMA channel 1 transfer
```

3.1 DMA Use 3.1

The IML501 controller uses the DMA channel 1 for DMA transfers to/from the memory.

How to address the DMA confer description of DMA in RC850 Controller Reference Manual, chapter 4, [1].

DMA Initialization

The 'command register' should be reinitialized as described in the RC850 Controller Reference Manual, chapter 4, [1].

DMA Channel 1 Use

When a transfer to or from the IML501 is wanted the following should be performed:

.set mode register as follows:
    select channel 1
    read or write transfer,
    Single mode
    Address increment/decrement

.set base address and
.set base word count

as follows:

```
lda ...          ; set register A to mode register content
out FB           ; write register A to mode register
out FC           ; clear internal flip/flop
                 ; set base address
lda 'low byte'   ; low byte in register A
out F2           ; set low byte of base address
lda 'high byte'; high byte in register A
out F2           ; set high byte of base address

out FC           ; clear internal flip/flop
                 ; should not be necessary
                 ; set base byte count
lda 'low byte'   ; set 'low byte' of byte count
out F3           ;
lda 'high byte'; set 'high byte' of byte count
out F3           ;
```

When this is performed the DMA channel 1 is waiting for a kick to get started. This kick is received when the IML501 start port is accessed.

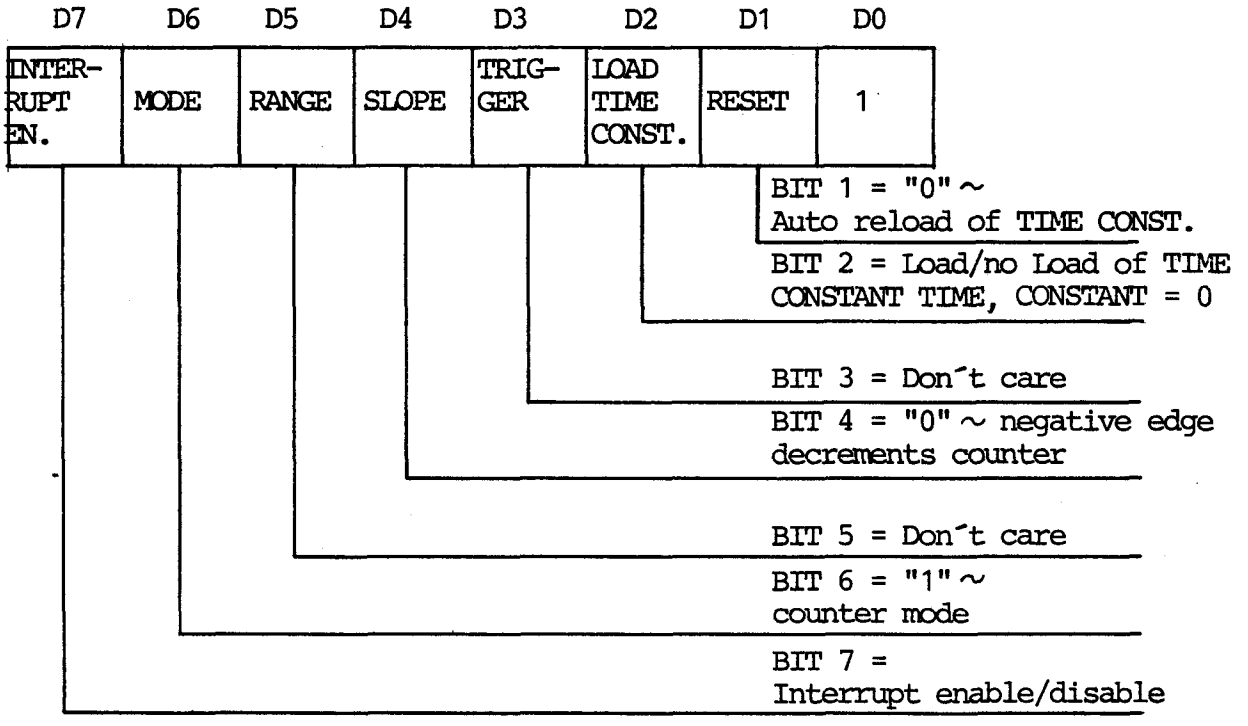
3.2 CTC Use

3.2

The IML501 controller uses CTC channel 3 for interrupt purposes. An interrupt is generated when terminal count is reached, i.e. when the DMA channel 1 byte count reaches zero. During write transfers, i.e. DMA transfers from IML501 to memory, the interrupt is directly generated by means of the EOP pulse from the DMA controller. During read transfers, i.e. DMA Transfers from memory to IML501 (programming of the EPROM's), the interrupt is delayed until the last byte has been programmed.

3.2.1 Channel 3 Control Register

3.2.1



3.2.2 Channel 3 Time Constant Register

An 8-bit time constant is loaded into the time constant register following a channel control word with bit 2 set.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1

3.2.3 Interrupt Vector

The desired interrupt vector is loaded into channel 0 with D0 = "0". D7-D3 contain the stored interrupt vector. D2-D1 are not used in loading the vector. When the CTC responds to an interrupt acknowledge, these two bits contain the binary code of the highest priority channel which requested the interrupt. IML501 has lowest priority and will respond with D2-D1 = 1,1.

D7	D6	D5	D4	D3	D2	D1	D0
V7	V6	V5	V4	V3	X	X	0

IML 501 responds with
D2 - D1 = 1,1

A. REFERENCES A.

[1] RC850 Controller Reference Manual
RCSL No.: 31-D594

[2] IML501 Technical Description
RCSL No.: 52-AA1058

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