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CRT505/507 - CRT controller
Technical Manual

RCSL No 42-i 2164

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Keywords:

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Abstract:

This manual contains relevant technical information on CRT505 and CRT507.

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RCSL No 42-I 2164

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FOREWORD

First edition RCSL No 44-RT2041.
Second edition RCSL No 44-RT2067.

The first edition did only cover the CRT505, whereas the second edition has been extended to cover the CRT507 as well.

1. DESCRIPTION 1.

CRT505/507 is the interface between MIC50x and the CRT monitor.

The two units, CRT505 and CRT507, are functional identical and therefore completely interchangeable.

The CRT507 is a later version of the CRT505, and the only difference between the units is, that a number of pull up/down resistors has been added on the CRT507 in order to ease automatic testing in the production.

Throughout the manual, the two units are described as one. Except for some logic diagrams, which is specific for one of the two, no distinction is made between them.

CRT505/507 displayes continously the contents of a 2 k x 16 bit refresh memory, which is maintained as a copy of the highest 4 k bytes of main memory (i.e. addresses F000 to FFFF): Every time a byte is written in this area, it is written into the corresponding address of the refresh memory as well. Each pair of addresses in the refresh memory corresponds to a position on the screen.

The first byte plus one bit of the second selects a character in the character font to be displayed. Two bits in the second select a shadow character to be superponed the first. The remaining bits (the attribute selectors) select one out of 32 programdefined combinations of the 8 attributes, which control the display of the character.

1.1 Refresh Memory 1.1

As the character frequency to the 60 Hz screen is too high for the MC6845 chip (3 MHz), this is run at half the character frequency, and two characters (32 bit) are read out of the refresh memory for each read operation.

The address multiplexer U31, U32, U11 (p13) to the refresh memory is controlled by CCLK. CCLK is low during the last character period, letting the CRT controller read the character for display. During the first CCLK phase however, the refresh memory is addressed with the MIC address lines, making write access possible.

The leading edge of a write to the refresh area is caught in the F.F. U6 (p13), generating a write request, which is syncronized to CCLK in the F.F. U8 (p1) which makes U27 (p1) generate a writepulse beginning after CCLK goes high and ending before CCLK goes low.

During the refresh phase, the refresh memory is addressed by the CRT controller MC6845 and the read data is locked into the buffer register on the rising edge of CCLK.

1.2 Character Font 1.2

The character font consists of three memories: a ROM (U65 and U55 p5), containing predefined dot patterns for 128 or 256 characters, a RAM (M9-16 p6), with space for programming of 256 character patterns and a RAM (U 67, 68, 69) with space for the programming of 4 dot patterns, one of which is always superponed the character pattern displayed.

The character font contains 9 x 16 bits for each character pattern or shadow pattern and they are read with 18 bits in parallel (DOT 0-8 and SDOT0-8). The SDOT's and DOT's are "ored" together giving 9 compound dots being parallel loaded into the shifter and the shifted out one by one at a frequency of 27 MHz.

1.3 Video Generation 1.3

The output of the dot shifter is used to select the display of foreground or background. Foreground and background are defined for each character position in the refresh memory by 5 bits. The 5 bits are used to select one out of 32 combinations of 8 attributes stored in the attribute RAM (U34 p3).

Six of the attributes are converted into a back- and foreground colour or grey scale value, in the attribute ROM ROB234, U35 p3. Three bits out of the attribute control ROM ROB235, select display mode, Normal, end display, cursor, Blank and blink states.

The control ROM is addressed with cursor position information, blink information, display disable and two attribute bits.

The three colour signals from the dot selector go to J4 for a colour monitor or to the D/A converter on p1 generating a grey scale video signal for a BW monitor.

The grey scale video is chopped with the 27 MHz to create an impression of dots in horizontal direction.

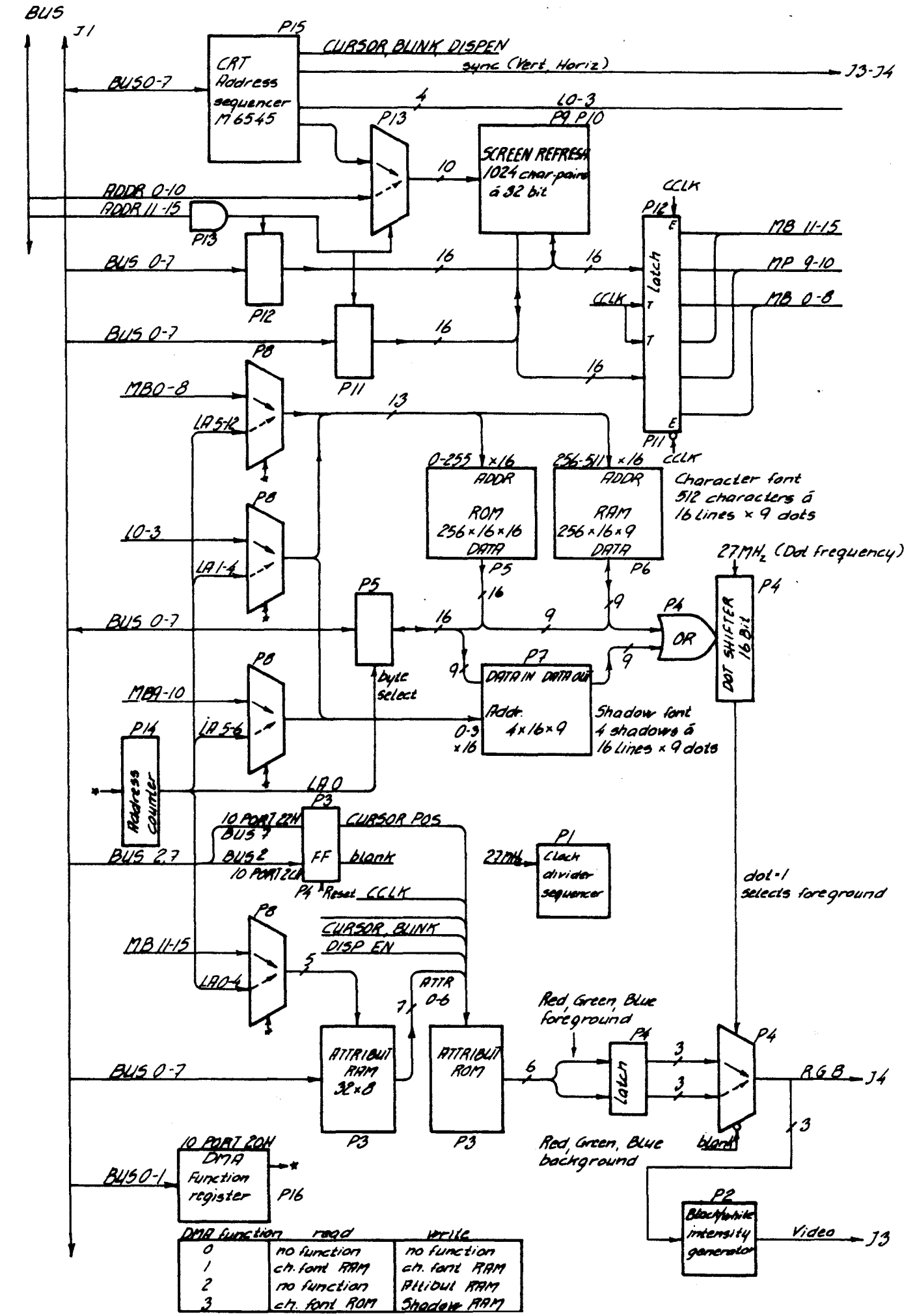
1.4 DMA 1.4

The character fonts and the attribute RAM are accessed from the MIC board via DMA, controlled by the DMA controller on the MIC board.

The memory to be accessed is selected with an I/O write command to port 20 Hex. This write command clears the load address counter and sets the DMA RUN flipflop U5a p12, which then lets the DRQ EN flip-flop U56 p12 generate a DMA REQ next time DISP EN goes low (during horizontal retrace). The DMA REQ (REQ 0) makes the DMA controller perform two DMA cycles: DRQ EN is reset only after the LA counter (bit 0) is counted up on the trailing edge of DMA ACK, this causes the DMA controller to generate the second DMA cycle. So DMA transfers take place with two bytes every 64 microsecond, always starting with the even byte.

2. BLOCK DIAGRAM

2.



DMA function	read	write
0	no function	no function
1	ch. font RAM	ch. font RAM
2	no function	Attibut RAM
3	ch. font ROM	Shadow RAM

3. LOGIC DIAGRAMS AND FUNCTIONAL DESCRIPTION 3.

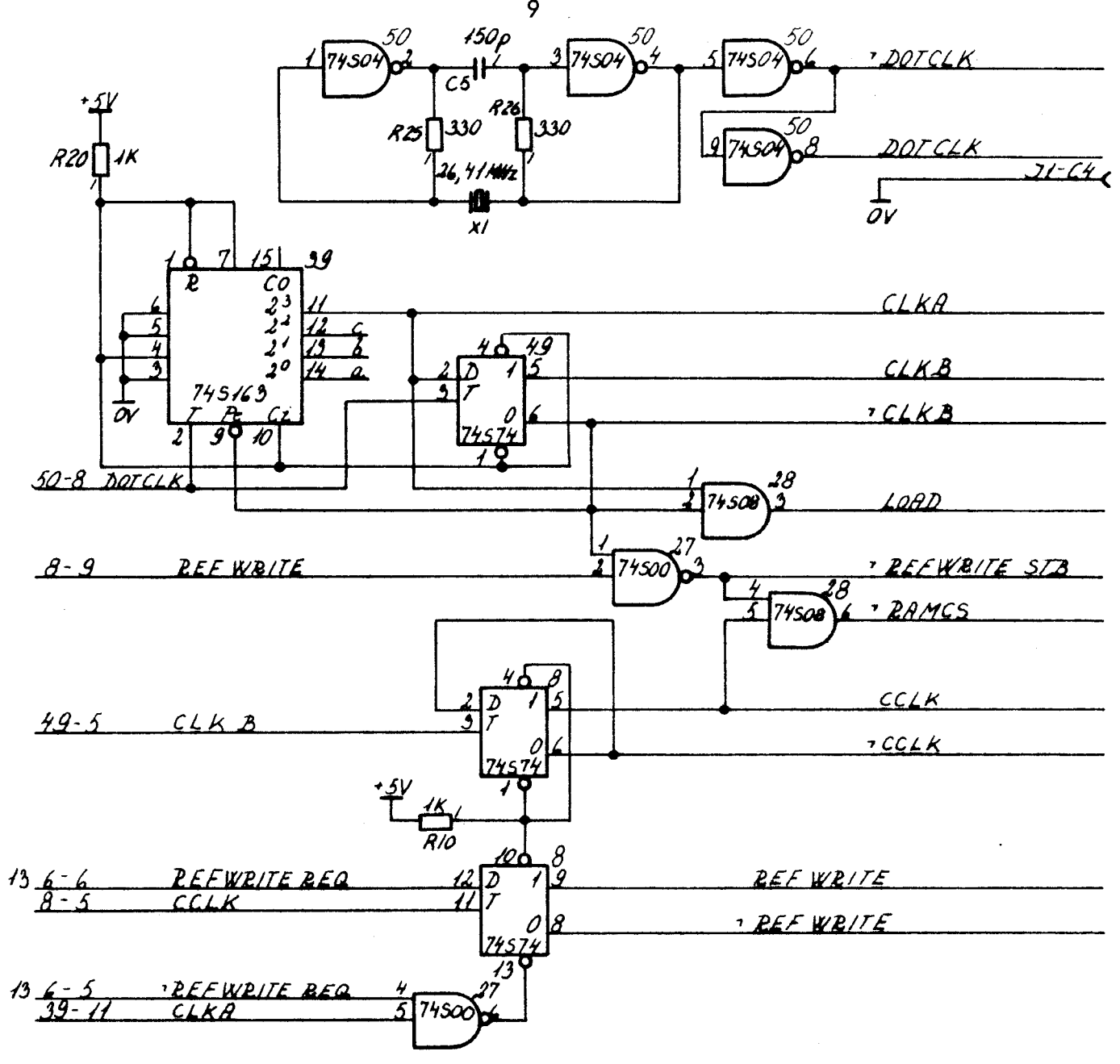
The following pages contain logic diagrams for CRT505/507. A functional description is given on the left hand page to the corresponding diagram sheet.

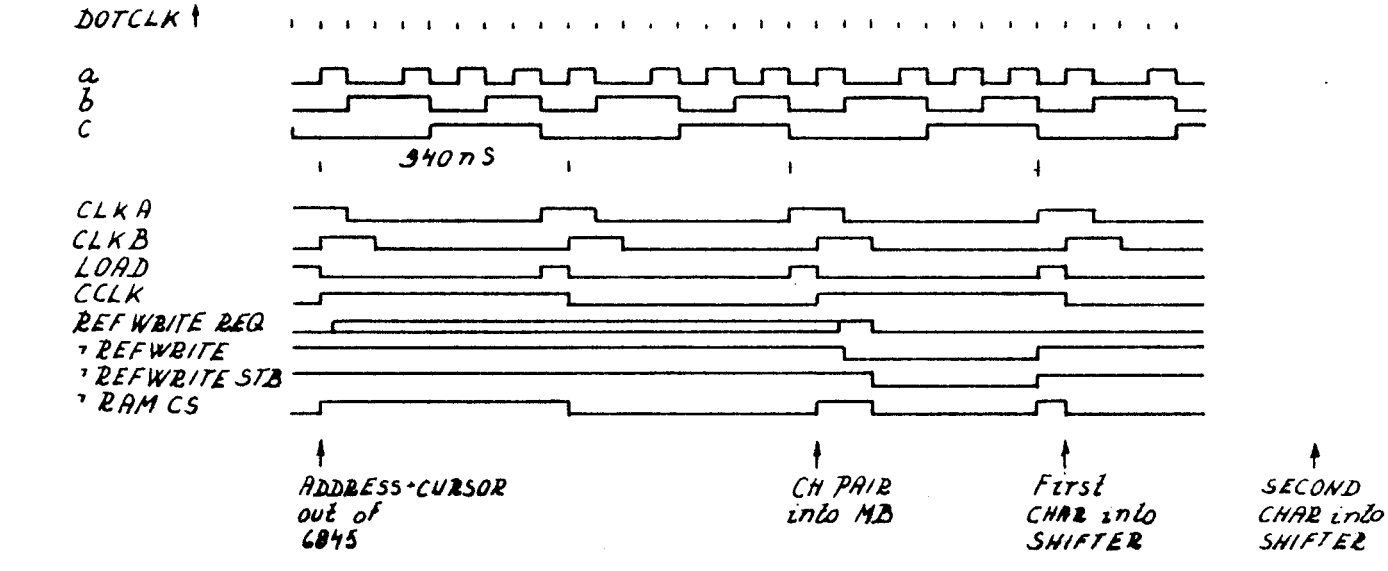
The functional description consists of a schematic listing of all signals generated on the page. A short description and a listing of the diagrams to which the signal is transferred is given for each signal.

Most diagram sheets and corresponding description are valid for both CRT505 and CRT507. Some pages, however, are specific for one of the two. The identification of the diagrams are found in the lower left corner.

Note: All references between individual diagram sheets make use of diagram numbers (lower right corner) and not page numbers.

Signal	Destination	Description
-,DOT CLK	2	26.4 MHz master clock
DOTCLK	1, 4	
CLK A	1	High during last and first dot
CLK B	4	High during two first dots
-,CLK B	1	
LOAD	4	Loads dotshifter after test dot
-,REF WRITE STB	1, 13	Indicates write time in Refresh memory and clears write request fifo
-,RAM CS	9, 10	Disable Refresh memory after each read, to let the outputs reach high impedance state before write. During write, -,RAM CS is the write strobe controlled by -,REF WRITE STB
REF WRITE	1	Is the synchronized value of REF WRITE REQ
-,REF WRITE	13	
CCLK -,CCLK		CCLK is the half character frequency. The low to high transition defines the time to read a new character pair into the refresh memory. The state indicates which of the two characters is to be displayed.


74S04
150p
C5
R25 330
R26 330
26,41MHz
X1
+5V
R20 1K
DOTCLK
DOTCLK
J1-C4
0V
74S163
CLKA
CLKB
74S74
50-8 DOTCLK
74S08
LOAD
8-9 REFWRITE
74S00
REFWRITE STB
RAMCS
49-5 CLKB
CCLK
R10 1K
13 6-6 REFWRITE REQ
8-5 CCLK
REF WRITE
13 6-5 REFWRITE REQ
39-11 CLKA


DOTCLK
a
b
c
340nS
CLKA
CLKB
LOAD
CCLK
REF WRITE REQ
REFWRITE
REFWRITE STB
RAM CS
ADDRESS+CURSOR out of 6845
CH PAIR into MB
First CHAR into SHIFTER
SECOND CHAR into SHIFTER

Signal	Destination	Description
-,DOT CLK	2	26.4 MHz master clock
DOTCLK	1, 4	
CLK A	1	High during last and first dot
CLK B	4	High during two first dots
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LOAD	4	Loads dotshifter after test dot
-,REF WRITE STB	1, 13	Indicates write time in Refresh memory and clears write request fifo
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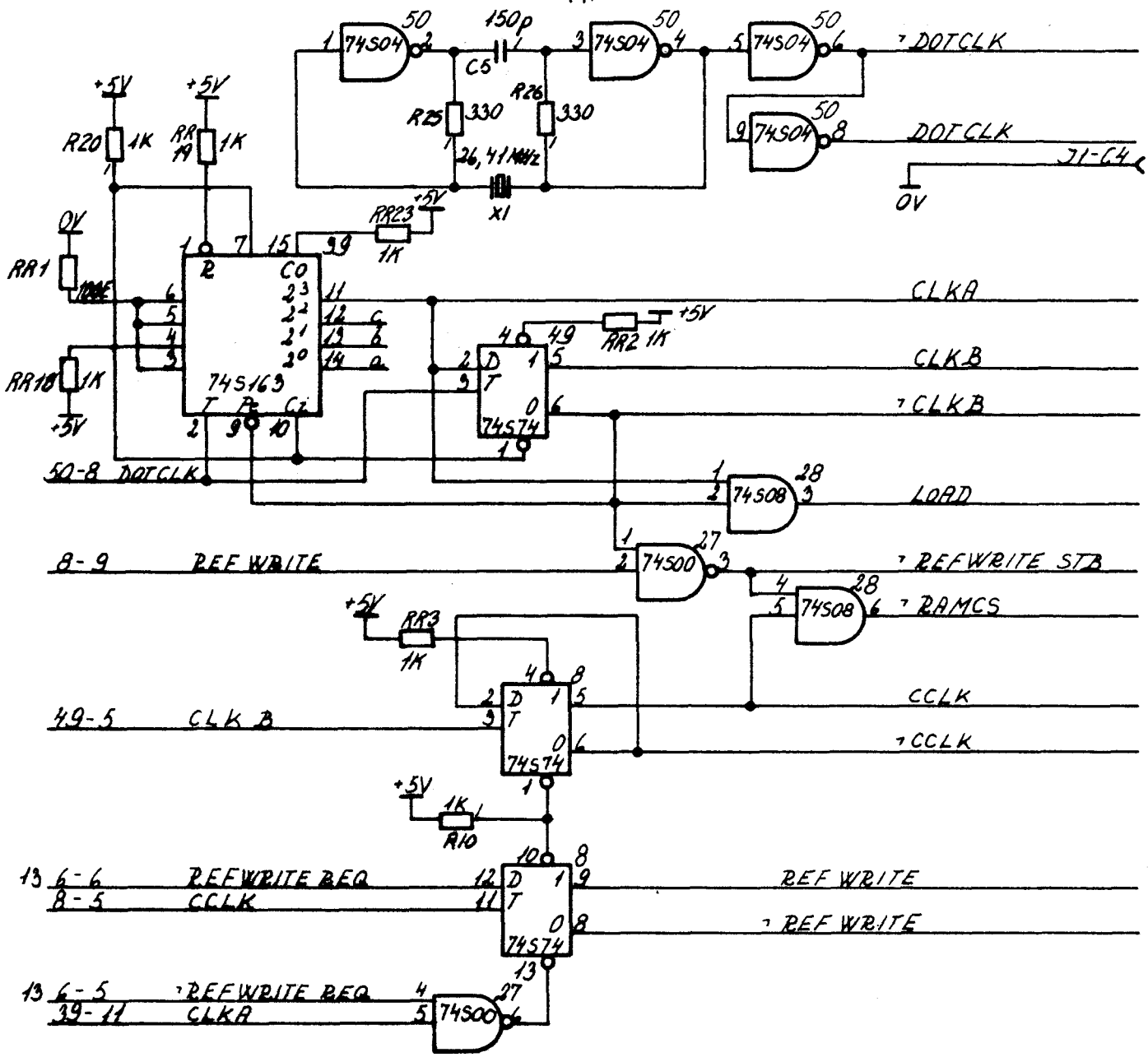
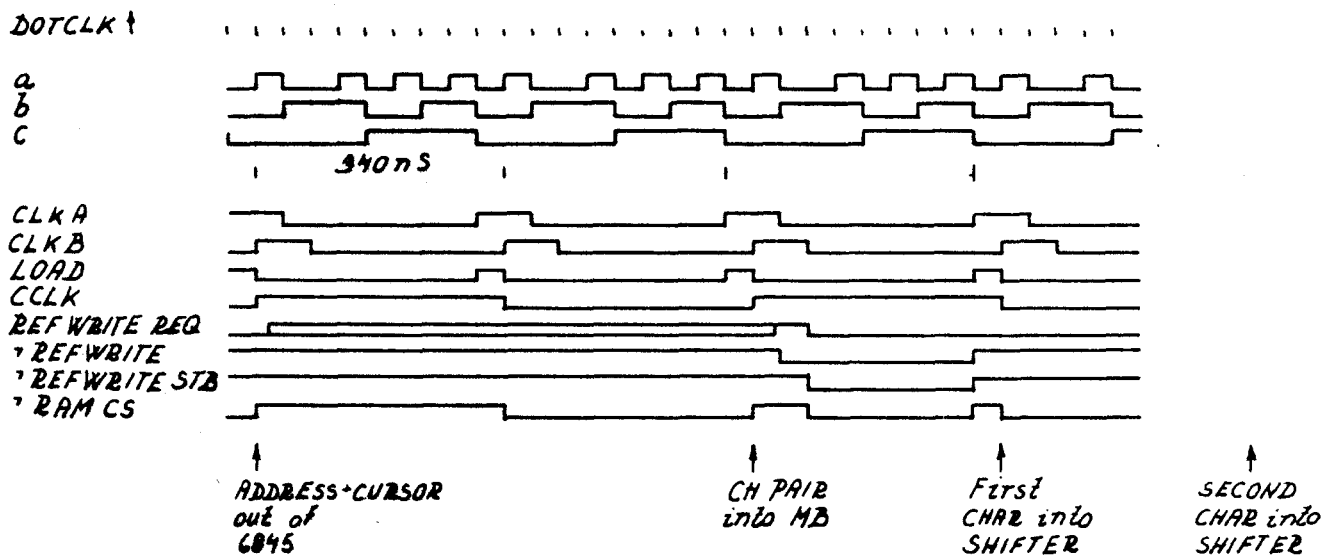
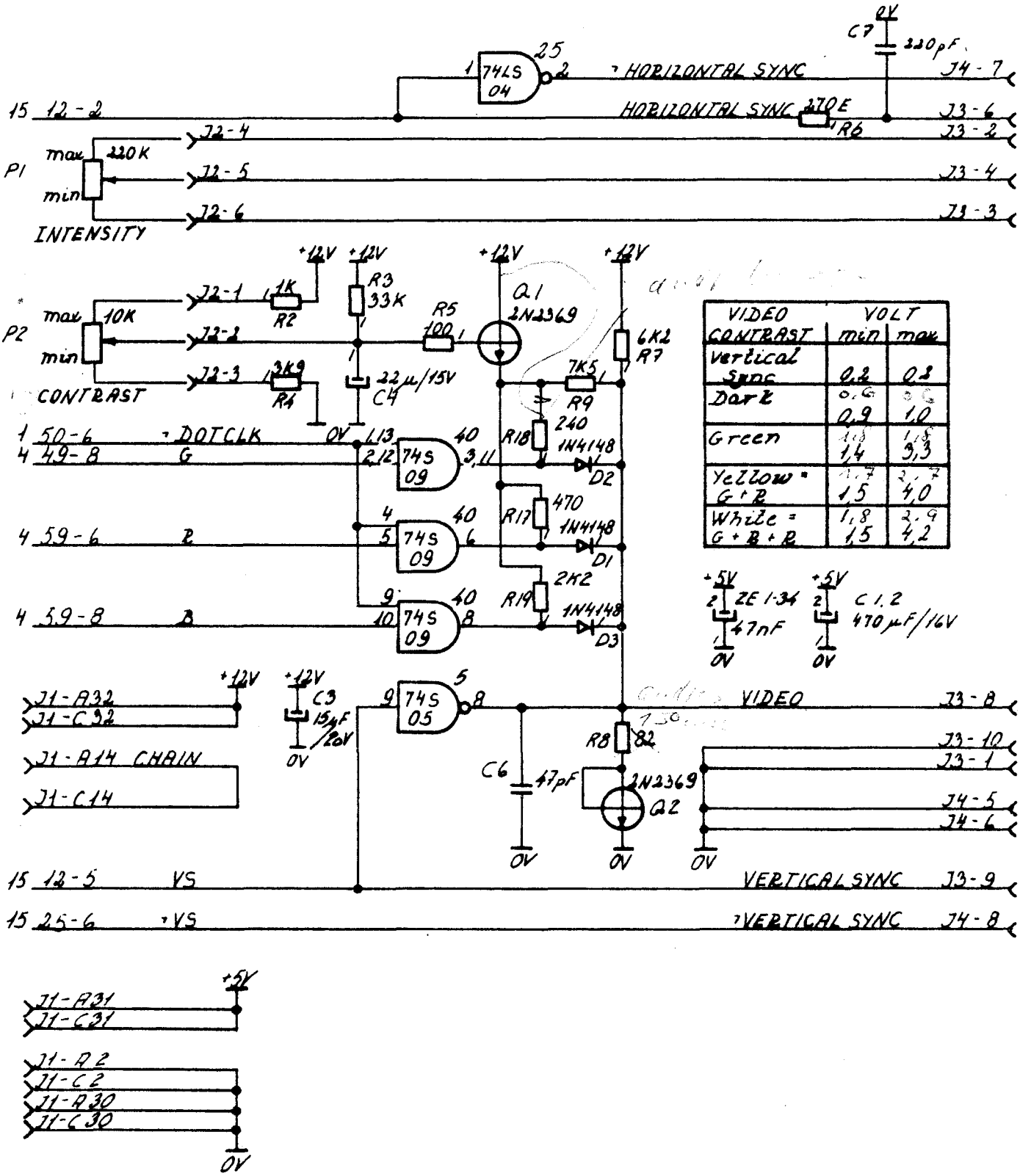
REF WRITE	1	Is the synchronized value of REF WRITE REQ
-,REF WRITE	13	
CCLK -,CCLK		CCLK is the half character frequency. The low to high transition defines the time to read a new character pair into the refresh memory. The state indicates which of the two characters is to be displayed.


74S04
150p
C5
R25 330
R26 330
26,41MHz
X1
+5V
R20 1K
RR19 1K
RR23 1K
RR1
RR18 1K
0V
74S163
74S74
RR2 1K
RR3 1K
R10 1K
74S08
74S00
DOTCLK
CLKA
CLKB
LOAD
CCLK
RAMCS
REFWRITE STB
REFWRITE REQ
REFWRITE
50-8 DOTCLK
8-9 REFWRITE
49-5 CLKB
6-6 REFWRITE REQ
8-5 CCLK
6-5 REFWRITE REQ
39-11 CLKA
J1-C4


DOTCLK
a
b
c
940nS
CLKA
CLKB
LOAD
CCLK
REFWRITE REQ
REFWRITE
REFWRITE STB
RAM CS
ADDRESS+CURSOR out of 6845
CH PAIR into MB
First CHAR into SHIFTER
SECOND CHAR into SHIFTER

Signal	Destination	Description
-,Horizontal sync	J4-7	Line pulse to colour display sync
Horizontal sync	J3-6	Line sync pulse to B&W display
J2-4 J2-5 J2-6	J3-2 J3-4 J3-3	Intensity control for the B&W display
Video	J3-8	Video signal for B&W display
chain	J1-A14 J1-C14	
Vertical sync	J3-9	Frame syncpulse to the B&W display
-,Vertical sync	J4-8	Frame syncpulse to the Colour display



VIDEO CONTRAST	VOLT min	VOLT max
Vertical Sync	0,2	0,2
Dark	0,6 0,9	1,0
Green	1,4	3,3
Yellow = G + R	1,5	4,0
White = G + B + R	1,8 1,5	3,9 4,2

A/C 03 04 08

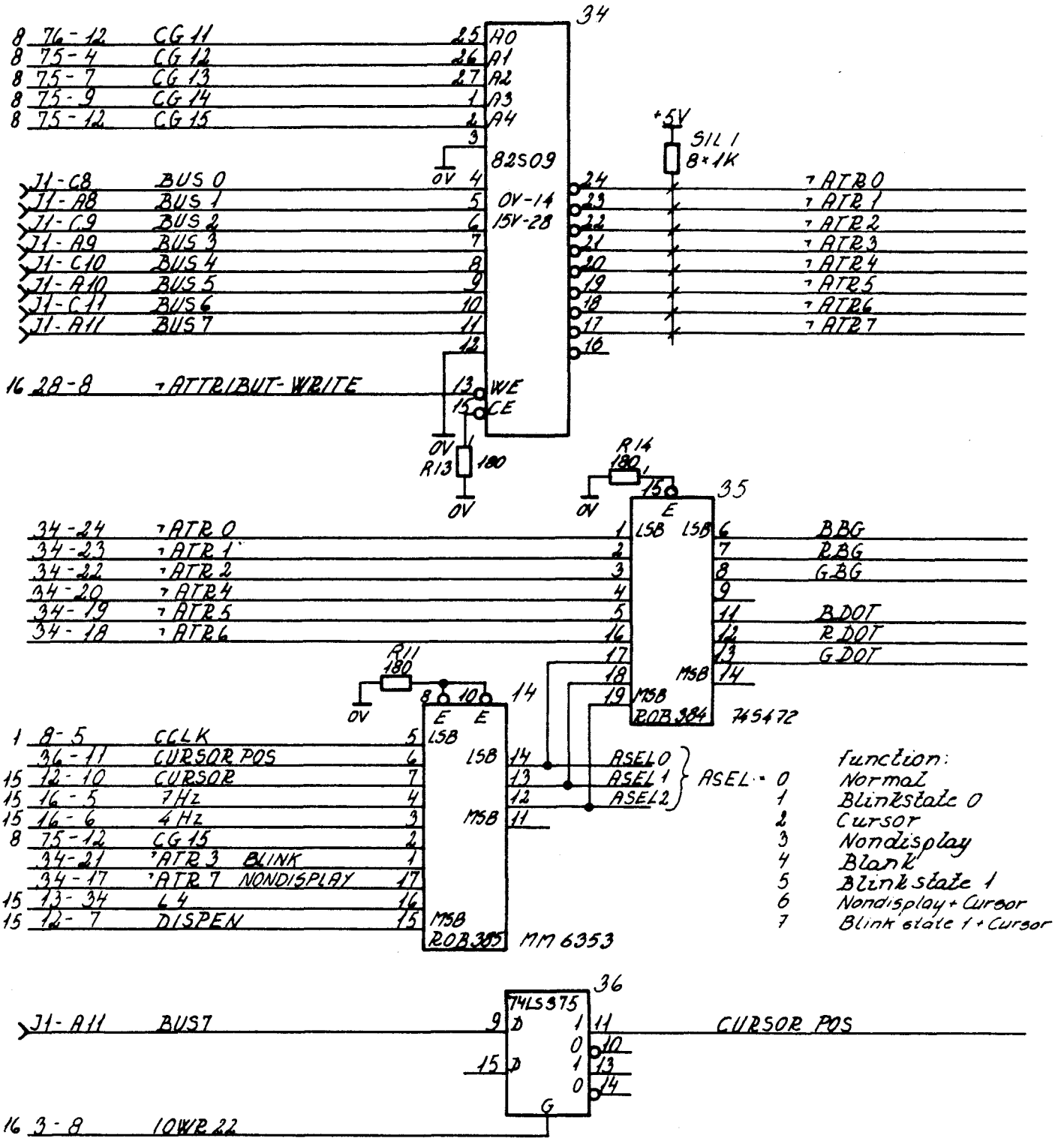
CP 03 03 05

505a
CRT 507

A 13566

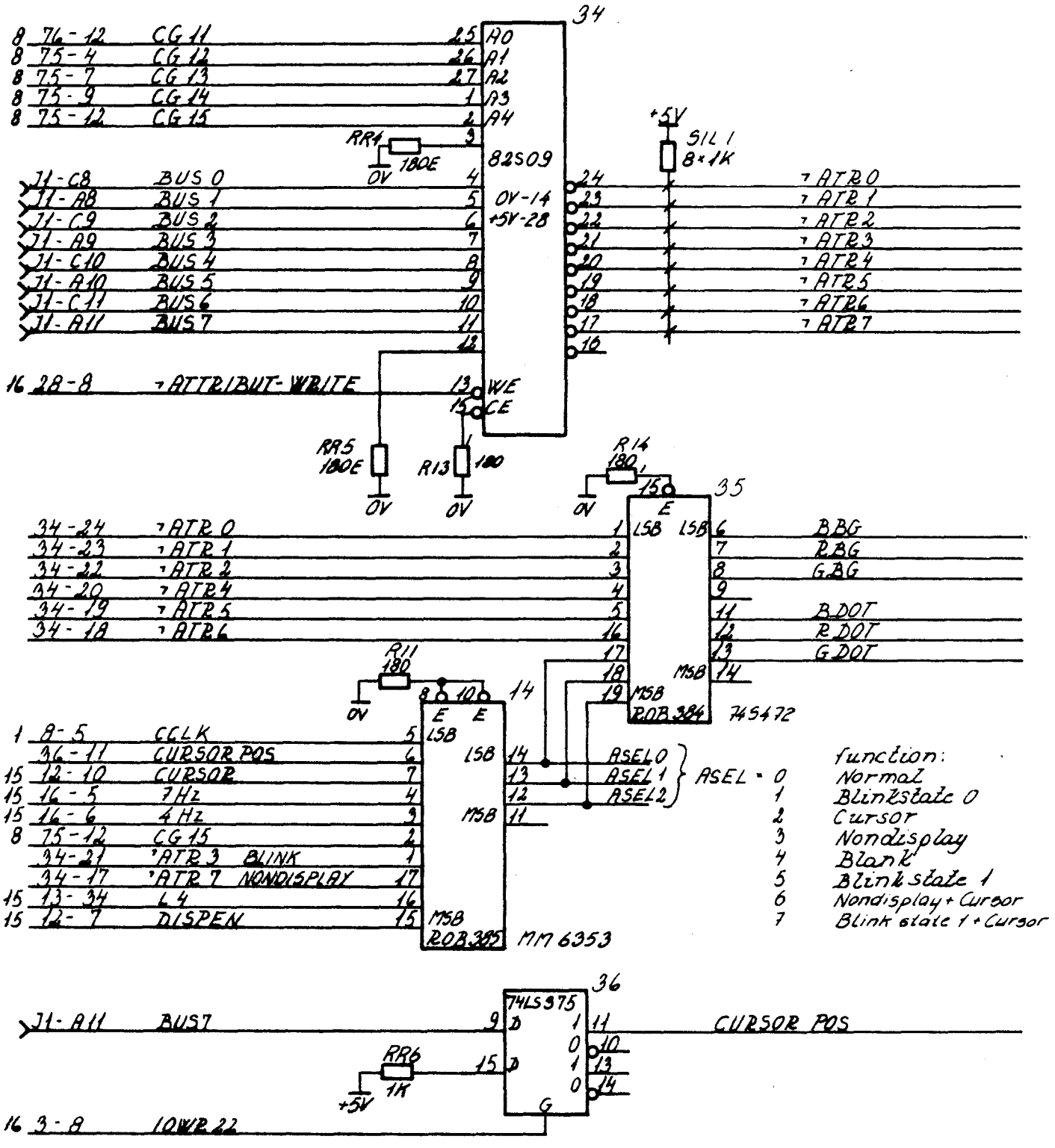
VIDEO CONVERTER

Signal	Destination	Description
-,ATR0-2	3	Attribute memory output Define normally background colour (except in compatibility mode)
-,ATR3	3	Enables blink
-,ATR4-6	3	Define normally foreground (DOT) colour. If -,ATR4-6 = (1,1,1), compatibility mode is selected
-,ATR7	3	Selects nondisplay (foreground := background)
ASEL0-2	3	Select attribute conversion as shown in the table on the diagram
CURSOR POS	3	Is the least significant bit of the cursor position (the rest of the cursor position designator is loaded into the MC6845)



PKA 820723 R6A 821026

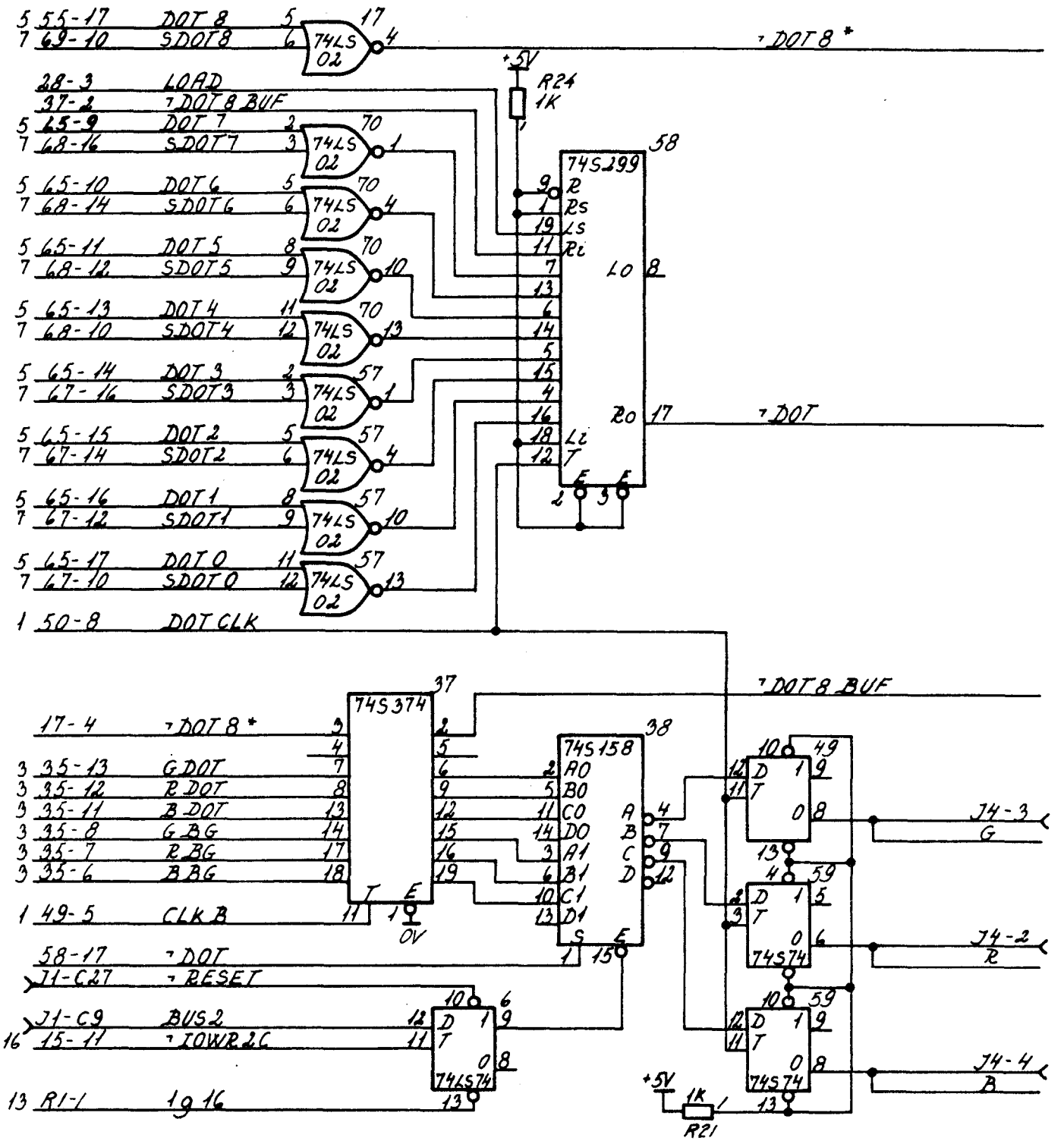
Signal	Destination	Description
-,ATR0-2	3	Attribute memory output Define normally background colour (except in compatibility mode)
-,ATR3	3	Enables blink
-,ATR4-6	3	Define normally foreground (DOT) colour. If -,ATR4-6 = (1,1,1), compatibility mode is selected
-,ATR7	3	Selects nondisplay (foreground := background)
ASEL0-2	3	Select attribute conversion as shown in the table on the diagram
CURSOR POS	3	Is the least significant bit of the cursor position (the rest of the cursor position designator is loaded into the MC6845)



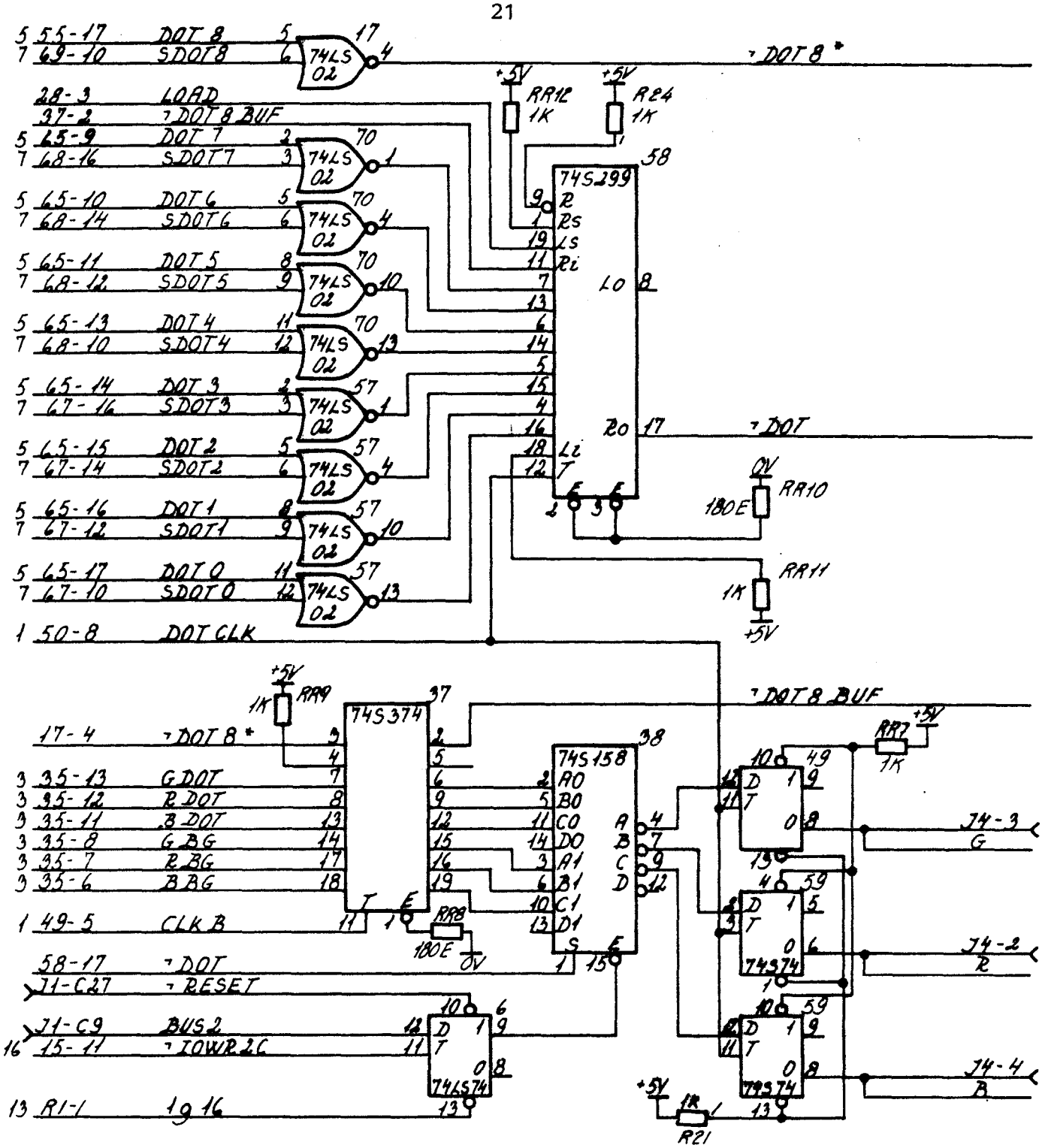
RIC 930408

CP 930405

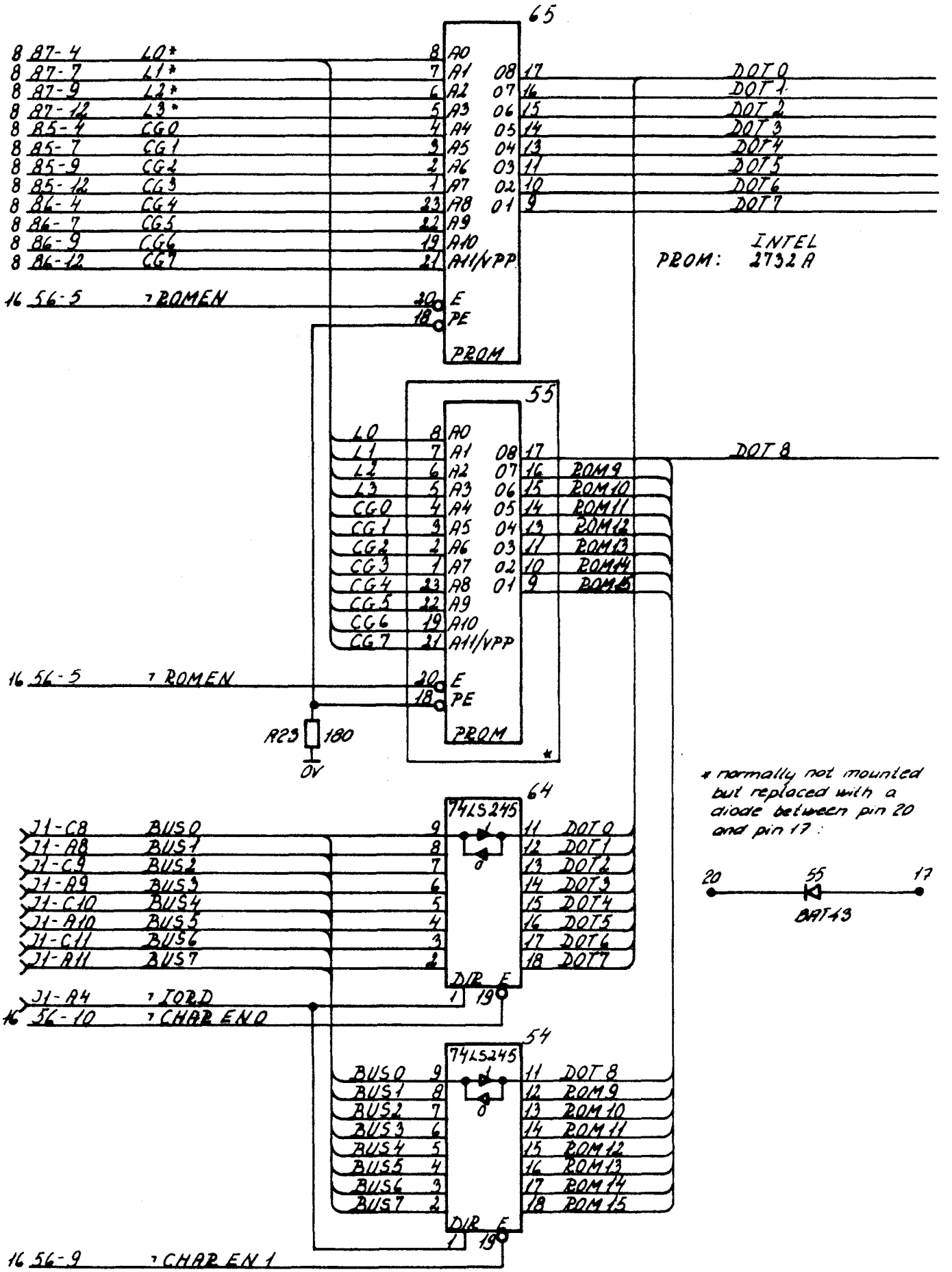
Signal	Destination	Description
-,DOT	4	Selects foreground, if low, to be displayed in the actual pixel
G	2, J4-3	Green
R	2, J4-2	Red
B	2, J4-4	Blue
		Colour signals to the colour monitor or to the D/A converter on diagram 2.


55-17 DOT 8
69-10 SDOT8
74LS 02
DOT 8 *
+5V
R24 1K
28-3 LOAD
37-2 DOT 8 BUF
65-9 DOT 7
68-16 SDOT7
65-10 DOT 6
68-14 SDOT6
65-11 DOT 5
68-12 SDOT5
65-13 DOT 4
68-10 SDOT4
65-14 DOT 3
67-16 SDOT3
65-15 DOT 2
67-14 SDOT2
65-16 DOT 1
67-12 SDOT1
65-17 DOT 0
67-10 SDOT0
50-8 DOT CLK
74S299
LO
RO
DOT
74S374
74S158
DOT 8 BUF
17-4 DOT 8 *
35-13 G DOT
35-12 R DOT
35-11 B DOT
35-8 G BG
35-7 R BG
35-6 B BG
49-5 CLK B
58-17 DOT
J1-C27 RESET
J1-C9 BUS 2
15-11 IOWR2C
74S74
J4-3 G
J4-2 R
J4-4 B
1K R21

Signal	Destination	Description
-,DOT	4	Selects foreground, if low, to be displayed in the actual pixel
G	2, J4-3	Green
R	2, J4-2	Red
B	2, J4-4	Blue
		Colour signals to the colour monitor or to the D/A converter on diagram 2.


DOT 8
SDOT8
74LS 02
+DOT 8*
+5V
RR12 1K
R24 1K
LOAD
+DOT 8 BUF
DOT 7
SDOT7
DOT 6
SDOT6
DOT 5
SDOT5
DOT 4
SDOT4
DOT 3
SDOT3
DOT 2
SDOT2
DOT 1
SDOT1
DOT 0
SDOT0
74S299
+DOT
RR10
180E
0V
RR11
1K
DOT CLK
RR9
74S374
+DOT 8 BUF
+DOT 8*
GDOT
RDOT
BDOT
GBG
RBG
BBG
74S158
RR8
CLK B
+DOT
-RESET
BUS2
-IOWR2C
RR7
J4-3 G
J4-2 R
J4-4 B
R21

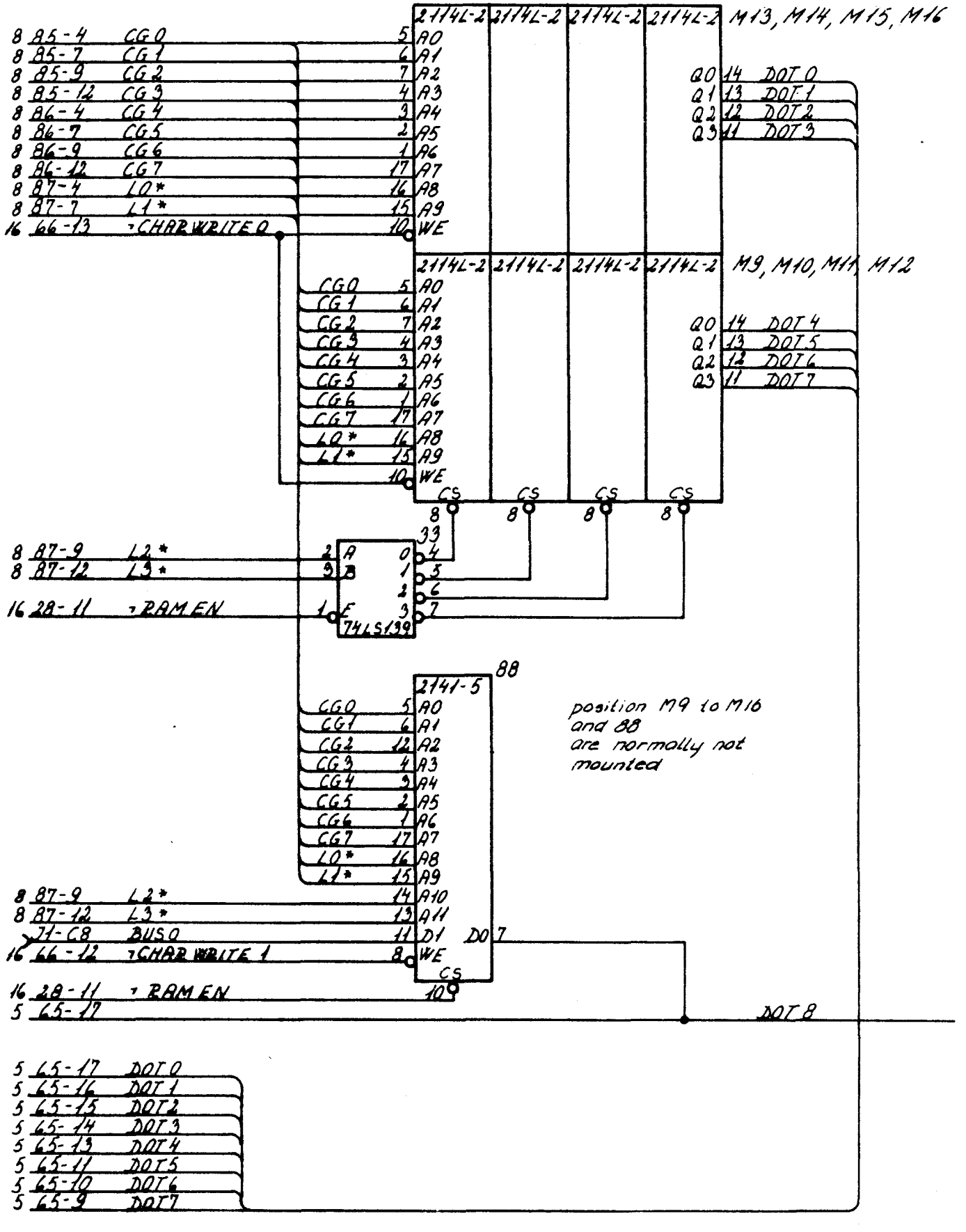
Signal	Destination	Description
DOT0-8	4	Tristate bus containing input to DOT shifter The other sources to the Tristate bus are found on diagram 6 The PROM in position 55 is normally not mounted. A diode between pin 20 and pin 17 is inserted instead



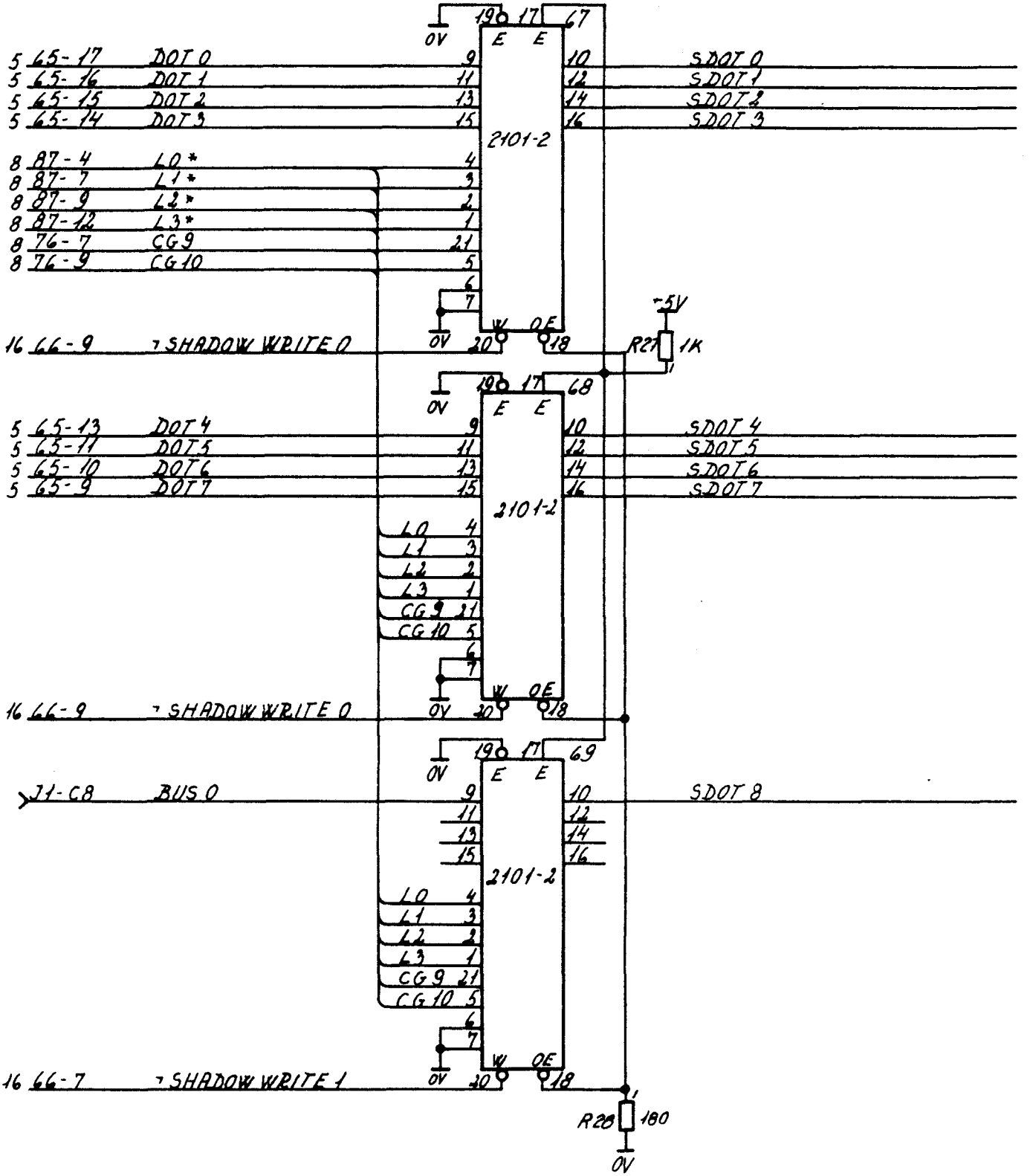
507a
CRT 505
R13562

RESIDENT CHARACTER FONT &
GATES FOR CPU ACCESS to CHARACTERFONTS

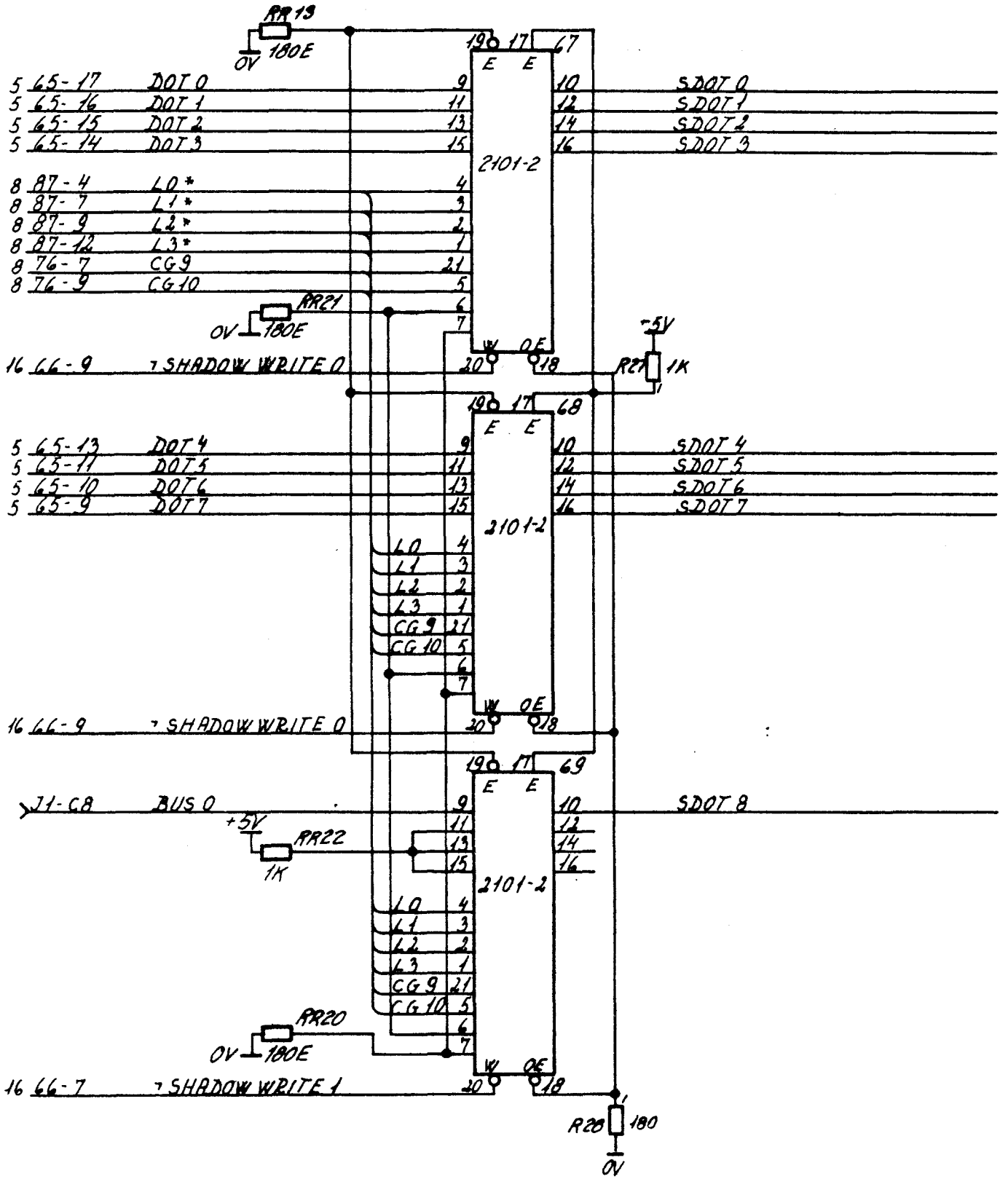
Signal	Destination	Description
DOT0-8	4	Tristate bus containing input to DOT shifter The other sources to the Tristate bus are found on diagram 5 The character font RAM's are normally not mounted


2114L-2
M13, M14, M15, M16
M9, M10, M11, M12
8 A5-4 CG0
8 A5-7 CG1
8 A5-9 CG2
8 A5-12 CG3
8 A6-4 CG4
8 A6-7 CG5
8 A6-9 CG6
8 A6-12 CG7
8 A7-4 LO*
8 A7-7 L1*
16 A6-13 ↑CHARWRITE 0
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 WE
Q0 Q1 Q2 Q3
DOT 0 DOT 1 DOT 2 DOT 3
DOT 4 DOT 5 DOT 6 DOT 7
CS
8 A7-9 L2*
8 A7-12 L3*
16 A8-11 ↑RAMEN
33
74LS139
2141-5
88
position M9 to M16 and 88 are normally not mounted
A10 A11
71-C8 BUS 0
16 A6-12 ↑CHAR WRITE 1
D1 DO
16 A8-11 ↑RAMEN
5 A5-17
DOT 8
5 A5-17 DOT 0
5 A5-16 DOT 1
5 A5-15 DOT 2
5 A5-14 DOT 3
5 A5-13 DOT 4
5 A5-11 DOT 5
5 A5-10 DOT 6
5 A5-9 DOT 7
A04 820125
A04 820125

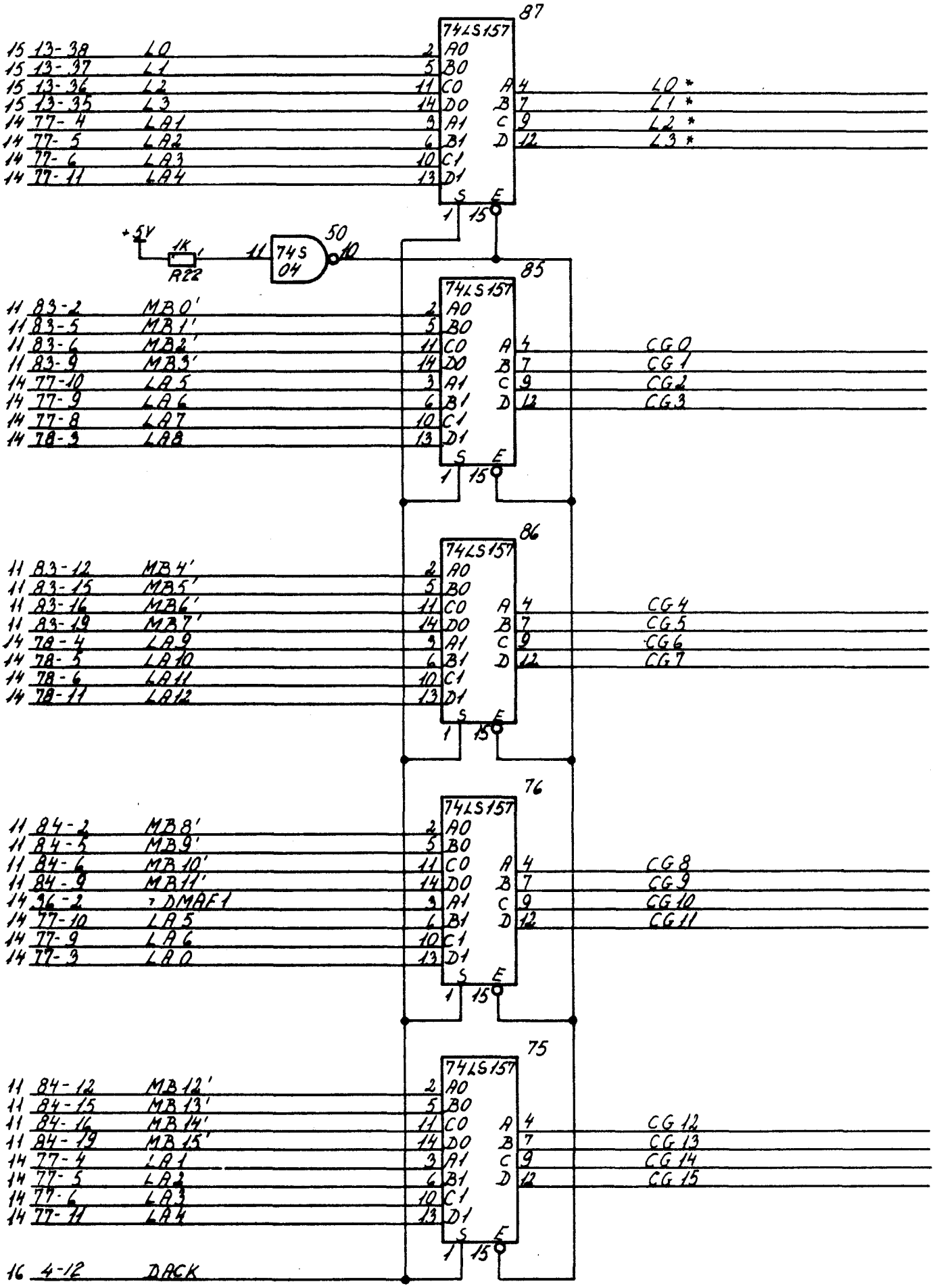
Signal	Destination	Description
SDOT0-8	4	Shadow character dots input to the DOT shifter


5 65-17 DOT 0
5 65-16 DOT 1
5 65-15 DOT 2
5 65-14 DOT 3
8 87-4 L0*
8 87-7 L1*
8 87-9 L2*
8 87-12 L3*
8 76-7 CG9
8 76-9 CG10
16 66-9 SHADOW WRITE 0
5 65-13 DOT 4
5 65-11 DOT 5
5 65-10 DOT 6
5 65-9 DOT 7
16 66-9 SHADOW WRITE 0
J1-C8 BUS 0
16 66-7 SHADOW WRITE 1
SDOT 0
SDOT 1
SDOT 2
SDOT 3
SDOT 4
SDOT 5
SDOT 6
SDOT 7
SDOT 8
2101-2
2101-2
2101-2
-5V
R27 1K
R28 180
0V

Signal	Destination	Description
SDOT0-8	4	Shadow character dots input to the DOT shifter


RR19
180E
0V
5 65-17 DOT 0
5 65-16 DOT 1
5 65-15 DOT 2
5 65-14 DOT 3
8 87-4 L0*
8 87-7 L1*
8 87-9 L2*
8 87-12 L3*
8 76-7 CG9
8 76-9 CG10
RR21
180E
0V
16 66-9 SHADOW WRITE 0
2101-2
SDOT 0
SDOT 1
SDOT 2
SDOT 3
-5V
R27 1K
5 65-13 DOT 4
5 65-11 DOT 5
5 65-10 DOT 6
5 65-9 DOT 7
SDOT 4
SDOT 5
SDOT 6
SDOT 7
16 66-9 SHADOW WRITE 0
J1-C8 BUS 0
+5V
RR22
1K
SDOT 8
RR20
180E
0V
16 66-7 SHADOW WRITE 1
R28 180
0V

Signal	Destination	Description
L0-4*	p5, p6, p7	Used to address the video line number of the character generators
CG0-7	p5, p6	Addresses a character in the character font
CG 8	p16	Selects character ROM or RAM
CG 9-10	p7	Selects shadow character
CG 11-15	p3	Select attributes; CG15 also selects blink frequency



PHD 821023 A&D

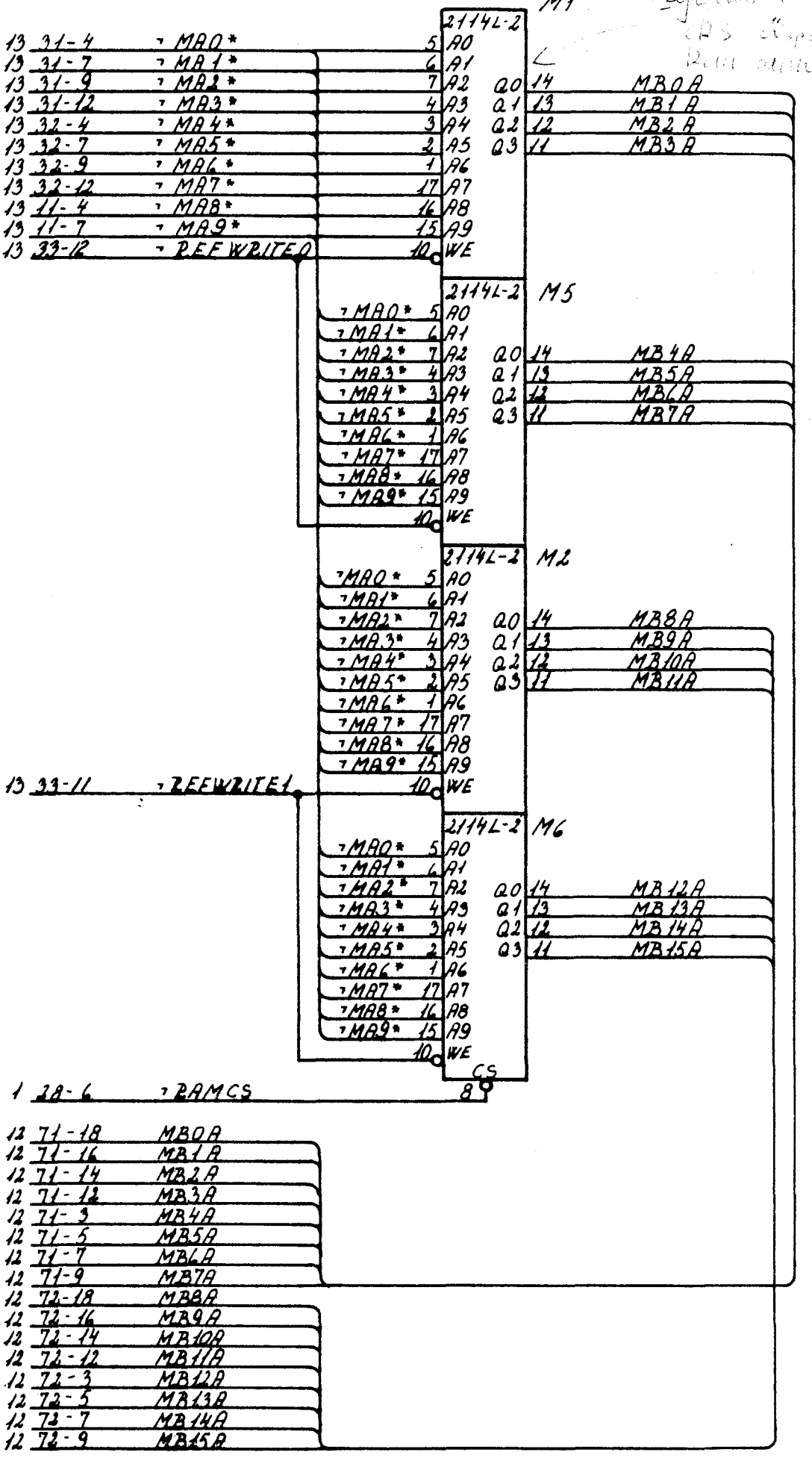
507a

CRT 505

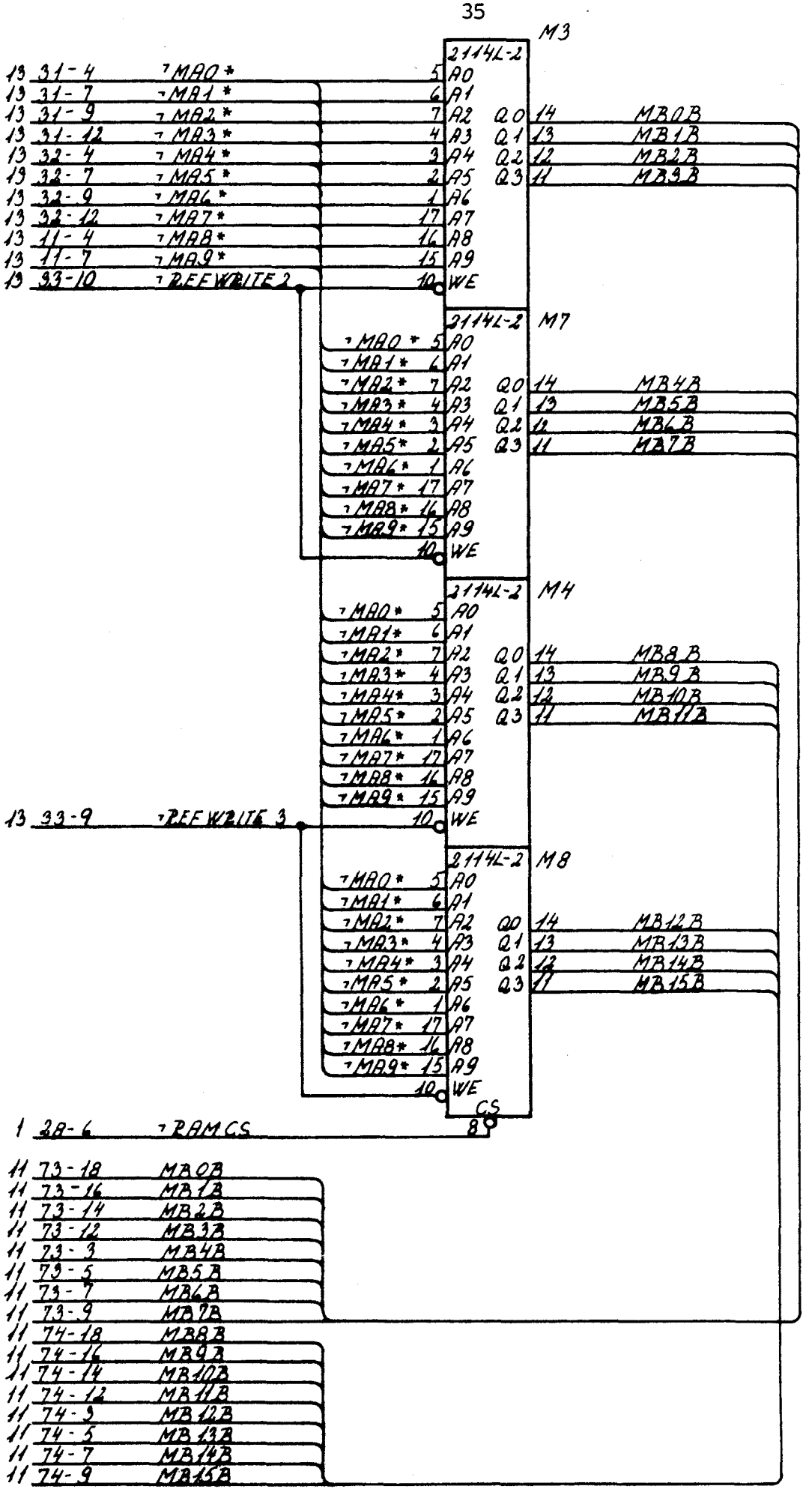
R13492

ADDRESS SWITCH for CHARACTER FONTS

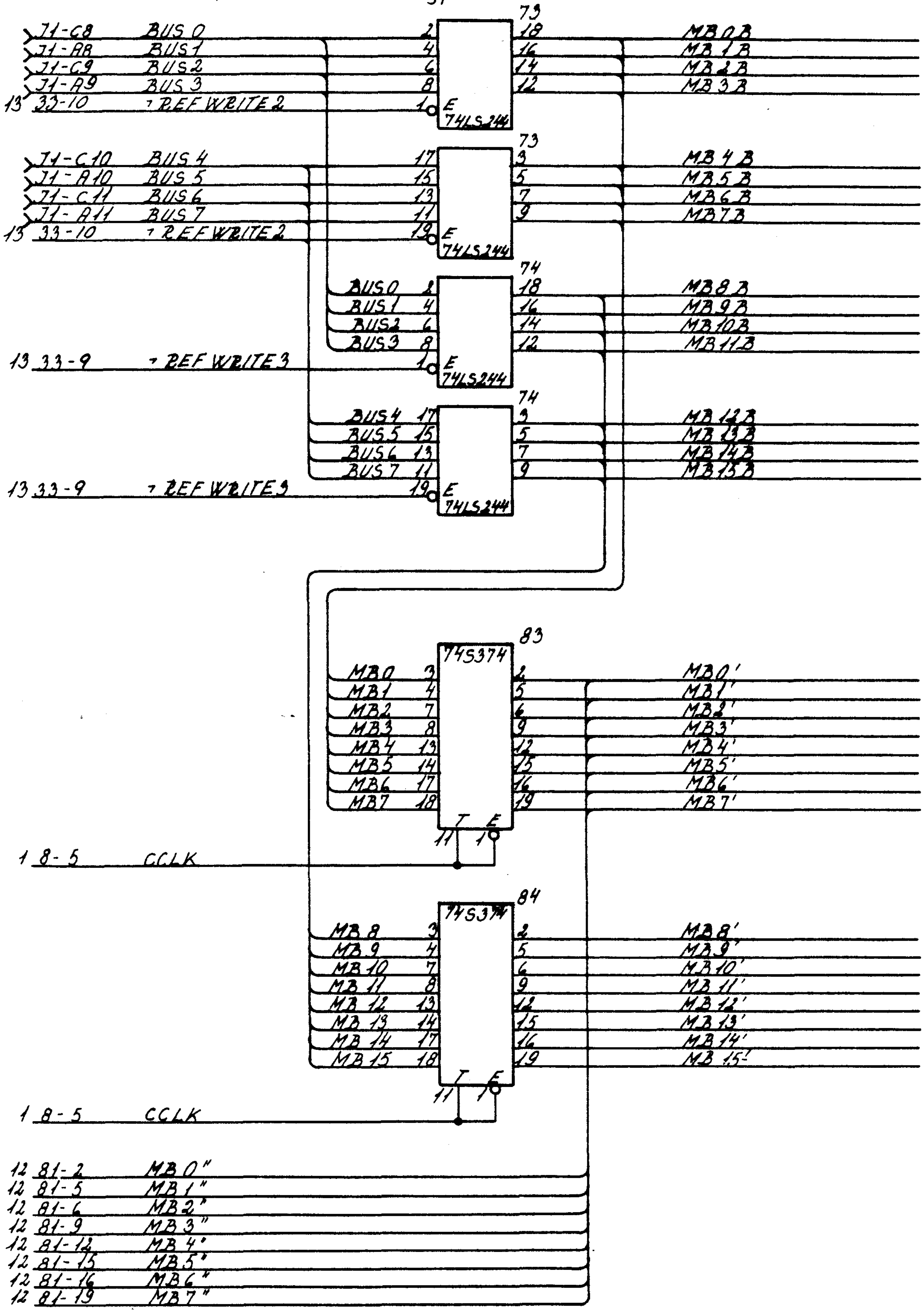
Signal	Destination	Description
MB 0-15A	12	Left side of the 32 bit wide refresh memory databus


M1
2114L-2
13 31-4 ¬MA0* 5 A0
13 31-7 ¬MA1* 6 A1
13 31-9 ¬MA2* 7 A2 Q0 14 MB0A
13 31-12 ¬MA3* 4 A3 Q1 13 MB1A
13 32-4 ¬MA4* 3 A4 Q2 12 MB2A
13 32-7 ¬MA5* 2 A5 Q3 11 MB3A
13 32-9 ¬MA6* 1 A6
13 32-12 ¬MA7* 17 A7
13 11-4 ¬MA8* 16 A8
13 11-7 ¬MA9* 15 A9
13 33-12 ¬REFWRITE0 10 WE
M5
¬MA0* 5 A0
¬MA1* 6 A1
¬MA2* 7 A2 Q0 14 MB4A
¬MA3* 4 A3 Q1 13 MB5A
¬MA4* 3 A4 Q2 12 MB6A
¬MA5* 2 A5 Q3 11 MB7A
¬MA6* 1 A6
¬MA7* 17 A7
¬MA8* 16 A8
¬MA9* 15 A9
10 WE
M2
¬MA0* 5 A0
¬MA1* 6 A1
¬MA2* 7 A2 Q0 14 MB8A
¬MA3* 4 A3 Q1 13 MB9A
¬MA4* 3 A4 Q2 12 MB10A
¬MA5* 2 A5 Q3 11 MB11A
¬MA6* 1 A6
¬MA7* 17 A7
¬MA8* 16 A8
¬MA9* 15 A9
13 33-11 ¬REFWRITE1 10 WE
M6
¬MA0* 5 A0
¬MA1* 6 A1
¬MA2* 7 A2 Q0 14 MB12A
¬MA3* 4 A3 Q1 13 MB13A
¬MA4* 3 A4 Q2 12 MB14A
¬MA5* 2 A5 Q3 11 MB15A
¬MA6* 1 A6
¬MA7* 17 A7
¬MA8* 16 A8
¬MA9* 15 A9
10 WE
CS
1 28-6 ¬RAMCS 8
12 71-18 MB0A
12 71-16 MB1A
12 71-14 MB2A
12 71-12 MB3A
12 71-3 MB4A
12 71-5 MB5A
12 71-7 MB6A
12 71-9 MB7A
12 72-18 MB8A
12 72-16 MB9A
12 72-14 MB10A
12 72-12 MB11A
12 72-3 MB12A
12 72-5 MB13A
12 72-7 MB14A
12 72-9 MB15A

Signal	Destination	Description
MB 0-15B	11	Right side of the 32 bit wide refresh memory databus


M3
2114L-2
13 31-4 ⁊MA0* 5 A0
13 31-7 ⁊MA1* 6 A1
13 31-9 ⁊MA2* 7 A2 Q0 14 MB0B
13 31-12 ⁊MA3* 4 A3 Q1 13 MB1B
13 32-4 ⁊MA4* 3 A4 Q2 12 MB2B
13 32-7 ⁊MA5* 2 A5 Q3 11 MB3B
13 32-9 ⁊MA6* 1 A6
13 32-12 ⁊MA7* 17 A7
13 11-4 ⁊MA8* 16 A8
13 11-7 ⁊MA9* 15 A9
13 33-10 ⁊REFWRITE2 10 WE
M7
2114L-2
⁊MA0* 5 A0
⁊MA1* 6 A1
⁊MA2* 7 A2 Q0 14 MB4B
⁊MA3* 4 A3 Q1 13 MB5B
⁊MA4* 3 A4 Q2 12 MB6B
⁊MA5* 2 A5 Q3 11 MB7B
⁊MA6* 1 A6
⁊MA7* 17 A7
⁊MA8* 16 A8
⁊MA9* 15 A9
10 WE
M4
2114L-2
⁊MA0* 5 A0
⁊MA1* 6 A1
⁊MA2* 7 A2 Q0 14 MB8B
⁊MA3* 4 A3 Q1 13 MB9B
⁊MA4* 3 A4 Q2 12 MB10B
⁊MA5* 2 A5 Q3 11 MB11B
⁊MA6* 1 A6
⁊MA7* 17 A7
⁊MA8* 16 A8
⁊MA9* 15 A9
13 33-9 ⁊REFWRITE3 10 WE
M8
2114L-2
⁊MA0* 5 A0
⁊MA1* 6 A1
⁊MA2* 7 A2 Q0 14 MB12B
⁊MA3* 4 A3 Q1 13 MB13B
⁊MA4* 3 A4 Q2 12 MB14B
⁊MA5* 2 A5 Q3 11 MB15B
⁊MA6* 1 A6
⁊MA7* 17 A7
⁊MA8* 16 A8
⁊MA9* 15 A9
10 WE
CS
1 28-6 ⁊RAMCS 8
11 73-18 MB0B
11 73-16 MB1B
11 73-14 MB2B
11 73-12 MB3B
11 73-3 MB4B
11 73-5 MB5B
11 73-7 MB6B
11 73-9 MB7B
11 74-18 MB8B
11 74-16 MB9B
11 74-14 MB10B
11 74-12 MB11B
11 74-9 MB12B
11 74-5 MB13B
11 74-7 MB14B
11 74-9 MB15B
PHD 820723 PHD 821026

Signal	Destination	Description
MB0-15B	10	Right side of the refresh memory databus
MB0'-15'	12, 8	Tristate bus containing character + attributes to be displayed



PKA 820723. ABA 821026

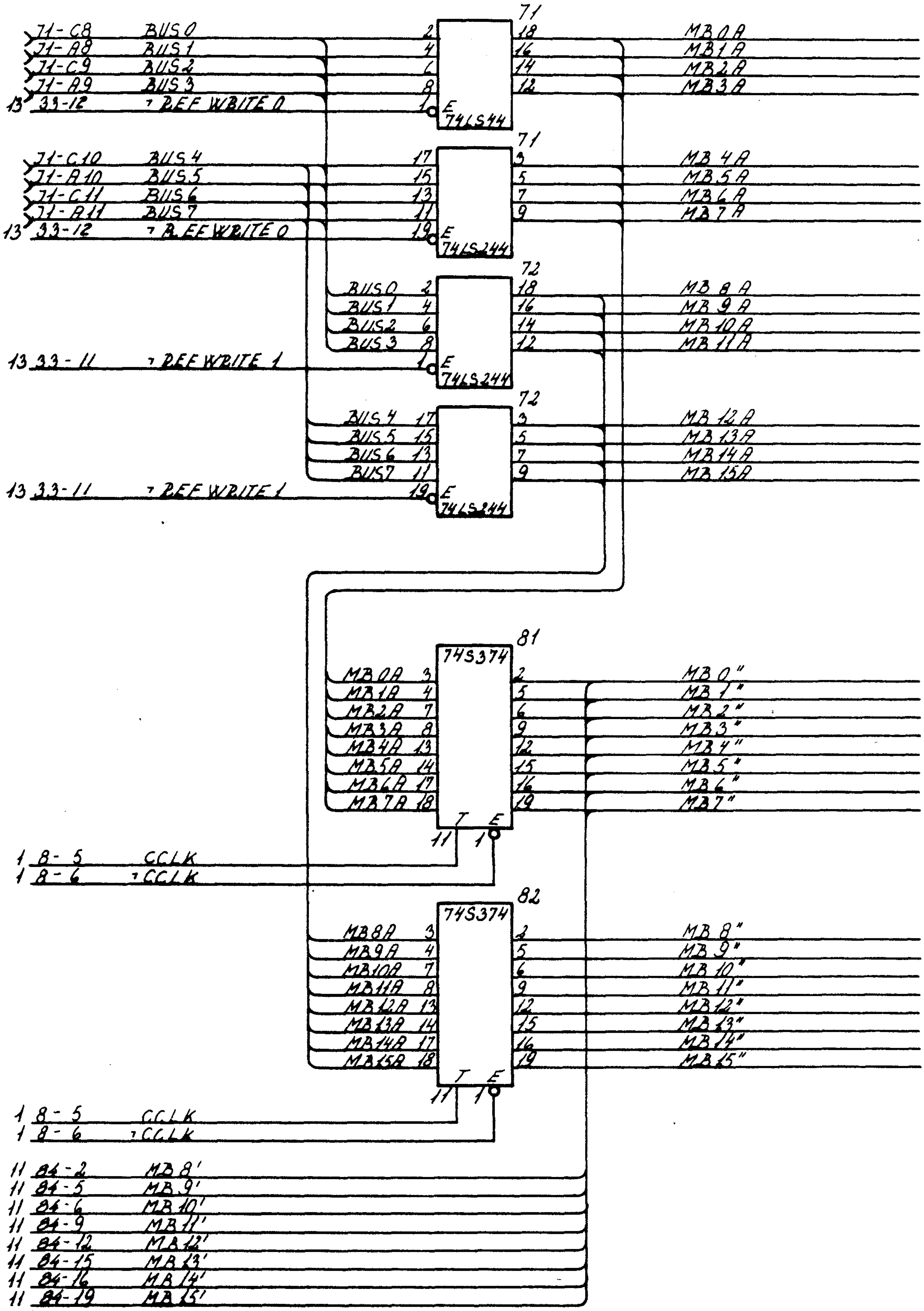
507e
CRT 505

REFRESH MEMORY WRITE GATE & READ BUFFER

11

R13495

Signal	Destination	Description
MB0-15A	9	Left side of the refresh memory databus
MB0-15"	11, 8	Tristate bus containing character + attributes to be displayed



A 13496

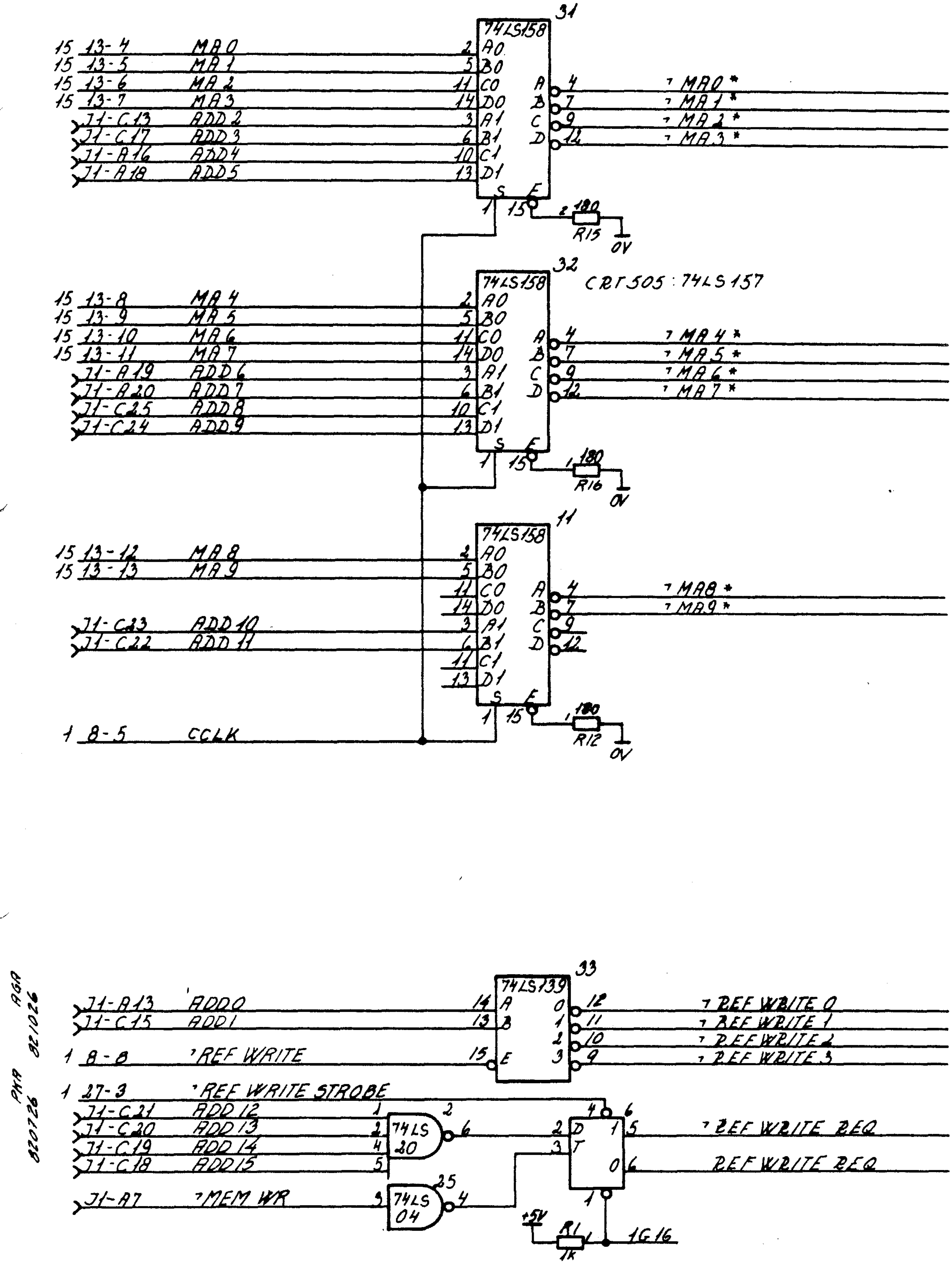
ÅGA 821026

PKA 820723

507E
CRT 505 REFRESH MEMORY WRITE GATE & READ BUFFER 12

A 13563

Signal	Destination	Description
-,MA0-9*	9, 10	Addressing of Refresh memory
-,REF WRITE 0, 1 -,REF WRITE 2, 3	9	Write enable signals to the Refresh memory
-,REF WRITE REQ REF WRITE REQ		



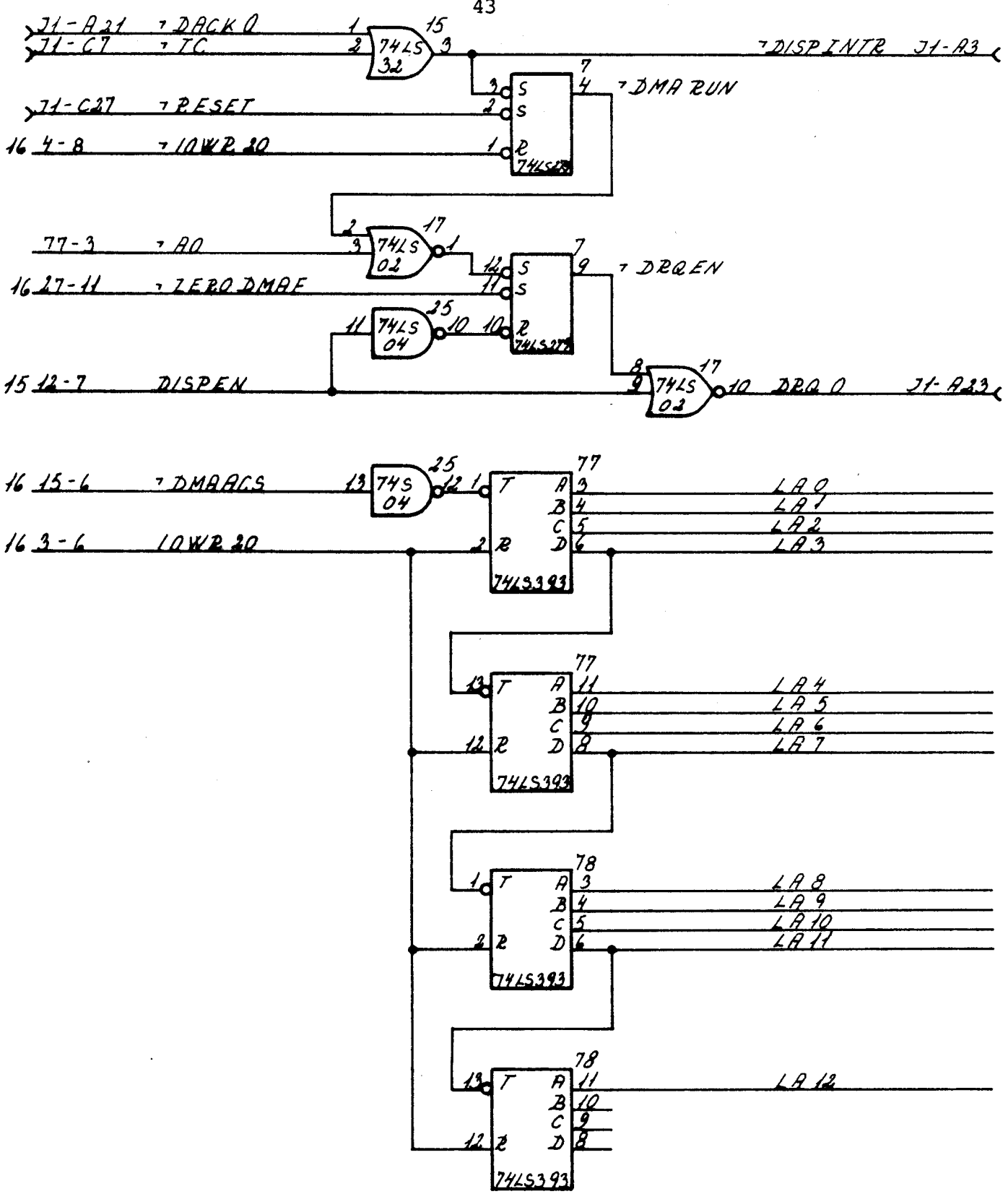
CRT 505 507c

ADDRESS SWITCH for REFRESH MEMORY

13

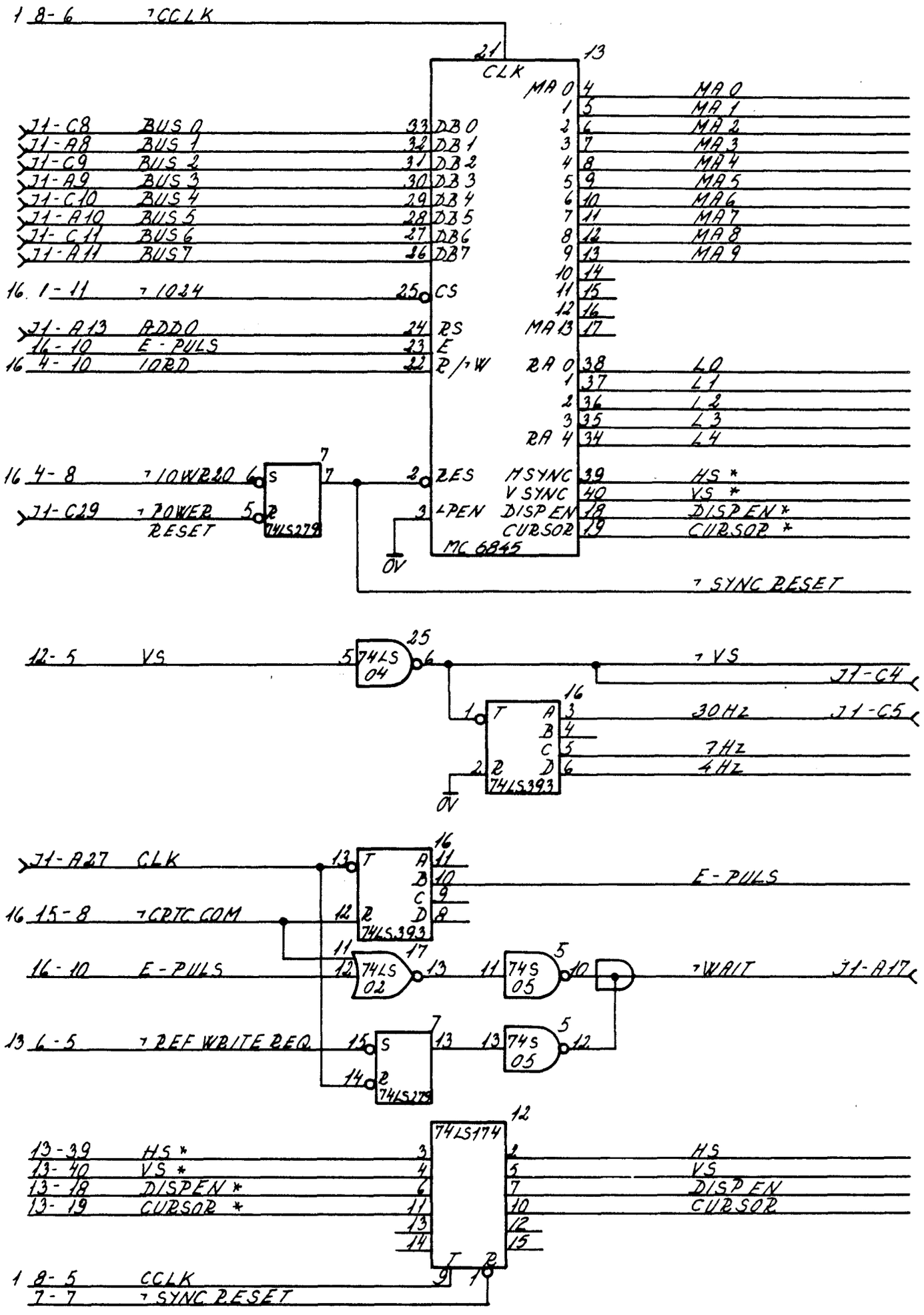
R13497

Signal	Destination	Description
-,DISP INTR	J1-A3	Terminal count interrupt after CRT-DMA transfer
DRQ 0	J1-A23	DMA Request signal
LA 0 LA 1-12	16 8	Load address bits for control of DMA transfers



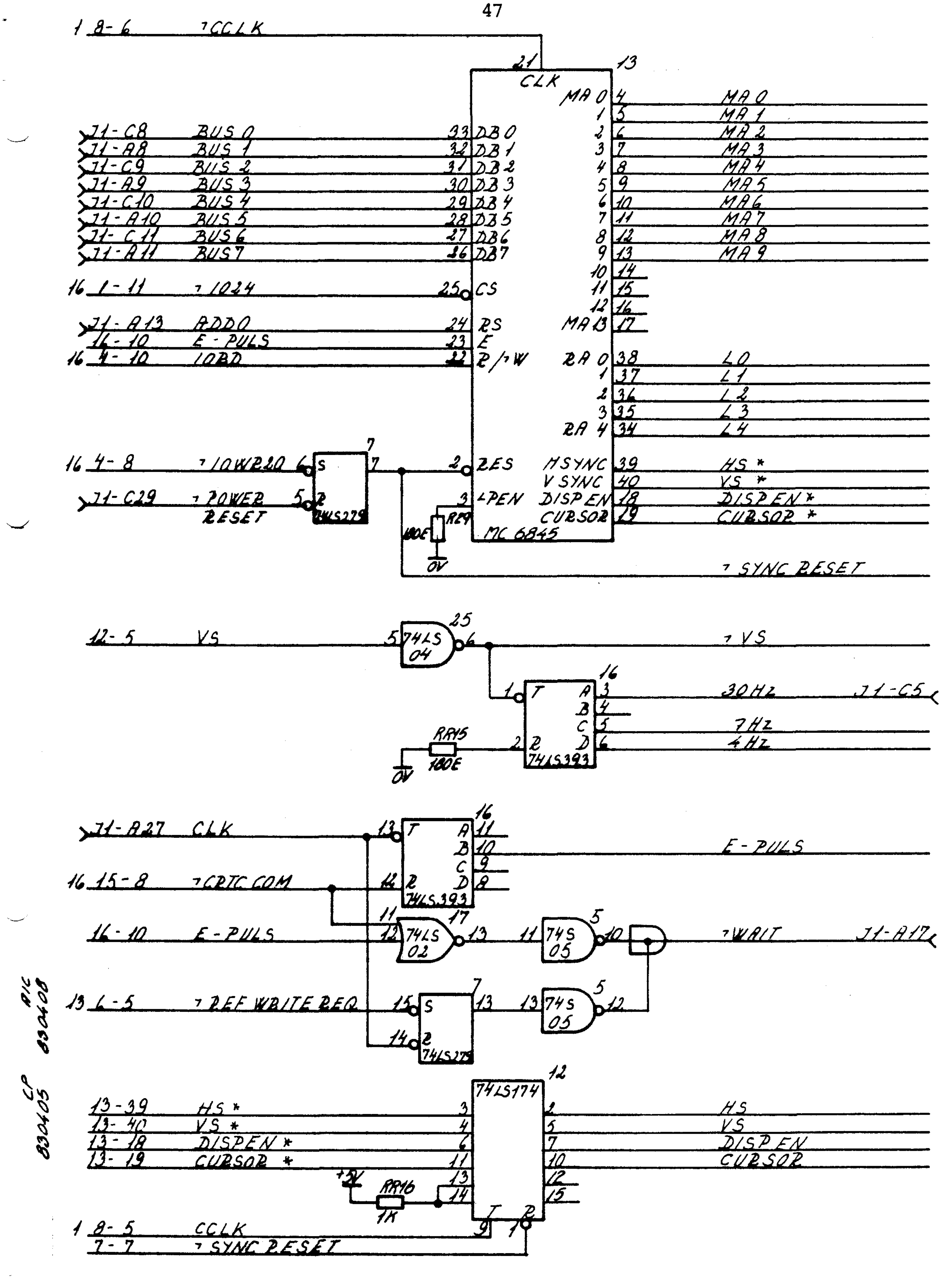
8207-13 PKA AGA 8/10/26

Signal	Destination	Description
MA 0-9	13	Read address for refresh memory
L0-3 L4	8 3	Line address to character font
-,SYNC RESET	15	Low after power reset until leading edge of IOWR20
-,VS	2, J1-C4	Vertical sync
30 Hz	J1-C5	Timer signal to CPU
7 Hz, 4 Hz	3	Blink frequencies
-,WAIT	J1-A17	Wait state generator for CPU access to MC6845
HS	2	Horizontal sync
VS	2	Vertical sync
DISP EN	3, 14	True when the e-beam is inside the picture field
CURSOR	3	True when the e-beam is in the cursor position and its neighbour

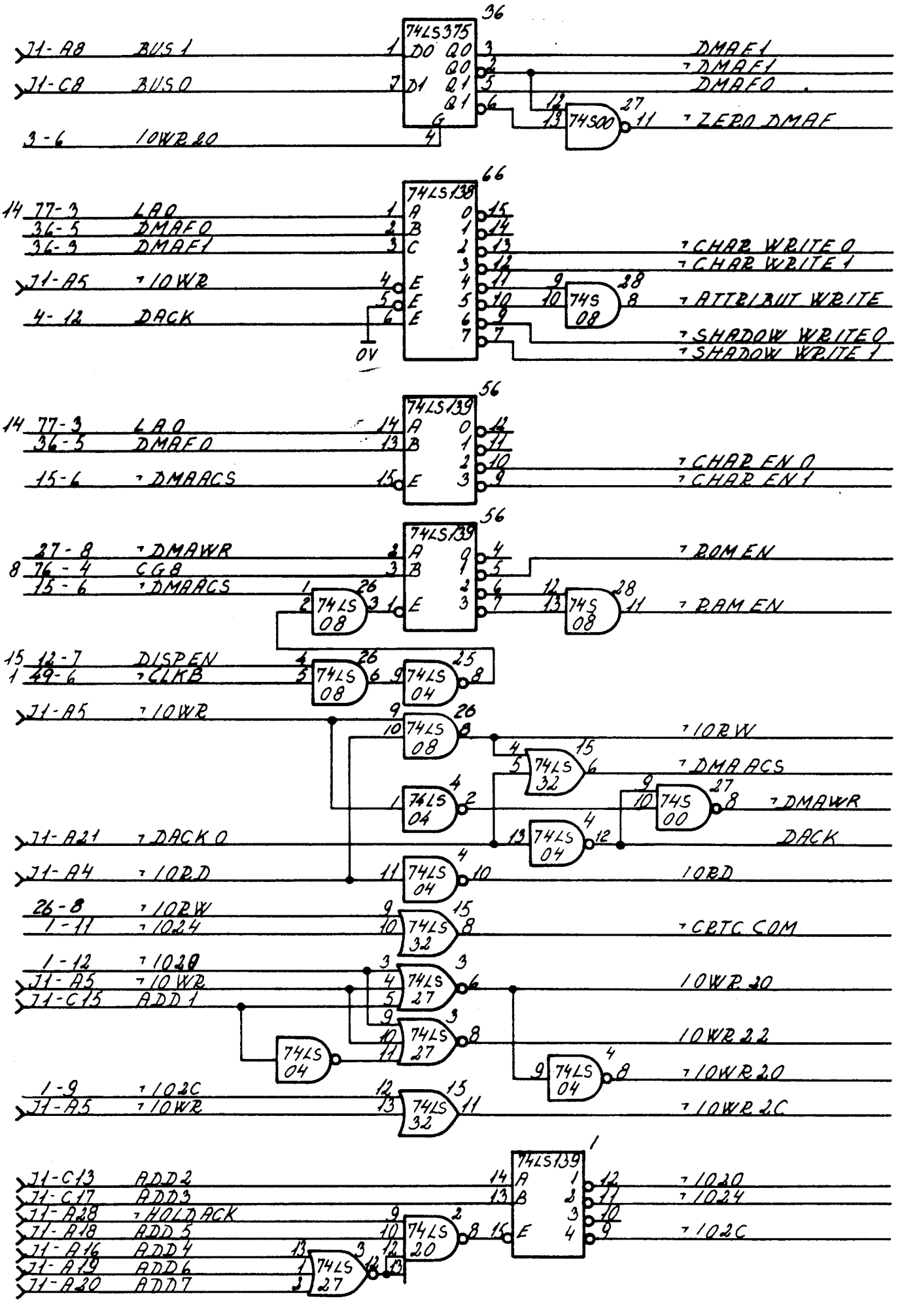


820723 PHA
820726 RSO

Signal	Destination	Description
MA 0-9	13	Read address for refresh memory
L0-3 L4	8 3	Line address to character font
-,SYNC RESET	15	Low after power reset until leading edge of IOWR20
-,VS	2, J1-C4	Vertical sync
30 Hz	J1-C5	Timer signal to CPU
7 Hz, 4 Hz	3	Blink frequencies
-,WAIT	J1-A17	Wait state generator for CPU access to MC6845
HS	2	Horizontal sync
VS	2	Vertical sync
DISP EN	3, 14	True when the e-beam is inside the picture field
CURSOR	3	True when the e-beam is in the cursor position and its neighbour

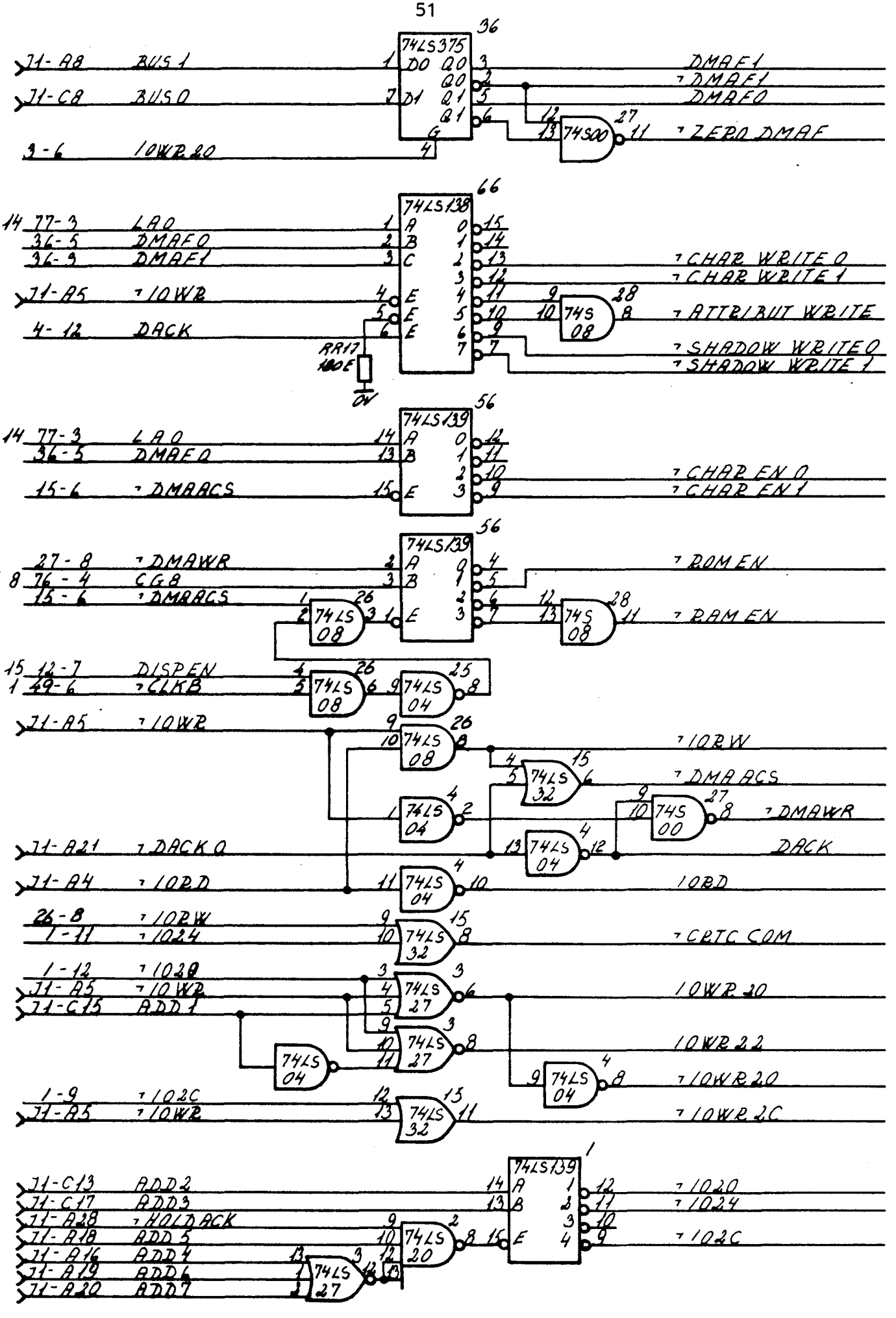

1 8-6 ¬CCLK
CLK
MC 6845
J1-C8 BUS 0
J1-A8 BUS 1
J1-C9 BUS 2
J1-A9 BUS 3
J1-C10 BUS 4
J1-A10 BUS 5
J1-C11 BUS6
J1-A11 BUS7
DB 0
DB 1
DB 2
DB 3
DB 4
DB 5
DB6
DB7
16 1-11 ¬1024
CS
J1-A13 ADD0
16-10 E-PULS
16 4-10 IORD
RS
E
R/¬W
MA 0
MA 13
MA 0
MA 1
MA 2
MA 3
MA 4
MA 5
MA6
MA7
MA 8
MA 9
RA 0
RA 4
L0
L1
L2
L3
L4
16 4-8 ¬IOWR20
J1-C29 ¬POWER RESET
74LS279
RES
LPEN
HSYNC
V SYNC
DISPEN
CURSOR
HS *
VS *
DISPEN *
CURSOR *
R29
100E
0V
¬SYNC RESET
12-5 VS
74LS 04
¬VS
74LS393
30Hz
J1-C5
7Hz
4Hz
RR15
100E
0V
J1-A27 CLK
16 15-8 ¬CRTC COM
74LS393
E-PULS
16-10 E-PULS
74LS 02
74S 05
¬WAIT
J1-A17
13 6-5 ¬REF WRITE REQ
74LS279
74S 05
A/C 830408
CP 830405
74LS174
13-39 HS *
13-40 VS *
13-18 DISPEN *
13-19 CURSOR *
HS
VS
DISPEN
CURSOR
+5V
RR16
1K
1 8-5 CCLK
7-7 ¬SYNC RESET

Signal	Destination	Description
DMA F0-1 -,DMA F1	16 8	Outputs of the DMA Function register
-,ZERO DMAF	14	Low when DMA Function is (0,0)
-,CHAR WRITE 0,1	6	Write enable signals to the Character font
-'ATTRIBUT WRITE	3	Write enable signal to the Attribut store
-,SHADOW WRITE 0,1	7	Write enable signals to the Shadow font
CHAR EN 0,1	5	Bus gate enable signals
-,ROM EN	5	Character font selection
-,RAM EN	6	Signals
-,DMA ACS	14	DMA transfer to CRT active
IORD	15	IO Read operation
-,CRTC COM	15	IO command to MC6845
IOWR20 -,IOWR20	14 14, 15	IO write to start DMA transfer
IOWR22	3	Write least significant cursor position bit
-,IOWR2C	4	Enable/disable CRT display



820723 BE1026 PWA PGA

Signal	Destination	Description
DMA F0-1 -,DMA F1	16 8	Outputs of the DMA Function register
-,ZERO DMAF	14	Low when DMA Function is (0,0)
-,CHAR WRITE 0,1	6	Write enable signals to the Character font
-'ATTRIBUT WRITE	3	Write enable signal to the Attribut store
-,SHADOW WRITE 0,1	7	Write enable signals to the Shadow font
CHAR EN 0,1	5	Bus gate enable signals
-,ROM EN	5	Character font selection
-,RAM EN	6	Signals
-,DMA ACS	14	DMA transfer to CRT active
IORD	15	IO Read operation
-,CRTC COM	15	IO command to MC6845
IOWR20 -,IOWR20	14 14, 15	IO write to start DMA transfer
IOWR22	3	Write least significant cursor position bit
-,IOWR2C	4	Enable/disable CRT display


J1-A8 BUS 1
J1-C8 BUS 0
3-6 IOWR20
74LS375
DMAF1
DMAF1
DMAF0
ZERO DMAF
14 77-3 LA0
36-5 DMAF0
36-9 DMAF1
J1-A5 IOWR
4-12 DACK
RR17 100E
74LS138
CHAR WRITE 0
CHAR WRITE 1
ATTRIBUT WRITE
SHADOW WRITE 0
SHADOW WRITE 1
14 77-3 LA0
36-5 DMAF0
15-6 DMAACS
74LS139
CHAR EN 0
CHAR EN 1
27-8 DMAWR
8 76-4 CG8
15-6 DMAACS
ROM EN
RAM EN
15 12-7 DISPEN
1 49-6 CLKB
J1-A5 IOWR
IORW
DMA ACS
DMAWR
J1-A21 DACK 0
DACK
J1-A4 IORD
IORD
26-8 IORW
1-11 1024
CRTC COM
1-12 1028
J1-A5 IOWR
J1-C15 ADD1
IOWR 20
IOWR 22
IOWR 20
1-9 102C
J1-A5 IOWR
IOWR 2C
J1-C13 ADD2
J1-C17 ADD3
J1-A28 HOLDACK
J1-A18 ADD5
J1-A16 ADD4
J1-A19 ADD6
J1-A20 ADD7
74LS20
74LS27
1020
1024
102C

4. ATTRIBUTE ROM'S 4.

The following two pages contain listings of ROB384 and ROB385 respectively.

The output codes of ROB385 are:

	Function
0:	Normal
1:	Blink state 0
2:	Cursor
3:	Non display
4:	Blank
5:	Blink state 1
6:	Non display + cursor
7:	Cursor blink state 1

The output codes of ROB384 are grouped in foreground or background, each having one of the values:

	Colour	Intensity
8:	black	black
9:	blue	very low
A:	red	low
B:	pink	reduced
C:	green	normal
D:	turquoise	increased
E:	yellow	high
F:	white	very high

Listing of ROB384.

Addresses and data are hexadecimal.

```
$A0000,
8F FE FD FC FB FA F9 F8 EF 8E ED EC EB EA E9 E8
DF DE 8D DC DB DA D9 D8 CF CE CD 8C CB CA C9 C8
BF BE BD BC 8B BA B9 B8 AF AE AD AC AB 8A A9 A8
9F 9E 9D 9C 9B 9A 89 98 EE CC 8E 8C 88 88 F8 C8
8F FE FD FC FB FA F9 F8 EF 8E ED EC EB EA E9 E8
DF DE 8D DC DB DA D9 D8 CF CE CD 8C CB CA C9 C8
BF BE BD BC 8B BA B9 B8 AF AE AD AC AB 8A A9 A8
9F 9E 9D 9C 9B 9A 89 98 8E 8C 8E 8C F8 C8 F8 C8

$A0080,
F8 EF DF CF BF AF 9F 8F FE E8 DE CE BE AE 9E 8E
FD ED D8 CD BD AD 9D 8D FC EC DC C8 BC AC 9C 8C
FB EB DB CB B8 AB 9B 8B FA EA DA CA BA A8 9A 8A
F9 E9 D9 C9 B9 A9 98 89 88 88 F8 C8 EE CC 8E 8C
FF EE DD CC BB AA 99 88 FF EE DD CC BB AA 99 88
FF EE DD CC BB AA 99 88 FF EE DD CC BB AA 99 88
FF EE DD CC BB AA 99 88 FF EE DD CC BB AA 99 88
FF EE DD CC BB AA 99 88 EE CC 8E 8C 88 88 F8 C8

$A0100,
88 88 88 88 88 88 88 88 88 88 88 88 88 88 88 88
88 88 88 88 88 88 88 88 88 88 88 88 88 88 88 88
88 88 88 88 88 88 88 88 88 88 88 88 88 88 88 88
88 88 88 88 88 88 88 88 88 88 88 88 88 88 88 88
FF EE DD CC BB AA 99 88 FF EE DD CC BB AA 99 88
FF EE DD CC BB AA 99 88 FF EE DD CC BB AA 99 88
FF EE DD CC BB AA 99 88 FF EE DD CC BB AA 99 88
FF EE DD CC BB AA 99 88 88 88 C8 C8 88 88 C8 C8

$A0180,
FF FF FF FF FF FF FF FF EE EE EE EE EE EE EE EE
DD DD DD DD DD DD DD DD CC CC CC CC CC CC CC CC
BB BB BB BB BB BB BB BB AA AA AA AA AA AA AA AA
99 99 99 99 99 99 99 99 88 88 88 88 88 88 88 88
FF FF FF FF FF FF FF FF EE EE EE EE EE EE EE EE
DD DD DD DD DD DD DD DD CC CC CC CC CC CC CC CC
BB BB BB BB BB BB BB BB AA AA AA AA AA AA AA AA
99 99 99 99 99 99 99 99 F8 C8 8F 8C 8E 8C 8C 8C
```

Listing of ROB385.

Addresses and data are hexadecimal

```
$A0000;
4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4
```

this pattern is repeated until

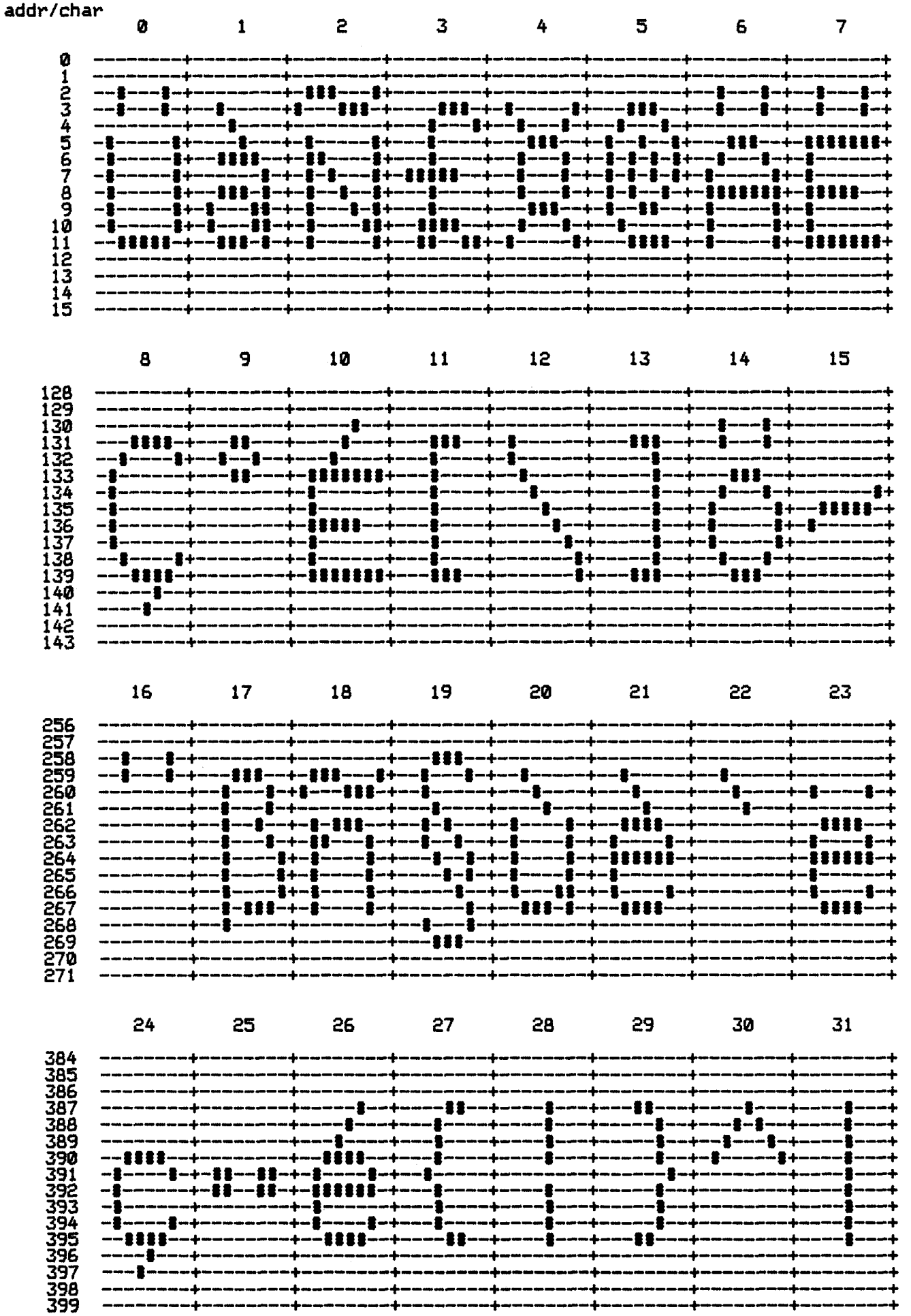
```
$A0200;
3 3 3 3 3 6 6 3 3 3 3 3 3 6 6 3
3 3 3 3 3 6 6 3 3 3 3 3 3 6 6 3
3 3 3 3 3 6 6 3 3 3 3 3 3 6 6 3
3 3 3 3 3 6 6 3 3 3 3 3 3 6 6 3
3 3 3 3 3 6 6 3 3 3 3 3 3 6 6 3
3 3 3 3 3 6 6 3 3 3 3 3 3 6 6 3
3 3 3 3 3 6 6 3 3 3 3 3 3 6 6 3
3 3 3 3 3 6 6 3 3 3 3 3 3 6 6 3

$A0280;
1 1 1 1 1 2 2 1 5 5 5 5 5 7 7 5
1 1 1 1 1 2 2 1 5 5 5 5 5 7 7 5
1 1 1 1 1 2 2 1 1 1 1 1 1 2 2 1
5 5 5 5 5 7 7 5 5 5 5 5 5 7 7 5
0 0 0 0 0 2 2 0 0 0 0 0 0 2 2 0
0 0 0 0 0 2 2 0 0 0 0 0 0 2 2 0
0 0 0 0 0 2 2 0 0 0 0 0 0 2 2 0
0 0 0 0 0 2 2 0 0 0 0 0 0 2 2 0

$A0300;
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3

$A0380;
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3
```

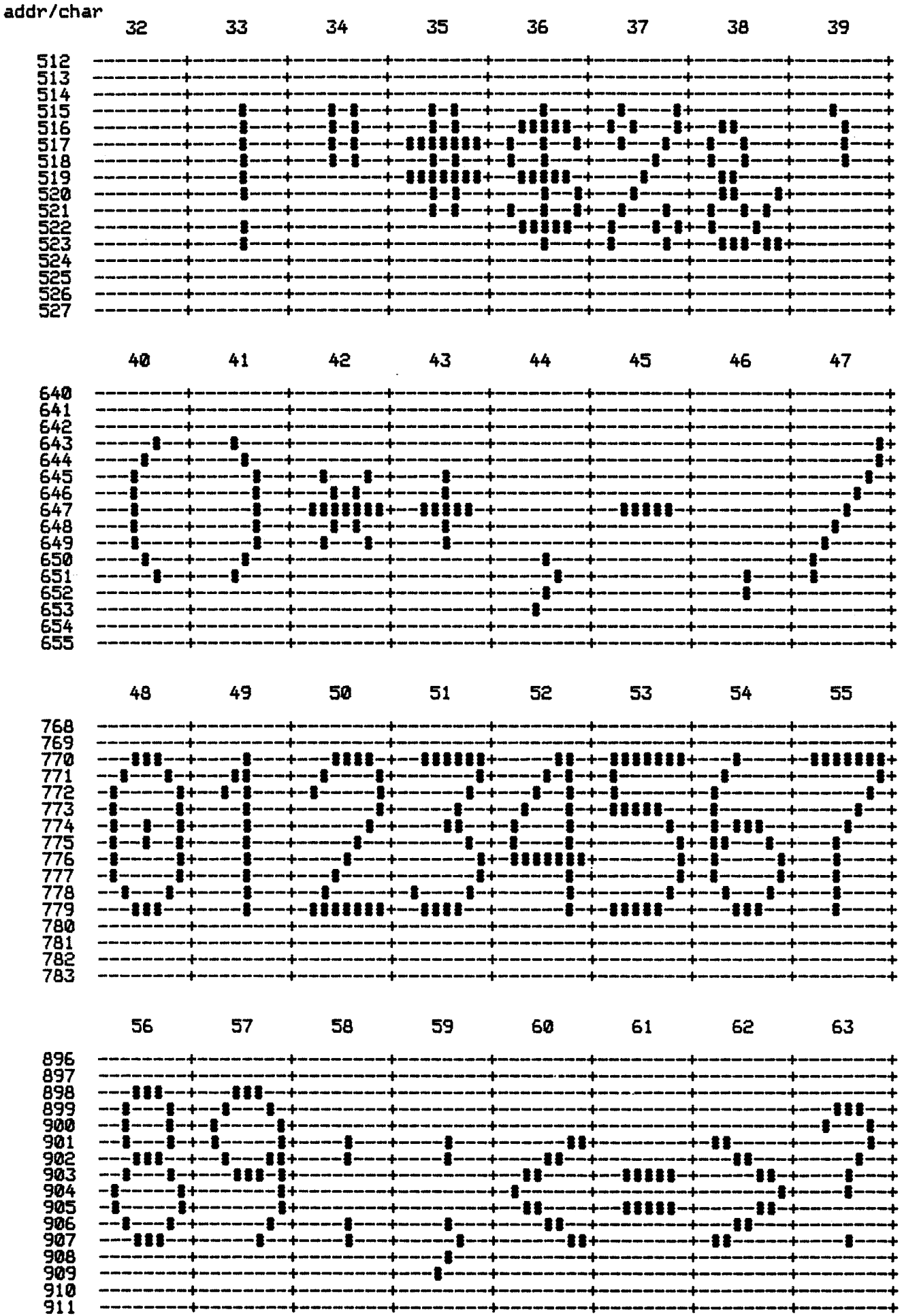
5. CHARACTER ROM 5.

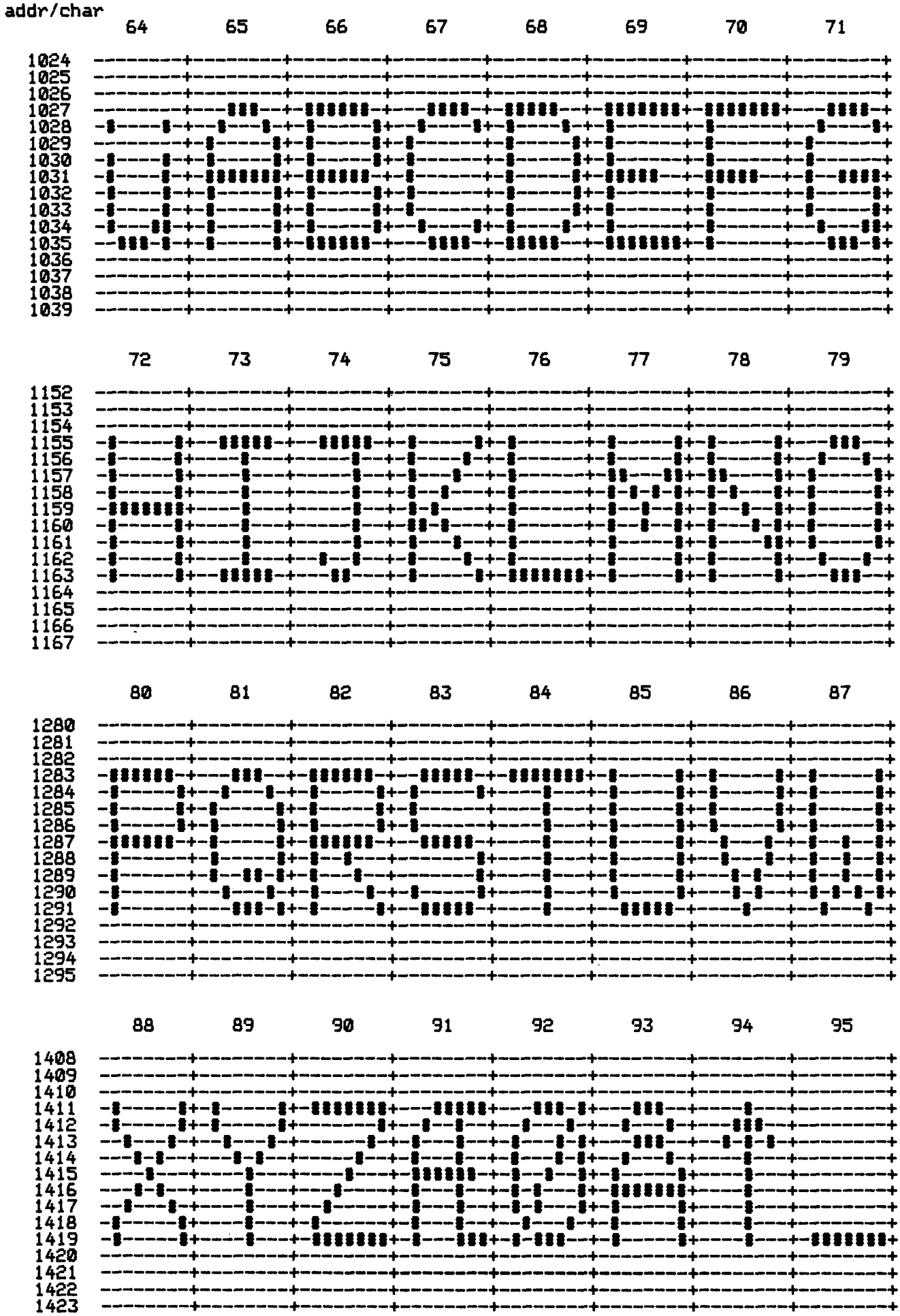
The character ROM used is ROB270 containing 4096 x 8 bit, and is installed in position ?.

The following 8 pages give a listing if ROB270 organized in groups of 16 by 8 words. The address of the first word in a line is indicated in the left margin. The address of the next word on the same line is found by adding 16 to this address etc. Each word is organized with the least significant bit first. Dots are represented with a 1 in the ROM.

Contents of ROB270 page 1 of 8.




addr/char
32 33 34 35 36 37 38 39
512 513 514 515 516 517 518 519 520 521 522 523 524 525 526 527
40 41 42 43 44 45 46 47
640 641 642 643 644 645 646 647 648 649 650 651 652 653 654 655
48 49 50 51 52 53 54 55
768 769 770 771 772 773 774 775 776 777 778 779 780 781 782 783
56 57 58 59 60 61 62 63
896 897 898 899 900 901 902 903 904 905 906 907 908 909 910 911


addr/char
64 65 66 67 68 69 70 71
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
72 73 74 75 76 77 78 79
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
80 81 82 83 84 85 86 87
1280
1281
1282
1283
1284
1285
1286
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1288
1289
1290
1291
1292
1293
1294
1295
88 89 90 91 92 93 94 95
1408
1409
1410
1411
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1416
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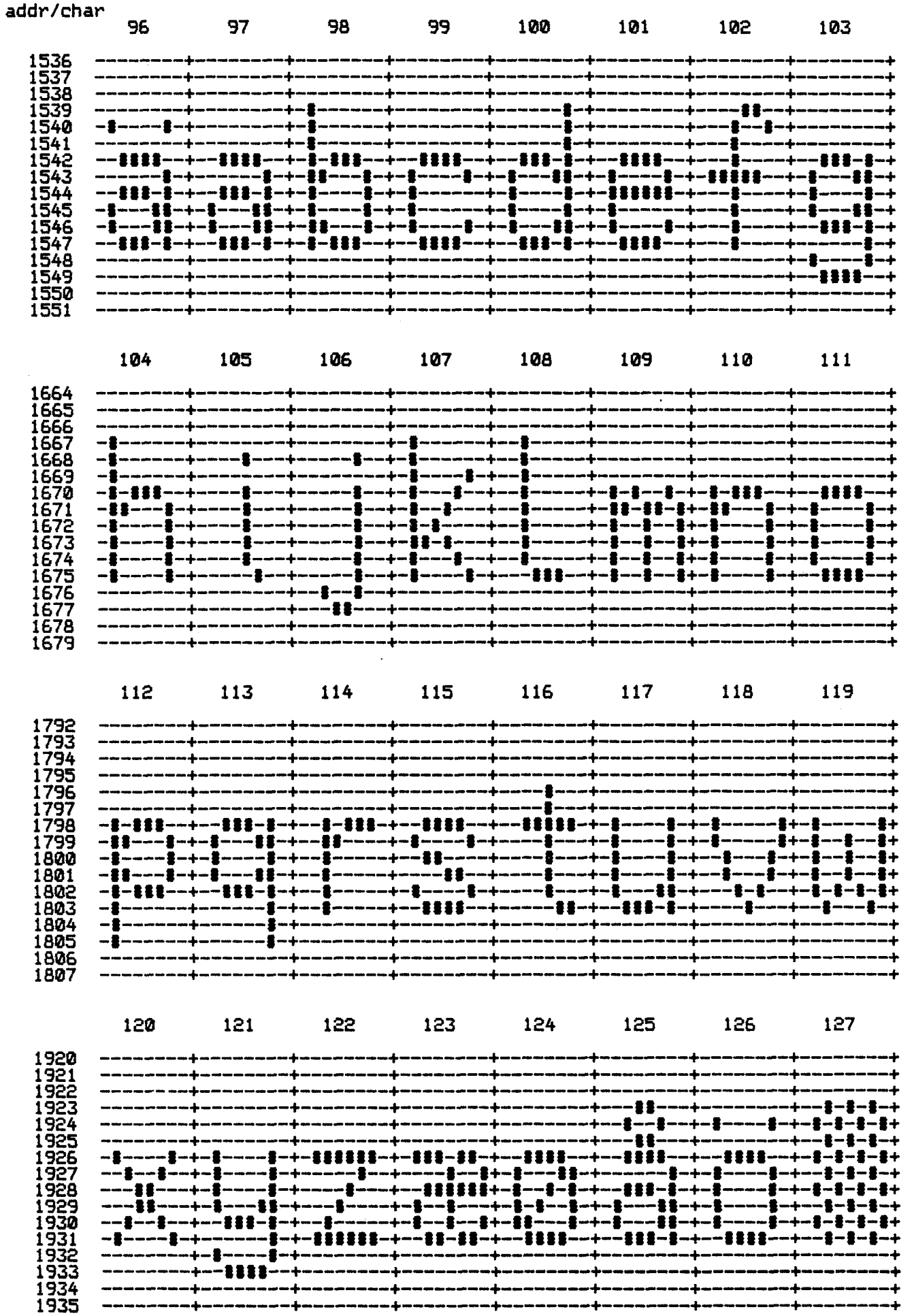
1419
1420
1421
1422
1423

addr/char


96 97 98 99 100 101 102 103
1536
1537
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1549
1550
1551
104 105 106 107 108 109 110 111
1664
1665
1666
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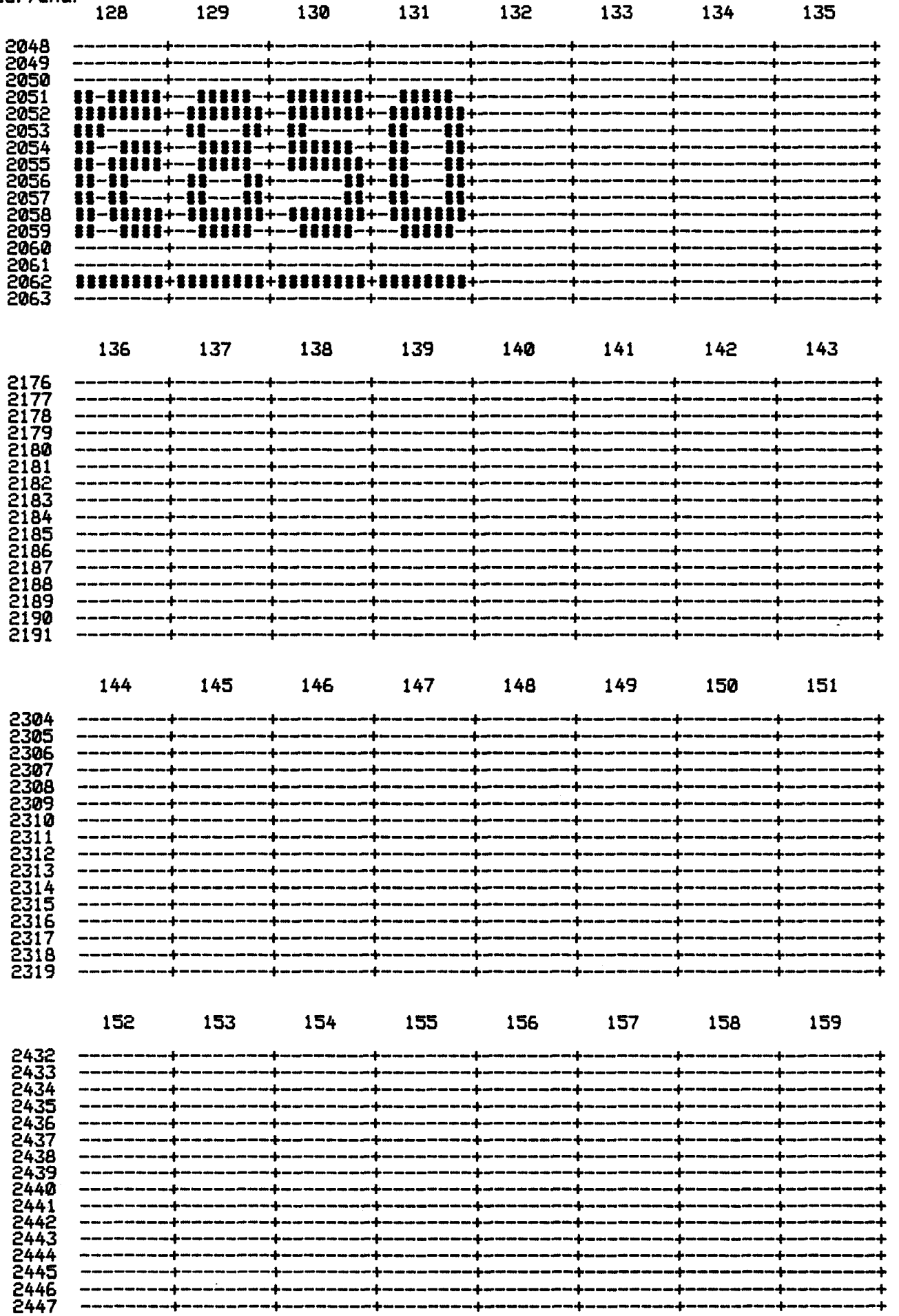
1672
1673
1674
1675
1676
1677
1678
1679
112 113 114 115 116 117 118 119
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
120 121 122 123 124 125 126 127
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935

addr/char


128 129 130 131 132 133 134 135
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
136 137 138 139 140 141 142 143
2176
2177
2178
2179
2180
2181
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2183
2184
2185
2186
2187
2188
2189
2190
2191
144 145 146 147 148 149 150 151
2304
2305
2306
2307
2308
2309
2310
2311
2312
2313
2314
2315
2316
2317
2318
2319
152 153 154 155 156 157 158 159
2432
2433
2434
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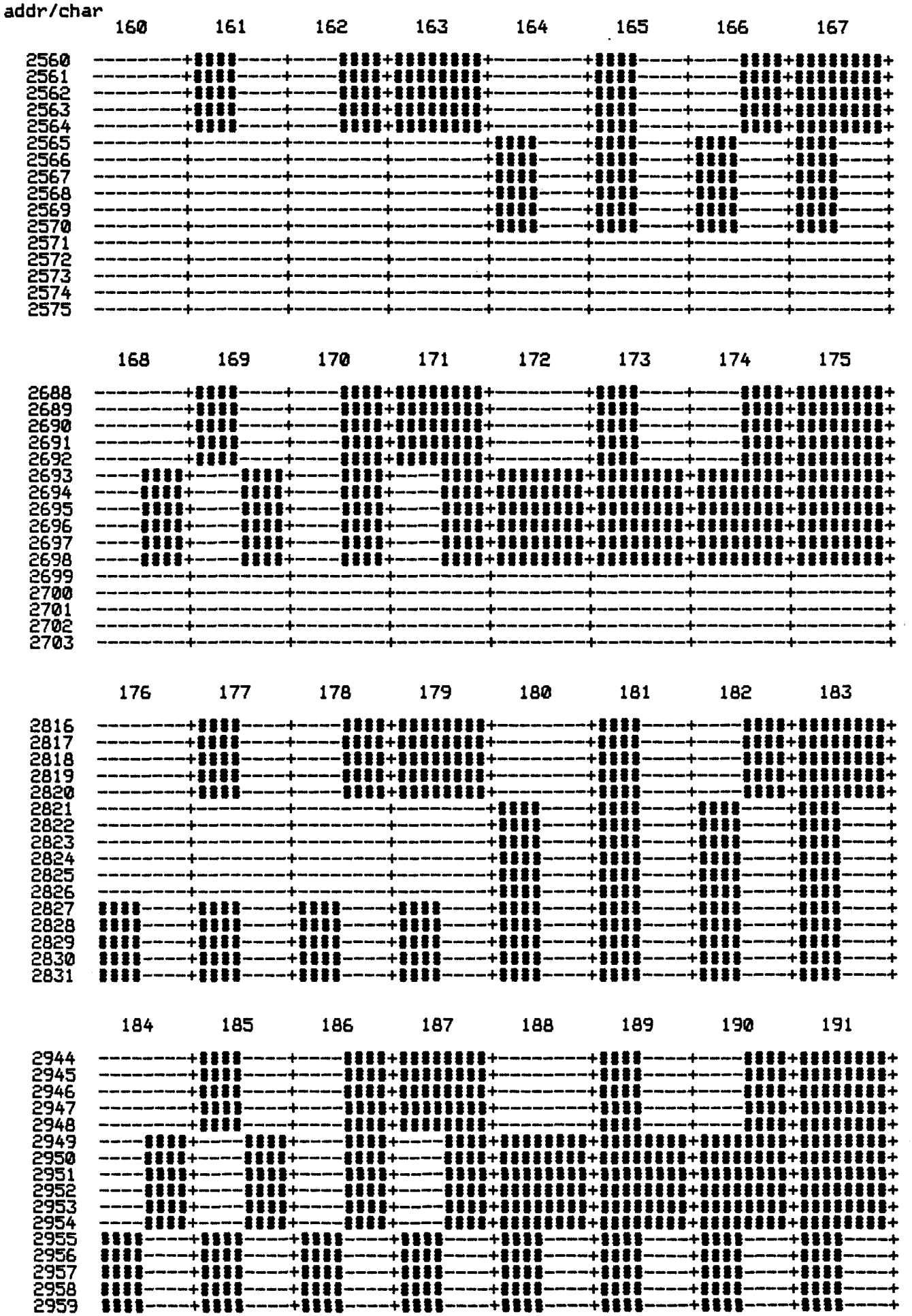
2446
2447


addr/char
160 161 162 163 164 165 166 167
2560
2561
2562
2563
2564
2565
2566
2567
2568
2569
2570
2571
2572
2573
2574
2575
168 169 170 171 172 173 174 175
2688
2689
2690
2691
2692
2693
2694
2695
2696
2697
2698
2699
2700
2701
2702
2703
176 177 178 179 180 181 182 183
2816
2817
2818
2819
2820
2821
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2823
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2825
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2828
2829
2830
2831
184 185 186 187 188 189 190 191
2944
2945
2946
2947
2948
2949
2950
2951
2952
2953
2954
2955
2956
2957
2958
2959

addr/char

	192	193	194	195	196	197	198	199
3072								
3073								
3074								
3075								
3076								
3077								
3078								
3079								
3080								
3081								
3082								
3083								
3084								
3085								
3086								
3087								

	200	201	202	203	204	205	206	207
3200								
3201								
3202								
3203								
3204								
3205								
3206								
3207								
3208								
3209								
3210								
3211								
3212								
3213								
3214								
3215								

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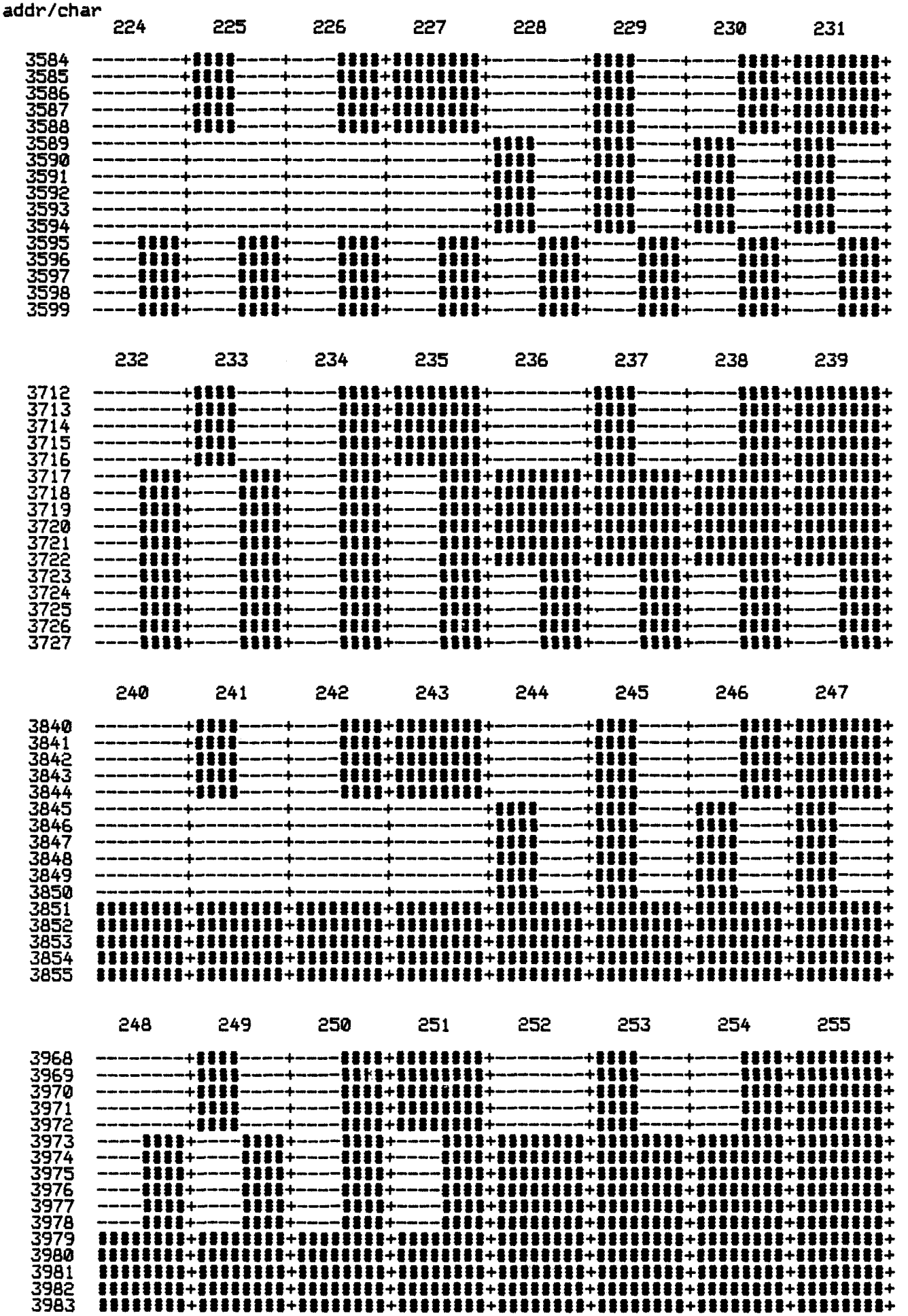
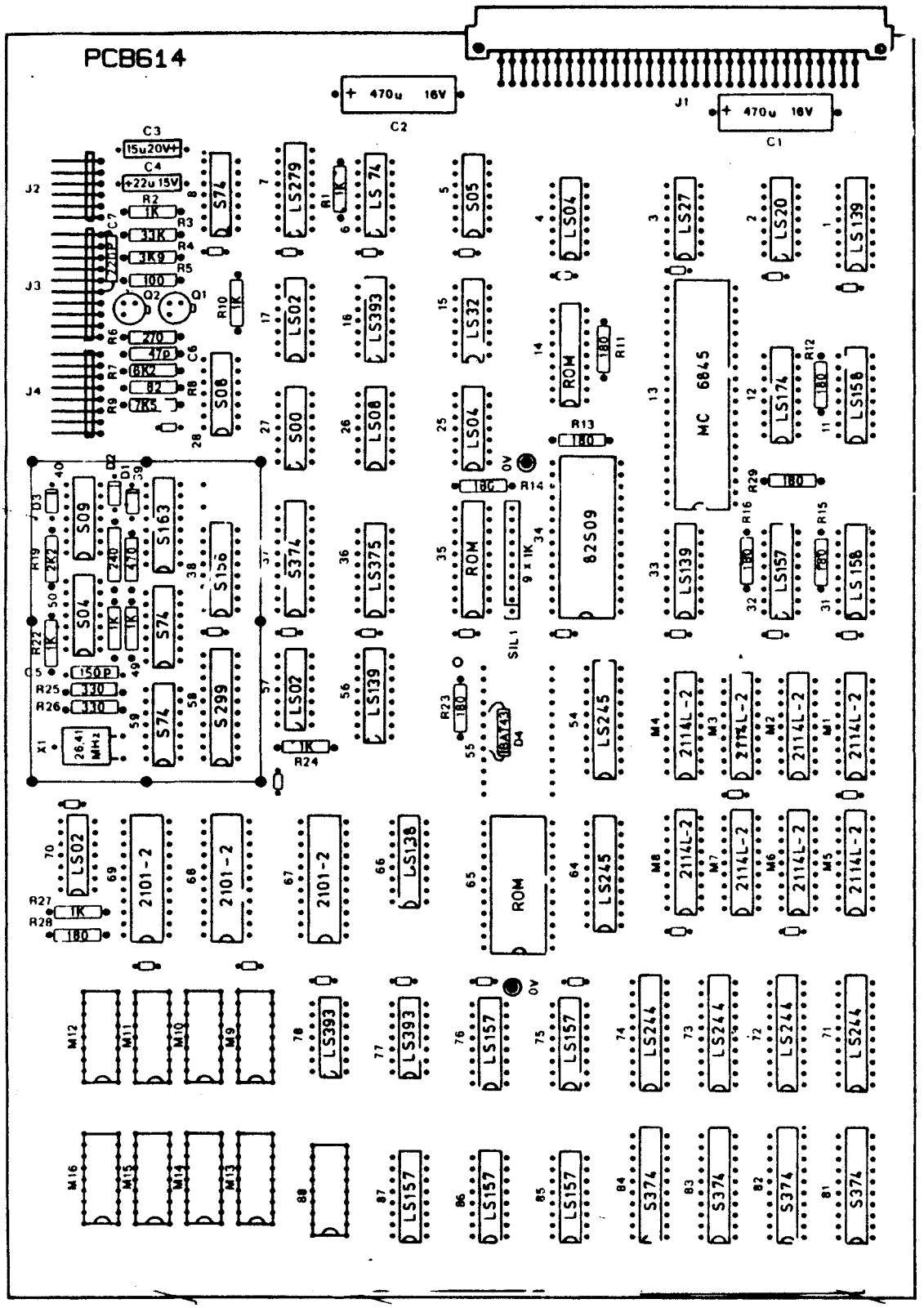
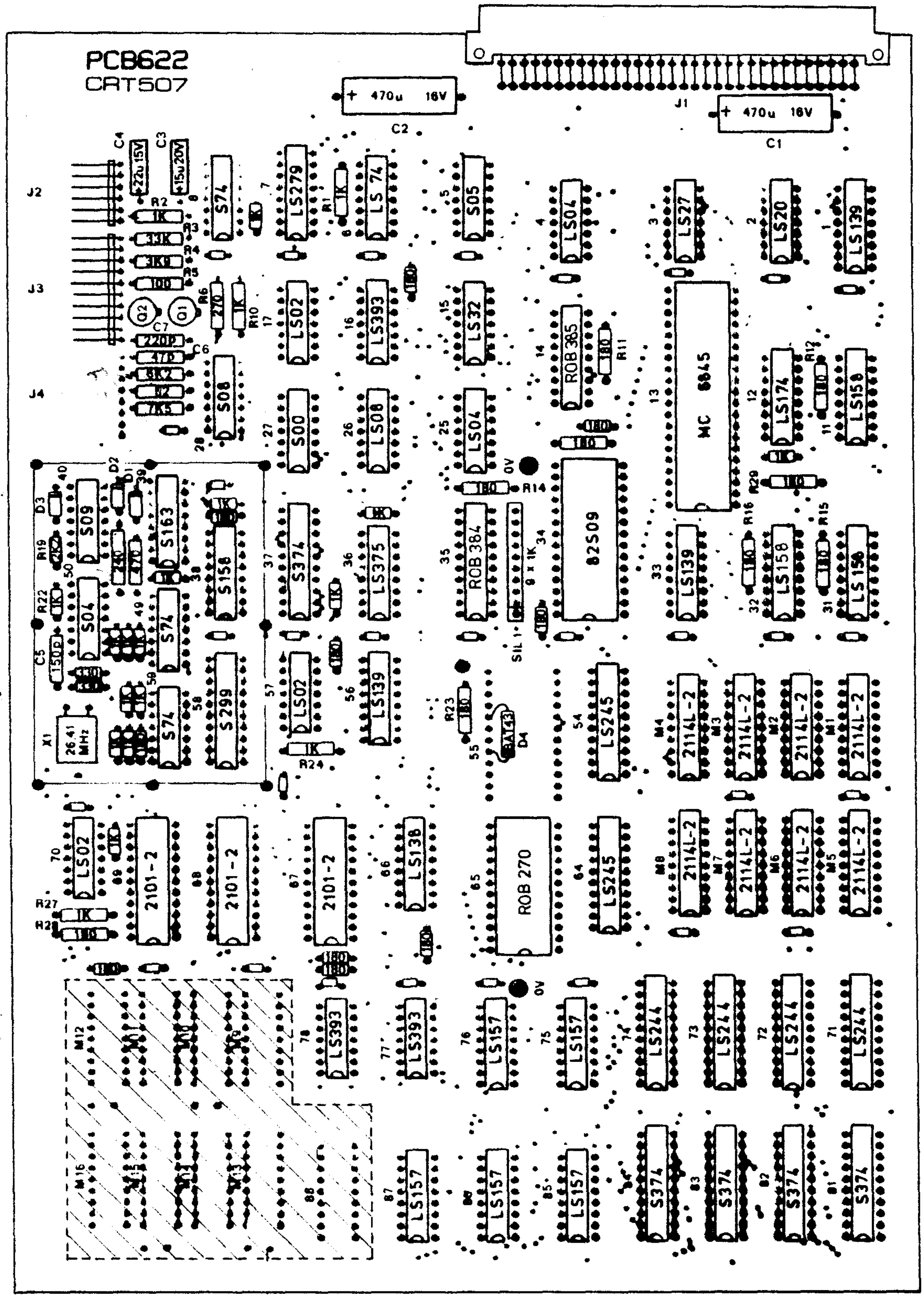
Contents of ROB270 page 8 of 8.



6. ASSEMBLY DRAWING

6.1 CRT505




PCB622
CRT507
470u 16V
C2
J1
470u 16V
C1
J2
J3
J4
S74
LS279
LS 74
S05
LS04
LS27
LS20
LS139
LS02
LS393
LS32
ROB 385
MC 6845
LS174
LS158
S08
S00
LS08
LS04
S09
S163
S158
S374
LS375
ROB 384
82S09
LS139
LS158
LS 158
S04
S74
S299
LS02
LS139
LS245
2114L-2
26.41 MHz
R24
LS02
2101-2
2101-2
2101-2
LS138
ROB 270
LS245
LS393
LS393
LS157
LS157
LS244
LS244
LS244
LS244
LS157
LS157
LS157
S374
S374
S374
S374

7. PLUGS

J1. pin	A	C
1		
2		
3	-,DISP INTR	
4	-,IORD	GND
5	-,IOWR	25Hz
6		
7	-,MEMWR	-,TC
8	BUS1	BUS0
9	BUS3	BUS2
10	BUS5	BUS4
11	BUS7	BUS6
12		
13	ADD0	ADD2
14	Chain	Chain
15		ADD1
16	ADD4	
17	-,WAIT	ADD3
18	ADD5	ADD15
19	ADD6	ADD14
20	ADD7	ADD13
21	-,DACK 0	ADD12
22		ADD11
23	DRQ 0	ADD10
24		ADD9
25		ADD8
26		
27	CLK	-,RESET
28	-,HOLD ACK	
29		-,POWER RESET
30		
31		
32	+12V	+12V

J2. pin

1	Contrast pot. max
2	Contrast pot. top
3	Contrast pot. min
4	Intensity pot. max
5	Intensity pot. tap
6	Intensity pot. min

J3. BW Monitor connected to CBL

pin

1	GND
2	Intensity max
3	Intensity min
4	Intensity top
5	Not used
6	Horizontal sync
7	Not used
8	Video
9	Vertical sync
10	GND

J4. Colour monitor

pin

1	
2	RED
3	GREEN
4	BLUE
5	GND
6	GND
7	-,Horizontal sync
8	-,Vertical sync

RETURN LETTER

Title: CRT505/507 - CRT controller Technical Manual

RCSL No.: 44-RT2067

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Do you find errors in this manual? If so, specify by page.

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_____

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Other comments?

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_____

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Company: _____

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