RCSL No: 44-RT2032

Edition: October 1982

Author: Peter Koch Andersson

Title:

CRT504 - CRT Controller
Technical Manual

RCSL 42-i1905

A/S REGNECENTRALEN
af 1979

Keywords:

RC850, CRT504, CRT controller.

Abstract:

This manual contains all relevant technical information on CRT504.

(46 printed pages)

Printed by A/S Regnecentralen af 1979, Copenhagen

RCSL 42-i1905

TABLE OF CONTENTS PAGE

1. DESCRIPTION 1.

CRT504 is the interface between MIC50x and the CRT monitor.

CRT504 displayes continously the contents of a 2 k x 16 bit refresh memory, which is maintained as a copy of the highest 4 k bytes of main memory (i.e. addresses F000 to FFFF): Every time a byte is written in this area, it is written into the corresponding address of the refresh memory as well. Each pair of addresses in the refresh memory corresponds to a position on the screen.

The first byte plus one bit of the second selects a character in the character font to be displayed. Two bits in the second select a shadow character to be superponed the first. The remaining bits (the attribute selectors) select one out of 32 programdefined combinations of the 8 attributes, which control the display of the character.

1.1 Refresh Memory 1.1

The address multiplexer U12, U11, U1 (p11) to the refresh memory is controlled by CCLK. CCLK is low during the last half of the character period, letting the CRT controller read the character for display. During the first CCLK phase however, the refresh memory is addressed with the MIC address lines, making write access possible.

The leading edge of a write to the refresh area is caught in the F.F. U16 (p11), generating a write request, which is syncronized to CCLK in the F.F. U50 (p11) which makes U40 (p11) generate a writepulse beginning after CCLK goes high and ending before CCLK goes low. U40 is reset by U60-6 giving a low pulse before CCLK falls.

During the refresh phase, the refresh memory is addressed by the CRT controller MC6845 and the read data is locked into the buffer register on the rising edge of CCLK.

1.2 Character Font 1.2

The character font consists of three memories: a ROM (U64 and U84 p5), containing predefined dot patterns for 128 or 256 characters, a RAM (M9-24 p6), with space for programming of 256 character patterns and a RAM (U66, 67, 86, 87) with space for the programming of 4 dot patterns, one of which is always superponed the character pattern displayed.

The character font contains 16 x 16 bits for each character pattern or shadow pattern and they are read with 32 bits in parallel (DOT 0-15 and SDOT0-15). The SDOT's and DOT's are "ored" together giving 16 compound dots being parallel loaded into the shifter and the shifted out one dot at the time at a frequency of 32 MHz.

1.3 Video Generation 1.3

The output of the dot shifter is used to select the display of foregound or background. Foreground and background are defined for each character position in the refresh memory by 5 bits. The 5 bits are used to select one out of 32 combinations of 8 attributes stored in the attribute RAM (U48 and U49 p3).

Seven of the attributes are converted into a back- and foreground colour or grey scale value, in the attribute ROM ROB046, U39 p3.

The last attribute bit is used to hide the character by disabling dots for that character.

The three colour signals from the dot selector go to J4 for a colour monitor or to the D/A converter on p1 generating a grey scale video signal for a BW monitor.

1.4 DMA

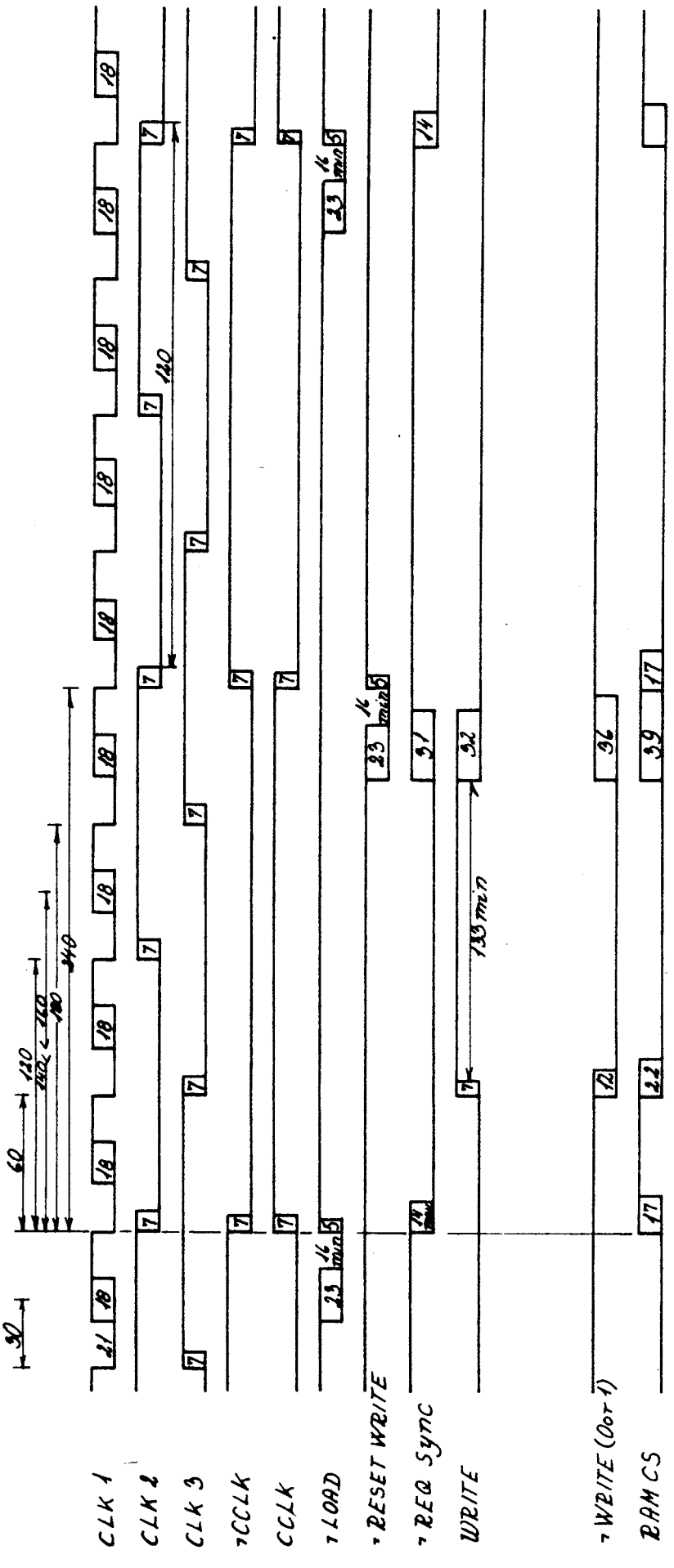
1.4

The character fonts and the attribute RAM are accessed from the MIC board via DMA, controlled by the DMA controller on the MIC board.

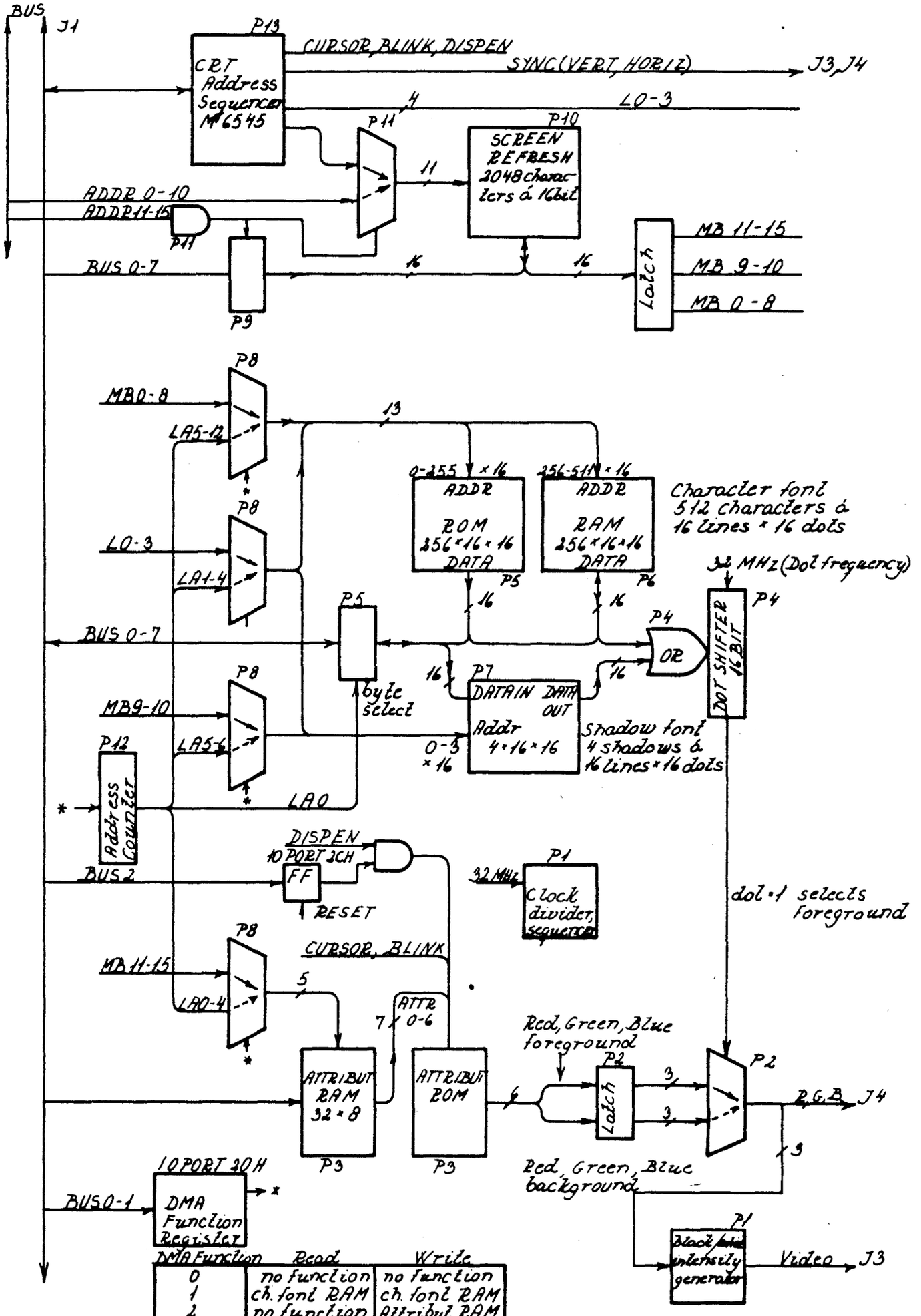
The memory to be accessed is selected with an I/O write command to port 20 Hex. This write command clears the load address counter and sets the DMA RUN flipflop U5a p12, which then lets the DRQ EN flip-flop U56 p12 generate a DMA REQ next time DISP EN goes low (during horizontal retrace). The DMA REQ (REQ 0) makes the DMA controller perform two DMA cycles: DRQ EN is reset only after the LA counter (bit 0) is counted up on the trailing edge of DMA ACK, this causes the DMA controller to generate the second DMA cycle. So DMA transfers take place with two bytes every 64 microsecond, always starting with the even byte.

2. TIMING DIAGRAM

2.



3. BLOCK DIAGRAM



DMA Function	Read	Write
0	no function	no function
1	ch. font RAM	ch. font RAM
2	no function	Attribut RAM
3	ch. font ROM	Shadow RAM

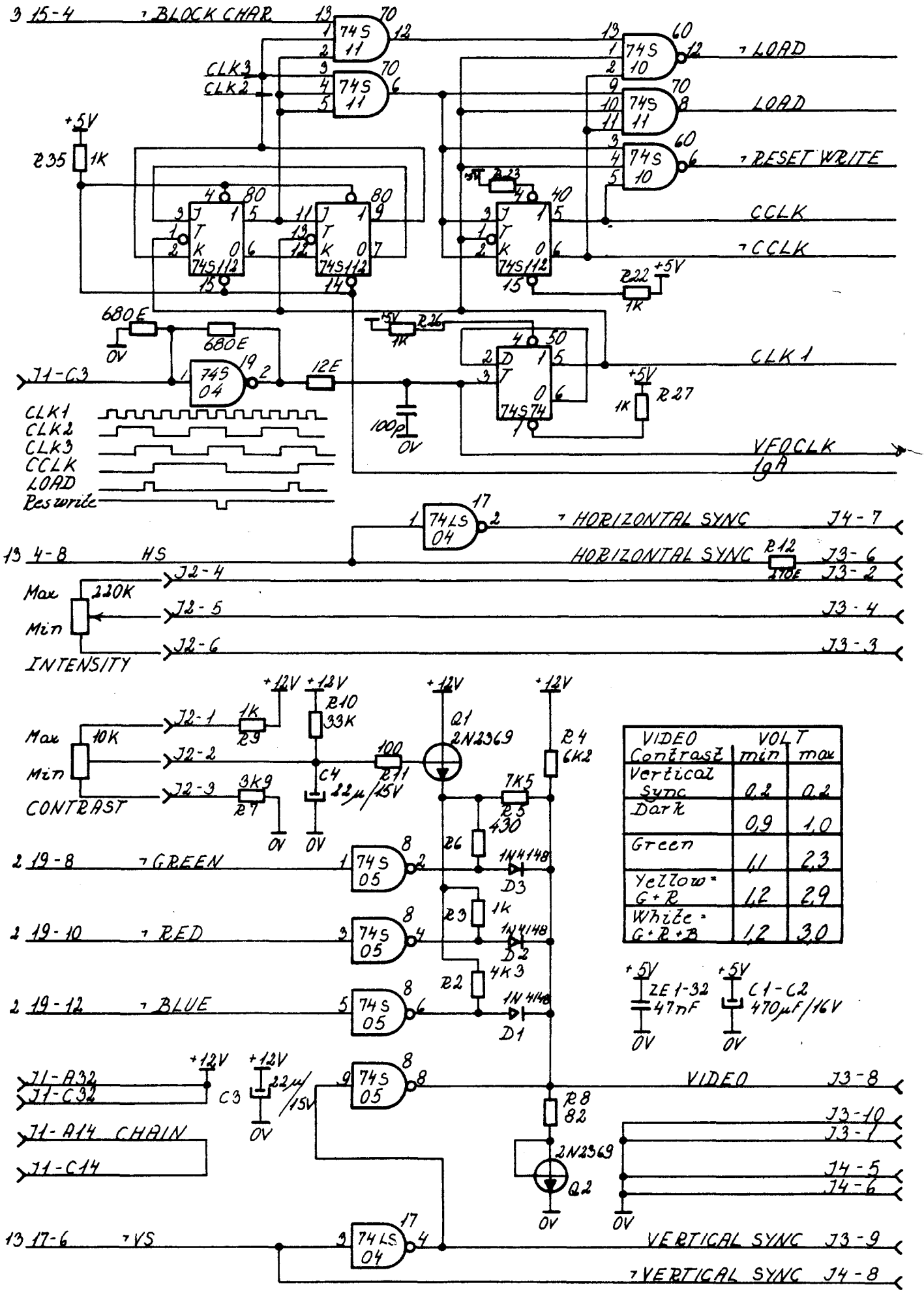
4. LOGIC DIAGRAMS AND FUNCTIONAL DESCRIPTION 4.

The following pages contain logic diagrams for CRT504. A functional description is given on the left hand page to the corresponding diagram sheet.

The functional description consists of a schematic listing of all signals generated on the page. A short description and a listing of the diagrams to which the signal is transferred is given for each signal.

Note: All references between individual diagram sheets make use of diagram numbers (lower right corner) and not page numbers.

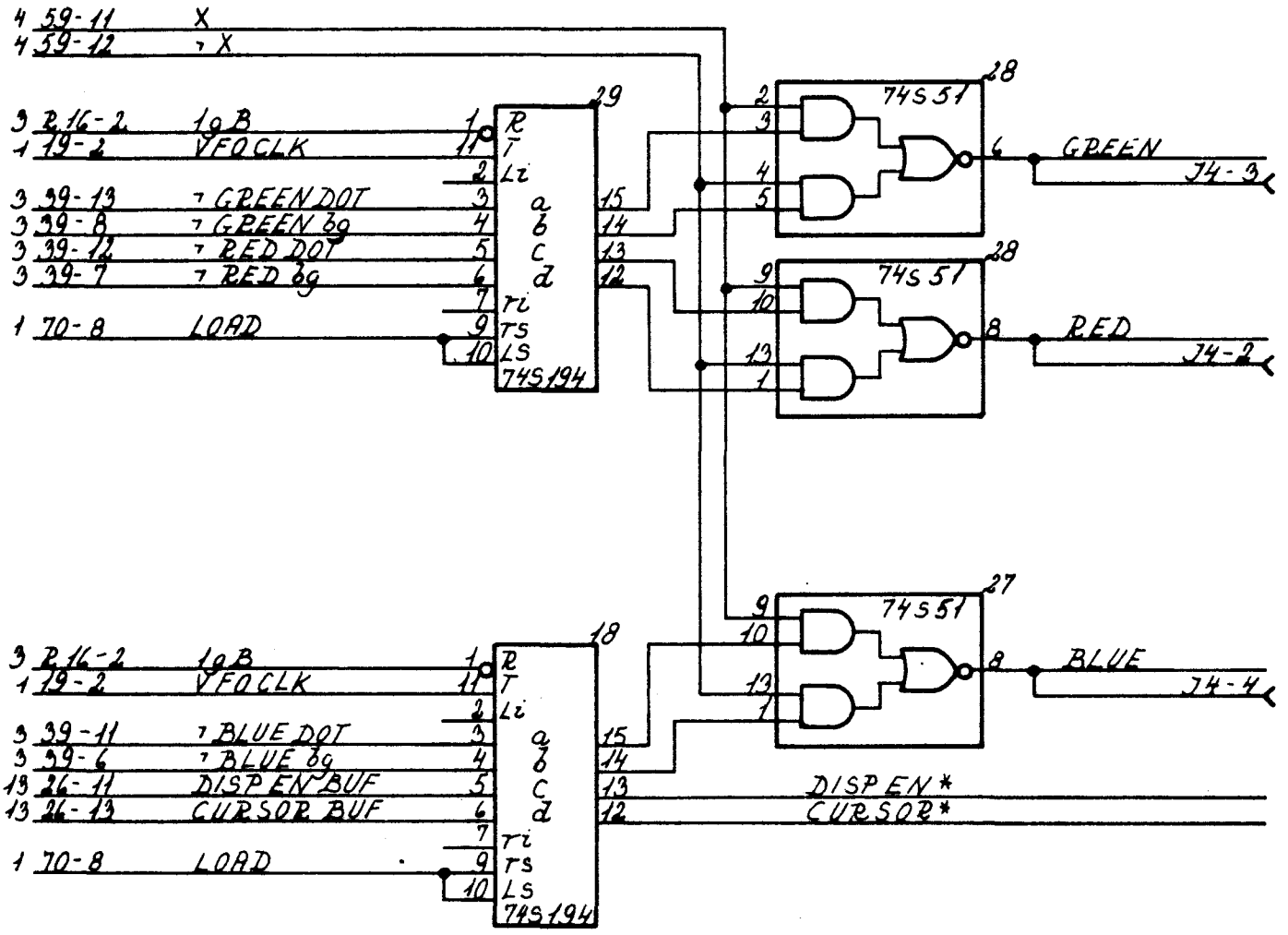
Signal	Destination	Description
-,LOAD	p4	parallel load of dot shifter every 16'th VFO clk, if not block char.
LOAD	p2	Loads dot control register every 16'th VFO CLK.
-,RESET WRITE	p11	Resets the writepulses to the refresh memory.
CCLK	p9, p11	Goes high in the beginning of each character time.
-,CCLK	p9, p13	
CLK1	p11	Alternates at half the frequency of VFO clk.
-,HORIZONTAL SYNC	Colour monitor	
HORIZONTAL SYNC	Black & white monitor	
VIDO	Black & white monitor	Analog video signal.
VERTICAL SYNC	Black & white monitor	
-,VERTICAL SYNC	Colour monitor	

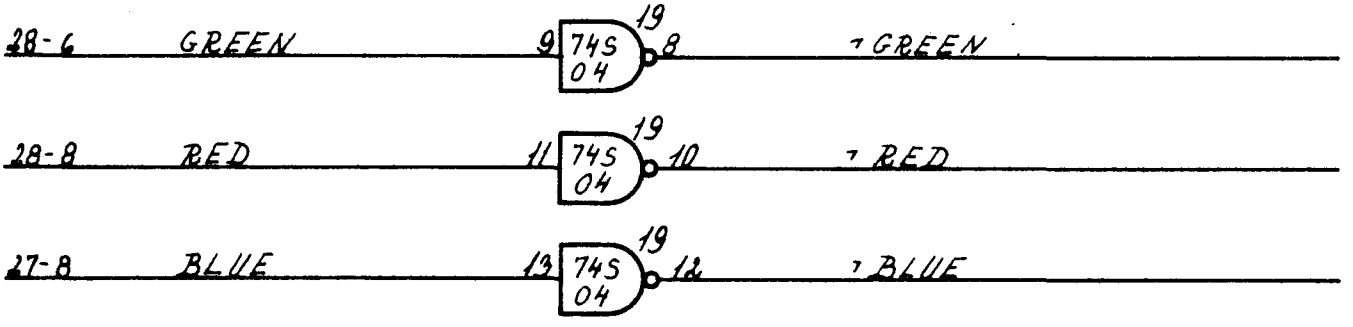


VIDEO Contrast	VOLT min	max
Vertical sync	0,2	0,2
Dark	0,9	1,0
Green	1,1	2,3
Yellow = G+R	1,2	2,9
White = G+R+B	1,2	3,0

AGA 820420
PKA 81 12 21

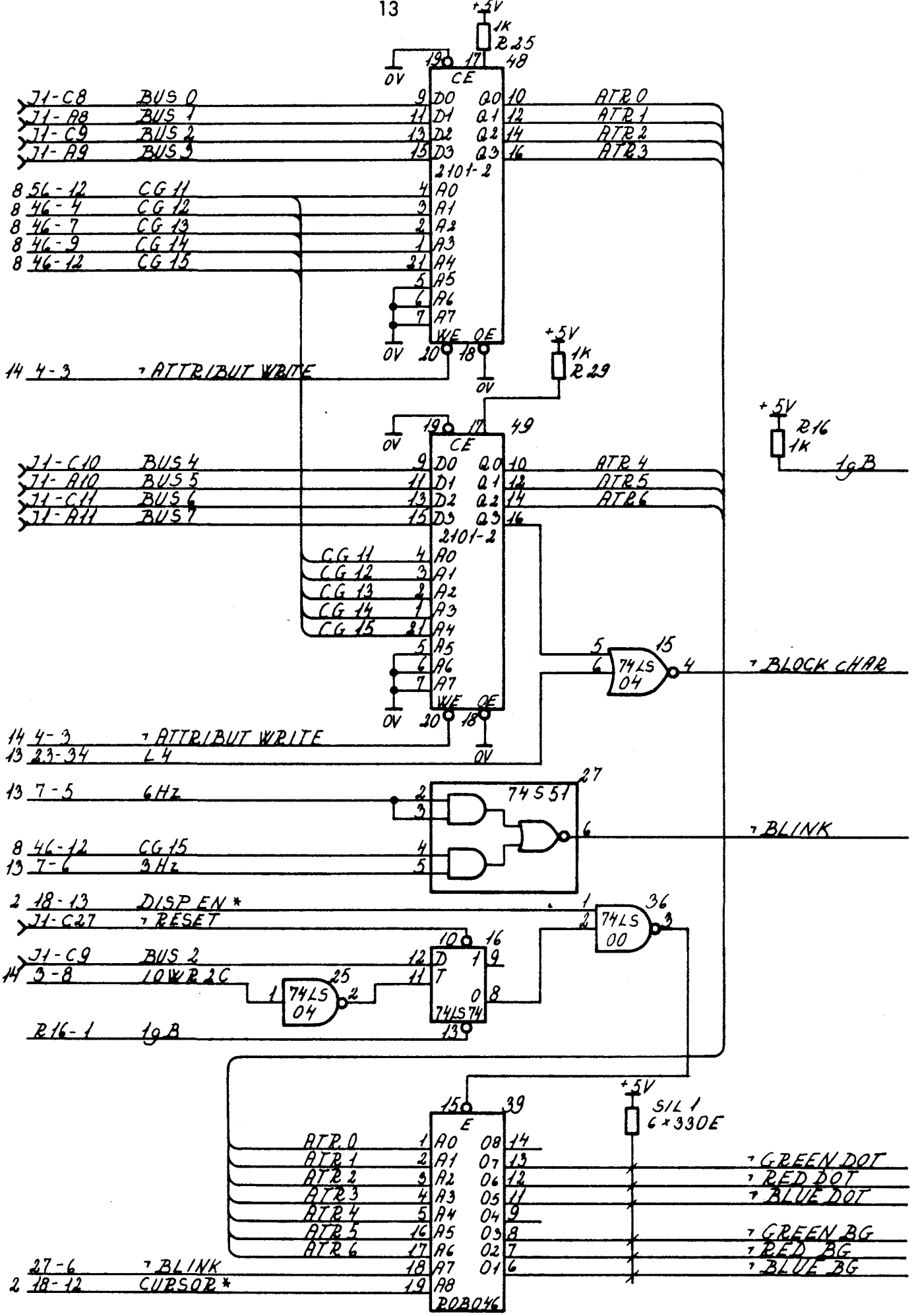
Signal	Destination	Description
Green	Colour monitor	TTL-dot signals.
Red		
Blue		
-,Green	pl	
-,Red	pl	
-,Blue	pl	





81 12 21 PKA RGA 820420

Signal	Destination	Description
ATR 0-6	p3	Output from attribute RAM.
-,GREEN DOT -,RED DOT -,BLUE DOT	p2 p2 p2	Colour of the dots in the character.
-,GREEN BG -,RED BG -,BLUE BG	p2 p2 p2	Colour of the background in the character.
U36-3	p3	Blanks the display by forcing the outputs of U39 high.
-,BLOCK CHAR	p1	Disables dot generation. Only the background is visible in the character.
-,BLINK	p3	Blink frequency to the attribute ROM.

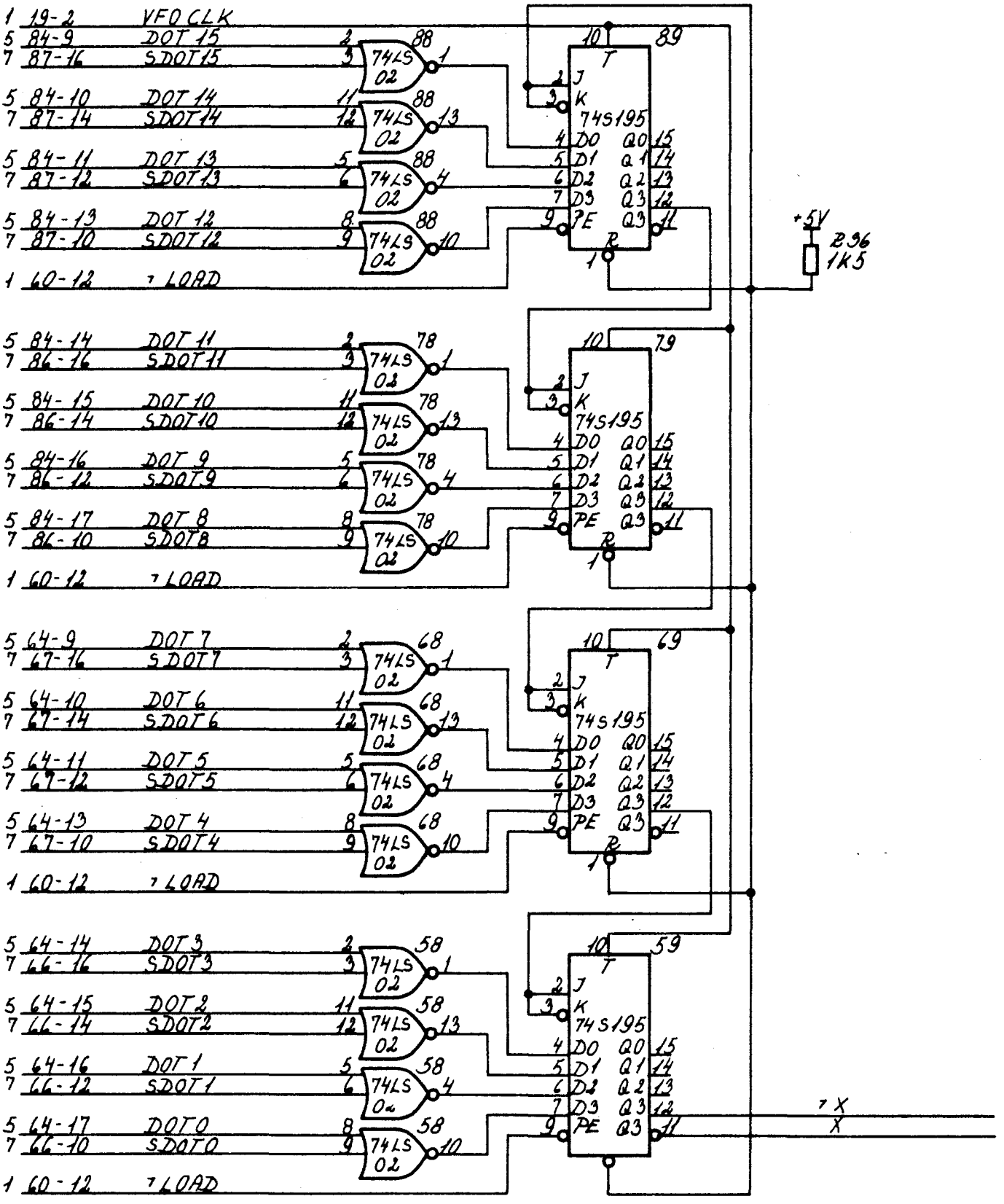


PKA
81.12.21

CRT 504 ATTRIBUT LOGIC 3

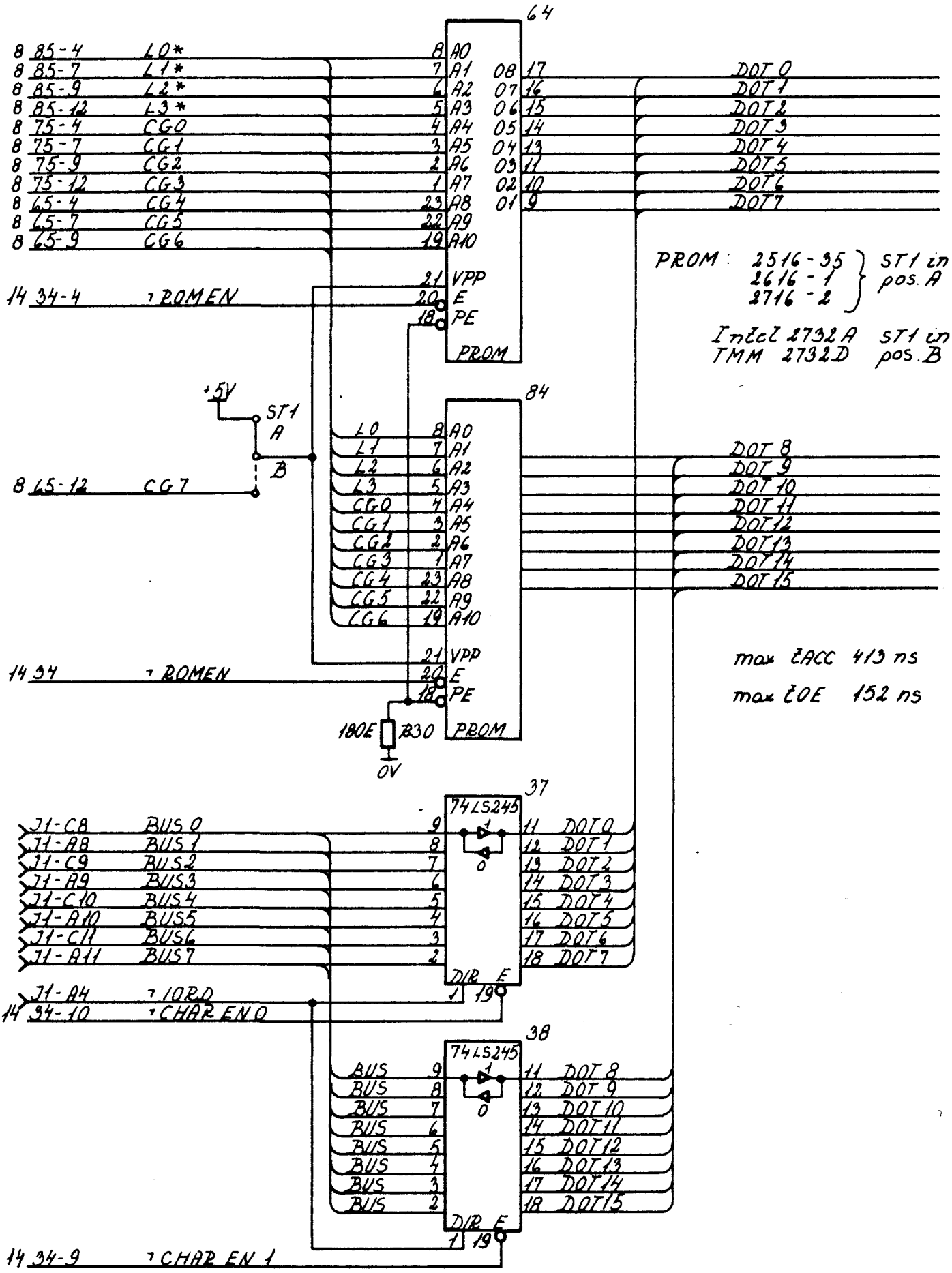
R 13342

Signal	Destination	Description
-,x	p2	Output of dot shifter. When x active a dot is displayed.

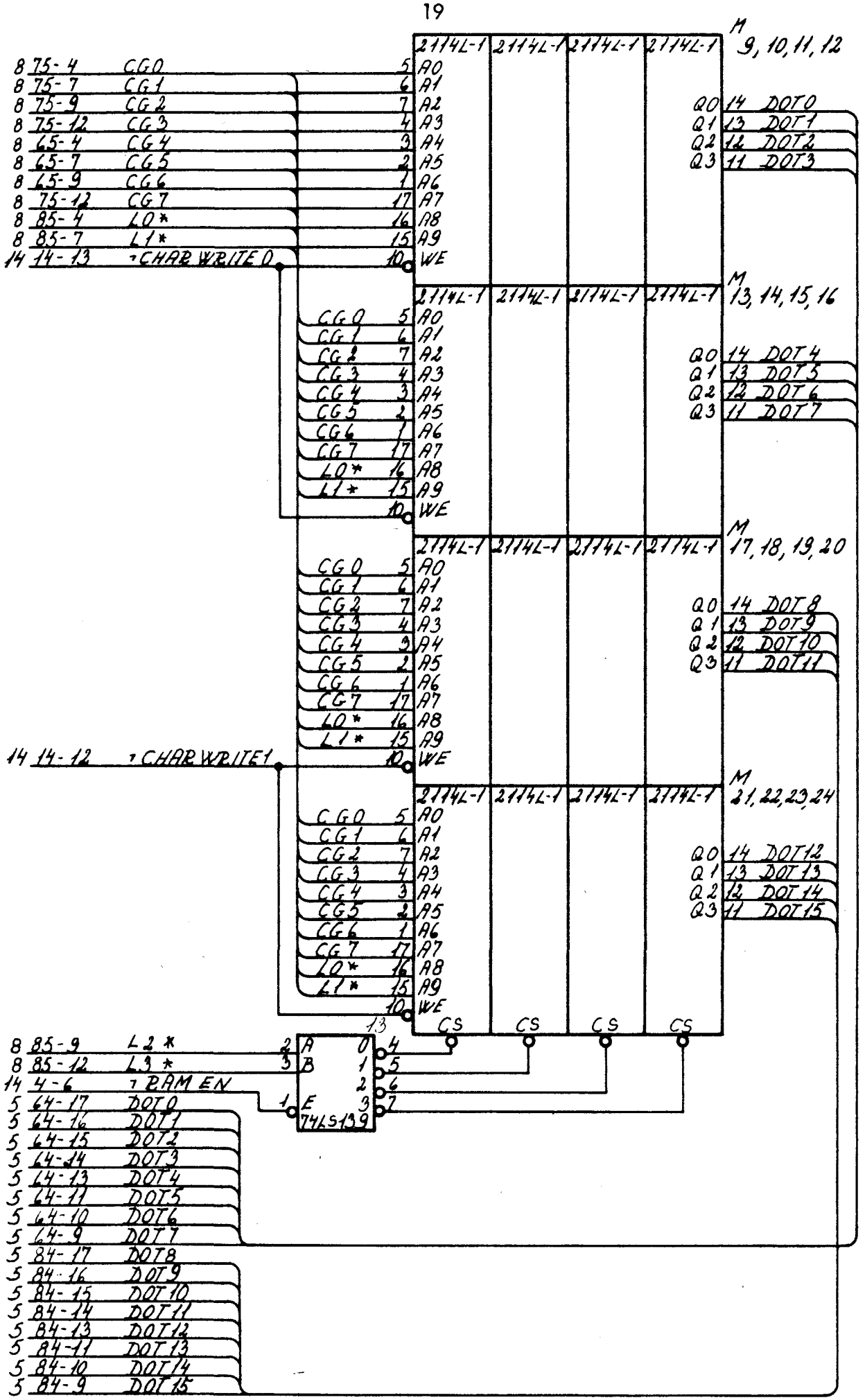


AGA 820420
PKA 811221

Signal	Destination	Description
DOT 0-15	p4, p5, p6	Tristate bus for input to dot shifter. Also accessible from MIC board thrugh U37 and U38. DOT 0-15 are sourced from the character ROM's U64 and U84 or the character RAM's p6.

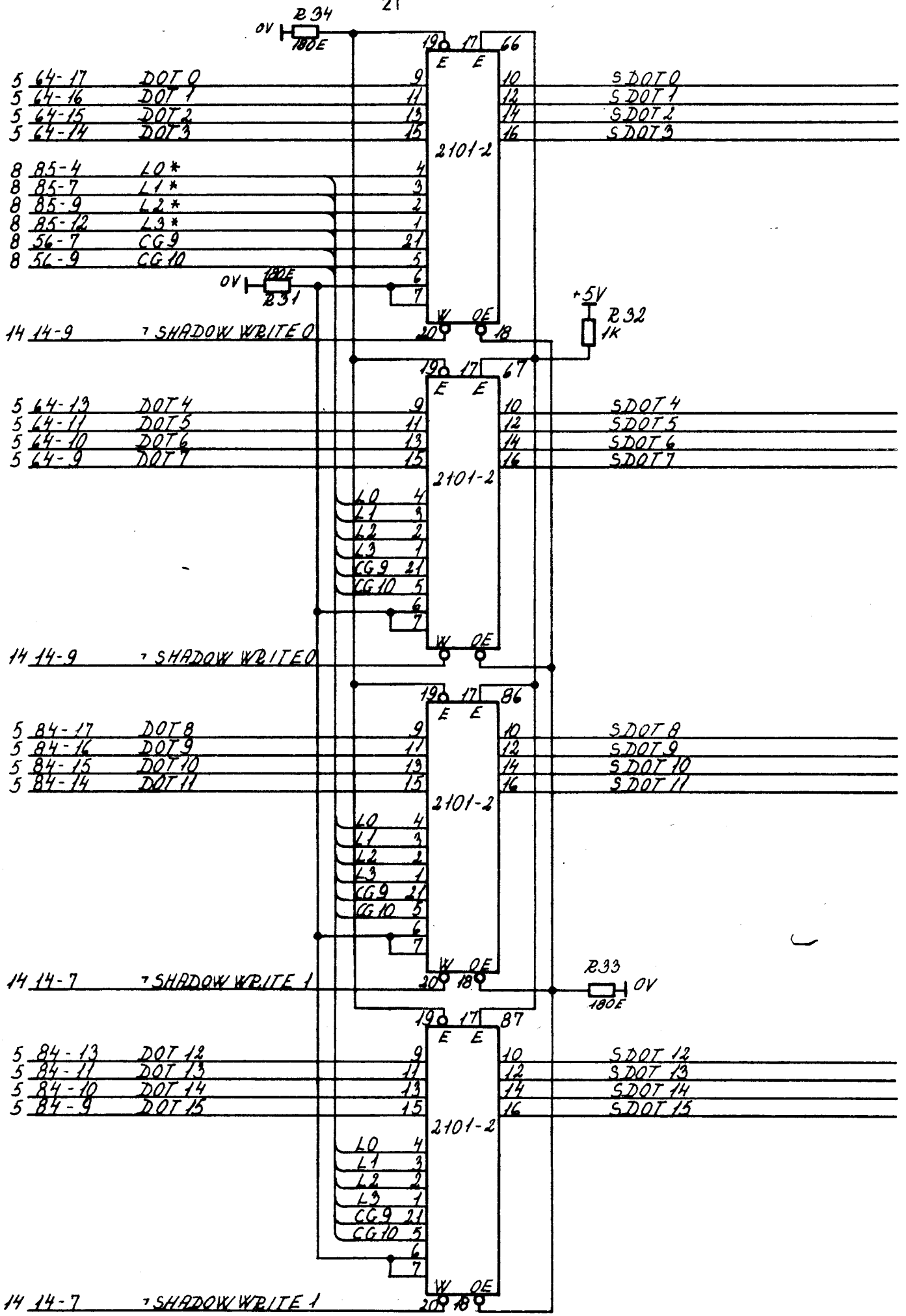

64
8 85-4 LO*
8 85-7 L1*
8 85-9 L2*
8 85-12 L3*
8 75-4 CGO
8 75-7 CG1
8 75-9 CG2
8 75-12 CG3
8 65-4 CG4
8 65-7 CG5
8 65-9 CG6
14 34-4 ↑ROMEN
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
VPP E PE
PROM
DOT 0 DOT 1 DOT 2 DOT 3 DOT 4 DOT 5 DOT 6 DOT 7
PROM: 2516-35 2616-1 2716-2 } ST1 in pos. A
Intel 2732A TMM 2732D ST1 in pos. B
+5V
ST1
A
B
8 65-12 CG7
84
LO L1 L2 L3 CGO CG1 CG2 CG3 CG4 CG5 CG6
DOT 8 DOT 9 DOT 10 DOT 11 DOT 12 DOT 13 DOT 14 DOT 15
max tACC 413 ns
max tOE 152 ns
14 34 ↑ROMEN
180E R30
0V
37
74LS245
J1-C8 BUS 0
J1-A8 BUS 1
J1-C9 BUS 2
J1-A9 BUS 3
J1-C10 BUS 4
J1-A10 BUS 5
J1-C11 BUS 6
J1-A11 BUS 7
DOT 0 DOT 1 DOT 2 DOT 3 DOT 4 DOT 5 DOT 6 DOT 7
D/R E
J1-A4 ↑IORD
14 34-10 ↑CHAR EN 0
38
74LS245
BUS 0 BUS 1 BUS 2 BUS 3 BUS 4 BUS 5 BUS 6 BUS 7
DOT 8 DOT 9 DOT 10 DOT 11 DOT 12 DOT 13 DOT 14 DOT 15
D/R E
14 34-9 ↑CHAR EN 1
AGA 820420
PK-A 811221

Signal	Destination	Description
DOT 0-15	p4, p5	Tristate bus feeding the dot shifter.



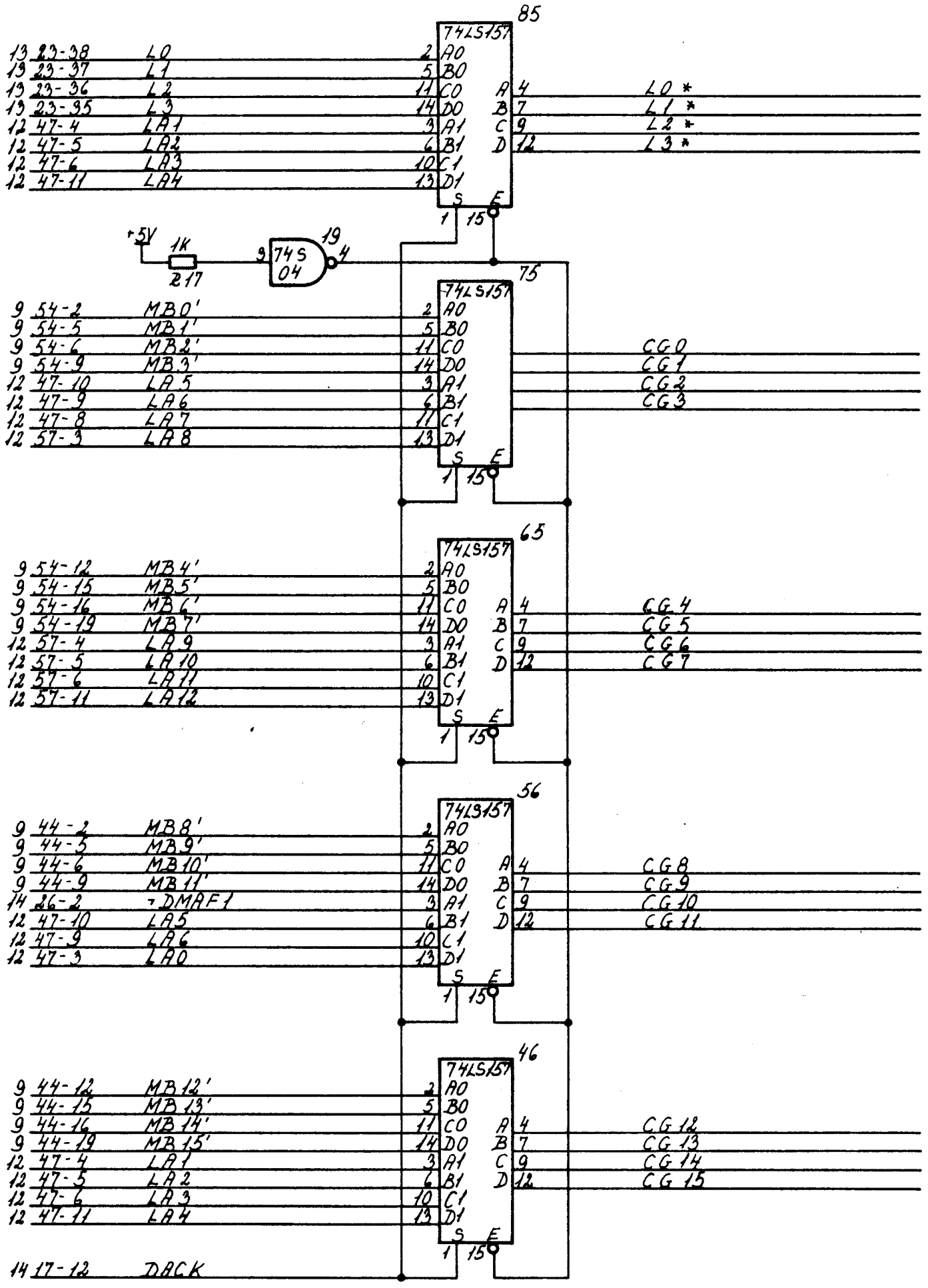
PHA 820430 AGA 81/12/21

Signal	Destination	Description
SDOT 0-15	p4	Are the dots of the shadow character.



81 12 21 PKA 820421 AGA

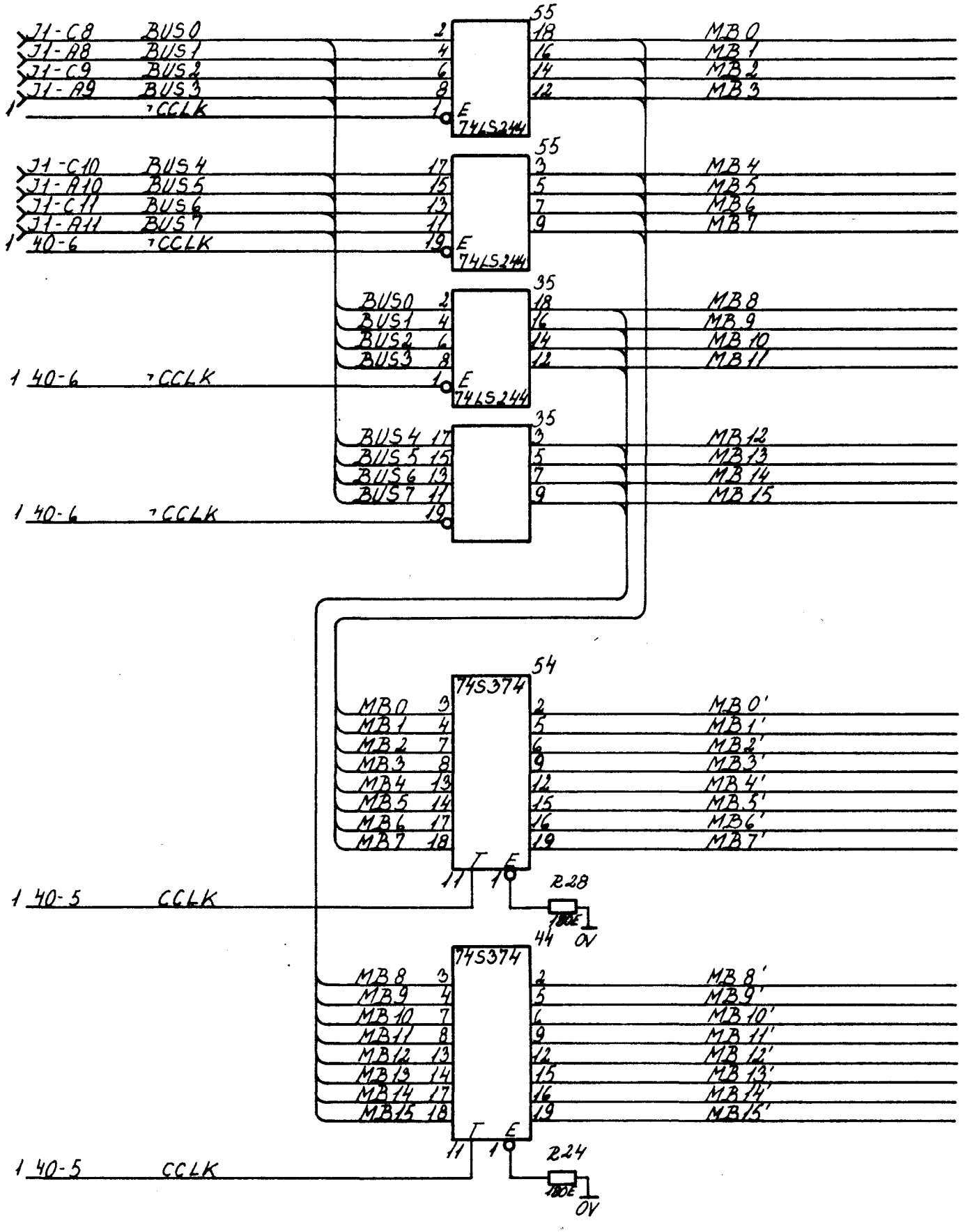
Signal	Destination	Description
L0-4*	p5, p6, p7	Used to address the video line number of the character generators.
CG0-7	p5, p6	Addresses a character in the character font (ROM or RAM).
CG 8	p14	Selects character ROM or RAM.
CG 9-10	p7	Selects shadow character.
CG 11-15	p3	Select attributes; CG15 also selects blink frequency.



CRT 504
R 13347

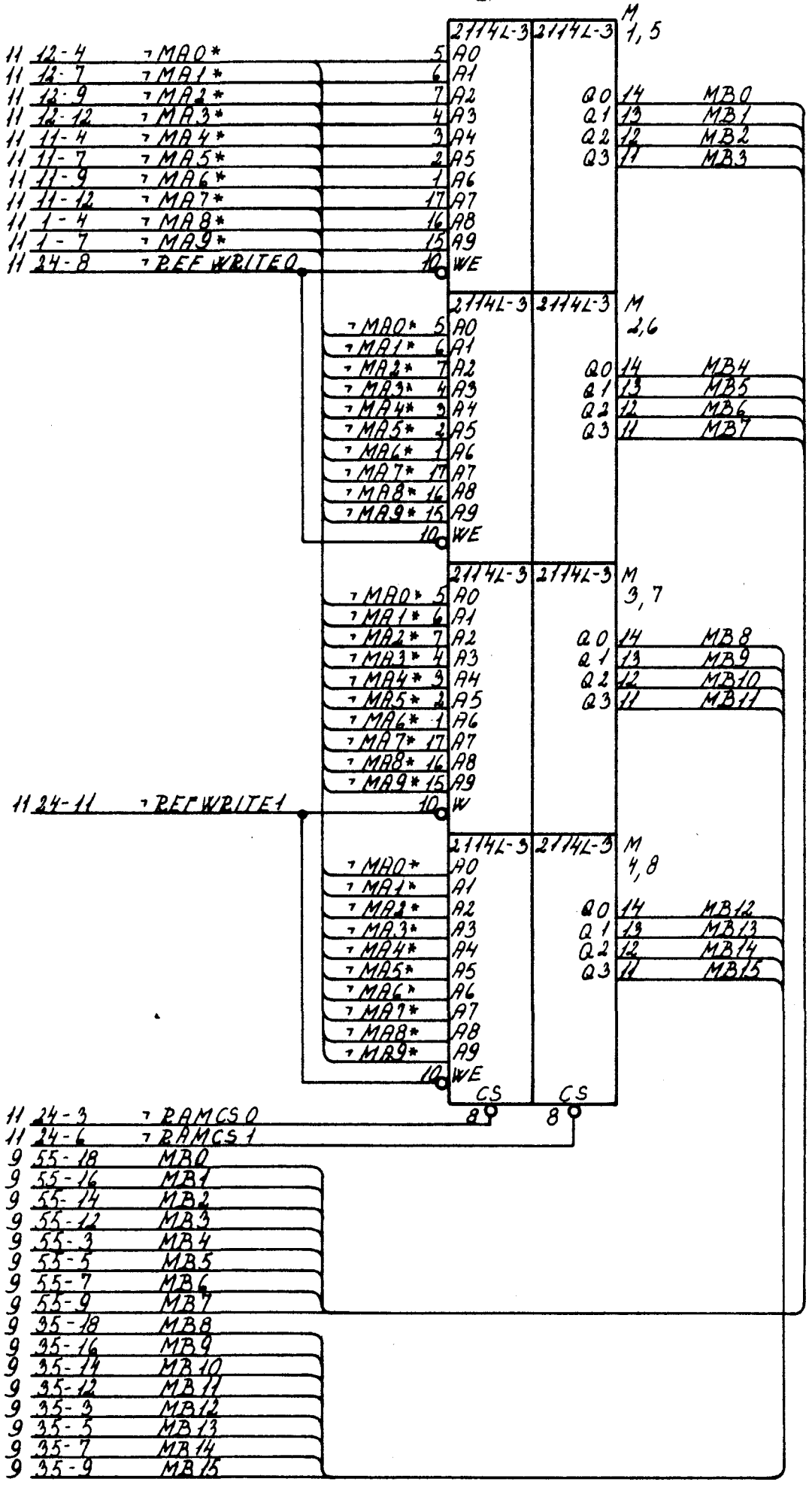
ADDRESS SWITCH for CHARACTER FONTS

Signal	Destination	Description
MB 0-15	p9, p10	Databus for refresh memory.
MB 0-15'	p8	Are gated to CG 0-15 during display time.

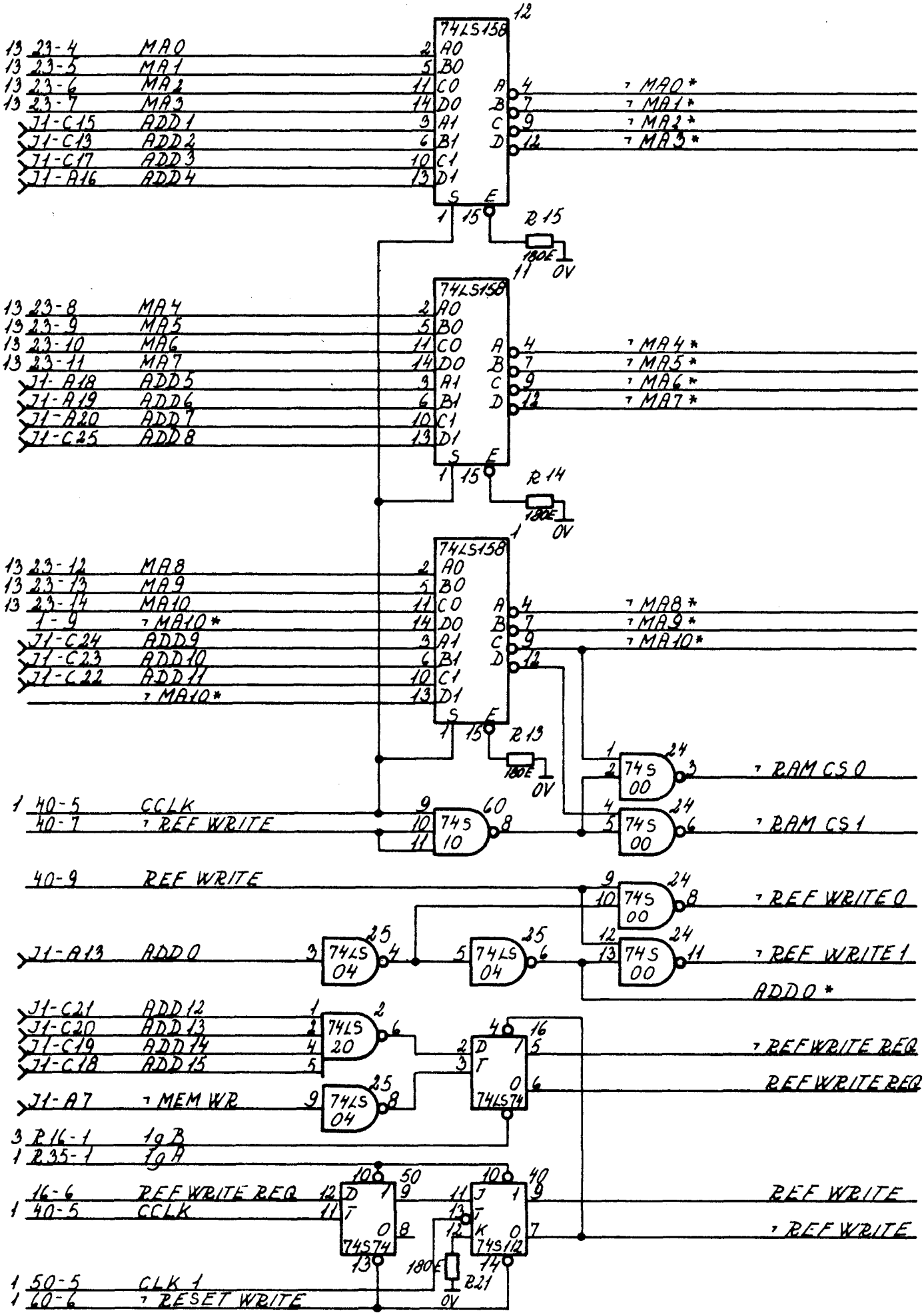


811221 PKA 82 2 1 AGA

Signal	Destination	Description
MB 0-15	p9	Databus for Refresh memory.


2114L-3
M 1,5
11 12-4 ¬MA0* 5 A0
11 12-7 ¬MA1* 6 A1
11 12-9 ¬MA2* 7 A2
11 12-12 ¬MA3* 4 A3
11 11-4 ¬MA4* 3 A4
11 11-7 ¬MA5* 2 A5
11 11-9 ¬MA6* 1 A6
11 11-12 ¬MA7* 17 A7
11 1-4 ¬MA8* 16 A8
11 1-7 ¬MA9* 15 A9
11 24-8 ¬REFWRITE0 10 WE
Q0 14 MB0
Q1 13 MB1
Q2 12 MB2
Q3 11 MB3
M 2,6
MB4
MB5
MB6
MB7
M 3,7
MB8
MB9
MB10
MB11
11 24-11 ¬REFWRITE1
M 4,8
MB12
MB13
MB14
MB15
CS
11 24-3 ¬RAMCS0
11 24-6 ¬RAMCS1
9 55-18 MB0
9 55-16 MB1
9 55-14 MB2
9 55-12 MB3
9 55-3 MB4
9 55-5 MB5
9 55-7 MB6
9 55-9 MB7
9 35-18 MB8
9 35-16 MB9
9 35-14 MB10
9 35-12 MB11
9 35-3 MB12
9 35-5 MB13
9 35-7 MB14
9 35-9 MB15
PKA 81.12.21 AGA 82.2.1.

Signal	Destination	Description
-,MA 0-10*	p10	Address lines to the refresh memory. during first character phase, -,MA 0-10* are derived from the MIC board-addressbus for writing in the refresh RAM, in the second character phase -,MA 0-10* are generated by the MC 6845 address sequencer for refresh of the character on the screen.
-,RAMCS 0-1	p10	Enable signals for refresh mem. controlled by -,MA 10*
-,REF WRITE 0-1	p10	Writepulse to frefresh memory, ADD 0 selects which byte.
ADD0*	p13	Buffered version of DD 0.
-,REFWRITE REQ	p13	The flip-flop is set when a memory write to the highest 4 k is issued by the CPU on the MIC board.
REFWRITE REQ	p11	
REF WRITE	p11	This pulse is generated if REF WRITE REQ is active, and falls entirely within the first character phase and has a guaranted minimum duration of 133 nanoseconds.
-,REF WRITE	p11	



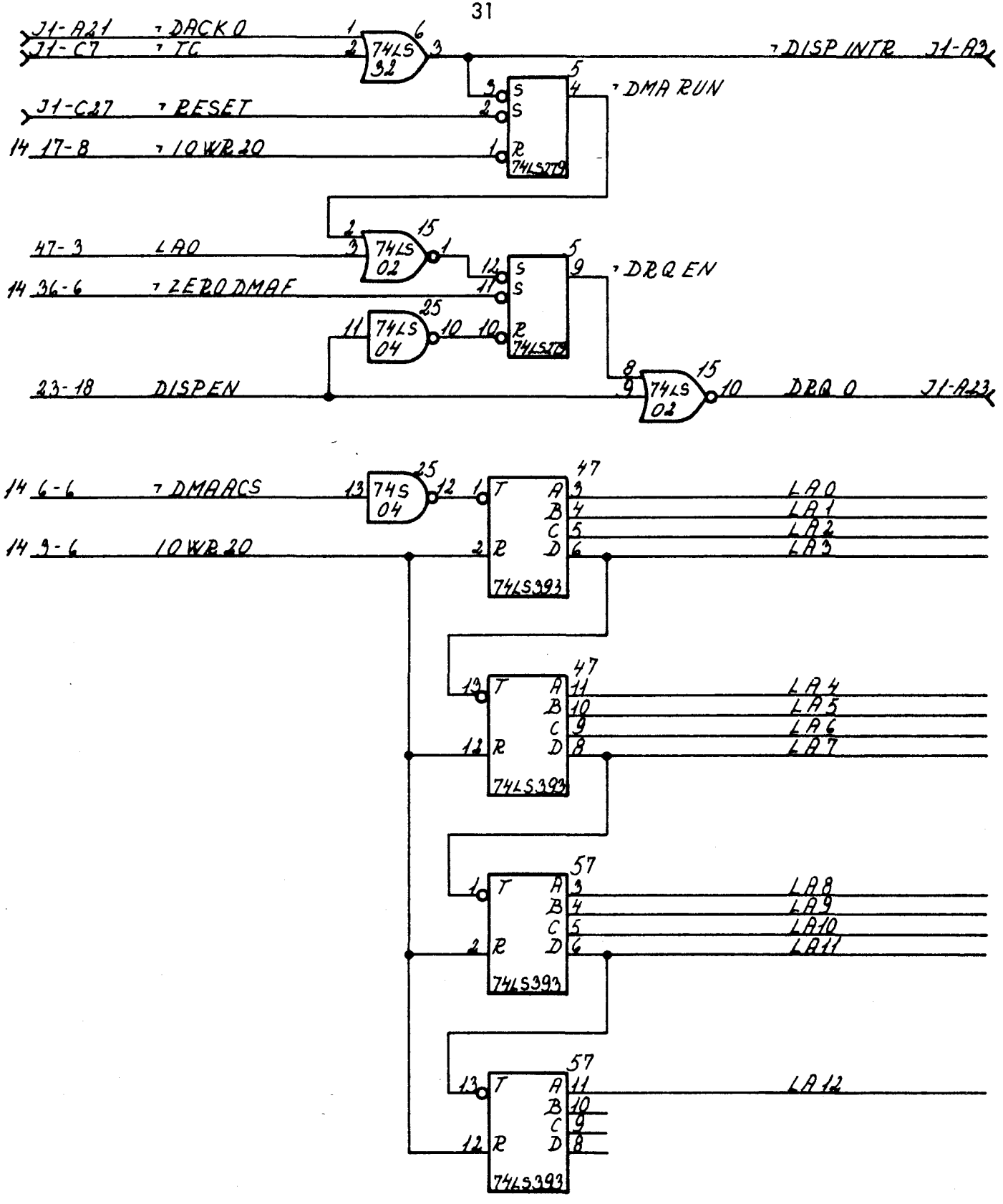
PKA 81 12 21 AGA 82.2.2

CRT 504
R 13350

ADDRESS SWITCH for REFRESH MEMORY

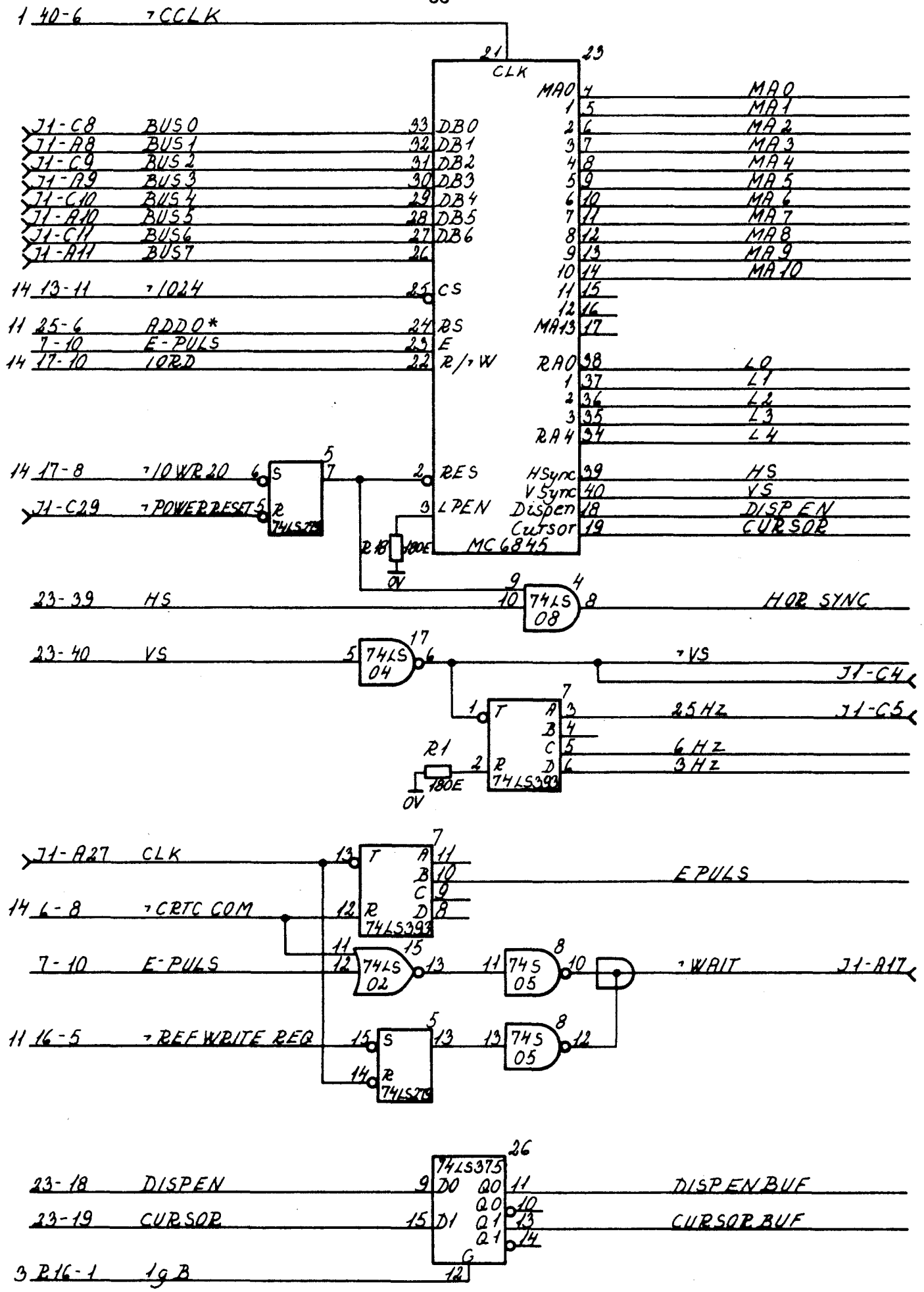
11

Signal	Destination	Description
-,DISP INTR	MIC board	Active, when Dack 0 and -,Terminal count are active.
-,DMA RUN		Active from -,IOWR20 to -,DISPINTR or -,RESET.
-,DRQ EN		Goes active when -,DMA RUN is low, if LA0 is low, -,ZERO DMAF is high and DISP EN is high. -,DRQ EN is reset by LA0 going high.
DRQ 0	MIC board	is set when DISPEN goes low, -,DRQ EN is active. Drops when one byte is transferred late enough to ensure that another DMA cycle is started.
LA 0-12	p8	Load Address counter for memories accessed by the MIC board via DMA.

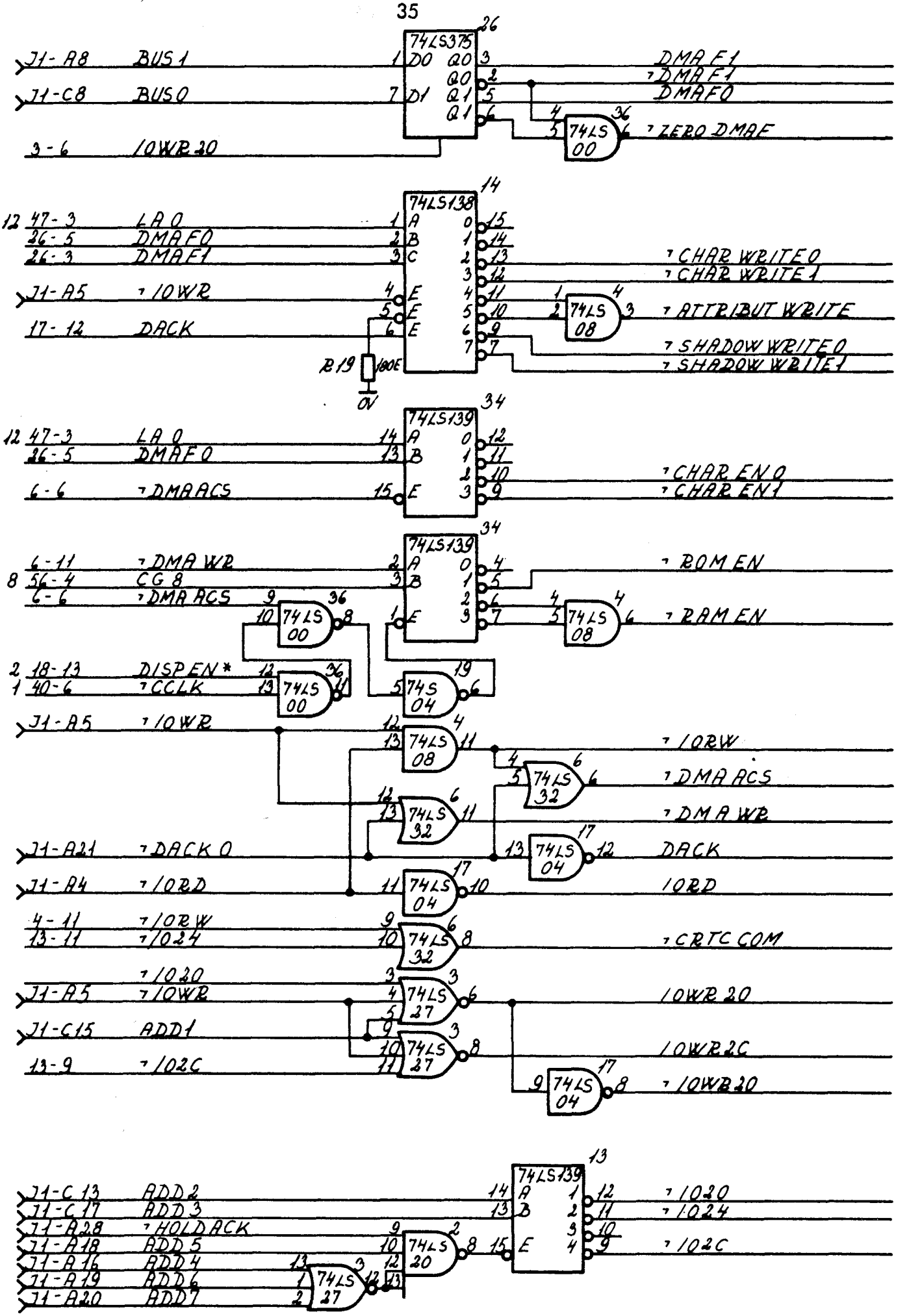


81.12.21 PKA 82.2.2. AGA

Signal	Destination	Description
MA 0-10	p11	Output of address sequence controller used for addressing the refresh memory for display.
L 0-3	p8	Video line number within the character line.
L4	p3	
HS	p13	Horizontal syncronization pulse.
VS	p13	Vertical syncronization pulse.
HOR SYNC	p1	Horsizontal sync gated with power up flip-flop.
-,VS	p1	
25 Hz	Mic board	Used for timer interrupt.
6 Hz	p3	Used for blink frequencies.
3 Hz	p3	
E Puls	p13	Enable pulse for programming of MC6845.
-,Wait	Micboard	Waitstates are inserted during memwrite in the refresh and programming of MC6845.
DISP EN BUF	p3	Display enable goes inactive during e-beam retrace.
CURSOR BUF	p3	

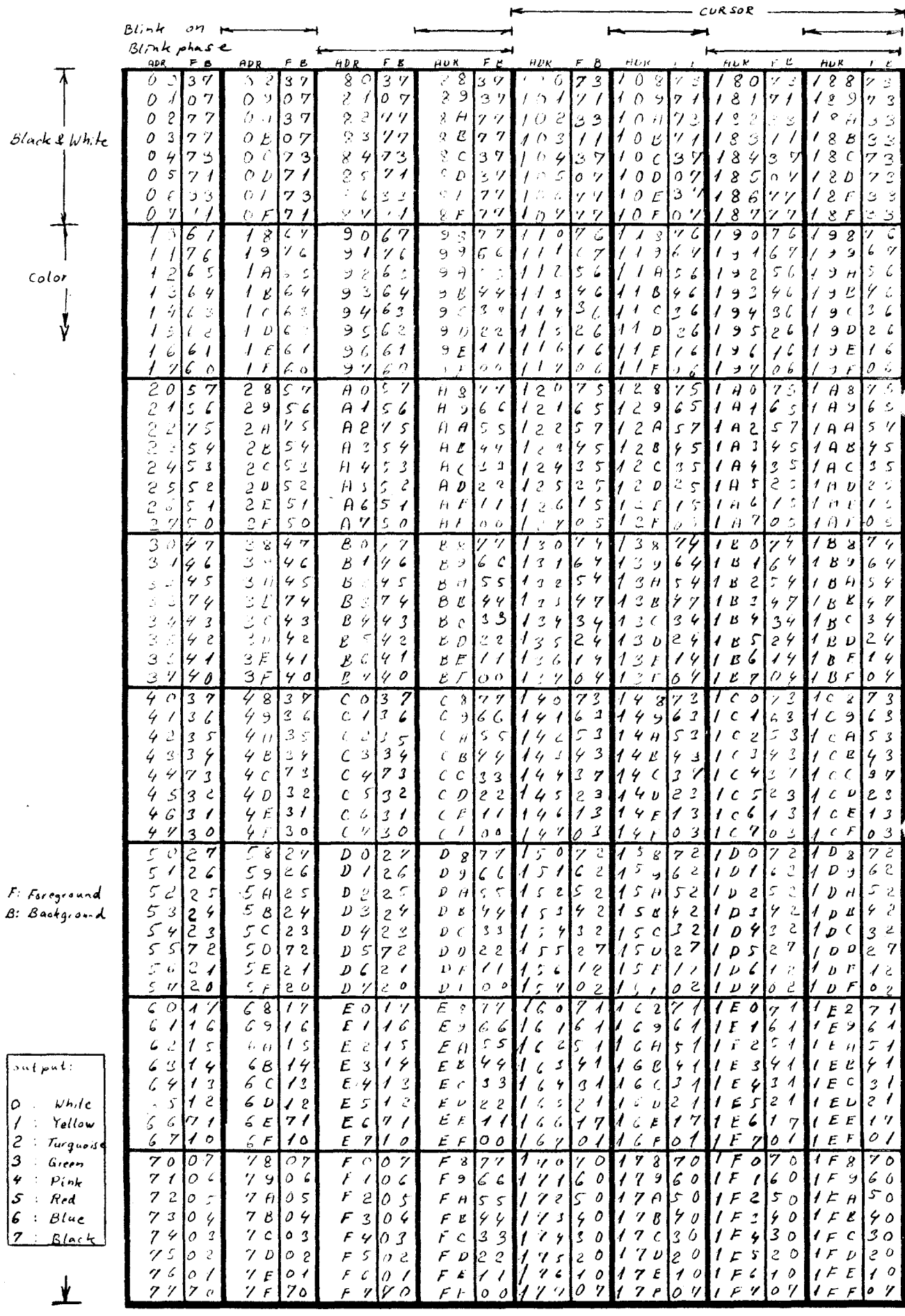

1 40-6 ~CCLK
CLK
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
J1-C8 BUS0
J1-A8 BUS1
J1-C9 BUS2
J1-A9 BUS3
J1-C10 BUS4
J1-A10 BUS5
J1-C11 BUS6
J1-A11 BUS7
DB0
DB1
DB2
DB3
DB4
DB5
DB6
14 13-11 ~1024
CS
11 25-6 ADDO*
RS
7-10 E-PULS
E
14 17-10 IORD
R/~W
RA0
RA1
RA2
RA3
RA4
L0
L1
L2
L3
L4
14 17-8 ~IOWR20
J1-C29 ~POWERRESET
RES
LPEN
HSync
VSync
Dispen
Cursor
HS
VS
DISPEN
CURSOR
MC6845
180E
0V
23-39 HS
74LS 08
HOR SYNC
23-40 VS
74LS 04
~VS
J1-C4
25Hz
J1-C5
6Hz
3Hz
74LS393
J1-A27 CLK
14 6-8 ~CRTC COM
EPULS
7-10 E-PULS
74LS 02
74S 05
~WAIT
J1-A17
11 16-5 ~REFWRITE REQ
74LS279
74LS375
23-18 DISPEN
23-19 CURSOR
DISPENBUF
CURSORBUF
3 R16-1 1gB
PKA 82.2.2. AGA
81 12 21

Signal	Destination	Description
DMA F1	p14	DMA function register.
-,DMA F1	p14	
DMA F0	p14	
-,ZERO DMAF	p12	Active when DMAF(0,1) = 0.
-,CHAR WRITE 0-1	p6	Write signal to character RAM.
-,ATTRIBUT WRITE	p3	Write signal to Attribut RAM.
-,SHADOWWRITE 0-1	p7	Write signal to shadow RAM.
-,CHAR EN 0-1	p5	Enables connection between DOT bus and MIC board data bus.
-,ROM EN	p5	Enables character ROM output.
-,RAM EN	p6	Enables Character RAM.
-,IORW	p14	-,(10 Read or 10 write).
-,DMA ACS	p12	IORW issued by DMA controller.
-,DMA WR	p14	Output by DMA.
DACK	p14	
IORD	p13	
-,CRTC COM	p13	10 port e4 addressed.
IOWR 20	p13, p14	10 port 20 addressed for write.
IOWR 2C	p3	
-,IOWR 20	p12	


J1-A8 BUS1
J1-C8 BUS0
3-6 /IOWR20
74LS375
DMAF1
¬DMAF1
DMAF0
74LS 00
¬ZERO DMAF
12 47-3 LA0
26-5 DMAF0
26-3 DMAF1
J1-A5 ¬IOWR
17-12 DACK
R19 100E
0V
74LS138
¬CHAR WRITE0
¬CHAR WRITE1
74LS 08
¬ATTRIBUT WRITE
¬SHADOW WRITE0
¬SHADOW WRITE1
12 47-3 LA0
26-5 DMAF0
6-6 ¬DMAACS
74LS139
¬CHAR EN0
¬CHAR EN1
6-11 ¬DMA WR
8 56-4 CG8
6-6 ¬DMA ACS
¬ROM EN
¬RAM EN
2 18-13 DISPEN*
1 40-6 ¬CCLK
74LS 04
J1-A5 ¬IOWR
74LS 32
¬IORW
¬DMA ACS
¬DMA WR
J1-A21 ¬DACK0
DACK
J1-A4 ¬IORD
IORD
4-11 ¬IORW
13-11 ¬IO24
¬CRTC COM
¬IO20
J1-A5 ¬IOWR
74LS 27
IOWR20
J1-C15 ADD1
13-9 ¬IO2C
IOWR2C
¬IOWR20
J1-C13 ADD2
J1-C17 ADD3
J1-A28 ¬HOLDACK
J1-A18 ADD5
J1-A16 ADD4
J1-A19 ADD6
J1-A20 ADD7
74LS 20
¬IO20
¬IO24
¬IO2C
PKA AGA
81/12/21 82.2.3.

5. ATTRIBUTE ROM

5.



Contents of ROB 046 type 74S472

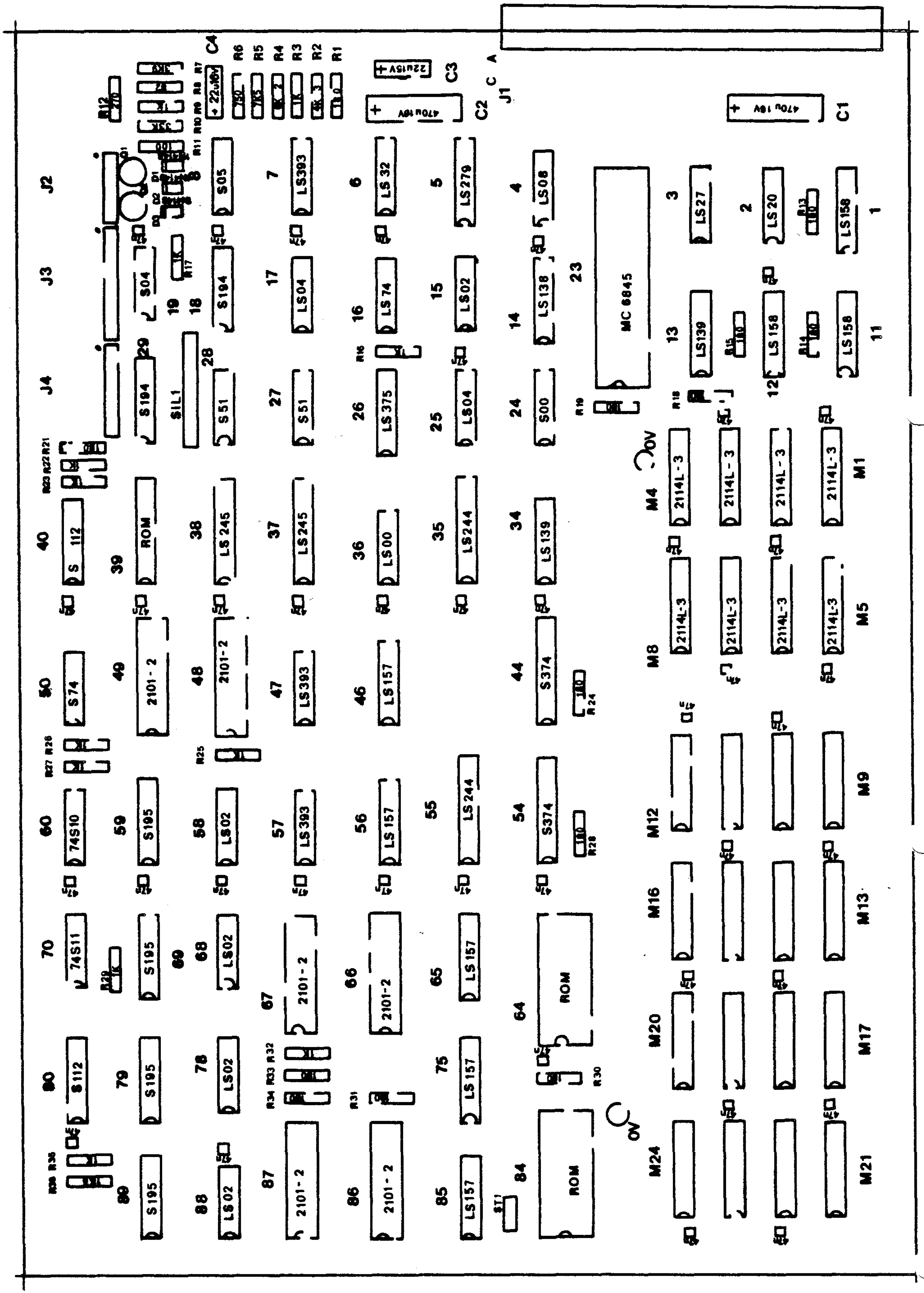
6. CHARACTER ROM's 6.

As character ROM's are used

U64 : ROA416

U84 : ROA417

7. ASSEMBLY DRAWING



8. PLUGS

J1. pin	A	C
1		
2		
3	-,DISP INTR	-,VFO CLK
4	-,IORD	-,VS
5	-,IOWR	25Hz
6		
7	-,MEMWR	-,TC
8	BUS1	BUS0
9	BUS3	BUS2
10	BUS5	BUS4
11	BUS7	BUS6
12		
13	ADD0	ADD2
14	Chain	Chain
15		ADD1
16	ADD4	
17	-,WAIT	ADD3
18	ADD5	ADD15
19	ADD6	ADD14
20	ADD7	ADD13
21	-,DACK 0	ADD12
22		ADD11
23	DRQ 0	ADD10
24		ADD9
25		ADD8
26		
27	CLK	-,RESET
28	-,HOLD ACK	
29		-,POWER RESET
30		
31		
32	+12V	+12V

J2. pin

1	Contrast pot. max
2	Contrast pot. top
3	Contrast pot. min
4	Intensity pot. max
5	Intensity pot. tap
6	Intensity pot. min

J3. BW Monitor connected to CBL

pin

1	GND
2	Intensity max
3	Intensity min
4	Intensity top
5	Not used
6	Horizontal sync
7	Not used
8	Video
9	Vertical sync
10	GND

J4. Colour monitor

pin

1	
2	RED
3	GREEN
4	BLUE
5	GND
6	GND
7	-,Horizontal sync
8	-,Vertical sync

RETURN LETTER

Title: CRT504 - CRT Controller Technical Manual

RCSL No.: 44-RT2032

A/S Regnecentralen af 1979/RC Computer A/S maintains a continual effort to improve the quality and usefulness of its publications. To do this effectively we need user feedback, your critical evaluation of this manual.

Please comment on this manual's completeness, accuracy, organization, usability, and readability:

_____

_____

_____

_____

Do you find errors in this manual? If so, specify by page.

_____

_____

_____

_____

How can this manual be improved?

_____

_____

_____

_____

Other comments?

_____

_____

_____

_____

_____

Name: _____ Title: _____

Company: _____

Address: _____

Date: _____

Thank you

42-i 1288

..... Fold here .....

..... Do not tear - Fold here and staple .....

Affix
postage
here

REGNECENTRALEN
af 1979

Information Department
Lautrupbjerg 1
DK-2750 Ballerup
Denmark