RCSL No: 52-AA1054

Edition: June, 1981

Author: K. Øllgård

Title:

RC850 Display Terminal

Technical Manual

RCSL 42-i1592

A/S REGNECENTRALEN
af 1979

Keywords:

RC850.

Abstract:

This manual contains the technical description of the RC850.

(120 printed pages)

Printed by A/S Regnecentralen af 1979, Copenhagen

RCSL 42-i1592

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1. INTRODUCTION 1.

1.1 The RC850 Family 1.1

The RC850 Display Terminals are all members of a powerful, intelligent terminal-family.

The RC850 family of Display Terminals are microprocessor-based terminals which are able to emulate several terminals of the market. There will be different versions reaching from the "hard-programmed" version to the "soft-programmed down line loaded" version or even the microcomputer -high-level- language version.

Common to all versions is the real professional design of the cabinet and keyboard. No efforts have been avoided to obtain the most comfortable and reliable place of work. Special human engineering has taken place in the areas: Operator accomodation, operating-environment, and service-ability.

In this manual the general hardware of the RC850 Display Terminals is described.

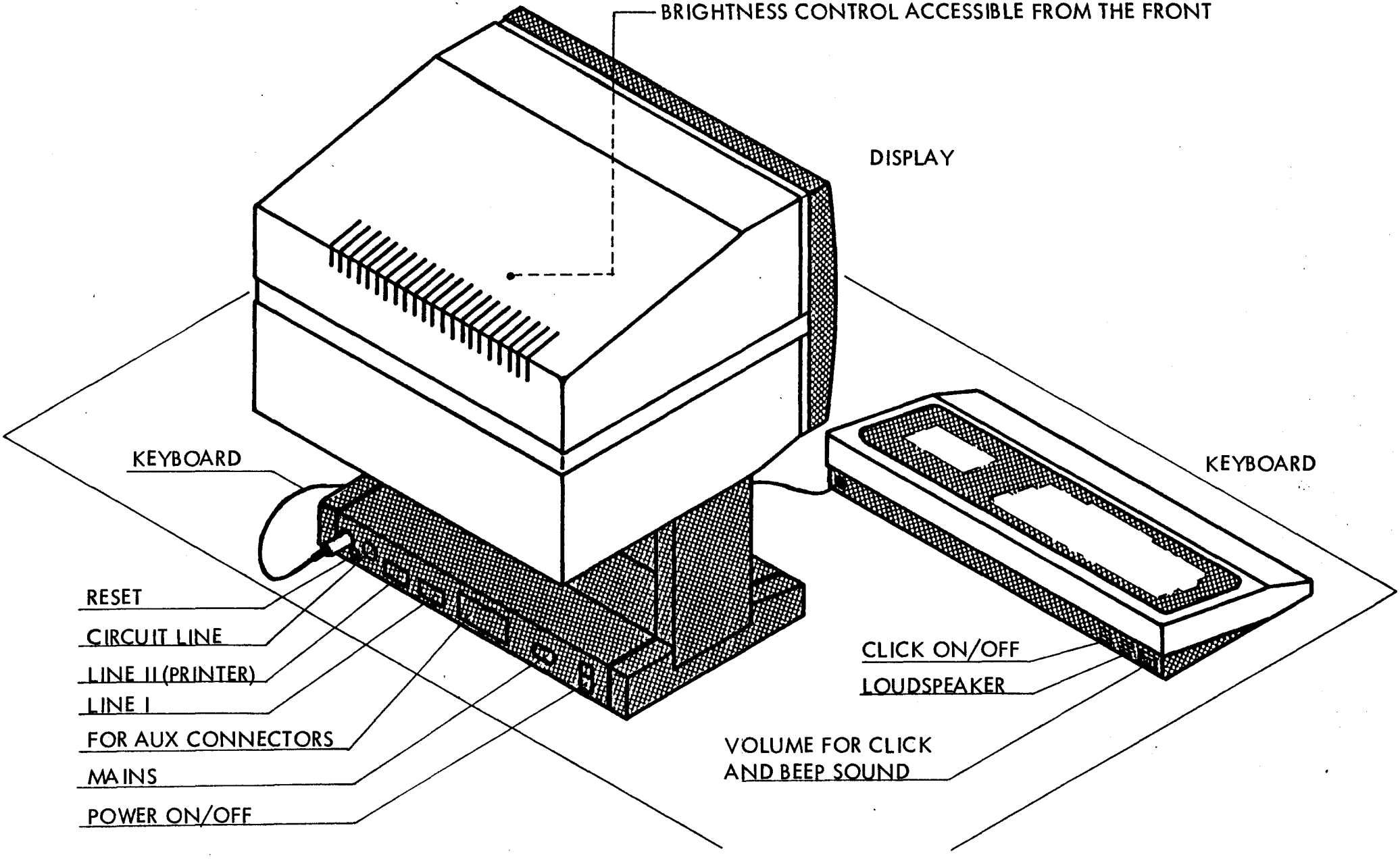


Fig. 1.1

RC8(`ackpanel connector and switch location(

2. TERMINAL MODULES 2.

The RC850 is a microcomputer based terminal, where all terminal functions are programmed.

2.1 Module Survey 2.1

In fig. 2.2 the functional diagram of RC850 is shown, and fig. 2.1 shows the actual module layout of the terminal.

2.2 Functional Description 2.2

The functional description follows the block diagram. This paper does not contain a full description of all the functions of the VLSI circuits used in RC850. This kind of informations may be supplied by the manufacturers of the VLSI circuits.

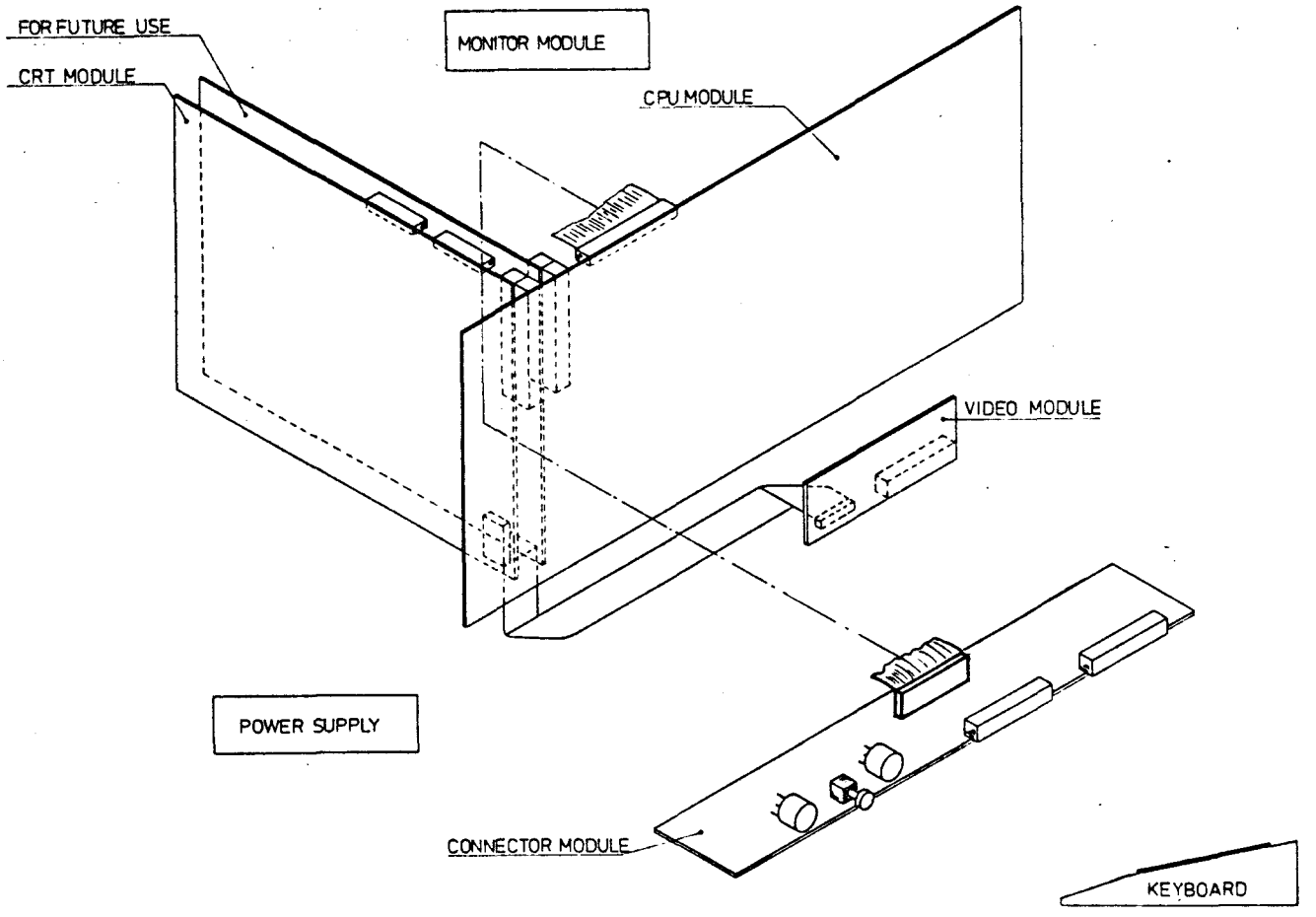


Fig. 2.1
RC 850 Module Survey

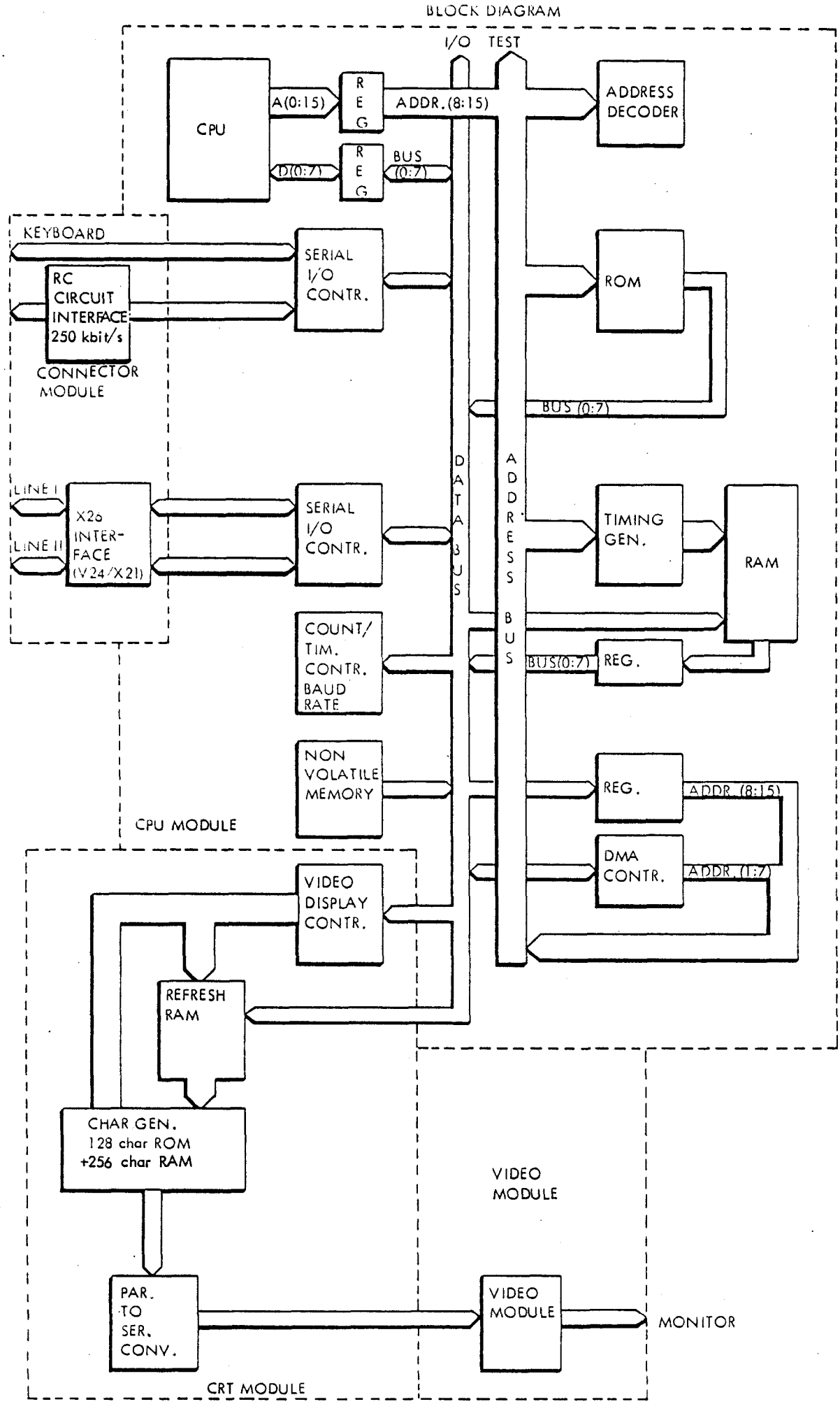

BLOCK DIAGRAM
I/O
TEST
CPU
A(0:15)
REG
ADDR.(8:15)
ADDRESS DECODER
D(0:7)
REG
BUS (0:7)
KEYBOARD
SERIAL I/O CONTR.
RC CIRCUIT INTERFACE 250 kbit/s
CONNECTOR MODULE
ROM
BUS (0:7)
DATA BUS
ADDRESS BUS
LINE I
LINE II
X26 INTER-FACE (V24/X21)
SERIAL I/O CONTR.
TIMING GEN.
RAM
COUNT/ TIM. CONTR. BAUD RATE
BUS(0:7)
REG.
NON VOLATILE MEMORY
REG.
ADDR (8:15)
CPU MODULE
DMA CONTR.
ADDR (1:7)
VIDEO DISPLAY CONTR.
REFRESH RAM
CHAR GEN.
128 char ROM
+256 char RAM
VIDEO MODULE
PAR. TO SER. CONV.
VIDEO MODULE
MONITOR
CRT MODULE

Fig. 2.2

3. FUNCTIONAL DESCRIPTION 3.

3.1 CPU-Module 3.1

The CPU-module contains the microprocessor, oscillator, program source ROM's, RAM, and NVM for terminal setups, and the serial input-output communications.

3.2 CPU Description 3.2

A block diagram of the architecture of the Z-80A CPU is shown in fig. 3.1. The diagram shows all the major elements in the CPU and it should be referred to throughout the following description.

Z-80A CPU contains 208 bits of R/W memory that are accessible to the programmers. Fig. 3.2 illustrates how this memory is configurated into eighteen 8-bit registers and four 16-bit registers.

All Z-80A registers are implemented using static RAM. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or in pairs as 16-bit registers. There are also two sets of accumulators and flag registers.

CPU timing can be broken down into a few very simple timing diagrams. The diagrams show basic operations with one wait state (the wait state is added to synchronize the CPU to the RAM memory). Figs. 3.3 to 3.5 show the CPU timing.

The Z-80A CPU can execute 158 different instruction types including all 78 of the 8080A CPU. A description of this may be obtained from Zilog Z-80A CPU Technical Manual.

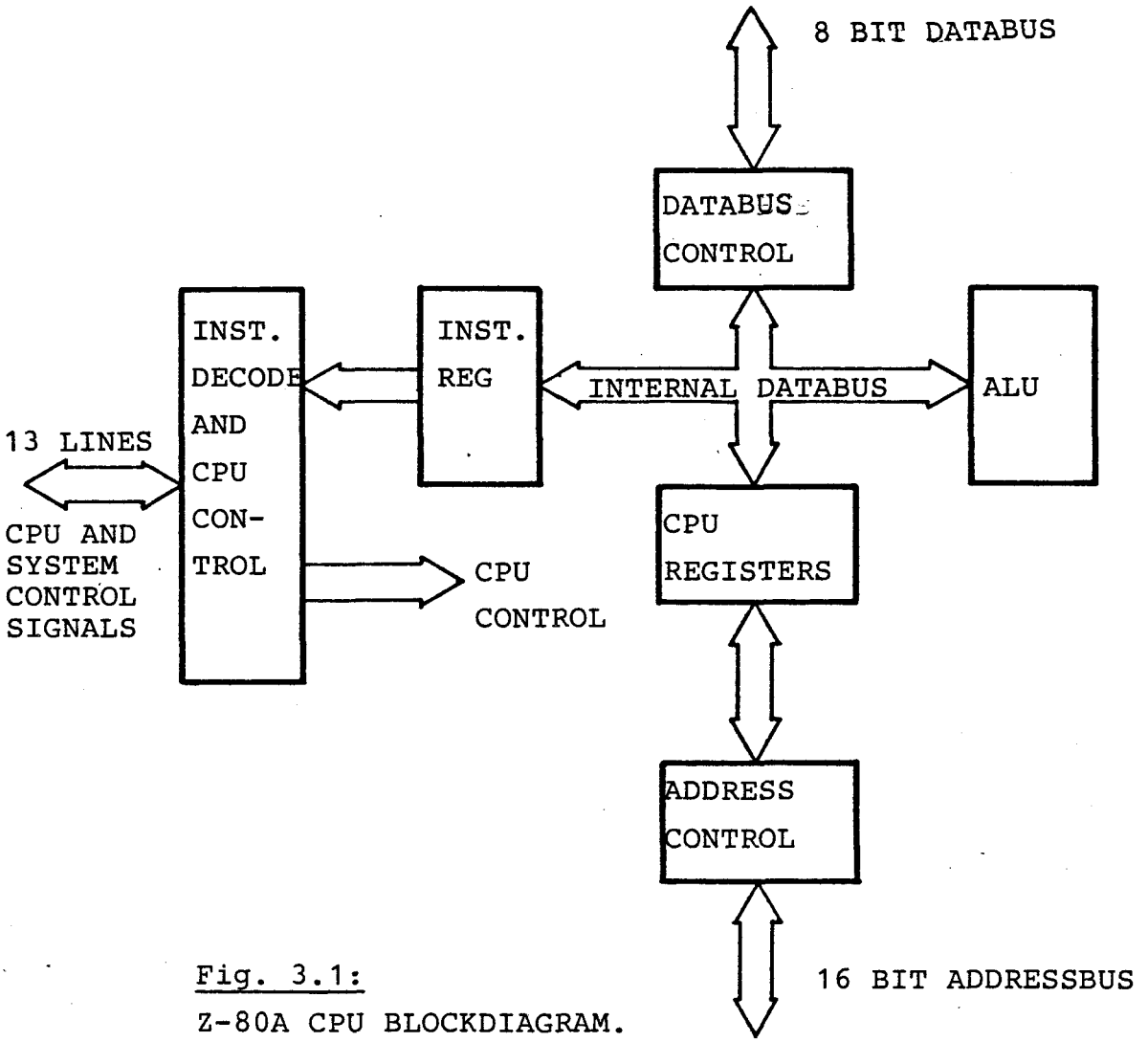


Fig. 3.1:
Z-80A CPU BLOCKDIAGRAM.

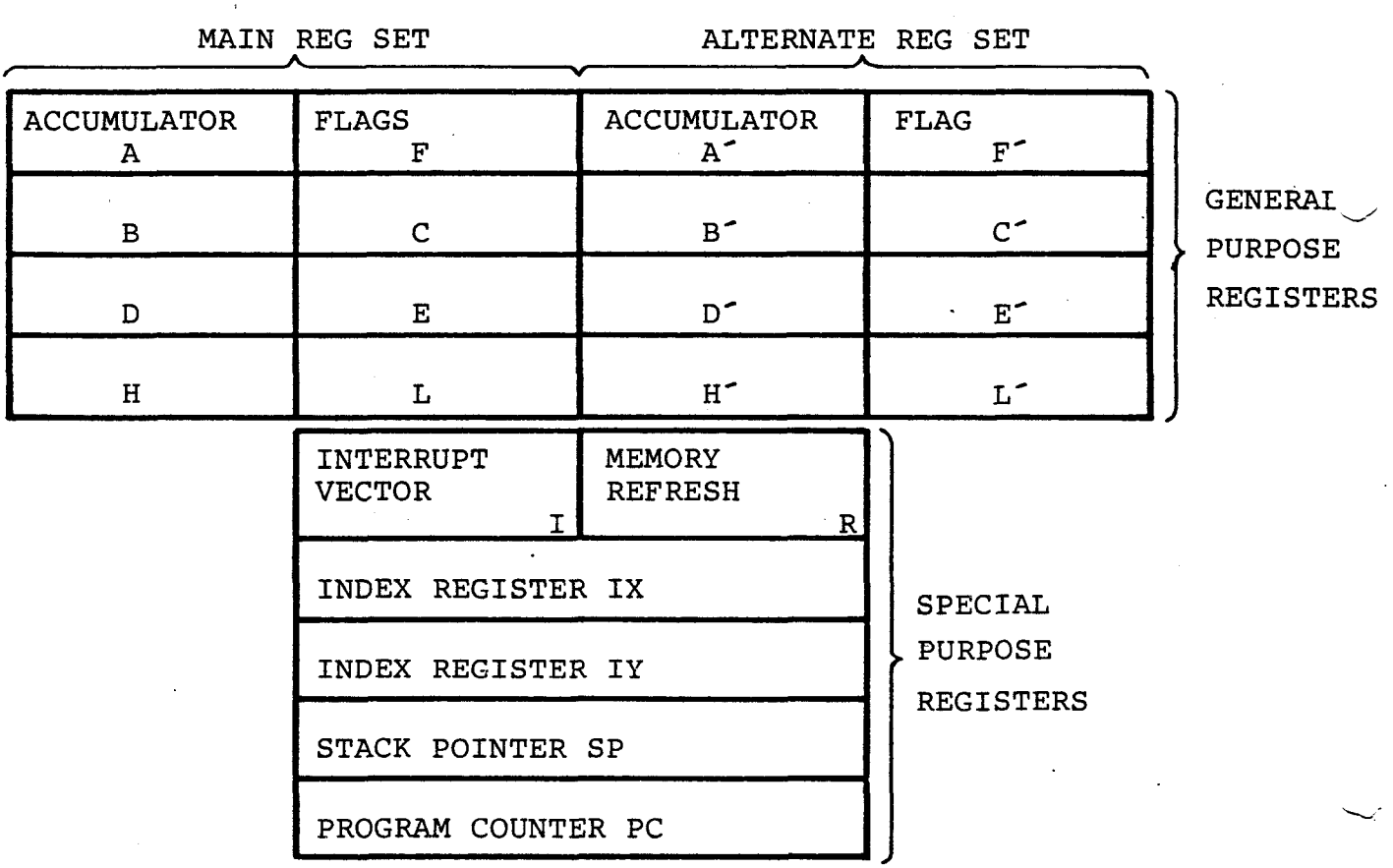


Fig. 3.2

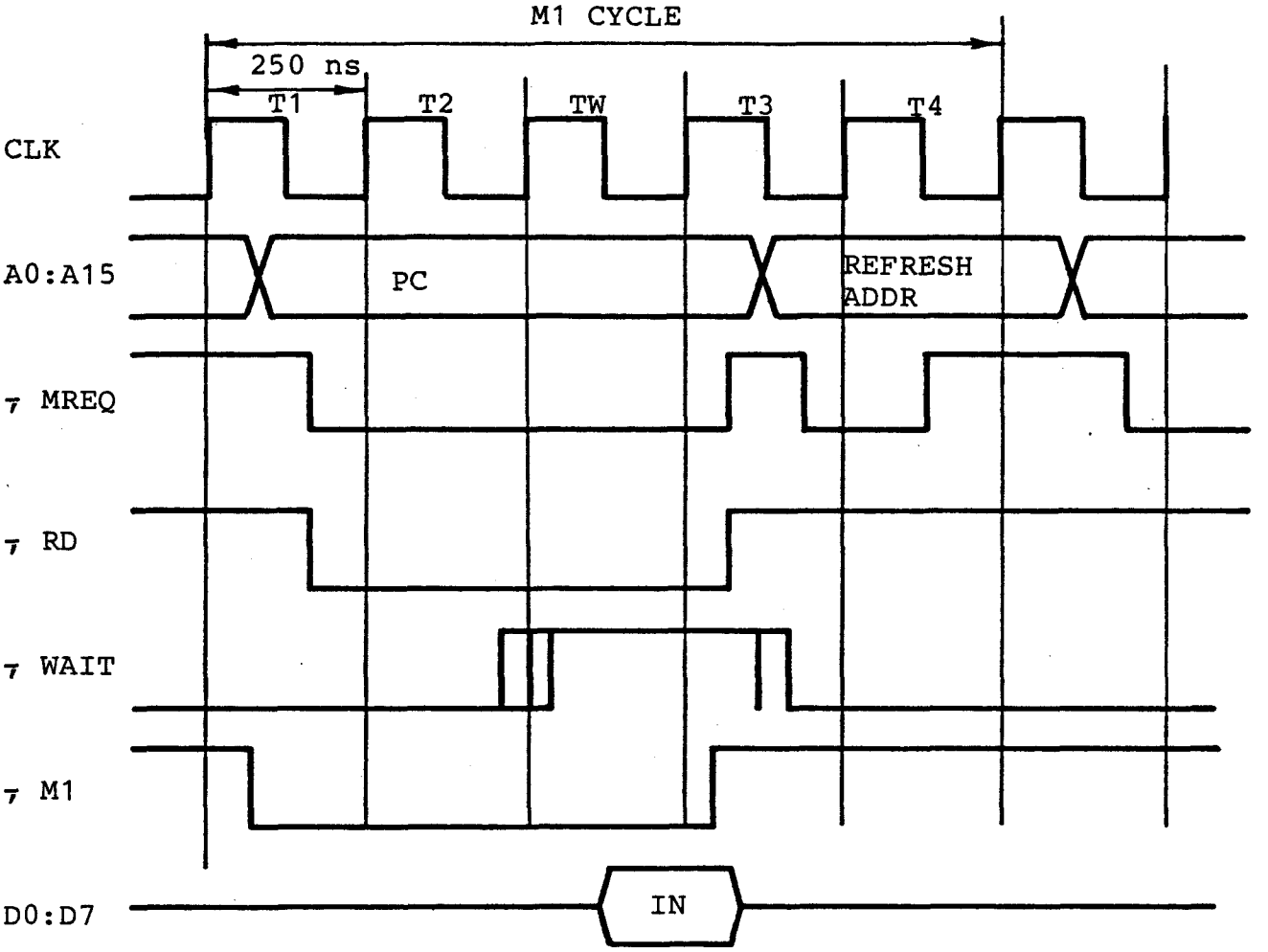


Fig. 3.3
INSTRUCTION OP CODE FETCH

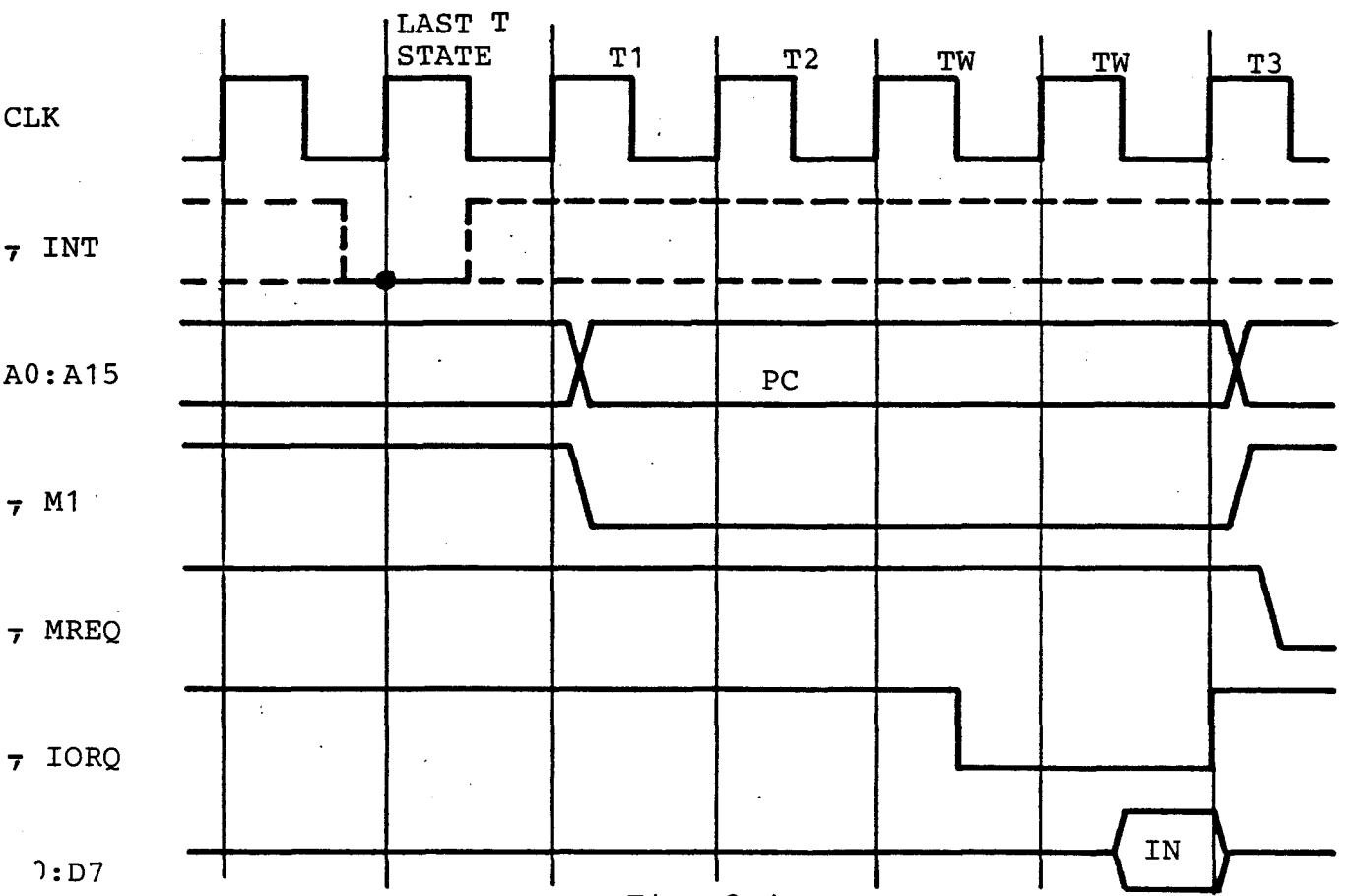


Fig. 3.4
INTERRUPT REQUEST/ACKNOWLEDGE

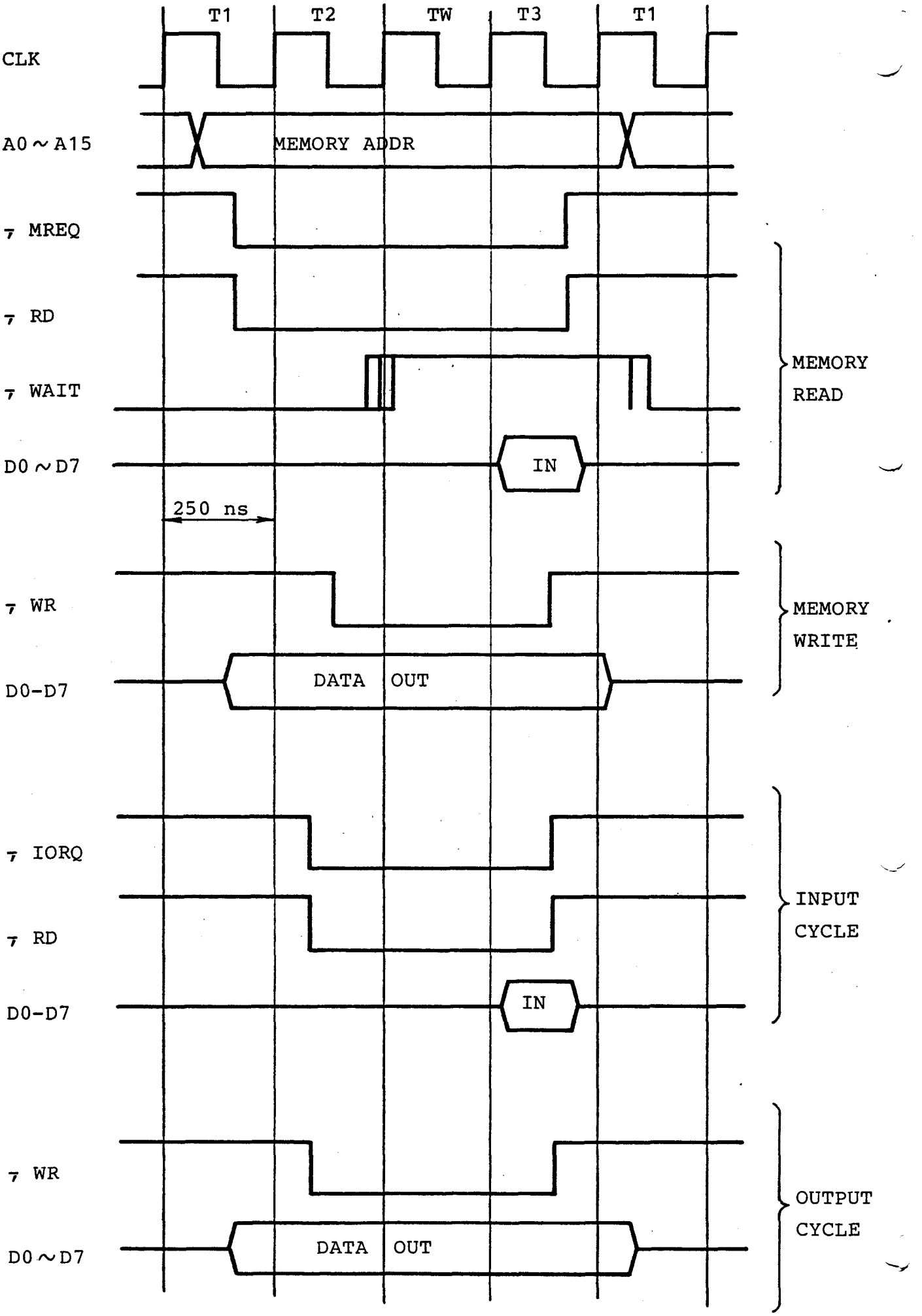


Fig.3.5

TIMING WAVEFORM FOR Z-80A DIAGRAM

3.3 Address Decoder

The addressing of devices is made very simple with the circuit shown in diagram page 5 of 15, MIC50x, and page 17 of 18, CRT50x. Each device uses 4 addresses except the DMA controller which uses 16 addresses. This is shown in fig. 3.6.

Addressing of dynamic RAM and ROM in the whole 64K address area is made possible using the PROM in Pos. U87 MIC50x.

RAM - Random Access Memory, up to 64K of 8 bits dynamic RAM, used as buffer and program memory. Contains also a copy of the refresh memory.

ROM - Read Only Memory that contains the program to the microprocessor.

Most significant bit in the PROM is controlled by the flip-flop in Pos. 82. The flip-flop is reset by the RESET signal and set or reset by the program using the following instructions:

$$\text{OUT } (19_H),A \Rightarrow \text{ROM} \frown \text{RAM}$$

$$\text{OUT } (18_H),A \Rightarrow \text{RAM} \frown \text{ROM}$$

When the ROM is connected to an address area, the RAM is disconnected from the same area.

Address No.	Name	IC type	Comments
00 01 02 03			
04 05 06 07			
08 09 0A 0B	SIO - - -	Z80A-SIO2	DATA CHANNEL A DATA CHANNEL B CONTROL CHANNEL A CONTROL CHANNEL B

Address No.	Name	IC type	Comments
0C 0D 0E 0F	CTC - - -	Z80A-CTC	CLOCK TO LINE 1 CLOCK TO LINE 2 (PRINTER) INT. from CRT module INT. from FUTURE module
10 11 12 13			
14 15 16 17	SWITCH - - -	74LS240	INPUT (OC_H) if selected
18 19 1A 1B	ENABLE ROM DISABLE ROM ENABLE ROM DISABLE ROM		
1C 1D 1E 1F	READ STATUS - - - -	74LS240	READ LINE 1 & 2 STATUS Data Set READY and Calling Indicator
20 21 22 23	DISP.CONT.Port - - - - - -		Used to select the CRT-DMA channel 0 transport direction
24 25 26 27	CRT.C - - - - - -	MC6845	Address register (pointer) Data register Address register (pointer) Data register
28 29 2A 2B	NVM	NC7033	NON Volatile Memory
2C 2D 2E 2F	DBP		DISP. BLOCK PORT
30 31 32 33	SIO	Z80A-SIO2	DATA CHANNEL A DATA CHANNEL B CONTROL CAHNNEL A CONTROL CHANNEL B
34 35 36			
EE EF			
F0 FF	DMA	AM9517A-4 or I8237-2	Use of the Registers is described in the manufacturer's manual

Fig. 3.6

3.4 Serial Input/Output Controller 3.4

The Z-80-SIO/2 (Serial Input/Output) is a dual channel multi-function peripheral component designed to satisfy a wide variety of serial data communications requirements in microcomputer systems. Its basic function is a serial-to-parallel, parallel-to-serial converter/controller, but - within that role - it is configurable by system software so its "personality" can be optimized for a given serial data communications application.

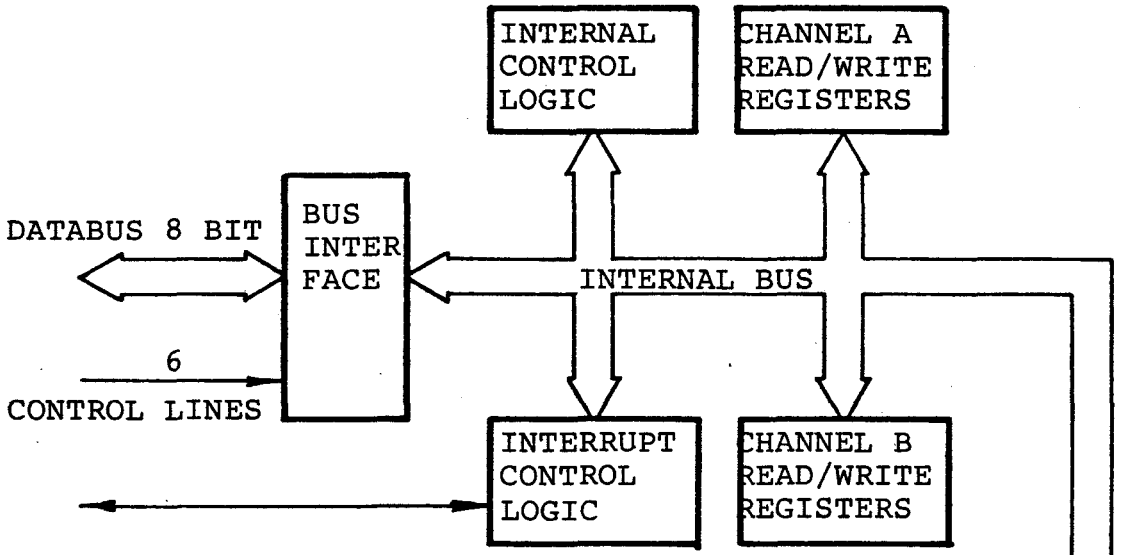
One SIO in the RC85x is handling the LINE 1 and LINE 2 (Printer), the other SIO is handling the RC circuit transmission line (250K bit/s. synchronous) and the 300 bit/s. asynchronous keyboard transmission.

The Z80-SIO/2 can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The device also has facilities for modem controls in both channels. Block diagram for the Z80-SIO/2 is shown in fig. 3.7.

The internal structure includes Z-80A CPU interface, internal control and interrupt logic, and two full duplex channels. Each channel contains read and write registers, and discrete control and status logic that provides interface to modems.

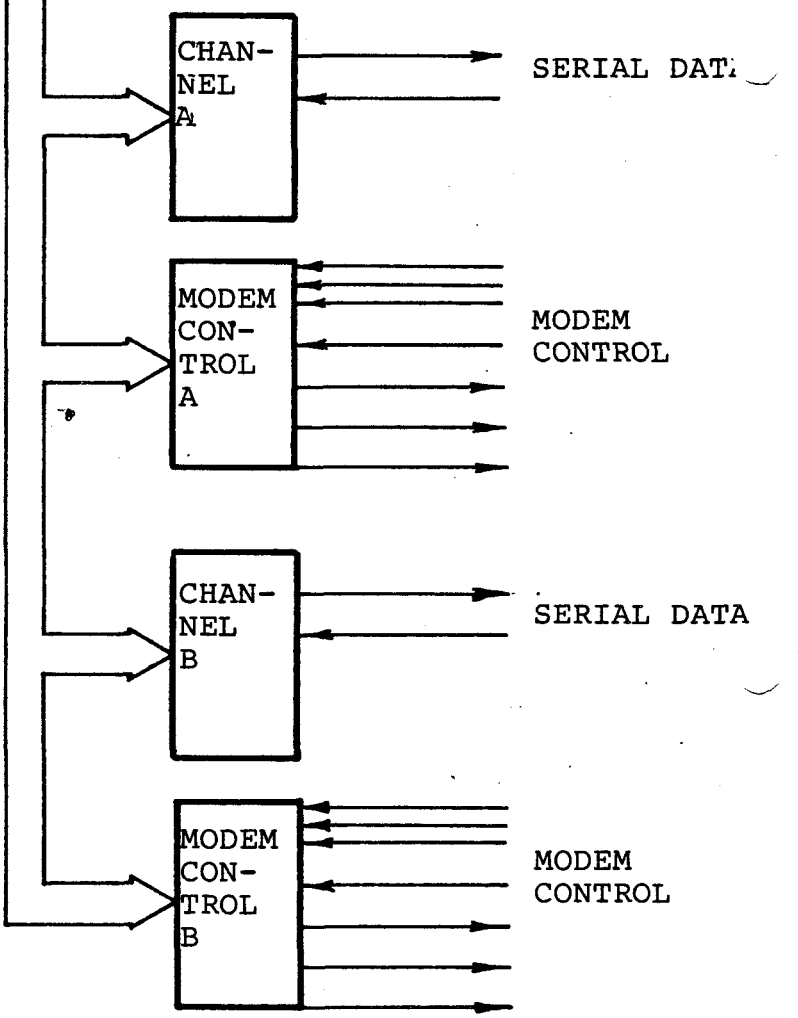
The logic for both channels provides formats, synchronization, and validation for data transferred to and from the channel interface. The modem control inputs, Clear to Send (CTS) and Data Carrier Detect (DCD) are monitored by the discrete control logic under program control. All the modem control signals are general purpose in nature, and some of the signals from the RC circuit/keyboard SIO are used in this way.

The programming for the SIO/2 is very complex and is described in manuals from Zilog.



LINE 1 AND 2 SIO PIN CONNECTION

PIN	SIGNAL	
2	TRANS. DATA	OUT
3	REC. DATA	IN
4	REQ. TO SEND	OUT
5	CLEAR TO SEND*	IN
6	DATA SET READY	IN
7	GROUND	
8	DATA CARRIER DET	IN
20	DATA TERM READY	OUT
21	CALLING INDICATOR	IN



PIN CONNECTION FOR
SERIAL I/O CONTROLLER
CONNECTOR 25 PIN CANNON.
CHANNEL A TO LINE 1
CHANNEL B TO LINE 2
*IF PRINTER CONNECTOR TO 7 BUSY

Fig. 3.7

BLOCK DIAGRAM FOR Z-80A SIO/2 AND SIGNAL CONNECTION TO J1 AND J2.

3.5 Counter Timer Controller 3.5

The Z80A Counter Timer Controller (CTC) is a programmable four channel device that provides counting and timing functions for the system. The diagram is shown on page 9 of 15, MIC50x, and the block diagram is shown in fig. 3.8.

The internal structure of the Z80-CTC consists of a Z80 CPU bus interface, internal control logic, four counter channels, and interrupt control logic. Each channel has an interrupt vector for automatic interrupt vectoring, and interrupt priority is determined by channel number with channel 0 having the highest priority.

The channel logic is composed of 2 registers, 2 counters, and control logic as shown in fig. 3.9. The registers include an 8-bit constant register and an 8-bit channel control register. The counters include an 8-bit readable down counter and an 8-bit prescaler. The prescaler may be programmed to divide the system clock by either 16 or 256.

Channel 0 and 1 are used to generate the clock to LINE 1 and 2 in one of the Z80A-SIO/2. The clock delivered to the SIO is again divided in the SIO to make the baudrate for the terminal and printer connections. Input to these two channels is a clock of 0.614MHz.

Channel 2 and 3 are initiated in counter mode with interrupt enabled and with a time constant of 1. This means that for every clock input an interrupt is sent to the CPU. Channel 2 is connected to the display controller connector and channel 3 is connected to the connector for FUTURE USE, and in this way their interrupt is connected to the CPU.

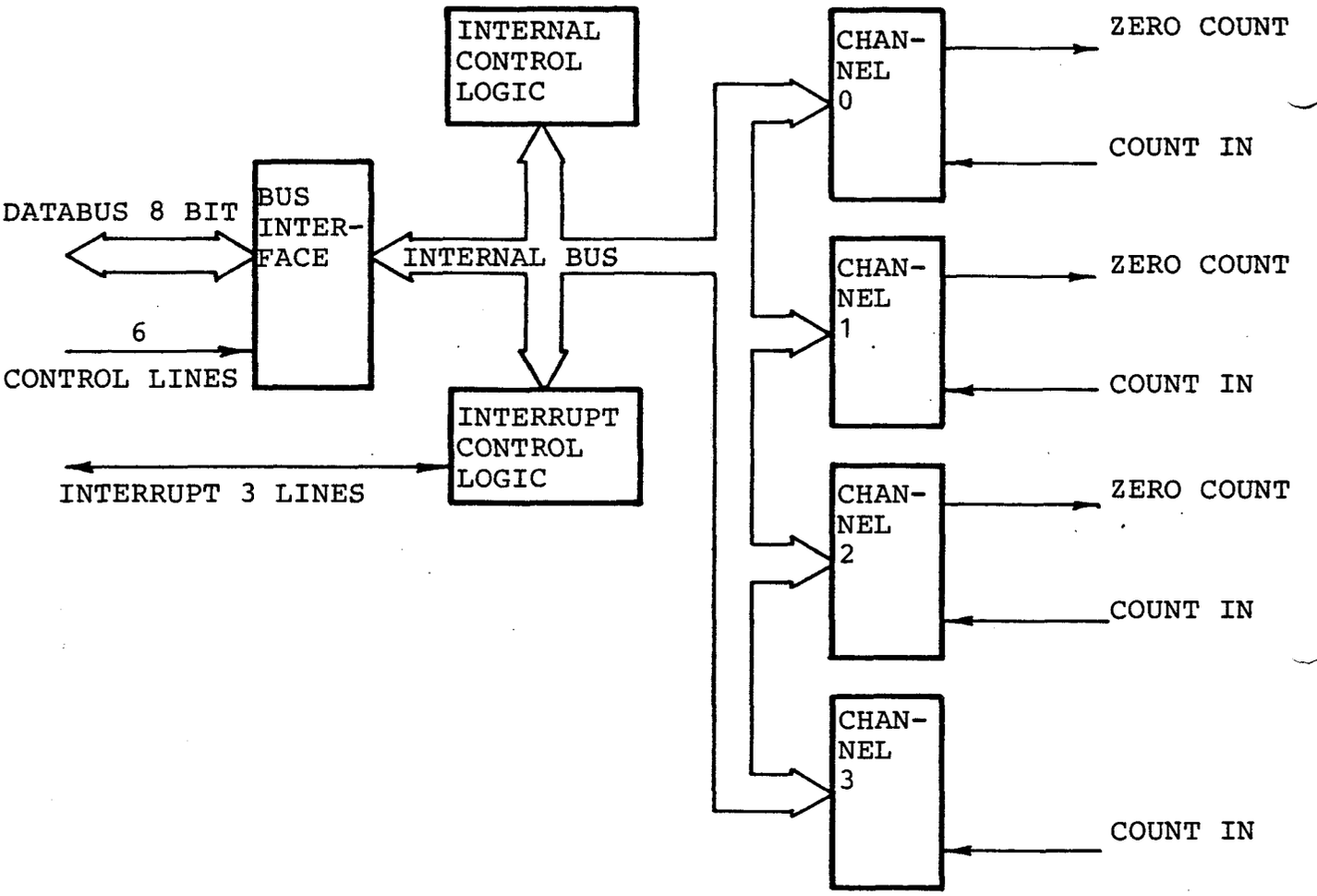


Fig. 3.8
BLOCK DIAGRAM FOR Z-80A CTC

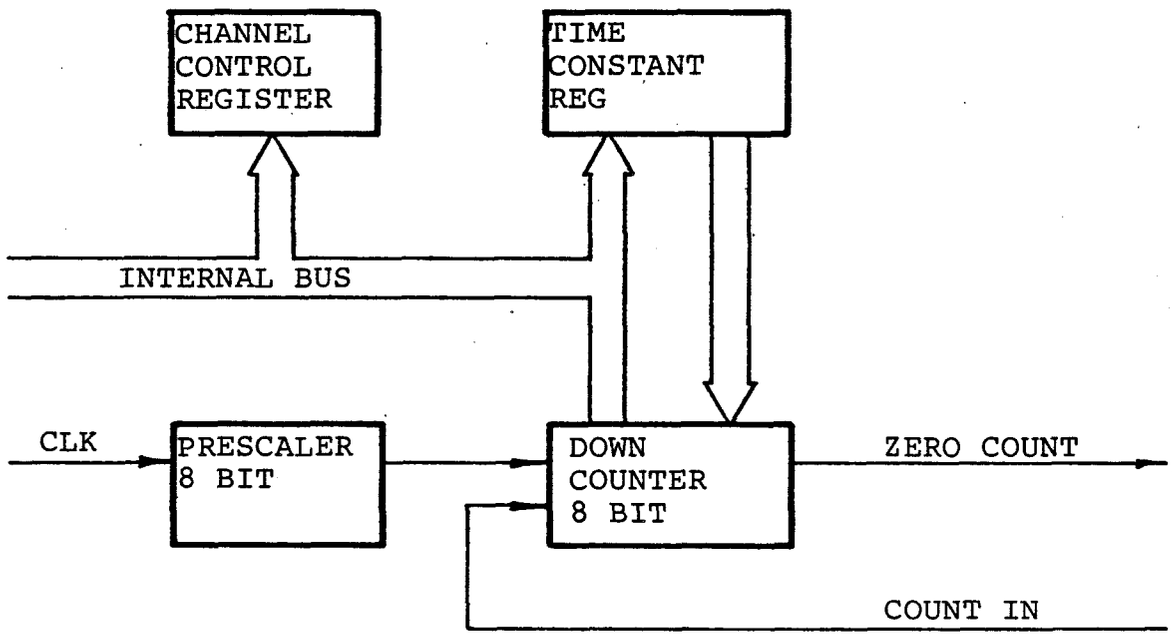


Fig. 3.9
BLOCK DIAGRAM FOR ONE CHANNEL IN Z-80A CTC.

3.6 Interrupt System 3.6

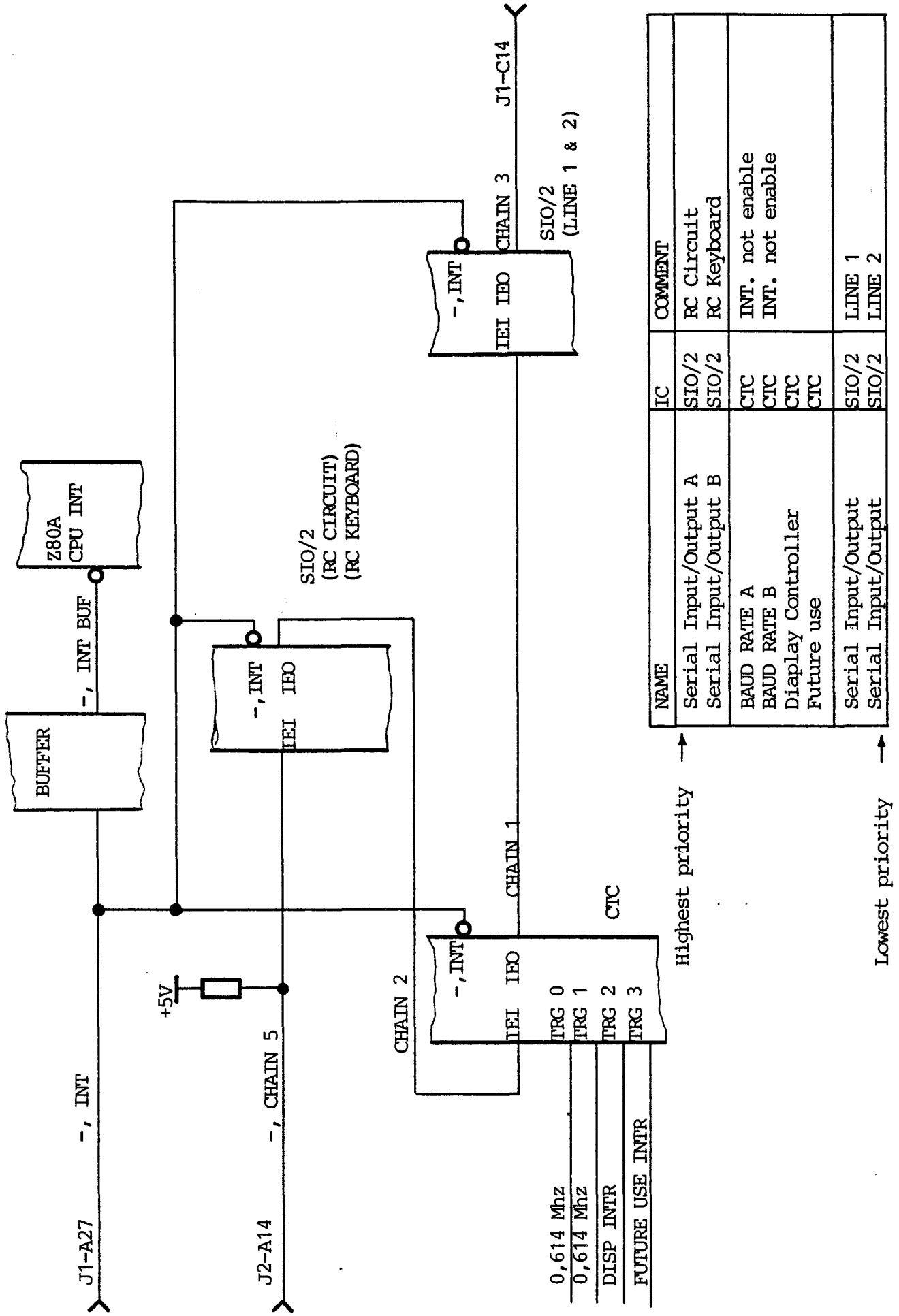
The CPU has two interrupt inputs, a software maskable interrupt and a non-maskable interrupt. The non-maskable interrupt (NMI) cannot be disabled by the program and is not used in RC850. The CPU can be programmed to respond to maskable interrupts in one of three modes. In RC850 mode 2 is selected. In this mode a single 8-bit byte from the controller (the interrupt vector) is used to make an indirect call instruction.

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted a special M1 cycle (INTA) is generated. During this M1 cycle IORQ becomes active (instead of MREQ) indicating the INTA cycle.

The Z80 peripherals have an interrupt enable input (IEI) and an interrupt enable output (IEO) and are connected in daisy chain. The peripheral with IEI high and IEO low, will during INTA place the preprogrammed 8-bit interrupt vector on the data bus.

IEO is held low until a return from interrupt (RETI) instruction is executed by the CPU while IEI is high. The 2-byte RETI instruction is decoded internally by the peripheral for this purpose.

Fig. 3.10 shows the daisy chain interrupt system in RC850.



NAME	IC	COMMENT
Serial Input/Output A	SIO/2	RC Circuit
Serial Input/Output B	SIO/2	RC Keyboard
BAUD RATE A	CTC	INT. not enable
BAUD RATE B	CTC	INT. not enable
Diaplay Controller	CTC	
Future use	CTC	
Serial Input/Output	SIO/2	LINE 1
Serial Input/Output	SIO/2	LINE 2

Fig. 3.10
Interrupt Priority in RC 850

3.7 ROM Memory 3.7

The ROM, Read Only Memory, contains the power up program. After a reset signal is generated, the CPU starts to execute the program from address 0.

3.8 RAM Memory 3.8

The RAM, Random Access Memory, is shown in 3 blocks in the block diagram: the TIMING GEN block, the 64K BYTES RAM block, and the REG. block. This subsection describes these 3 blocks. The circuit diagram is on page 7 of 15, MIC50x. The timing generator is made using the IC I8202. This circuit makes all the signals which the RAM circuits need. Fig. 3.11 shows the block diagram for the I8202 and the timing diagram for the whole RAM circuit is shown in fig. 3.12.

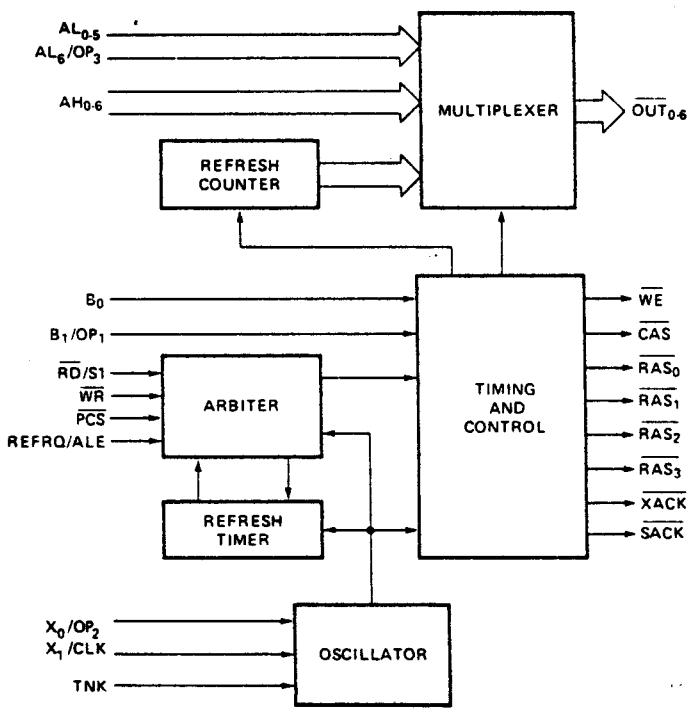


Fig. 3.11
Block Diagram for I 8202 RAM Controller

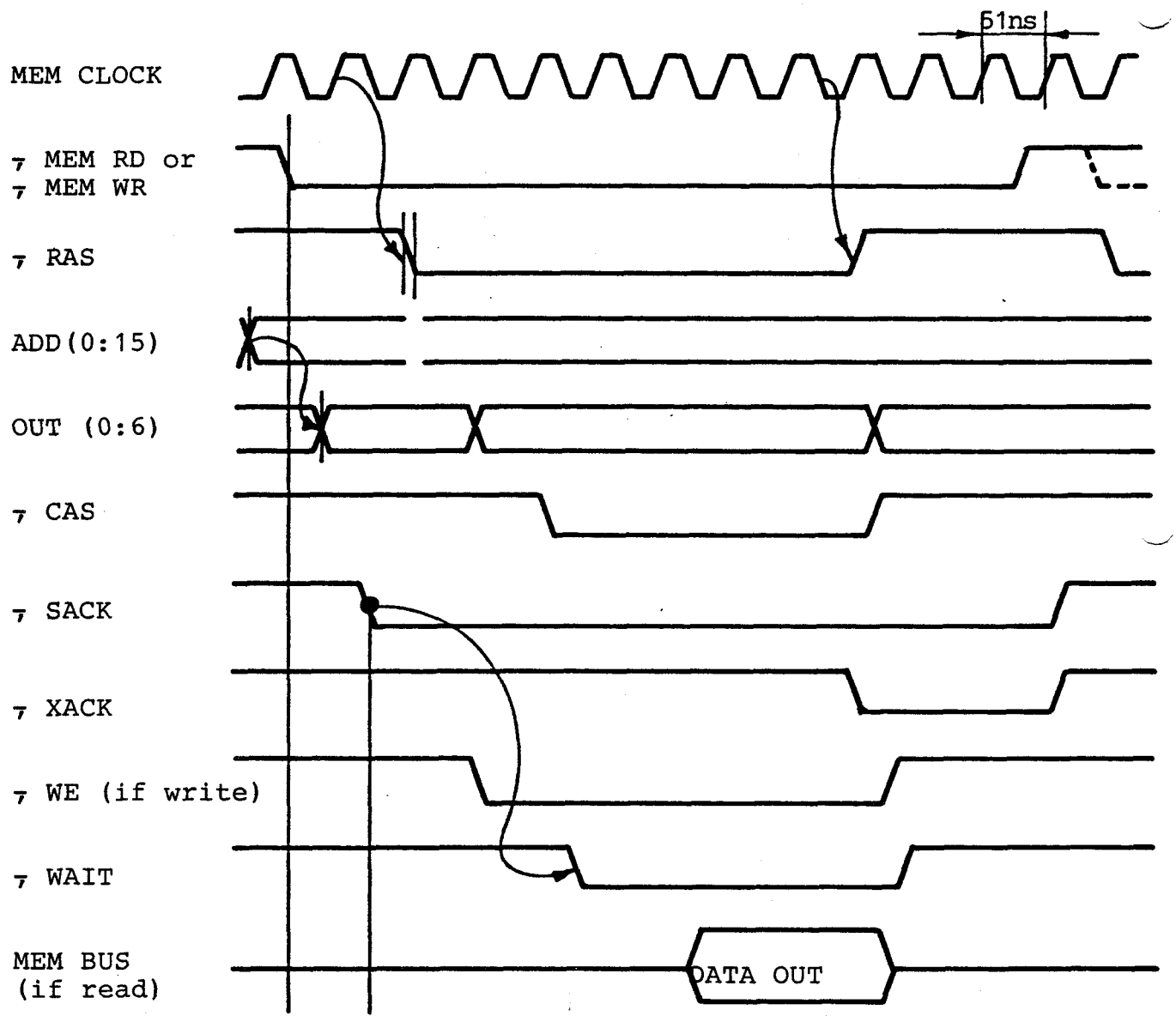


Fig. 3.12

TIMING DIAGRAM FOR RAM SYSTEM

3.9 DMA Controller

The DMA controller to MIC702 is based on the Am9517A-4 from Advance Micro Devices or an 8237-2 from Intel. The IC is designed to be used in conjunction with an external 8-bit address register made by an 74LS373. The circuit diagram is shown on page 4 of 25, MIC50x. The Am9517A-4 contains 4 channels which have full 64K address and word count capability.

The four channels are in RC850 used in the following way:

channel 0: VISUAL display controller
channel 1: FUTURE USE
channel 2: FUTURE USE
channel 3: External debugger.

The block diagram for Am9517A-4 is shown in fig. 3.13.

Fig. 3.14 shows the timing diagram for a normal operation of Am9517A-4.

More specific description of the units may be obtained from one of the two manufacturers.

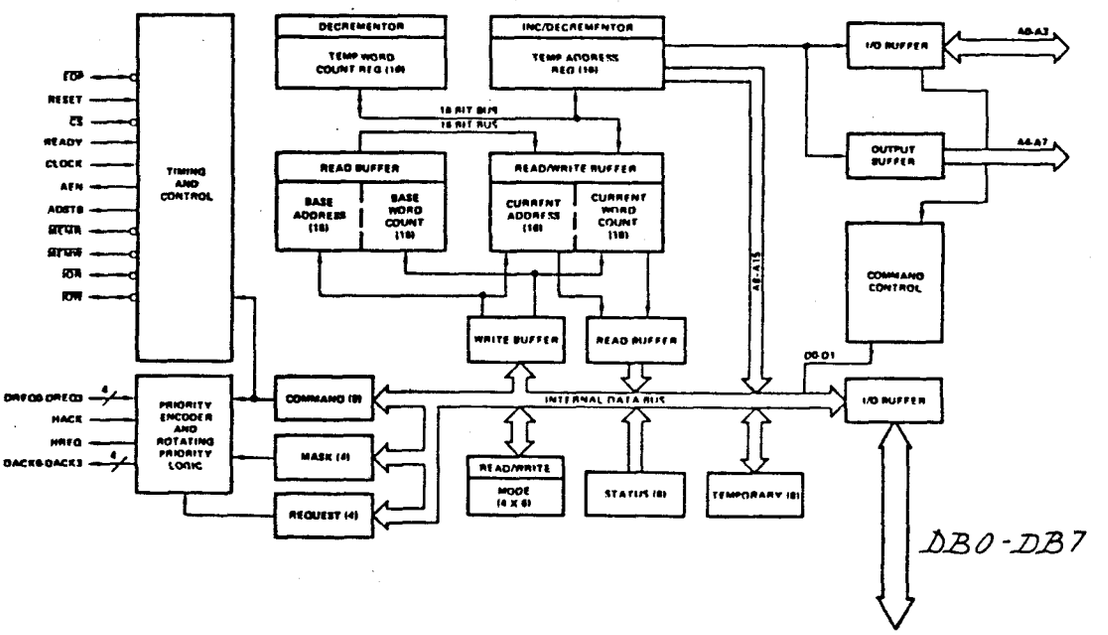
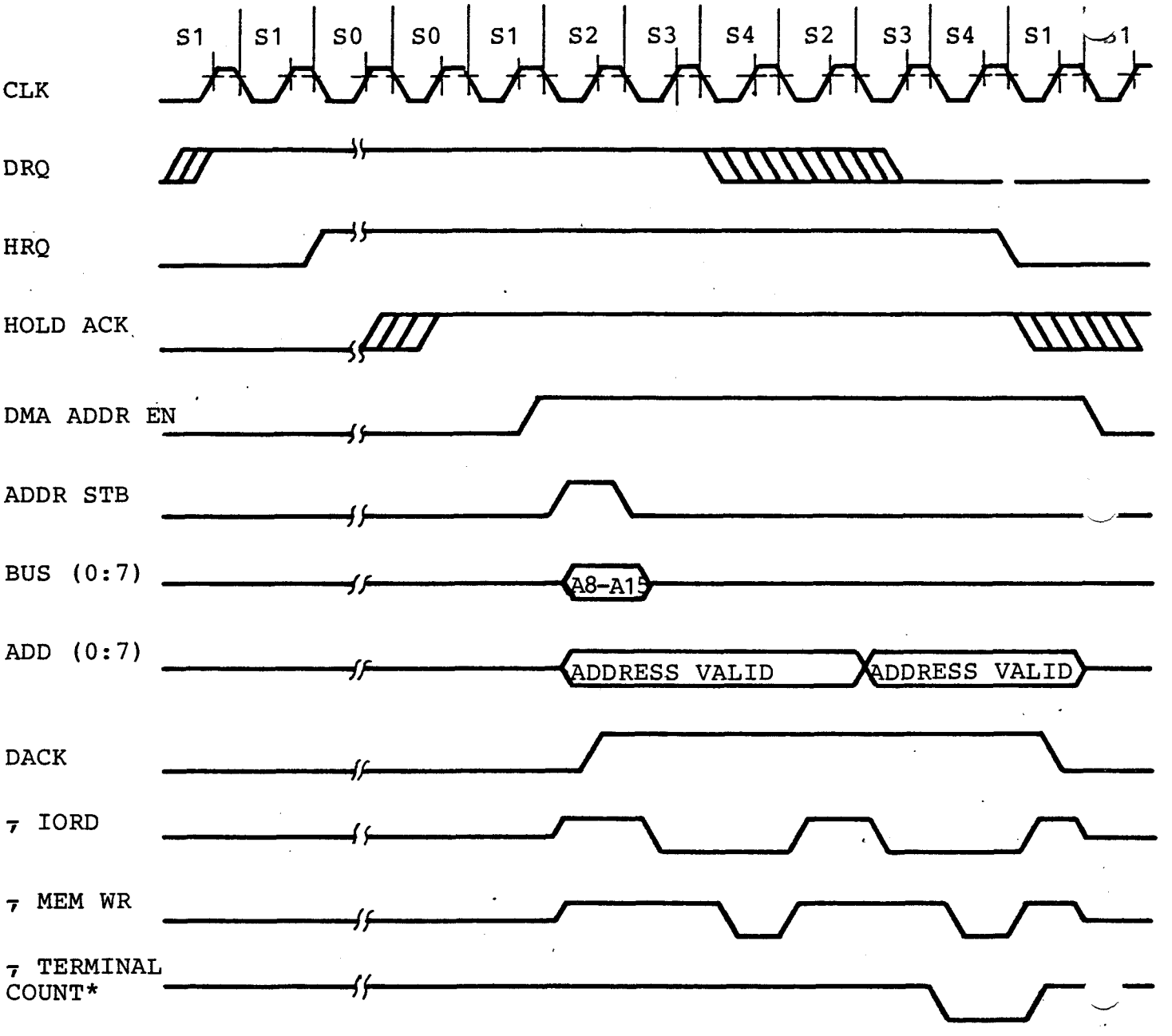


Fig. 3.13
Block Diagram for AM 9517A-4



* Only if last byte in the block

Fig. 3.14

TIMING DIAGRAM FOR Am 9517A-4 DMA CONTROLLER

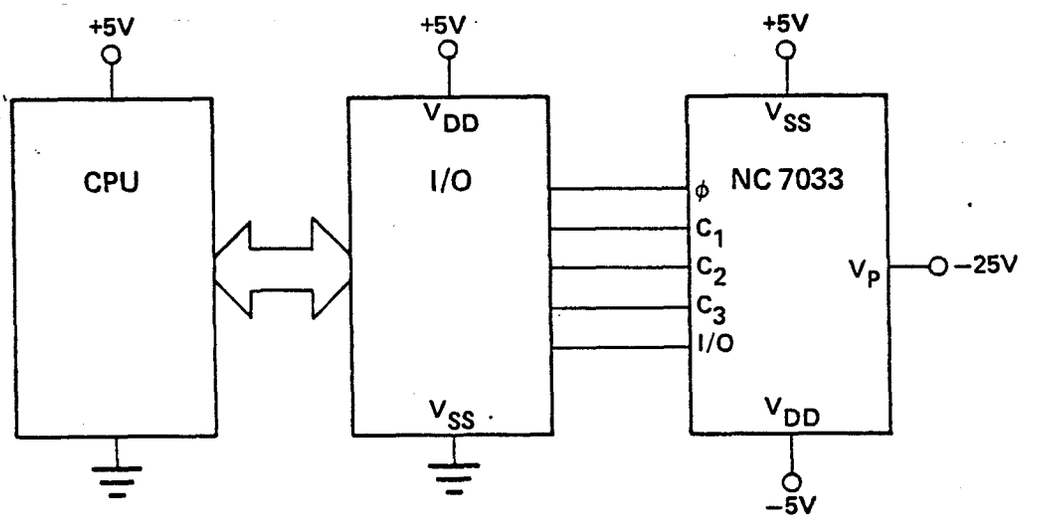
3.10 Non Volatile Memory 3.10

The NC7033 is a low-cost 21 word by 16-bit electrically alterable non volatile memory designed especially for use in the systems which require secure, yet alterable, data storage. Each entire 16-bit word is individually addressable and alterable by means of three control lines (C_1, C_2, and C_3) and a serial input/output port. An external clock is used to synchronize all operations of READ, WRITE, and ERASE.

Each active (READ, ERASE, WRITE) operation is initiated by the proper sequencing of control line (see fig. 3.15) followed by the appropriate 5-bit binary address code presented to the I/O port. The corresponding operation is then completed by the external clock. When not in use the NC7033 should be left either OFF or in a stand-by condition for maximum data retention.

The programming is described in detail in data sheet from NITRON.

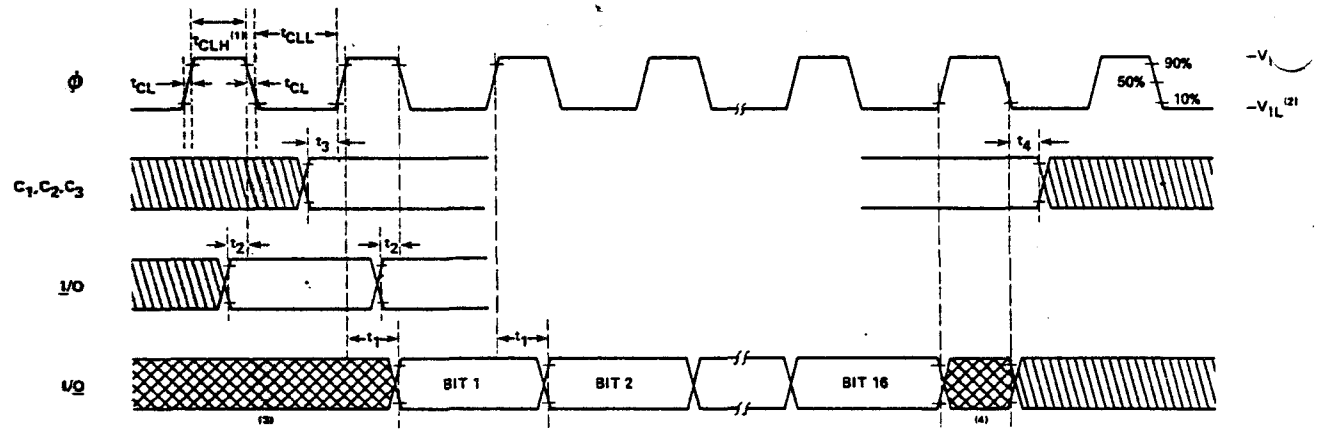
INTERFACE SCHEMATICS



C_1*	C_2*	C_3*	Instruction
1	1	1	STANDBY
0	0	1	ERASE
0	1	0	WRITE
0	1	1	SERIAL DATA OUT
0	0	0	SETUP
1	0	0	SERIAL ADDRESS IN
1	0	1	SERIAL DATA IN
1	1	0	READ

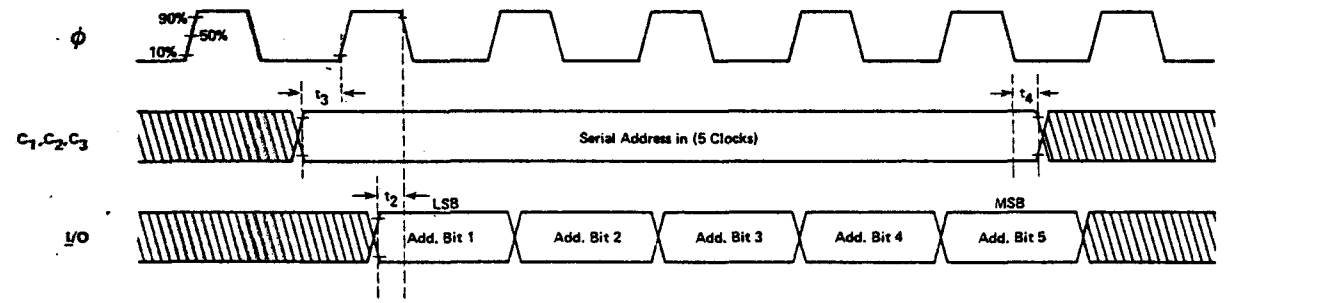
Fig. 3.15

TIMING DIAGRAMS

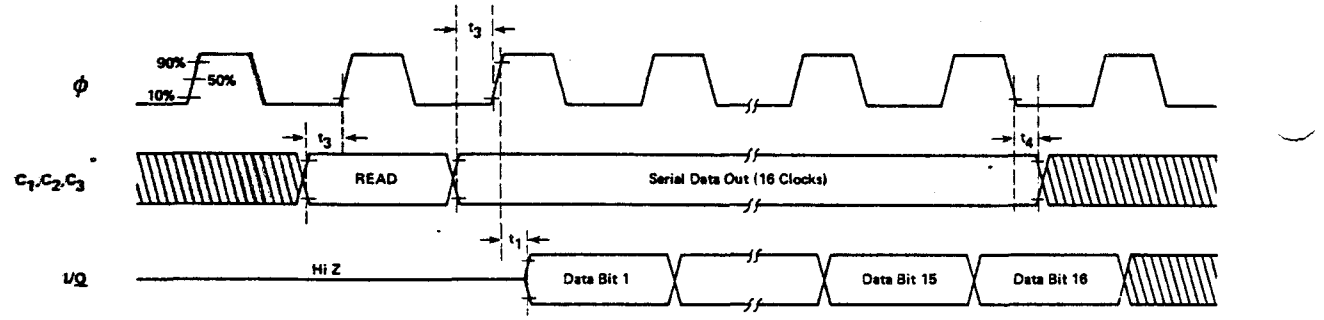


NOTES:
1. Independent of clock frequency t_{CLH} maximum is 10μsec.
2. Defines V_{IH}, V_{IL} levels for all figures.
3. Output depends on mode: (a) Internal pull up to V_{SS} acts during Address or Data Input, (b) Hi Z all other modes except Data Out.
4. Last data bit output indeterminate during this time.

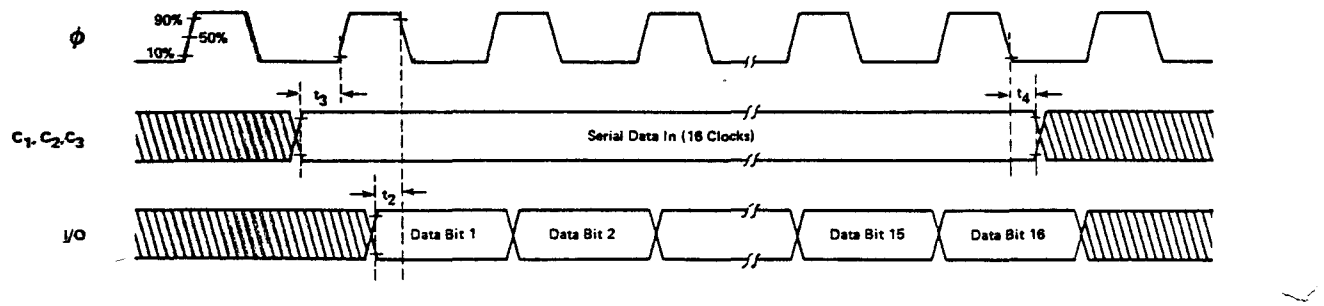
GENERAL



SERIAL ADDRESS IN



READ AND SERIAL DATA OUT



SERIAL DATA IN

Fig. 3.16

3.11 CRT-Module 3.11

The CRT-module contains the CRT-controller, refresh RAM, the character generator, and the parallel-to-serial conversion of video information.

3.11.1 CRT-Controller 3.11.1

The MC6845 CRT-controller performs the interface to raster scan CRT display, and it is optimized for hardware/software balance in order to achieve integration of all key functions and maintain flexibility.

The primary function of the CRT C is to generate refresh addresses (MA0-MA13) to the refresh memory, row selects (RA0-RA4) to the character generator, and video monitor timing (H SYNC, V SYNC) and Display Enable. Other functions include an internal cursor register which generates a cursor output when its contents compare to the current Refresh Address. The processor communicates with the CRT C through a buffered 8-bit Data Bus by reading/writing into the 18-register file of the CRT C (see fig. 3.17).

The programming is described in detail in manual from MOTOROLA.

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Register #	Register File	Program Unit	Read	Write	Number of Bits 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	–	–	–	–								
0	0	X	X	X	X	X	X	Address Register	–	No	Yes								
0	1	0	0	0	0	0	R0	Horizontal Total	Char.	No	Yes								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Char.	No	Yes								
0	1	0	0	0	1	0	R2	H. Sync Position	Char.	No	Yes								
0	1	0	0	0	1	1	R3	H. Sync Width	Char.	No	Yes								
0	1	0	0	1	0	0	R4	Vertical Total	Char. Row	No	Yes								
0	1	0	0	1	0	1	R5	V. Total Adjust	Scan Line	No	Yes								
0	1	0	0	1	1	0	R6	Vertical Displayed	Char. Row	No	Yes								
0	1	0	0	1	1	1	R7	V. Sync Position	Char. Row	No	Yes								
0	1	0	1	0	0	0	R8	Interlace Mode	–	No	Yes								
0	1	0	1	0	0	1	R9	Max Scan Line Address	Scan Line	No	Yes								
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line	No	Yes		B	P			(Note 1)		
0	1	0	1	0	1	1	R11	Cursor End	Scan Line	No	Yes								
0	1	0	1	1	0	0	R12	Start Address (H)	–	No	Yes								
0	1	0	1	1	0	1	R13	Start Address (L)	–	No	Yes								
0	1	0	1	1	1	0	R14	Cursor (H)	–	Yes	Yes								
0	1	0	1	1	1	1	R15	Cursor (L)	–	Yes	Yes								
0	1	1	0	0	0	0	R16	Light Pen (H)	–	Yes	No								
0	1	1	0	0	0	1	R17	Light Pen (L)	–	Yes	No								

Note (1): Bit 5 of the Cursor Start Raster Register is used for blink period control, and Bit 6 is used to select blink or non-blink.

Fig. 3.17

3.11.2 Refresh RAM

3.11.2

2K of 8 or 16 bits Random Access Memory used to contain the picture of the screen. No. of bits installed depends on Character Generator size and attribute facilities.

The refresh RAM contains a copy of part of the main memory, which includes the picture. This is done to release the main memory from the time consuming refresh work. The refresh RAM is under DMA control updated from the main memory.

3.11.3 Character Generator

3.11.3

Generates the dot matrix to be displayed on the screen. Characters are presented in a 16 dot wide and up to 16 dot high dot matrix, normally 16 x 14. The dot information is stored in ROMs (128 characters) and (if installed) up to 256 characters in RAM. All most common European national letters are covered by the ROMs.

3.11.4 Parallel-to-Serial Video Conversion

3.11.4

Converts the parallel output from the character generator to serial video information. This again is fed to the video module (see below) for pulse shaping. The level of brightness for high intensity characters may be adjusted in the CRT module.

3.12 Video Module

3.12

This module performs signal conditioning and pulse shaping in order to obtain a crisp and clear picture on the screen.

3.13 Connector Module

3.13

All connectors in and out of the Display Terminal are assembled here, so this module contains the line conditioning circuits for the CCITT V24, X21 and the EIA RS232C. It also contains the RC circuit interface, which is a 259K bit/s. transformer connected serial interface.

3.14 Power Supply Module 3.14

This module is assembled of an AC (Alternate Current) part including ON/OFF switch, fuse, noise filter, and a transformer with thermal shut-down, and a DC (Direct Current) part including a switching regulator for +5V, and 2 serial regulators for +12 V and -12V. The power supply includes overvoltage and current fold-back features.

3.15 Monitor Module 3.15

This module contains a high quality, high resolution and high reliable CRT (Cathode Ray Tube) monitor of 15" diagonal. A separate AC module is incorporated in the monitor. The monitor has its own manual from the manufacturer.

3.16 Keyboard Module 3.16

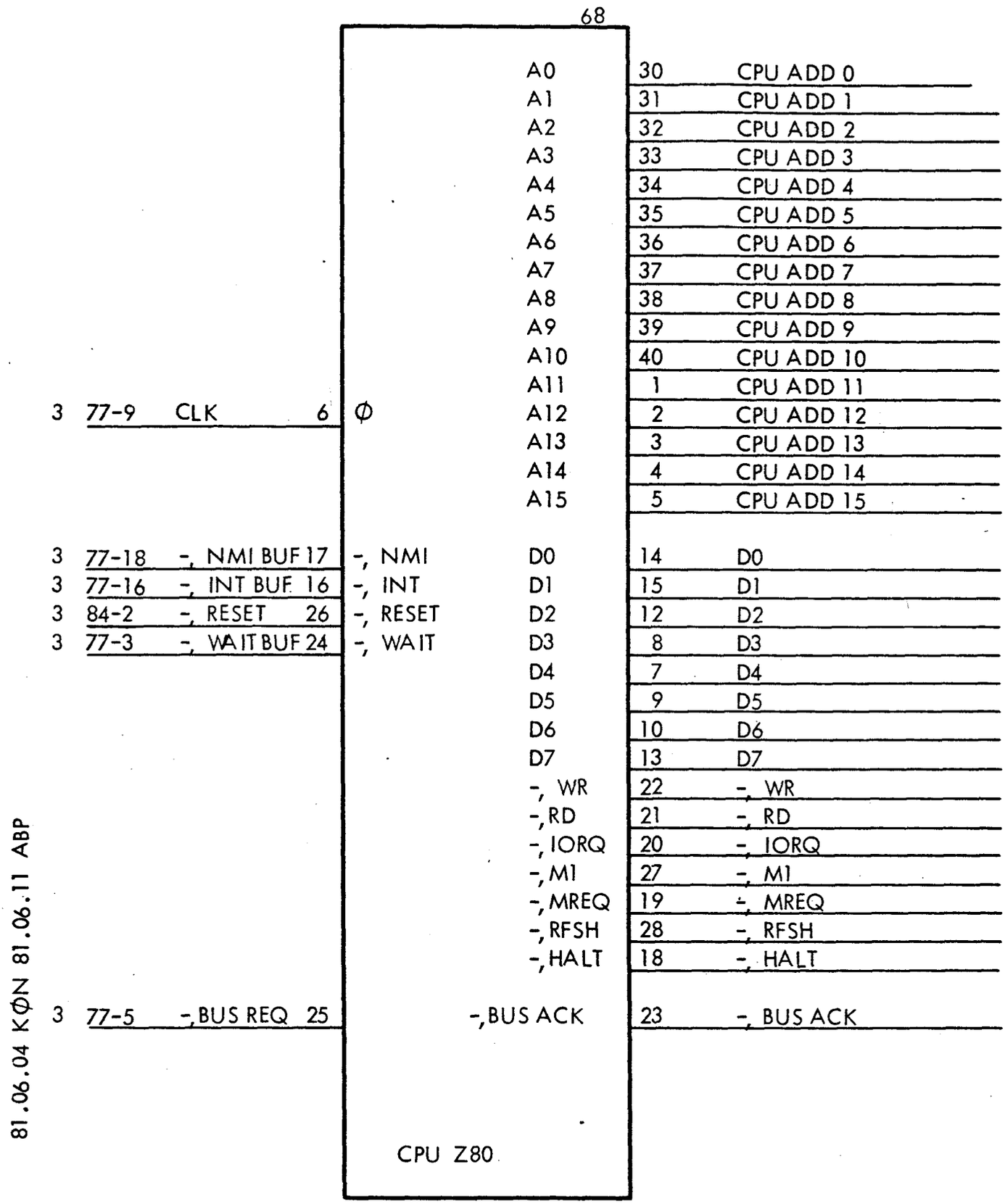
This module includes its own microprocessor, which does the scanning of the keys to determine key closures. The microprocessor also converts the key information to a serial bit stream, which is sent to the SIO placed in the CPU-module. Output to the keyboard ("beep", "click", and indicators) are likewise received in serial form.

The keys are of the capacitive type to ensure long and reliable life. To indicate a proper key closure a "click" sound is included. This sound together with the "beep" sound may be adjusted (even to zero) by the regulator on back of the keyboard.

The keyboard has its own manual.

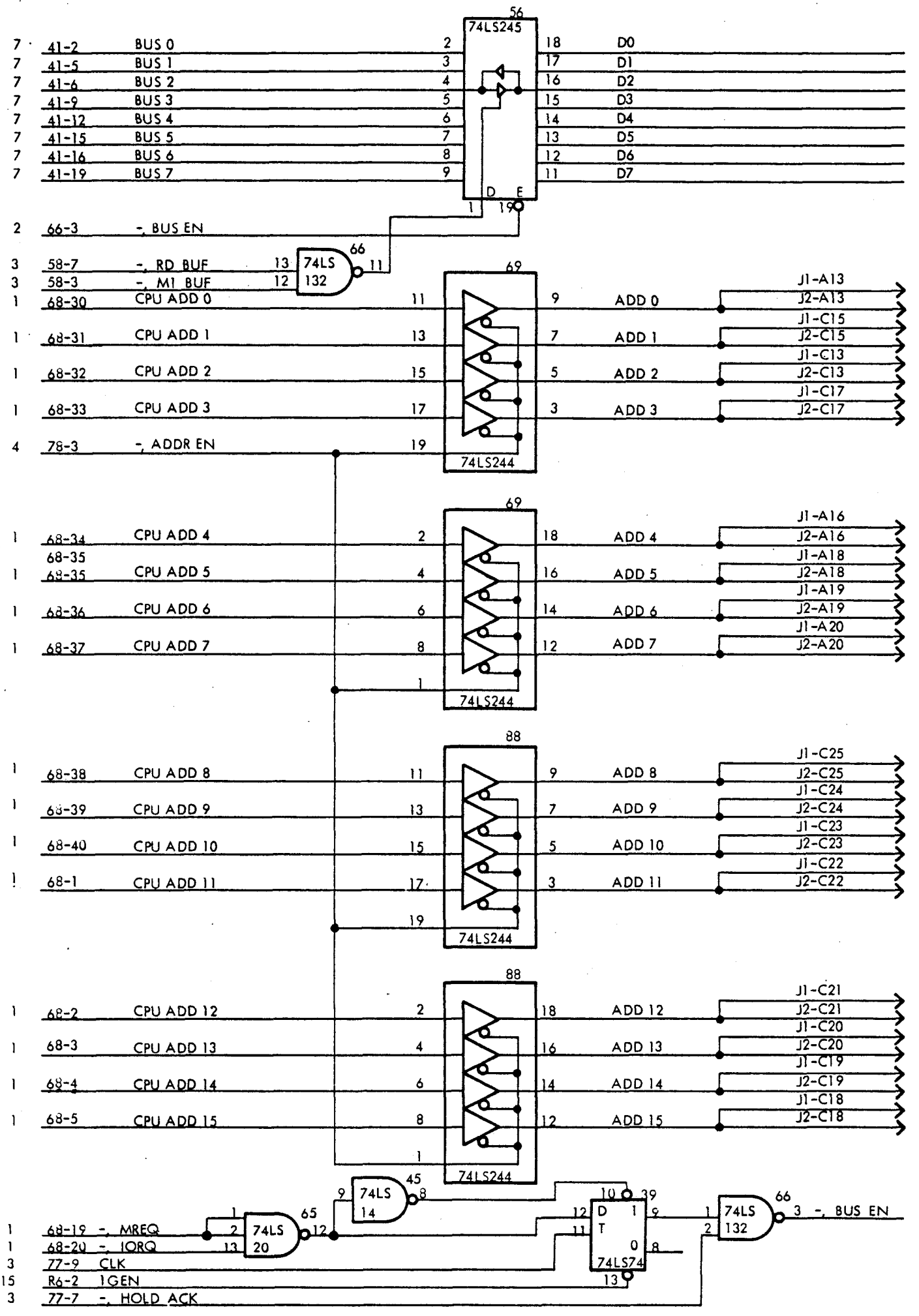
SIGNAL	DESTINATION	DESCRIPTION
-, BUS ACK	p. 3	BUS ACKnowledge
CPU ADD 0-15	p. 2	Central Processing Unit ADDress 0-15
D 0-7	p. 2	Data bus bit 0-7
-, HALT	p. 3	HALT state
-, IORQ	p. 2 p. 3	Input/Output ReQuest
-, M1	p. 3	Machine cycle one, the op-code fetch cycle
-, MREQ	p. 2 p. 3	Memory REQuest
-, RD	p. 3	ReaD
-, RFSH	p. 3	ReFreSH
-, WR	p. 3	WRite

14.05.1981 KØN


68
A0 30 CPU ADD 0
A1 31 CPU ADD 1
A2 32 CPU ADD 2
A3 33 CPU ADD 3
A4 34 CPU ADD 4
A5 35 CPU ADD 5
A6 36 CPU ADD 6
A7 37 CPU ADD 7
A8 38 CPU ADD 8
A9 39 CPU ADD 9
A10 40 CPU ADD 10
A11 1 CPU ADD 11
3 77-9 CLK 6 Φ A12 2 CPU ADD 12
A13 3 CPU ADD 13
A14 4 CPU ADD 14
A15 5 CPU ADD 15
3 77-18 -, NMI BUF 17 -, NMI D0 14 D0
3 77-16 -, INT BUF 16 -, INT D1 15 D1
3 84-2 -, RESET 26 -, RESET D2 12 D2
3 77-3 -, WAIT BUF 24 -, WAIT D3 8 D3
D4 7 D4
D5 9 D5
D6 10 D6
D7 13 D7
-, WR 22 -, WR
-, RD 21 -, RD
-, IORQ 20 -, IORQ
-, M1 27 -, M1
-, MREQ 19 -, MREQ
-, RFSH 28 -, RFSH
-, HALT 18 -, HALT
3 77-5 -, BUS REQ 25 -, BUS ACK 23 -, BUS ACK
CPU Z80
81.06.04 KΦN 81.06.11 ABP

SIGNAL	DESTINATION	DESCRIPTION
ADD 0	p. 4 p. 5 p. 6 p. 7 p. 9 p. 11 p. 14	ADDress bit 0
ADD 1	p. 4 p. 6 p. 7 p. 9 p. 11 p. 14	See above
ADD 2-11	p. 4 p. 5 p. 6 p. 7	See above
ADD 12-15	p. 4 p. 5 p. 7	See above
-, BUS EN	p. 2	BUS ENable. This signal is true when the central processing unit is the bus master.
D 0-7	p. 1	Data bus bit 0-7

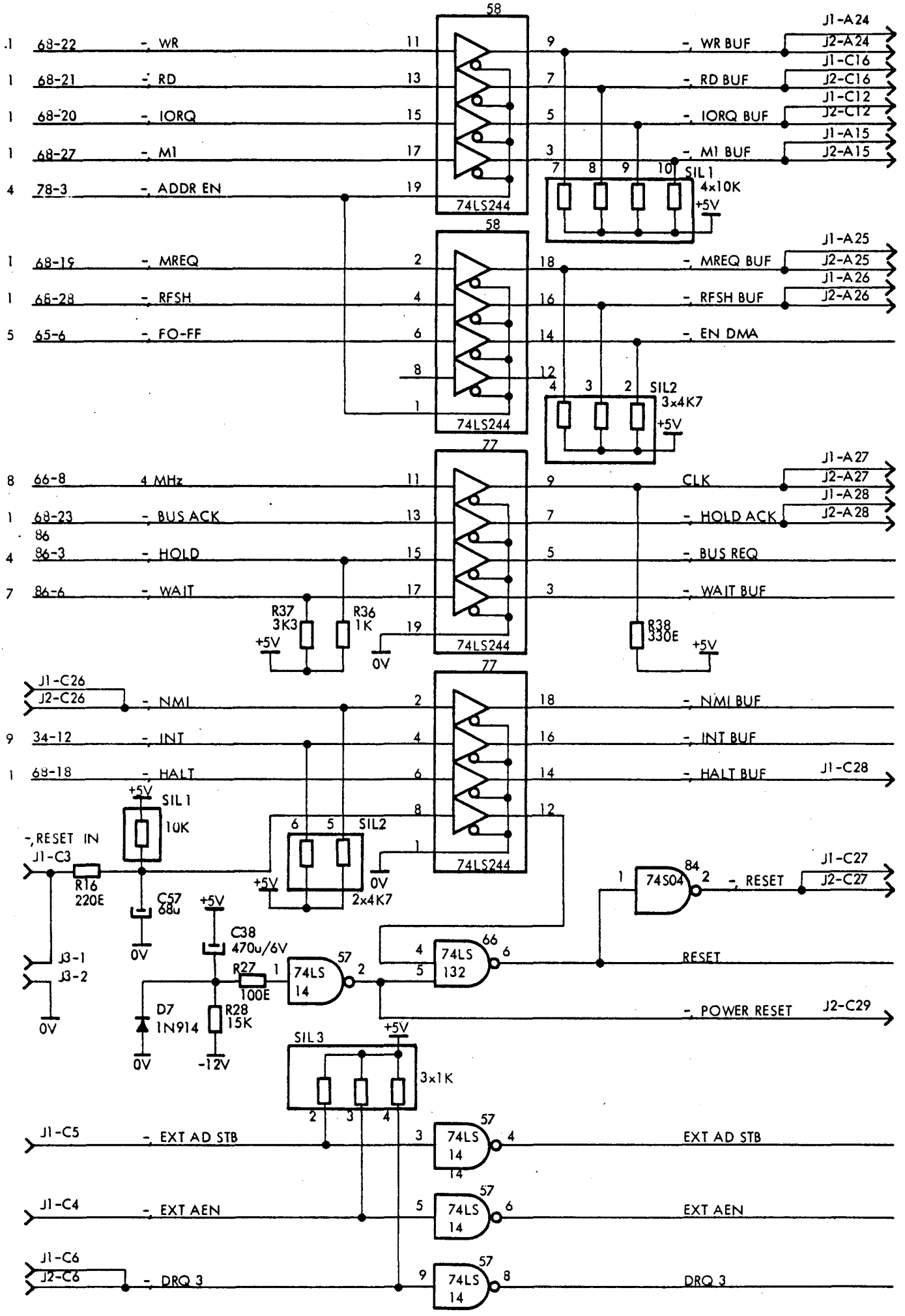
14.05.1981 KØN



81.06.04 KØN 81.06.11 ABP

SIGNAL	DESTINATION	DESCRIPTION
-, BUS REQ	p. 1	BUS REQuest
CLK	p. 1 p. 2 p. 5 p. 15 p. 20	CLocK
DRQ 3	p. 4	Direct memory access ReQuest 3
-, EN DMA	p. 4	ENable the Direct Memory Access controller
EXT AD STB	p. 4	EXTernal ADdress STroBe
EXT A EN	p. 4	EXTernal Address ENable
-, HALT BUF	p. 3	HALT BUFfered
-, HOLD ACK	p. 2 p. 4	HOLD ACKnowledge
-, INT BUF	p. 1	INTerrupt BUFfered
-, IORQ BUF	p. 2 p. 4 p. 9 p. 11 p. 14	Input/Output ReQuest BUFfered
-, M1 BUF	p. 2 p. 9 p. 11	Machine cycle one BUFfered
-, MREQ BUF	p. 4 p. 7	Memory REQuest BUFfered
-, NMI BUF	p. 1	Non Maskable Interrupt BUFfered
-, POWER RESET	p. 3	POWER RESET
-, RD BUF	p. 2 p. 4 p. 9 p. 11	-, ReaD BUFfered
RESET	p. 4	RESET
-, RESET	p. 1 p. 9 p. 10 p. 11	See above
-, RFSH BUF	p. 3	ReFreSH BUFfered
-, WAIT BUF	p. 1	WAIT BUFfered
-, WR BUF	p. 2 p. 4	WRite BUFfered

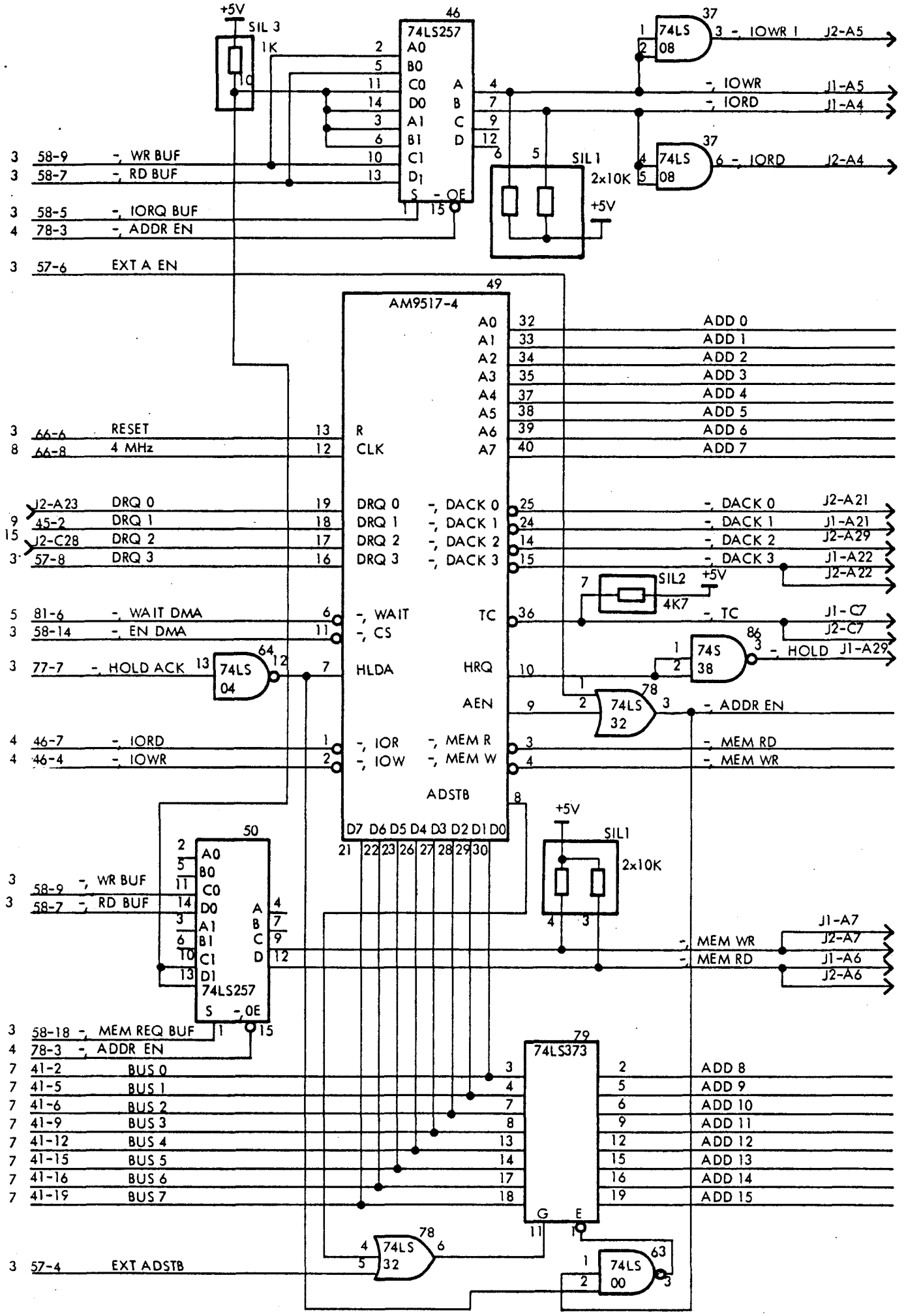
14.05.1981 KØN



81.06.04 KØN 81.06.11 ABP

SIGNAL	DESTINATION	DESCRIPTION
ADD 0	p. 4 p. 5 p. 6 p. 7 p. 9 p. 11 p. 14	ADDress bit 0
ADD 1	p. 4 p. 6 p. 7 p. 9 p. 11 p. 14	See above
ADD 2-11	p. 4 p. 5 p. 6 p. 7	See above
ADD 12-15	p. 4 p. 5 p. 7	See above
¬, ADDR EN	p. 2 p. 3 p. 4 p. 5	The ADDRess ENable signal is used to select the address bus master.
¬, DACK 0-1		Direct memory access ACKnowledge 0-1
¬, DACK 2	p. 14	See above
¬, DACK 3		See above
¬, HOLD	p. 3	HOLD request to the CPU
¬, IORD	p. 4 p. 10 p. 11 p. 13 p. 14	Input/Output ReaD
¬, IORD 1		See above
¬, IOWR	p. 4 p. 5 p. 10	Input/Output WRite
¬, IOWR1		See above
¬, MEM RD	p. 4 p. 5 p. 7	MEMory ReaD
¬, MEM WR	p. 4 p. 5 p. 7	
¬, TC		Terminal Count

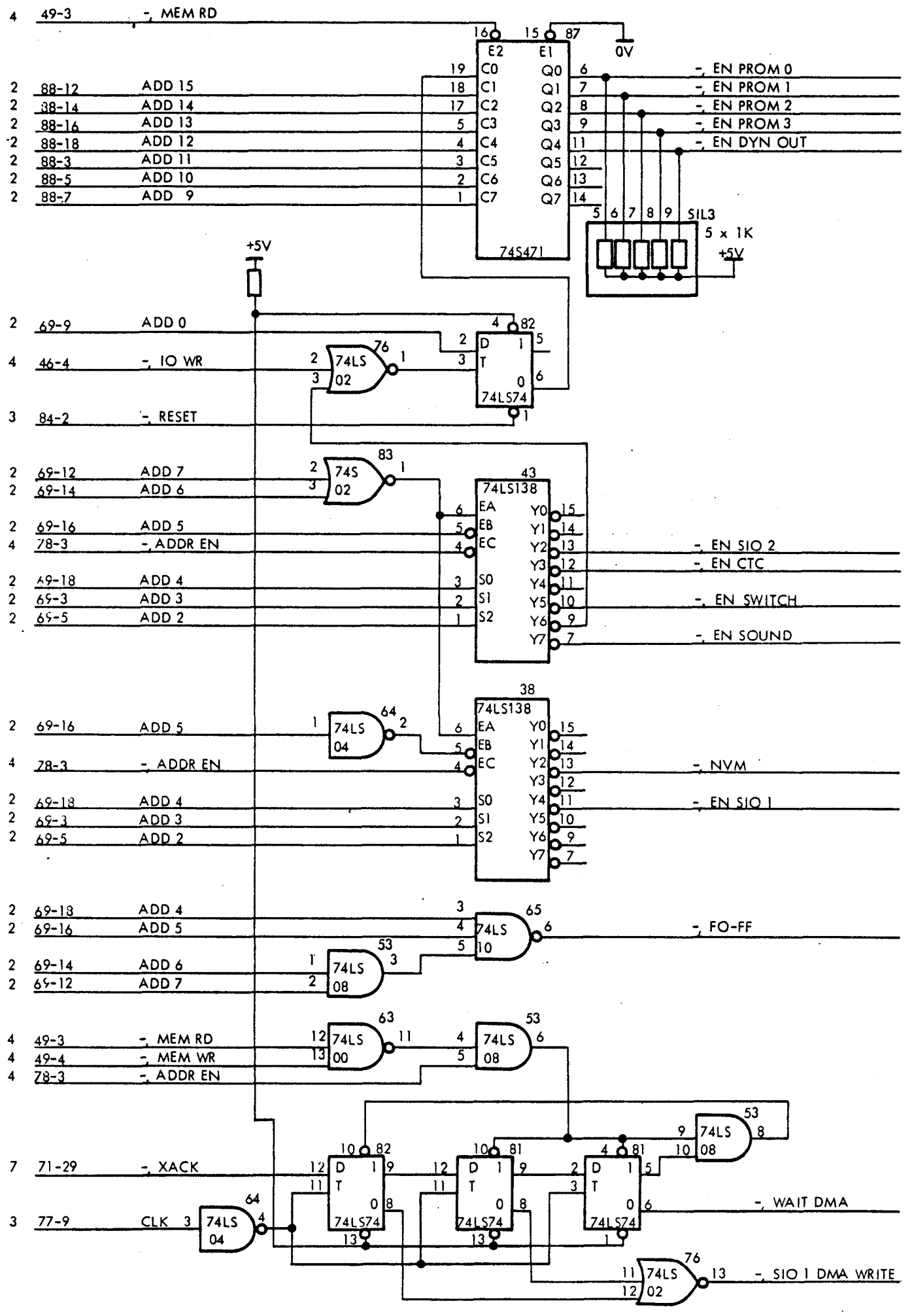
14.05.1981 KØN



81.06.04 KØN 81-06.11 ABP

SIGNAL	DESTINATION	DESCRIPTION
-, EN CTC	p. 9	ENable Counter Timing Circuit
-, EN DYN OUT	p. 7	ENable DYNamic memory OUTput
-, EN PROM 0-3	p. 6	ENable Programmable Read Only Memory
-, EN SIO1	p. 14	ENable Serial Input/Output
-, EN SIO2	p. 11	See above
-, EN SOUND	p. 13	ENable the V24 read status port
-, EN SWITCH	p. 13	ENable SWITCH information OC_H
-, F0-FF	p. 3	address $F0_H$-FF_H
-, NVM	p. 10	enable the Non-Volatile Memory
-, WAIT DMA	p. 4	WAIT for the Direct Memory Access controller
-, SIO1 DMA WRITE	p. 14	WRITE to SIO1 under DMA transfer

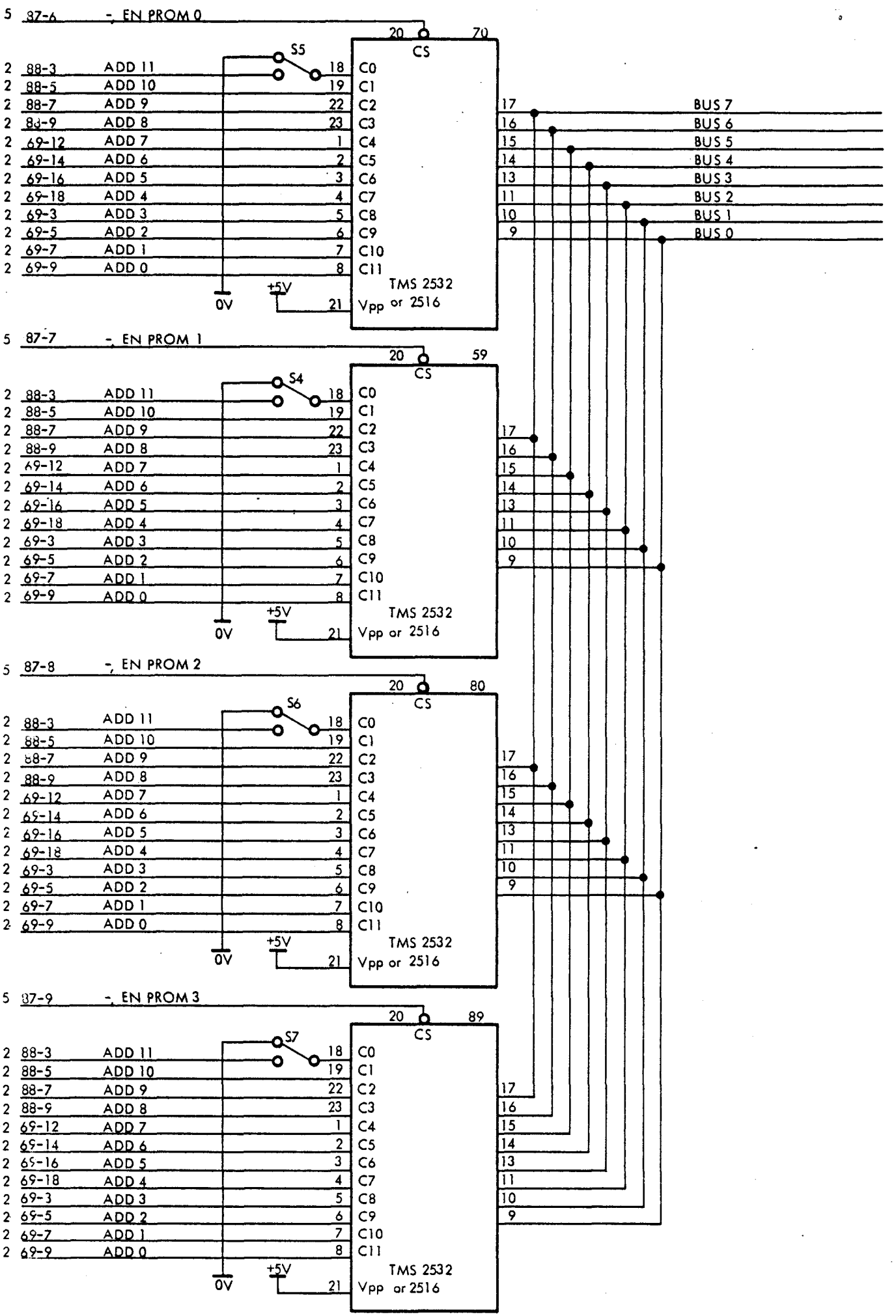
14.05.1981 KØN



81.06.04 KØN 81.06.11 ABP

SIGNAL	DESTINATION	DESCRIPTION
BUS 0-7	p. 2 p. 4 p. 7 p. 9 p. 10 p. 11 p. 13	data BUS bit 0-7

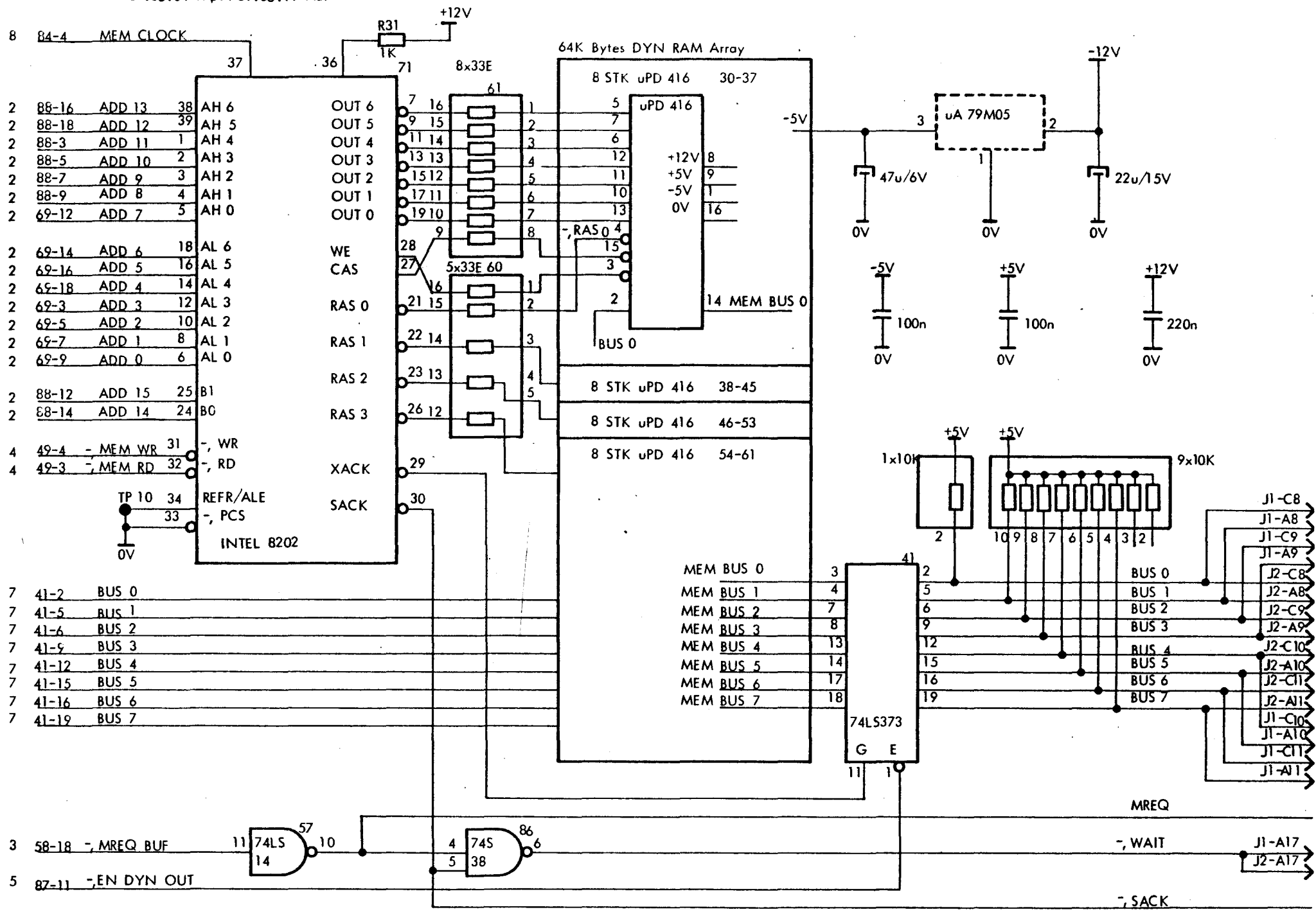
14.05.1981 KØN



81.06.04 KØN 81.06.11 ABP

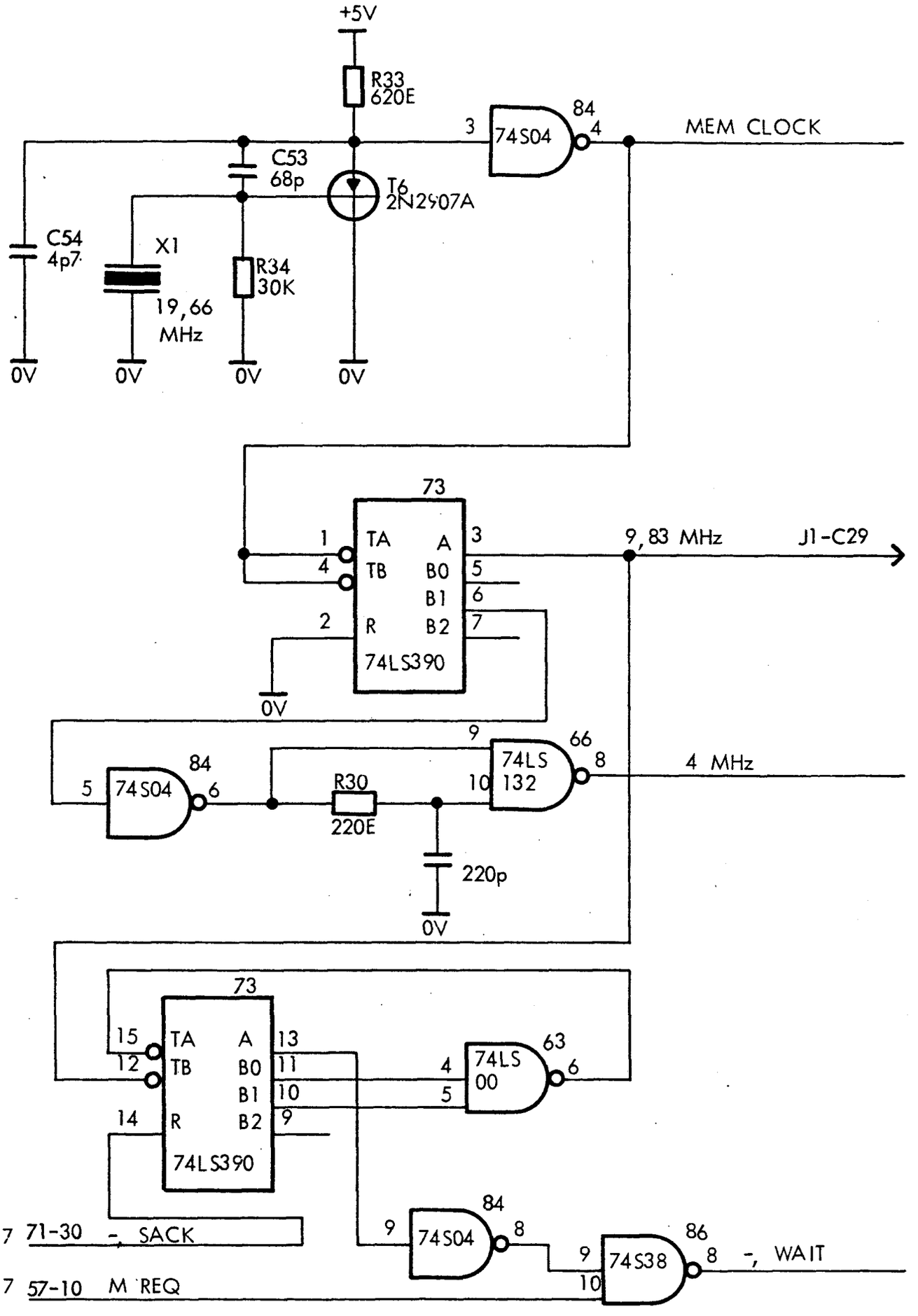
SIGNAL	DESTINATION	DESCRIPTION
BUS 0-7	p. 2 p. 4 p. 6 p. 9 p. 10 p. 11 p. 13	data BUS bit 0-7
MREQ	p. 8	Memory REQuest
-, SACK	p. 8	System ACKnowledge
-, WAIT	p. 3 p. 8 p. 11	WAIT for the CPU

14.05.1981 KØN


81.06.04 KØN 81.06.11 ABP
8 84-4 MEM CLOCK
R31
1K
+12V
37
36
71
8x33E
61
64K Bytes DYN RAM Array
8 STK uPD 416 30-37
8 STK uPD 416 38-45
8 STK uPD 416 46-53
8 STK uPD 416 54-61
uPD 416
+12V
+5V
-5V
0V
-, RAS 0
14 MEM BUS 0
BUS 0
-5V
uA 79M05
47u/6V
22u/15V
100n
220n
0V
2 88-16 ADD 13 38 AH 6
2 88-18 ADD 12 39 AH 5
2 88-3 ADD 11 1 AH 4
2 88-5 ADD 10 2 AH 3
2 88-7 ADD 9 3 AH 2
2 88-9 ADD 8 4 AH 1
2 69-12 ADD 7 5 AH 0
2 69-14 ADD 6 18 AL 6
2 69-16 ADD 5 16 AL 5
2 69-18 ADD 4 14 AL 4
2 69-3 ADD 3 12 AL 3
2 69-5 ADD 2 10 AL 2
2 69-7 ADD 1 8 AL 1
2 69-9 ADD 0 6 AL 0
2 88-12 ADD 15 25 B1
2 88-14 ADD 14 24 B0
OUT 6
OUT 5
OUT 4
OUT 3
OUT 2
OUT 1
OUT 0
WE
CAS
RAS 0
RAS 1
RAS 2
RAS 3
XACK
SACK
5x33E 60
4 49-4 -, MEM WR 31 -, WR
4 49-3 -, MEM RD 32 -, RD
TP 10 34 REFR/ALE
33 -, PCS
INTEL 8202
0V
7 41-2 BUS 0
7 41-5 BUS 1
7 41-6 BUS 2
7 41-9 BUS 3
7 41-12 BUS 4
7 41-15 BUS 5
7 41-16 BUS 6
7 41-19 BUS 7
MEM BUS 0
MEM BUS 1
MEM BUS 2
MEM BUS 3
MEM BUS 4
MEM BUS 5
MEM BUS 6
MEM BUS 7
74LS373
G E
41
1x10K
9x10K
BUS 0
BUS 1
BUS 2
BUS 3
BUS 4
BUS 5
BUS 6
BUS 7
J1-C8
J1-A8
J1-C9
J1-A9
J2-C8
J2-A8
J2-C9
J2-A9
J2-C10
J2-A10
J2-C11
J2-A11
J1-C10
J1-A10
J1-C11
J1-A11
MREQ
3 58-18 -, MREQ BUF
74LS 14
57
74S 38
86
-, WAIT
J1-A17
J2-A17
5 87-11 -, EN DYN OUT
-, SACK

SIGNAL	DESTINATION	DESCRIPTION
MEM CLOCK	p. 7	MEMory CLOCK
4 MHz	p. 3 p. 4	4 MHz clock
9,83 MHz	p. 9	9,83 MHz clock
-, WAIT	p. 3 p. 7 p. 11	WAIT for the CPU

14.05.1981 KØN



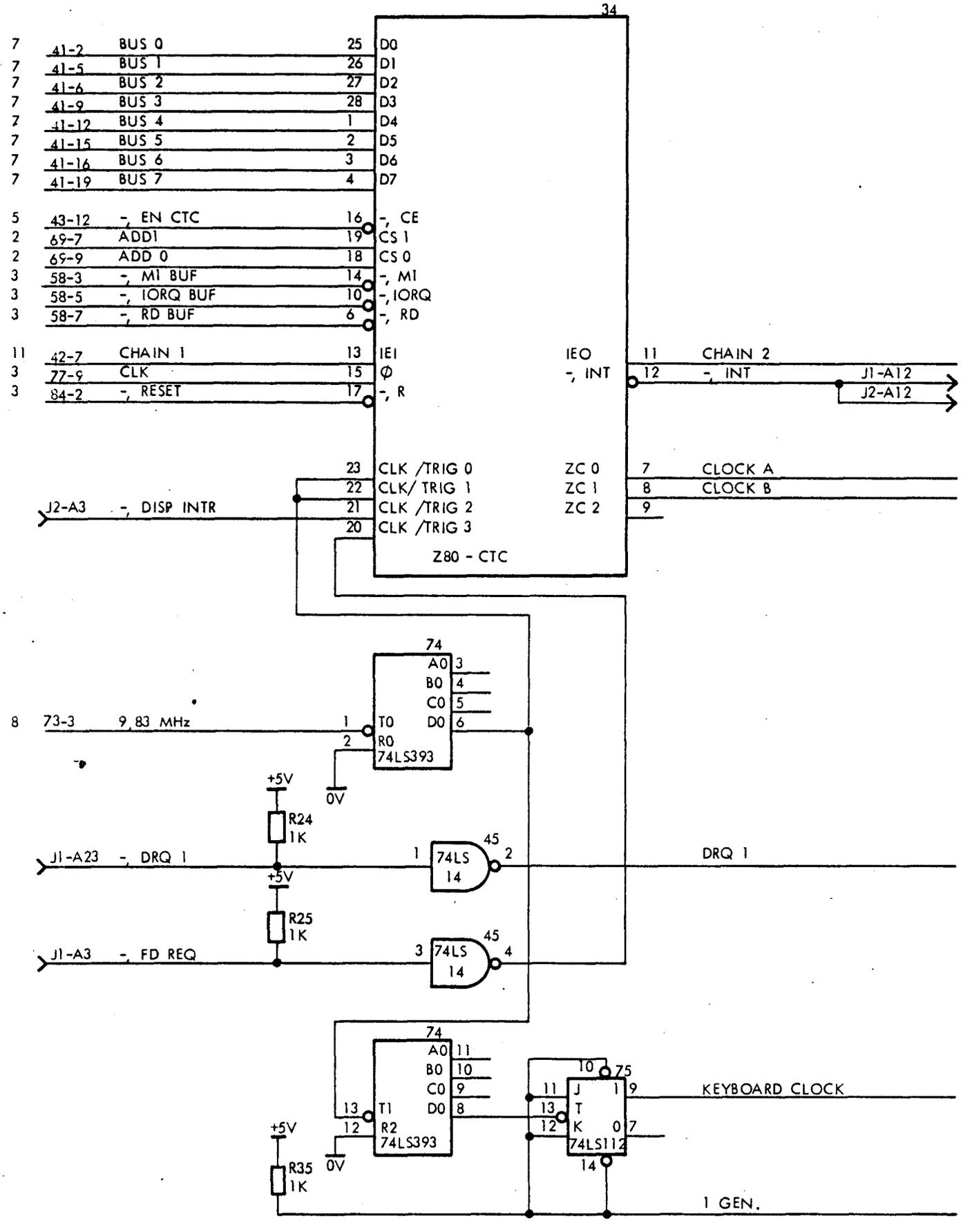
81.06.04 KØN 81.06.11 ABP

MIC 50x SYSTEM CLOCK p8 of 15

A25942 Circuit Diagram

SIGNAL	DESTINATION	DESCRIPTION
CHAIN 2	p. 11	second part of the priority daisy CHAIN
CLOCK A	p. 12	Programmable clock for the line channel
CLOCK B	p. 11	Programmable clock for the printer channel
DRQ 1	p. 4	Dma REQuest 1
-, INT	p. 11 p. 3	INTerrupt request line
KEYBOARD CLOCK	p. 11	clock for the KEYBOARD channel

14.05.1981 KØN



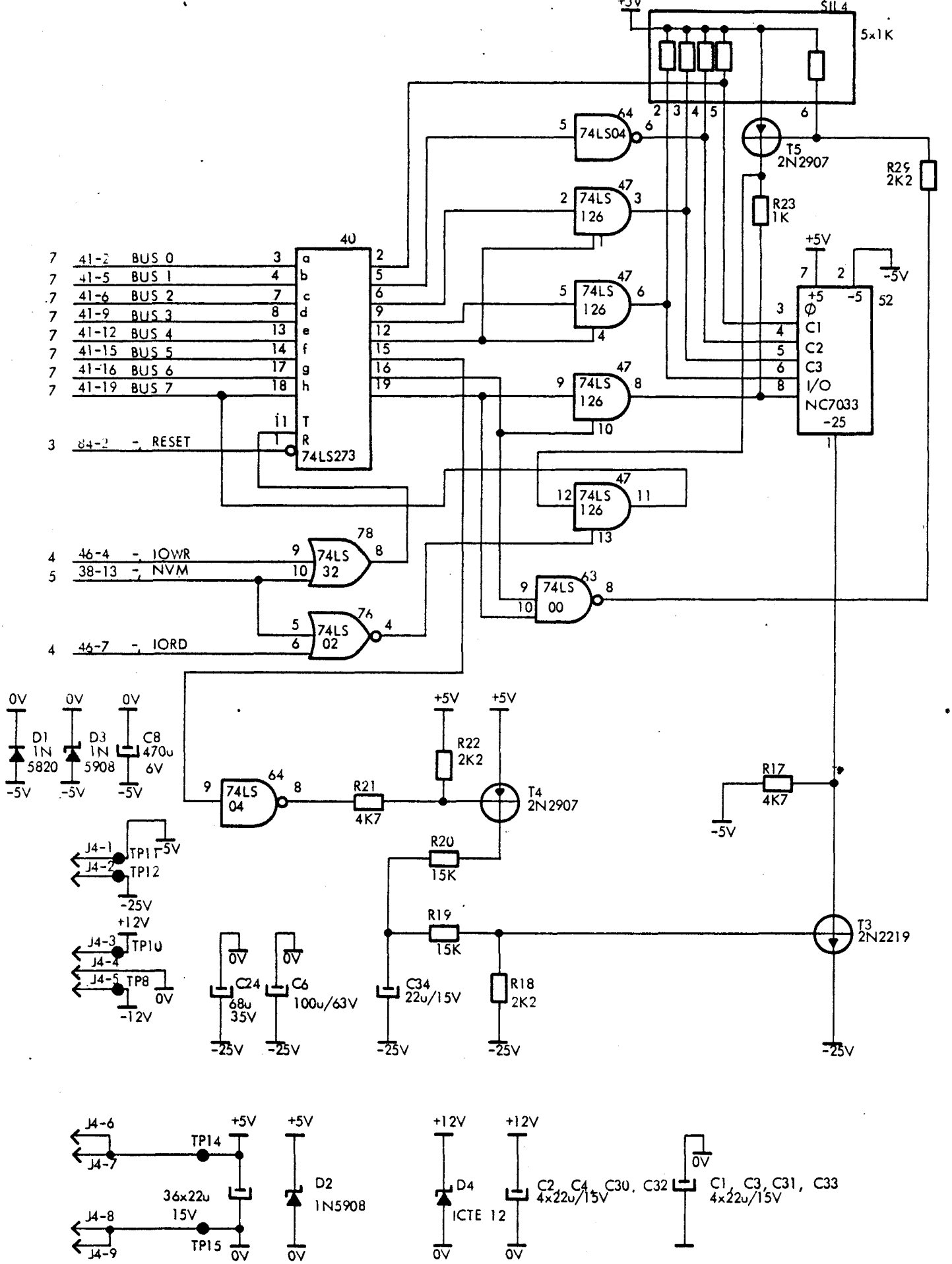
81.06.04 KØN 81.06.11 ABP

SIGNAL	DESTINATION	DESCRIPTION

Designed by

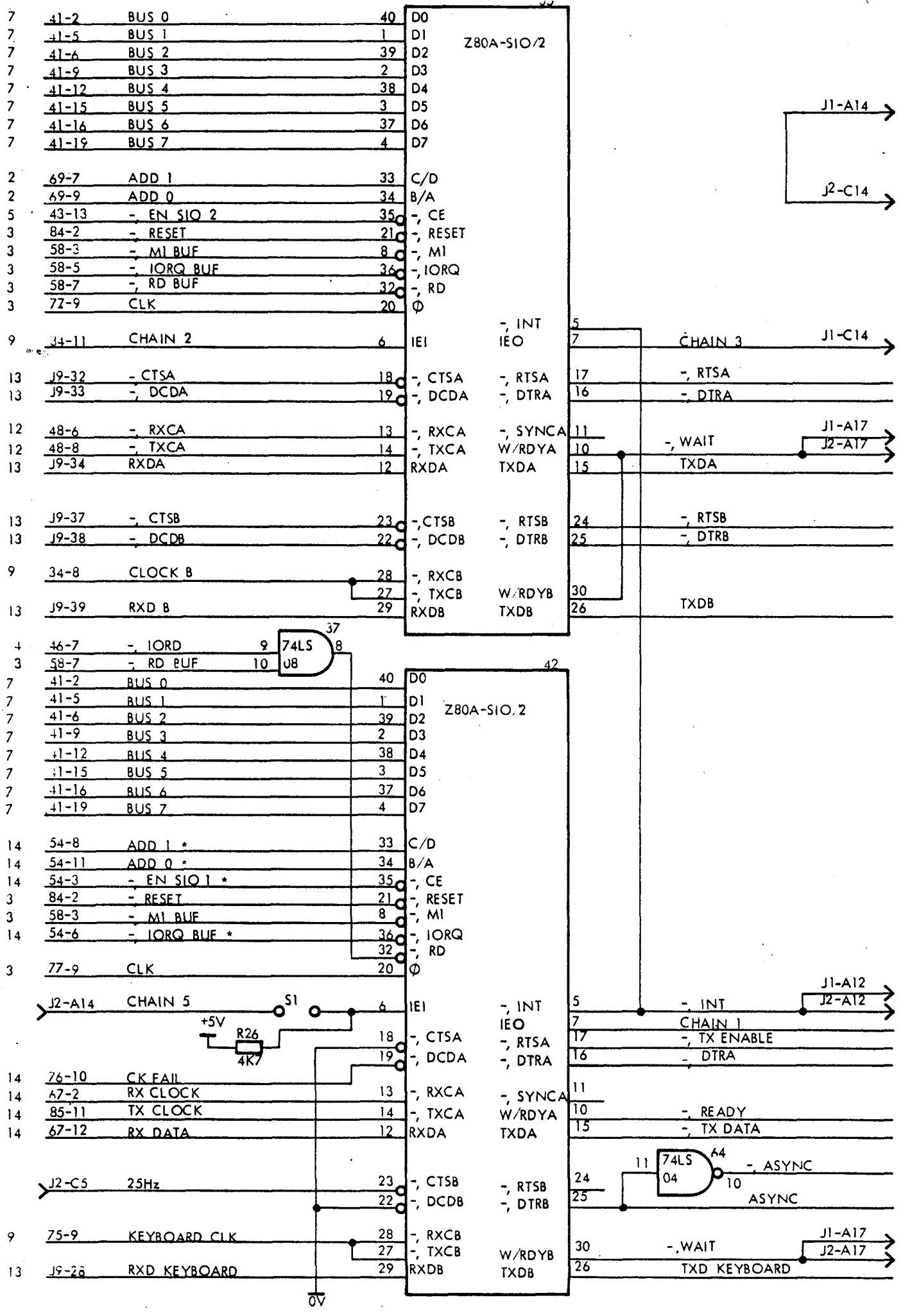
Drawn by

Office Check


SIL4
5x1K
74LS04
T5
2N2907
R29
2K2
R23
1K
74LS
126
74LS273
BUS 0
BUS 1
BUS 2
BUS 3
BUS 4
BUS 5
BUS 6
BUS 7
RESET
IOWR
NVM
IORD
74LS
32
74LS
02
74LS
00
NC7033
-25
C1
C2
C3
I/O
D1
IN
5820
D3
IN
5908
C8
470u
6V
R22
2K2
R21
4K7
T4
2N2907
R17
4K7
R20
15K
R19
15K
T3
2N2219
TP11
TP12
TP10
TP8
C24
68u
35V
C6
100u/63V
C34
22u/15V
R18
2K2
TP14
TP15
36x22u
15V
D2
1N5908
D4
ICTE 12
C2, C4, C30, C32
4x22u/15V
C1, C3, C31, C33
4x22u/15V

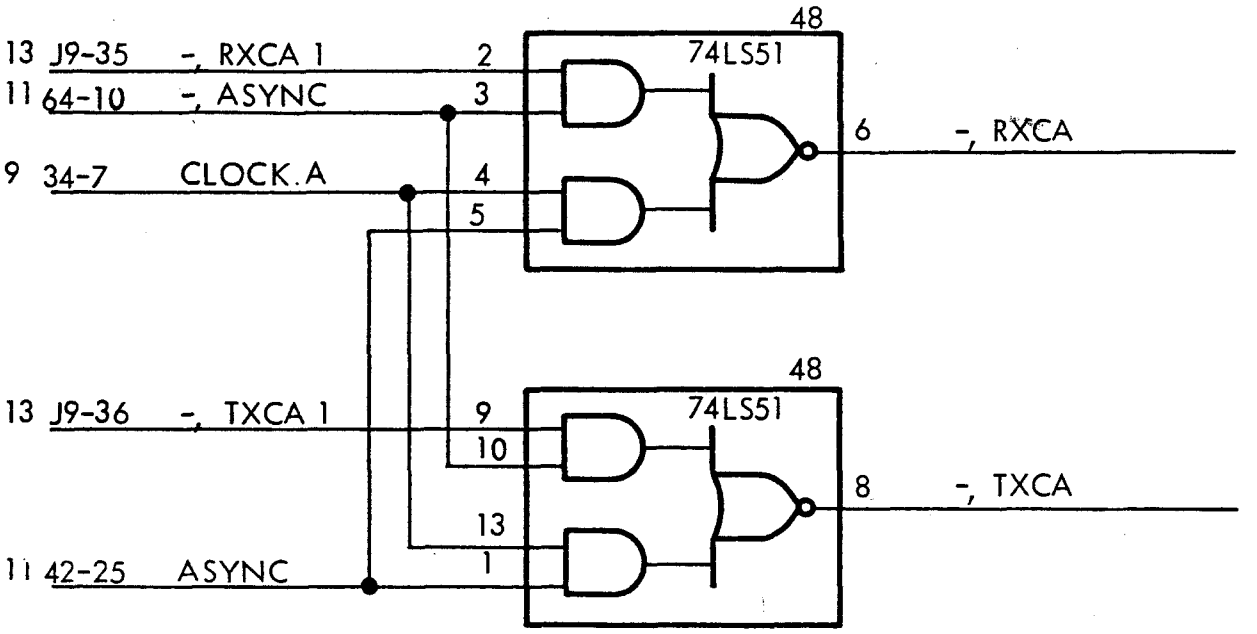
SIGNAL	DESTINATION	DESCRIPTION
ASYNC	p. 12	ASYNChronous/synchronous clock switch for the line channel
-, ASYNC	p. 12	See above
CHAIN 1	p. 9	first part of the priority daisy CHAIN
CHAIN 3		See above
-, DTRA	p. 13	Data Terminal Ready for the line channel
-, DTRA 1	p. 14	block the clock failure information from the RC-CIRCUIT channel
-, DTRB	p. 13	Data Terminal Ready for the printer channel
INT	p. 9 p. 3	INTerrupt request line
-, READY	p. 15	READY to the DMA from the RC-CIRCUIT channel
-, RTSA	p. 13	Request To Send for the line channel
-, RTSB	p. 13	Request To Send for the printer channel
TXDA	p. 13	Transmit Data to the line channel
TXDATA	p. 14	Transmit Data to the RC-CIRCUIT channel
TXDB	p. 13	Transmit Data to the printer channel
TXD KEYBOARD	p. 13	Transmit Data to the Keyboard
-, TX ENABLE	p. 13	ENABLE the Transmitter on the RC-CIRCUIT channel
-, WAIT	p. 3 p. 7 p. 8	WAIT for the CPU

14.05.1981 KØN


Z80A-SIO/2
BUS 0
BUS 1
BUS 2
BUS 3
BUS 4
BUS 5
BUS 6
BUS 7
ADD 1
ADD 0
-, EN SIO 2
-, RESET
-, M1 BUF
-, IORQ BUF
-, RD BUF
CLK
CHAIN 2
-, CTSA
-, DCDA
-, RXCA
-, TXCA
RXDA
-, CTSB
-, DCDB
CLOCK B
RXD B
-, IORD
-, RD BUF
74LS 08
Z80A-SIO/2
ADD 1 *
ADD 0 *
-, EN SIO 1 *
-, IORQ BUF *
CLK
CHAIN 5
S1
+5V
R26
4K7
CK FAIL
RX CLOCK
TX CLOCK
RX DATA
25Hz
KEYBOARD CLK
RXD KEYBOARD
0V
-, INT
CHAIN 3
-, RTSA
-, DTRA
-, WAIT
TXDA
-, RTSB
-, DTRB
TXDB
J1-A14
J2-C14
J1-C14
J1-A17
J2-A17
J1-A12
J2-A12
CHAIN 1
-, TX ENABLE
-, READY
-, TX DATA
74LS 04
-, ASYNC
ASYNC
TXD KEYBOARD

SIGNAL	DESTINATION	DESCRIPTION
-, RXCA	p. 11	Receiver Clock for the line channel
-, TXCA	p. 11	Transmitter Clock for the line channel

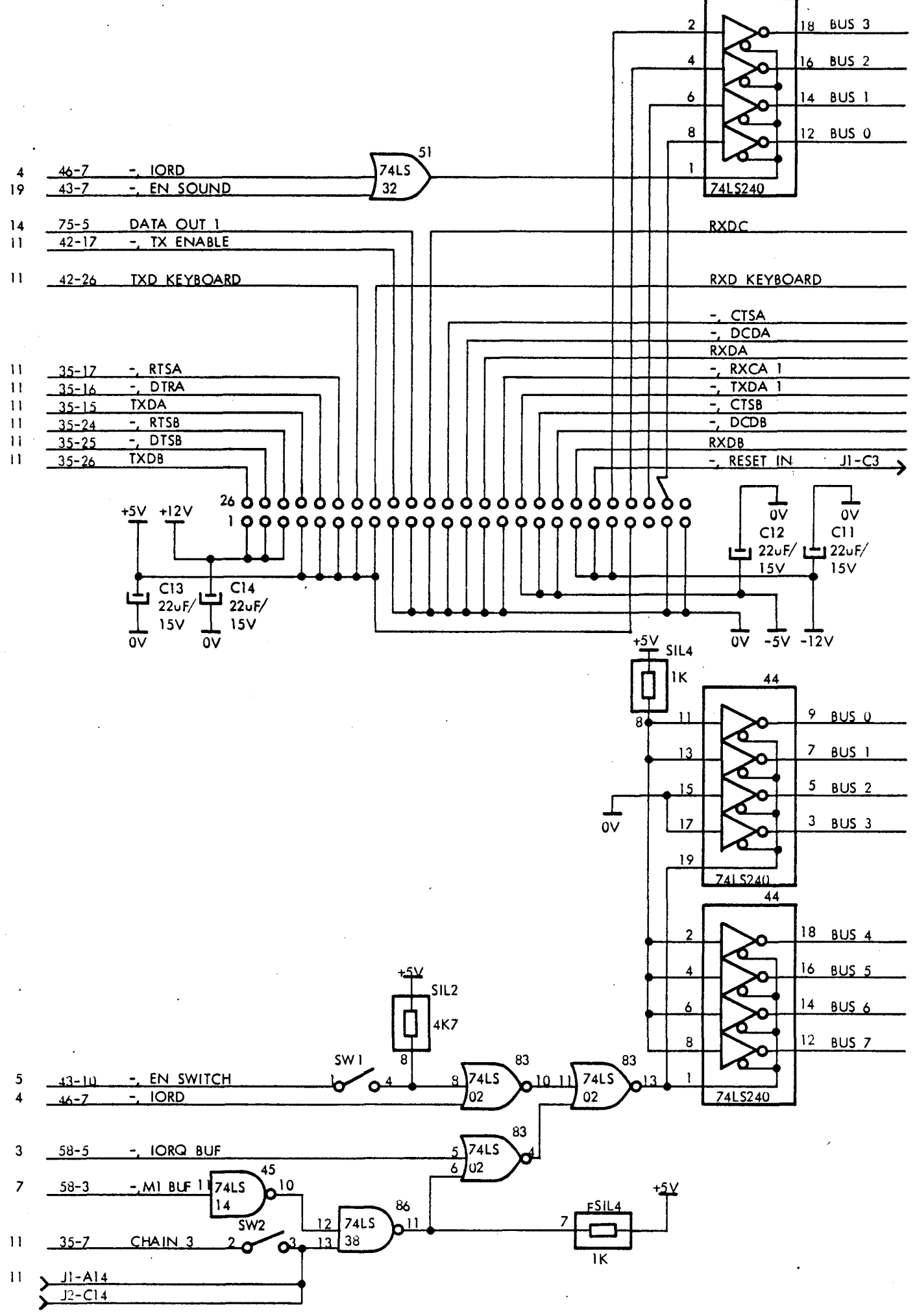
14.05.1981 KØN



81.06.04 KØN81.06.04 ABP

SIGNAL	DESTINATION	DESCRIPTION
BUS 0-7	p. 2 p. 4 p. 6 p. 7 p. 9 p. 10 p. 11	Data BUS bit 0-7
-, CTS A	p. 11	Clear To Send from the line channel
-, CTS B	p. 11	Clear To Send from the printer channel
-, DCD A	p. 11	Data Carrier Detected from the line channel
-, DCD B	p. 11	Data Carrier Detected from the printer channel
-, RESET IN	p. 3	Signal from the RESET switch
RXCA 1	p. 12	Receiver Clock from the line channel
RXDA	p. 11	Receive Data from the line channel
RXDB	p. 11	Receive Data from the printer channel
RXDC	p. 14	Receive Data from the Circuit channel
RXD KEYBOARD	p. 11	Receive Data from the KEYBOARD
TXCA 1	p. 12	Transmitter Clock from the line channel

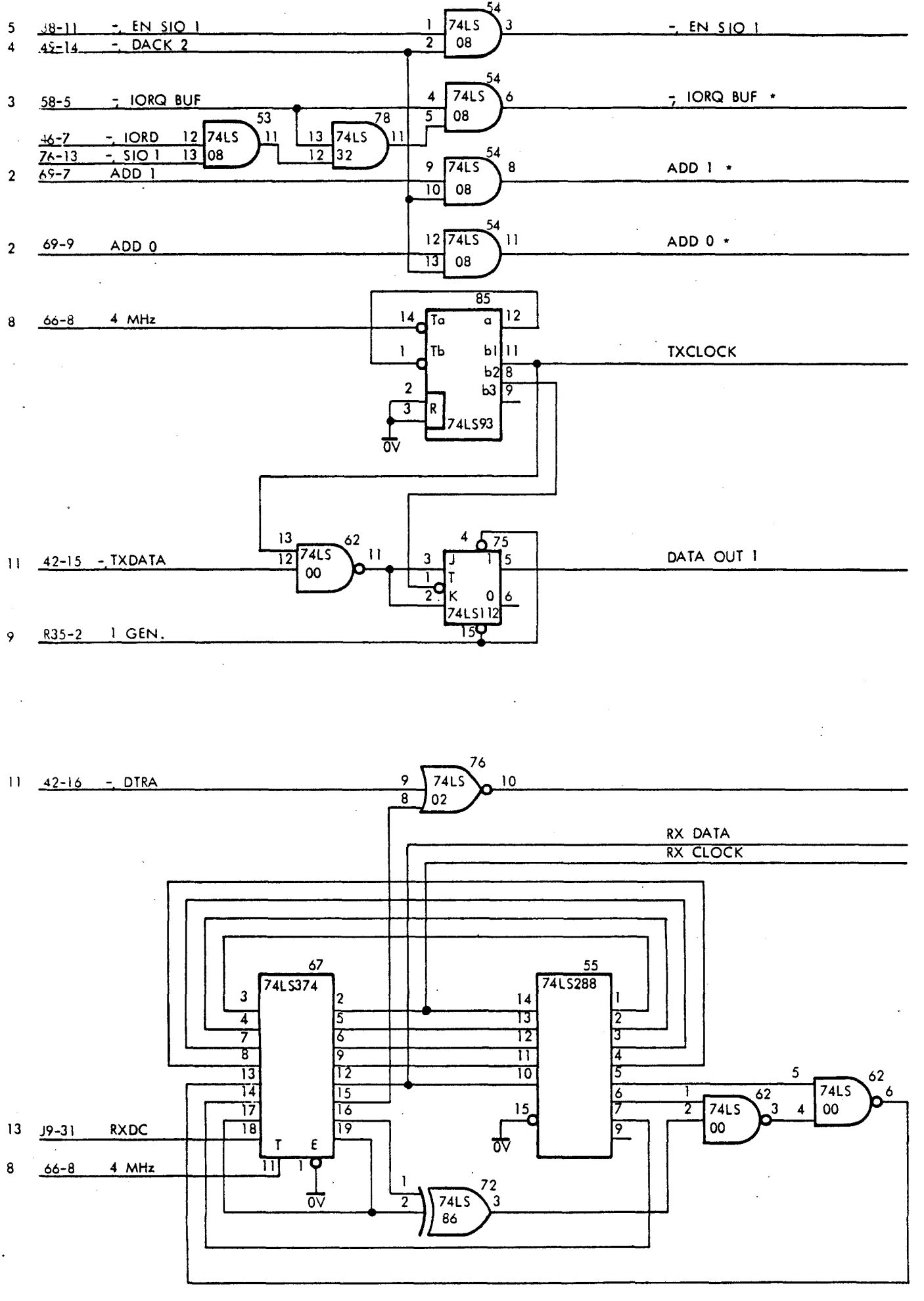
15.05.1981 KØN



81.06.04 KØN 81.06.11ABP

SIGNAL	DESTINATION	DESCRIPTION
ADD 0-1 *	p. 11	ADDress bit 0-1
CK FAIL	p. 11	ClocK FAILure from the RC-CIRCUIT channel
DATA OUT 1	p. 13	DATA OUT to the RC-CIRCUIT channel
¬, EN SIO *	p. 11	ENable Serial Input/Output
¬, IORQ BUF *	p. 11	Input/Output ReQuest BUFfered
RX CLOCK	p. 11	Receive CLOCK from the RC-CIRCUIT channel
RX DATA	p. 11	Receive DATA from the RC-CIRCUIT channel
TX CLOCK	p. 11	Transmit CLOCK for the RC-CIRCUIT channel

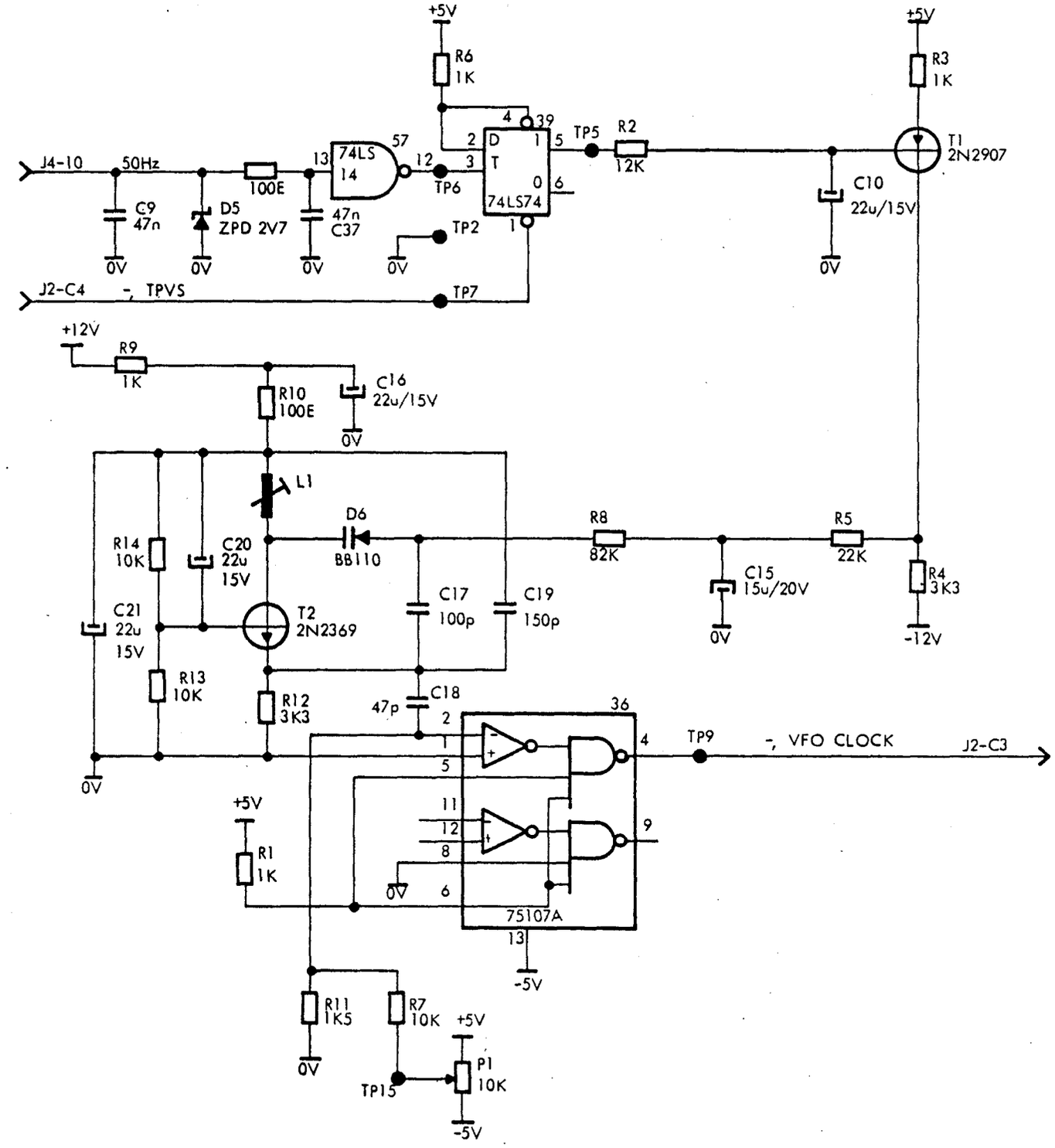
14.05.1981 KØN



81.06.04 KØN 81.06.11 ABP

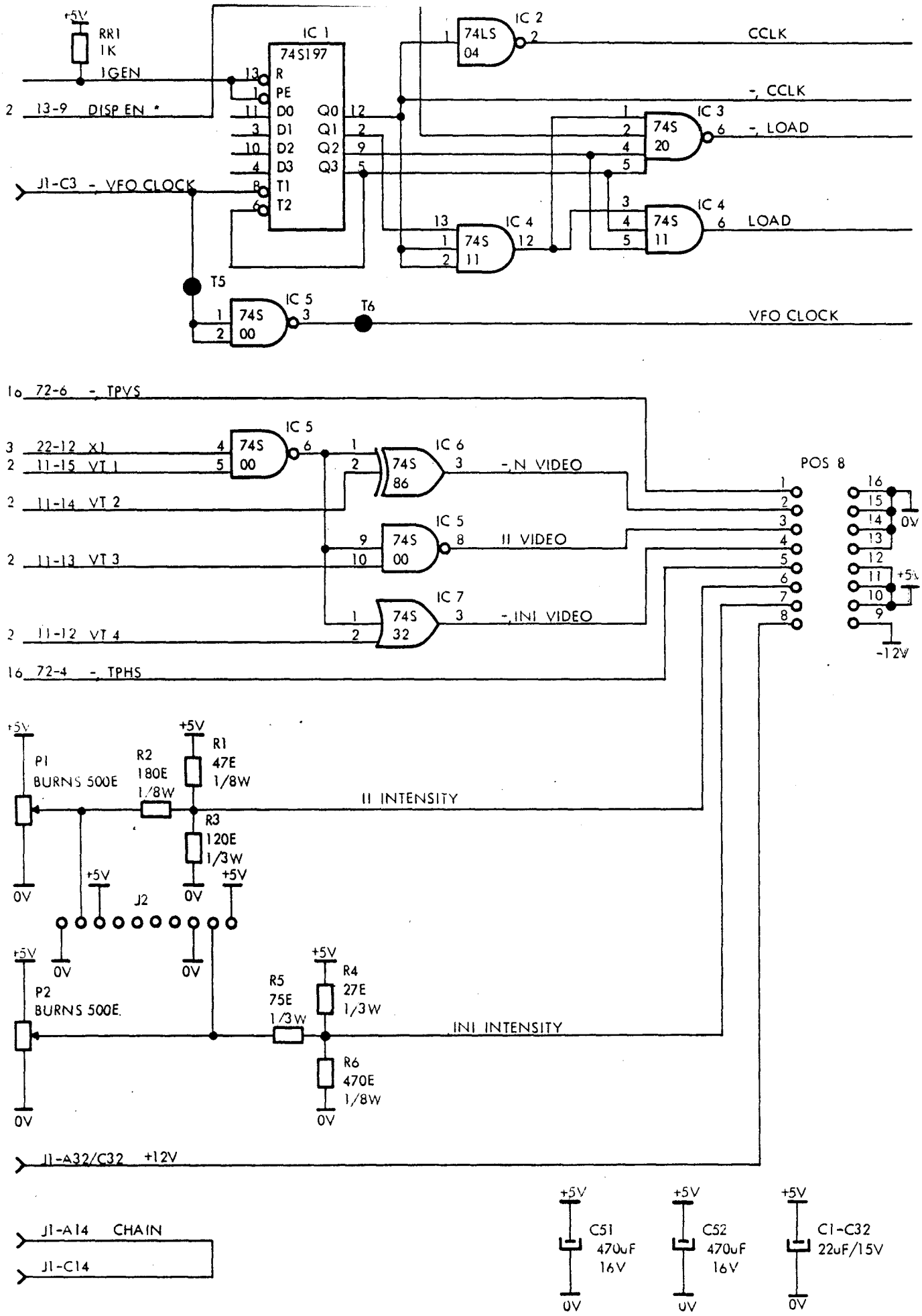
SIGNAL	DESTINATION	DESCRIPTION
DRQ 2		DMA ReQuest from the RC-Circuit channel
⁻, VFO CLOCK		Variable Frequency Oscillator CLOCK for the display controller for picture phase-lock to the mains

14.05.1981 KØN



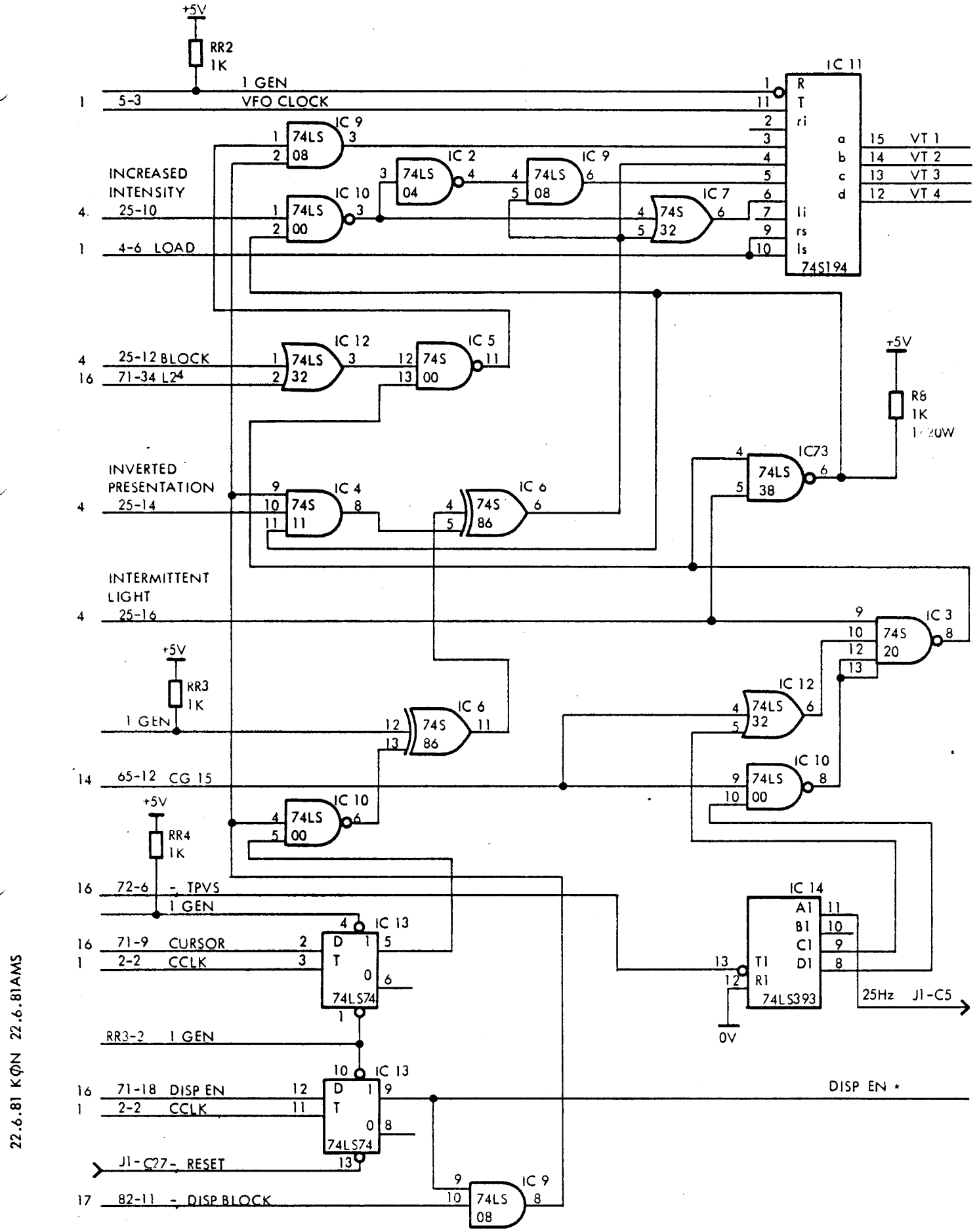
81.06.04 KØN 81.06.11 ABP

SIGNAL	DESTINATION	DESCRIPTION
CCLK	p. 2 p. 11	Character CLocK
-, CCLK	p. 10 p. 16	See above
LOAD	p. 2	LOAD of the dot register
-, LOAD	p. 3	See above
VFO CLOCK	p. 2 p. 3	Variable Frequency Oscillator CLOCK
II INTENSITY		Increased Inverted INTENSITY
II VIDEO		Increased Inverted Video
INI INTENSITY		Increased Not Inverted INTENSITY
-, INI VIDEO		Increased Not Inverted VIDEO
-, N VIDEO		Normal VIDEO



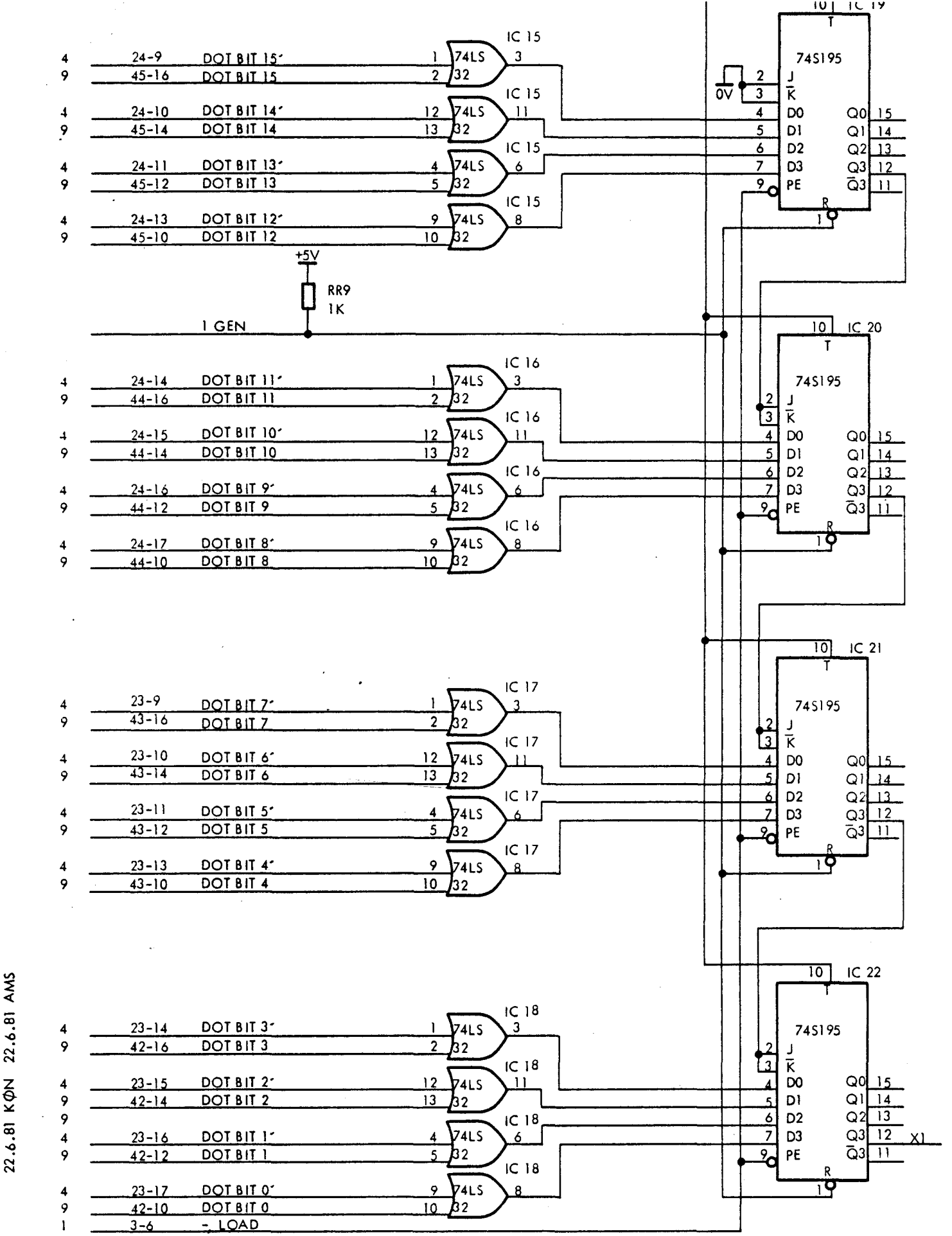
22.6.81KØN 22.6.81AMS

SIGNAL	DESTINATION	DESCRIPTION
DISP EN *	p. 10	DISPlay ENable
25Hz		25Hz clock signal
VT 1-4	p. 1	Video Timing 1-4



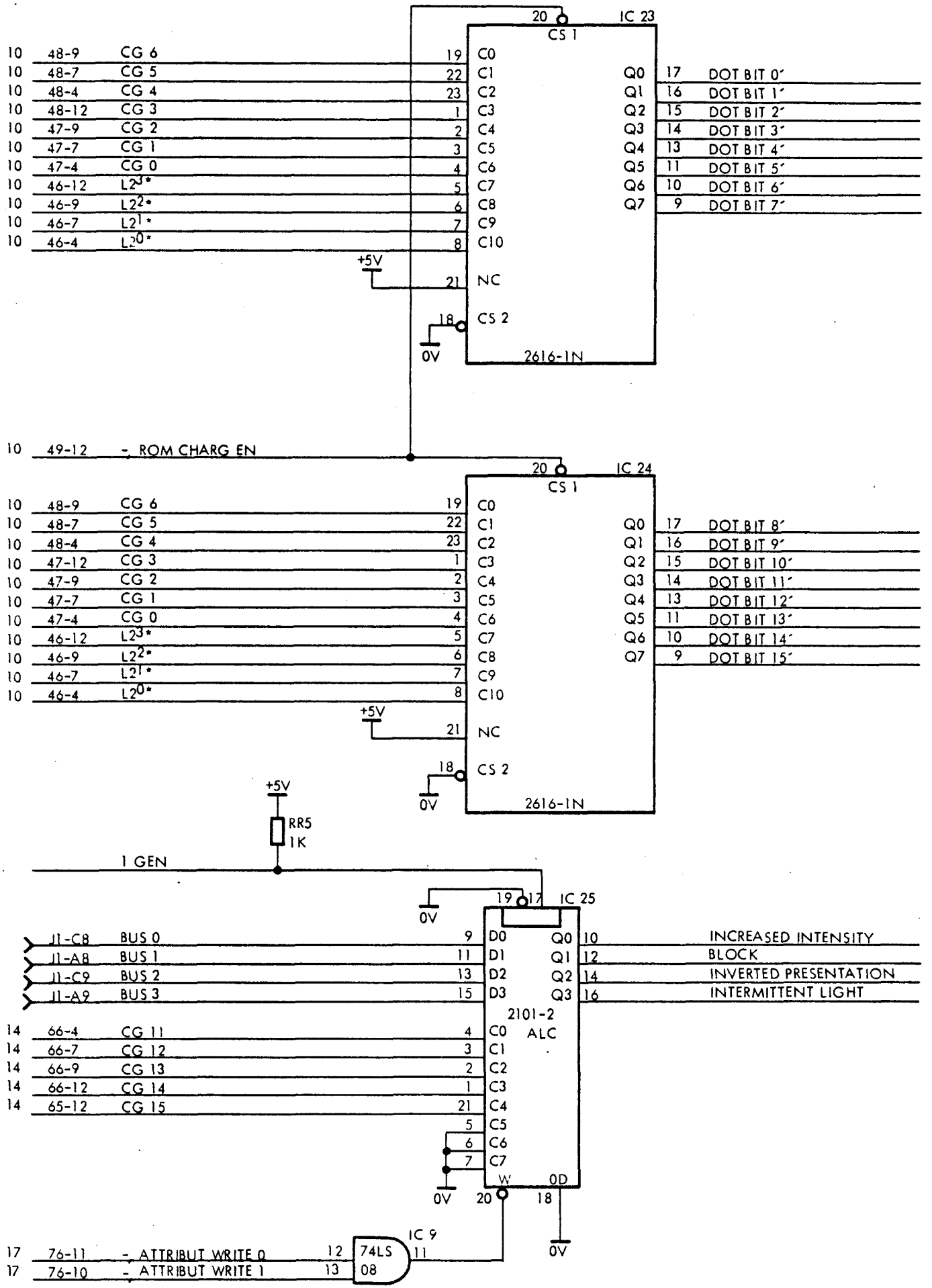
22.6.81 KØN 22.6.81AMS

SIGNAL	DESTINATION	DESCRIPTION
X1	p. 1	Video output



22.6.81 KØN 22.6.81 AMS

SIGNAL	DESTINATION	DESCRIPTION
BLOCK	p. 2	BLOCKing of the video signal
DOT BIT 0´-3´	p. 5 p. 9 p. 18	BIT number 0-3 in the video DOT register
DOT BIT 4´-7´	p. 6 p. 9 p. 18	See above
DOT BIT 8´-11´	p. 7 p. 9 p. 18	See above
DOT BIT 12´-15´	p. 8 p. 9 p. 18	See above
INCREASED INTENSITY	p. 2	Causes the video to be shown with INCREASED INTENSITY
INTERMITTENT LIGHT	p. 2	Causes the video to be shown with INTERMITTENT LIGHT
INVERTED PRESENTATION	p. 2	Causes the video to be shown with INVERTED PRESENTATION



22.6.81 KØN 22.6.81 AMS

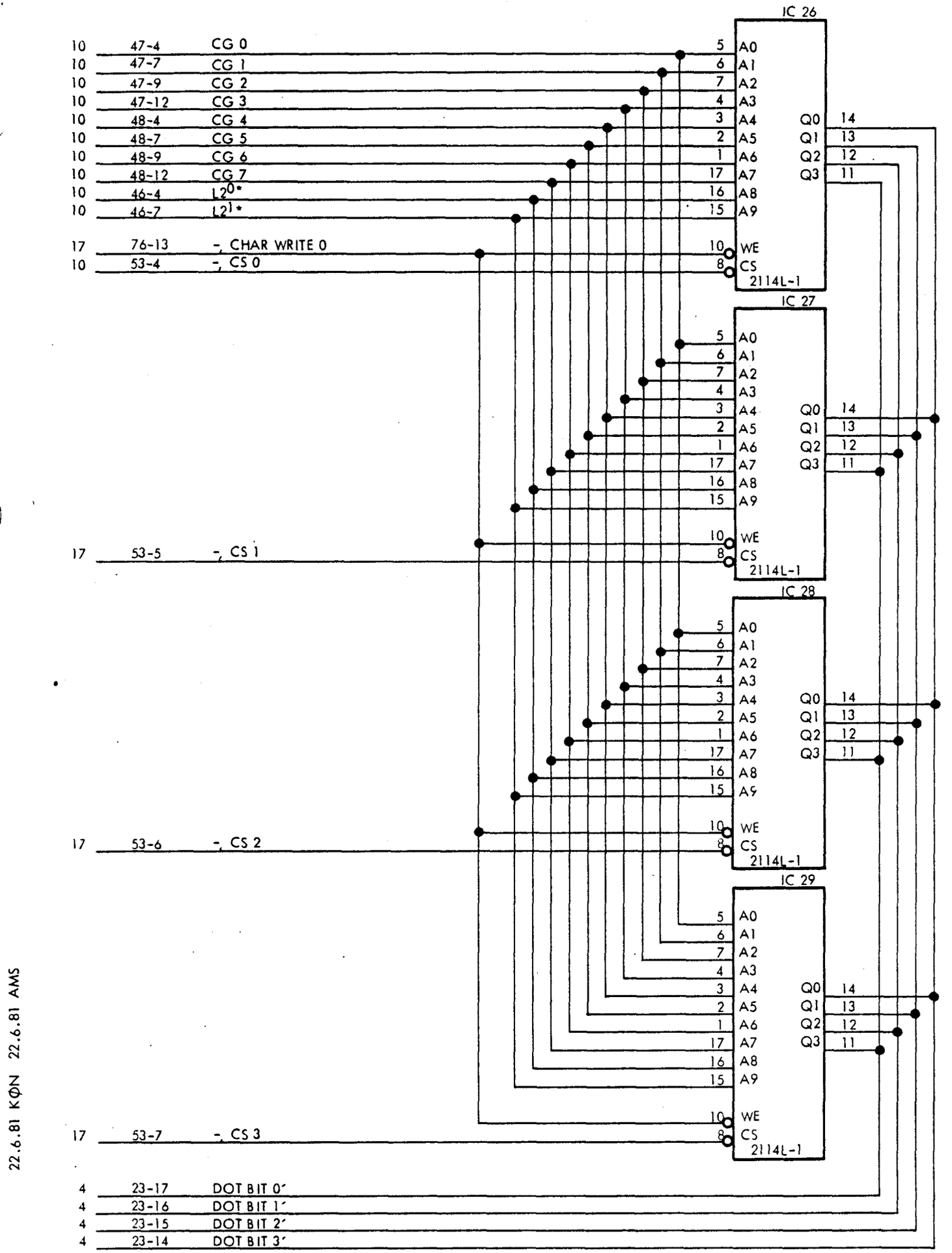
SIGNAL	DESTINATION	DESCRIPTION

Designed by

Drawn by

D

Office Check



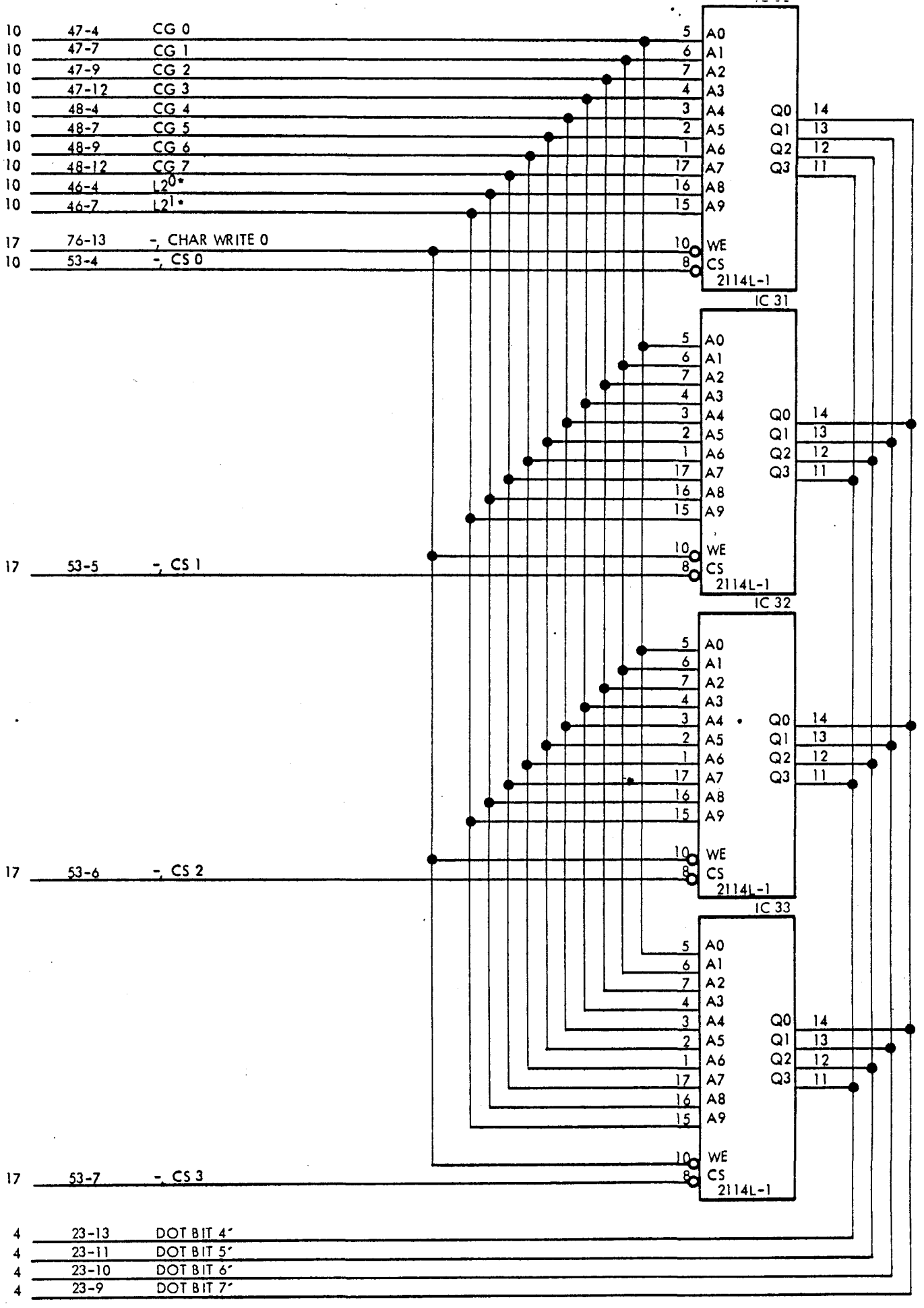
22.6.81 KØN 22.6.81 AMS

SIGNAL	DESTINATION	DESCRIPTION

Designed by

Drawn by

Office Check


10 47-4 CG 0
10 47-7 CG 1
10 47-9 CG 2
10 47-12 CG 3
10 48-4 CG 4
10 48-7 CG 5
10 48-9 CG 6
10 48-12 CG 7
10 46-4 L2 0*
10 46-7 L2 1*
17 76-13 -, CHAR WRITE 0
10 53-4 -, CS 0
17 53-5 -, CS 1
17 53-6 -, CS 2
17 53-7 -, CS 3
4 23-13 DOT BIT 4'
4 23-11 DOT BIT 5'
4 23-10 DOT BIT 6'
4 23-9 DOT BIT 7'
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9
WE CS
Q0 Q1 Q2 Q3
2114L-1
IC 31
IC 32
IC 33
22.6.81 KØN 22.6.81 AMS

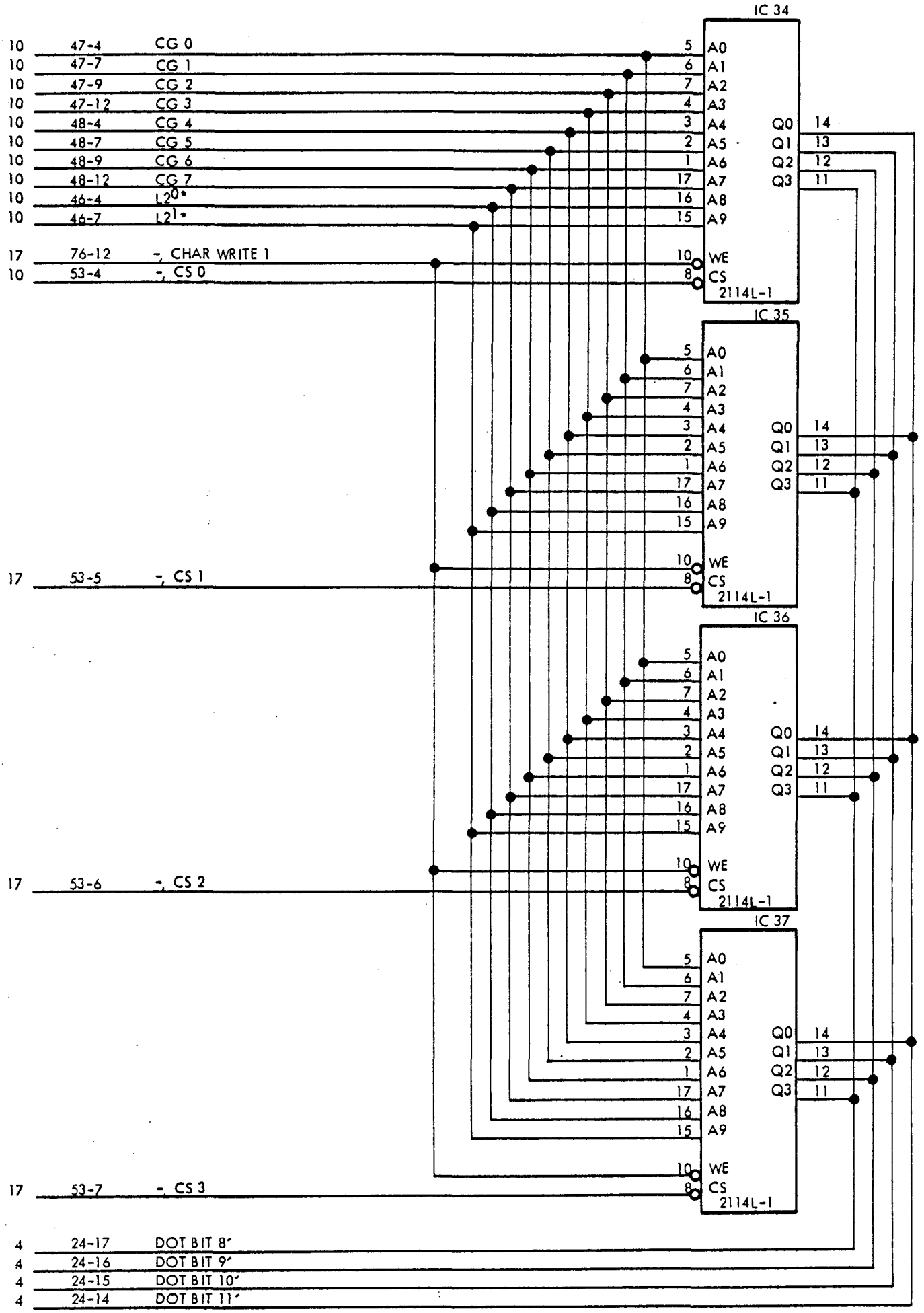
SIGNAL	DESTINATION	DESCRIPTION

Designed by

Drawn by

D·

Office Check

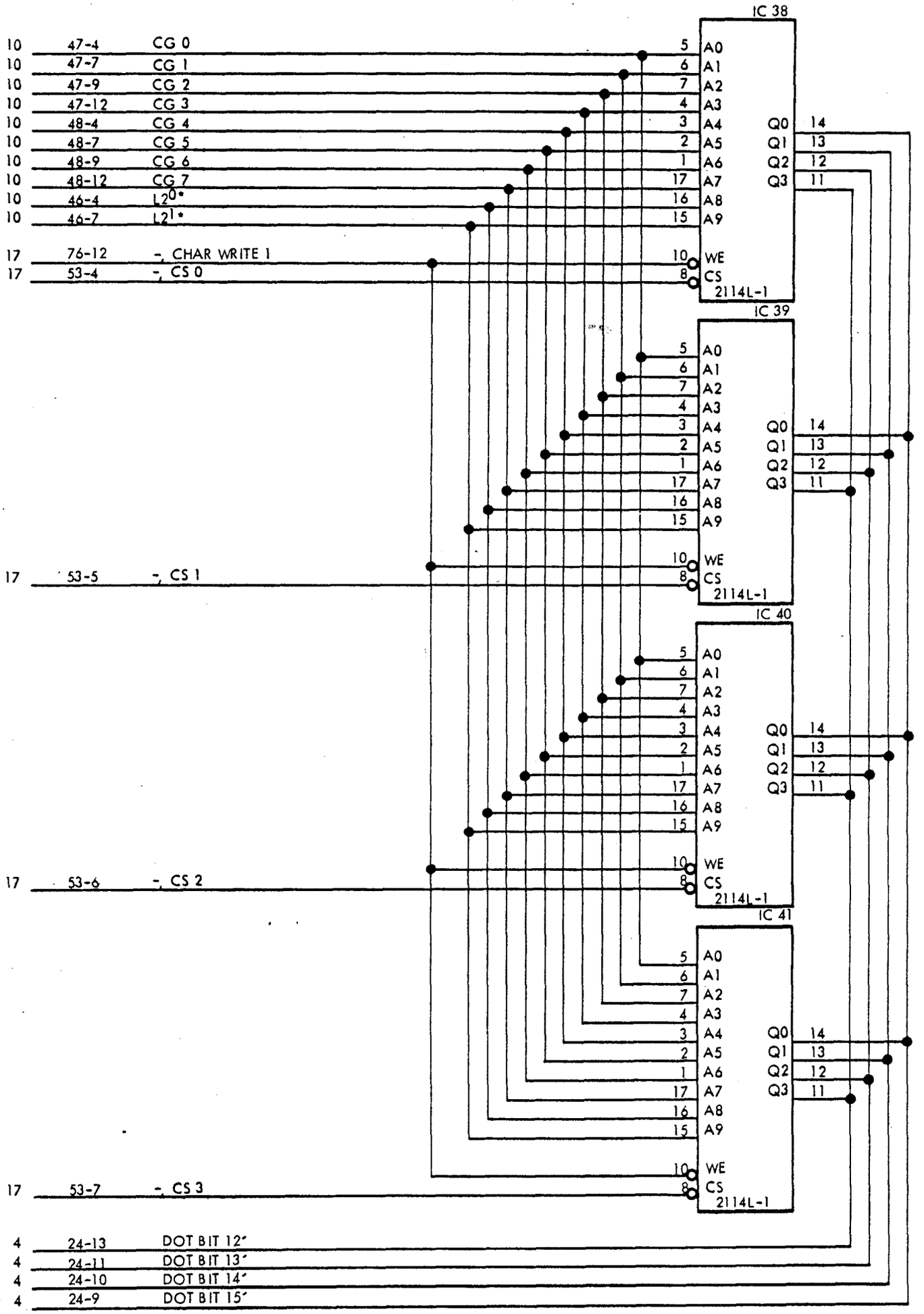

IC 34
IC 35
IC 36
IC 37
2114L-1
10 47-4 CG 0
10 47-7 CG 1
10 47-9 CG 2
10 47-12 CG 3
10 48-4 CG 4
10 48-7 CG 5
10 48-9 CG 6
10 48-12 CG 7
10 46-4 L2⁰*
10 46-7 L2¹*
17 76-12 -, CHAR WRITE 1
10 53-4 -, CS 0
17 53-5 -, CS 1
17 53-6 -, CS 2
17 53-7 -, CS 3
4 24-17 DOT BIT 8'
4 24-16 DOT BIT 9'
4 24-15 DOT BIT 10'
4 24-14 DOT BIT 11'
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9
WE CS
Q0 Q1 Q2 Q3
22.6.81 KØN 22.6.81 AMS

SIGNAL	DESTINATION	DESCRIPTION

Designed by

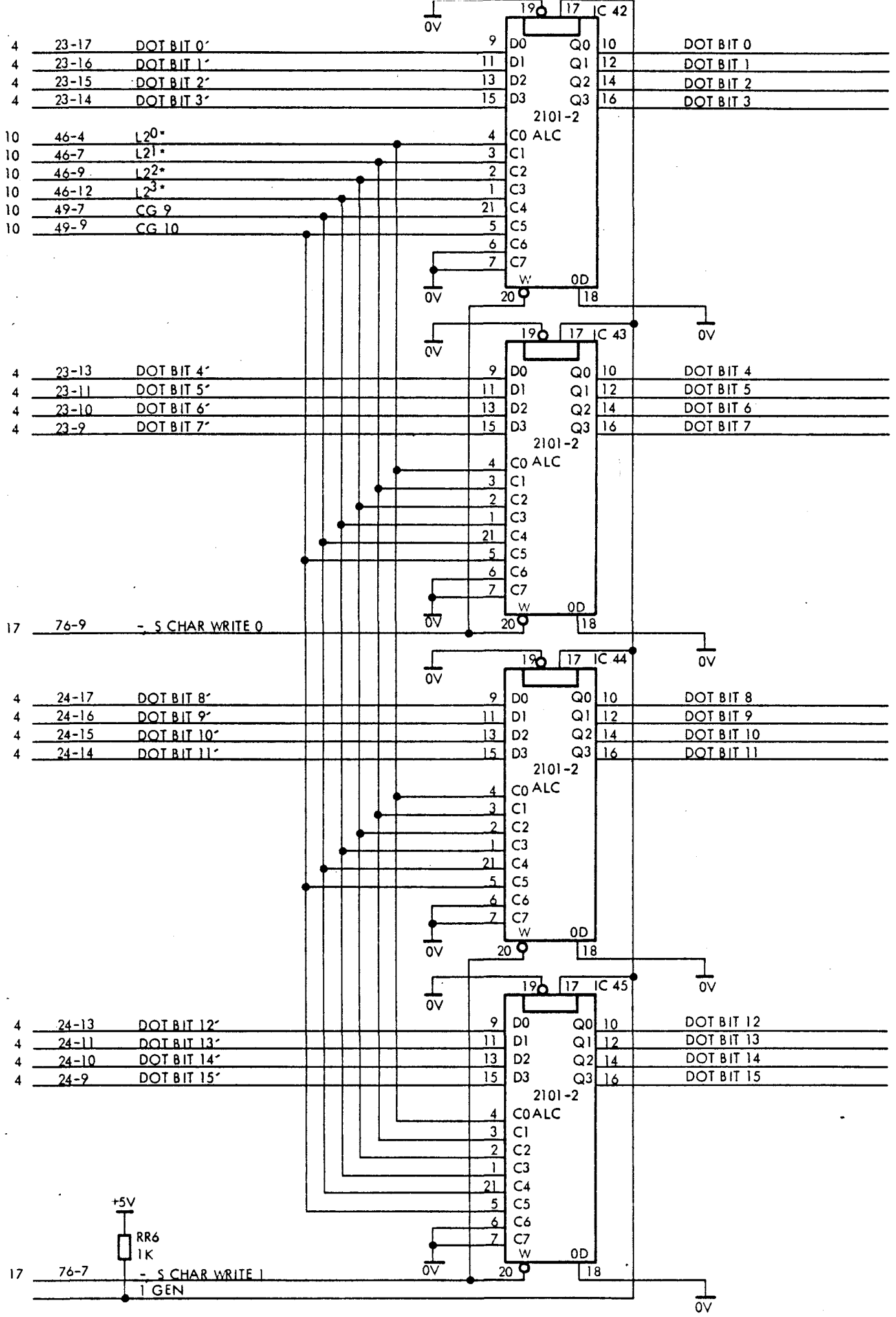
Drawn by

Dwg. Office Check



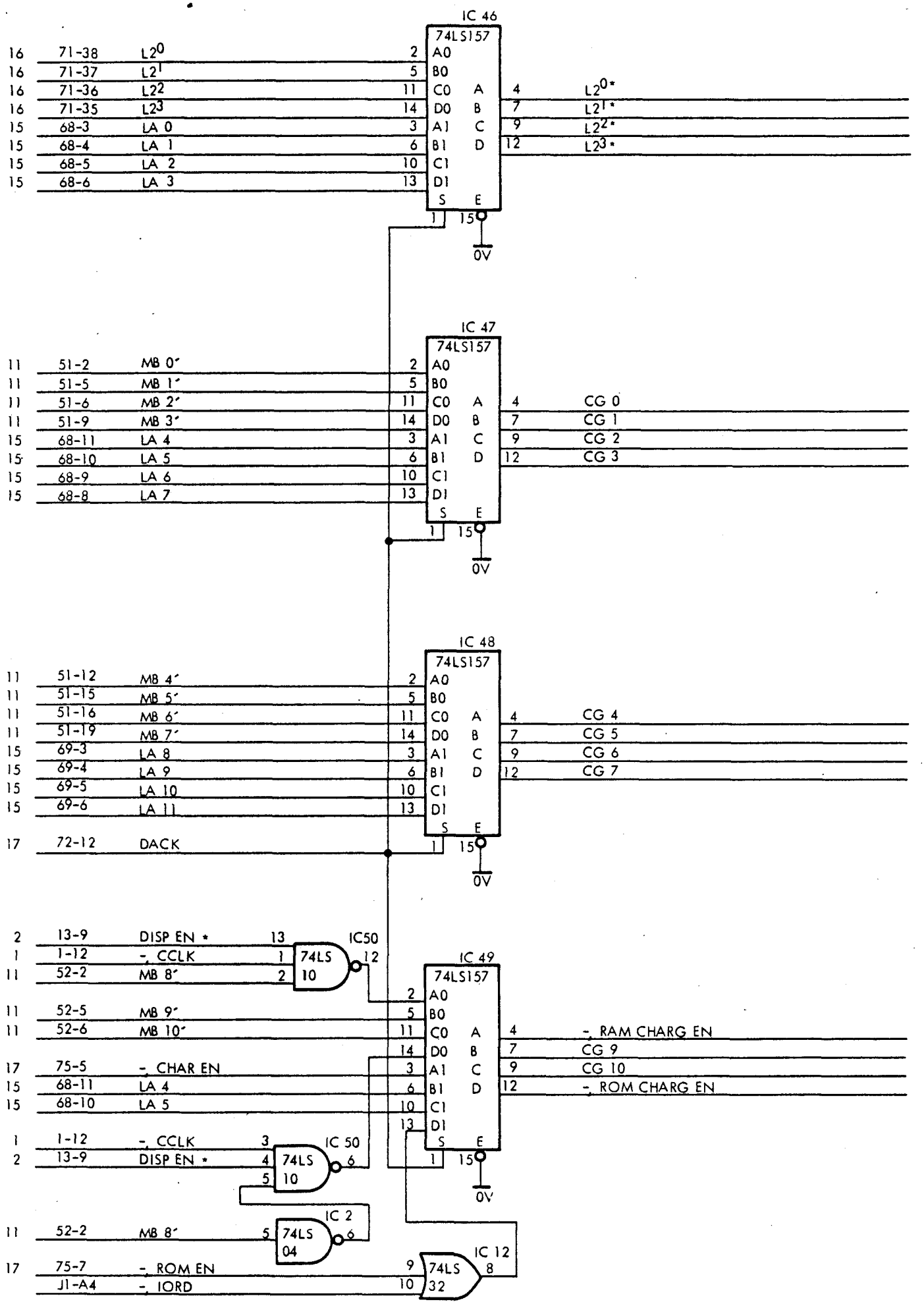
22.6.81 KØN 22.6.81 AMS

SIGNAL	DESTINATION	DESCRIPTION
DOT BIT 0-15	p. 3	BIT number 0-15 from the shadow character generator to the video DOT register.



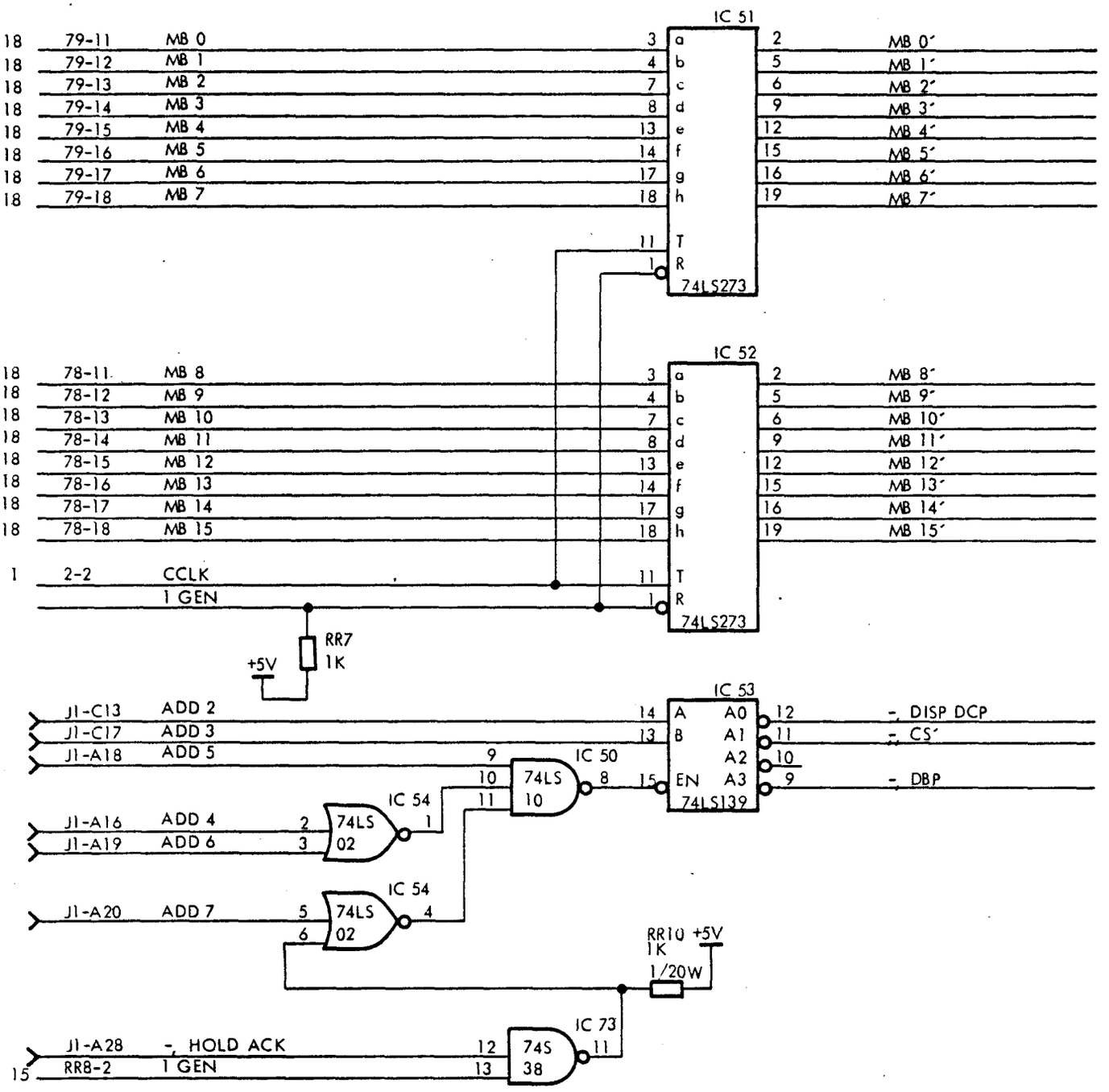
22.6.81 KØN 22.6.81 AMS

SIGNAL	DESTINATION	DESCRIPTION
CG 0-6	p. 4 p. 5 p. 6 p. 7 p. 8	Character Generator address bit 0-6
CG 7	p. 5 p. 6 p. 7 p. 8	See above
CG 9-10	p. 9	See above
$L2^{0-1}$ *	p. 4 p. 5 p. 6 p. 7 p. 8	Line address for the character generator
$L2^{3-4}$ *	p. 4 p. 17	See above
-, RAM CHARG EN	p. 4	This signal ENables the RAM CHARacter Generator
-, ROM CHARG EN	p. 17	This signal ENables the ROM CHARacter Generator



22.6.81 KØN 22.6.81 AMS

SIGNAL	DESTINATION	DESCRIPTION
-, CS	p. 16	The Chip Select line selects the CRT controller for programming
-, DBP	p. 17	Display Block Port
-, DISP DCP	p. 17	DISPlay Direction Control Port
MB 0'-10'	p. 10	Refresh Memory output Bit 0-10
MB 11'-15'	p. 14	See above



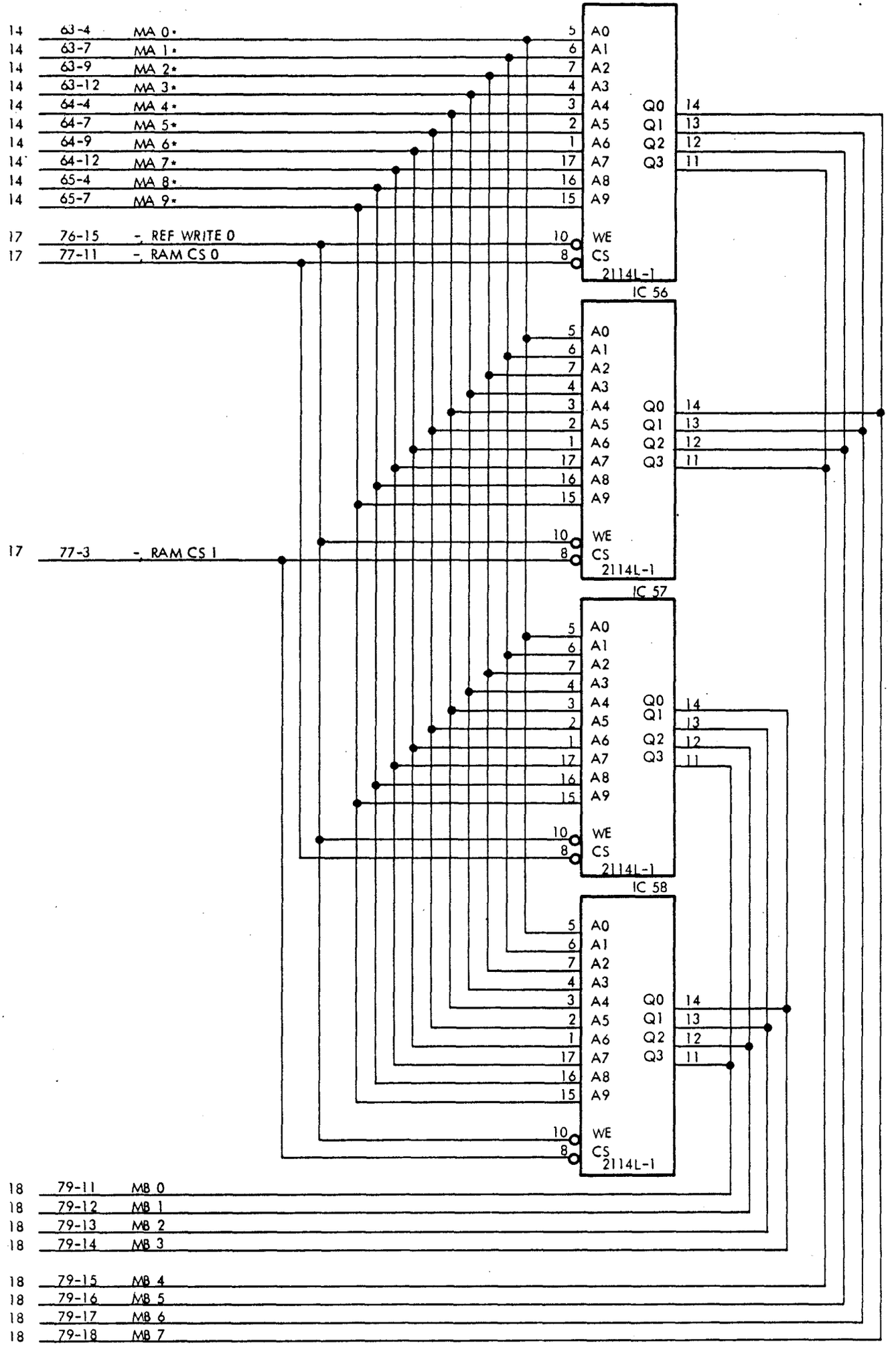
22.6.81 KØN 22.6.81 AMS

SIGNAL	DESTINATION	DESCRIPTION

Designed by

Drawn by

Office Check



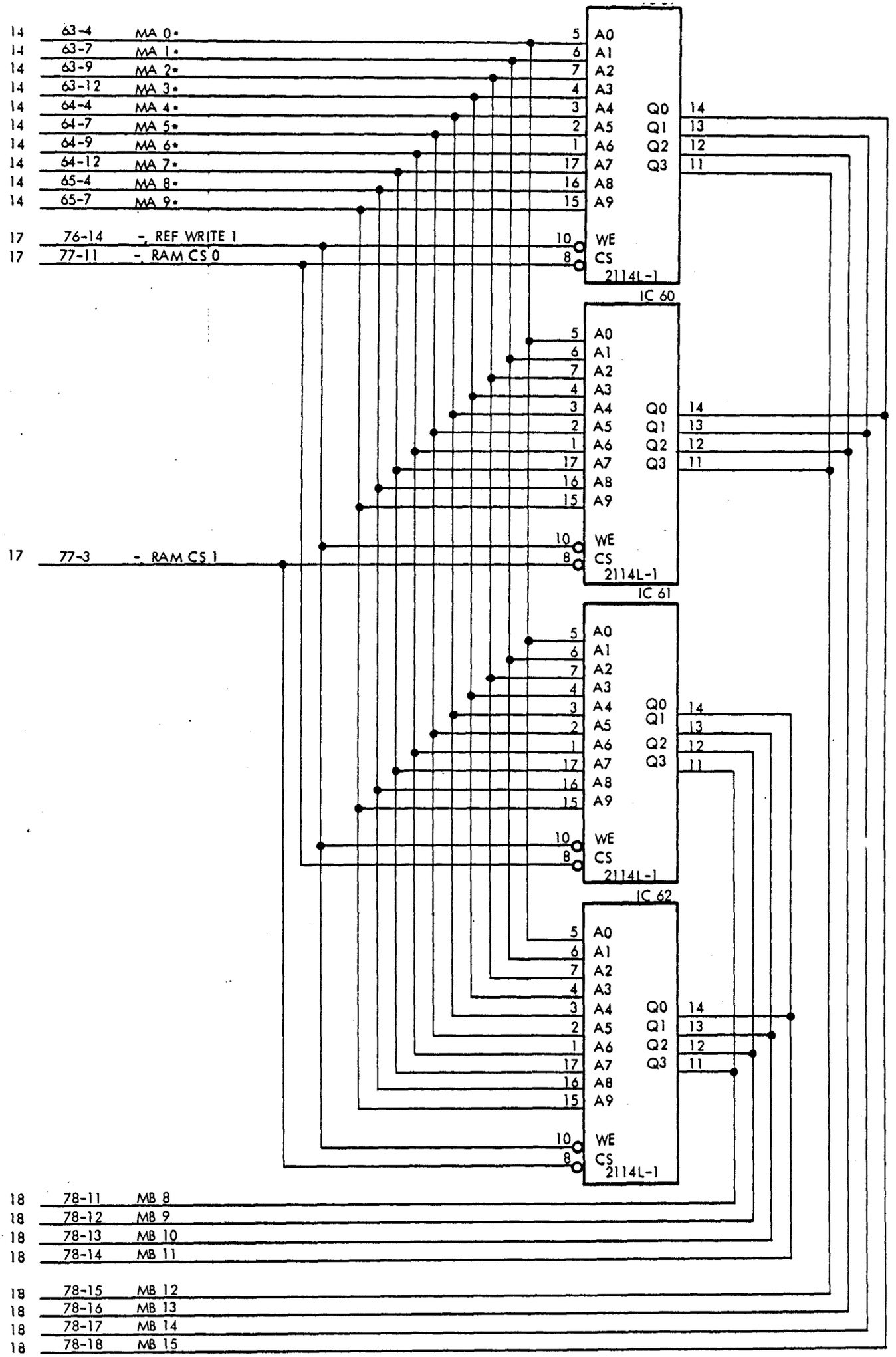
22.6.81 KΦN 22,6.81 AMS

SIGNAL	DESTINATION	DESCRIPTION

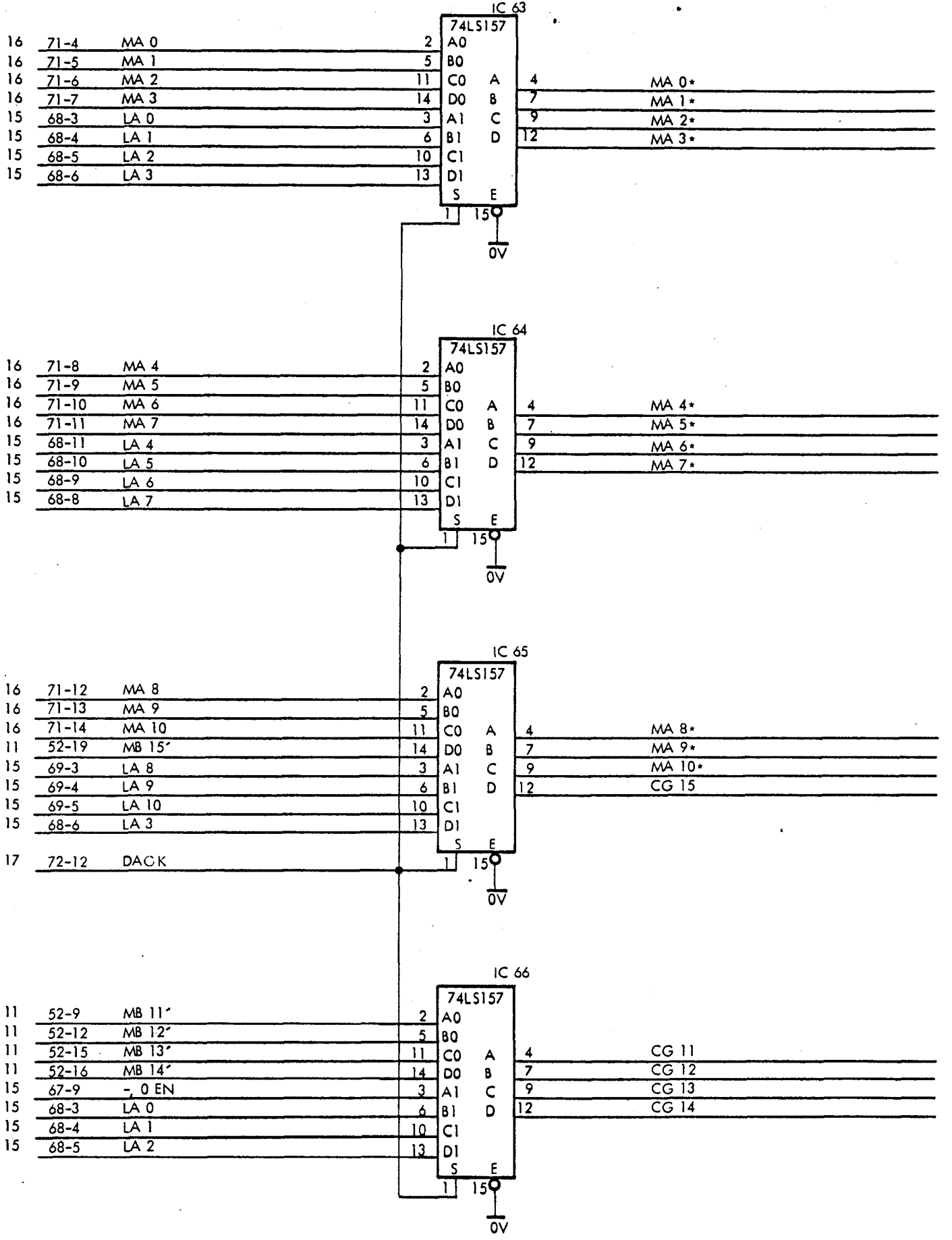
Designed by

Drawn by

D Office Check

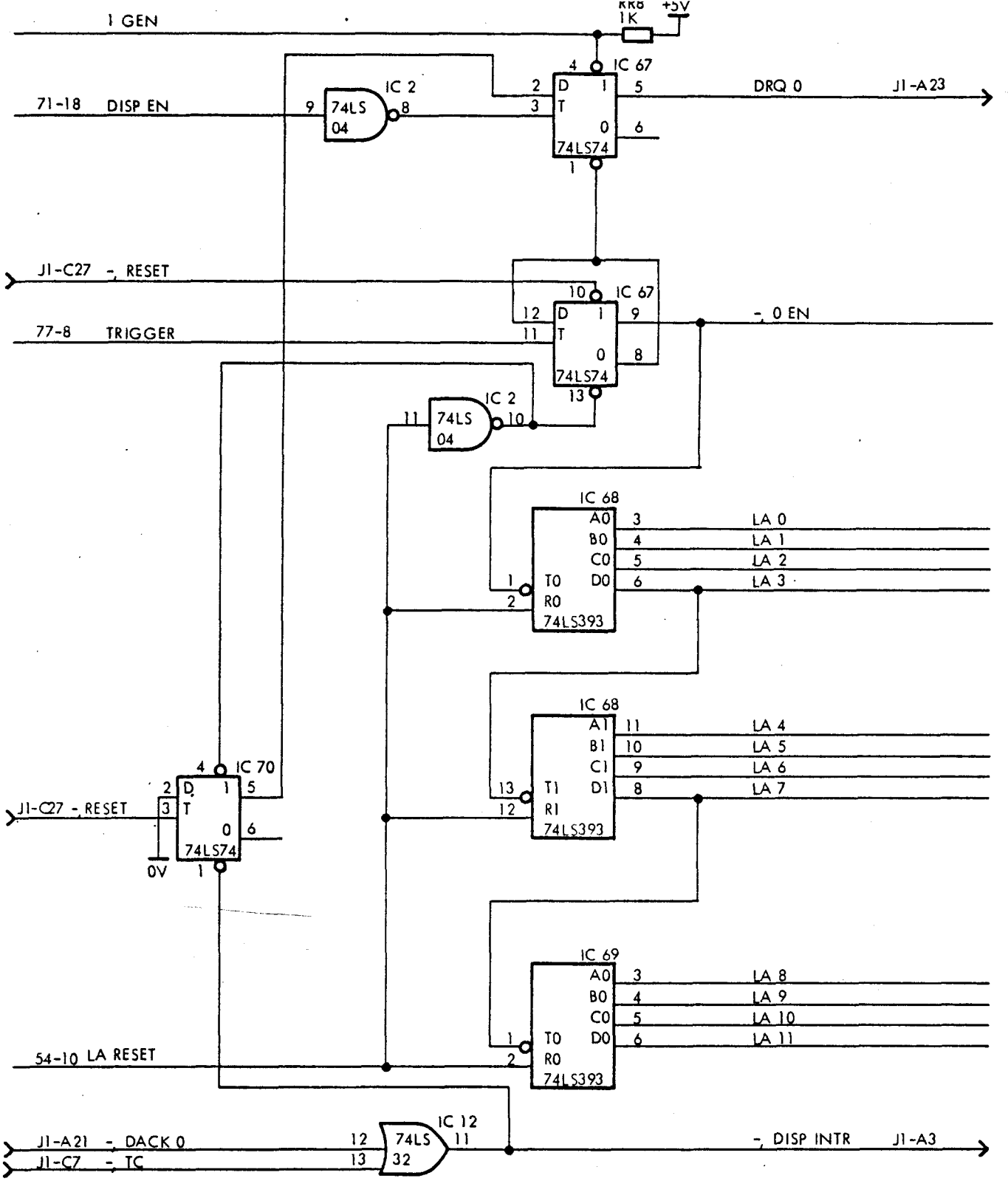

14 63-4 MA 0•
14 63-7 MA 1•
14 63-9 MA 2•
14 63-12 MA 3•
14 64-4 MA 4•
14 64-7 MA 5•
14 64-9 MA 6•
14 64-12 MA 7•
14 65-4 MA 8•
14 65-7 MA 9•
17 76-14 -, REF WRITE 1
17 77-11 -, RAM CS 0
17 77-3 -, RAM CS 1
IC 60
IC 61
IC 62
2114L-1
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
WE
CS
Q0
Q1
Q2
Q3
18 78-11 MB 8
18 78-12 MB 9
18 78-13 MB 10
18 78-14 MB 11
18 78-15 MB 12
18 78-16 MB 13
18 78-17 MB 14
18 78-18 MB 15
22.6.81 KØN
22.6.81 AMS

SIGNAL	DESTINATION	DESCRIPTION
CG 11-15	p. 4	Character Generator address bit 11-15
MA 0*-9*	p. 12 p. 13	Refresh Memory Address bit 0-9
MA 10*	p. 17	See above



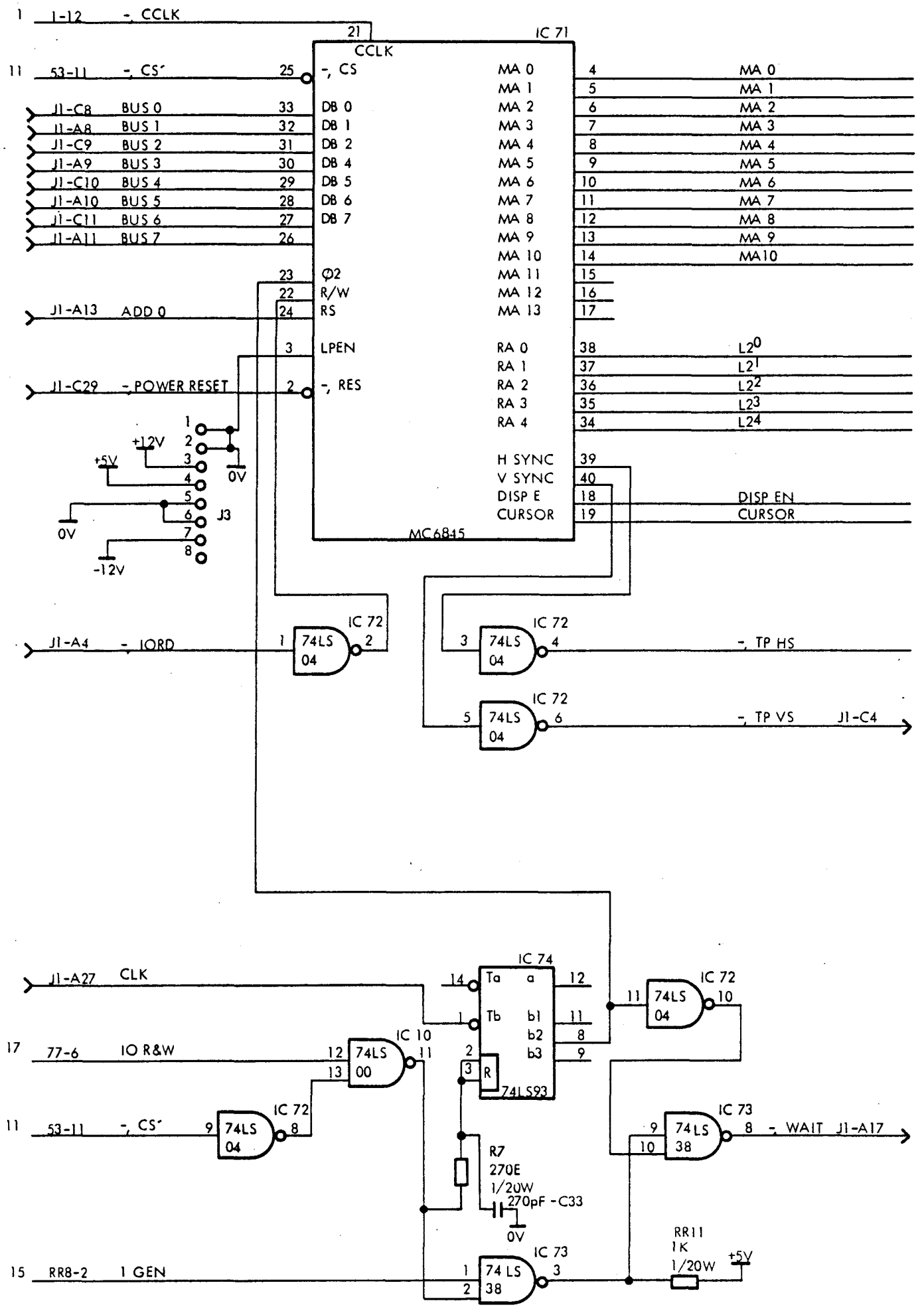
22.6.81 KØN 22.6.81 AMS

SIGNAL	DESTINATION	DESCRIPTION
-, DISP INTR		DISPlay INTerRupt
DRQ 0		DMA channel 0 ReQuest
-, 0 EN	p. 17 p. 14	This signal selects the even byte of the pair transferred under the vertical return sweep
LA 0-10	p. 10 p. 14	Load Address 0-10 used for DMA transport
LA 11	p. 10	See above



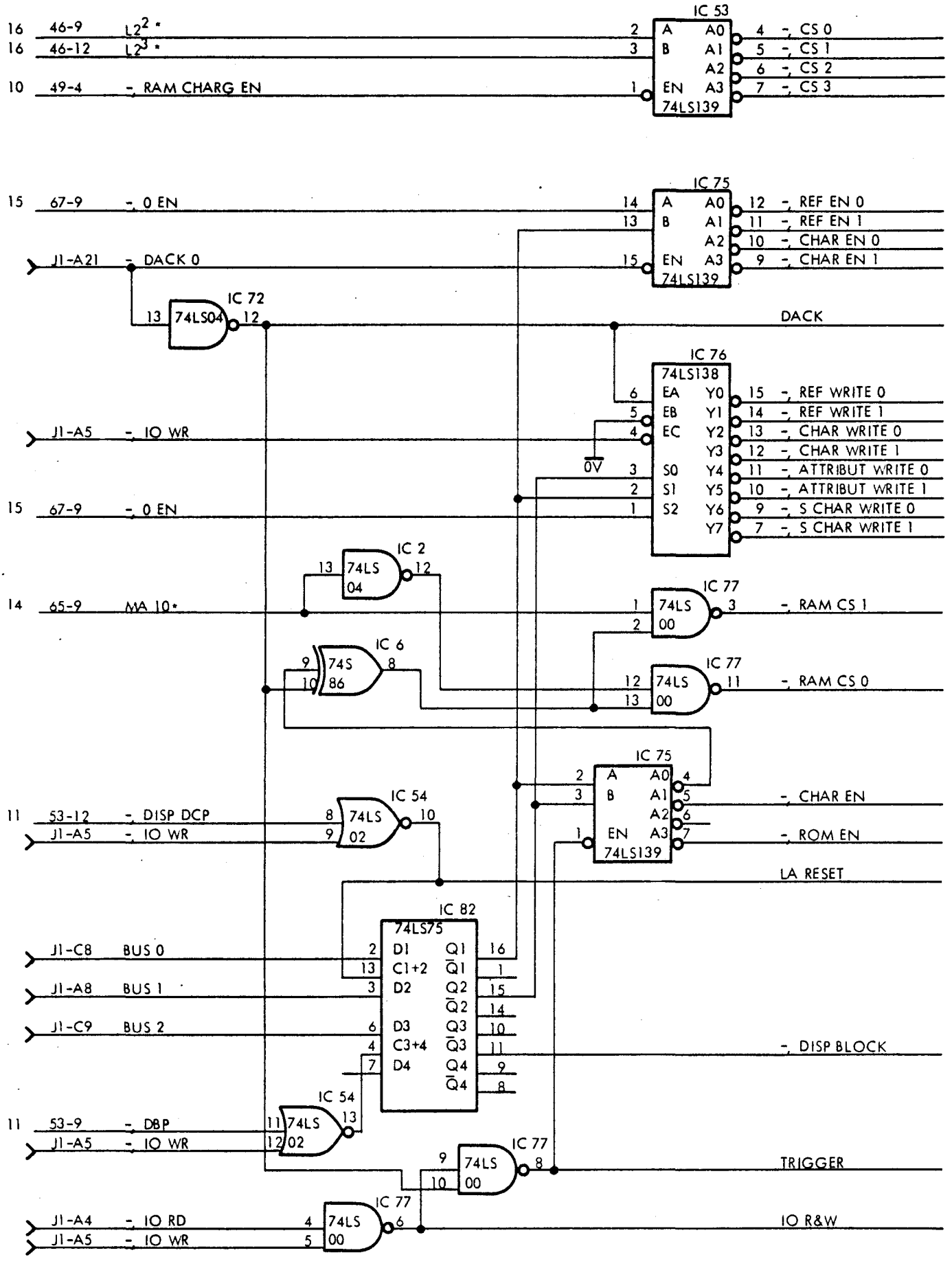
22.6.81 KØN 22.6.81 AMS

SIGNAL	DESTINATION	DESCRIPTION
CURSOR	p. 2	This signal indicates CURSOR position
DISP EN	p. 2 p. 15	This signal indicates that the CRT controller is addressing in the visible display area
$L2^{0-3}$	p. 10	Line address for the character generator
$L2^{4}$	p. 2	See above
MA 0-10	p. 14	Refresh Memory Addresses from the CRT controller
MA 11-13		Not used
-, WAIT		WAIT for the CPU



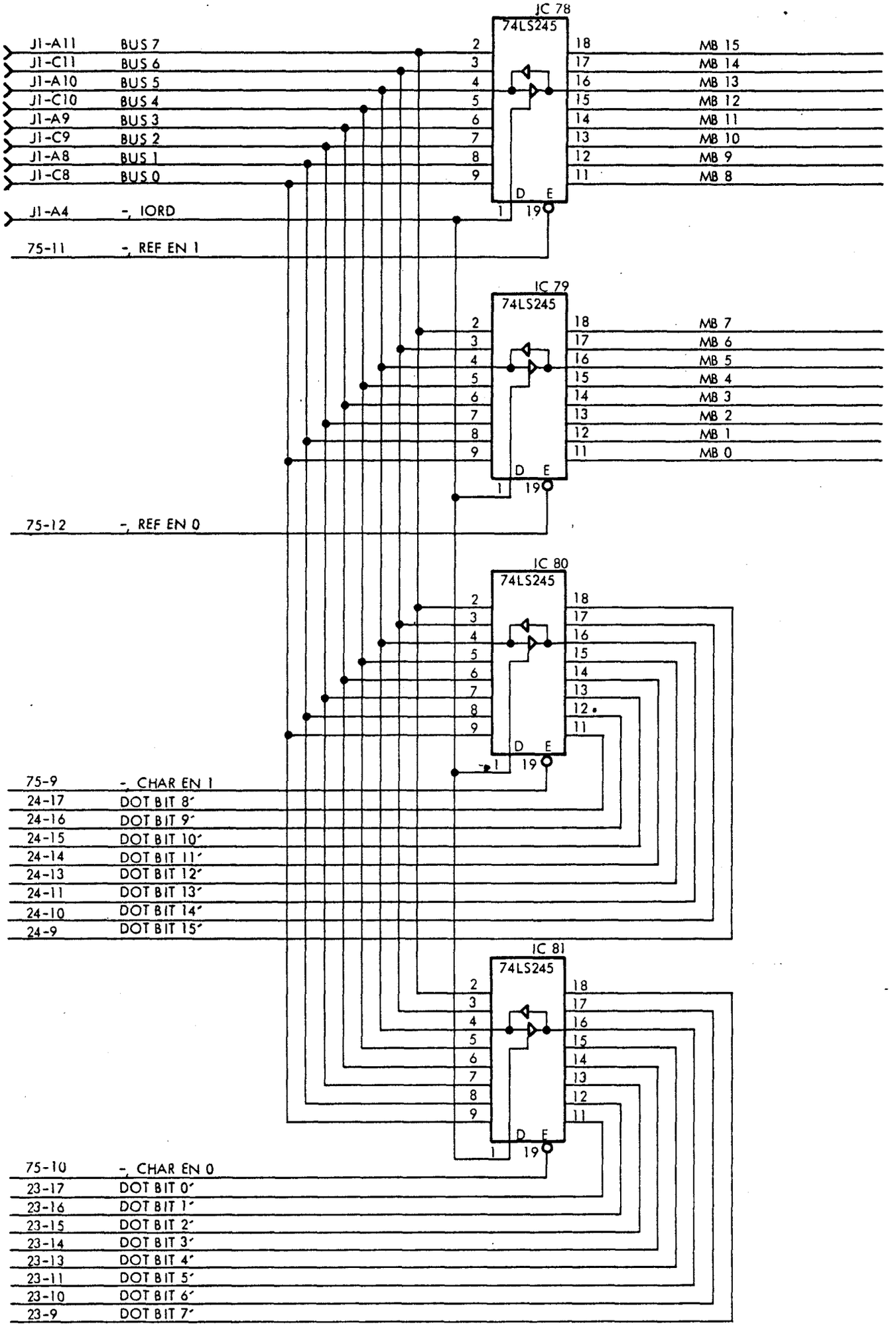
22.6.81 KΦN 22.6.81 AMS

SIGNAL	DESTINATION	DESCRIPTION
-, ATTRIBUT WRITE 0-1	p. 4	WRITE to the ATTRIBUTe juggler RAM
-, CHAR EN	p. 10	RAM CHARacter generator ENable for the DMA transport
-, CHAR EN 0-1	p. 18	ENable the RAM CHARacter bus drivers
-, CHAR WRITE 0	p. 5 p. 6	WRITE to the RAM CHARacter generator
-, CHAR WRITE 1	p. 7 p. 8	See above
-, CS 0-3	p. 5 p. 6 p. 7 p. 8	Chip Select for the RAM CHARacter generator
DACK	p. 10 p. 14	DMA ACKnowledge
-, DISP BLOCK	p. 2	BLOCK of the video
IO R & W	p. 16	Input/Output Read or Write
LA RESET	p. 15	RESET of the Load Address counter
-, REF WRITE 0	p. 12	WRITE to the REFresh RAM
-, REF WRITE 1	p. 13	See above
-, ROM EN	p. 10	ROM character generator ENabled for the DMA transport
S CHAR WRITE 0-1	p. 9	WRITE to the Shadow CHARacter generator
TRIGGER	p. 15	TRIGGER for the load address counter

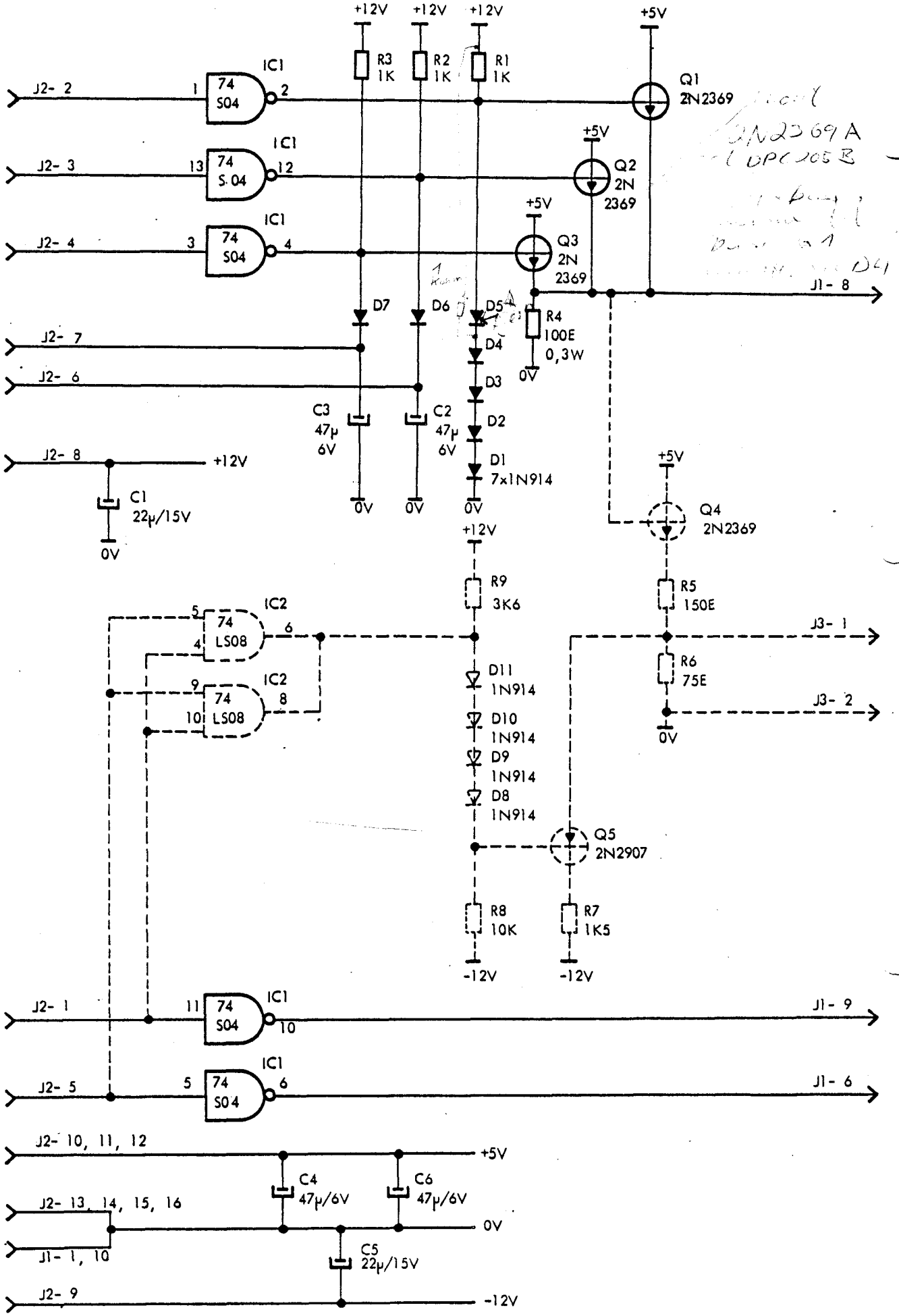


22.6.81 KØN 22.6.81 AMS

SIGNAL	DESTINATION	DESCRIPTION
MB 0-7	p. 11 p. 12	Refresh Memory Bit 0-7
MB 8-15	p. 11 p. 13	See above



22.6.81 KØN 22.6.81 AMS



JOM 800627

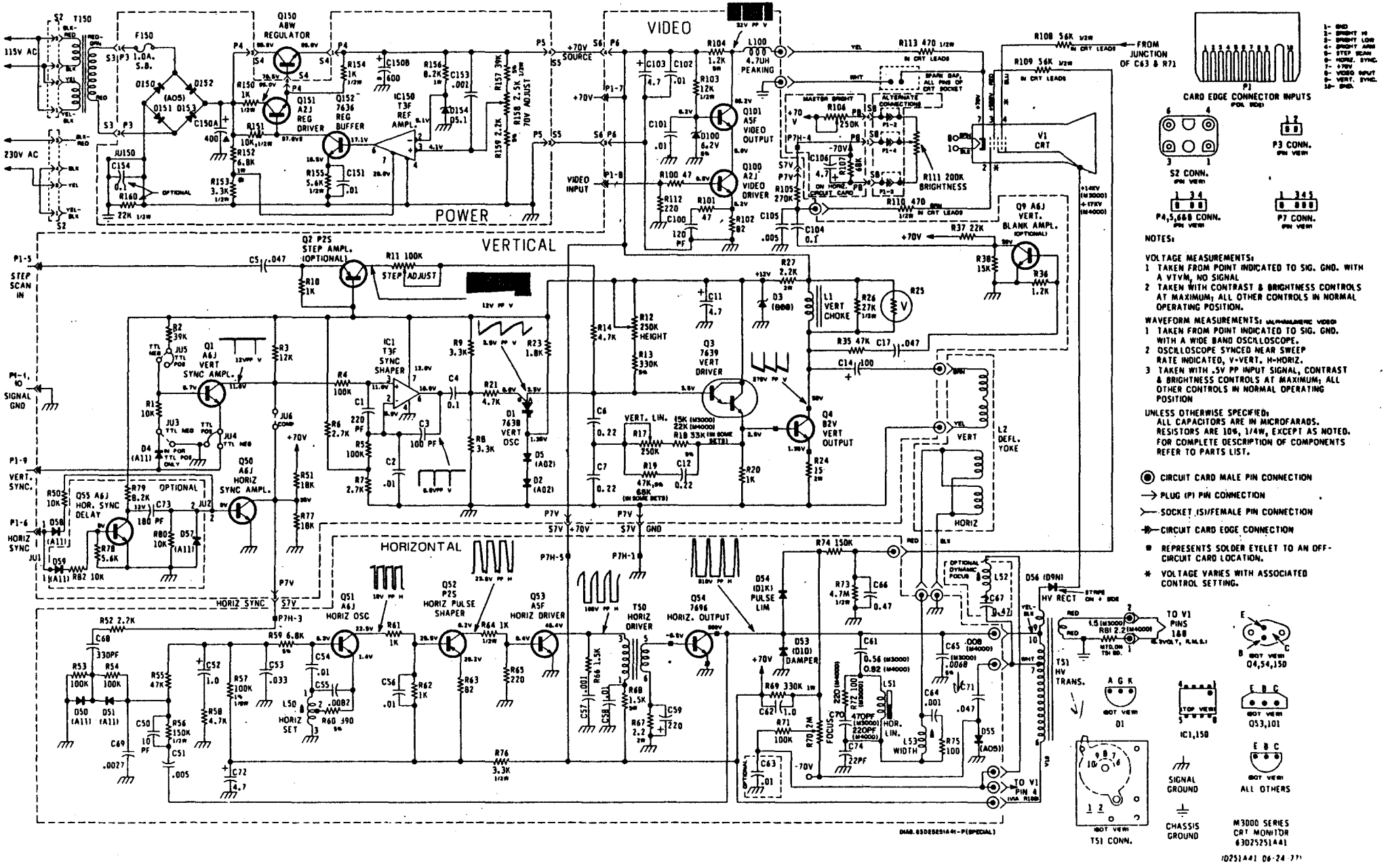
KØN

VIM 502

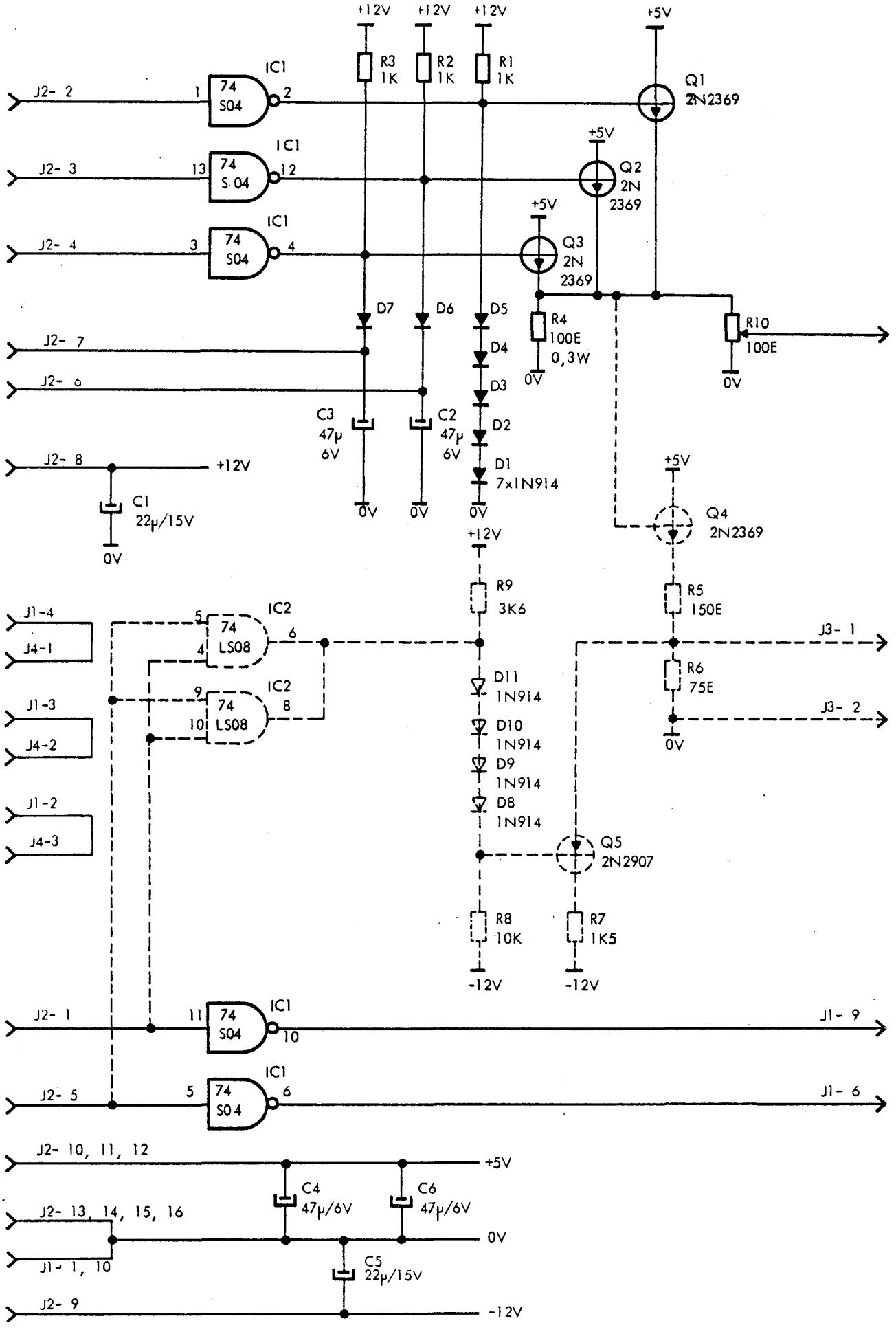
A13861

VIDEO-CONVERTER
Circuit diagram

p.1of 1



Schematic Diagram



KØN 800904 800904 JOM

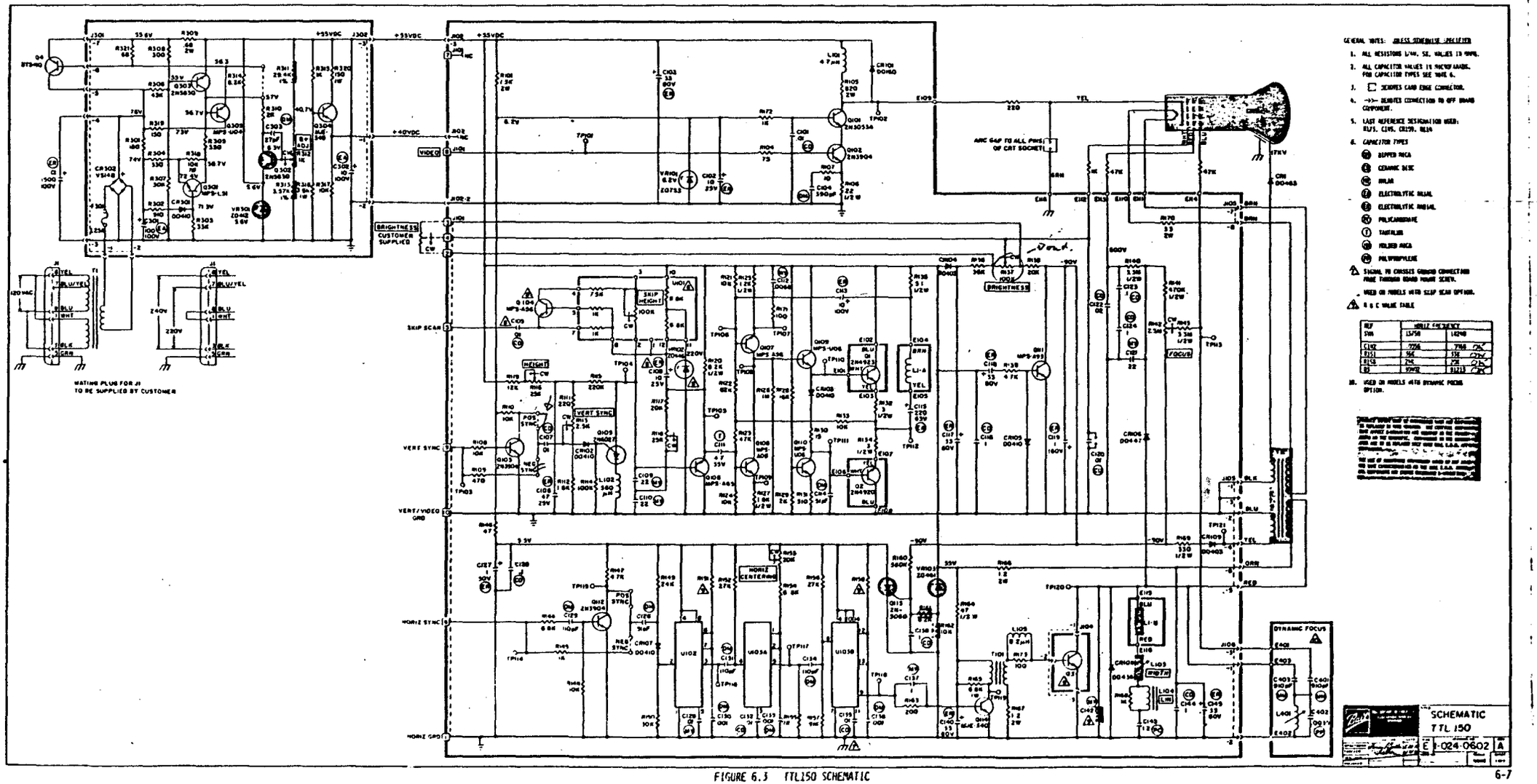
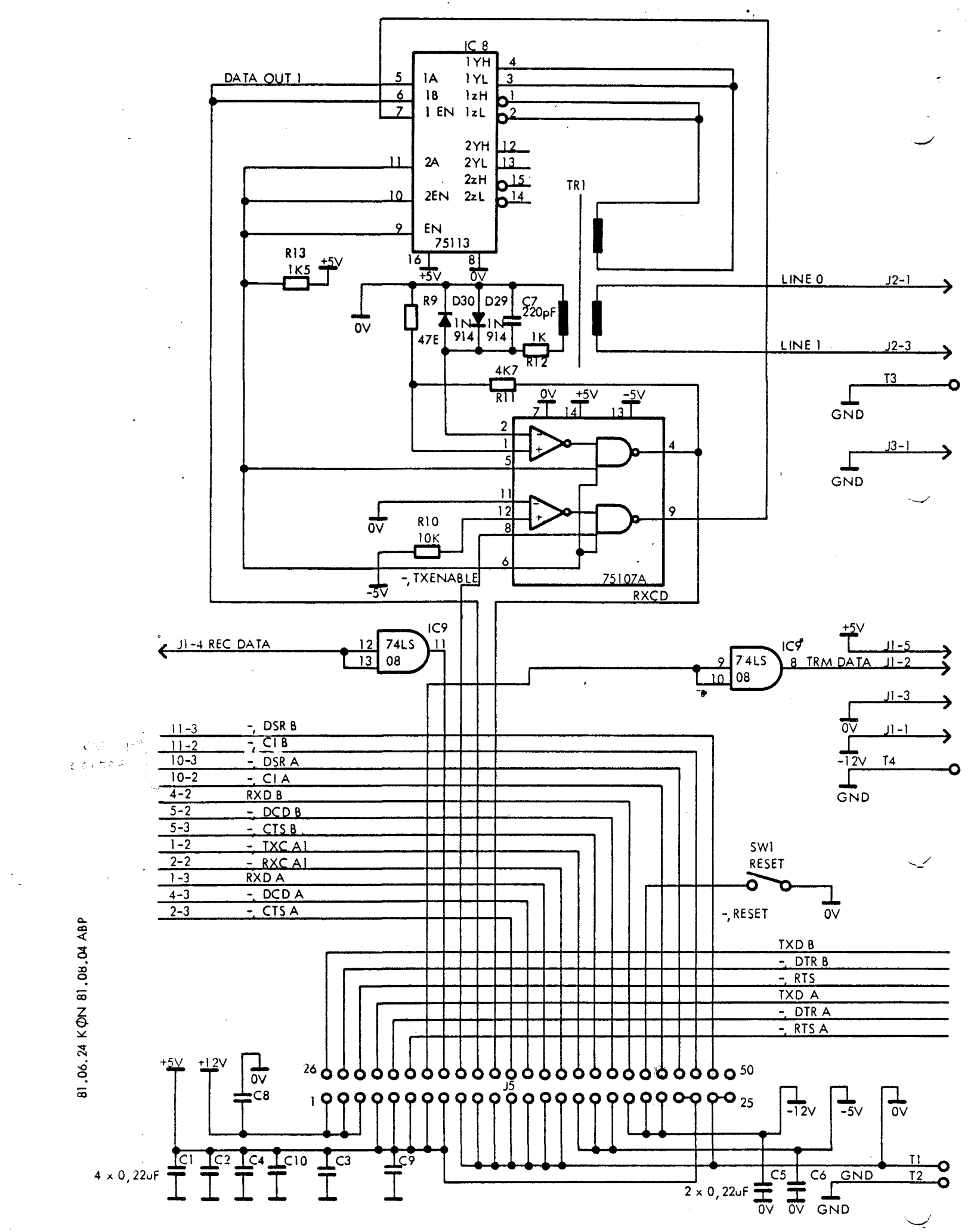


FIGURE 6.3 TTL150 SCHEMATIC

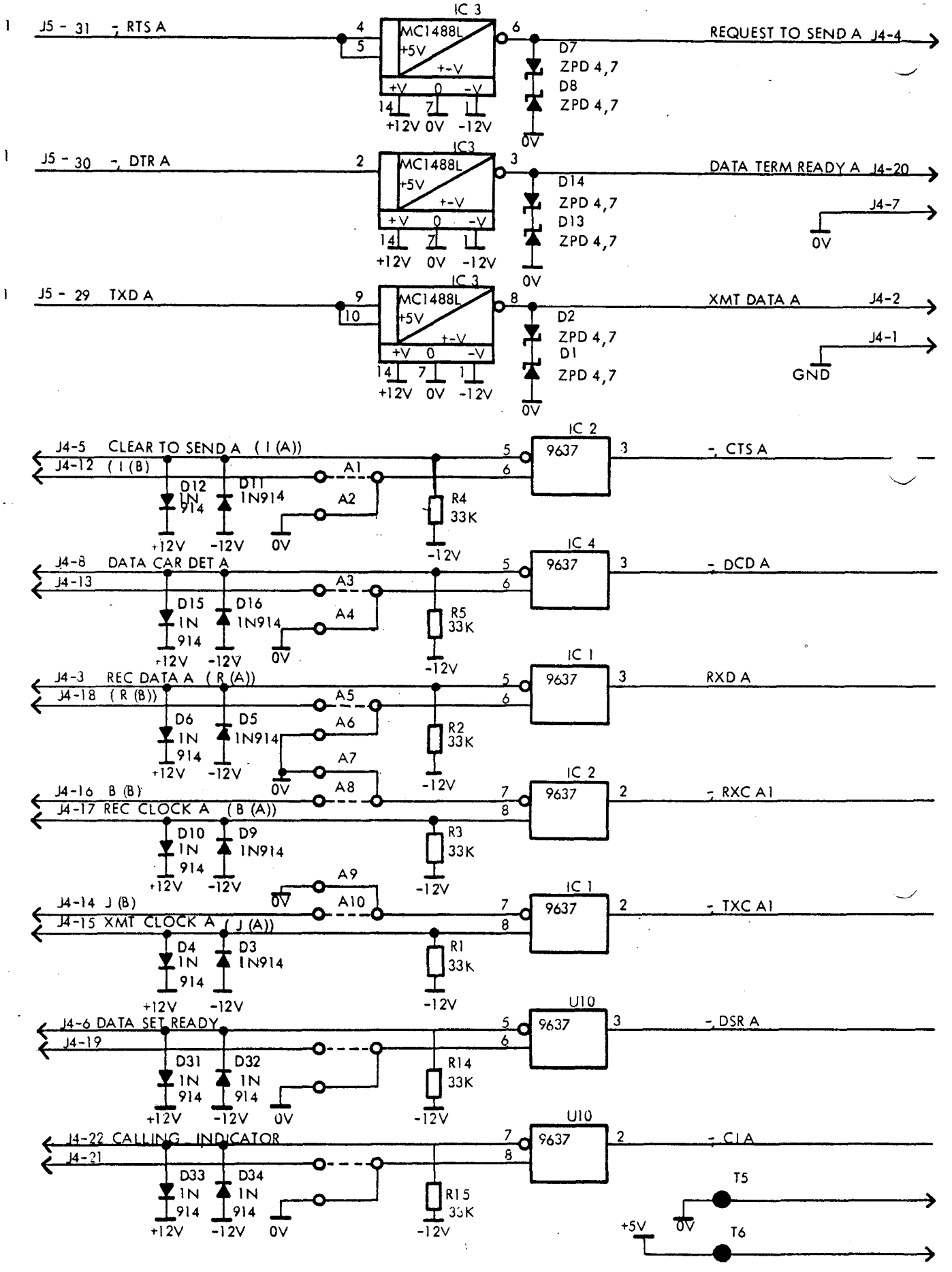
SIGNAL	DESTINATION	DESCRIPTION
-, DTR A	2	Data Terminal Ready to line 1
-, DTR B	3	Data Terminal Ready to line 2
LINE 0-1		RC Circuit LINE I/O
-, RTS A	2	Request To Send to line 1
-, RTS B	3	Request To Send to line 2
TRM DATA		TRansMit DATA to keyboard
TXD A	2	Transmit Data to line 1
TXD B	3	Transmit Data to line 2

KØN 19.6.1981


IC 8
75113
DATA OUT 1
1A
1B
1 EN
1YH
1YL
1zH
1zL
2A
2EN
EN
2YH
2YL
2zH
2zL
TR1
R13
1K5
+5V
0V
R9
47E
D30
D29
1N914
1N914
C7
220pF
1K
RT2
LINE 0
J2-1
LINE 1
J2-3
4K7
R11
T3
GND
J3-1
R10
10K
-, TXENABLE
75107A
RXCD
IC9
74LS
08
J1-4 REC DATA
J1-5
TRM DATA
J1-2
J1-3
J1-1
-12V
T4
11-3 -, DSR B
11-2 -, CI B
10-3 -, DSR A
10-2 -, CI A
4-2 RXD B
5-2 -, DCD B
5-3 -, CTS B
1-2 -, TXC A1
2-2 -, RXC A1
1-3 RXD A
4-3 -, DCD A
2-3 -, CTS A
SW1
RESET
-, RESET
TXD B
-, DTR B
-, RTS
TXD A
-, DTR A
-, RTS A
+12V
C8
J5
26
50
1
25
C1
C2
C4
C10
C3
C9
4 x 0,22uF
C5
C6
2 x 0,22uF
T1
T2
81.06.24 KØN 81.08.04 ABP

SIGNAL	DESTINATION	DESCRIPTION
¬, CI A	1	Calling Indicator from line 1
¬, CTS A	1	Clear To Send from line 1
DATA TERM READY A		DATA TERMinal READY to line 1
¬, DCD A	1	Data Carrier Detected from line 1
¬, DSR A	1	Data Set Ready from line 1
REQUEST TO SEND A		REQUEST TO SEND to line 1
¬, RXC A1	1	Receiver Clock from line 1
¬, RXD A	1	Receive Data from line 1
¬, TXC A1	1	Transmitter Clock from line 1
XMIT DATA A		Transmit Data to line 1

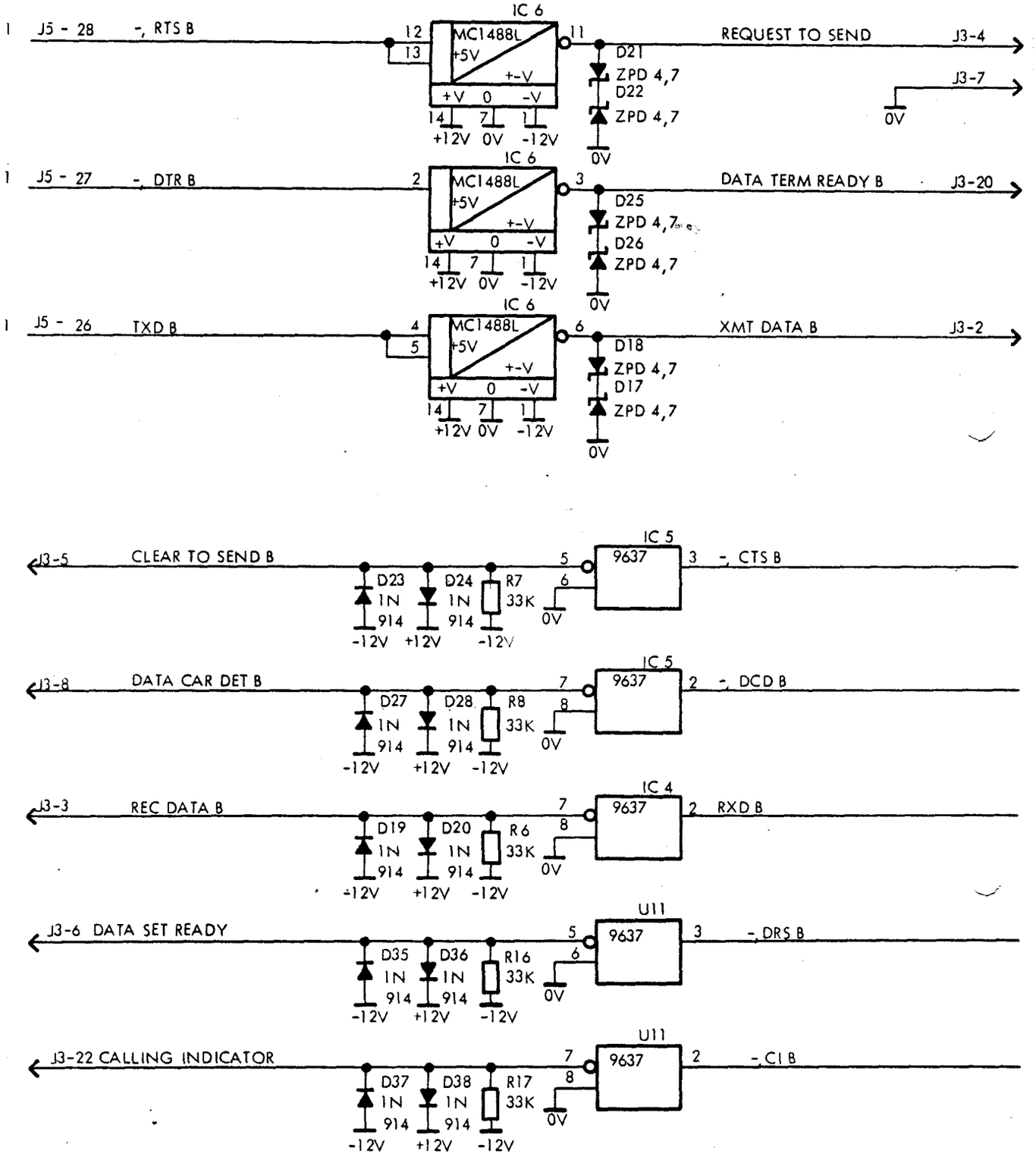
KØN 19.6.1981



810624 KØN 810624 AMS

SIGNAL	DESTINATION	DESCRIPTION
¬, CI B	1	Calling Indicator from line 2
¬, CTS B	1	Clear To Send from line 2
DATA TERM READY B		DATA TERMinal READY to line 2
¬, DCD B	1	Data Carrier Detected from line 2
¬, DSR B	1	Data Set Ready from line 2
REQUEST TO SEND B		REQUEST TO SEND to line 2
¬, RXD B	1	Receive Data from line 2
XMT DATA B		Transmit Data to line 2

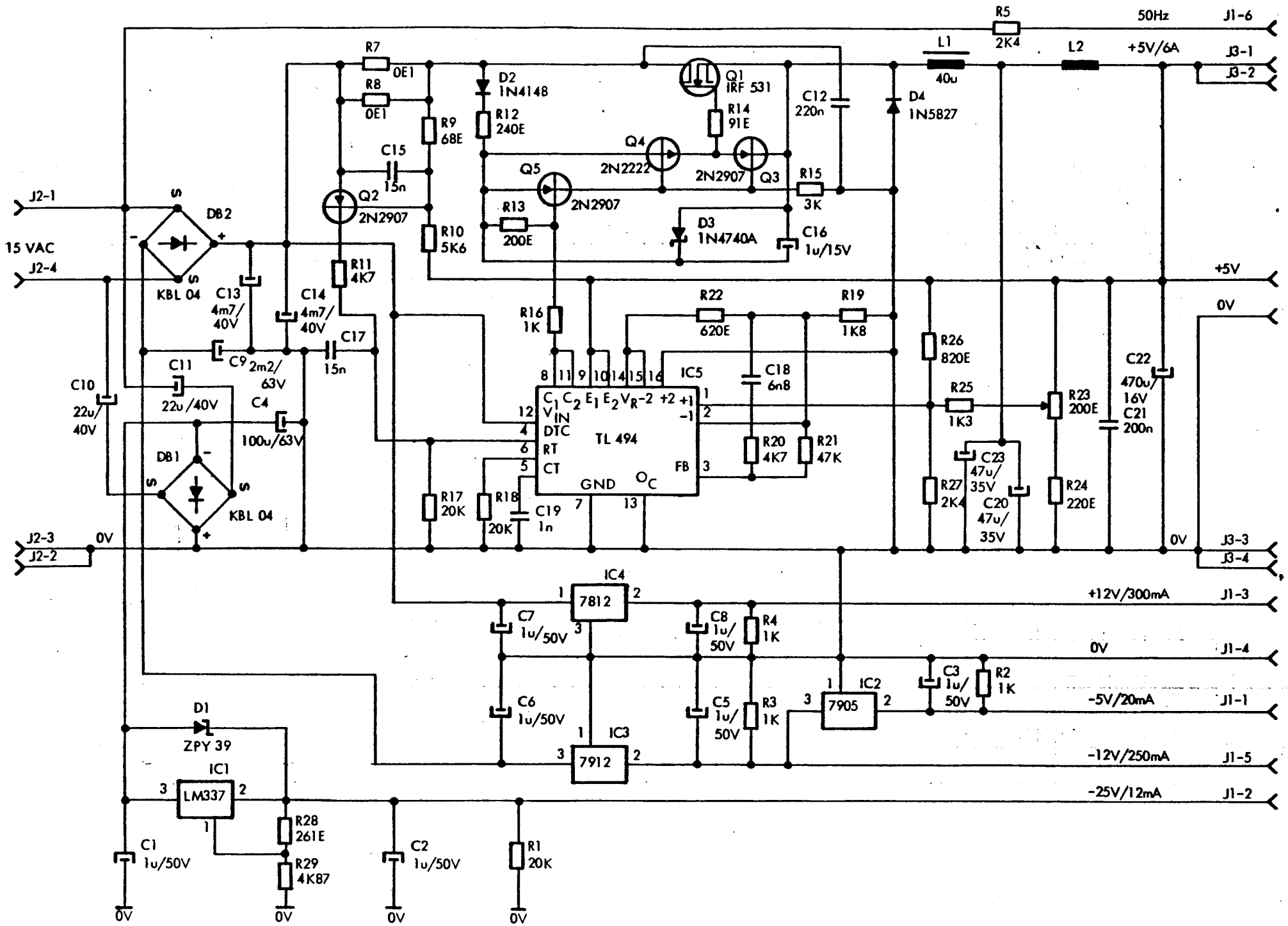
KØN 19.6.1981

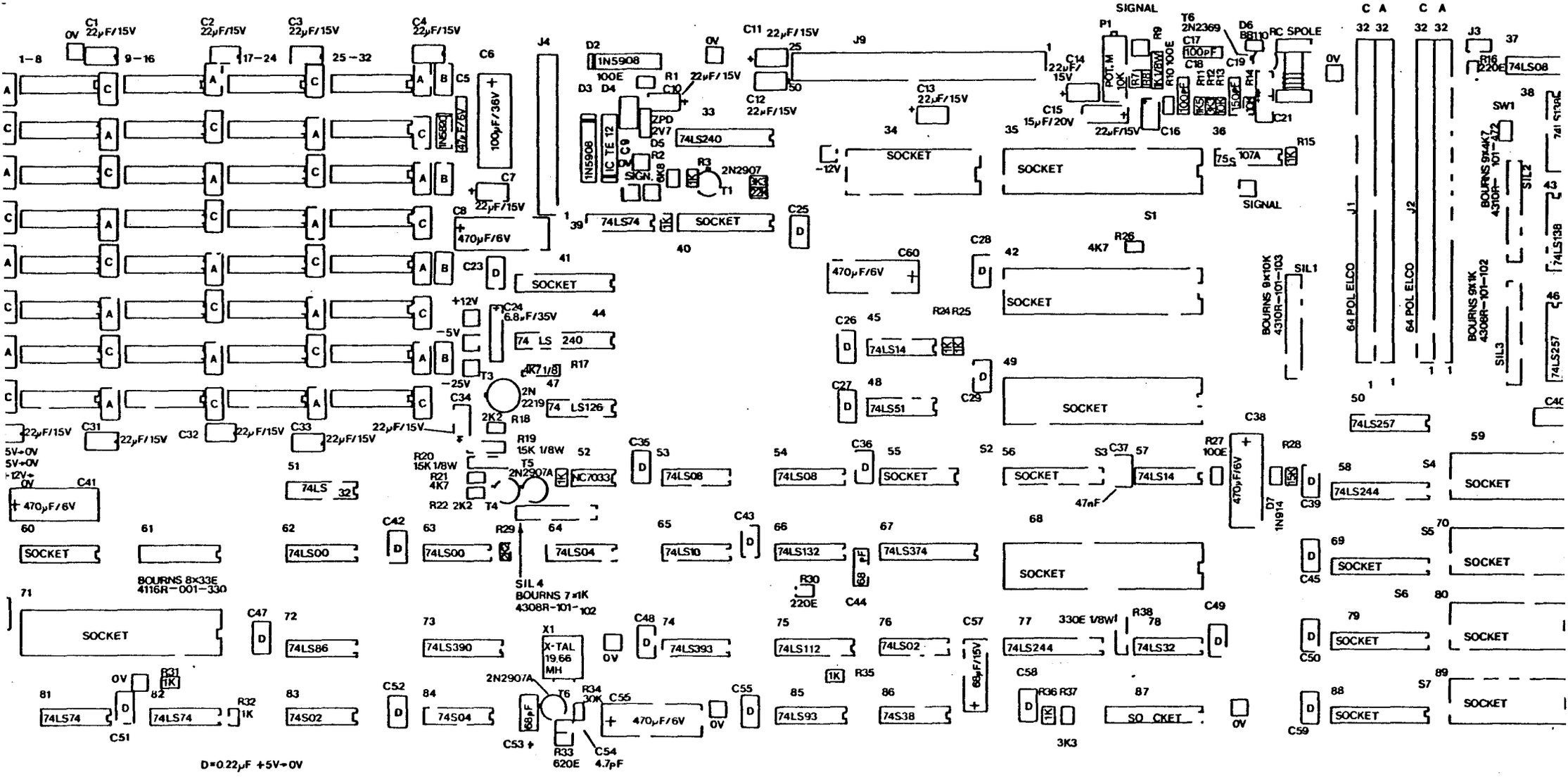


810624 KØN 810624 AMS

RGM 502

H15999





Assembly Drawing for MIC 50x

CONNECTOR : J1
64 PIN ELCO 8257-096-000-124

PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME
A 1		-12V	B 1			C 1		-12V
A 2		0V	B 2			C 2		0V
A 3		-, DISP INTR	B 3			C 3		-, VFO CLOCK
A 4		-, IO RD	B 4			C 4		-, TPVS
A 5		-, IO WR	B 5			C 5		25 Hz
A 6			B 6			C 6		
A 7			B 7			C 7		-, TC
A 8		BUS 1	B 8			C 8		BUS 0
A 9		BUS 3	B 9			C 9		BUS 2
A10		BUS 5	B10			C10		BUS 4
A11		BUS 7	B11			C11		BUS 6
A12			B12			C12		
A13		ADD 0	B13			C13		ADD 2
A14		CHAIN	B14			C14		CHAIN
A15			B15			C15		
A16		ADD 4	B16			C16		
A17		-, WAIT	B17			C17		ADD 3
A18		ADD 5	B18			C18		
A19		ADD 6	B19			C19		
A20		ADD 7	B20			C20		
A21		-, DACK 0	B21			C21		
A22			B22			C22		
A23		DRQ 0	B23			C23		
A24			B24			C24		
A25			B25			C25		
A26			B26			C26		
A27		CLK	B27			C27		-, RESET
A28		-, HOLD ACK	B28			C28		
A29			B29			C29		-, POWER RESET
A30		0V	B30			C30		0V
A31		+5V	B31			C31		+5V
A32		+12V	B32			C32		+12V

CONNECTOR: Pos. 8 16 PIN DUAL - IN LINE SOCKET		
PIN	GEN. ADR.	SIGNAL NAME
1		-, TPVS
2		-, N VIDEO
3		I VIDEO
4		-, INI VIDEO
5		-, TPHS
6		II INTENSITY
7		INE INTENSITY
8		+12V
9		-12V
10		+5V
11		+5V
12		+5V
13		0V
14		0V
15		0V
16		0V

CONNECTOR TO VIDEO CONVERTER

CONNECTOR : J1
64PIN ELCO 8257-096-648-124

PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME
A 1		-12V	B 1			C 1		-12V
A 2		0V	B 2			C 2		0V
A 3		-, FD REQ	B 3			C 3		-, RESET IN
A 4		-, IO RD	B 4			C 4		-, EXT AEN
A 5		-, IO WR	B 5			C 5		-, EXT AD STB
A 6		-, MEM RD	B 6			C 6		-, DRQ 3
A 7		-, MEM WR	B 7			C 7		-, TC
A 8		BUS 1	B 8			C 8		BUS 0
A 9		BUS 3	B 9			C 9		BUS 2
A10		BUS 5	B10			C10		BUS 4
A11		BUS 7	B11			C11		BUS 6
A12		-, INT	B12			C12		-, IORQ BUF
A13		ADD 0	B13			C13		ADD 2
A14			B14			C14		CHAIN 3
A15		-, M1 BUF	B15			C15		ADD 1
A16		ADD 4	B16			C16		-, RD BUF
A17		-, WAIT	B17			C17		ADD 3
A18		ADD 5	B18			C18		ADD 15
A19		ADD 6	B19			C19		ADD 14
A20		ADD 7	B20			C20		ADD 13
A21		-, DACK 1	B21			C21		ADD 12
A22		-, DACK 3	B22			C22		ADD 11
A23		-, DRQ 1	B23			C23		ADD 10
A24		-, WR BUF	B24			C24		ADD 9
A25		-, MREQ BUF	B25			C25		ADD 8
A26		-, RFSH BUF	B26			C26		-, NMI
A27		CLK	B27			C27		-, RESET
A28		-, HOLD ACK	B28			C28		-, HALT BUF
A29		-, HOLD	B29			C29		9,83 Mhz
A30		0V	B30			C30		0V
A31		+5V	B31			C31		+5V
A32		+12V	B32			C32		+12V

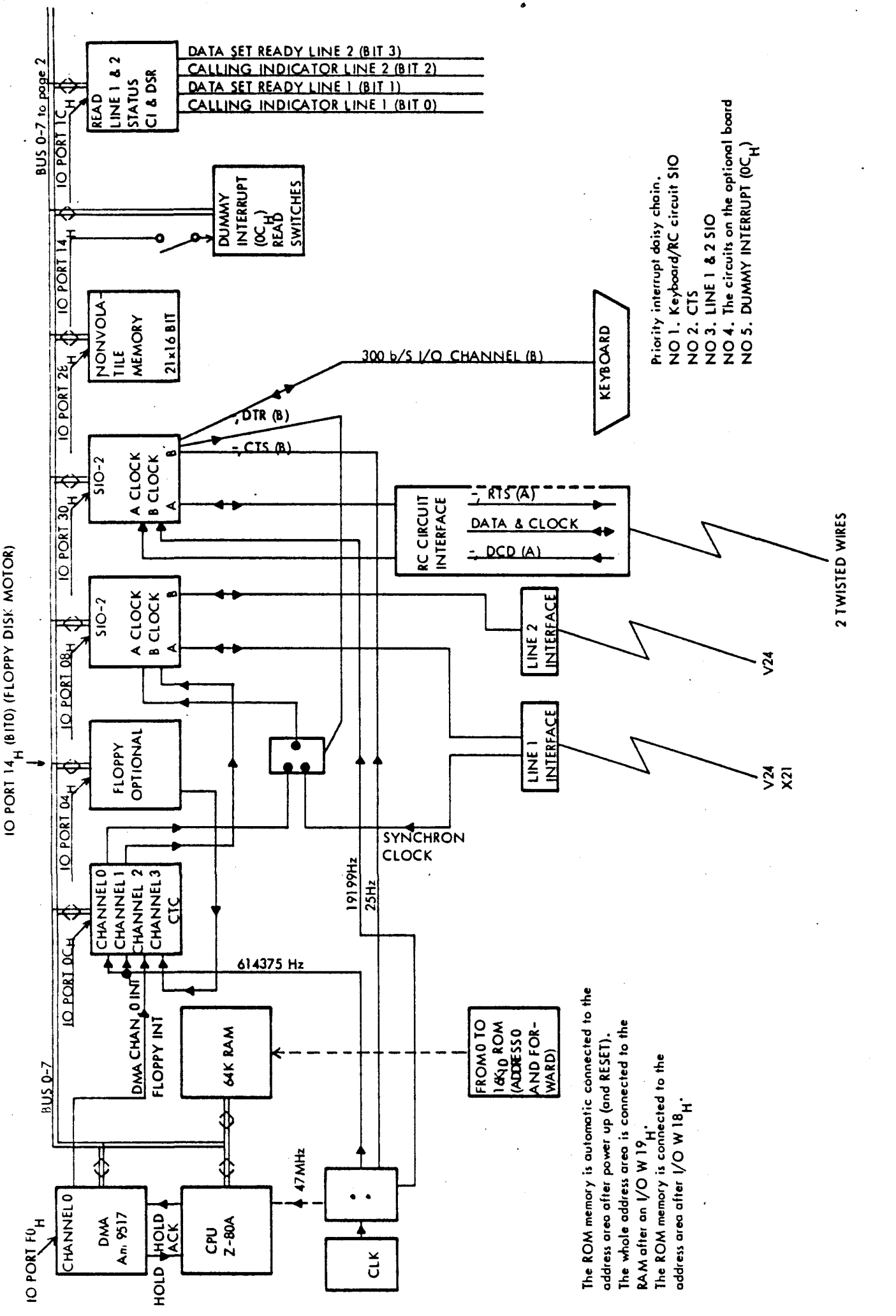
CONNECTOR : J2
64 PIN ELCO 8257-096-648-124

PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME
A 1		-12V	B 1			C 1		-12V
A 2		0V	B 2			C 2		0V
A 3		-, DISP INTR	B 3			C 3		-, VFO CLOCK
A 4		-, IO RD	B 4			C 4		-, TPVS
A 5		-, IO WR	B 5			C 5		25Hz
A 6		-, MEM RD	B 6			C 6		-, DRQ 3
A 7		-, MEM WR	B 7			C 7		-, TC
A 8		BUS 1	B 8			C 8		BUS 0
A 9		BUS 3	B 9			C 9		BUS 2
A10		BUS 5	B10			C10		BUS 4
A11		BUS 7	B11			C11		BUS 6
A12		-, INT	B12			C12		-, IORQ BUF
A13		ADD 0	B13			C13		ADD 2
A14		CHAIN 5	B14			C14		
A15		-, M1 BUF	B15			C15		ADD 1
A16		ADD 4	B16			C16		-, RD BUF
A17		-, WAIT	B17			C17		ADD 3
A18		ADD 5	B18			C18		ADD 15
A19		ADD 6	B19			C19		ADD 14
A20		ADD 7	B20			C20		ADD 13
A21		-, DACK 0	B21			C21		ADD 12
A22		-, DACK 3	B22			C22		ADD 11
A23		DRQ 0	B23			C23		ADD 10
A24		-, WR BUF	B24			C24		ADD 9
A25		-, MREQ BUF	B25			C25		ADD 8
A26		-, RFSH BUF	B26			C26		-, NMI
A27		CLK	B27			C27		-, RESET
A28		-, HOLD ACK	B28			C28		DRQ 2
A29		-, DACK 2	B29			C29		-, POWER RESET
A30		0V	B30			C30		0V
A31		+5V	B31			C31		+5V
A32		+12V	B32			C32		+12V

CONNECTOR : J4 AMP MODU I 280613-2		
PIN	GEN. ADR.	SIGNAL NAME
1		-5V
2		- 25V
3		+12V
4		0V
5		-12V
6		+5V
7		+5V
8		0V
9		0V
10		50 Hz

POWER CONNECTOR TO MIC 50x

CONNECTOR: J9 2 x AMP 2-825433-0				
PIN	SIGNAL NAME		PIN	SIGNAL NAME
1	+12V		26	TX DB
2	+12V		27	-, DT RB
3	+12V		28	-, RT SB
4	+5V		29	TX DA
5	+5V		30	-, DT RA
6	+5V		31	-, RT SA
7	+5V		32	TXD KEYBOARD
8	+5V		33	RXD KEYBOARD
9	0V		34	-, TX ENABLE
10	0V		35	DATA OUT 1
11	0V		36	RX DC
12	0V		37	-, CT SA
13	0V		38	-, DC DA
14	0V		39	RX DA
15	0V		40	-, RX CA 1
16	-5V		41	-, TX CA 1
17	-5V		42	-, CT SB
18	-5V		43	-, DC DB
19	-12V		44	RX DB
20	-12V		45	RESET IN
21	-12V		46	-, DSR B
22	+5V		47	-, CI B
23	+5V		48	-, DSR A
24	0V		49	-, CI A
25	0V		50	-, CI A


BUS 0-7 to page 2
IO PORT 1C H
READ LINE 1 & 2 STATUS CI & DSR
DATA SET READY LINE 2 (BIT 3)
CALLING INDICATOR LINE 2 (BIT 2)
DATA SET READY LINE 1 (BIT 1)
CALLING INDICATOR LINE 1 (BIT 0)
IO PORT 14 H
DUMMY INTERRUPT (0C H) READ SWITCHES
IO PORT 26 H
NONVOLATILE MEMORY 21x16 BIT
300 b/S I/O CHANNEL (B)
KEYBOARD
IO PORT 30 H
SIO-2
A CLOCK
B CLOCK
B
A
DTR (B)
CTS (B)
RC CIRCUIT INTERFACE
RTS (A)
DATA & CLOCK
DCD (A)
IO PORT 08 H
SIO-2
A CLOCK
B CLOCK
B
A
LINE 2 INTERFACE
V24
2 TWISTED WIRES
IO PORT 14 H (BIT0) (FLOPPY DISK MOTOR)
IO PORT 04 H
FLOPPY OPTIONAL
LINE 1 INTERFACE
V24
X21
SYNCHRON CLOCK
IO PORT 0C H
CHANNEL 0
CHANNEL 1
CHANNEL 2
CHANNEL 3
CTC
19199Hz
25Hz
614375 Hz
DMA CHAN. 0 INT
FLOPPY INT
BUS 0-7
64K RAM
FROM 0 TO 16K10 ROM (ADDRESS 0 AND FORWARD)
IO PORT F0 H
CHANNEL 0
DMA An. 9517
HOLD
HLDA
CPU Z-80A
4.7MHz
CLK
HOLD
Priority interrupt daisy chain.
NO 1. Keyboard/RC circuit SIO
NO 2. CTS
NO 3. LINE 1 & 2 SIO
NO 4. The circuits on the optional board
NO 5. DUMMY INTERRUPT (0C H)
The ROM memory is automatic connected to the address area after power up (and RESET).
The whole address area is connected to the RAM after an I/O W 19 H.
The ROM memory is connected to the address area after I/O W 18 H.
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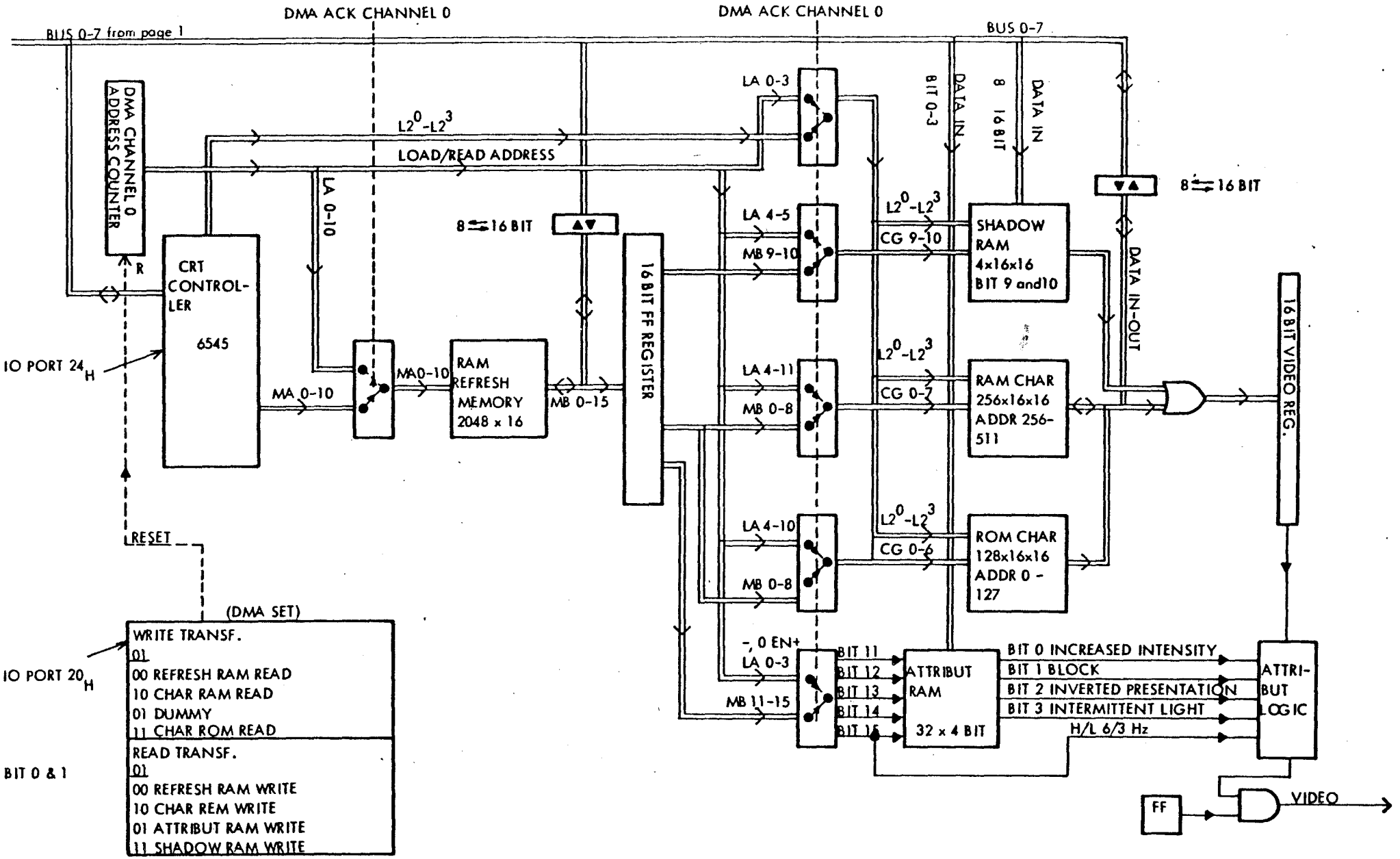

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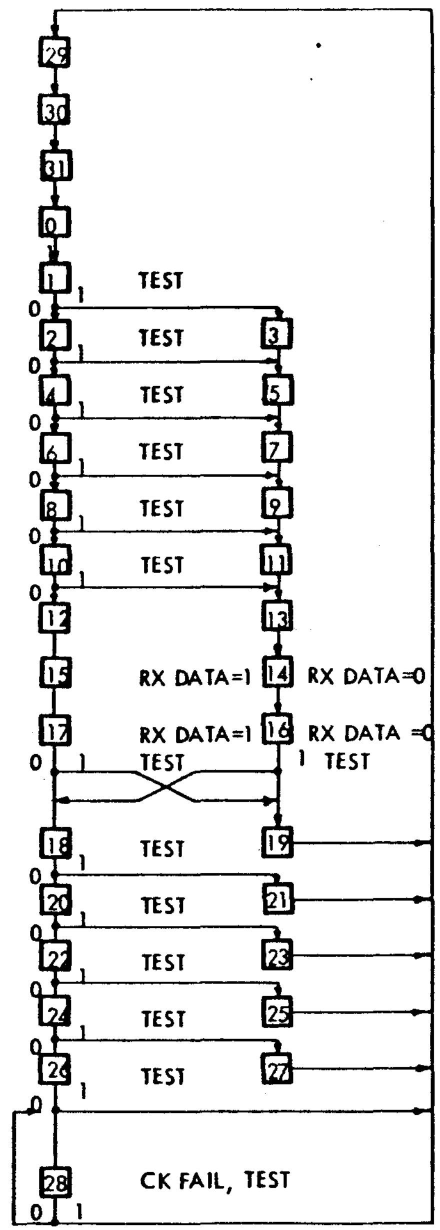


SEQUENCE DIAGRAM

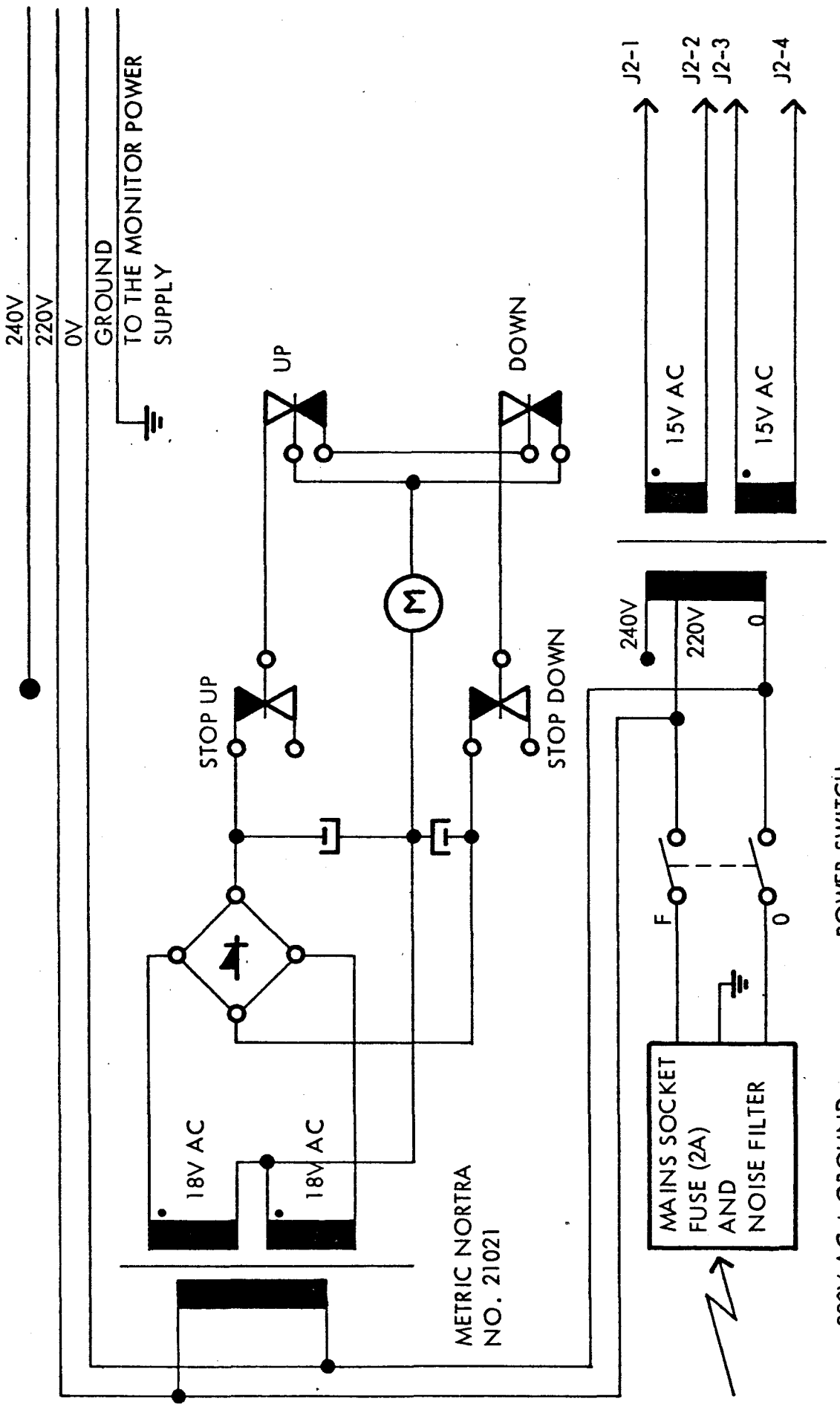
5	6	
0	0	NEXT LSB = 1
0	1	NEXT LSB = 1
1	0	NEXT LSB = 0
1	1	NEXT LSB = TEST RESULT

RX CLOCK → ADDR; RX DATA → ADDR 10; CK FAIL

PN NO	ADDR 14	ADDR 13	ADDR 12	ADDR 11	ADDR 10	NEXT ADDRESS MSB 1	2	3	4	5	6	CK 7	FAIL 9
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	1	1	1	0	0
2	0	0	0	1	0	0	0	1	0	1	1	0	0
3	0	0	0	1	1	0	0	1	0	0	0	0	0
4	0	0	1	0	0	0	0	1	1	1	1	0	0
5	0	0	1	0	1	0	0	1	1	0	0	0	0
6	0	0	1	1	0	0	1	0	0	1	1	0	0
7	0	0	1	1	1	0	1	0	0	0	0	0	0
8	0	1	0	0	0	0	1	0	1	1	1	0	0
9	0	1	0	0	1	0	1	0	1	0	0	0	0
10	0	1	0	1	0	0	1	1	0	1	1	0	0
11	0	1	0	1	1	0	1	1	0	0	0	0	0
12	0	1	1	0	0	0	1	1	1	0	0	0	0
13	0	1	1	0	1	0	1	1	1	1	0	0	0
14	0	1	1	1	0	1	0	0	0	1	0	0	0
15	0	1	1	1	1	1	0	0	0	0	0	0	0
16	1	0	0	0	0	1	0	0	1	1	1	0	0
17	1	0	0	0	1	1	0	0	1	1	1	0	0
18	1	0	0	1	0	1	0	1	0	1	1	0	0
19	1	0	0	1	1	1	1	1	0	0	0	0	0
20	1	0	1	0	0	1	0	1	1	1	1	0	0
21	1	0	1	0	1	1	1	1	0	0	0	0	0
22	1	0	1	1	0	1	1	0	0	1	1	0	0
23	1	0	1	1	1	1	1	1	0	0	0	0	0
24	1	1	0	0	0	1	1	0	1	1	1	0	0
25	1	1	0	0	1	1	1	1	0	0	0	0	0
26	1	1	0	1	0	1	1	1	0	1	1	0	0
27	1	1	0	1	1	1	1	1	0	0	0	0	0
28	1	1	1	0	0	1	1	1	0	1	1	1	0
29	1	1	1	0	1	1	1	1	1	1	0	0	0
30	1	1	1	1	0	1	1	1	1	0	0	0	0
31	1	1	1	1	1	0	0	0	0	1	0	0	0

ROA 516

LISTING OF DEMODULATOR ROM FOR RC CIRCUIT
ROA 516



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