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RC850 Controller
Reference Manual

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Keywords:

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Abstract:

This paper describes the structure of the RC850 hardware, and how it can be accessed software-wise.

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1. RC850 DISPLAY COMPONENTS 1.

The RC850-display contains the following components, see figs. 1 and 2:

Name	Use	IO port number Hex.
CPU Z80A	CPU	
ROM	4k Read only Memory	
RAM	64k Random access Memory	
Floppy disc		04 (-07)
Z80 SIO 2	Channel A Line interface	08 (0A)
	Channel B Printer interface	09 (0B)
CTC	Line speed selector Line interf.	0C
	Line speed selector Printer intf.	0D
	Interrupt handler for Display	0E
	Interrupt handler for Floppy	0F
PROM->RAM	IO port used for selection of RAM/PROM memory	18(-1B)
DMA FUNCTION	Selects a memory part of the Display module and access it	20(-23)
CRT	Display controller	24(-27)
NVM	Non Volatile memory Memory for storing configuration information.	28(-2B)
Display Blank	Display blanked for any signal	2C(-2F)

Name	Use	IO port number Hex.
Z80-SIO2	Channel A CIRCUIT	30
	Channel B Keyboard	31
	CIRCUIT control	32
	Real time clock	33
	Switch selecting sync/async for line interface	33
DMA	Direct memory access	F0-FF
	Priority in the shown order	
	Channel 0 Display Channel 1 Floppy Channel 2 CIRCUIT/COAX Channel 3 Extension	
CLK	Clock pulse device	
	4 MHz for CPU 614375 Hz for Channel 0 and 1 in CTC 19199 Hz for Keyboard SIO 25 Hz on CTS in keyboard SIO used for Real time clock	
Switch (not named)	Switch box for line interface synch/asynch selector. It is selected by the DTR signal at the keyboard SIO.	

Priorities

BUS:	1	Keyboard/CIRCUIT	
	2	CTC	
	3	Line/printer SIO	
CTC	1	Channel 0. Line interface	SIO ch. A
	2	Channel 1. Printer interface	SIO ch. B
	3	Display interrupt	
	4	Floppy interrupt	

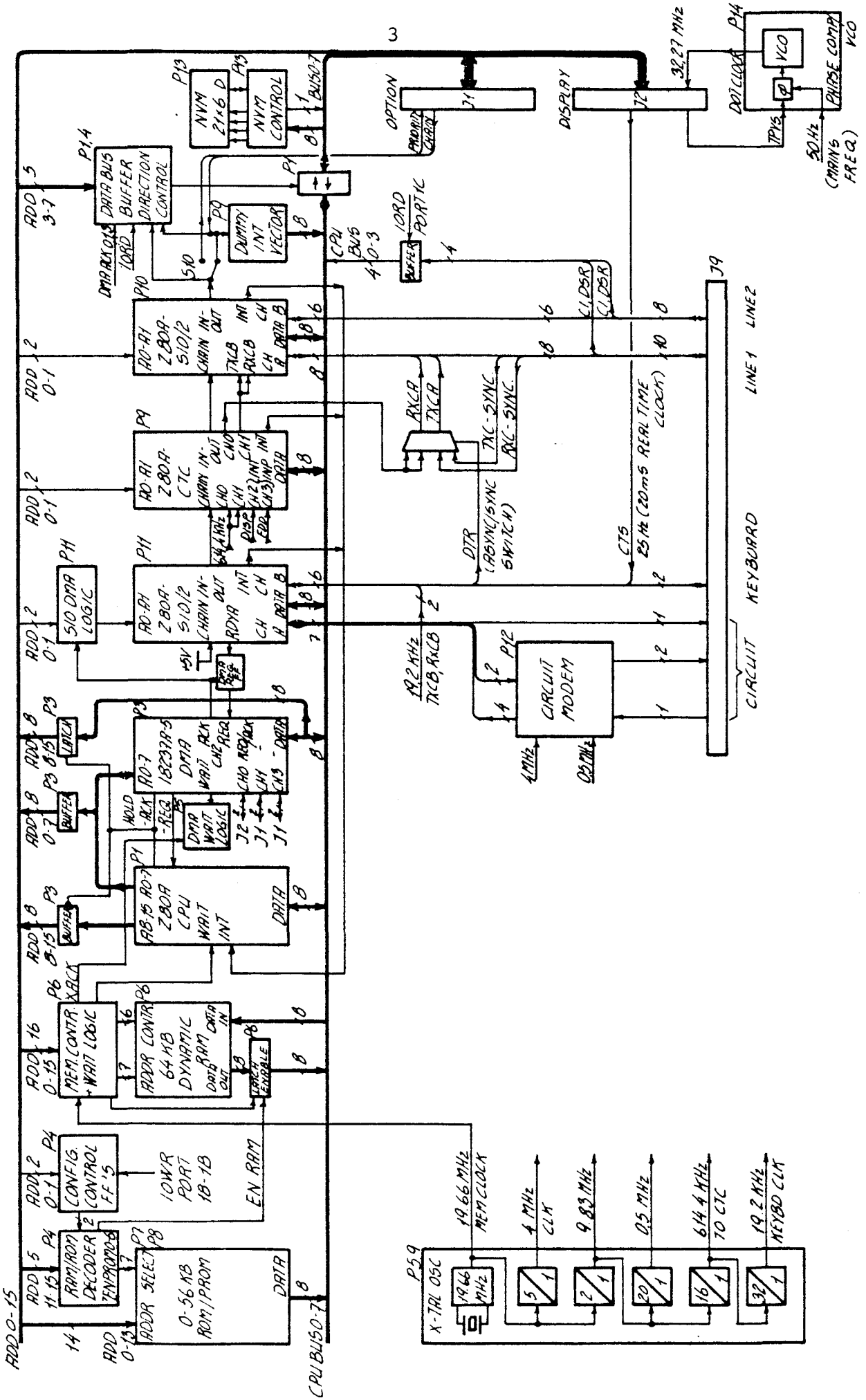


Figure 1: Microprocessor System, Block Diagram.

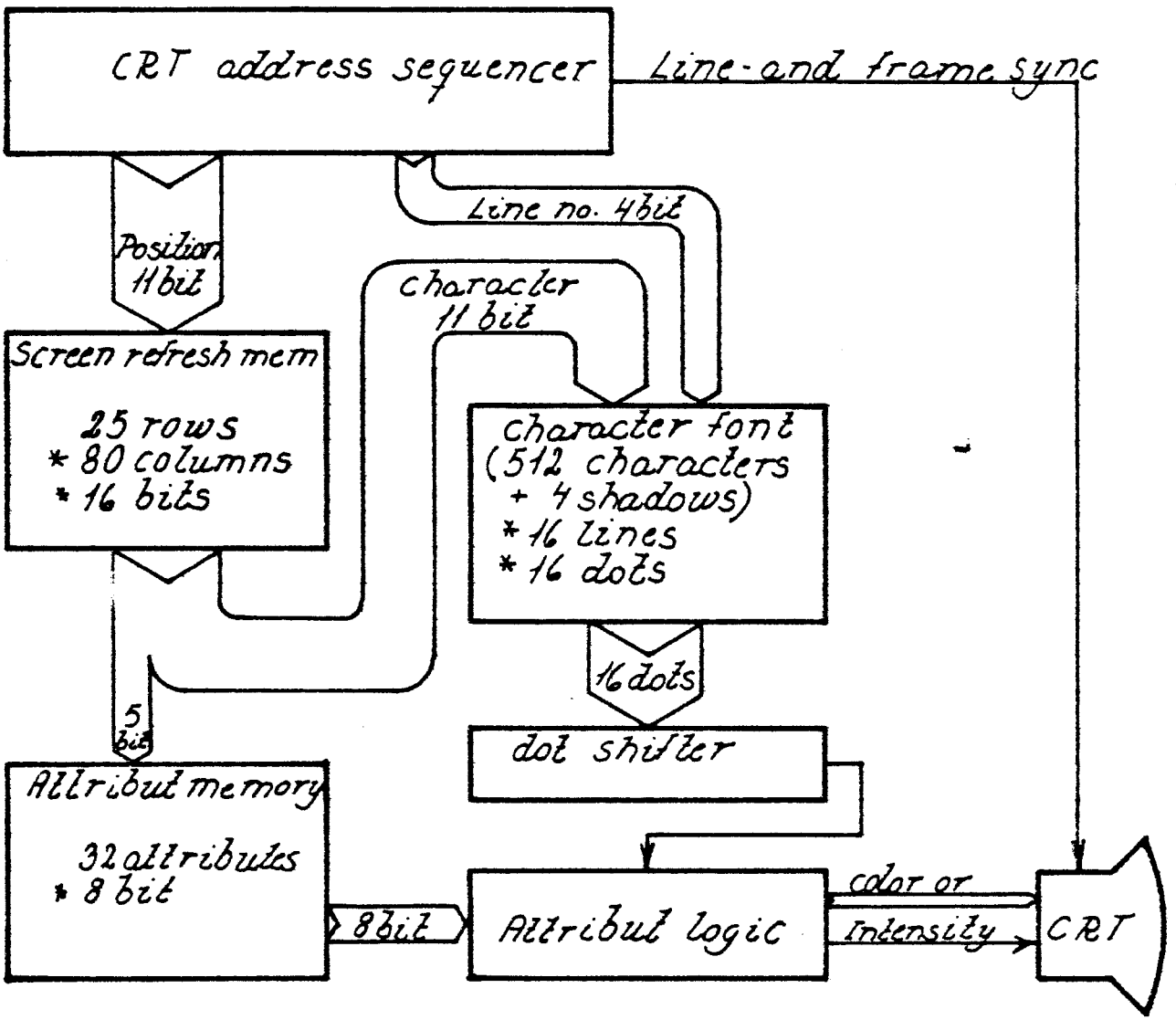


figure 2: Blockdiagram for CRT504

2. HOW TO USE THE DISPLAY MODULE

2.1 General Description

To create the visual impression of a picture on the CRT (Catode Ray Tube = electron beam tube) screen, the screen contents must be output to the CRT with a repetition rate of more than 50 times per second.

As the screen contains 448000 "pixels" (i.e. dots with mutually independent light intensity or colour), the CRT must constantly be fed with an information stream with an average speed of 50 x 448000 x 3 = 67.2 Mbits/sec. Clearly the CPU cannot supply that directly, so this is the task of the display module.

The electron beam sweeps the screen in horizontal lines covering the screen as shown in fig. 3.

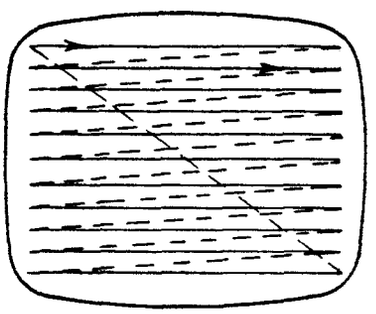


Figure 3: Scan pattern on the CRT screen.

Wherever the beam hits the screen, the phosphor will transform the energy of the electrons being decellerated from a high velocity into light, the intensity of which depends on the intensity (current) of the beam.

So modulating the beam current in dependence of the momentary position of the impact gives control of the distribution of light over the screen.

The pixels are hence organized in 350 lines grouped in 25 rows with 14 lines each.

The lines consist of 1280 pixels each, organized in 80 columns with 16 pixels each.

Each intersection of a row and a column makes out one character position hence the screen can display 25 rows with 80 characters in each.

Each character position has 14 lines with 16 pixels each. Referring to the block diagram, the display module has some memories for refreshing the screen.

The screen refresh memory has an item (two bytes) for each character position, selecting which character is to be displayed at that position, and how the character is displayed (green on black, black on green, blinking or white (ultra bright) on black, or in case of a colour screen: which colour on which).

The information for a certain character position is (controlled by the CRT address sequencer) coming out of the screen refresh memory every time the e-beam is coming into this character position. This happens 14 times for each character position for each screen refresh due to the way in which the CRT is swept.

11 bits are used to select two characters to be superimposed eachother in this position. 9 bits select one character (out of 512), 2 bits select the other character called the "shadow".

5 bits are used to select one of 32 eight bit attributes explained in detail in section 2.7.

The character fonts are addressed by the 9 + 2 bits from the screen refresh memory plus a 4 bit number from the CRT address sequencer indicating which of the 14 lines within the character is to be displayed.

The output of the character fonts are two 16 bit words superimposed eachother (logically or'ed) making out the dotpattern to be displayed.

The 16 bits are shifted out of the shifter one by one, and used in the attribute logic to select background (0) or foregorund (1) to be displayed in this pixel.

The following describes the components of the Display module and how to control them from the CPU.

Name	Use	Access method
CRT Address sequencer	Initialize display constants, cursor control	IO port 24 HEX
DMA FUNCTION register	Selects which display part should be accessed, and starts the transfer	IO port 20 HEX
Screen refresh Memory	Memory for characters and attributes for every position on the display 2048 x 16. 2000 x 16 used for 2000 display positions	Normal memory-write in main memory loc. F000-FFFF implies a write into the corresponding refresh memory location as well
Shadow font RAM	Memory for a shadow pattern which is displayd together with the character pattern. 4 x 16 x 16 used for 4 shadow patterns	WRITE DMA operation
Character font ROM	Memory for 128 or 256 preloaded character patterns 128 x 16 x 16 or 256 x 16 x 16	READ DMA operation
Character font RAM	Memory for 256 loadable character patterns 256 x 16 x 16	Read or write DMA operation
Attribute RAM	Memory which converts the 5 attribute bits to the possible light effects	WRITE DMA operation

Display Disable	A Flip-Flop which when set turns the e-beam off	IO port 2C

2.2 CRT Address Sequencer 2.2

The task of the CRT address sequencer is repeatedly to generate addresses for reading the screen refresh memory and the character fonts. It also generates the necessary line sync and frame sync signals to the CRT.

The CRT address controller used is a Motorola MC6845 CRT Controller. For further information refer the data sheet.

Initialization of the CRT controller

The following table shows which registers should be initialized and the used values.

Register address	Value Decimal	Name and description	Size in bits	Access method HEX
		Address register, point out the accessed register	5	IO port 24
R0	96	Horizontal total is the total of displayed and non displayed characters time units minus one(95)	8	IO port 25
R1	80	Horizontal Displayed register number of displayed characters on a horizontal line	8	IO port 25
R2	90	Horiz. Sync Position For horizontal ajustment	8	IO port 25

Register address	Value Decimal	Name and description	Size in bits	Access method HEX
R3	10	Horiz. Sync. width For horizontal ajustment.	4	IO port 25
R4	25	Vertical Total Visual number of Lines -1 = 24	7	IO port 25
R5	10	Vertical Total ajust No of Scan lines not visible	5	-
R6	25	Vertical displayed no of character lines	7	-
R7	25	Vertical sync. position For vertical ajustment	7	-
R8	00	Interface mode Controls the master scan mode	2	-
R9	13	Max. scan line Addr. No of scan lines pr. character -1	5	-
R10	2x32+14	Cursor start Sets the blink timing of cursor bit 5 - blink bit 6 - frequency 1/16 or 1/32 of field rate (50 Hz) bit 0 - bit 4 cursor start addr scanline no.	7	-

Register address	Value Decimal	Name and description	Size in bits	Access method HEX
R11	14	Cursor end bit 0 - bit 5 cursor end addr Scan line no.	5	IO port 25
R12	0	Start addr Heigh Heigh byte of first refresh address	6	-
R13	0	Start addr Low Lower byte of above	8	-
R14	0	Cursor heigh heigh byte of cursor position 0-1999	6	-
R15	0	Cursor low lower byte of above	8	-
R16	-	Light pen Heigh and low	6	-
R17	-	not used	8	-

This initialization can be performed at any time and is recommended now and then at idle time e.g. in a dummy loop to prevent errors in the display.

R0-R13 are write only registers.
R14 and R15 are read and write registers.
R16 and R17 read only registers.

The initialization should take place as follows:

.Set register address

```
Set register A to register address
out 24_16; IO port 24 used
```

.Write register value

```
set register A to register value
out 25_16; IO port 25 used
```

or

.Read register value

```
in  25_16; IO port 25 used
        ; Register A contains the
        ; register value of the
        ; addressed register.
```

2.3 DMA Use 2.3

The CRT controller uses the DMA channel 0 for DMA transfers to the display.
How to address the DMA is described in DMA chapter 4.

DMA Initialization

The 'command register' should be reinitialized as described in the DMA chapter.

DMA Channel 0 Use

When a transfer to or from the display is wanted the following should be performed:

.set mode register as follows:
    select channel 0
    read or write transfer,
    Demand mode
    Address increment/decrement

.set base address and
.set base word count

as follows:

```
lda ...          ; set register A to mode register content
out FB           ; write register A to mode register.
out FC           ; clear internal flip/flop
                 ; set base address
lda 'low byte'   ; low byte in register A
out F0           ; set low byte of base address
lda 'high byte'; high byte in register A
out F0           ; set high byte of base address

out FC           ; clear internal flip/flop
                 ; should not be necessary.
                 ; set base byte count
lda 'low byte'   ; set 'low byte' of byte count
out F1           ;
lda 'high byte'; set 'high byte' of byte count
out F1           ;
```

DMA TRANSFER

Writing a number = 1, 2 or 3 into IO port 20H starts the DMA transfer selected by the number:

DMA FUNCTION select	DMA WRITE to main memory from	DMA READ from main memory to
1	Char. font RAM	Char. font RAM
2	nowhere	Attribute memory
3	Char. font ROM	Shadow font

```
lda DMAF  ;  Select the display memory and
out 20    ;  start the transfer.
```

The transfer starts to address 0 of the selected memory, and takes place byte by byte.

When a DMA transfer is finished, the DMA interrupts the CPU on channel 2 on the CTC.

2.4 Screen Refresh Memory 2.4

The screen refresh memory consists of 4096 bytes of which only the 4000 bytes are accessed by the CRT address sequencer.

The refresh memory is maintained as a copy of the CPU work memory with addresses F000H to FFFFH. This identity is maintained as follows: whenever the CPU or the DMA writes into a location in the mentioned area, the same data is written into the corresponding location of the refresh memory.

After power up, the contents of the two memories are hardly identical, so initialization of the area must be performed.

The existence of a separat refresh memory is caused by the huge load, direct refresh in CPU memory would represent, causing the CPU to run much slower.

Each pair of addresses in the refresh memory corresponds to a character position on the screen.

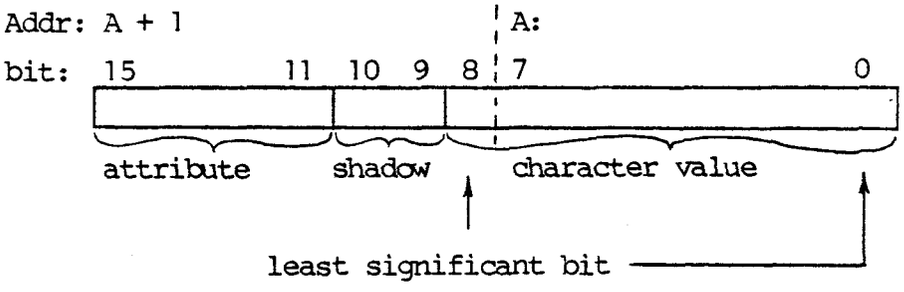
The 2000 character positions are numbered position by position, row by row; that is, the first row contains the positions P = 0 to 4FH left to right, second row contains the positions P = 50H to 9FH etc. Last row contains the positions P = 780H to 7CFH.

The address of the first byte in a pair is thus the even number A = F000H + 2 * P, and the address of the second is A + 1.

The last address displayed is thus F000H + 2 * 7CFH + 1 = FF9FH.

The Refresh RAM (2048 x 16) bits has the following format.

The bytepair is used as follows:



2.5 Character Font

The character font converts character value to dotpattern, i.e. defines the "look" of the character with the given value.

A character consists of 16 lines (only the first 14 are displayed) each containing 16 pixels.

The character font consists of:

1) a read only font containing up to 256 characters,
2) a writeable font containing up to 256 characters and
3) a writeable "shadow"-font containing up to 4 "shadows" to be superimposed (logically or'ed to) the displayed character.

The character value Ch(0:10) from the refresh memory is used together with the correct line number from the CRT address sequencer to address a line of a character and the same line of a shadow. The 16 output bits from the two are or'ed in 16 or-gates, and the result is loaded into the shift register to be shifted bit by bit into the attribute logic at a rate of 32 Mbits/sec.

Ch(0:8) selects the character, if Ch(2) is zero, the read-only font is addressed, else the writeable font is addressed.

Ch(9:10) selects the shadow.

All three fonts may be accessed by the CPU, by means of DMA transfers to or from the CPU memory. The shadow font cannot be read from the CPU.

When a font is transferred, the characters (or shadows) are transferred in the order of increasing value (zero first corresponding to lowest memory address), each character occupying 32 bytes in the CPU memory.

		first byte								second byte								
	bit	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
line	byte																	byte
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	3	0	1	1											1	1	0	2
2	5	0	1	1	1										1	1	0	4
3		0	1	1	1	1									1	1	0	
4		0	1	1		1	1								1	1	0	
5		0	1	1			1	1							1	1	0	
6		0	1	1				1	1						1	1	0	
7		0	1	1					1	1					1	1	0	
8		0	1	1						1	1				1	1	0	
9		0	1	1							1	1			1	1	0	
10		0	1	1								1	1		1	1	0	
11		0	1	1									1	1	1	1	0	
12		0	1	1										1	1	1	0	
13		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
14		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	
15		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	

Figure 4: A possible design of the capital letter N.

Fig. 4 shows the correlation between the character image in the CPU memory and the representation on the screen. Second and first byte refer to the location in the CPU memory. The dots are displayed from left to right.

Fig. 4 also shows some good design rules for character patterns:

1) To get proper separation from surrounding characters on the screen, make sure to keep the bits indicated with "0" clear when not graphics.

2) Regarding the frequency response of the CRT: make sure always to concate at least two "ones" on same line, when a dot is required, to maintain uniform "dot-intensity".

The bits marked with "x" are "don't cares", as they are never displayed.

The shadow font is intended for underlining or other marking of character positions.

To be able to disable "shadowing", you will have to load one of the four shadows with zeroes.

2.6 Attribute Memory 2.6

The attribute memory may be loaded with 32 different combinations of the attribute bits Att(0:7). The five most significant bits Ch(11:15) from the screen refresh memory are used to select one of the 32 attribute combinations to control the display of the character.

The 32 combinations are loaded from the CPU memory by means of the DMA in the same order, in which they are organized in the attribute memory, i.e. corresponding to increasing value of ch(11:15).

Apart from selecting combinations, the most significant bit from the refresh memory Ch(15) also selects the blink frequence of the character. This has no effect, if Att(0:7) do not specify blink. If Ch(15) = 0, the frequency is 6 blinks/sec. else it is 3 blinks/sec.

The attributes Att(0:7) are used to control the display in the two modes specified in subsections 2.6.1 and 2.6.2.

2.6.1 Black & White 2.6.1

This mode is selected when Att(4:7) = 0.
In the B&W mode Att(0:3) have the following meaning:

Att(0): High intensity
Att(1): Non display
Att(2): Reverse
Att(3): Blink

If a colour screen is used, normal intensity is displayed as green and high intensity as white.

"High intensity" augments the intensity of the e-beam, when on.

"Non display" hides the character in the background, i.e. the character is invisible, unless blink is on.

"Reverse" reverses dots and background, i.e. dots become black and the background gets the selected intensity.

"Blink" has no effect if none of the other attributes are on.

If "Blink" is on together with one of the other attributes alone or with "High intensity" and "Reverse", the character will alternatingly be displayed with and without these attributes.

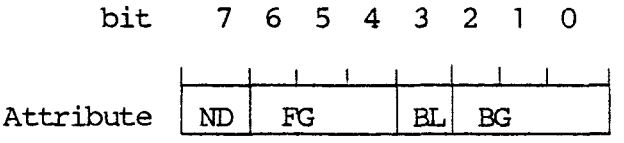
If "Blink" is on together with "Non display" and one or both of the other attributes, the display is alternatingly black and showing the character without the "Non display".

In the cursor position an extra blinking reversal is active. This blink frequency is selectable independent of the "attribute blink" (see section 2.2), and the blink is out of phase (unpredictable how much) with the "attribute blink".

2.6.2 Colour

2.6.2

In Colour mode the attribute byte is divided into four fields:



Att(7): Non Display
Hides the character in the background when on

Att(4:6): ForeGround colour select
values 1 to 7 are valid, selects the colour of the character dots

Att(3): BLink
when on, the character is alternatingly displayed and non displayed

Att(0:2): BackGround colour select
values 0 to 7 are valid

The following table gives the correspondence between the values of the colour select fields and the colours displayed, or the intensity if no colour CRT is installed.

colour select	colour	intensity
0	black	black
1	blue	very low
2	red	low
3	pink	reduced
4	green	normal
5	turquoise	increased
6	yellow	high
7	white	very high

Selecting same non-zero colour code in foreground and background gives black dots on the selected background (provided ND is off).

2.7 Video Blocking Flip-Flop 2.7

This Flip-Flop is used to blank the entire display. The Flip-Flop is initially set to prevent curious light effects.

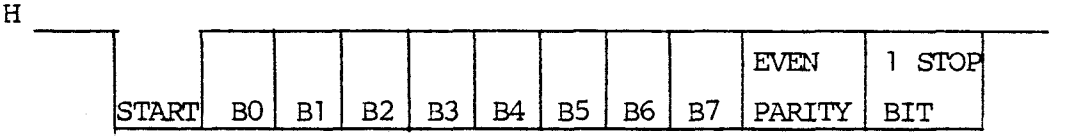
The data sent to the IO port $2C_{16}$ should have
bit 2 = 1 for set blanking bit 2=0 for release blanking
the remaining 7 bits are dummy.

3. HOW TO HANDLE THE KEYBOARD MODULE 3.

The keyboard is connected to a Z80 SIO2 channel B, confer data sheet for further information. The line speed 300 b/s asynchronous is set by a clock of 19199 Hz and a SIO clock of 1/64.

3.1 Keyboard SIO Initialization 3.1

The SIO should be in Asynchronous receive mode, with the following format:



Set write registers

The registers are addressed by setting a pointer in write register 0.

The write registers 2, 3, 4, and 5 shall have the following content, and should be set in the shown sequence

w2 Set interrupt vector

w4

Bit 7	6	5	4	3	2	1	0
1	1	0	0	0	1	1	1

clock x 64 1 stop bit even parity

w3

1	1	0	0	0	0	0	1 (receive)

8 bits/char

w5

DTR	1	1	0	1	0	0	0

DTR: 0 async, 1 sync, other SIO
1: 8 bits/char
1: transmit
0
1
0
0
0

w1

0	0	0	1	0	1	1	1

1: receive interr
0
1: Vector interr
1: Transm interr.
1: External interrupt

Note:
w5 (write register 5) is used for letting DTR (bit 7) determine if the line Interface SIO channel should be asynchronous = 0 or synchronous = 1.

w1 (write register 1) CTS is used to generate a Real time clock interrupt every 20 msec (16.67 msec in 60 Hz Displays).

Output format
The commands are sent to the SIO as follows:

.set register address in w0
.set register A to the wanted value of address register
.out 31

This is done for all used registers.

3.2 Keyboard Initialization 3.2

For each keyposition on the keyboard the key will deliver a pre-defined binary code or ascii code when it is pressed.
If a code is wanted when the key is released too, this code must be initialized. There can at most be 15 such keyes.

The initialization is done as follows:

	Bit 7							Bit 0	
byte 1:	1	1	0	0	0	0	0	0	INITIALIZE

byte code 3

	Bit 7							Bit 0	
byte 2:									

Key position number

The whole sequence must be repeated for each key (max. 15 times)

	Bit 7							Bit 0	
byte 3:									

wanted value on release of key

```
lda  'byte 1' ;
out  31       ;
lda  'byte 2' ;
out  31       ;
lda  'byte 3' ;
out  31       ;
```

If more than 15 double keyes are defined, the last 15 are used.

3.3 Keyboard Input 3.3

Read from keyboard will give a code depending on the key depressed cf. Fig. 5.

single code key:
key depressed : code 1 (1 byte)
key released : none

double code key:
key depressed : code 1 (1 byte)
key released : code 2 (1 byte)

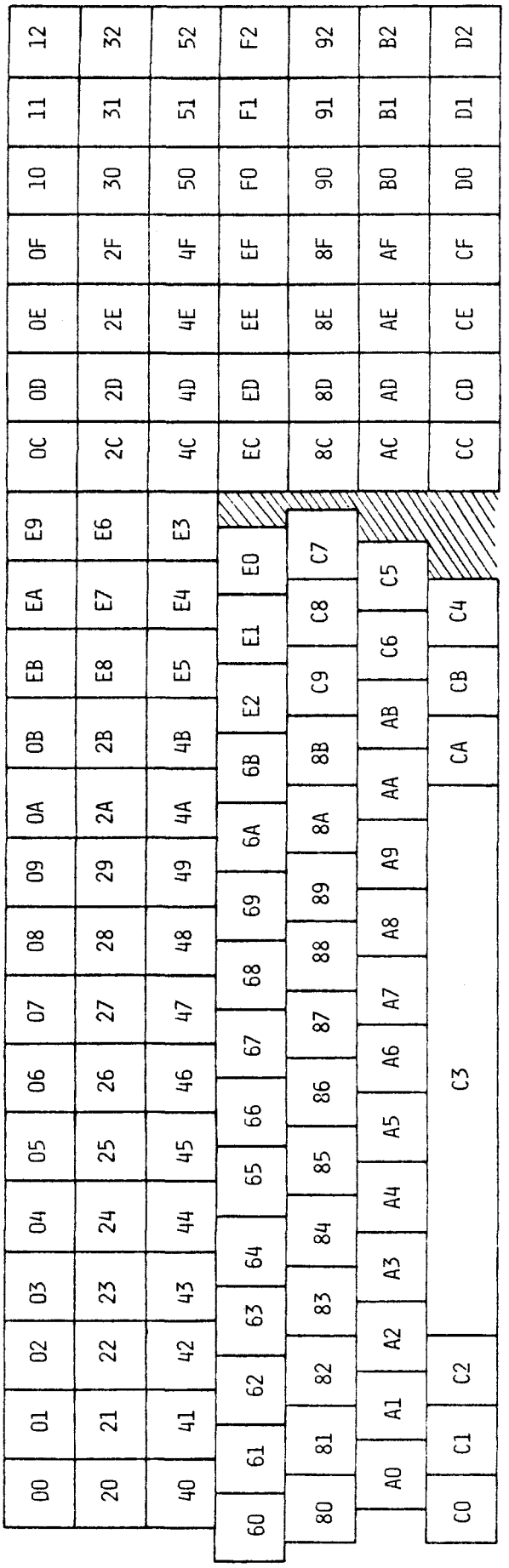


Figure 5: Output codes, HEX values.

where code 1 is given from the hardware and code 2 is the value defined in the initialization
The read is performed with

in 31

3.4 Keyboard Output 3.4

To the keyboard two kinds of output can be performed.

.set/clear lamp

.set/clear audio circuit on

One or more of the following 3 bytes are used to send this data to the keyboard.

byte 1:

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	1	2	3	4	5	0	0
lamp no.						byte code 0	

byte 2:

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
6	7	8	9	10	11	1	0
lamp no.						byte code 1	

byte 3:

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
12	13	X	15	X	X	0	1
lamp no.			AUDIO CIRCUIT			byte code 2	

For all bits: 1 = ON, 0 = OFF

Only the relevant byte should be transmitted

Audio circuit on/off is set/cleared by using a byte with byte code 2. bit 3 in this word selects the audio circuit.

Lamp on/off

The different lamp positions are shown in fig. 6.
The lamp can be placed Hardware-wise in any of the number position shown. The lamp is set on/off by writing byte 1, byte 2 or byte 3 depending on the lamp number.

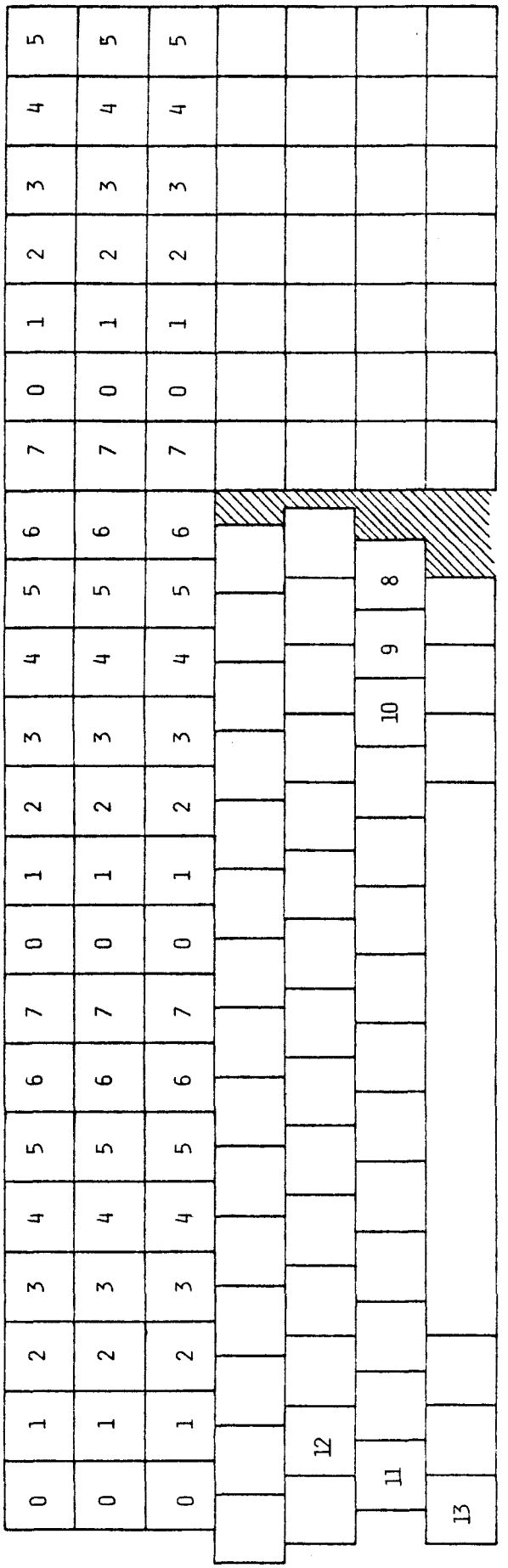

5 5 5
4 4 4
3 3 3
2 2 2
1 1 1
0 0 0
7 7 7
6 6 6
5 5 5
4 4 4
3 3 3
2 2 2
1 1 1
0 0 0
7 7 7
6 6 6
5 5 5
4 4 4
3 3 3
2 2 2
1 1 1
0 0 0
8
9
10
12
11
13

Figure 6.

4. DMA CONTROLLER 4.

The DMA controller has 4 independent channels used for Display, RC-CIRCUIT and options (Floppy).
Here follows a short description of the chip, for further information refer to the Am9517 or INTEL 8237A-5 datasheet.

4.1 DMA Initialization 4.1

The DMA controller contains the following registers:

Register name	Size in bits*no	Use	Access port HEX
Base addr reg.	16*4	Base address of transfer	WRITE: F0+channel#x2
Base word count	16*4	Byte count of transfer	WRITE: F1+channel#x2
Current addr	16*4	Address used during transfer Incremented/decremented	READ: F0+channel#x2
Current word count	16*4	Number of byte transfers incremented/decremented	READ: F1+channel#x2
Temporary addr	16*4	Memory to memory transf.	
Temporary word count	16*4	Memory to memory transf.	
Status	8*1	Status of all channels	READ F8
Command	8*1	Controls operation of DMA	WRITE F8
Temporary	8*4	Used for Memory to memory transfer	READ FD
Mode	6*4	Determines the transfer mode of the channel	WRITE FB
Mask	4*1	Mask to disable requests set/Reset or write	WRITE: FA or FF

Register name	Size in bits	Use	Access port	HEX
Request	4	SW - DMA requests	WRITE	F9

4.2 Software Commands 4.2

Clear Internal First/Last Flip/Flop

Used to reset the Flip-Flop for byte addressing in address and count registers. Common to all channels.
Should be initialized before access to double byte registers.
Access WRITE FC

Master clear

Clears the following registers:
Command, Status, Request, Temporary.
Internal Flip/Flop, set:mask.

Access WRITE FD

Should be used when the DMA is initialized.

4.3 Base Addr Register, Base Word Count Register, Current Address and Current Word Count Register 4.3

These registers are read or written according to fig. 7.

Remember the internal Flip-Flop should be cleared before accessing a new byte pair.

To avoid malfunction of some earlier DMA controller parts it is recommended that Base addresses are set to an even address (LSB = 0).

The problem has been seen as the DMA-transfer to the display being halted before reaching terminal count (when the DMA-address crosses a 256 byte border).

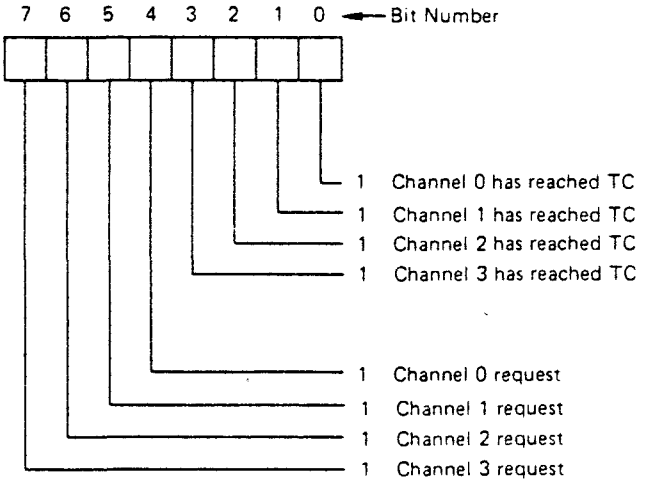
(fig. 7)

Channel	Register	Operation	Signals							Internal Flip/Flop	Data Bus DB0—DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base & Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base & Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base & Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base & Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base & Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

4.4 Status Register

The Status register contains information about the status of the device at the time of reading. This information includes which channels have reached terminal count and which channels have pending DMA requests. Bits 0-3 are set any time a TC is reached by a channel. These bits are cleared upon Reset and on Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service.

Addressing: in F8

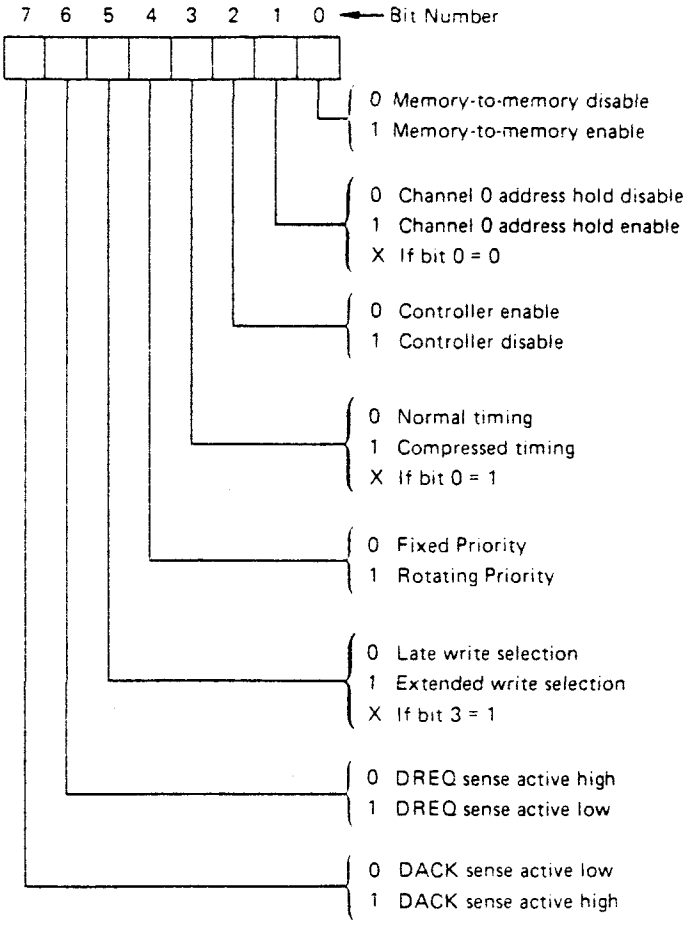


4.5 Command Register 4.5

This 8 bit register controls the operation of the DMA-controller. It is programmed by the microprocessor in the Program Condition and is cleared by Reset. The following table lists the function of the command bits.

All bits are normally initialized to 0. Bit 3, 6 and 7 MUST always be 0.

Addressing: out F8



4.6 Mode Register

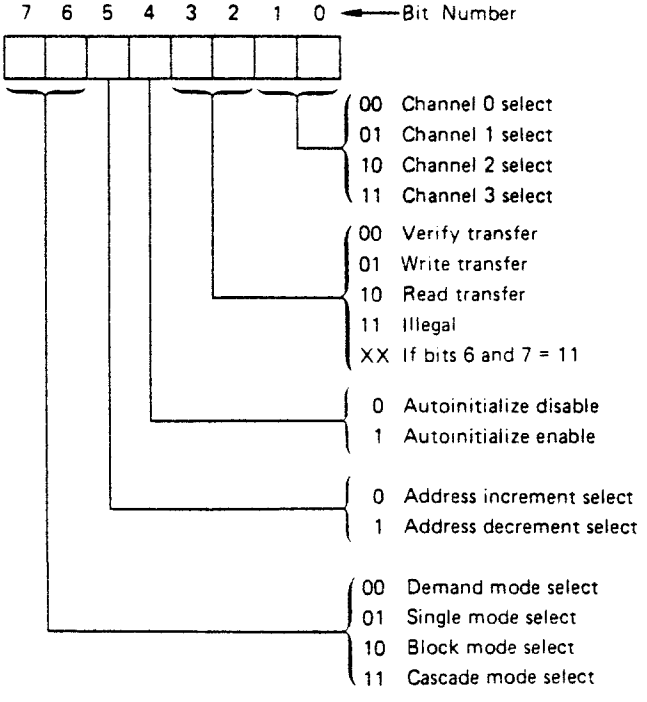
Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program Condition, bits 0 and 1 determine which channel Mode register is to be written.

Bit 6 and 7 is transfer mode select which is normally initialized to:

00: Demand Mode, for Display channel (CH 0)

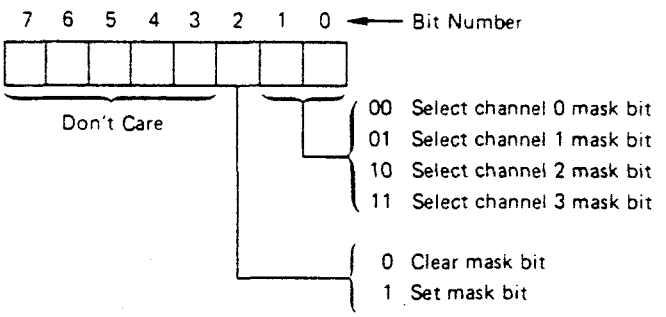
01: Single Mode, for CIRCUIT and FDC channels (CH 2, CH 1)

Addressing: out FB



4.7 Mask Register 4.7

Each channel has associated with it a mask bit which can be set to disable the incoming DREQ. Each mask bit is set when its associated channel produces an EOP if the channel is not programmed for Autoinitialize. Each bit of the four bit Mask register may also be set or cleared separately under software control. The entire register is also set by a Reset. This disables all DMA requests until a clear Mask register instruction allows them to occur. The instruction to separately set or clear the mask is similar in form to that used with the Request register.
Addressing: out FA



When the mask register is set the corresponding channel is disabled, this should be done when the registers associated with the channel are accessed. The mask register bit concerning a channel must be cleared before the channel is used for a transfer.

5. REAL TIME CLOCK 5.

A real time clock is generated as an interrupt on the CTS (clear to send) signal on the keyboard SIO each time this signal changes its logic level.

This interrupt signal is generated in the CRT-controller by dividing a signal at refresh rate by 2.

The real time clock frequency will be as follows:

Refresh rate	Real time clock frequency	Interrupt interval time
50 Hz	25 Hz	20 ms.
60 Hz	30 Hz	16.67 ms.

6. CIRCUIT OR COAX, KEYBOARD AND CLOCK SIO 6.

One SIO is used for CIRCUIT keyboard, clock and line mode control.

The IO port numbers are used as follows:

Port use	IO port number Hex.
Channel A, Data, CIRCUIT, 250 kb/s or COAX, 540 kb/s	30
Channel B, Data, KEYBOARD, 300 b/s	31
Channel A, Control (RTS and DCD)	32
Channel B, Control (CTS and DTR)	33

6.1 Channel A 6.1

Channel A is used for either the CIRCUIT or the COAX transmission line, which ever is installed.

6.1.1 CIRCUIT 6.1.1

To drive a CIRCUIT interface the SIO channel A should be programmed for SDLC operation and for DMA operation. Initialization of Write Registers:

WR 1: D7 - set when Ready (DMA req) should be enabled
D6 - always 1
D5 ... D0 - as required

WR 3: D7, D6 - 1,1, Rx 8 bits/character
D5 ... D0 - as required

WR 4: D7 ... D0 - 20 hex. x1 clock, SDLC, SYNC, no parity mode

WR 5: D7 - DTR is used for gating Clock Fail signal to DCD input of SIO
0: disables clock fail (DCD always 1)

1: enables clock fail sense
(DCD = 0 if clock pulses exist on the circuit line and DCD = 1 if the line is silent)

D6, D5 - 1,1, Tx 8 bits/character

D4, D3 - as required

D2 - always 0

D1 - RTS enables CIRCUIT transmitter to control the line. It should not be enabled until the CIRCUIT line is silent

D0 - as required

WR 6: Receive/Transmit address

WR 7: D7 ... D0 - Flag = 7E hex.

For further information on SIO operation refer to Z80A - SIO/2 Technical Manual from ZILOG.

SIO/DMA Operation

Preparing for a DMA transfer requires a sequence of initializations to take place. SIO, DMA controller and a DMA request flip/flop must all be initialized in a way that meets the following requirements:

1) The SIO must be in a state where it does not activate its READY signal

2) The DMA request flip/flop can then be reset by an OUT 34 hex.

3) DMA controller channel 2 is set as required by the next transfer

4) SIO is enabled to Receive or Transmit

DMA - Interrupt Interaction

When receiving and a character is assembled in the SIO it generates both an interrupt and a DMA request. The CPU responds to the interrupt with an interrupt acknowledge and gets an interrupt vector from the SIO. If, however, (as often happens) the DMA con-

troller reads the receive buffer before the CPU acknowledges interrupt then no vector will be sent by the SIO. Instead a "dummy" device at the end of the priority chain generates an interrupt vector (0C hex.).

6.1.2 COAX

6.1.2

To drive the COAX-interface, the SIO channel A should be programmed to

x1 clock mode and
asynchronous mode.

The signal on the COAX is composed by clockpulses and datapulses: the clockpulses indicate the beginning of the bittime (approx. 1.85 µsecs.) in the middle of which a datapulse may occur.

datapulse present means 0
datapulse not present means 1

All the pulses have a duration of approx. 240 nsecs., and an amplitude of approx. +8 volt into 95 Ohm.

If RTS is set prior to a transmission, the transmission of clockpulses will start with the first transmitted startbit.

RTS should be cleared as early as possible after the last character to be transmitted is loaded into the transmit buffer.

DCD follows RTS. If RTS is cleared while a transmission is going on, DCD is not cleared until the transmission is finished (the transmit buffer is empty).

On a correctly terminated coaxline, the transmitted data will not be looped back into the receive buffer of the transmitting station. However, a loop back test may be carried out by reflecting the transmitted data back to the receiver by means of approx. 40 meter openended coaxcable or a 200 nsecs. openended delayline connected to the coax interface.

6.2 Channel B

Channel B is used for the keyboard input/output.
The received clock 19199 Hz should be divided by 64 to give the 300 baud data rate.

CTS (Clear to Send) is used to generate a Real time clock interrupt every 20 ms from a 25 Hz clock (16.67 ms., 30 Hz in 60 Hz version). An interrupt is generated every time CTS change value.

The clock interrupt is sensed as follows:

. Set 'status affects vector' bit in write register 1.

. When interrupt occurs:
  Read register 0.
  If CTS has changed value the interrupt was a clock interrupt.
  Reset external interrupt with write register 0.

DTR (Data Terminal Ready) is used to control the clockswitch on the line and printer SIO, channel A.

The DTR bit in write Register 5 should be set as follows:

bit 7 = 0 Asynchronous transmission
bit 7 = 1 Synchronous transmission

cf. section 3.1.

7. LINE, PRINTER SIO 7.

An SIO and a 4 bit input port is used for LINE (asynchronous or synchronous) and printer (asynchronous) interface.

The I/O port numbers are used as follows:

Port use	I/O port number
Channel A, Data, LINE	08
Channel B, Data, Printer	09
Channel A, Control	0A
Channel B, Control	0B
4 bit input port, CI, DSR for LINE and printer	1C

7.1 Channel A 7.1

Channel A is used for asynchronous, synchronous or X.21 communication. Asynch. or Synch. clocks is selected by the DTR output of the Keyboard SIO. The asynchronous baud rate clock is derived from the CTC channel 0 (Port 0C hex.).

X.21 operation uses the modem signals in the following way:

- I signal is sensed by the CTS input
- DTR controls the C-signal
- R signal is connected to receiver input but can also be sensed by the DCD input
- RTS gates TXD to the T-output as follows:
  RTS = 0: T always 0
  RTS = 1: T = transmitted data.

7.2 Channel B 7.2

Channel B is used for asynchronous communication with a printer.

Its baud rate clock is derived by the CTC channel 1 (Port address 0D hex.).

7.3 4 Bit Input Port

In addition to the modem signals monitored by the two SIO-channels, a 4 bit input port (address 1C hex.) senses the state of CI and DSR from both channels. The port input is as follows:

bit no. (0 = LSB)	Signal
0	CI (Calling Indicator), LINE, CH A
1	DSR (Data Set Ready), LINE, CH A
2	CI, printer line, CH B
3	DSR, printer line, CH B
4-7	Undefined

8. CTC, COUNTER TIMER CONTROLLER 8.

The CTC contains four counter timers used in the following way:

Port use	I/O port number, hex.
Channel 0, Baud rate clock for LINE SIO, CH A	0C
Channel 1, Baud rate clock for Printer SIO, CH B	0D
Channel 2, Display interrupt	0E
Channel 3, Option interrupt (floppy disc)	0F

Channel 0 and 1 are used as counters and have their interrupt disabled. Their clock input is a 614.4 kHz clock.

The division ratios required for in the CTC channel and the SIO can be found in the following table:

Baud rate	CTC divisor	SIO divisor
50	193	64
75	128	64
110	88	64
150	64	64
300	32	64
600	64	16
1200	32	16
2400	16	16
4800	8	16
9600	4	16
19200	2	16

The two interrupt channels are initialized to count down by 1 and then generate an interrupt. Channel 2, display is required to count on a negative edge, while channel 3 uses the positive edge.

For further information on programming the Z80A-CTC refer to the data sheet.

9. RAM/ROM CONFIGURATION 9.

A ROM decodes the 5 MSB address lines and determines the partition of address space between RAM and ROM when reading from memory. Writing to an address always writes to the corresponding place in the RAM-memory.

Besides the address inputs the decoder has 3 other inputs, one from HOLD ACK and 2 from a dual F/F. The ROM (ROB232) is coded so that DMA always enables RAM regardless of the F/F states. After RESET the first 56 K of memory is decoded as ROM and the last 8 K as RAM. By I/O instructions it is possible to select only the first 16 K as ROM or all memory as RAM, as shown in the following table:

OUT (addr.)	Function
18	Enable ROM 0-56 K
19	All RAM
1A	Enable ROM 0-16 K
1B	All RAM

The decoder ROM, ROB232 requires the ROM sockets to be strapped for 8 K byte ROM's, using other ROM sizes will require another decoder ROM.

10. NVM I/O PORT 10.

The Non Volatile Memory is a small memory of 21 words by 16 bit (NC7033) which retains its data after power is removed.

The NVM has 5 pins for serial interface, one clock, three command lines and a bidirectional data line for serial address and data. These lines are under program control from a parallel input/ output register (only bit 7 is input).

The register is reset at power up, which zeroes all outputs and thereby assures that the command inputs (PINS 4, 5, 6) receives a standby command (1,1,1) and that no programming voltage (-25 V) is applied to pin 1.
(Pin numbers refer to the NC7033 data sheet).

The register bits are used as follows:

BIT NO.	Description
0	Clock signal for NVM. Program is responsible for timing. Clock low time: more than 5 µsec. Clock high time: between 4 and 10 µsec.
1	Inverse of NVM command signal, pin 4.
2	If register bit 4 is high this signal is enabled and directly controls NVM signal C2 (pin 5). If register bit 4 is low as after reset then C2 is pulled high.
3	Controls NVM signal C3 (pin 6) if register bit 4 is high. (Similar to bit 2).
4	Enables register bit 2 and 3 to control NVM (C2, C3) if high. If low then both C2 and C3 are pulled high.
5	Enables program voltage (-25 V) to NVM pin 1 if high. After enableing at least 200 ms. should be allowed for the voltage switching circuit to turn on.

BIT NO.	Description
6	Data direction control. HIGH: enables data out to NVM. LOW: allows reading data from NVM.
7	Data out to NVM pin 8 if direction out is selected. Data in from NVM pin 8 if direction in is selected.

More detailed information on operation of the NVM (NC7033) can be found in the data sheet in chapter 9 of RCSL No 44-RT2043: MIC 507/508 Technical Manual or RCSL No 44-RT2044: MIC 509 Technical Manual.

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