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Author: Mogens V. Pedersen

Title:

FDI501 and FDI502 Floppy Disk Interface Technical Manual

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Keywords:

RC850, RC855, FDI501, FDI502.

Abstract:

This manual contains a technical description of the FDI501 and the FDI502 Floppy Disk Interface to the RC850 system.

(44 printed pages)

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1. DESCRIPTION 1.

The FDI501 and FDI502 Floppy Disk Interface are controller boards to the RC850 system. The controller may be connected to the microcomputer board housed in RC850. Connection to the floppy disk drive is made using the cable CBL960 which makes a standard connection for floppy disk drives used in the RC700 and RC850 systems.

This manual contains the following main parts:

Floppy Disk Interface
Optional Parallel Interface
Signal Cables

Note: FDI501 and FDI502 have the same format, fit and function. FDI502 is a new print layout which removes the FCO20-005.

In FDI502 the switches are replaced with wrappings and removable shorts.

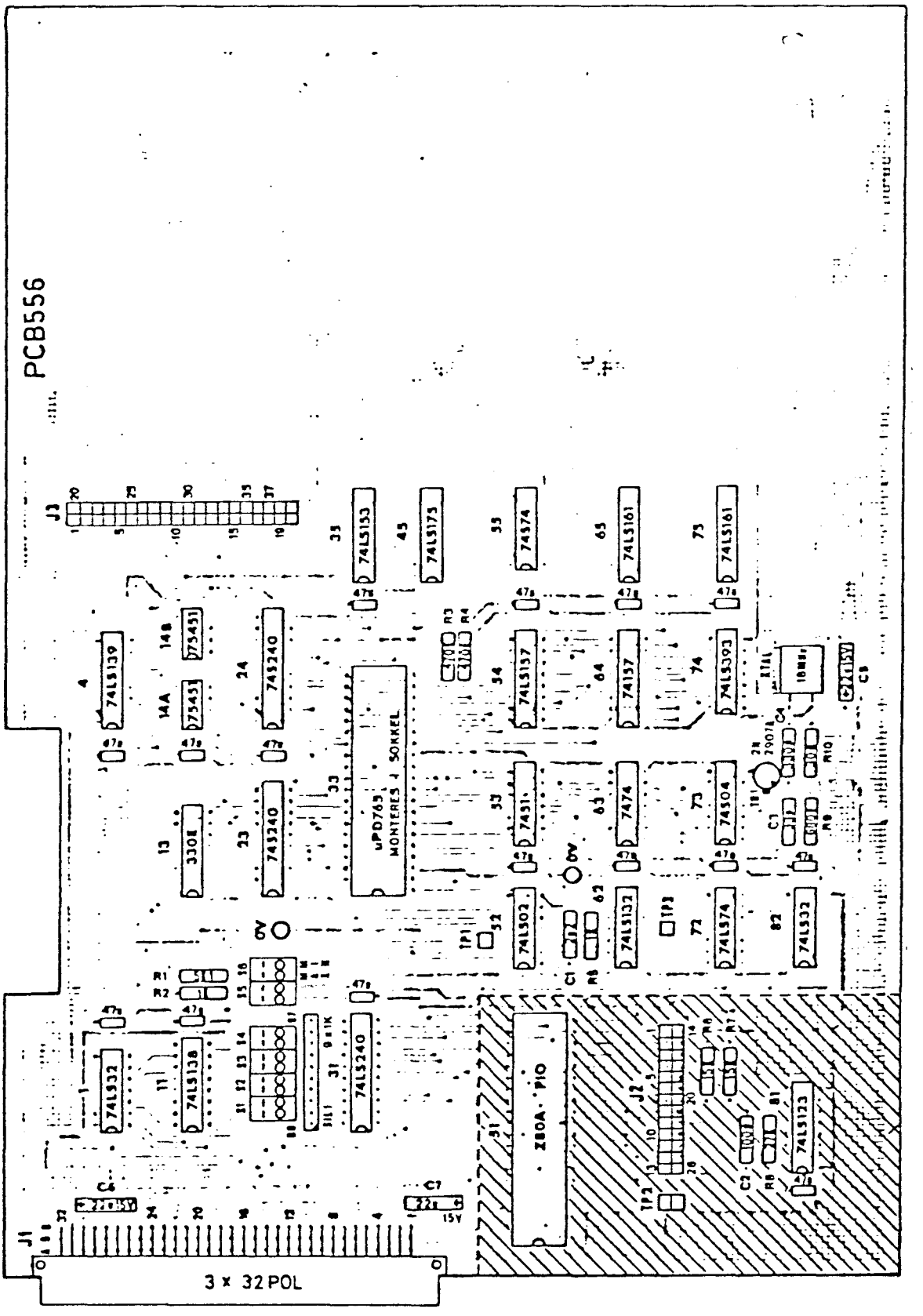


Fig. 1. FDI 501 BOARD LAYOUT.

2. FLOPPY DISK INTERFACE 2.

2.1 General Description 2.1

The FDI501 and FDI502 are built on single circuit boards. They are connected to J1 on the microcomputer board housed in the RC850. Through this connector the power to the board is supplied. FDI501 needs the following power: +5 V. Typical power consumption: 0.6 A.

The board layout is shown in fig. 1.

2.2 Block Diagram 2.2

Fig. 2 shows a block diagram for FDI501 and FDI502. In the diagram is shown, where each block is found in the circuit diagrams.

2.3 Functional Description 2.3

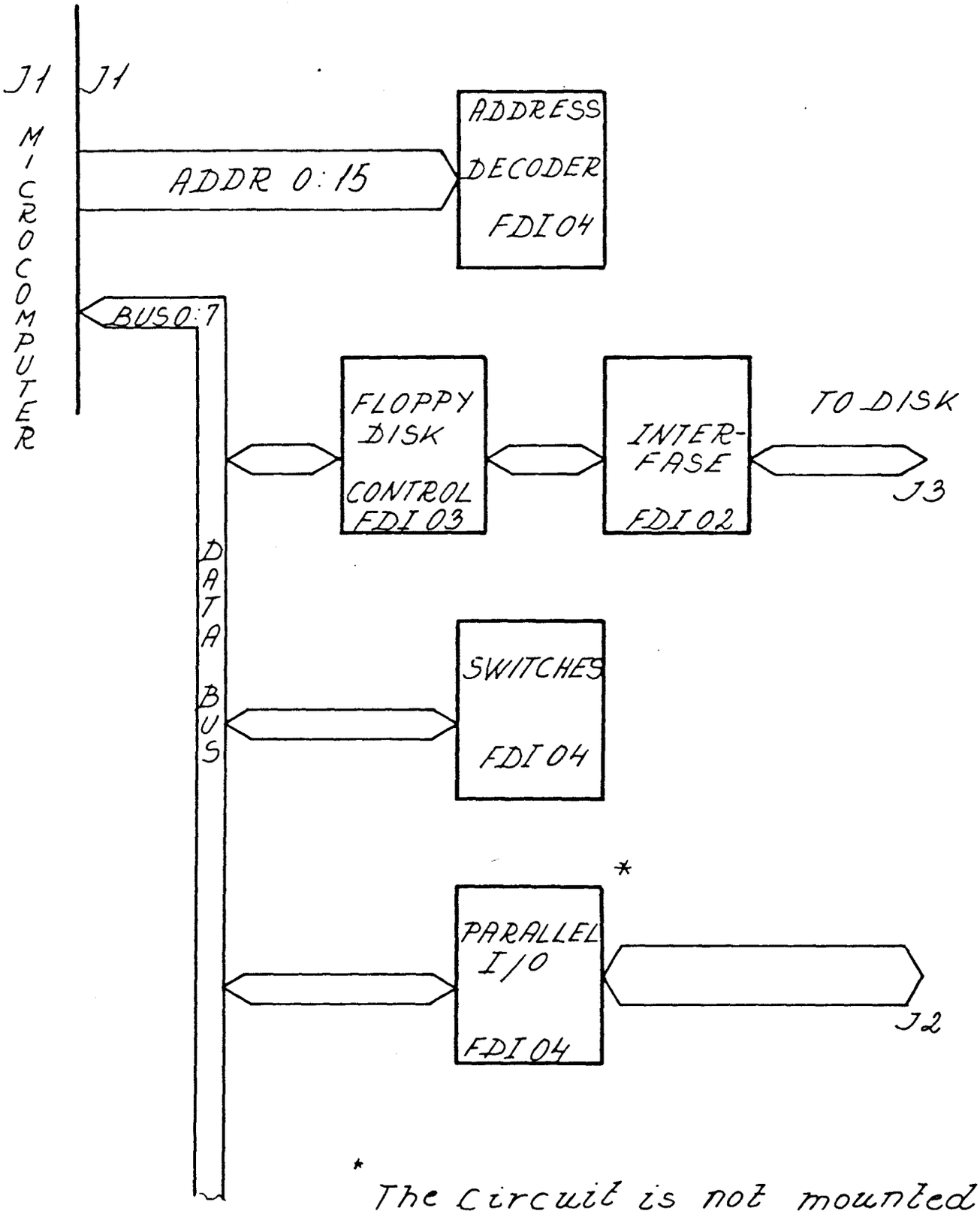
The functional description follows the block diagram. This paper does not contain a full description of all the functions of the VLSI circuits used. This kind of information may be supplied by the manufacturers of the VLSI circuits.

2.3.1 Address Decoder 2.3.1

The addressing of the devices is made very simple with the circuits shown in diagram page FDI04. Each device uses 4 addresses as shown in fig. 3.

2.3.2 Floppy Disk Controller 2.3.2

The floppy disk controller to FDI501 and FDI502 is based on the FDC chip uPD765 from NEC or 8272 from Intel. The chip contains the circuitry and control functions for interfacing the processor to 4 floppy disk drives. It supports both IBM3740 single density



* The circuit is not mounted in FDI 501.

Fig. 2. Block Diagram for FDI 501.

Address No.	Name	IC type	Comments
00	DISP	I 8275	PARAMETER PORT
01	-		COMMAND PORT
02	-		
03	-		
04	FLOP *	μPD 765	MAIN STATUS REG
05	-		DATA REG
06	-	or I 8272	
07	-		
08	SIO	Z 80A - SIO2	DATA CHANNEL A
09	-		DATA CHANNEL B
0A	-		CONTROL CHANNEL A
0B	-		CONTROL CHANNEL B
0C	CTC	Z 80A - CTC	CHANNEL 0 to SIO A
0D	-		CHANNEL 1 to SIO B
0E	-		CHANNEL 2 INT DISP
0F	-		CHANNEL 3 INT FLOP
10	PIO *	Z 80A - PIO	DATA KEYBOARD
11	-		DATA PARALLEL I/O
12	-		CONTROL KEYBOARD
13	-		CONTROL PARALLEL I/O
14	SWITCH		INPUT: 8 bit from switch
15	- *		
16	-		OUTPUT: ENABLE MOTOR
17	-		AND SELECT FLOPPY TYPE
18	DIS PROM		
19	-		
1A	-		
1B	-		
1C	SOUND		
1D	-		
1E	-		
1F	-		

* Used in FDI 501

Fig. 3. Address Decode in FDI 501.

format (FM) and IBM system 34 double density format including double sided recording.

Fig. 4 shows a block diagram for the controller chip.

The uPD765 contains two registers which may be accessed by the program. The 8-bit main status register contains the status information of the FDC and may be accessed at any time. The 8-bit data register (actually consists of several registers in stack with only one register present to the bus at a time), stores data, commands, parameters and floppy disk drive information. Fig. 5 shows the information stored in the status register.

Fig. 6 shows the information to and from the data register during a read or write instruction to the controller. The programming of uPD765 is very complex and is described by the manufacturer. The controller interfaced to both Maxi- and Mini disc drives. The circuits on diagrams FDI02 and FDI03 show this.

Fig. 7 shows the data media floppy disk. The diskette contains a number of tracks which again are divided into a number of sectors as shown in fig. 8. The controller is able to format, read or write the diskette. Information about the actual formats used is available in the software manuals. Fig. 9 shows the two recording methods used.

2.3.3 Strapping FDI501 and FDI502 2.3.3

Besides the 8 switches selectable for the program using the device code 14(Hex) (see subsection 2.3.2), FDI801 contains 4 other switches. The way to strap them is shown in fig. 10.

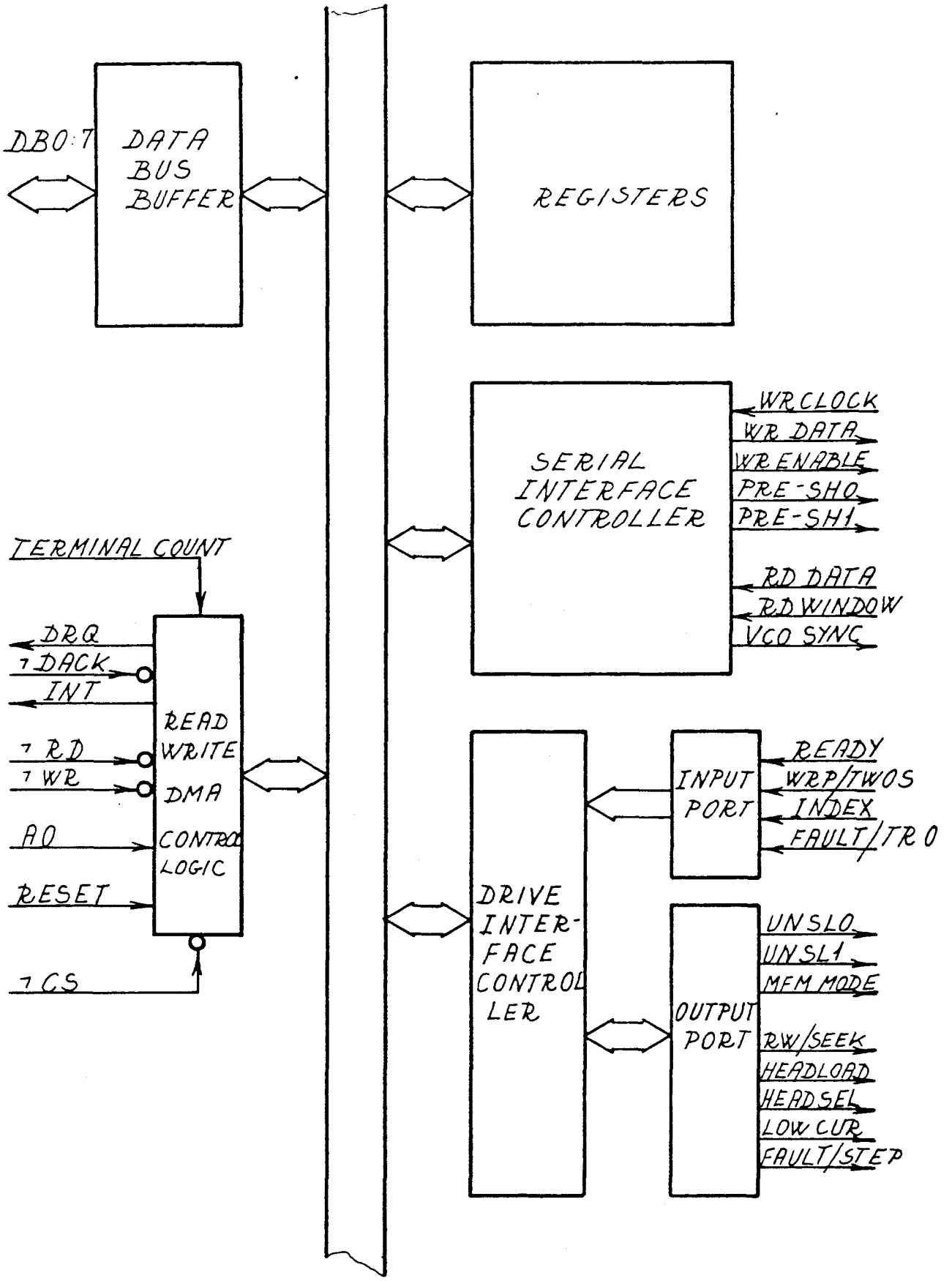
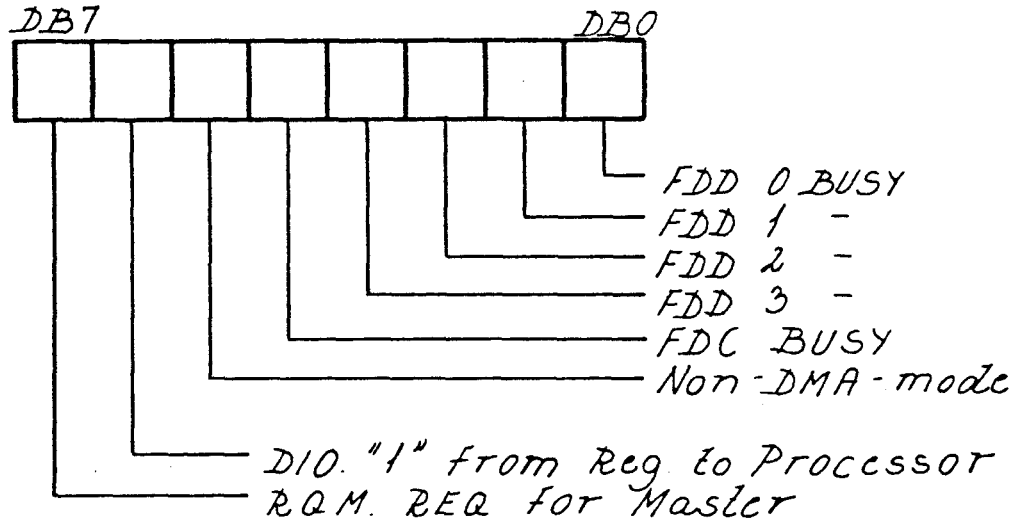
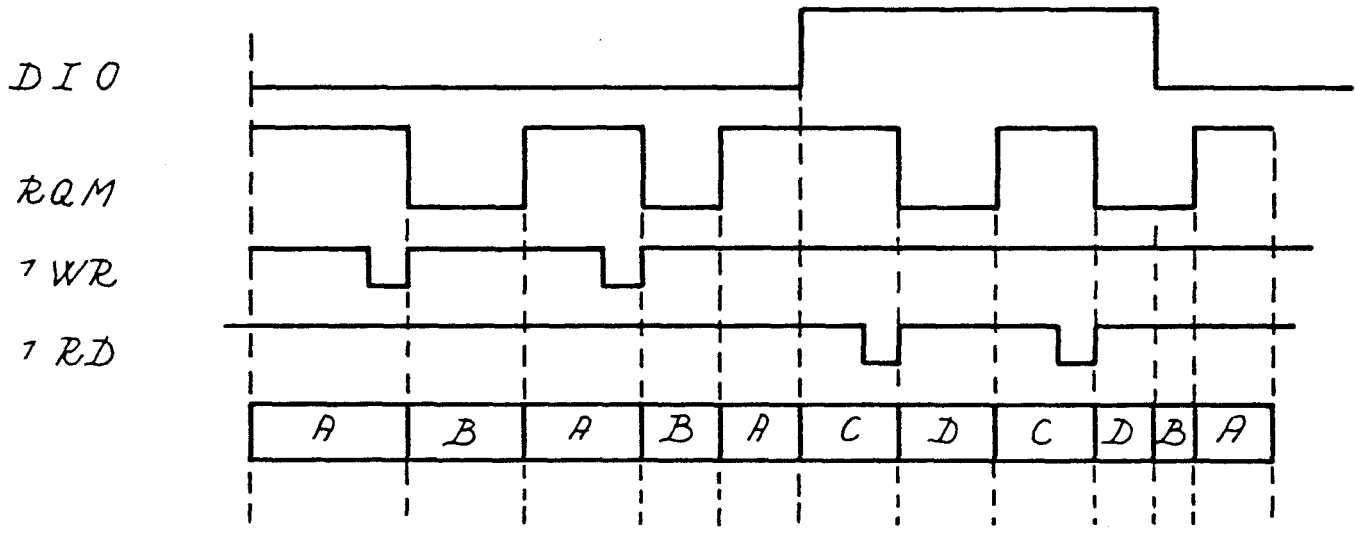


Fig. 4. BLOCK DIAGRAM FOR μ PD 765 FLOPPY DISK CONTROLLER CHIP.

STATUS REGISTER (MAIN STATUS REGISTER)

One 8-bit byte with inf. of the controller.





A Data register ready to be written into by CPU

B - - not ready - - - - - -

C - - ready for next byte to be read

D - - not ready - - - - -

Fig. 5. STATUS REGISTER IN μPD 765.

Data Register of 8-bit bytes
(Several registers in a stack)
All commands contains a command phase, an execution phase and a result phase.

PHASE	R/W	DATA BUS D7 D6 D5 D4 D3 D2 D2 D0	REMARKS
READ DATA			
Command	W	MT MF SK 0 0 1 1 0	
	W	X X X X X HD US1 US0	
	W	Cylinder number (current)	
	W	Head address	
	W	Record (Sector number)	
	W	Number (of data bytes/sector)	
	W	End of track	
	W	Gap Length	
	W	Data Length	
Execute			
Result	R	Status 0	
	R	- 1	
	R	- 2	
	R	Cylinder number (current)	
	R	Head address	
	R	Record (sector number)	
	R	Number (of data bytes/sector)	

Fig. 6. INFORMATION SUPPLIED TO AND FROM DATA REGISTER IN μPD 765 DURING READ OR WRITE

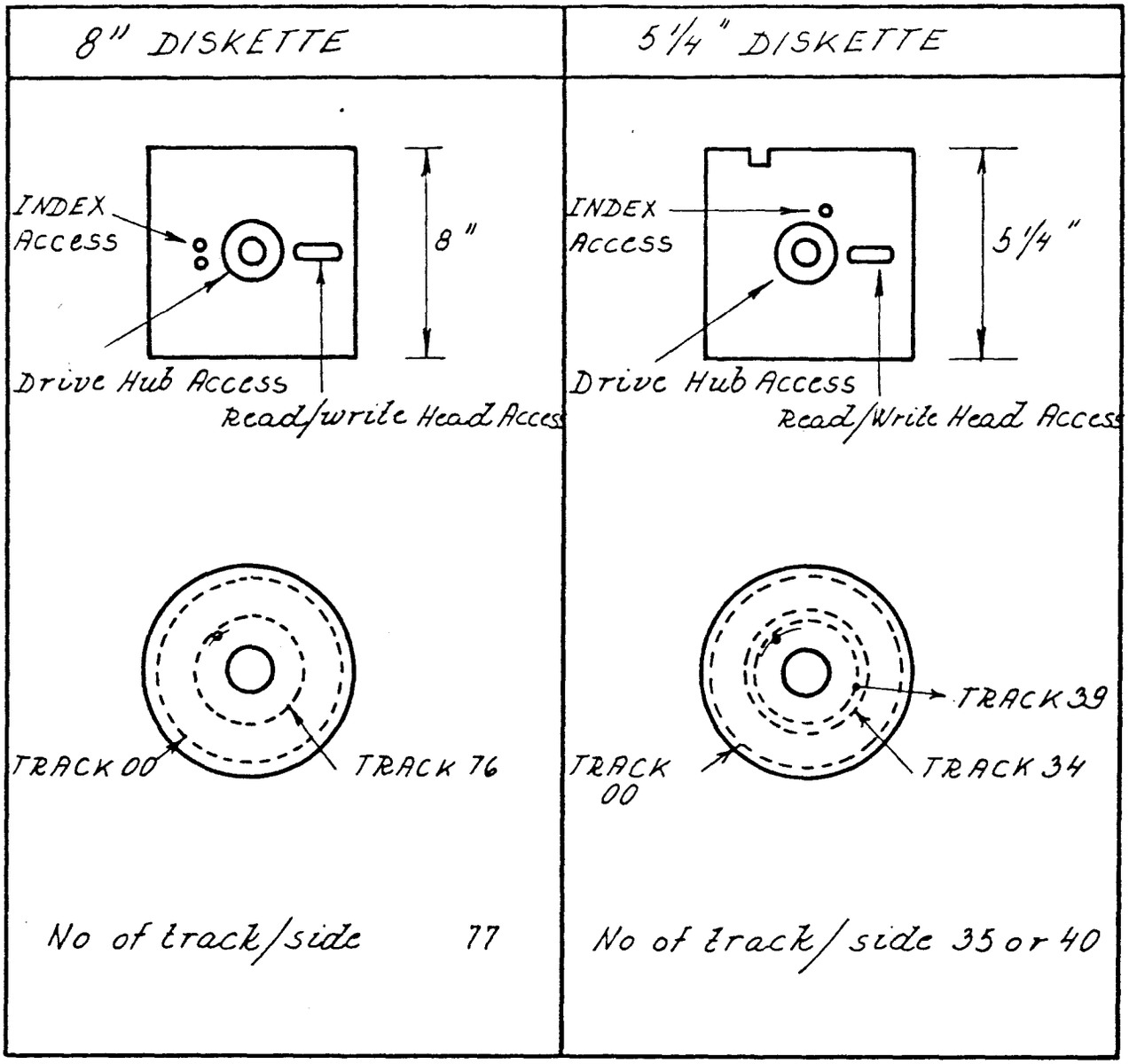
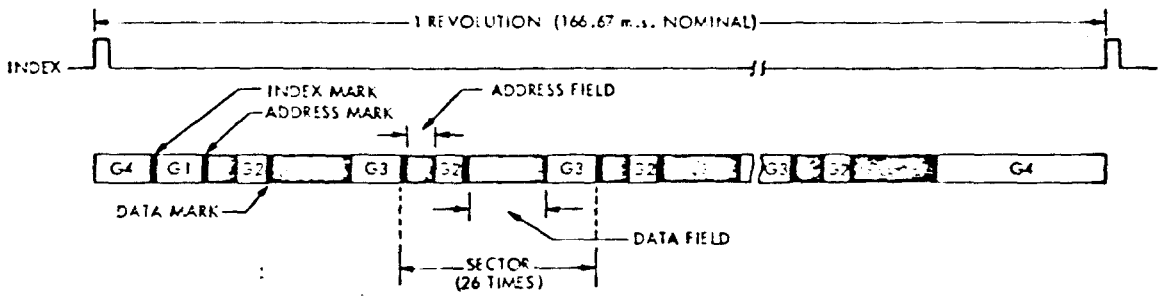
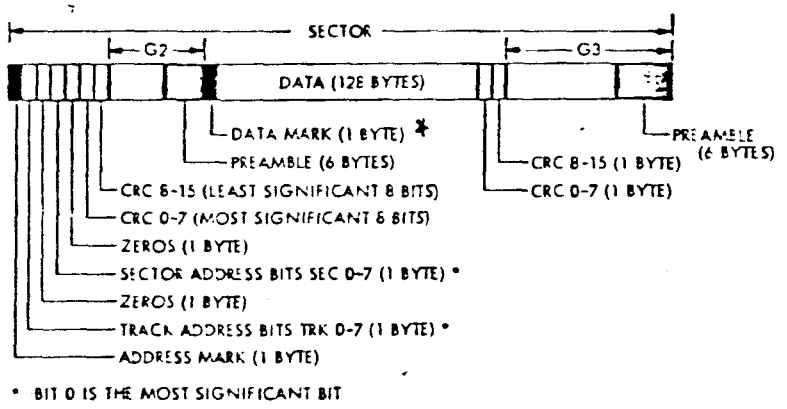


Fig. 7. FLOPPY DISK DATA MEDIA.



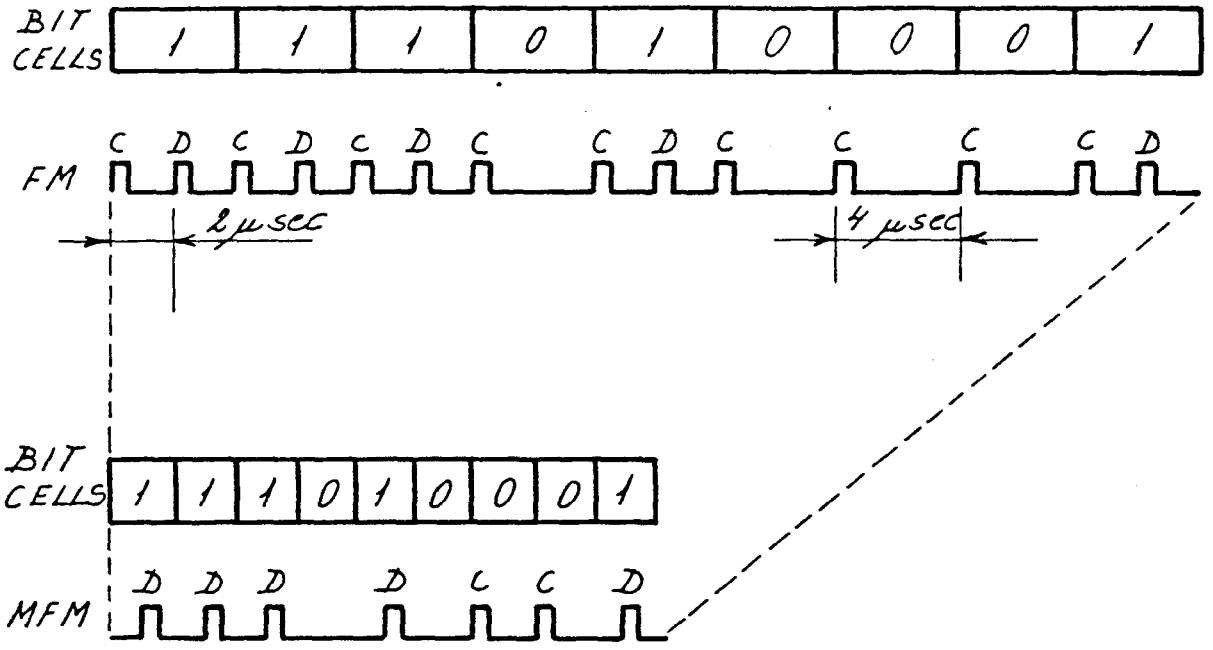


GAP FIELDS

G1 = 26 BYTES HEX FF
6 BYTES HEX 00
G2 = 11 BYTES HEX FF
6 BYTES HEX 00
G3 = 27 BYTES HEX FF
6 BYTES HEX 00
G4 = 314 BYTES HEX FF
6 BYTES HEX 00

* DATA MARK is also called 'Data Address Mark'

Fig. 8. Information stored on one Track of a Diskette. The Example here shows a 8" Diskette.

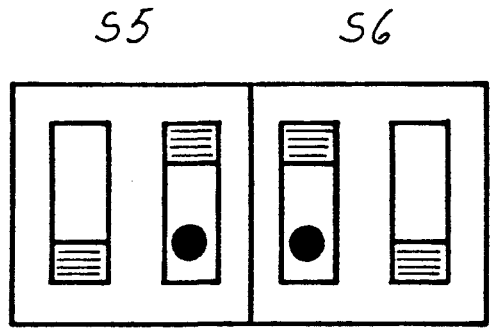


D ~ Data Pulse
C ~ Clock

FM is also called single Density.
MFM - - - double -

	8" DISK		5 1/4" DISK	
	FM	MFM	FM	MFM
Bit Cell	4 μs	2 μs	8 μs	4 μsec
Flux Changes/Cell	2	1	2	1
- - /Inch	6536	6536	2728	5456
Kilo Bits/sec	250	500	125	250
Frecuency Ratios	2/1	2/1	2/1	2/1
Bit to Bit spacing	2 μs 4 μs	2 μs 3 μs 4 μs	4 μs 8 μs	4 μs 6 μs 8 μs

Fig. 9. RECORDING METHODS OF FLOPPY DISKS.



RED DOT VISIBLE • ON

ON ~ MINI FLOPPY SELECTED

ON ~ MAXI FLOPPY SELECTED

BOTH OFF ~ THE PROGRAM SELECTS MINI OR MAXI FLOPPY. AFTER RESET IS MINI FLOPPY SELECTED.

ON ~ SWITCHES ON FDI 501 (DEVICE NO. 14 (HEX)) IS USED. SWITCHES ON THE CPU BOARD USING THE SAME DEVICE NO SHOULD BE DISCONNECTED.

SWITCH SHOULD BE ON, WHEN A MINI FLOPPY WITHOUT READY SIGNAL IS USED.

Fig. 10. STRAPPING FDI 501.

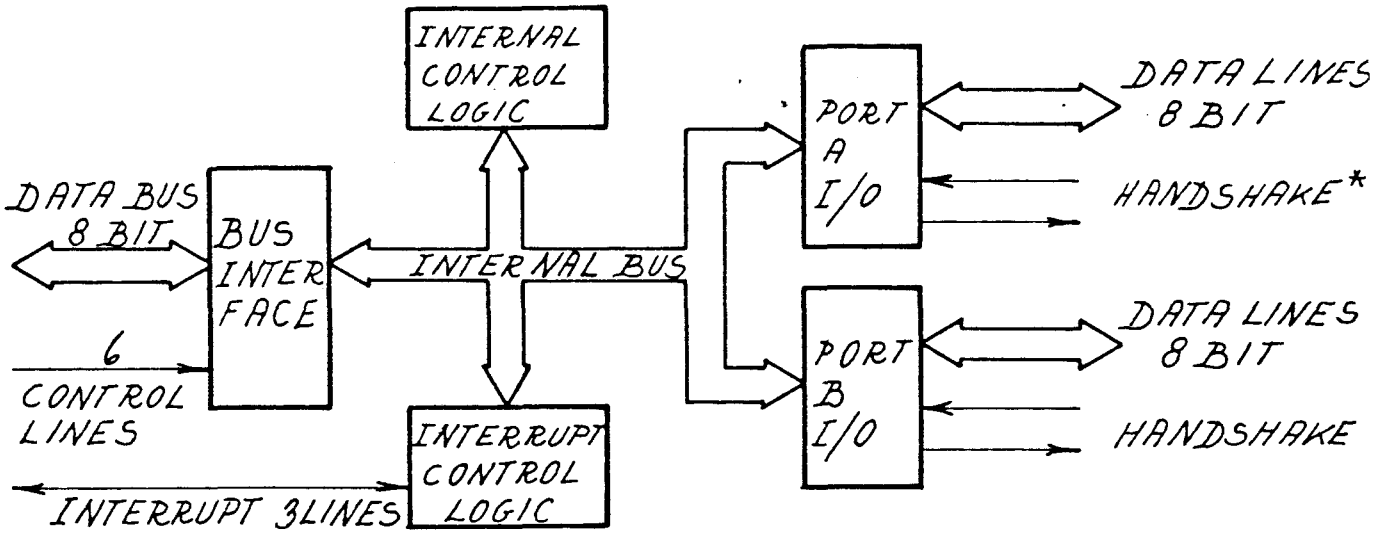
3. OPTIONAL PARALLEL INTERFACE

The layout of FDI501 and FDI502 is prepared for connection of a parallel interface. Although the IC's are not mounted, the following description of the circuit is contained in this paper. The Z80A parallel I/O (PIO) interface controller is a programable, two port device which provides interface between the CPU and the connector J2 for parallel I/O. The diagram is shown on page FDI04. The block diagram is shown in fig. 11. The internal structure of the Z80A-PIO consists of a bus interface, internal control logic, port A I/O logic, port B I/O logic and interrupt control logic.

Each of the two port I/O logic is composed of 6 registers. The registers include: an 8-bit input register, an 8-bit output register, a 2-bit moderegister, an 8-bit mask register, an 8-bit input/output select register and a 2-bit mask control register.

Before using the PIO it has to be programmed to the wanted Interrupt Vector and operating mode. This is described in manuals from Zilog.

The timing diagram in fig. 12 shows input from a keyboard. The interrupt system is described in the manual for the microcomputer.



* HANDSHAKE not used to KEYBOARD

Fig. 11 BLOCK DIAGRAM Z-80A PIO

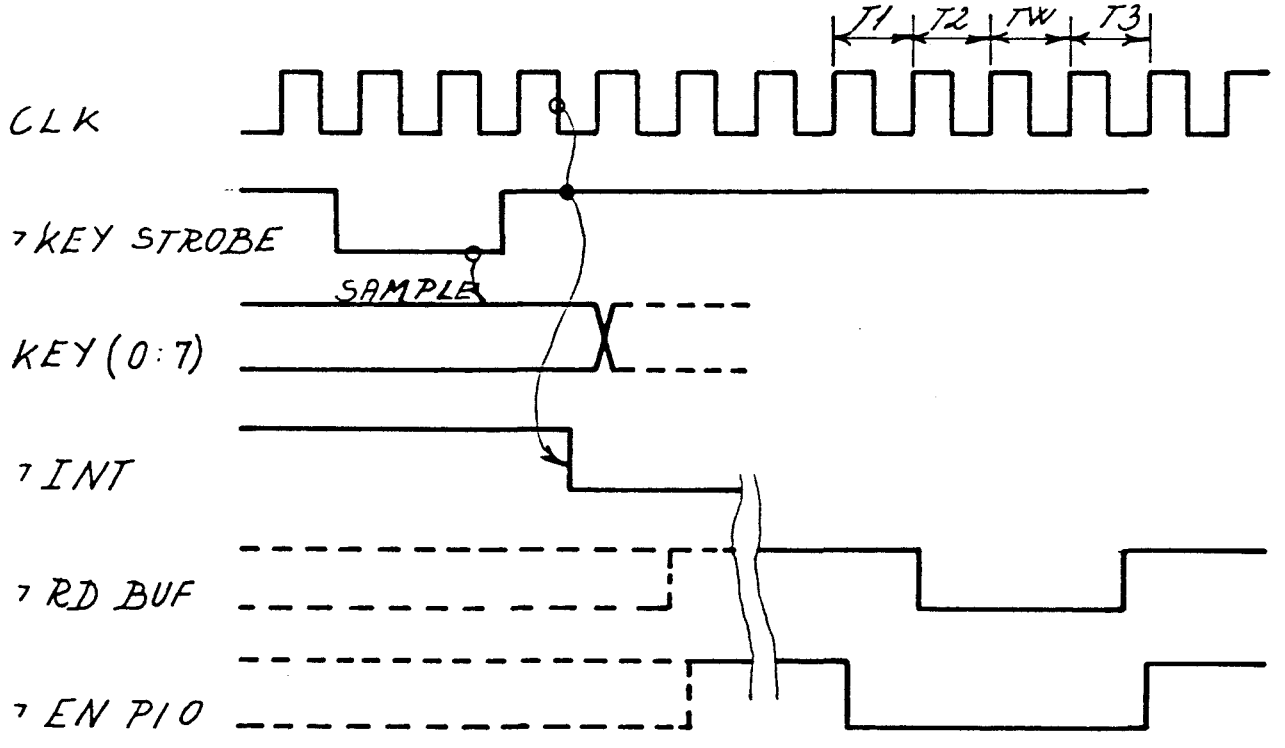
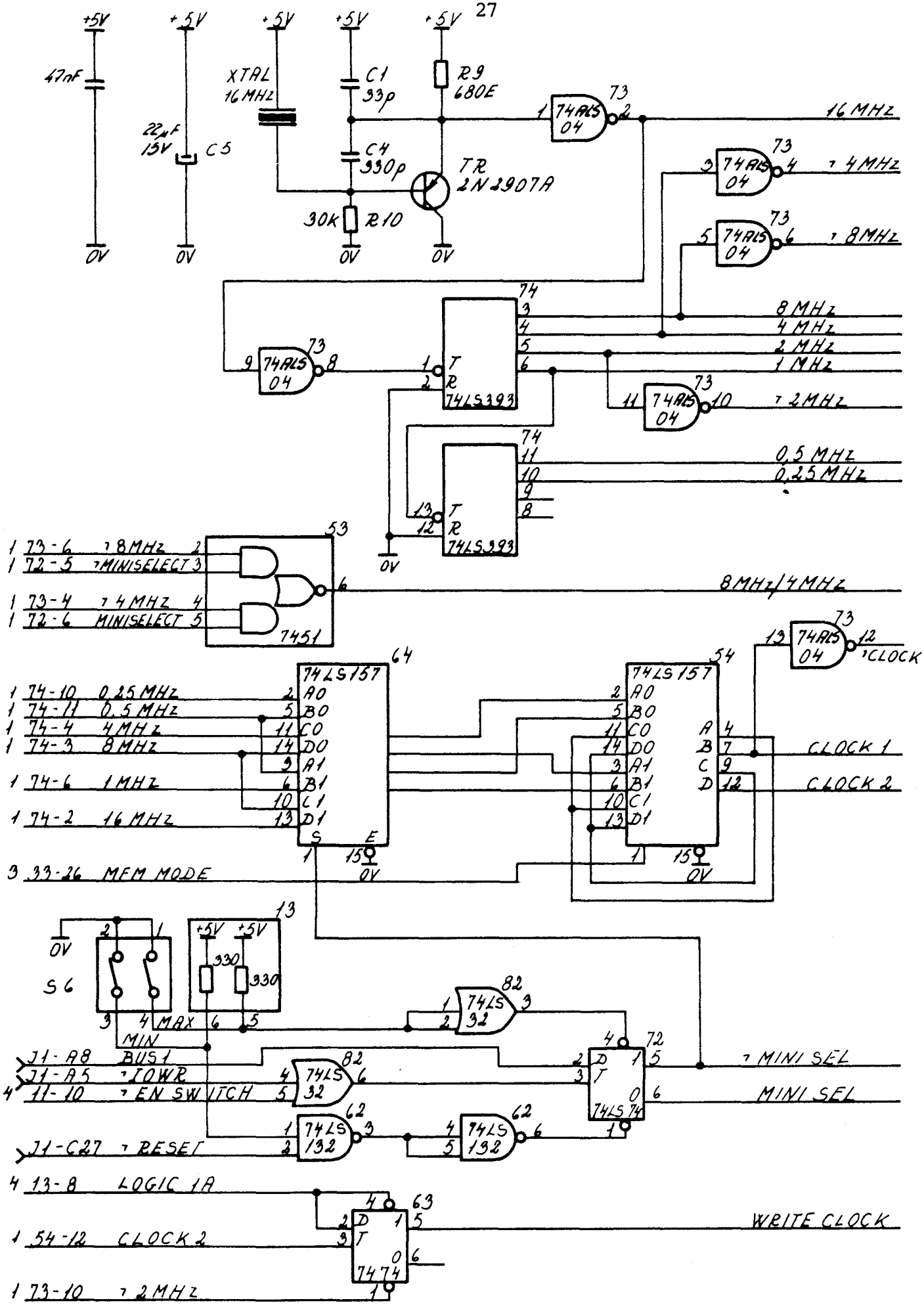


FIG. 12 TIMING DIAGRAM SHOWING INPUT TO THE PIO

4. CIRCUIT DIAGRAM 4.

The following 5 pages contain the circuit diagrams for FDI501 and FDI502. They are made according to the RC standard for diagrams to the RC700 and RC850 systems.

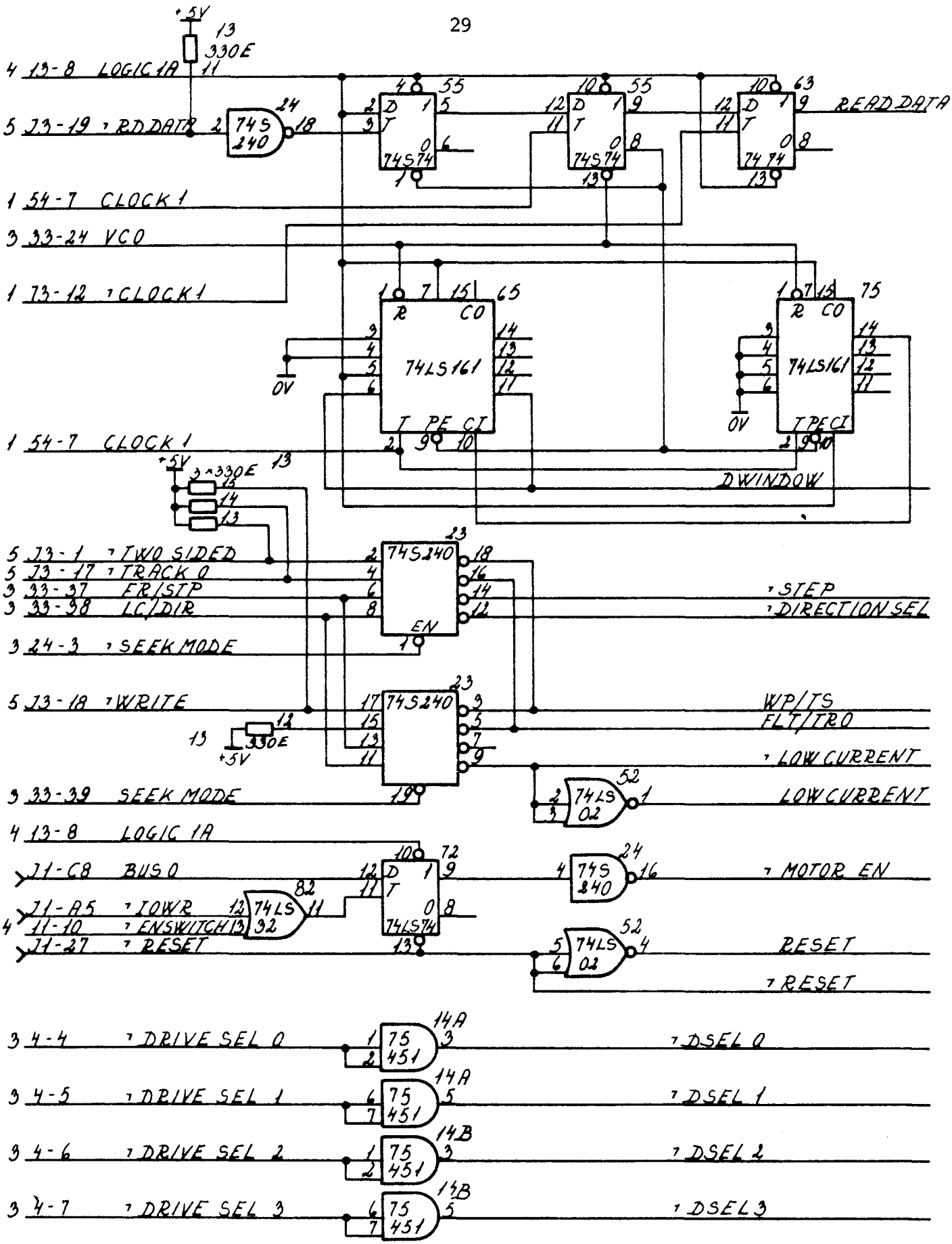
Signal	Destination	Description
16 MHz		Symmetric clock signal of 16 MHz
8 -		- - - - 8 -
4 -		- - - - 4 -
2 -		- - - - 2 -
1 -		- - - - 1 -
0.5 -		- - - - 0.5 -
0.25 -		- - - - 0.25 -
8 MHz/4 MHz	3	Clock to floppy controller 8 MHz for MAXI floppy and 4 MHz for MINI floppy drives
CLOCK1	2	Clock to read logic for floppy controller
CLOCK2		Clock signal to generate WRITE CLOCK
MINI SELECT	3, 4	Selects MINI floppy as strapped or as programmed. Strapping is described in fig. 10.
WRITE CLOCK	3	Write clock input to floppy controller. High for about 250 nS. Period time is 4 µS., 2 µS. or 1 µS.



FDI 501 — Floppy Controller Clock System Circuit Diagram — FDI 01

R 13482

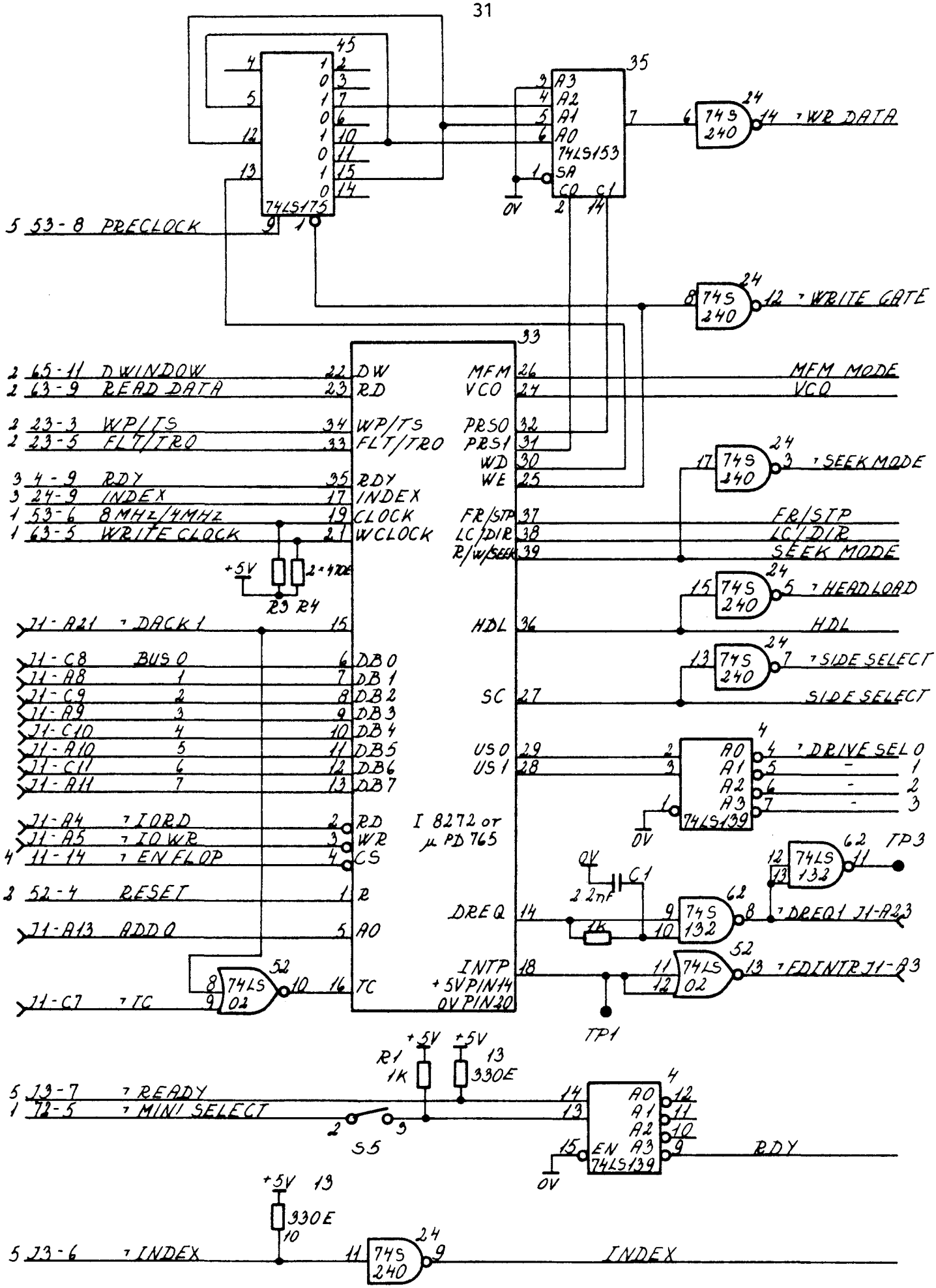
Signal	Destination	Description
READ DATA	3	Read data from the floppy, synchronized with the VCO signal to separate phase bits and data bits
D WINDOW	3	Data window is used by the floppy controller to separate data bits from phase bits
STEP	5	Output pulse to make the floppy head move from one cylinder to the next
DIRECTION SEL	5	Used together with the step pulse. A low signal together with a step pulse makes the floppy head move towards the center
WP/TS	3	Write protect/two sided. Signal from the floppy disk drive
FLT/TRO	3	Fault/Track 0. Signal from the floppy disk drive
LOW CURRENT	5	Signal to the MAXI disk drive. Used to decrease the write current when the head is close to the center of the disk
MOTOR EN	5	Signal to the MINI disk. Used to start and stop the motor
RESET	3	Power Reset and Master Reset
DSEL 0	5	DRIVE SELECT 0
- 1	5	- - 1
- 2	5	- - 2
- 3	5	- - 3



FD1501 Floppy Disk Read and Select Circuit FD102

213108 Circuit Diagram

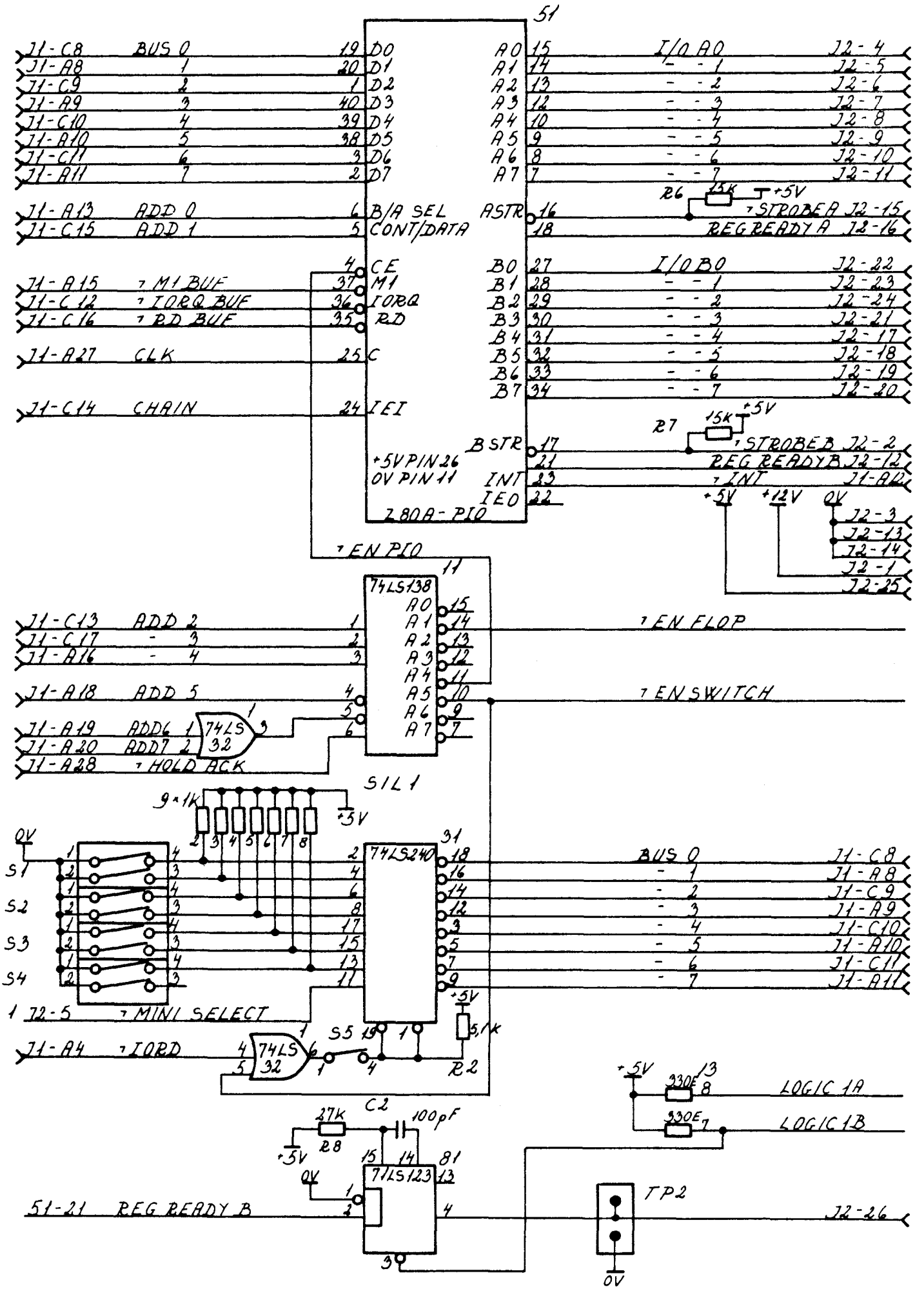
Signal	Destination	Description
WR DATA	5	WRITE Data to the floppy disk drive. Valid when WRITE GATE is on
WRITE GATE	5	Control signal to the floppy disk drive. Informs that now the WR DATA is valid
MFM MODE	1	MFM MODE is dual density, MF MODE is single density
VCO	2	Voltage Controlled Oscillator. The signals is used to enable the read control logic
SEEK MODE	2	Sets input and output selector in seek mode
FR/STP	2	Control signal. Fault Reset/Step
LC/DIR	2	Control signal. Low Current/Direction
HEAD LOAD	5	Control signal. Head Load
SIDE SELECT	5	Control signal. Side Select
DRIVE SEL 0	2	Control signal. Drive Select 0
DRIVE SEL 1	2	Control signal. Drive Select 1
DRIVE SEL 2	2	Control signal. Drive Select 2
DRIVE SEL 3	2	Control signal. Drive Select 3
DREQ1		DMA Request from the floppy controller
FD INTR		Interrupt Request from the floppy controller
RDY		Floppy Disk Drive is Ready. When S5 is closed a Minifloppy without Ready signal may be used
INDEX		Index Mark from floppy disk drive


74LS175
74LS153
74S 240
74LS139
74LS 132
74LS 02
I 8272 or μ PD 765
5 53-8 PRECLOCK
→WR DATA
→WRITE GATE
→SEEK MODE
→HEADLOAD
→SIDE SELECT
→DRIVE SEL 0
→DREQ1 J1-A23
→FDINTR J1-A3
2 65-11 DWINDOW
2 63-9 READ DATA
2 23-3 WP/TS
2 23-5 FLT/TRO
3 4-9 RDY
3 24-9 INDEX
1 53-6 8MHz/4MHz
1 63-5 WRITE CLOCK
MFM MODE
VCO
SEEK MODE
HDL
SIDE SELECT
J1-A21 →DACK1
J1-C8 BUS 0
J1-A8 1
J1-C9 2
J1-A9 3
J1-C10 4
J1-A10 5
J1-C11 6
J1-A11 7
J1-A4 →IORD
J1-A5 →IOWR
4 J1-14 →ENFLOP
2 52-4 RESET
J1-A13 ADD 0
J1-C7 →TC
DREQ
INTP
+5V PIN 14
0V PIN 20
TP1
TP3
R1 1K
330E
5 13-7 →READY
1 72-5 →MINI SELECT
S5
RDY
5 13-6 →INDEX
INDEX

Signal	Destination	Description
I/O A (0:7)		Input/Output signals from channel A of the PIO
STROBE A		Input Strobe signal for the channel A of the PIO
REG READY A		Register Ready A output signal for the channel A of the PIO
I/O B (0:7)		Input/output signals from channel B of the PIO
STROBE B		Input Strobe signal for the channel B of the PIO
REG READY B		Register Ready B output signal for the channel B of the PIO
INT		Interrupt request
EN FLOP		Enable Floppy Controller
EN SWITCH	1, 2	Enable Switch
BUS (0:7)		Data bus for the system
Test strobe		The signal is used when the PIO is tested

NOTE 1: POS51 and POS81 are not mounted in FDI501.

NOTE 2: S5 left open disables the switches (S1:S4) from being sensed by the program.

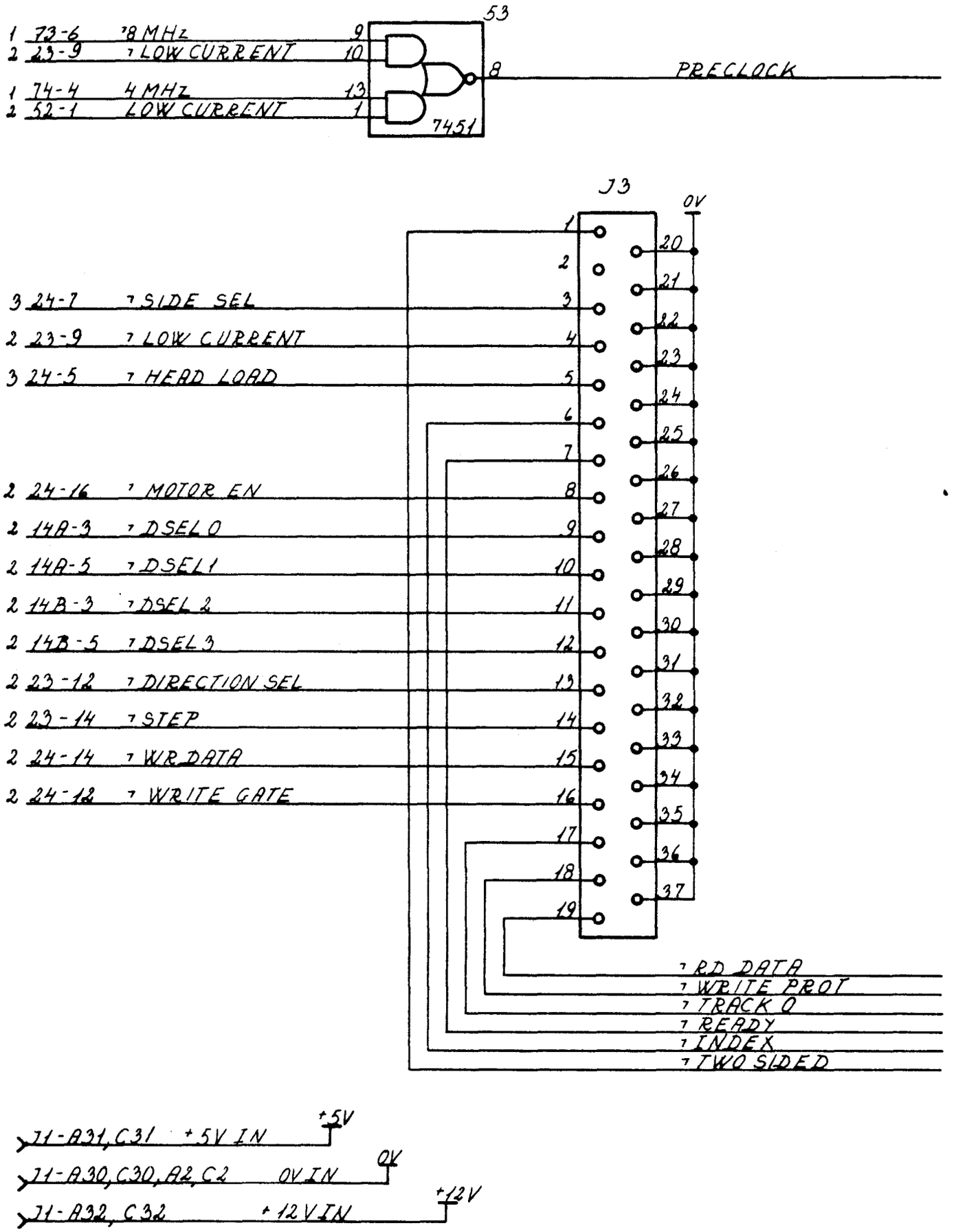


FDI 501
R 13 110

Parallel IN/OUT PORT CONTROLLER
Address Decoder
Circuit Diagram

FDI 04

Signal	Destination	Description
PRECLOCK	3	Clock to precompensation register
RD DATA	2	Input signal from floppy disk
WRITE PROT	2	- - - - -
TRACK0	2	- - - - -
READY	3	- - - - -
INDEX	3	- - - - -
TWO SIDED	2	- - - - -


53
1 73-6 8 MHz
2 23-9 ⁊ LOW CURRENT
1 74-4 4 MHz
2 52-1 LOW CURRENT
9
10
13
1
8
7451
PRECLOCK
J3
0V
3 24-7 ⁊ SIDE SEL
2 23-9 ⁊ LOW CURRENT
3 24-5 ⁊ HEAD LOAD
2 24-16 ⁊ MOTOR EN
2 14A-3 ⁊ DSEL 0
2 14A-5 ⁊ DSEL 1
2 14B-3 ⁊ DSEL 2
2 14B-5 ⁊ DSEL 3
2 23-12 ⁊ DIRECTION SEL
2 23-14 ⁊ STEP
2 24-14 ⁊ WR DATA
2 24-12 ⁊ WRITE GATE
A/3/11
⁊ RD DATA
⁊ WRITE PROT
⁊ TRACK 0
⁊ READY
⁊ INDEX
⁊ TWO SIDED
J1-A31, C31 +5V IN
J1-A30, C30, A2, C2 0V IN
J1-A32, C32 +12V IN
+5V
0V
+12V

5. SIGNAL CABLE 5.

The cable used is of the type CBL960. The signal cable is connected from J3 on the FDI501 board to the socket of RC850. The output plug placed in the socket of RC850 is a 37-pin D connector female and makes an RC standard for connection to floppy disk drives like RC762.

The pin numbers are shown in fig. 13.

5.1 Signal Cable if PIO is Used 5.1

If the PIO is used, the pin numbers of the cable are the same as shown in diagram FDI04, connector J2. The output connector is also placed in the socket of RC850 and is a 25-pin D connector female.

SIGNAL NAME	DIRECTION	PIN NO.
~ TWO SIDED	FROM FLOPPY	1
NOT USED		2
~ SIDE SELECT	TO FLOPPY	3
~ LOW CURRENT	TO FLOPPY	4
~ HEAD LOAD	TO FLOPPY	5
~ INDEX	FROM FLOPPY	6
~ READY	FROM FLOPPY	7
~ MOTOR EN	TO FLOPPY	8
~ DRIVESELECT 0	TO FLOPPY	9
~ DRIVE SELECT 1	TO FLOPPY	10
~ DRIVE SELECT 2	TO FLOPPY	11
~ DRIVE SELECT 3	TO FLOPPY	12
~ DIRECTIONSELECT	TO FLOPPY	13
~ STEP	TO FLOPPY	14
~ WRITE DATA	TO FLOPPY	15
~ WRITE GATE	TO FLOPPY	16
~ TRACK 0	FROM FLOPPY	17
~ WRITE PROT	FROM FLOPPY	18
~ READ DATA	FROM FLOPPY	19
SIGNAL RETURN	0 VOLT	20 to 37

Fig. 13. RC Standard Connection to Floppy Disk Drives.

RETURN LETTER

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