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MIC507/508 CPU-Board
Technical Manual

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Keywords:

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Abstract:

This manual contains technical descriptions and information on MIC507/508.

(66 printed pages)

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1. DESCRIPTION 1.

MIC507 and 508 is a Z80A microprocessor board for RC850, containing memory, program rom's, serial communication controllers and connectors for CRT-controller board and an optional controller (Floppy disc or Winchester).

A 50 conductor cable connects it to a separate PCB (COI50x) containing line interface buffers for the communication controllers.

MIC507 and MIC508 differ only in the type of PCB used. MIC507 uses a two layer board and MIC508 uses a 4 layer board. Circuit diagrams and component placement is the same for both versions.

The following descriptions and diagrams will only mention MIC507.

1.1 CPU/DMA Bus System 1.1

The main parts of the system (CPU, DMA, SIO and so on) are interconnected by an Address-, a Data- and a Control signal bus.

The Z80A CPU(P1) is normally bus master but if requested by the DMA controller (HOLD) it will three-state its bus lines as soon as the current CPU machine cycle is terminated. The DMA-controller will take over control of the busses as soon as it has received a busacknowledge (BUSACK) from the CPU and generate its own address and control signals to make a data transfer between memory and a I/O device.

The address lines 0 to 7 are buffered by a common buffer U75 (P3), while ADD 8-15 is buffered by U71 when the CPU is master and by the DMA address latch, U61 when the DMA-controller is master.

The read/write signals for I/O and memory (IORD, IOWR, MEMRD and MEMWR) are either generated from the CPU-signals by U81 and U82 (P2) or comes directly from the DMA-controller and use U84 as buffer.

The data bus is divided in an internal unbuffered bus (CPUBUS 0-7) and an external buffered bus (BUS 0-7) to the two connectors J1 and J2 and the NVM-control circuit.

Buffer direction of the buffer U85 (P1) is normally from internal to external as when data are read from memory or I/O devices on the internal bus. The direction is only reversed in the cases where an interrupt vector is read from an external interrupt controller, decoded by U42 (P9) or when data is to be read from an external I/O-device, decoded by IORD (P1) and either a DACK (DMA-acknowledge) from channel 0,1 or 3 or a decoding of an I/O device address not belonging to the local bus (U76, P4, EXT I/O EN).

1.2 Memory Control and Wait State Circuits 1.2

System memory consists of 64 K bytes of dynamic ram and up to 56 K bytes of rom (when using 8 K byte rom's).

The ROM in pos. U27 decodes the 5 MSB address lines and determines the partition of address space between RAM and ROM when reading from memory. Writing to an address always writes to the corresponding place in the RAM-memory.

Besides the address inputs the decoder has 3 other inputs, one from HOLD ACK and 2 from a dual F/F. The rom (ROB232) is coded so that DMA transfers always enables RAM regardless of the F/F states. After RESET the first 56 K of memory is decoded as ROM and the last 8 K as RAM. By I/O instructions it is possible to select only the first 16 K as ROM or all memory as RAM, see ROB232 rom listing and I/O-PORT ADDRESS LIST.

The decoder rom, ROB232 requires the ROM sockets to be strapped for 8 K byte rom's, using other rom sizes will require another decoder rom.

The dynamic RAM uses an INTEL 8202A memory controller for refresh and address multiplexing (U17, P6).

The memory controller derives its timing from a 19.66 MHz X-tal oscillator (P5) from which also the clock signals for the rest of the CPU-system is derived by a chain of counters (P5, P9).

The RAM access time together with the 4MHz CPU clock makes it necessary to insert at least one wait state at each memory access from the CPU. This is done by inserting a time delay (R17, C4) from SACK (U17) until WAIT is released.

SACK is removed by the 8202 (U17 PIN30 going high) each time a read or write cycle is requested and not granted again until the cycle has started (it may be postponed by an ongoing refresh cycle).

The XACK signal (U17, pin 29, -,XACK) is activated later in the memory cycle when valid data can be read from the datalines. This signal is used for wait state insertion during DMA-transfers since the Z80A SIO requires valid data on the bus before it receives an IOWR(circuit in top half of P5).

1.3 I/O-Address Decoding 1.3

The I/O address lines, the 8 LSB of the address bus, ADD 0-7 are decoded in blocks of 4 I/O port addresses by U77 and U78 (P4) covering the I/O addresses from 0 to 3F (HEX).

The decoder itself does not distinguish between memory- or I/O-addresses, this has to be done by each I/O device either internally as in the SIO or externally as on the RAM/ROM configuration control F/F's (U37, U88, P4).

The DMA controller I/O port range is decoded by U76, which also decodes internal/external I/O devices as required for direction control of the data bus buffer.

During DMA transfers the decoders are disabled by HLDA to avoid unintentional I/O accesses (DMA controller activates either IORD or IOWR during a transfer).

1.3.1 I/O - Port Address List

PORT (HEX)	PORT TYPE	FUNCTION	DESCRIPTION
00			
.			
.	EXTERNAL		Not allocated on CPU-BOARD
.			
07			
08	Z80A-SIO2	DATA CHA	Line I (A) and Line II (B)
09	-	- CHB	serial controller.
0A	-	CONTR. CHA	
0B	-	- CHB	
0C	Z80A-CTC	CH 0	Counter/timer: CH0 and CH1
0D	-	- 1	generates Baud rate clock
0E	-	- 2 (DISP)	for LINE I and II respect-
0F	-	- 3 (FLOPP)	tively. CH2 and 3 generat-
			es interrupt for Display
			and Floppy disc controller
			respectively.
10			
.			
.	EXTERNAL		Not allocated on CPU-BOARD
.			
17			

PORT (HEX)	PORT TYPE	FUNCTION	DESCRIPTION
18	74LS74	ENABLE ROM 0-56K	Output only, selects RAM/
19	-	DISABLE ROM	ROM address allocation.
1A	-	ENABLE ROM 0-16K	(Only output address is
1B	-	DISABLE ROM	significant, Data is don't care).
1C	74LS240	READ INPUTS	Reads auxiliary modem sig-
1D	-	-	nals from line I and II to
1E	-	-	data bus. (Calling Indica-
1F	-	-	tor and Data Set Ready
20 . . 27	EXTERNAL (DISPLAY)		Not allocated on CPU-BOARD
28	74LS273	NVM CONTROL	Read or Write in Non
29	and	-	Volatile Memory bit by bit
2A	NC7033	-	
2B		-	
2C . . 2F	EXTERNAL (DISPLAY)		Not allocated on CPU-BOARD
30	Z80A-SIO2	DATA CHA	Serial controller for CIR-
31	-	- CHB	CUIT/COAX (CHA) and Key-
32	-	CONTR. CHA	board (CHB)
33	-	- CHB	

PORT (HEX)	PORT TYPE	FUNCTION	DESCRIPTION
34	FLIP/FLOP	CLR F/F	An output to this address
35	-	-	clears the DMA-REQUEST
36	-	-	hold FF when preparing for
37	-	-	a SIO-DMA transfer.
38			
.			
.	EXTERNAL		Not allocated on CPU-BOARD
.			
EF			
F0	8237A-5	ADR CH0	DMA-controller for CPU-sy-
F1	-	COUNT CH0	stem.
F2	-	ADR CH1	Channel allocation:
F3	-	COUNT CH1	CH0: Display contr. (EXT).
F4	-	ADR CH2	CH1: External
F5	-	COUNT CH2	CH2: SIO (Circuit/Coax)
F6	-	ADR CH3	CH3: External
F7	-	COUNT CH3	
F8	-	COMM/STAT REG.	
F9	-	REQ REG	
FA	-	WR. SING. MASK	
FB	-	WR. MODE	
FC	-	CLEAR B.P.F/F	
FD	-	TEMP./MAST.CLR	
FE	-	CLEAR MASK REG	
FF	-	WRITE MASK REG.	

1.4 Interrupt System 1.4

Interrupt to the Z80A-CPU are generated by Z80A-I/O controllers (SIO,CTC) in a daisy chain priority connection. To generate an interrupt an I/O controller requires the priority chain input (IEI) to be high, it then lowers its chain output (IEO) and activates the open collector interrupt line.

Interrupt is acknowledged by the CPU when it activates IORQ and M1. In responce to this the interrupting controller places its interrupt vector on the data bus. At the end of the priority chain is placed a "dummy interrupt vector generator" (P9) needed when the CIRCUIT-SIO transfers data by DMA (the SIO generates interrupts without answering interrupt acknowledge from CPU). This assures that an interrupt ack. is always answered with a well defined vector.

The priority chain may be directed through an external interrupt controller in J1 by strap S10 (P9).

Interrupts from non-Z80 controllers (Display or Floppy disc) are directed through counter inputs on the Z80A-CTC (U48, P9) in which channels 2 and 3 are initialized to interrupt after one transition on the CK/TR input pin.

1.5 Serial Communication Controllers 1.5

The CPU board has 4 serial interfaces consisting of 2 Z80A-SIO/2's and a number of line buffers placed on a seperate PCB (COI50x) connected by a 50 conductor ribbon-cable.

1.5.1 Line 1 and 2 - SIO 1.5.1

The SIO, U58 (P10) interfaces to the main communication line (line 1) running in Async. or Synchronous mode and a printer line (line 2) running in Async. mode only.

Clock signals for async. mode are generated by CH0 and 1 in the CTC initialized as a clock divider. Channel 1 is used directly as clock for the printer channel while the CH0 clock is directed through a selector (U59) which allows line 1 clocks to come from the CTC (async.) or from an external source (Sync. modem).

The clock selector is controlled by an unused modem output on the Keyboard SIO (U57, P11). The SIO has no inputs for the modem signals CI and DSR, these are instead readable by a simple input port (U69).

1.5.2 Circuit, Keyboard SIO

1.5.2

The second SIO, U57 (P11) uses channel B for 300 baud serial communication with the keyboard. The CTS B input (U57, pin 23) receives a 25Hz square wave and is used for generating an interrupt on each edge of the signal i.e. each 20 mS. The DTRB output is used as a simple one bit output controlling the RX/TX-clock selector U59.

Channel A is used for the 250 Kbit/sec. CIRCUIT communication using a half duplex synchronous bit oriented protocol (the SIO is programmed to SDLC-mode).

When receiving or transmitting a block of data a byte needs to be transferred appr. each 32 microsec. A DMA-channel is used for this purpose and receives its DMA-request (DRQ2, U54) via a F/F (U54) which guarantees thåt DRQ2 is not removed before DACK2 is returned.

The acknowledge signal DACK2 forces the SIO-address, SIOADD 0-1 to zero (channel A, data register), enables the SIO and selects an IORQ generated by DMA signals by means of the selector U79 (P11).

The SIOIORQ signal (U79 pin 12) is an OR-function of the normal IORD signal (DMA reading from SIO) and SIOWR (DMA writing to SIO) activated by the DMA-wait circuit (U41, pin 9, P5) when data is ready from RAM.

After transmitting a data block the DMA REQ F/F is left with DRQ2 active. In preparation for the next block transfer the program has to reset the F/F by an output to the CLR F/F port.

Serial data are FM-modulated by U35, U33 (P12) which also delivers a 250 KHz transmit clock for the SIO.

Received data is converted to TTL-level on the COI-board (J9-36, RXDC, P12) and demodulated by a small sequencer U31, U32 (P12). A sequencer flow diagram is shown together with the ROM-listing in section 7.

The same circuit can be reconfigured for use with a COAX-COI-board by removing U35, inserting strap S7, moving strap S11 and changing of rom in pos. 32.

The COAX bit rate is higher (appro. 500 KBPS) and requires a different modulator placed on the COI-board where also the TXCLOCK is generated.

1.6 NVM Control Circuit 1.6

The Non Volatile Memory is a small memory of 21 words by 16 bit (NC7033, U107, P13) which retains its data after power is removed.

The NVM has 5 pins for serial interface, one clock, three command lines and a bidirectional data line for serial address and data. These lines are under program control from a parallel output register, U96.

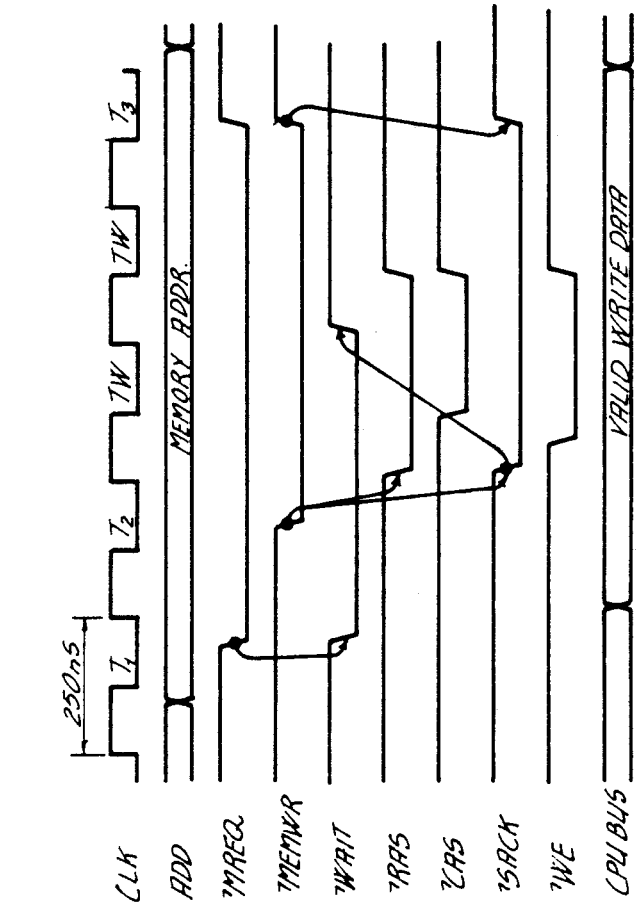
The register is reset at power up, which zeroes all outputs and thereby assures that the command inputs (U107, PINS 4, 5, 6) receives a standby command (1,1,1) and that no programming voltage (-25V) is applied to pin 1.

The register bits are used as follows:

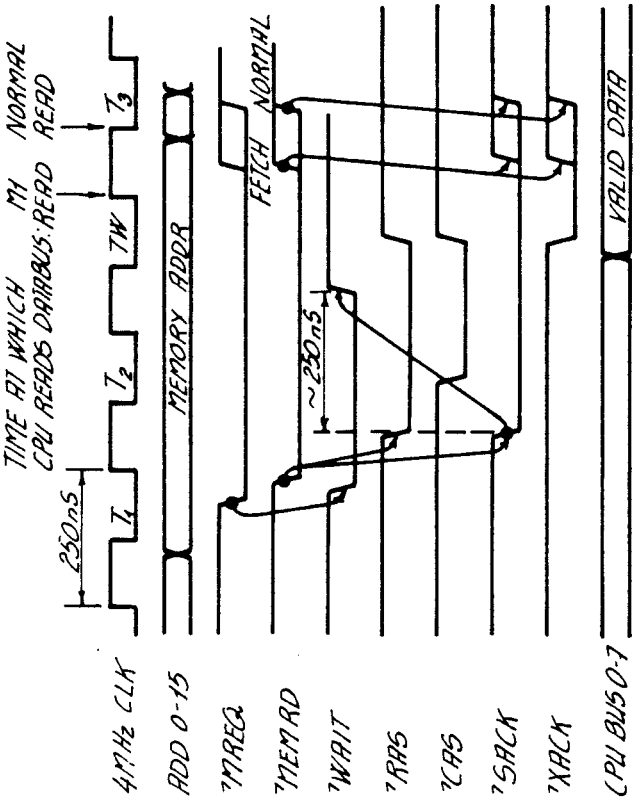
BIT NO.	U96 pin.no.	Description
0	2	Clock signal for NVM. Program is responsible for timing. Clock low time: more than 5 microsec. Clock high time: between 4 and 10 microsec.
1	5	Inverse of NVM command signal C1 on U107 pin 4.
2	6	If register bit 4 is high this signal is enabled and directly controls NVM signal C2 (U107, pin 5). If register bit 4 is low as after reset then C2 is pulled high.
3	9	Controls NVM signal C3 (U107, pin 6) if register bit 4 is high. (Similar to bit 2).
4	12	Enables register bit 2 and 3 to control NVM (C2, C3) if high. If LOW then both C2 and C3 are pulled high.
5	15	Enables program voltage (-25V) to NVM pin 1 if high. After enableing at least 200 mS should be allowed for the voltage switching circuit (T3) to turn on.
6	16	Data direction control. HIGH: enables data out to NVM (enables buffer and pull up resistor). LOW: allows reading data from NVM (disables buffer and disconnects pull up resistor).
7	19	Data out to NVM pin8 if direction out is selected.

More detailed information on operation of the NVM (NC7033) can be found in the data sheet in section 9 of this manual.

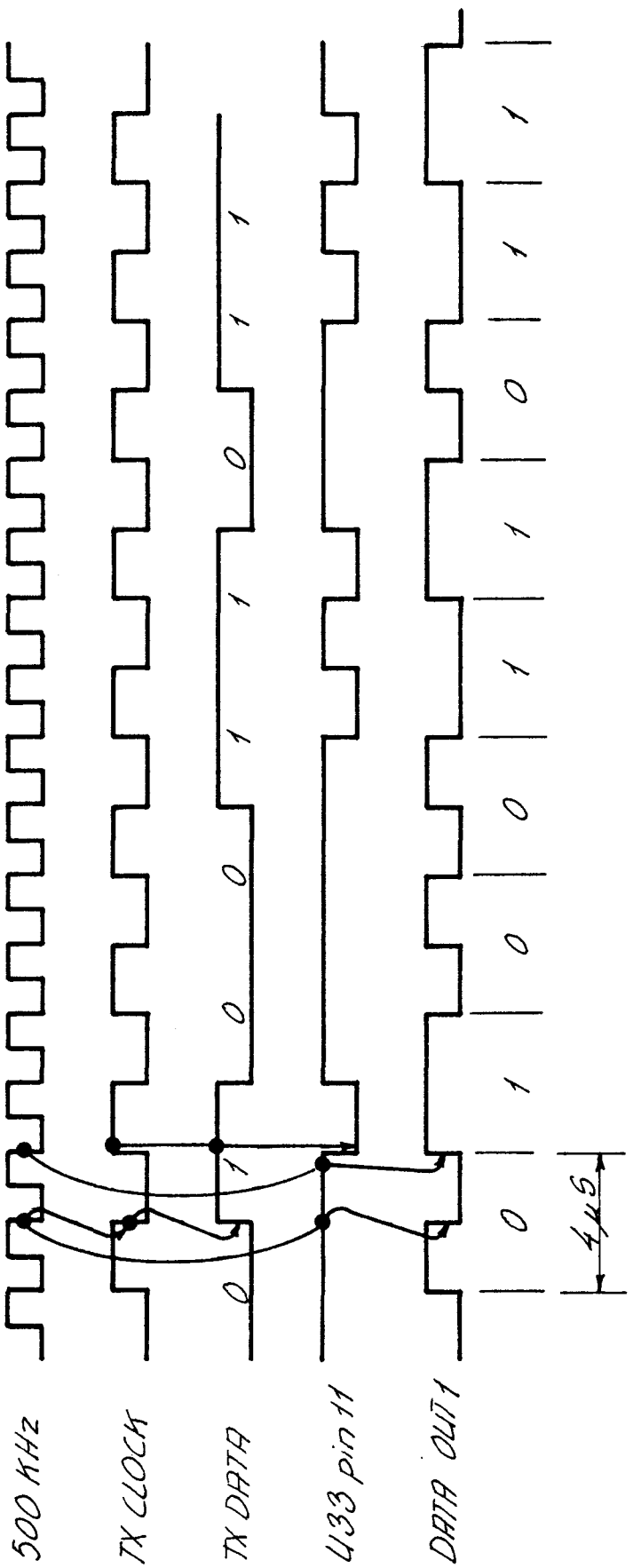
2. TIMING DIAGRAMS



MEMORY WRITE TIMING

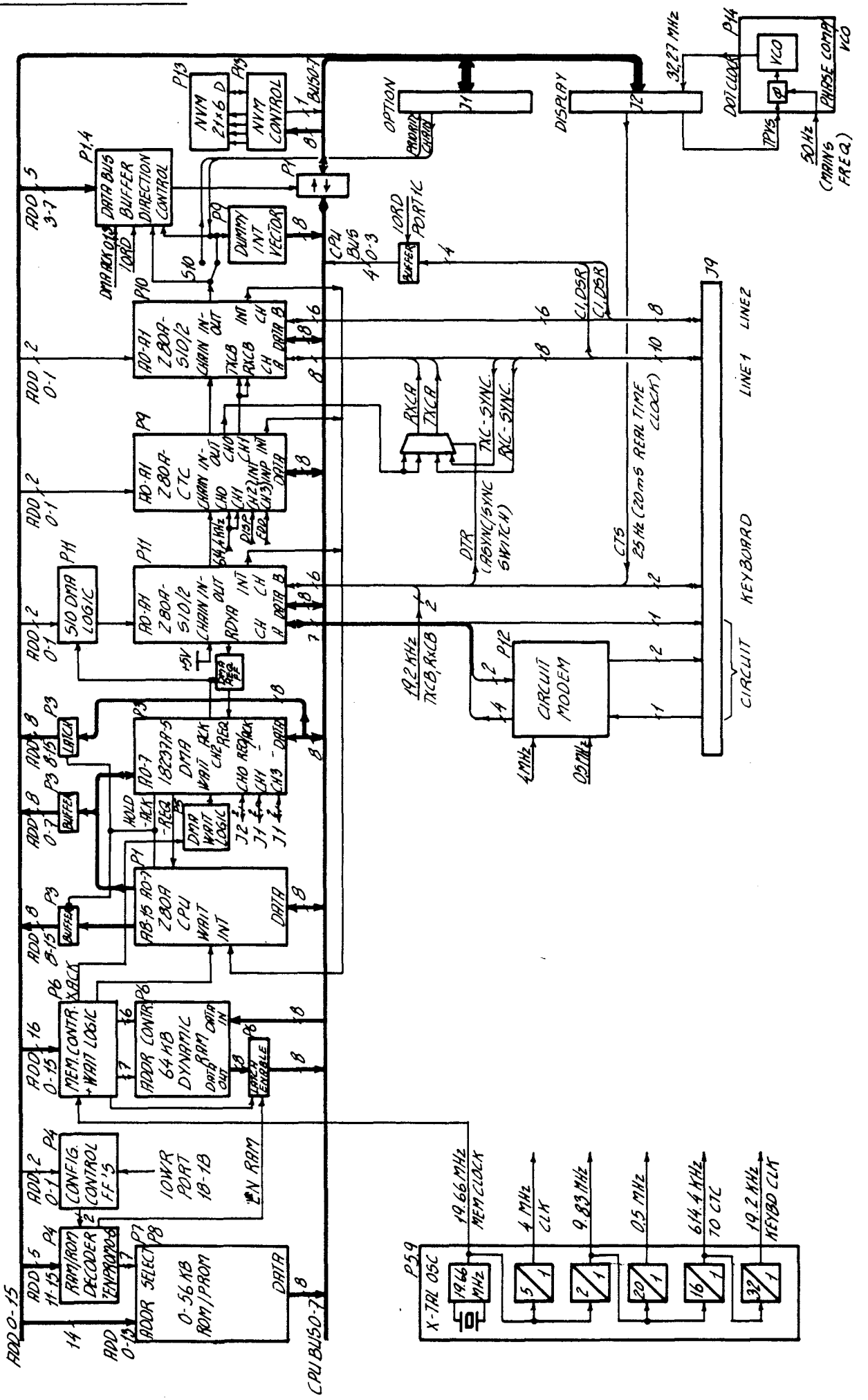


MEMORY READ TIMING


500 kHz
TX CLOCK
TX DATA
U33 pin 11
DATA OUT
4µs
0
1
0
1
1
0
1
1
0
1
1
0
1
1
0
1
1
1

3. BLOCK DIAGRAM

3.



4. LOGIC DIAGRAMS AND FUNCTIONAL DESCRIPTION 4.

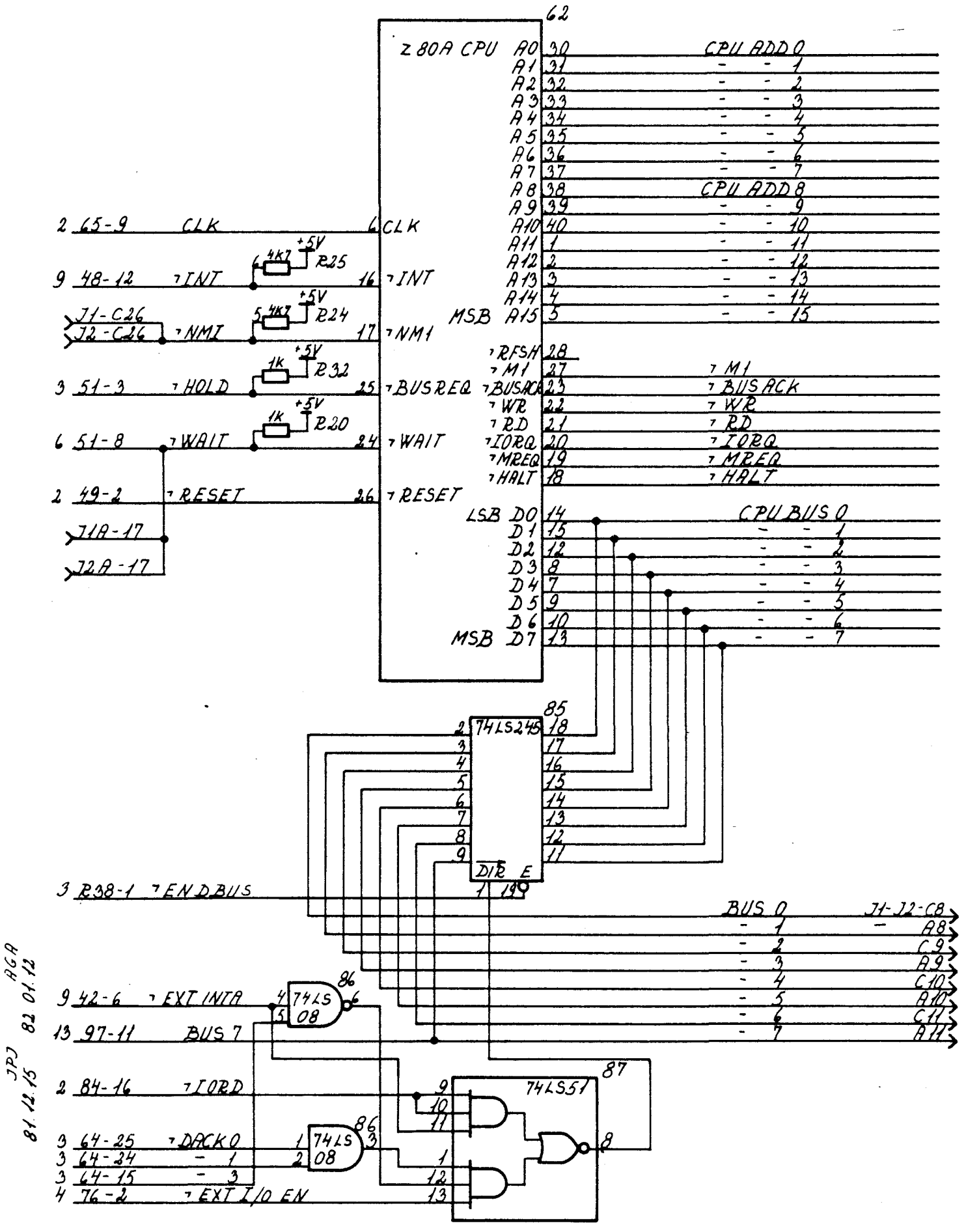
The following pages contain logic diagrams for MIC507/508.

A functional description is given on the left hand page to the corresponding diagram sheet.

The functional description consists of a schematic listing of all signals generated on the page. A short description and a listing of the diagrams to which the signal is transferred is given for each signal.

All references between diagram sheets make use of diagram numbers (lower right corner) and not page numbers.

Signal	Destination	Description
CPU ADD 0-15	3	CPU ADDRESS LINES
-,M1	2	CPU M1-CYCLE, ACTIVE WHEN CPU FETCHES OP-CODE
-,BUS ACK	2	BUS ACKNOWLEDGE, ACTIVE WHILE CPU HAS TRI-STATED ITS BUS-LINES:
-,WR	2	WRITE, CPU WRITES TO DATA BUS
-,RD	2	READ, CPU READS FROM DATA BUS
-,IORQ	2	IN/OUT REQUEST (IORQ TOGETHER WITH M1 INDICATES AN INTERRUPT ACKNOWLEDGE)
-,MREQ	2	MEMORY REQUEST
-,HALT	2	HALT STATE
CPU BUS 0-7	3,6,7,8,9, 10,11	CPU MAIN LOCAL DATA BUS
BUS 0-7	13, J1, J2	CPU EXTERNAL DATA BUS
		Normally data on the main bus is transmitted through a buffer to the external bus. Only when reading from external I/O devices is the buffer direction reversed.



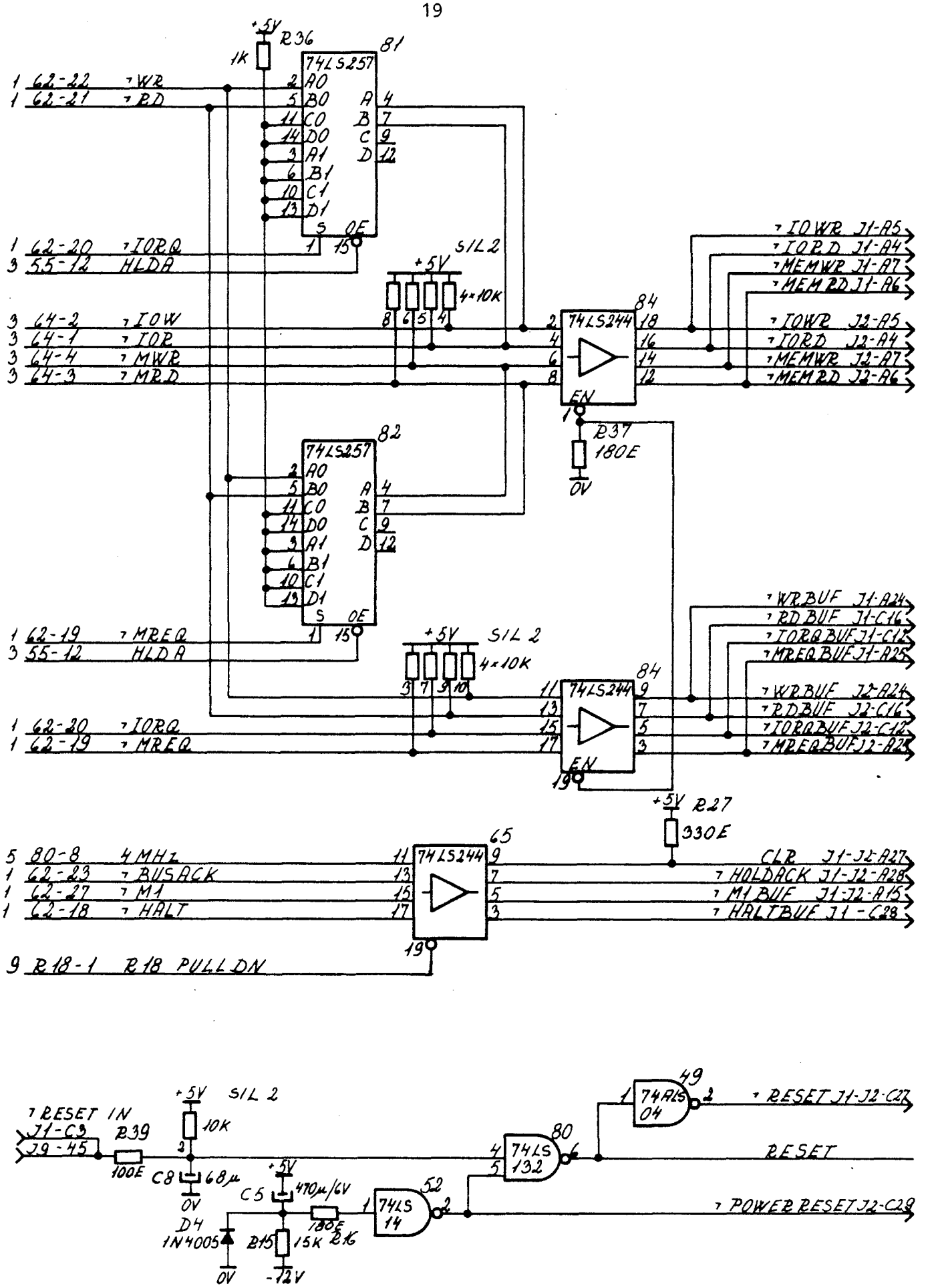
MIC 507 CPU AND EXTERNAL DATA BUS BUFFER 1

R 13326

Signal	Destination	Description
-,IOWR	4,11,13 J1, J2	IN/OUT WRITE *)
-,IORD	1,10,11,13, J1, J2	IN/OUT READ *)
-,MEMWR	5,6, J1, J2	MEMORY WRITE *)
-,MEMRD	4,5,6, J1,J2	MEMORY READ *)

*) These signals are generated by CPU or DMA-controller dependant on HOLD ACK.

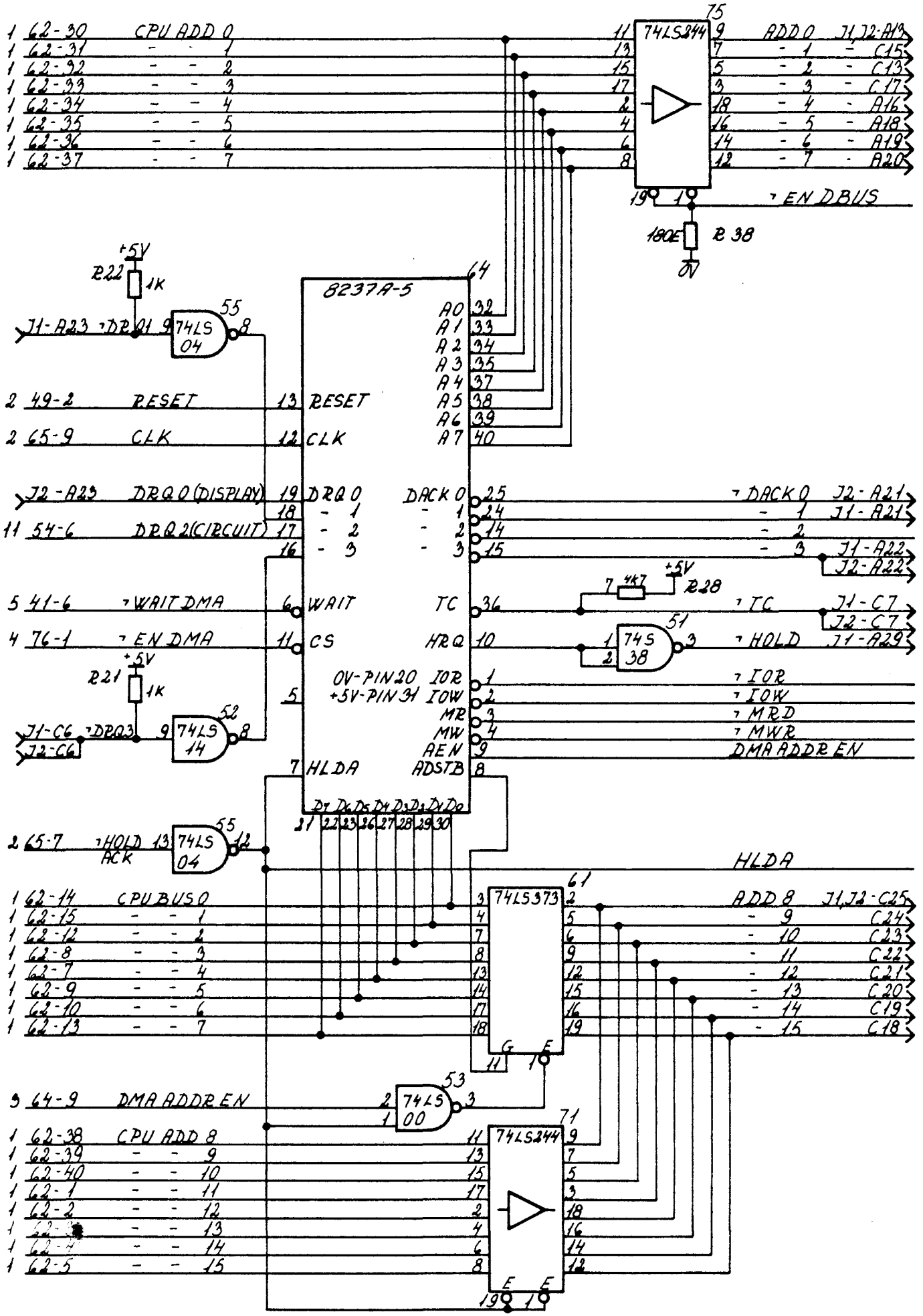
-,WRBUF	J1, J2	
-,RDBUF	9,10,11,J1,J2	
-,IORQ BUF	9,10,11,J1,J2	
CLK	1,3,5,9,10, 11,J1,J2	MAIN SYSTEM CLOCK, 4MHz
-,HOLDACK	3,J1,J2	HOLD ACKNOWLEDGE, CPU HAS RELEASED ITS BUS
-,M1BUF	9,10,11, J1,J2	M1 BUFFERED
-,HALT BUF	J1	HALT BUFFERED
-,RESET	3	RESET, Active at power up and after pressing the reset button.
-,POWER RESET	J2	POWER RESET, Active only at power up.



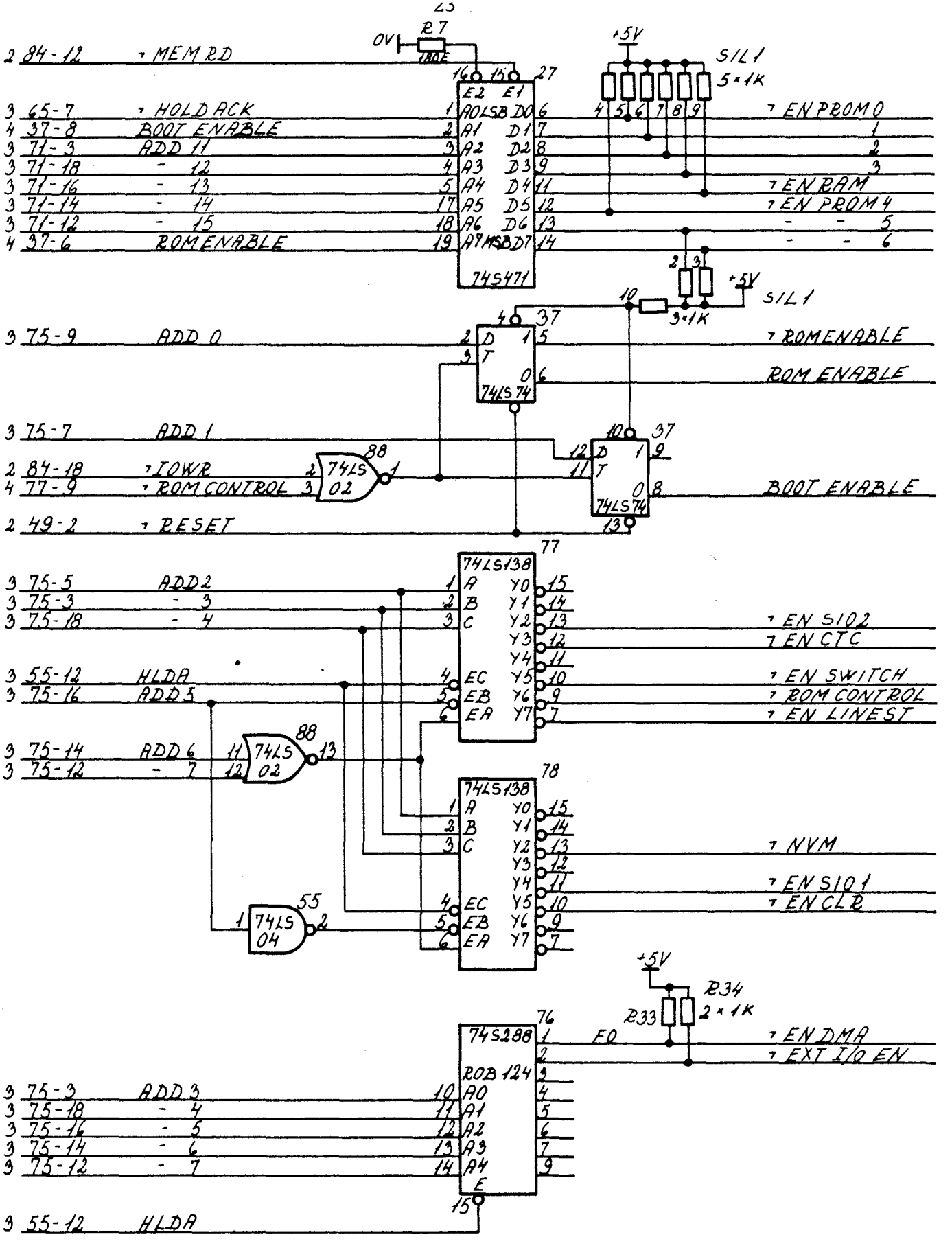
MIC 507 CONTROL SIGNAL BUFFERS AND RESET 2

R 13327

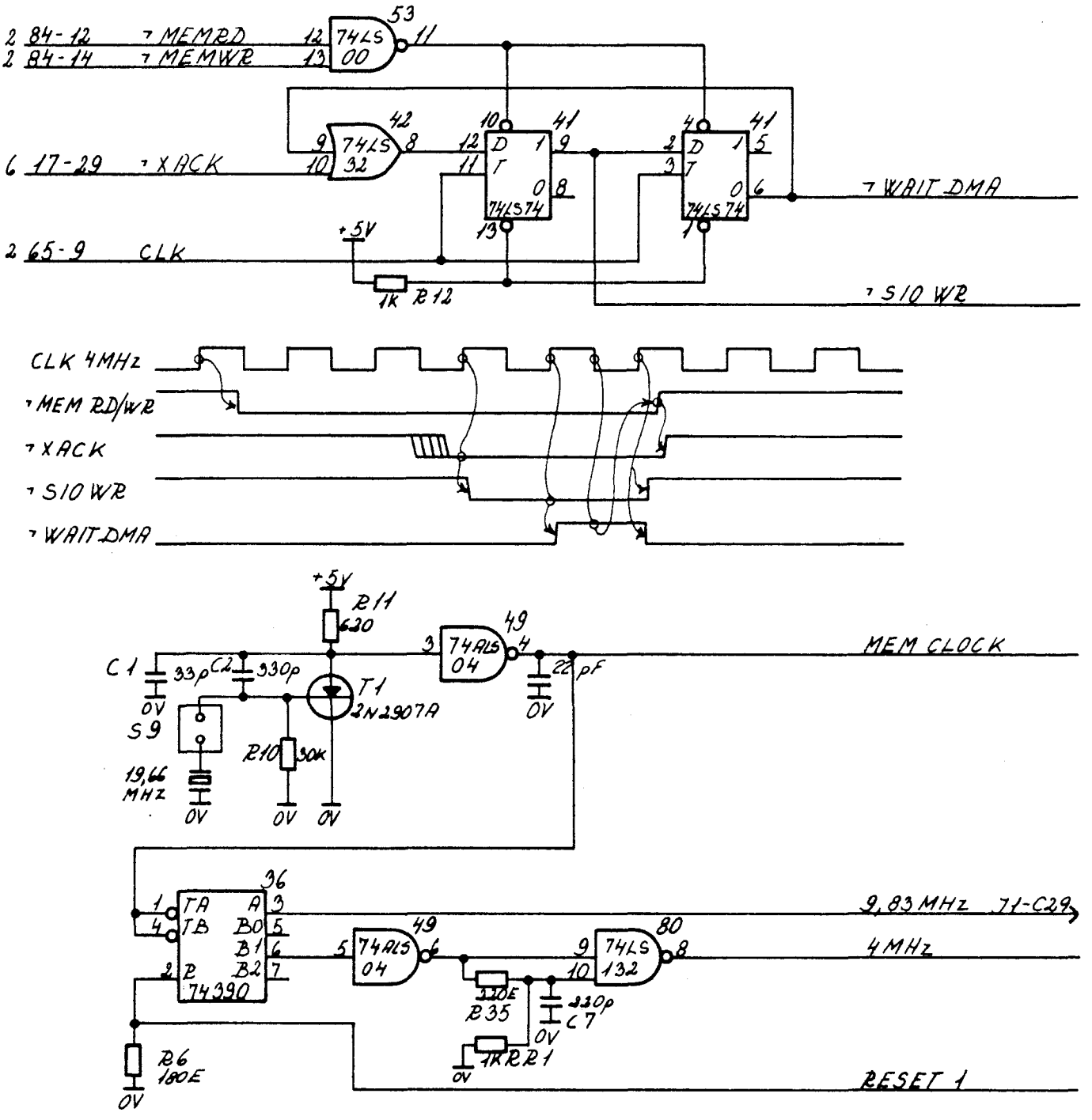
Signal	Destination	Description
ADD 0-1	4,6,7,8,9, 10,11,J1,J2	
ADD 2-7	4,6,7,8, J1,J2	ADDRESS BUS 8LSB, BUFFERED
-,EN DBUS	1	DISABLE BUFFERS FOR TEST
-,DACK0	J2	DMA-ACKN 0, DISPLAY
-,DACK1	J1	DMA-ACKN 1, CONTROLLER IN J1
-,DACK2	11	DMA-ACKN 2, CIRCUIT OR COAX - SIO
-,DACK3	J1,J2	DMA-ACKN 3, CONTROLLER IN J1 OR J2
-,TC	J1,J2	DMA TERMINAL COUNT, ACTIVE while the last byte in a block is transferred
-,HOLD	1,J1	BUS REQUEST, CPU IS REQUESTED to release its bus.
-,IOR	2	I/O READ TO/FROM DMA CONTROLLER
-,IOW	2	I/O WRITE TO/FROM DMA CONTROLLER
-,MRD	2	MEMORY READ
-,MWR	2	MEMORY WRITE
DMA ADDR EN	3	ENABLES A8-15 FROM DMA address latch to address bus.
HLDA	2,4	BUS ACKNOWLEDGE, CPU has released its bus.
ADD 8-10	6,7,8,J1,J2	
ADD 11-13	4,6,7,8,J1,J2	
ADD 14-15	4,6,J1,J2	ADDRESS BUS 8MSB, BUFFERED


8237A-5
74LS244
74LS373
74LS 04
74LS 14
74LS 38
74LS 00
CPU ADD 0
CPU ADD 8
CPU BUS 0
ADD 0
ADD 8
RESET
CLK
DRQ 0 (DISPLAY)
DRQ 2 (CIRCUIT)
WAIT DMA
EN DMA
HOLD ACK
HLDA
DMA ADDR EN
EN DBUS
DACK 0
TC
HRQ
IOR
IOW
MR
MW
AEN
ADSTB
R 38
R22 1K
R21 1K
R28 4K7

Signal	Destination	Description
-,ENPROM 0-4	7	
-,ENPROM 5-6	8	ENABLE DATA FROM PROM TO DATA BUS
-,EN RAM	6	ENABLE DATA FROM RAM TO DATA BUS
-,ROM ENABLE	7	ENABLES THE ROM ARRAY AT THE
ROM ENABLE	4	ADDRESSES DEFINED BY THE RAM/ROM DECODER IN POS. 27
BOOT ENABLE	4	IF ROM ENABLE IS ACTIVE THIS SIGNAL ALLOWS SOFTWARE SWITCHING BETWEEN TWO RAM/ROM CONFIGURATIONS WITH A SUITABLE DECODER ROM IN POS. 27
-,EN SIO2	10	ENABLE PRINTER/LINE SIO ADDRESSES 08-0B
-,EN CTC	9	ENABLE COUNTERTIMER (0C-0F)
-,ROM CONTROL	4	ENABLE RAM/ROM CONFIGURATION SETTING
-,EN LINEST	10	ENABLE CALLING INDICATOR AND DATA SET READY TO BUS 0-3
-,NVM	13	ENABLE NVM I/O PORT
-,EN SIO1	11	ENABLE KEYBOARD/CIRCUIT SIO
-,EN CLR	11	ENABLE CLEARING OF SIO DMA REQUEST FF
-,EN DMA	3	ENABLE DMA CONTROLLER
-,EXT I/O EN	1	ACTIVE AT I/O ADDRESSES NOT USED ON CPU BOARD


2 84-12 ↑MEMRD
3 65-7 ↑HOLD ACK
4 37-8 BOOT ENABLE
3 71-3 ADD 11
3 71-18 - 12
3 71-16 - 13
3 71-14 - 14
3 71-12 - 15
4 37-6 ROMENABLE
0V
R7
180E
74S471
+5V
SIL1
5×1K
↑EN PROM 0
1
2
3
↑EN RAM
↑EN PROM 4
- - 5
- - 6
3×1K
3 75-9 ADD 0
74LS74
↑ROMENABLE
ROM ENABLE
3 75-7 ADD 1
2 84-18 ↑IOWR
4 77-9 ↑ROM CONTROL
74LS02
BOOT ENABLE
2 49-2 ↑RESET
3 75-5 ADD2
3 75-3 - 3
3 75-18 - 4
74LS138
3 55-12 HLDA
3 75-16 ADD 5
↑EN SIO2
↑EN CTC
↑EN SWITCH
↑ROM CONTROL
↑EN LINEST
3 75-14 ADD 6
3 75-12 - 7
74LS04
↑NVM
↑EN SIO 1
↑EN CLR
R34
2×1K
R33
74S288
FO
↑EN DMA
↑EXT I/O EN
3 75-3 ADD 3
3 75-18 - 4
3 75-16 - 5
3 75-14 - 6
3 75-12 - 7
3 55-12 HLDA
JP1 81.12.15 AGA 82.1.13

Signal	Destination	Description
-,WAIT DMA	3	WAIT SIGNAL FOR DMA CONTROLLER
-,SIO WR	11	DMA WRITE STROBE FOR SIO. ACTIVE ONLY WHILE DATA FROM MEMORY IS STABLE
MEM CLOCK	6	19.66 MHz CLOCK FOR MEMORY CONTROLLER
9.83 MHz	9, J1	CLOCK FOR USE IN BAUD RATE GENERATION
4 MHz	2,12	4 MHz SYSTEM CLOCK UNBUFFERED
RESET1	9	COUNTER RESET FOR TEST

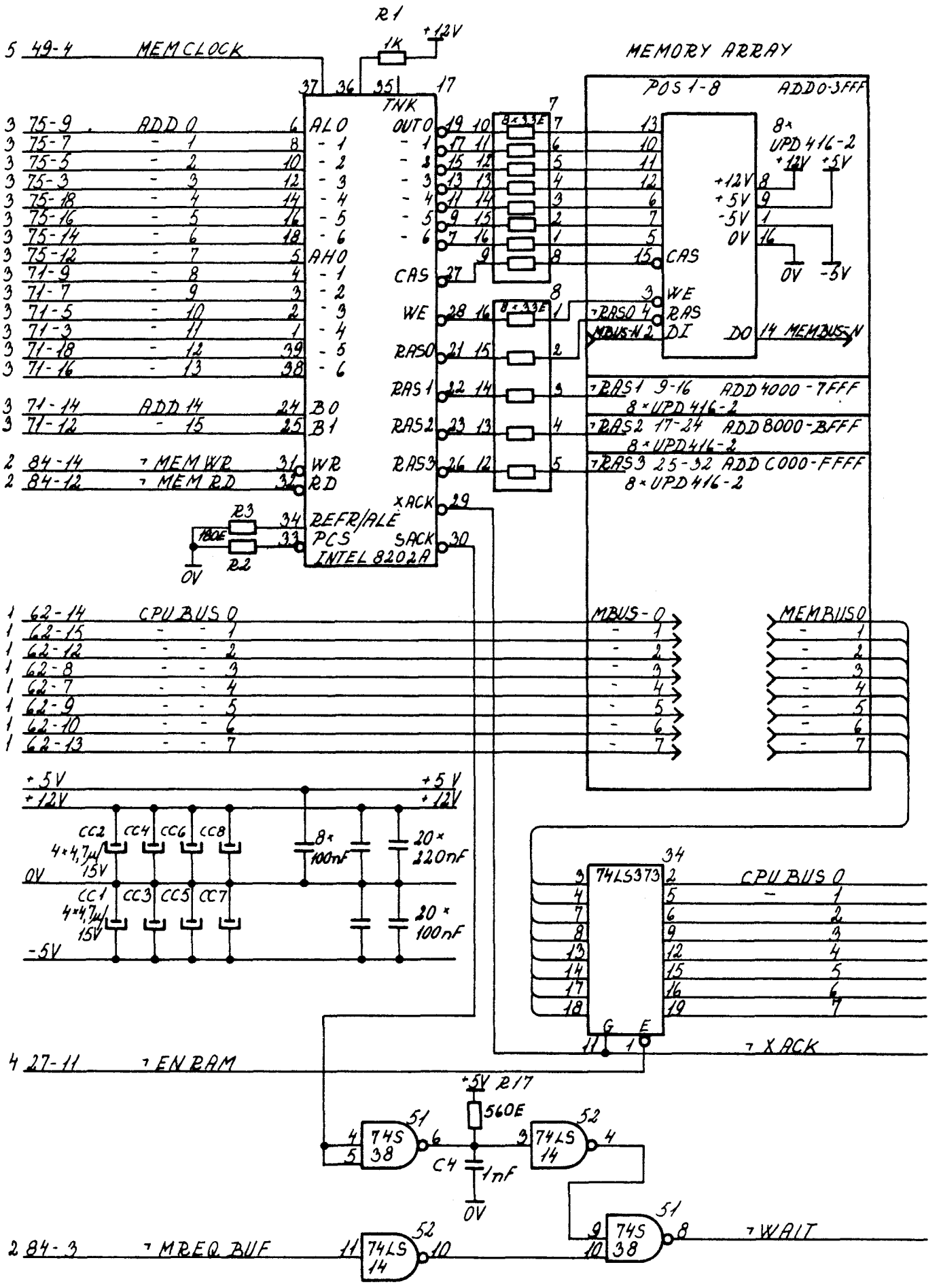


JPJ 81.12.15 AGA 82.1.14

MIC 507
R 13330

DMA WAIT STATE GENERATOR &
MEMORY/CPU CLOCK GENERATOR

Signal	Destination	Description
CPU BUS 0-7	3,7,8,9,10, 11	CPU MAIN LOCAL DATA BUS
-,XACK	5	STROBE INDICATING VALID DATA WHEN READING FROM MEMORY OR DATA WRITTEN WHEN WRITING
-,WAIT	1	WAIT SIGNAL TO CPU

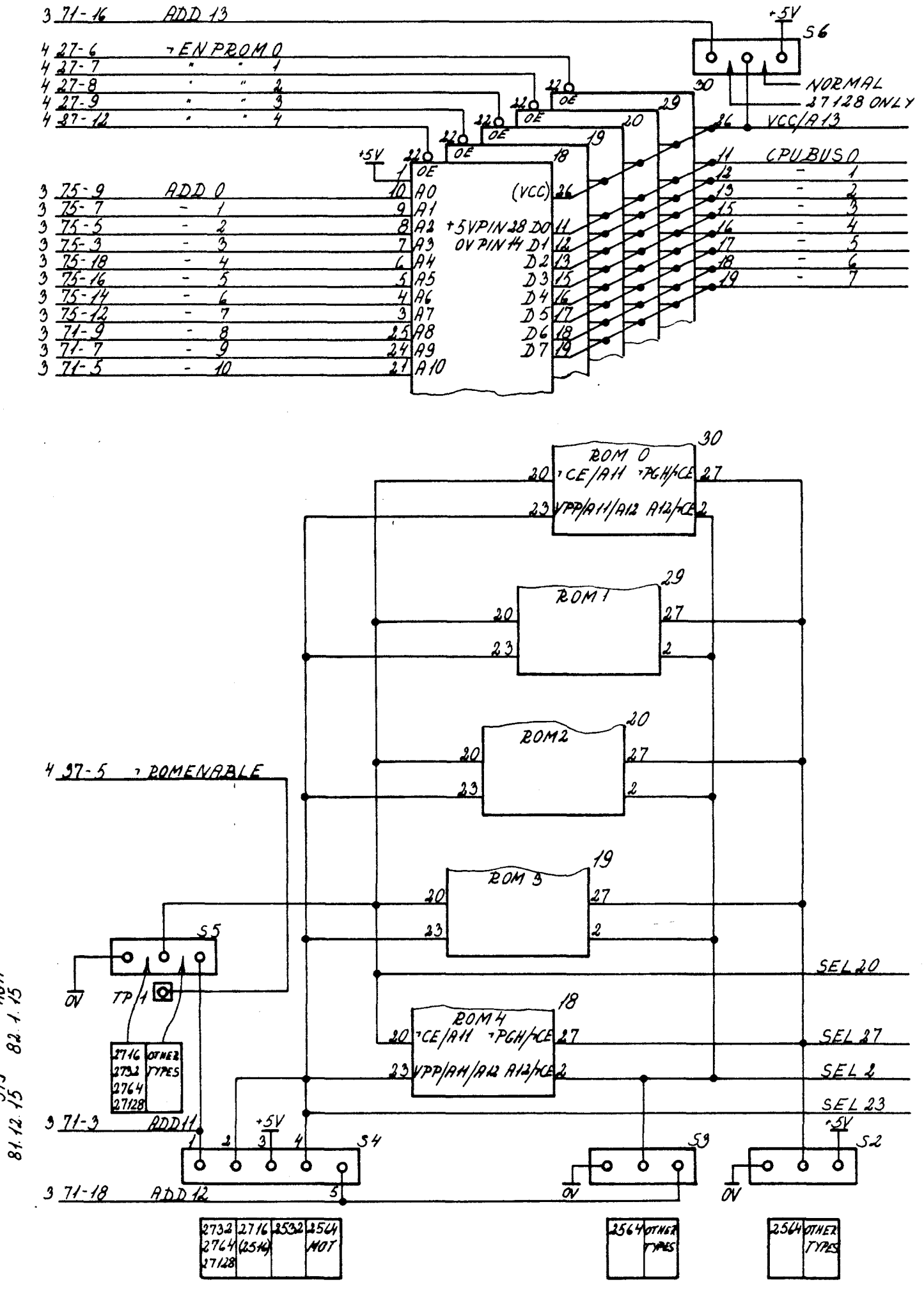


JPJ AGA
81.12.15 82.1.14

MIC 507
R 13331

64 K BYTE RAM &
CPU WAIT STATE GENERATOR

Signal	Destination	Description
VCC/A13	8	ROM ARRAY PIN 26 SIGNAL: ADD13 for INTEL 27128 OR +5V FOR OTHER TYPES
CPU BUS 0-7	3,6,8,9,10, 11	CPU LOCAL DATA BUS
SEL 20	8	PIN 20 SIGNAL SELECTED BY S5 AS PERMANENT CE, CE WHEN ROM's ARE ENABLED (POWER DOWN) OR A11 (FOR NON INTEL TYPES)
SEL 27	8	PIN 27 SIGNAL SELECTED BY S2. NORMALLY +5V, BUT OV FOR TMS 2564
SEL 2	8	PIN 2 SIGNAL SELECTED BY S3 NORMALLY ADD12, BUT 0V FOR TMS 2564
SEL 23	8	PIN 23 SIGNAL SELECTED BY S4 ADD11 FOR 2732, 2764, 27128 +5V FOR 2716, 2516, 2532 ADD12 FOR 2564, MOTOROLA TYPES

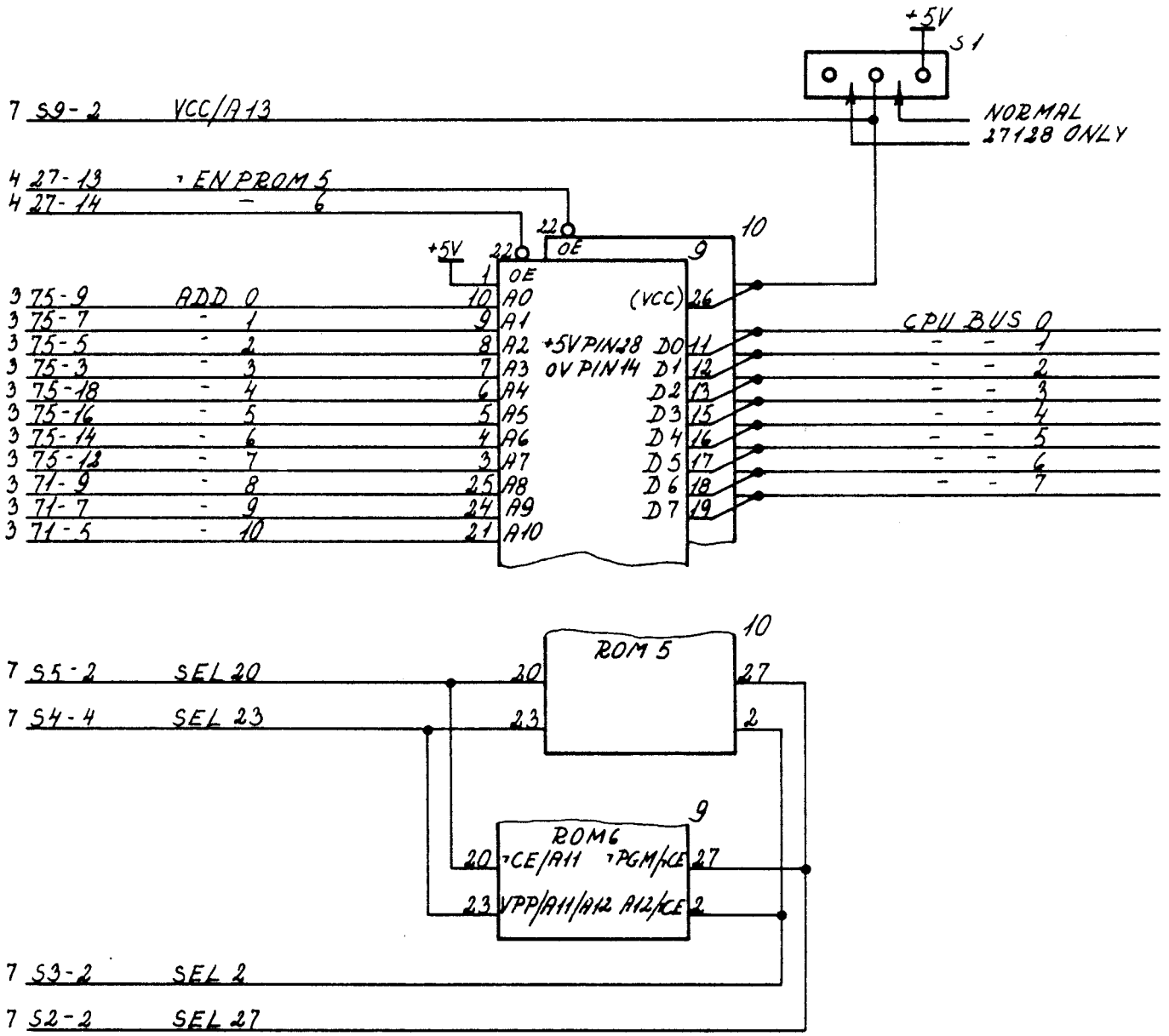


JPJ 81.12.15 AGA 82.1.15

•MIC 507 ROM ARRAY WITH STRAPPINGS 7

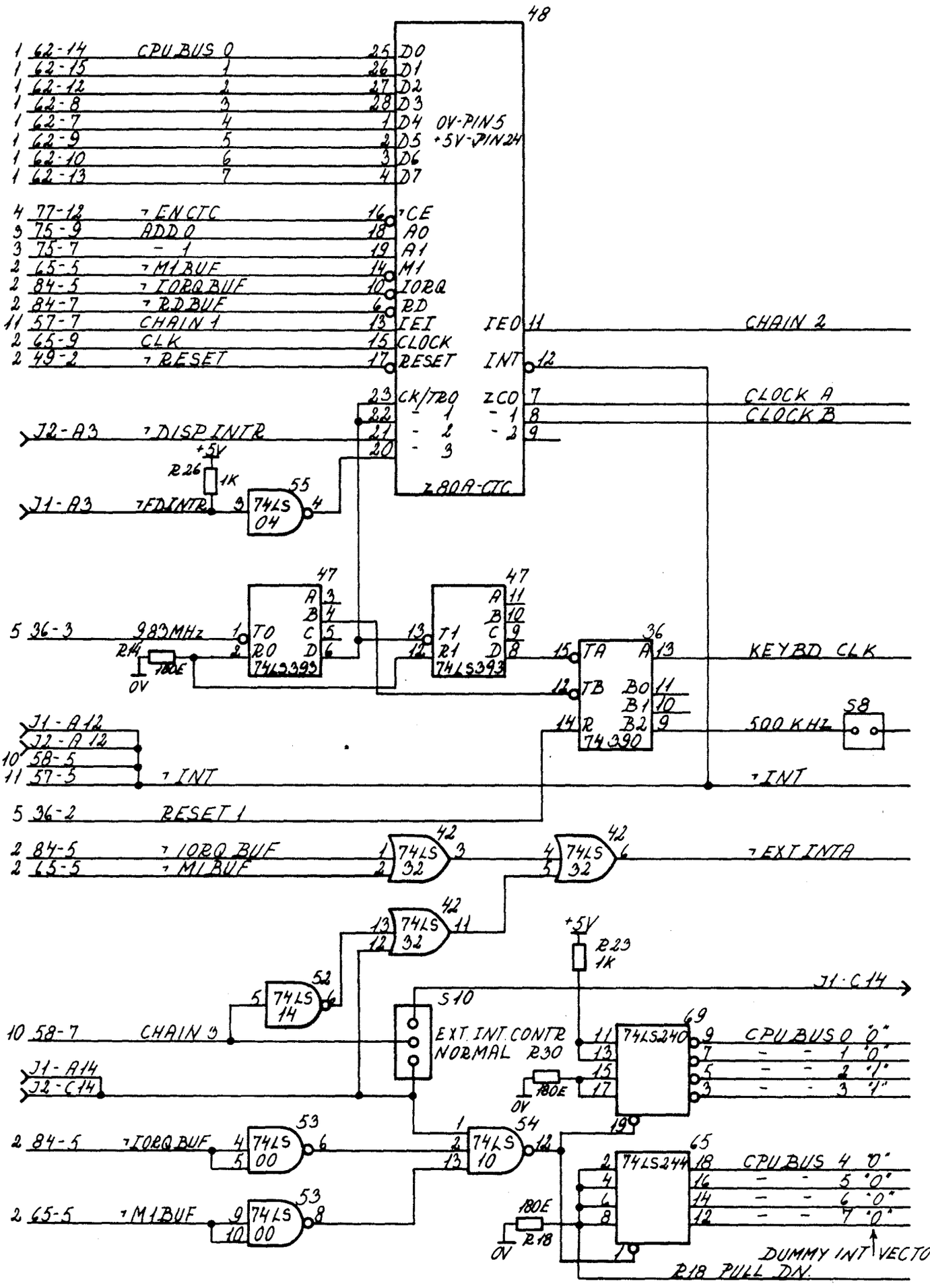
R13332

Signal	Destination	Description
CPU BUS 0-7	3,6,7,9,10, 11	CPU LOCAL DATA BUS



81.12.15 JPJ 82.1.15 AGA

Signal	Destination	Description
CHAIN 2	10	INTERRUPT PRIORITY CHAIN WHEN HIGH, ENABLES INTERRUPT FROM THE FOLLOWING CONTROLLER
CLOCK A	10	BAUD RATE CLOCK FOR LINE SIO
CLOCK B	10	BAUD RATE CLOCK FOR PRINTERLINE SIO
KEYBD CLK	11	BAUD RATE CLOCK FOR KEYBOARD SIO
500 KHz	12	CLOCK FOR "CIRCUIT" MODULATOR S8 IS CONNECTED IN "CIRCUIT"-VERSIONS OR MOVED TO S7 IN "COAX" VERSIONS. (SEE DIAGRAM 12).
-,INT	1	INTERRUPT LINE ACTIVATED BY A CONTROLLER REQUESTING INTERRUPT SERVICE
-,EXT INTA	1	SIGNAL INDICATING INTERRUPT ACKNOWLEDGE TO AN INTERRUPT CONTROLLER OUTSIDE THE CPU BOARD, WHICH REQUIRES REVERSAL OF DATA BUS BUFFER
EXT CHN OUT	J1	EXTERNAL PRIORITY CHAIN OUT. WHEN PIN 1 AND 2 IN S10 IS CONNECTED ENABLES INTERRUPT TO A CONTROLLER OUTSIDE THE CPU BOARD. THE CONTROLLER MUST RETURN THE CHAIN TO J1A-14, EXT CHN IN
CPU BUS 0-7	3,6,7,8,10, 11	DUMMY INTERRUPT VECTOR (0C HEX) TO LOCAL CPU BUS IF NO OTHER INT. CONTROLLER RESPONDS TO INT. ACK.
R18 PULL DN	2	DISABLE SIGNAL FOR TEST



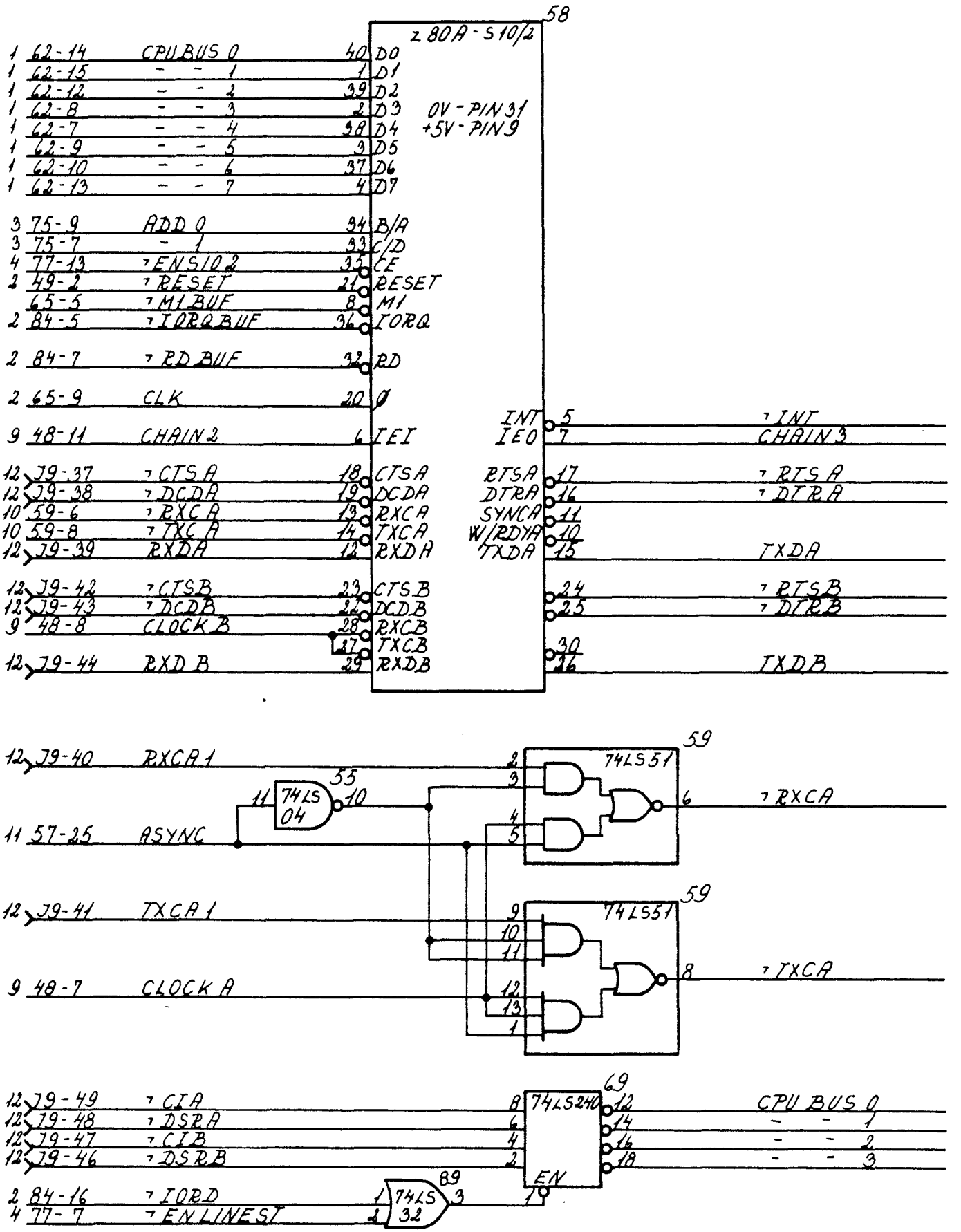
AGA 82.1.18
JPJ 81.12.15

MIC 507
R 13334

CTC AS INTERRUPT CONTROLLER AND BAUD RATE GENERATOR, DUMMY INT VECTOR GENERATOR

9

Signal	Destination	Description
-,INT	9	INTERRUPT LINE ACTIVATED BY A CONTROLLER REQUESTING INTERRUPT SERVICE
CHAIN 3	9	INTERRUPT PRIORITY CHAIN. WHEN HIGH, ENABLES INTERRUPT FROM THE FOLLOWING CONTROLLER
-,RTS A	12	REQUEST TO SEND, LINE CHANNEL
-,DTR A	12	DATA TERMINAL READY, LINE CHANNEL
TXD A	12	TRANSMITTED DATA, LINE CHANNEL
-,RTS B	12	REQUEST TO SEND, PRINTER CHANNEL
-,DTR B	12	DATA TERMINAL READY, PRINTER CHANNEL
TXD B	12	TRANSMITTED DATA, PRINTER CHANNEL
-,RXC A	10	RECEIVE CLOCK, LINE CHANNEL SELECTED FROM CLOCK A (INTERNAL) IF ASYNC IS HIGH OR FROM EXTERNAL MODEM SIGNAL IF ASYNC IS LOW
-,TXC A	10	TRANSMIT CLOCK, LINE CHANNEL SELECTED AS -,RXC A
CPU BUS 0-3	3,6,7,8,9,11	LOCAL CPU BUS



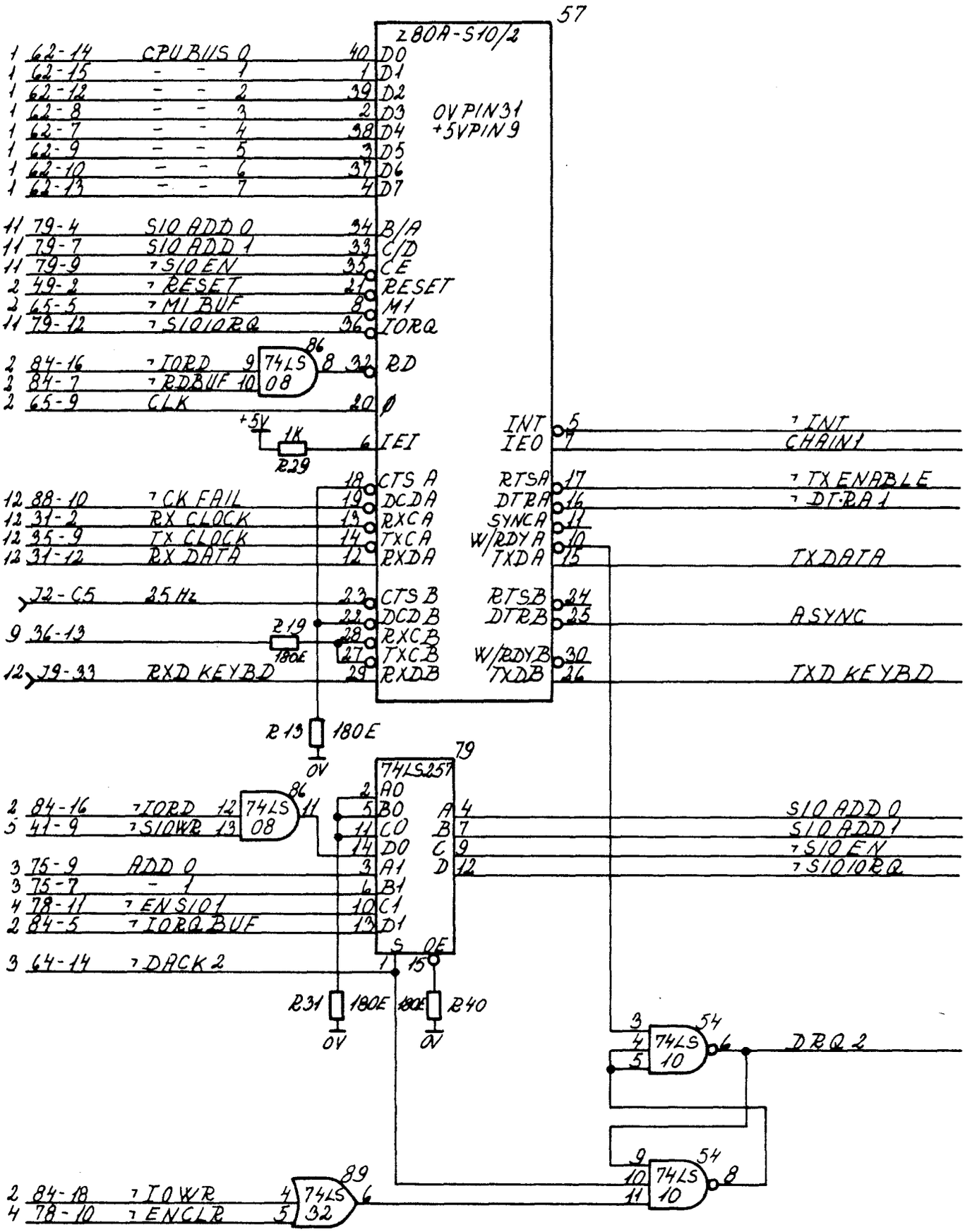
JPJ AGA
81.12.15 82.1.18

MIC 507
R 13335

SERIAL CONTROLLER FOR LINE (A CHANNEL) and FOR PRINTER (B CHANNEL)

10

Signal	Destination	Description
-,INT	9	INTERRUPT LINE ACTIVATED BY A CONTROLLER REQUESTING INTERRUPT SERVICE
CHAIN 1	9	INTERRUPT PRIORITY CHAIN
-,TXENABLE	12	ENABLE CIRCUIT LINE DRIVER WHEN TRANSMITTING
-,DTRA1	12	ENABLE CARRIER DETECTION BY CIRCUIT DEMODULATOR
TXDATA	12	TRANSMITTED DATA TO CIRCUIT OR COAX
ASYNC	10	ASYNCHRONOUS CLOCK SELECT FOR LINE CHANNEL SIO. HIGH SELECTS INTERNAL CLOCK FROM CTC LOW SELECTS EXTERNAL CLOCK (FROM A MODEM)
TXD KEYBD	12	TRANSMITTED DATA TO KEYBOARD
SIO ADD 0	11	CHANNEL A/B SELECT
SIO ADD 1	11	CONTROL/DATA SELECT TO CIRCUIT/KEYBOARD SIO NORMALLY CONNECTED TO CPU ADD 0-1, BUT FORCED TO LOW DURING DMA TRANSFER
-,SIO EN	11	SIO CHIP ENABLE
-,SIO IORQ	11	SIO IOREQUEST
DRQ 2	3	DMA REQUEST FROM SIO

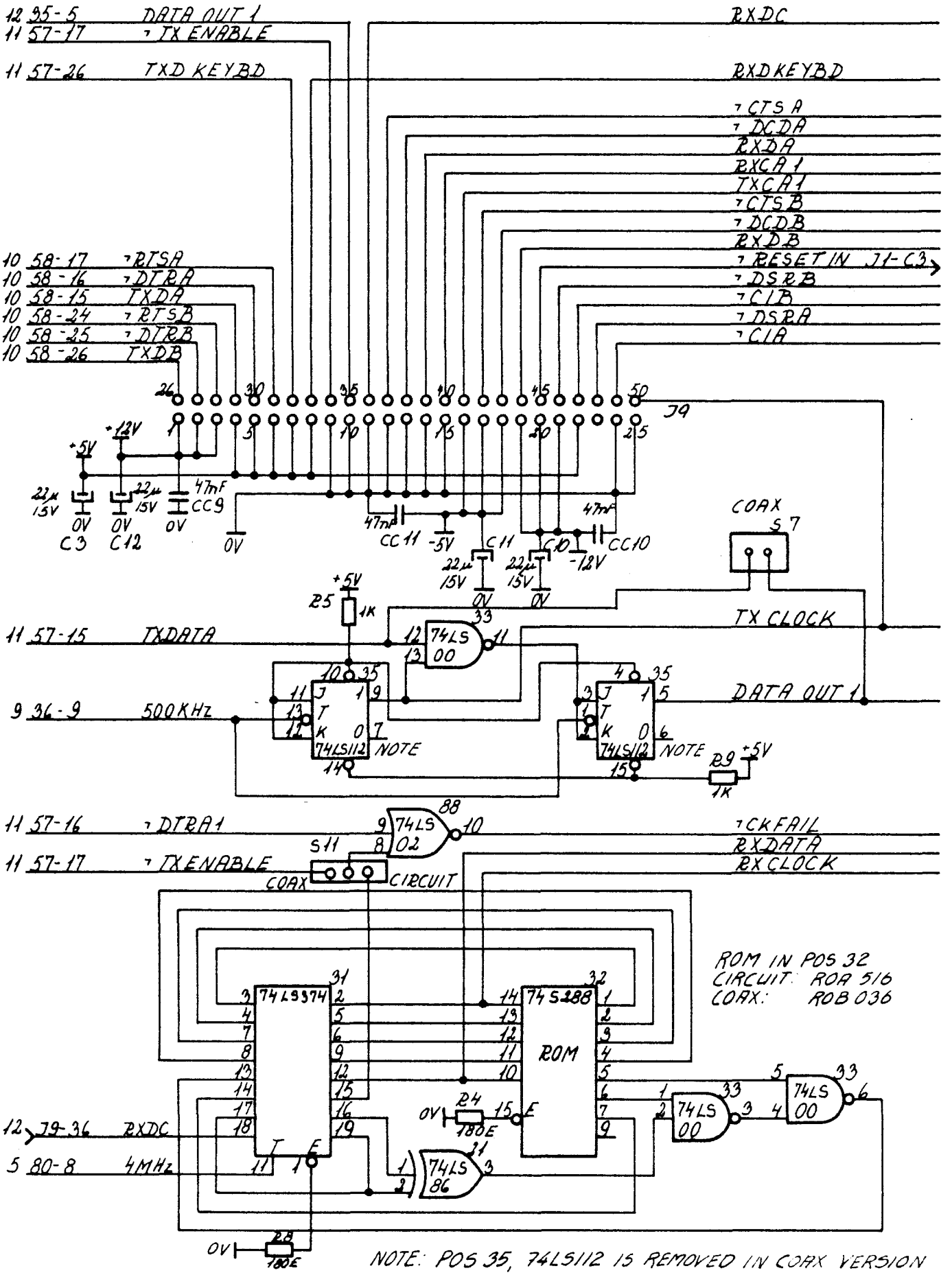


81.12.15 JPJ 82.1.18 AGA

MIC 507 SERIAL CONTROLLER FOR KEYBOARD, 30ms REALTIME CLOCK & "CIRCUIT" WITH DMA LOGIC 11

R 13336

Signal	Destination	Description
RXDC	12	RECEIVED CIRCUIT/COAX LINE SIGNAL (FM MODULATED)
RXDKEYBD	11	RECEIVED DATA FROM KEYBOARD
-,CTS A	10	CLEAR TO SEND, LINE CHANNEL
-,DCD A	10	DATA CARRIER DETECT, LINE CHANNEL
RXD A	10	RECEIVED DATA, LINE CHANNEL
RXCA1	10	RECEIVER CLOCK (EXT), LINE CHANNEL
TXCA1	10	TRANSMIT CLOCK (EXT), LINE CHANNEL
-,CTSB	10	CLEAR TO SEND, PRINTER CHANNEL
-,DCDB	10	DATA CARRIER DETECT, PRINTER CHANNEL
RXDB	10	RECEIVED DATA, PRINTER CHANNEL
-,RESET IN	2	MANUAL RESET
-,DSR B	10	DATA SET READY, PRINTER CHANNEL
-,CIB	10	CALLING INDICATOR, PRINTER CHANNEL
-,DSR A	10	DATA SET READY, LINE CHANNEL
-,CIA	10	CALLING INDICATOR, LINE CHANNEL
TX CLOCK	11	TRANSMIT CLOCK FOR CIRCUIT/COAX - SIO CIRCUIT: 250 KHz FROM U35 PIN 9 COAX: 540 KHz FROM J9 PIN 50 (U35, 74LS112 NOT MOUNTED)
DATA OUT1	12	CIRCUIT: 250 KBPS FM MODULATED DATA COAX: SERIAL DATA DIRECTLY FROM SIO (U35 REMOVED, S7 SHORTED)
-,CKFAIL	11	CIRCUIT: CLOCK FAILURE, A CLOCK PERIOD BEING TOO LONG HAS BEEN DETECTED BY THE DEMODULATOR (AS WHEN CARRIER IS REMOVED)
RX DATA	11	DEMODULATED DATA
RX CLOCK	11	DEMODULATED CLOCK



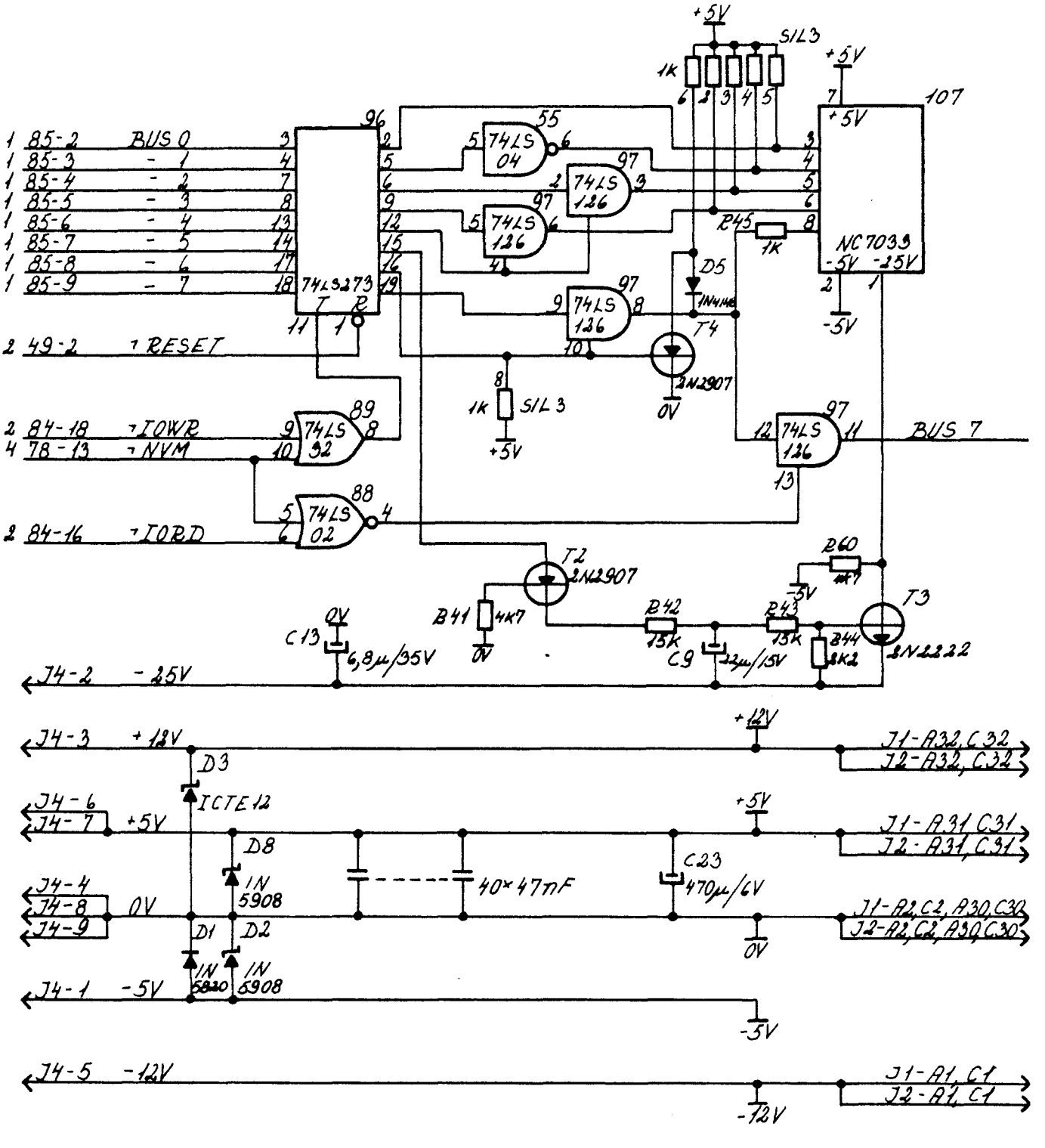
MIC 507

B13337

50 PIN FLAT-CABLE CONNECTOR &
CIRCUIT MODULATOR / DEMODULATOR

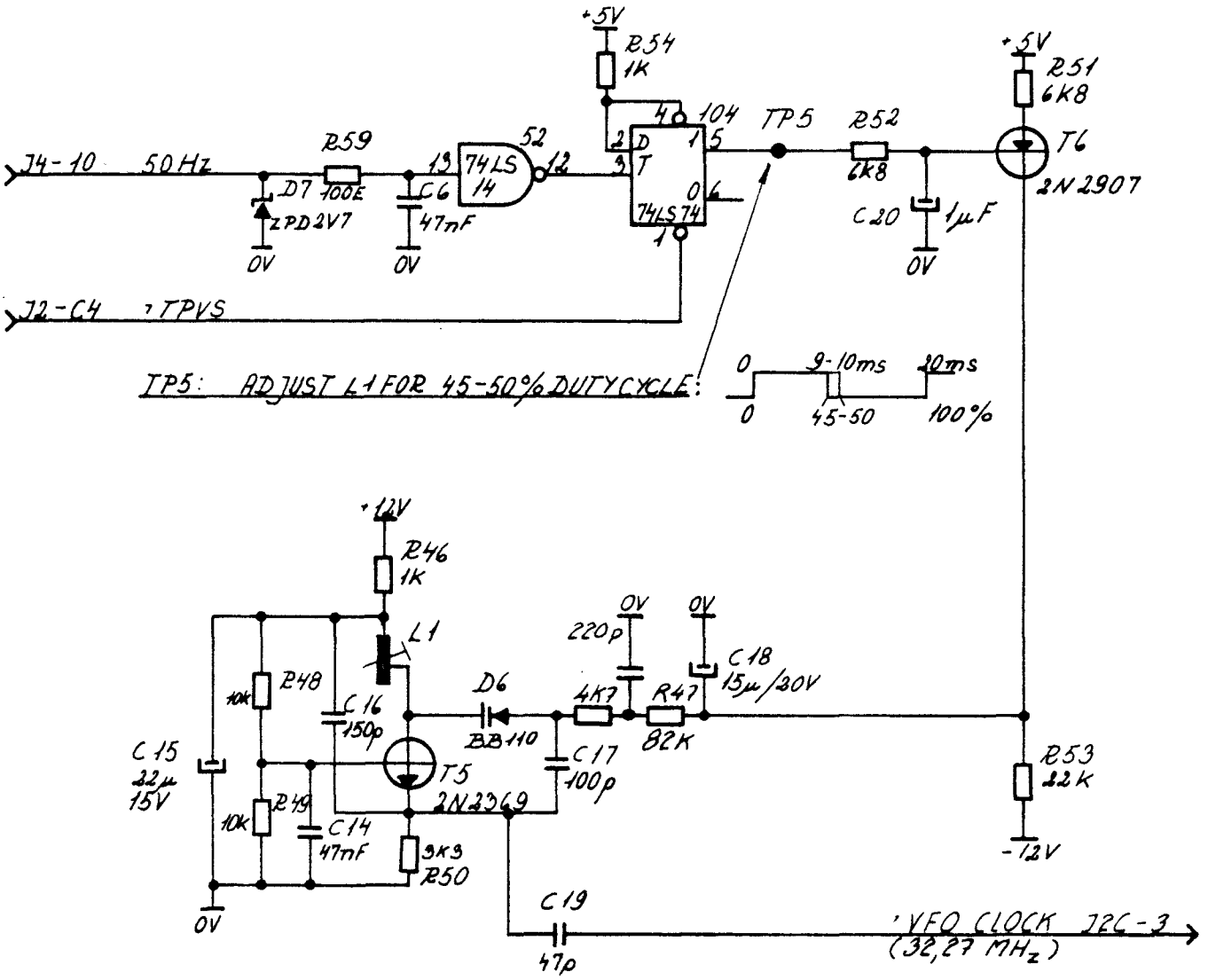
12

Signal	Destination	Description
BUS 7	1, J1,J2	CPU EXTERNAL DATA BUS BIT 7



AGA 82.1.19
JPJ 81.12.15

Signal	Destination	Description
-,VFO CLOCK	J2	32,27 MHz VFO CLOCK SIGNAL TO CRT-CONTROLLER WHERE THE SIGNAL IS CONVERTED TO TTL-LEVEL



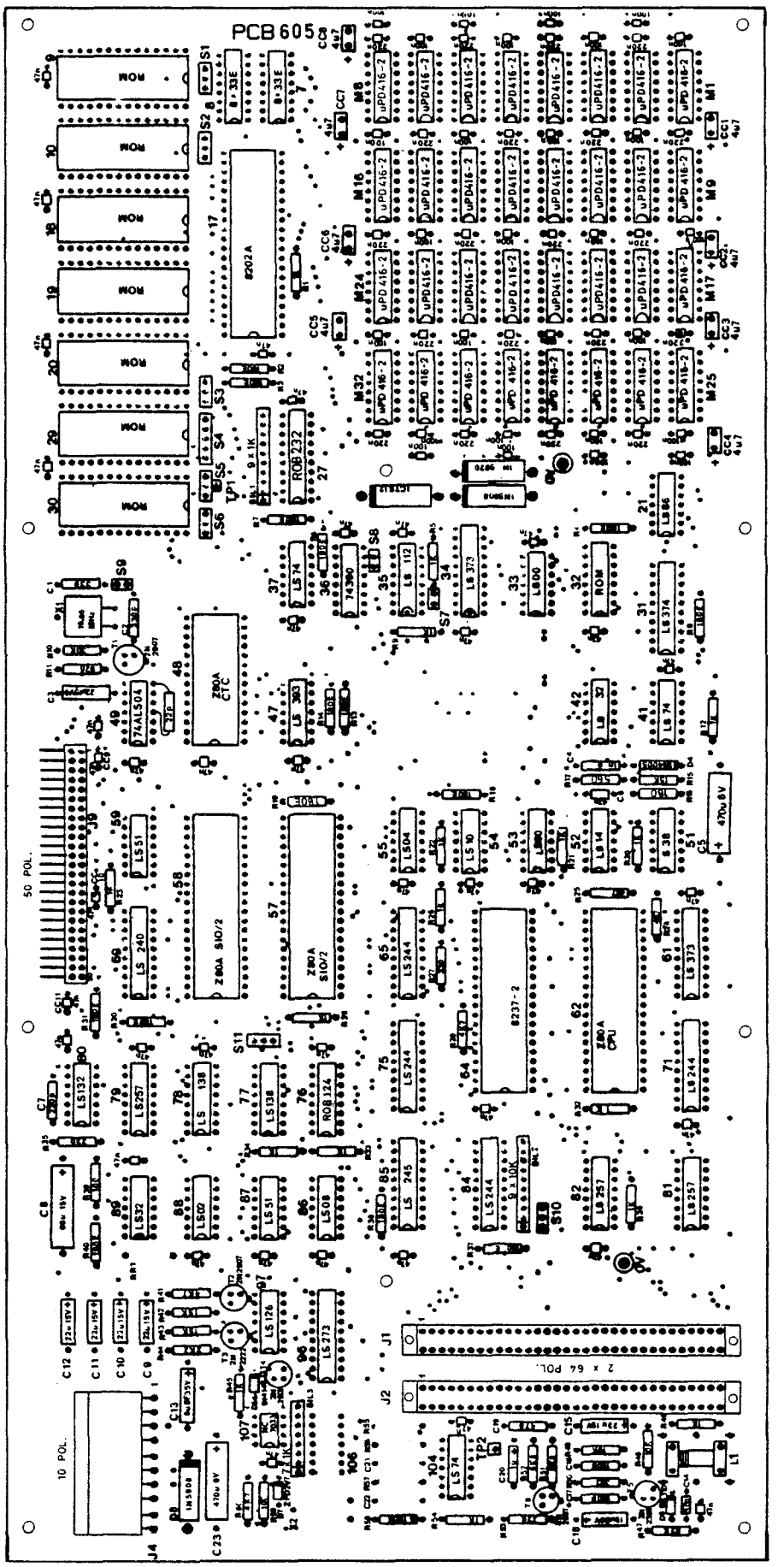
81.12.15 JPJ 82.1.19 AGA

MIC 507
R13339

PHASE LOCKED OSCILLATOR FOR DISPLAY CONTROLLER

5. ASSEMBLY DRAWING

5.

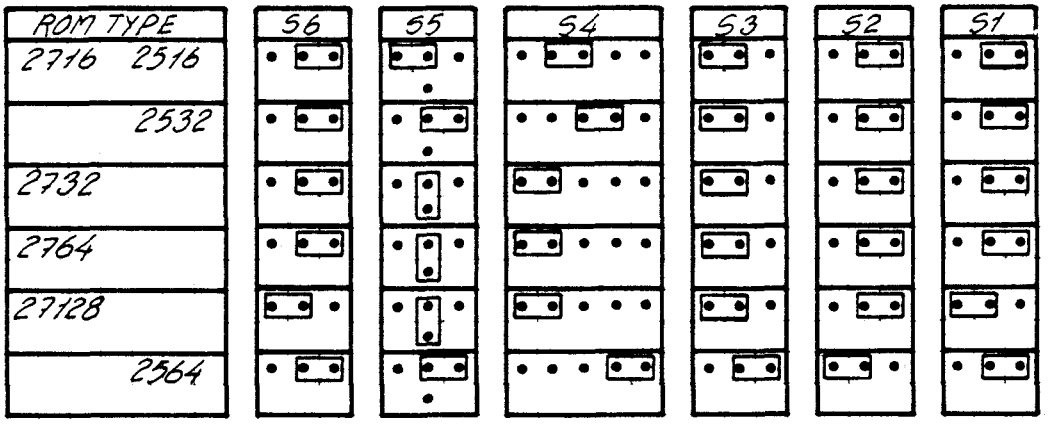


6. STRAPPINGS 6.

The MIC-board has 11 strap positions of which one is for test purpose (S9), 6 for ROM-type selection (S1-S6), 3 allows configuring for either CIRCUIT or COAX (S7, S8 and S11) and one strap allows an additional interrupt controller to be inserted in the priority chain on a controller card connected to J1.

All strapping are made by a mini-jump connector shorting two adjacent pins in a strapping position.

Test strap S9 disconnects 19.66 MHz X-tal for test purpose if removed (stops oscillator). Rom type selection straps S1-S6 are set according to the following table.



CIRCUIT/COAX-strapping is done as shown in the following table (S11 is shown as seen from component side and J1, J2 to the lefthand side).

	S11	S7	S8	Pos. 35 (74LS112)	DECODER ROM IN Pos. 32
CIRCUIT	• ▮ •	• •	▭	MOUNTED	ROM 516
COAX	▮ •	▭	• •	REMOVED	ROM036

The external interrupt controller strap, S10 is placed in the righthand position (away from J1, J2) when no controller or a controller without its own interrupt controller is placed in J1.

If a controller in J1 has to use the serial priority chain then the strap must be placed in the lefthand position (toward J1, J2).

7. ROM LISTINGS 7.

RAM/ROM decoder, ROB232

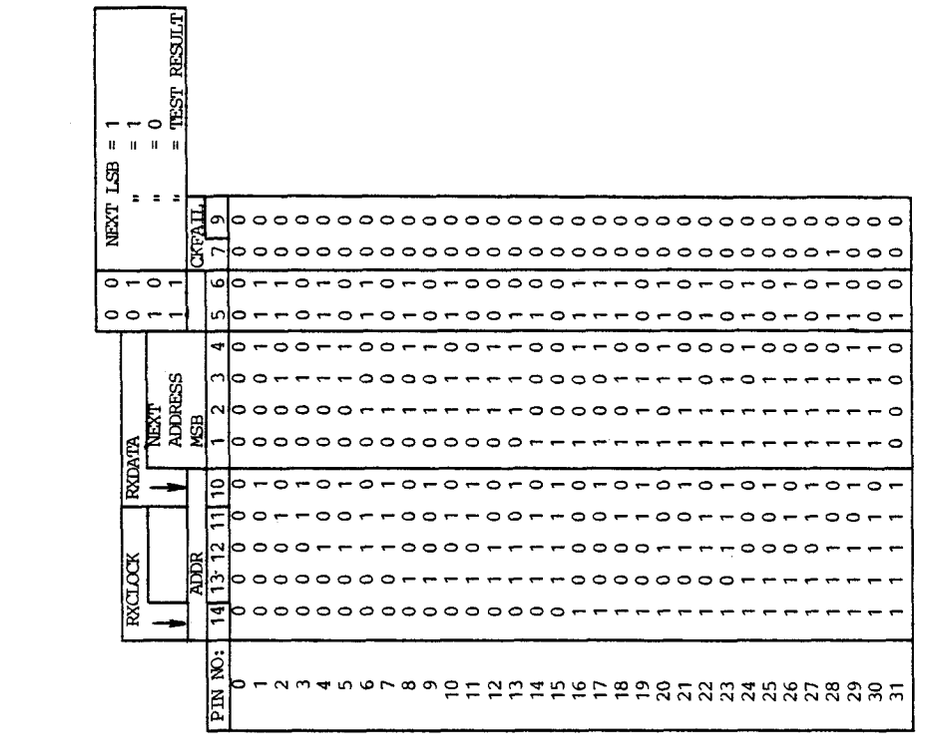
RAM/ROM CONTROL OUT. ADDRESS (HEX)	ROM ADDRESS INPUT								CONTROL FUNCTION
1B	0	x	x	x	x	0	x		DISABLE ROM (=RESET)
19	0	x	x	x	x	1	x		DISABLE ROM
1A	1	x	x	x	x	0	x		ENABLE ROM 0-16K
18	1	x	x	x	x	1	x		ENABLE ROM 0-56K
	↓					↓			
	ROM ENABLE	ADD 15	ADD 14	ADD 13	ADD 12	ADD 11	BOOT ENABLE	HOLD ACK	CHIP SELECTS: ROM 6 / ROM 5 / ROM 4 / RAM / ROM 3 / ROM 2 / ROM 1 / ROM 0

ROM ADDRESSES (HEX)	ROM PIN NO'S 19	18	17	5	4	3	2	1	ROM PIN NO'S 14	13	12	11	9	8	7	6	HEX DATA	
00 - 7F	0	x	x	x	x	x	x	x	1	1	1	0	1	1	1	1	EF	RAM 0-64K
80 - 8F	1	0	0	0	x	x	x	0	1	1	1	0	1	1	1	1	EF	RAM
	1	0	0	0	x	x	x	1	1	1	1	1	1	1	1	0	FE	ROM 0-8K
90 - 9F	1	0	0	1	x	x	x	0	1	1	1	0	1	1	1	1	EF	RAM
	1	0	0	1	x	x	x	1	1	1	1	1	1	1	0	1	FD	ROM 8-16K
A0 - AF	1	0	1	0	x	x	0	0	1	1	1	0	1	1	1	1	EF	RAM
	1	0	1	0	x	x	0	1	1	1	1	0	1	1	1	1	EF	RAM
	1	0	1	0	x	x	1	0	1	1	1	0	1	1	1	1	EF	RAM
	1	0	1	0	x	x	1	1	1	1	1	1	1	0	1	1	FB	ROM 16-24K
B0 - BF	1	0	1	1	x	x	0	0	1	1	1	0	1	1	1	1	EF	RAM
	1	0	1	1	x	x	0	1	1	1	1	0	1	1	1	1	EF	RAM
	1	0	1	1	x	x	1	0	1	1	1	0	1	1	1	1	EF	RAM
	1	0	1	1	x	x	1	1	1	1	1	1	0	1	1	1	F7	ROM 24-32K
C0 - CF	1	1	0	0	x	x	0	0	1	1	1	0	1	1	1	1	EF	RAM
	1	1	0	0	x	x	0	1	1	1	1	0	1	1	1	1	EF	RAM
	1	1	0	0	x	x	1	0	1	1	1	0	1	1	1	1	EF	RAM
	1	1	0	0	x	x	1	1	1	1	0	1	1	1	1	1	DF	ROM 32-40K
D0 - DF	1	1	0	1	x	x	0	0	1	1	1	0	1	1	1	1	EF	RAM
	1	1	0	1	x	x	0	1	1	1	1	0	1	1	1	1	EF	RAM
	1	1	0	1	x	x	1	0	1	1	1	0	1	1	1	1	EF	RAM
	1	1	0	1	x	x	1	1	1	0	1	1	1	1	1	1	BF	ROM 40-48K
E0 - EF	1	1	1	0	x	x	0	0	1	1	1	0	1	1	1	1	EF	RAM
	1	1	1	0	x	x	0	1	1	1	1	0	1	1	1	1	EF	RAM
	1	1	1	0	x	x	1	0	1	1	1	0	1	1	1	1	EF	RAM
	1	1	1	0	x	x	1	1	0	1	1	1	1	1	1	1	7F	ROM 48-56K
F0 - FF	1	1	1	1	x	x	0	0	1	1	1	0	1	1	1	1	EF	RAM
	1	1	1	1	x	x	0	1	1	1	1	0	1	1	1	1	EF	RAM
	1	1	1	1	x	x	1	0	1	1	1	0	1	1	1	1	EF	RAM
	1	1	1	1	x	x	1	1	1	1	1	0	1	1	1	1	EF	RAM

INT/EXT I/O decoder, ROB124

CPU I/O ADDRESS RANGE (HEX)		ROM ADDR (DEC)	ROM ADDRESS PINS	ROM DATA PINS		
				7 EN DMA		
				7 EN EXT I/O		
FROM	TO		AD:7 6 5 4 3 PI:14 13 12 11 10	PIN: 9 7 6 5 4 3	2	1
00	07	0	0 0 0 0 0	0 0 0 0 0 0	0	1
08	0F	1	0 0 0 0 1	. .	1	1
10	17	2	0 0 0 1 0	. .	0	1
18	1F	3	0 0 0 1 1	. .	1	1
20	27	4	0 0 1 0 0	. .	0	1
28	2F	5	0 0 1 0 1	. .	0	1
30	37	6	0 0 1 1 0	. .	1	1
38	3F	7	0 0 1 1 1	. .	0	1
40	47	8	0 1 0 0 0	. .	0	1
48	4F	9	0 1 0 0 1	. .	0	1
50	57	10	0 1 0 1 0	. .	0	1
58	5F	11	0 1 0 1 1	. .	0	1
60	67	12	0 1 1 0 0	. .	0	1
68	6F	13	0 1 1 0 1	. ALL .	0	1
70	77	14	0 1 1 1 0	. ZERO .	0	1
78	7F	15	0 1 1 1 1	. .	0	1
80	87	16	1 0 0 0 0	. .	0	1
88	8F	17	1 0 0 0 1	. .	0	1
90	97	18	1 0 0 1 0	. .	0	1
98	9F	19	1 0 0 1 1	. .	0	1
A0	A7	20	1 0 1 0 0	. .	0	1
A8	AF	21	1 0 1 0 1	. .	0	1
B0	B7	22	1 0 1 1 0	. .	0	1
B8	BF	23	1 0 1 1 1	. .	0	1
C0	C7	24	1 1 0 0 0	. .	0	1
C8	CF	25	1 1 0 0 1	. .	0	1
D0	D7	26	1 1 0 1 0	. .	0	1
D8	DF	27	1 1 0 1 1	. .	0	1
E0	E7	28	1 1 1 0 0	. .	0	1
E8	EF	29	1 1 1 0 1	. .	0	1
F0	F7	30	1 1 1 1 0	. .	1	0
F8	FF	31	1 1 1 1 1	0 0 0 0 0 0	1	0

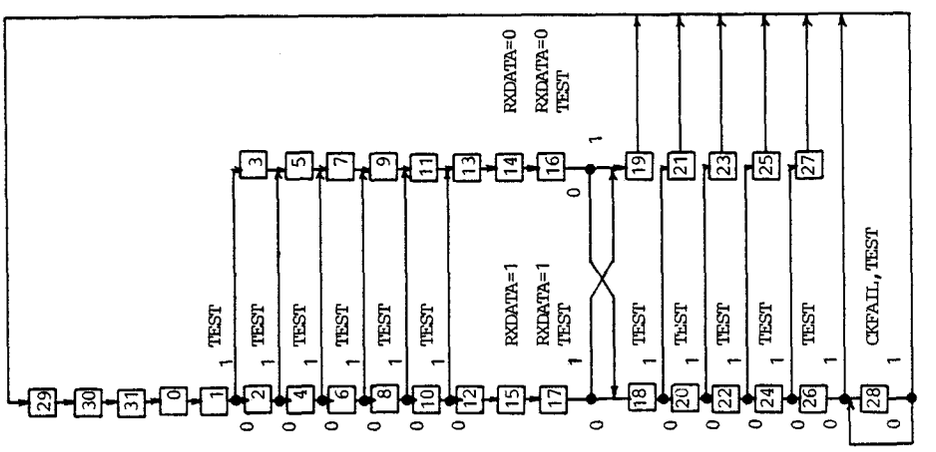
Circuit decoder, ROA516



PIN NO:	14	13	12	11	10	RXCLOCK / ADDR	RXDATA / NEXT ADDRESS MSB 1	2	3	4	5	6	CKFAIL 7	9
0	0	0	0	0	0		0	0	0	0	0	0	0	0
1	0	0	0	0	1		0	0	0	1	1	1	0	0
2	0	0	0	1	0		0	0	1	0	1	1	0	0
3	0	0	0	1	1		0	0	1	1	0	0	0	0
4	0	0	1	0	0		0	0	1	1	0	0	0	0
5	0	0	1	0	1		0	0	1	1	1	1	0	0
6	0	0	1	1	0		0	0	1	0	0	1	0	0
7	0	0	1	1	1		0	0	1	0	1	0	0	0
8	0	1	0	0	0		0	0	1	1	0	1	0	0
9	0	1	0	0	1		0	0	1	1	1	0	0	0
10	0	1	0	1	0		0	0	1	0	0	1	0	0
11	0	1	0	1	1		0	0	1	0	1	0	0	0
12	0	1	1	0	0		0	0	1	1	0	1	0	0
13	0	1	1	0	1		0	0	1	1	1	0	0	0
14	0	1	1	1	0		0	0	1	0	0	1	0	0
15	0	1	1	1	1		0	0	1	0	1	0	0	0
16	1	0	0	0	0		0	0	1	1	0	1	0	0
17	1	0	0	0	1		0	0	1	1	1	0	0	0
18	1	0	0	1	0		0	0	1	0	0	1	0	0
19	1	0	0	1	1		0	0	1	0	1	0	0	0
20	1	0	1	0	0		0	0	1	1	0	1	0	0
21	1	0	1	0	1		0	0	1	1	1	0	0	0
22	1	0	1	1	0		0	0	1	0	0	1	0	0
23	1	0	1	1	1		0	0	1	0	1	0	0	0
24	1	1	0	0	0		0	0	1	1	0	1	0	0
25	1	1	0	0	1		0	0	1	1	1	0	0	0
26	1	1	0	1	0		0	0	1	0	0	1	0	0
27	1	1	0	1	1		0	0	1	0	1	0	0	0
28	1	1	1	0	0		0	0	1	1	0	1	1	0
29	1	1	1	0	1		0	0	1	1	1	0	0	0
30	1	1	1	1	0		1	1	1	1	0	0	0	0
31	1	1	1	1	1		0	0	0	0	1	0	0	0

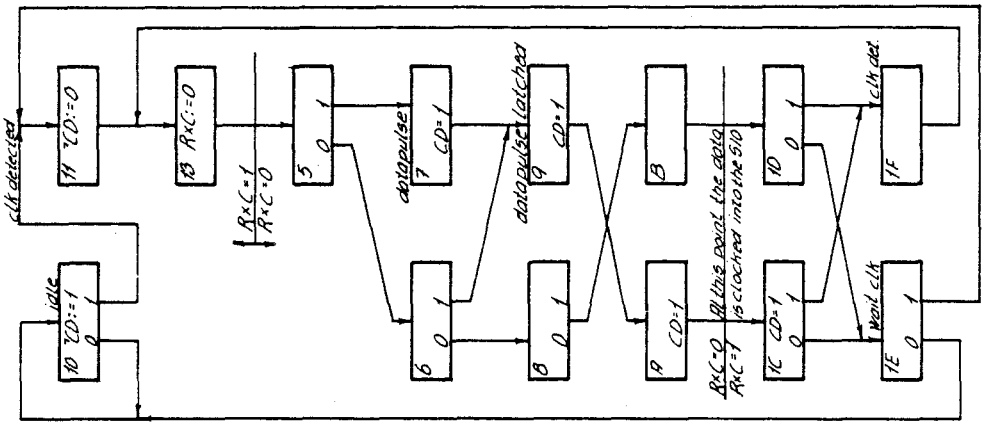
NEXT LSB = 1
" = 1
" = 0
" = TEST RESULT

ROA 516



SEQUENCE DIAGRAM

Coax decoder, ROB036



8. PLUG LISTS

8.

J1 - CONNECTOR, OPTIONS

A-ROW			C-ROW		
PIN	SOURCE	MNEMONIC	PIN	SOURCE	MNEMONIC
1		-12V	1		-12V
2		0V	2		0V
3		-,FDINTR	3		-,RESET IN
4	84-16	-,IORD	4		
5	84-18	-,IOWR	5		
6	84-12	-,MEMRD	6		-,DRQ3
7	84-14	-,MEMWR	7	64-36	-,TC
8	85-3	BUS 1	8	85-2	BUS 0
9	85-5	BUS 3	9	85-4	BUS 2
10	85-7	BUS 5	10	85-6	BUS 4
11	85-9	BUS 7	11	85-8	BUS 6
12		-,INT	12	84-5	-,IORQBUF
13	75-9	ADD 0	13	75-5	ADD 2
14		CHAIN 3 IN	14	S10	CHAIN 3 OUT
15	65-5	-,M1BUF	15	75-7	ADD 1
16	75-18	ADD 4	16	84-7	-,RDBUF
17		-,WAIT	17	75-3	ADD 3
18	75-16	ADD 5	18	61-19	ADD 15
19	75-14	ADD 6	19	61-16	ADD 14
20	75-12	ADD 7	20	61-15	ADD 13
21	64-24	-,DACK 1	21	61-12	ADD 12
22	64-15	-,DACK 3	22	61-9	ADD 11
23		-,DRQ 1	23	61-6	ADD 10
24	84-9	-,WRBUF	24	61-5	ADD 9
25	84-3	-,MREQBUF	25	61-2	ADD 8
26			26		-,NMI
27	65-9	CLK	27	49-2	-,RESET
28	65-7	-,HOLDACK	28	65-3	-,HALTBUF
29	51-3	-,HOLD	29	36-3	9.83 MHz
30		0V	30		0V
31		+5V	31		+5V
32		+12V	32		+12V

J2 - CONNECTOR, DISPLAY CONTROLLER

A-ROW			C-ROW		
PIN	SOURCE	MNEMONIC	PIN	SOURCE	MNEMONIC
1		-12V	1		-12V
2		0V	2		0V
3		-,DISPINTR	3	C19	-,VFO CLOCK
4	84-16	-,IORD	4		-,TPVS
5	84-18	-,IOWR	5		25 Hz
6	84-12	-,MEMRD	6		-,DRQ3
7	84-14	-,MEMWR	7	64-36	-,TC
8	85-3	BUS 1	8	85-2	BUS 0
9	85-5	BUS 3	9	85-4	BUS 2
10	85-7	BUS 5	10	85-6	BUS 4
11	85-9	BUS 7	11	85-8	BUS 6
12		-,INT	12	84-5	-,IORQBUF
13	75-9	ADD 0	13	75-5	ADD 2
14			14		CHAIN 3 IN
15	65-5	-,M1BUF	15	75-7	ADD 1
16	75-18	ADD 4	16	84-7	-,RDBUF
17		-,WAIT	17	75-3	ADD 3
18	75-16	ADD 5	18	61-19	ADD 15
19	75-14	ADD 6	19	61-16	ADD 14
20	75-12	ADD 7	20	61-15	ADD 13
21	64-25	-,DACK 0	21	61-12	ADD 12
22	64-15	-,DACK 3	22	61-9	ADD 11
23		-,DRQ 0	23	61-6	ADD 10
24	84-9	-,WRBUF	24	61-5	ADD 9
25	84-3	-,MREQBUF	25	61-2	ADD 8
26			26		-,NMI
27	65-9	CLK	27	49-2	-,RESET
28	65-7	-,HOLDACK	28		
29			29	52-2	-,POWER RESET
30		0V	30		0V
31		+5V	31		+5V
32		+12V	32		+12V

J4 - POWER CONNECTOR

PIN	MNEMONIC
1	-5V
2	-25V
3	+12V
4	0V
5	-12V
6	+5V
7	+5V
8	0V
9	0V
10	50 Hz, LINE FREQ

J9 - CONNECTOR TO COI

PIN	SOURCE	MNEMONIC	PIN	SOURCE	MNEMONIC
1	J4-3	+12V	26	58-26	TXDB
2	J4-3	+12V	27	58-25	-,DTRB
3	J4-6,J4-7	+5V	28	58-24	-,RTSB
4	-	+5V	29	58-15	TXDA
5	-	+5V	30	58-16	-,DTRA
6	-	+5V	31	58-17	-,RTSA
7	-	+5V	32	57-26	TXD KEYBD
8	-	+5V	33		RXD KEYBD
9	j4-4,J4-8, J4-9	0V	34	57-17	-,TX ENABLE
10	-	0V	35	35-5	DATA OUT 1
11	-	0V	36		RXDC
12	-	0V	37		-,CTSA
13	-	0V	38		-,DCDA
14	-	0V	39		RXDA
15	-	0V	40		RSCA1
16	J4-1	-5V	41		TXCA1
17	-	-5V	42		-,CTSB
18	-	-5V	43		-,DCDB
19	J4-5	-12V	44		RXDB
20	-	-12V	45		-,RESET IN
21	-	-12V	46		-,DSRB
22	J4-6,J4-7	+5V	47		-,CIB
23		NO. CONN.	48		-,DSRA
24	J4-4,J4-8 J4-9	0V	49		-,CIA
25	-	0V	50		TXCLOCK

Nitron NC 7033

21 x 16 MNOS EAROM

DESCRIPTION

The NC 7033 is a low-cost 21 word by 16 bit electrically alterable nonvolatile memory designed especially for use in those systems which require secure, yet alterable, data storage. Data integrity is maintained for a minimum of one year between rewrites and is immune to sudden power outages.

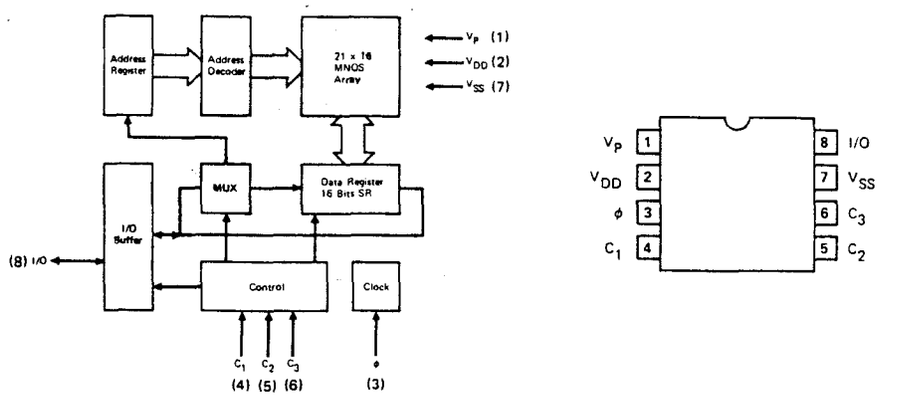
FEATURES

- 21 x 16 ORGANIZATION
- LOW-COST PACKAGING
- SERIAL INPUT/OUTPUT
- FULLY DECODED ADDRESSING
- SINGLE-WORD ALTERABLE
- SIMPLE INTERFACE REQUIREMENTS
- SIMPLE REFRESH CAPABILITY
- TYPICAL 10-YEAR UNPOWERED RETENTION

APPLICATIONS

- MICROPROCESSOR PERIPHERAL MEMORY
- BACKUP MEMORIES
- PRESET FREQUENCY TUNING FOR TV'S
- NUMERICAL MACHINE CONTROLS
- PROCESS CONTROLLERS
- REMOTE OR PORTABLE DATA ACQUISITION SYSTEMS
- STORAGE OF CALIBRATION OR TEST CONSTANTS
- PROGRAMMABLE LOCKS/SECURITY SYSTEMS

BLOCK DIAGRAM AND PIN CONNECTION



ABSOLUTE MAXIMUM RATINGS

Operating Temperature	0 to 70°C
Storage Temperature (Power Off) (NC7033L)	−55 to 150°C
Storage Temperature (Power Off) (NC7033P)	−55 to 125°C
Non Powered Data Storage	−20 to 100°C
Voltage, any Pin except V_P	V_{SS} +0.3V to V_{SS} −20V
Voltage at V_P, all others to V_{SS}	V_{SS} +0.3V to V_{SS} −38V

DC CHARACTERISTICS

For: $T_A = 0°C$ to 70°C, $V_{SS} = 10V \pm 1V$, $V_{DD} = 0V$, $V_P = -20V \pm 1V$

Parameter	Pin	Symbol	Min.	Typ.	Max.	Conditions
V_{SS} Supply Current V_P Supply Current	V_{SS} V_P	I_{SS} I_P(On) I_P(Off)		−1mA	20mA 8mA	All Modes Erase, Write Modes. Read, Setup, Standby, Serial Data Out, Serial Address In.
Output Active	I/O	I_{OH} I_{OL}	0.4mA 0.25mA			$V_{OH} = V_{SS} - 0.8V$ $V_{OL} = V_{DD} + 0.8V$
Pull-Ups to V_{SS}	C1,C2,C3,ϕ		30μA		300μA	$V_{OH} = V_{SS} - 0.8V$ $V_{OL} = V_{DD}$
Input High Voltage Input Low Voltage	I/O,C1,C2,C3	V_{IH} V_{IL}	$V_{SS} - 0.8V$		$V_{SS} + 0.4V$ $V_{SS} - 4.6V$	
Pin Capacitance	I/O,C1,C2,C3,ϕ				10pf	Pin to V_{SS}
Data Retention (Power Off or Standby Modes)	–	N_H	1.0 yr. – 2.5 yr.	3.0 yr. 10 yr.		$\leq 10^5$ ERASE/WRITE cycles $\leq 10^2$ ERASE/WRITE cycles

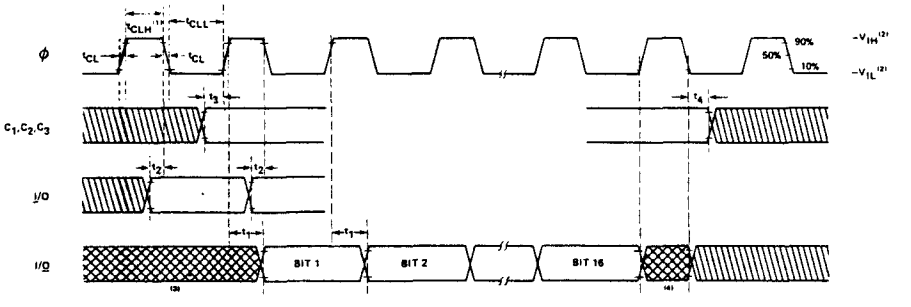
AC SWITCHING CHARACTERISTICS

For: $T_A = 0°C$ to 70°C, $V_{SS} = 10V \pm 1V$, $V_{DD} = 0V$, $V_P = -20V \pm 1V$

Parameter	Pin	Symbol	Min.	Typ.	Max.	Conditions
Clock Frequency FCL = 1/TCL	ϕ	FCL	(4)		100 KHz	
Clock High Level Hold Time	ϕ	t_{CLH}	4μs		10μs(1)	See Figure 1A
Clock Low Level Hold Time	ϕ	t_{CLL}	5μs			See Figure 1A
Clock Fall Time and Rise Time	ϕ	t_{CL}			1μs	See Figure 1A
Erase Time	–	t_{ERASE}	150ms	300ms	450ms	See Figure 1E
Write Time	–	t_{WRITE}	2.0ms	4.0ms	6.0ms	See Figure 1E
Erase to Write Time Ratio	–	t_E/t_W	50	75	100	See Figure 1E
Read Access Time (First bit)	I/O	t_{READ}	1 clock cycle			
Data Out Delay	I/O	t_1 (2)	50ns		2μs	See Figure 1A
Data In Setup	I/O	t_2	2μs			See Figures 1A, 1B
Instruction Setup Lead	C1,C2,C3	t_3	2μs			See Figures 1B,1C,1D,1E
Instruction Setup Lag	C1,C2,C3	t_4	50ns			See Figures 1B,1C,1D,1E
V_P Slew Rate	V_P				1V/μsec	Power On, Off
Number of Read Cycles	–	N_R	10^9	10^{10}		
Number of Erase Cycles	–	N_E	10^5	10^6		
Number of Write Cycles	–	N_W	10^5	10^6		

NOTES: 1. Independent of clock frequency t_{CLH} maximum is 10μsec.
2. t_1 applies only during data transition.
3. Output external loading capacitance will be 10pF.
4. See Table 1.

TIMING DIAGRAMS



NOTES: 1. Independent of clock frequency t_{CLH} maximum is 10usec.
2. Defines V_{IH}, V_{IL} levels for all figures.
3. Output depends on mode; (a) Internal pull up to V_{SS} acts during Address or Data Input, (b) Hi Z all other modes except Data Out.
4. Last data bit output indeterminate during this time.

Figure 1A. GENERAL

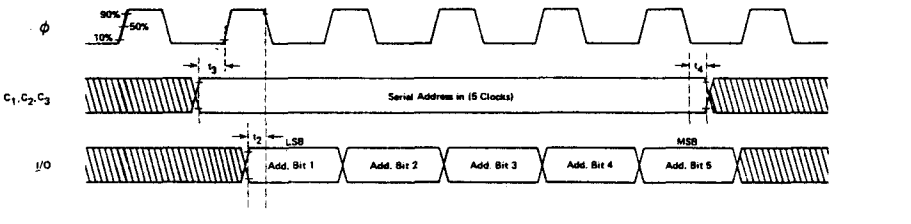


Figure 1B. SERIAL ADDRESS IN

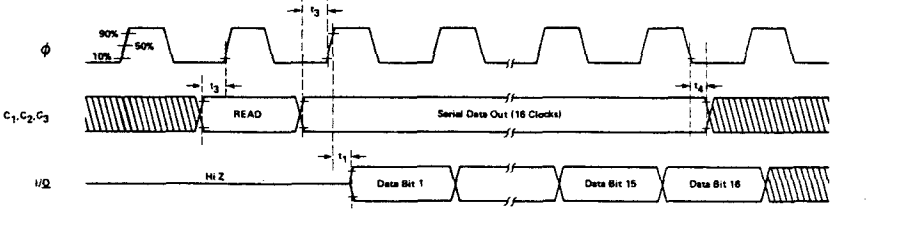


Figure 1C. READ AND SERIAL DATA OUT

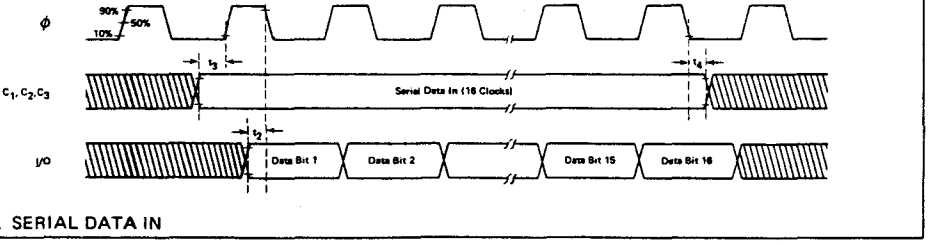


Figure 1D. SERIAL DATA IN

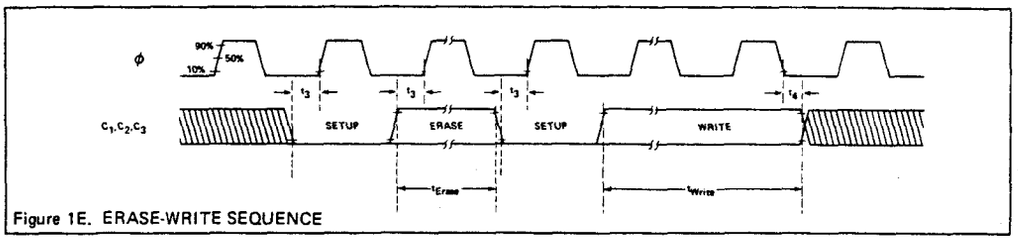


Figure 1E. ERASE-WRITE SEQUENCE

FUNCTIONAL DESCRIPTION

The NC7033 336-bit Metal-Nitride-Oxide Semiconductor (MNOS) array is organized into 21 rows of 16 bits. Each bit of storage is actually a dual-transistor pair, differentially sensed, one of which is charged to represent a logic "1" or "0." Each entire 16-bit row, or word, is individually addressable and alterable by means of three control lines (C_1, C_2, and C_3) and a serial input/output port. An external clock is used to synchronize all operations of READ, WRITE, and ERASE. In addition, the NC7033 utilizes advanced MNOS technology by eliminating the need for programming voltage (V_P) for all but ERASE and WRITE operations.

Each active (READ, ERASE, WRITE) operation is initiated by the proper sequencing of control lines followed by the appropriate 5-bit binary address code presented to the I/O port. The corresponding operation is then completed by the external clock. When not in use the NC7033 should be left either OFF or in a STANDBY condition for maximum data retention. Pull up resistors and protection diodes are on C_1, C_2, C_3 and clock inputs. I/O pull up is active only during SERIAL ADDRESS IN and SERIAL DATA IN. During SERIAL DATA OUT, I/O operates in a push-pull mode. All other modes I/O is high impedance. The following mode control functions are provided:

TABLE 1

C_1*	C_2*	C_3*	Instruction	V_P Pin**	F Clock	
					Min.	Max.
1	1	1	STANDBY	V_P,V_{DD}, Hi Z	0	100KHz
0	0	1	ERASE	V_P	0	100KHz
0	1	0	WRITE	V_P	5KHz	100KHz
0	1	1	SERIAL DATA OUT	V_P,V_{SS}	0	100KHz
0	0	0	SETUP	V_P	20KHz	100KHz
1	0	0	SERIAL ADDRESS IN	V_P,V_{DD}, Hi Z	0	100KHz
1	0	1	SERIAL DATA IN	V_P,V_{DD}, Hi Z	0	100KHz
1	1	0	READ	V_P,V_{DD}	20KHz	100KHz

*$V_H = 1$, $V_L = 0$

**V_P can remain at its nominal voltage, or be switched to one of the conditions indicated.

READ MODE

1. The (3-bit parallel) SERIAL ADDRESS IN instruction code is presented on C_1, C_2 and C_3 while the 5-bit serial address is shifted in on the I/O bus by five clocks. The 5-bit serial address utilizes a binary decoding scheme to address all 21 words. The most significant bit enters the chip first.
2. The READ instruction is presented for one clock time. This catches the word from the new address in the NVM array and parallel-loads it into a shift register. During READ the I/O port has an active tri-state output.
3. The SERIAL DATA OUT instruction is presented for 16 clock pulses, causing the data to be shifted out on the I/O bus. Data is handled on a first-in, first-out basis. If, after 16 bits of data has been read out the control lines are left in a SERIAL DATA OUT instruction code, the data will be circulated internally to allow further readout of the same data without access to the NVM array.

ERASE/WRITE MODE

An ERASE must preceed a WRITE for any location for data to be valid. However, a location can be pre-erased and left in an erased state anytime prior to the next write.

1. The address is changed, if necessary, in the same manner as in the read mode.
2. Data is serially loaded onto the chip by presenting the SERIAL DATA IN instruction for 16 clock pulses.
3. The SETUP instruction is presented for one clock pulse.
4. The ERASE instruction is presented for a nominal 300 msec: this erases only the addressed word.
5. The SETUP instruction is presented again for one clock pulse.
6. The WRITE instruction is presented for nominal 4 milliseconds. This transfers the data to the selected address in the NVM.

If a location is written without an intervening erase cycle and with different data the result will be a random readout because both transistors in the bit-pair will be in a high state.

ERASE MODE

In addition to the ERASE/WRITE sequence described above for an individual word address, all or part of the NC7033 can be pre-erased and left ready to initiate a WRITE sequence. Such would be the case if the NC7033 were to be used as a backup memory and data transferred in the event of a power failure.

1. The address is changed in the same manner as in the readout.
2. SETUP instruction is presented for one clock pulse.
3. ERASE instruction is presented for a nominal 300 msec.
4. SETUP instruction presented again for one clock pulse.
5. Address is changed again as in #1 above and process repeated as often as desired.

It should be noted that because the ERASE mode brings both transistors in the bit pair to a low state, it does not return the data to an all-logic "0" state but rather acts as a preconditioning to the array for the next WRITE pulse. If a READ is performed after a location has been erased but not rewritten the result will be a random pattern readout.

STANDBY

The STANDBY instruction puts the memory in a quiescent state where the output is high impedance and the clock is ignored.

CLOCK

Clock presence or absence will not disturb data in the array, except that the clock must be present during READ, WRITE, and SETUP modes.

SETUP

The SETUP instruction is necessary for the ERASE and WRITE modes. It isolates the particular addressed row and prevents adjoining rows or words from being inadvertently disturbed.

RETENTION

Data retention is a measurement of data validity between refresh (rewrite) cycles. The ability to alter data yet retain it during power interruptions is unique to MNOS-LSI. Both features of alterability and retention are interrelated and require clarification. The time data remains valid is inversely related to the number of rewrite/refresh cycles. (See Figure 2.) Excessive overstress of the nitride layer by too many erase and write cycles diminishes its ability to retain a charge.

Typically, long retention is not required for most applications. Data is normally altered or rewritten long before there is any danger of loss.

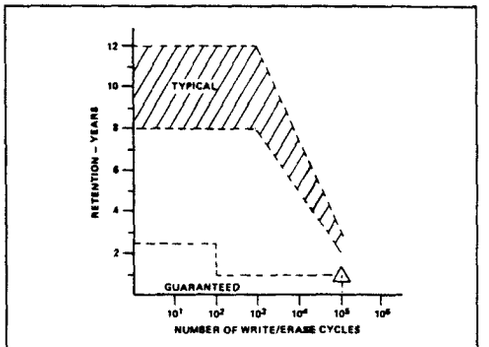


Figure 2. RETENTION CHARACTERISTICS OF MNOS.

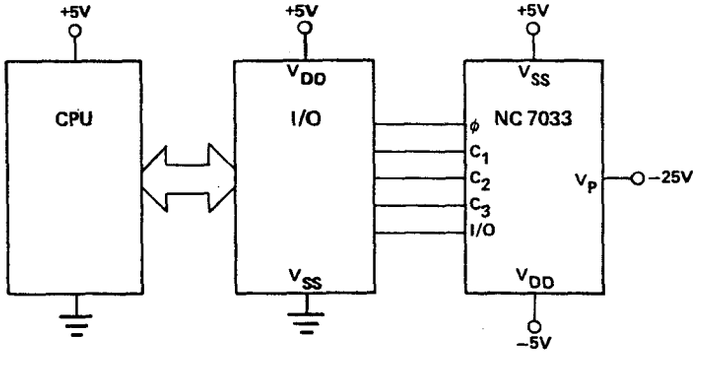
INSTRUCTION SEQUENCES

With the exception of the ERASE mode, instructions may be presented in any random sequence without disturbance of data stored in the MNOS array. For the Erase mode the instruction sequence SETUP – ERASE – SETUP must be followed.

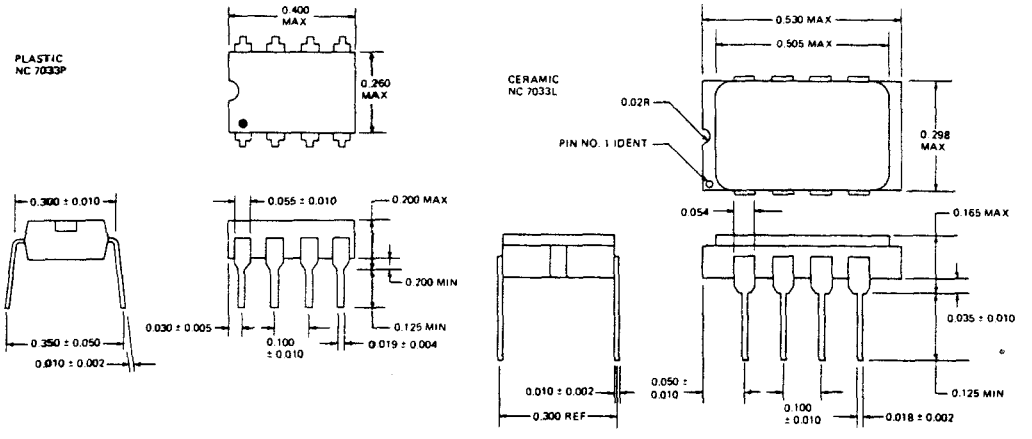
Normal sequence of operation is as follows:

1. Power On (and Off) should be made in the absence of SETUP, ERASE or WRITE instruction codes. The power supplies then can be turned on or off in any sequence without disturbance of the data. Note that when V_P is open circuit or at V_{DD} the data in the array is always protected independent of the instruction being clocked in.
2. Select SERIAL ADDRESS IN command.
3. Chip is addressed for five clocks to enter five bits of address. The 5-bit binary address code (00000 to 10100) shifts the MSB into the chip first (see Figure 1B).
4. Other functions on the selected address can be performed as shown in Figures 1C, 1D and 1E.

TYPICAL INTERFACE SCHEMATICS



PACKAGE DRAWINGS

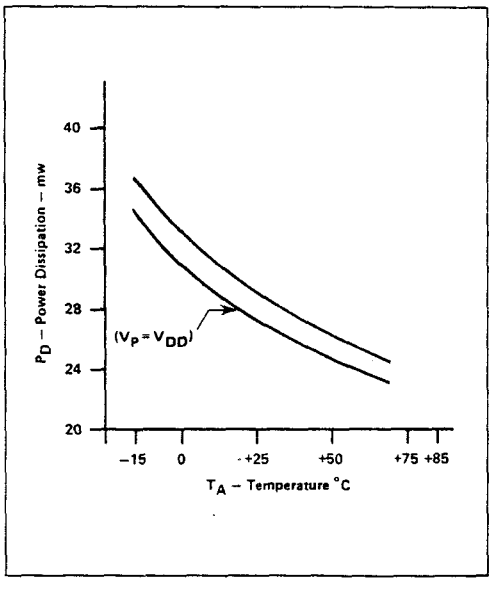


SERIAL ADDRESS IN DECODING

WORD	MSB				LSB
	B5	B4	B3	B2	B1
1	0	0	0	0	0
2	0	0	0	0	1
3	0	0	0	1	0
4	0	0	0	1	1
5	0	0	1	0	0
6	0	0	1	0	1
7	0	0	1	1	0
8	0	0	1	1	1
9	0	1	0	0	0
10	0	1	0	0	1
11	0	1	0	1	0
12	0	1	0	1	1
13	0	1	1	0	0
14	0	1	1	0	1
15	0	1	1	1	0
16	0	1	1	1	1
17	1	0	0	0	0
18	1	0	0	0	1
19	1	0	0	1	0
20	1	0	0	1	1
21	1	0	1	0	0

B5 ENTERS THE CHIP FIRST
B1 ENTERS THE CHIP LAST

TYPICAL POWER DISSIPATION CHARACTERISTICS



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