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CRT504/506 - CRT Controller
Technical Manual

RCSL No 42-I 2164

A/S REGNECENTRALEN
af 1979

Keywords:

RC850, CRT504, CRT506, CRT Controller.

Abstract:

This manual contains all relevant technical information on CRT504 and CRT506. Functionally the controllers are identical.

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RCSL No 42-I 2164

FOREWORD

First edition: RCSL No 44-RT2023.

Second edition: RCSL No 44-RT2032.

Third edition: RCSL No 44-RT2046.
The third edition is a complete reprint of the second edition, except that the identification number CRT504 has been changed to CRT504/506 throughout the text. The identification number CRT504 on the diagrams, however, has been maintained for practical reasons, yet the diagrams are valid for the CRT506 controller as well.

These changed have been made because the CRT504 and CRT506 controllers are functionally identical and as such they should be covered by one technical manual only.

Peter Koch Andersson
A/S REGNECENTRALEN af 1979, January 1983

TABLE OF CONTENTS PAGE

1. DESCRIPTION 1.

CRT504/506 is the interface between MIC50x and the CRT monitor.

CRT504/506 displayes continously the contents of a 2 k x 16 bit refresh memory, which is maintained as a copy of the highest 4 k bytes of main memory (i.e. addresses F000 to FFFF): Every time a byte is written in this area, it is written into the corresponding address of the refresh memory as well. Each pair of addresses in the refresh memory corresponds to a position on the screen.

The first byte plus one bit of the second selects a character in the character font to be displayed. Two bits in the second select a shadow character to be superponed the first. The remaining bits (the attribute selectors) select one out of 32 programdefined combinations of the 8 attributes, which control the display of the character.

1.1 Refresh Memory 1.1

The address multiplexer U12, U11, U1 (p11) to the refresh memory is controlled by CCLK. CCLK is low during the last half of the character period, letting the CRT controller read the character for display. During the first CCLK phase however, the refresh memory is addressed with the MIC address lines, making write access possible.

The leading edge of a write to the refresh area is caught in the F.F. U16 (p11), generating a write request, which is syncronized to CCLK in the F.F. U50 (p11) which makes U40 (p11) generate a writepulse beginning after CCLK goes high and ending before CCLK goes low. U40 is reset by U60-6 giving a low pulse before CCLK falls.

During the refresh phase, the refresh memory is addressed by the CRT controller MC6845 and the read data is locked into the buffer register on the rising edge of CCLK.

1.2 Character Font 1.2

The character font consists of three memories: a ROM (U64 and U84 p5), containing predefined dot patterns for 128 or 256 characters, a RAM (M9-24 p6), with space for programming of 256 character patterns and a RAM (U66, 67, 86, 87) with space for the programming of 4 dot patterns, one of which is always superponed the character pattern displayed.

The character font contains 16 x 16 bits for each character pattern or shadow pattern and they are read with 32 bits in parallel (DOT 0-15 and SDOT0-15). The SDOT's and DOT's are "ored" together giving 16 compound dots being parallel loaded into the shifter and the shifted out one dot at the time at a frequency of 32 MHz.

1.3 Video Generation 1.3

The output of the dot shifter is used to select the display of foregound or background. Foreground and background are defined for each character position in the refresh memory by 5 bits. The 5 bits are used to select one out of 32 combinations of 8 attributes stored in the attribute RAM (U48 and U49 p3).

Seven of the attributes are converted into a back- and foreground colour or grey scale value, in the attribute ROM ROB046, U39 p3.

The last attribute bit is used to hide the character by disabling dots for that character.

The three colour signals from the dot selector go to J4 for a colour monitor or to the D/A converter on p1 generating a grey scale video signal for a BW monitor.

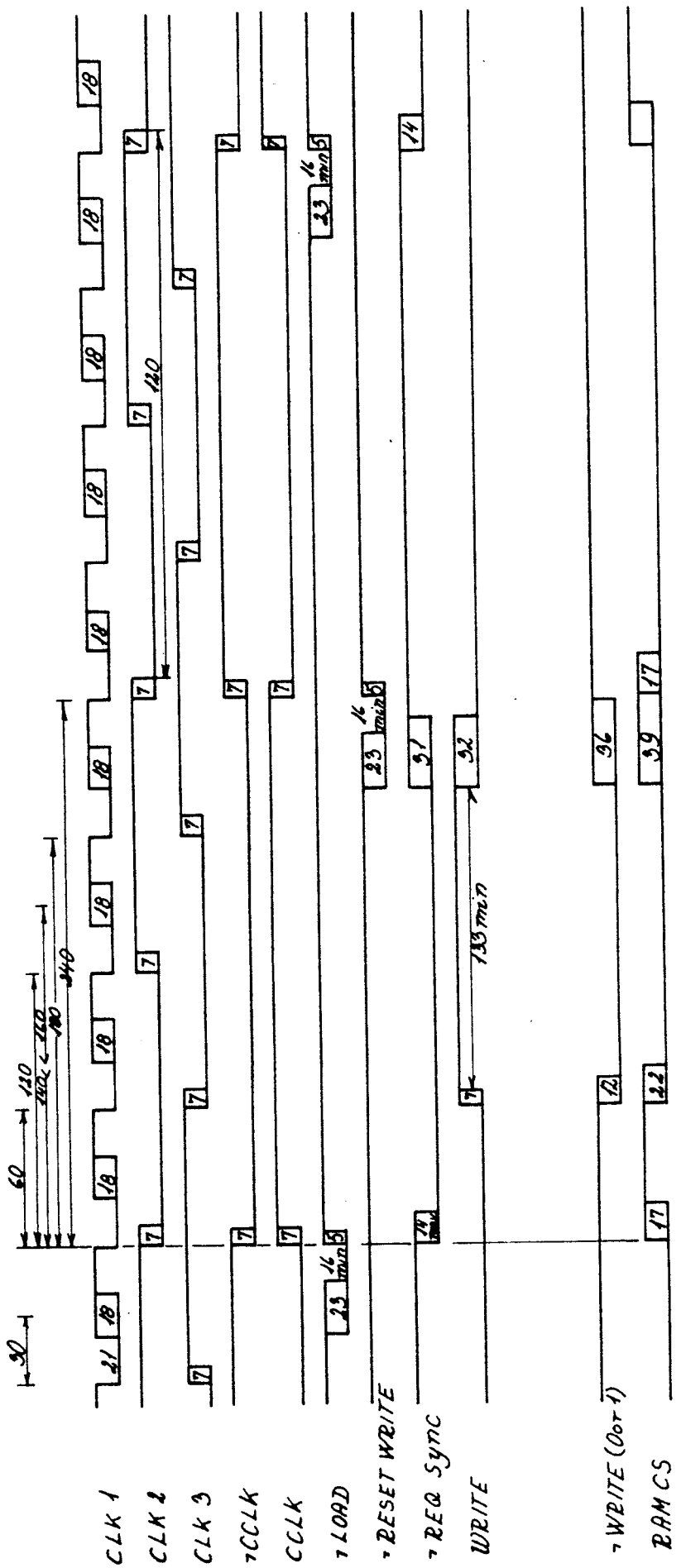
1.4 DMA 1.4

The character fonts and the attribute RAM are accessed from the MIC board via DMA, controlled by the DMA controller on the MIC board.

The memory to be accessed is selected with an I/O write command to port 20 Hex. This write command clears the load address counter and sets the DMA RUN flipflop U5a p12, which then lets the DRQ EN flip-flop U56 p12 generate a DMA REQ next time DISP EN goes low (during horizontal retrace). The DMA REQ (REQ 0) makes the DMA controller perform two DMA cycles: DRQ EN is reset only after the LA counter (bit 0) is counted up on the trailing edge of DMA ACK, this causes the DMA controller to generate the second DMA cycle. So DMA transfers take place with two bytes every 64 microsecond, always starting with the even byte.

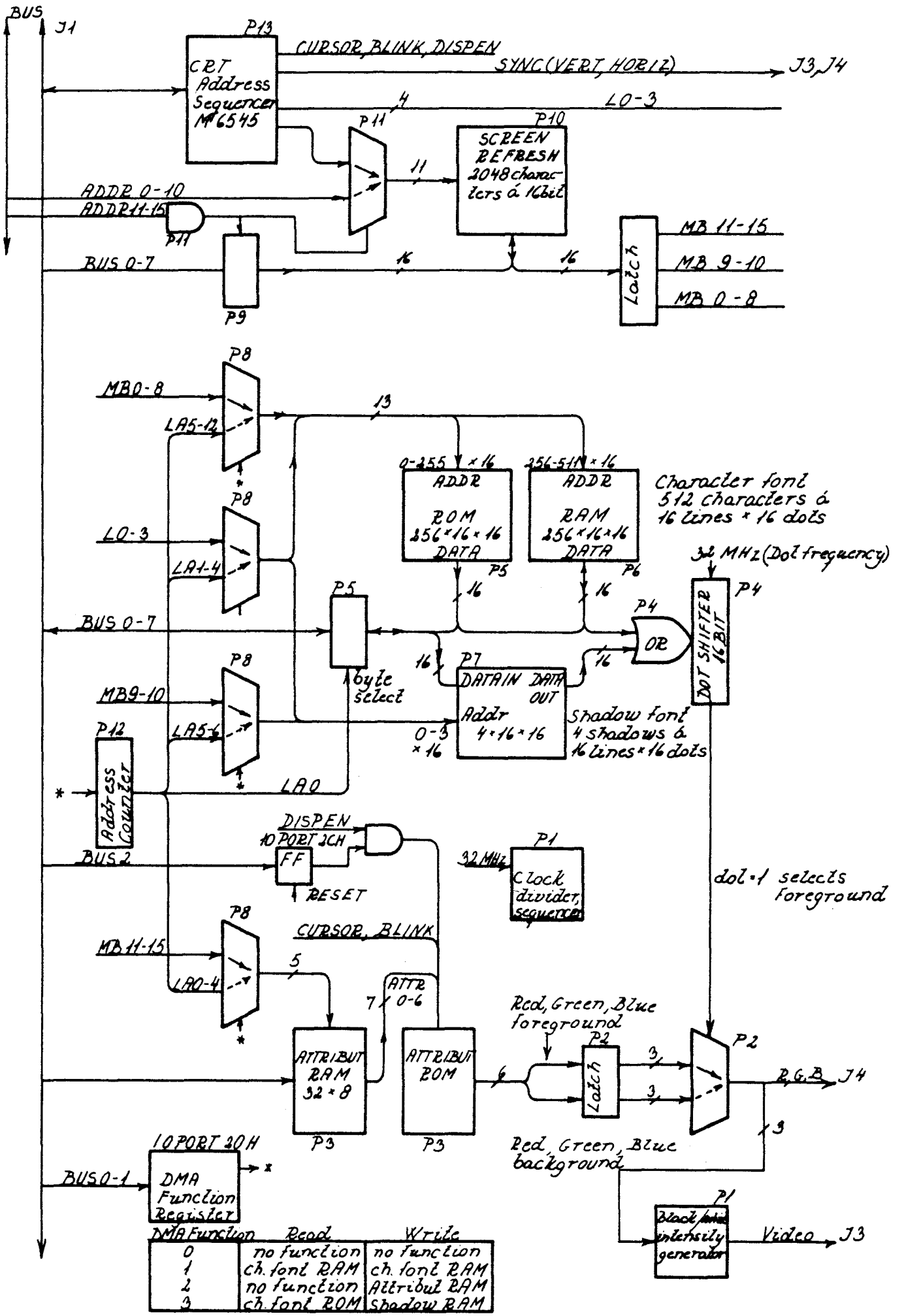
2. TIMING DIAGRAM

2.



3. BLOCK DIAGRAM

3.



DMA Function	Read	Write
0	no function	no function
1	ch. font RAM	ch. font RAM
2	no function	Attribut RAM
3	ch. font ROM	Shadow RAM

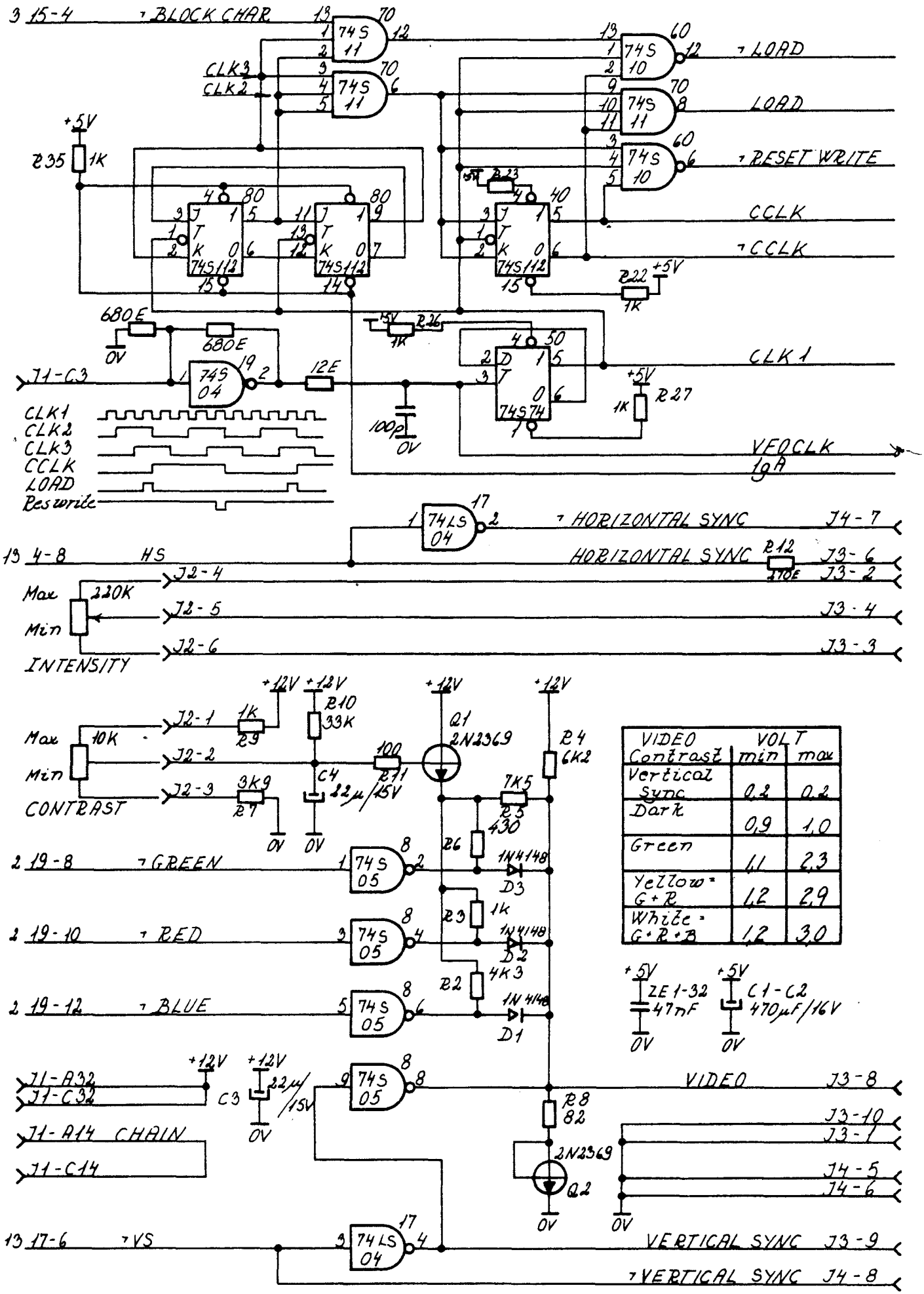
4. LOGIC DIAGRAMS AND FUNCTIONAL DESCRIPTION 4.

The following pages contain logic diagrams for CRT504/506. A functional description is given on the left hand page to the corresponding diagram sheet.

The functional description consists of a schematic listing of all signals generated on the page. A short description and a listing of the diagrams to which the signal is transferred is given for each signal.

Note: All references between individual diagram sheets make use of diagram numbers (lower right corner) and not page numbers.

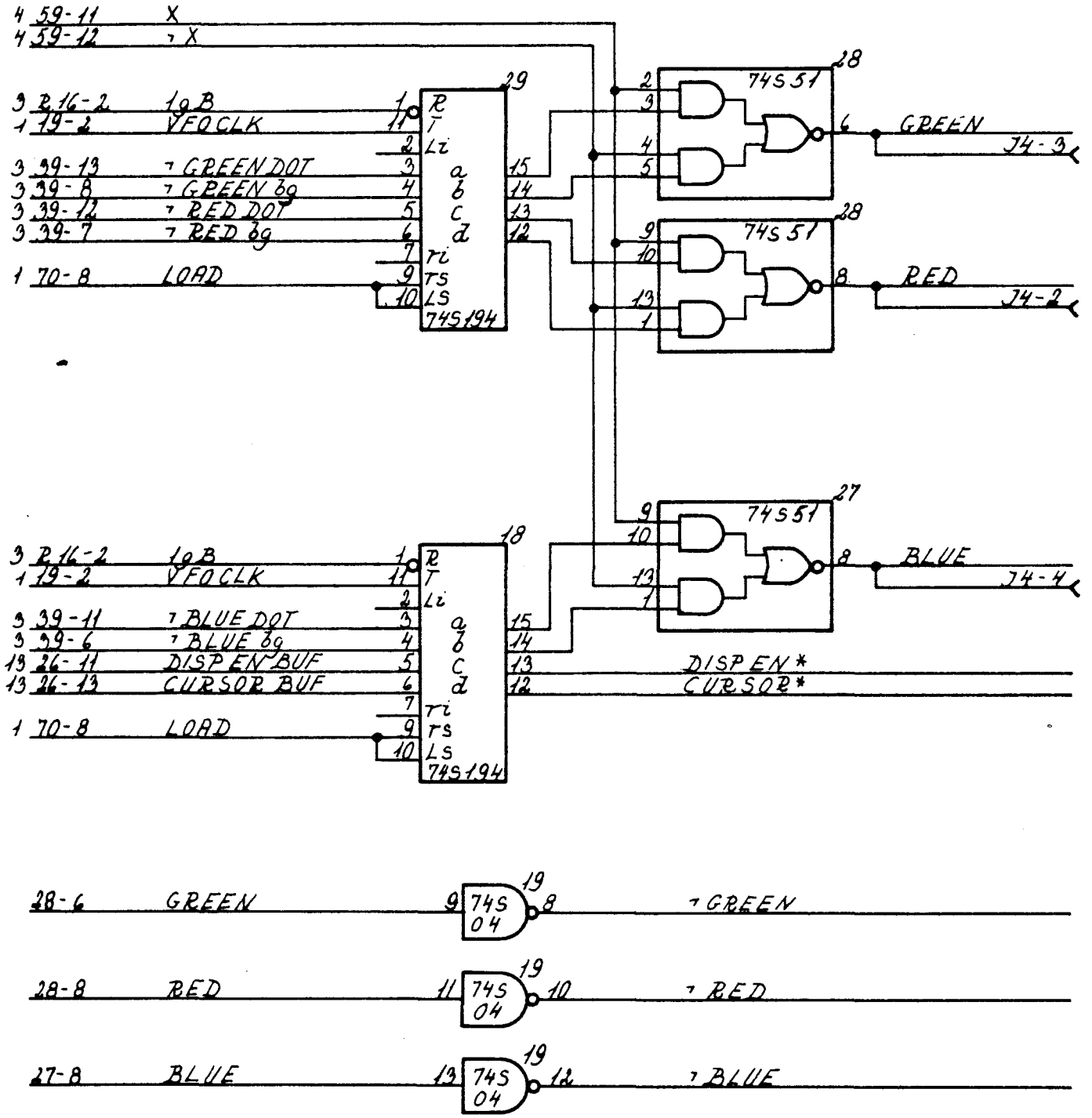
Signal	Destination	Description
-,LOAD	p4	parallel load of dot shifter every 16'th VFO clk, if not block char.
LOAD	p2	Loads dot control register every 16'th VFO CLK.
-,RESET WRITE	p11	Resets the writepulses to the refresh memory.
CCLK	p9, p11	Goes high in the beginning of each character time.
-,CCLK	p9, p13	
CLK1	p11	Alternates at half the frequency of VFO clk.
-,HORIZONTAL SYNC	Colour monitor	
HORIZONTAL SYNC	Black & white monitor	
VIDO	Black & white monitor	Analog video signal.
VERTICAL SYNC	Black & white monitor	
-,VERTICAL SYNC	Colour monitor	



VIDEO Contrast	VOLT min	VOLT max
Vertical sync	0,2	0,2
Dark	0,9	1,0
Green	1,1	2,3
Yellow = G+R	1,2	2,9
White = G+R+B	1,2	3,0

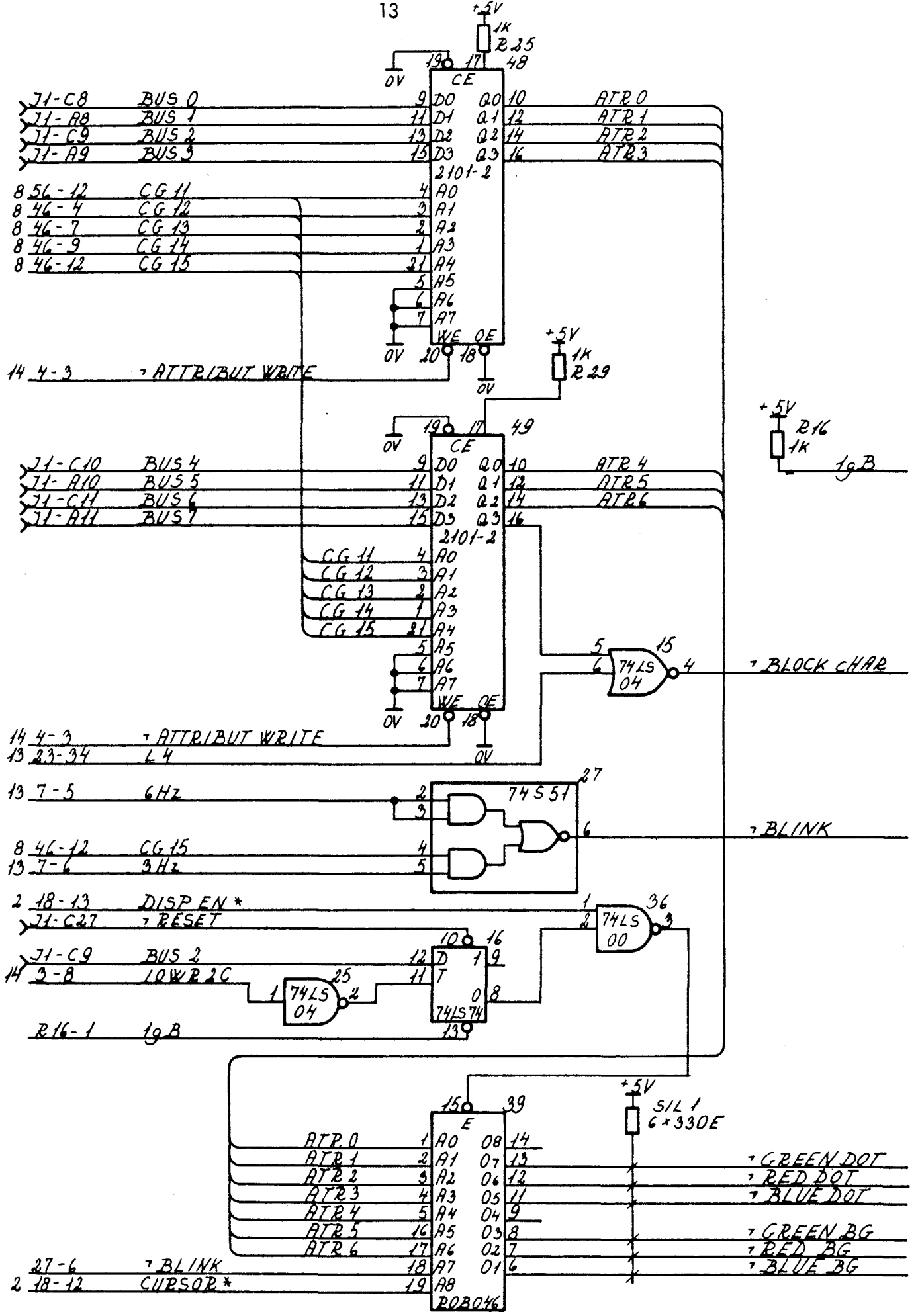
AGA 820420
PKA 81 12 21

Signal	Destination	Description
Green	Colour monitor	TTL-dot signals.
Red		
Blue		
-,Green	pl	
-,Red	pl	
-,Blue	pl	



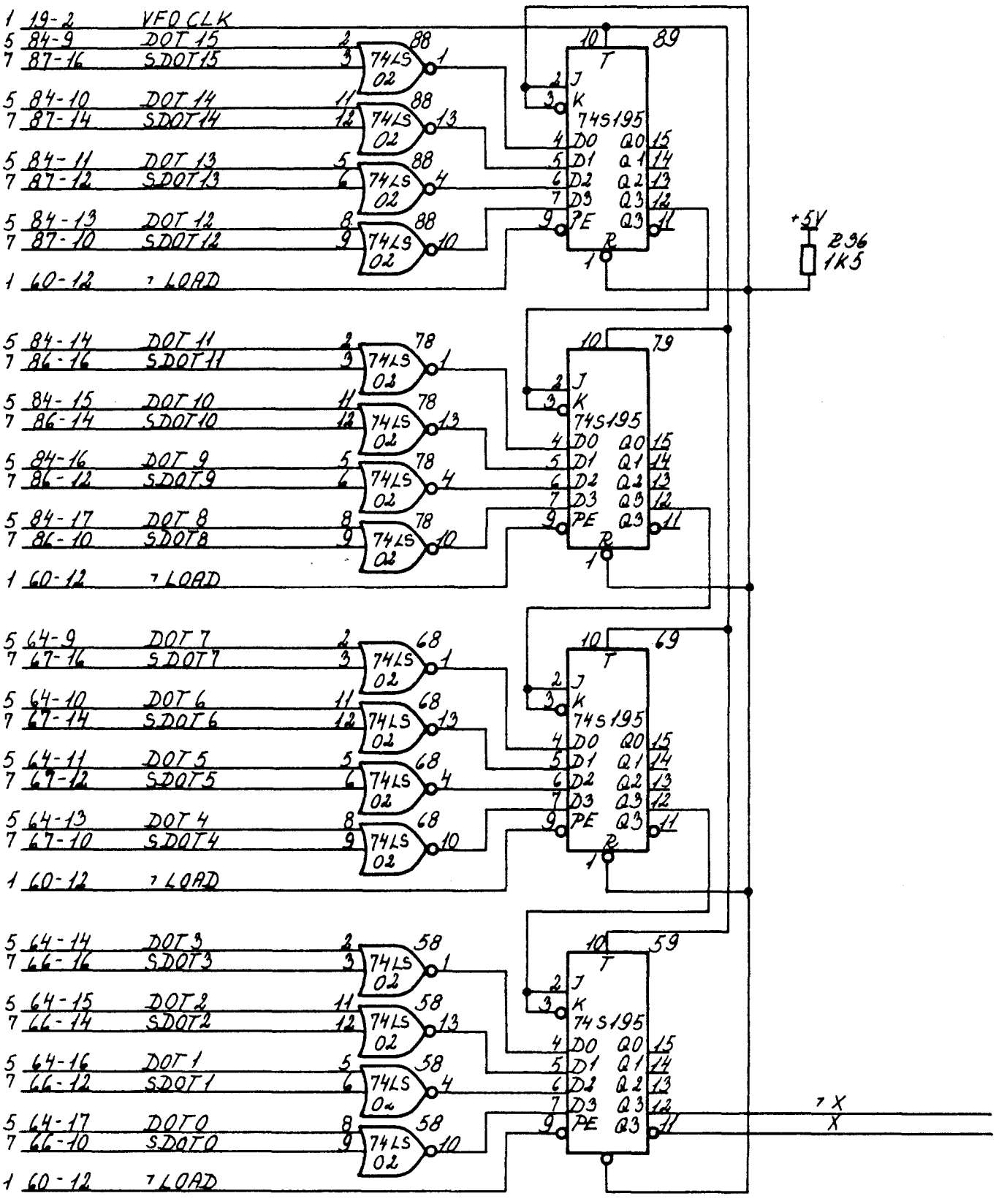
81 12 21 PKA 820420 RGA

Signal	Destination	Description
ATR 0-6	p3	Output from attribute RAM.
-,GREEN DOT -,RED DOT -,BLUE DOT	p2 p2 p2	Colour of the dots in the character.
-,GREEN BG -,RED BG -,BLUE BG	p2 p2 p2	Colour of the background in the character.
U36-3	p3	Blanks the display by forcing the outputs of U39 high.
-,BLOCK CHAR	p1	Disables dot generation. Only the background is visible in the character.
-,BLINK	p3	Blink frequency to the attribute ROM.


+5V
1K
R25
19
17
48
CE
J1-C8 BUS 0
J1-A8 BUS 1
J1-C9 BUS 2
J1-A9 BUS 3
9 D0 Q0 10 ATR 0
11 D1 Q1 12 ATR 1
13 D2 Q2 14 ATR 2
15 D3 Q3 16 ATR 3
2101-2
8 56-12 CG 11
8 46-4 CG 12
8 46-7 CG 13
8 46-9 CG 14
8 46-12 CG 15
4 A0
3 A1
2 A2
1 A3
21 A4
5 A5
6 A6
7 A7
OV
WE 20
OE 18
14 4-3 ATTRIBUT WRITE
+5V
1K
R29
OV
+5V
R16
1K
19B
19
17
49
CE
J1-C10 BUS 4
J1-A10 BUS 5
J1-C11 BUS 6
J1-A11 BUS 7
9 D0 Q0 10 ATR 4
11 D1 Q1 12 ATR 5
13 D2 Q2 14 ATR 6
15 D3 Q3 16
2101-2
CG 11 4 A0
CG 12 3 A1
CG 13 2 A2
CG 14 1 A3
CG 15 21 A4
5 A5
6 A6
7 A7
OV
WE 20
OE 18
14 4-3 ATTRIBUT WRITE
13 23-34 L4
OV
5
6
74LS 04
15
4
BLOCK CHAR
13 7-5 6Hz
27
74S51
2
3
6
BLINK
8 46-12 CG 15
13 7-6 3Hz
4
5
2 18-13 DISP EN*
J1-C27 RESET
1
2
74LS 00
36
3
10
16
J1-C9 BUS 2
14 3-8 IOWR2C
12 D
11 T
1
9
0
8
74LS74
13
25
1
74LS 04
2
R16-1 19B
15
39
E
+5V
SIL 1
6x330E
ATR 0 1 A0 08 14
ATR 1 2 A1 07 13
ATR 2 3 A2 06 12
ATR 3 4 A3 05 11
ATR 4 5 A4 04 9
ATR 5 16 A5 03 8
ATR 6 17 A6 02 7
18 A7 01 6
19 A8
ROB046
GREEN DOT
RED DOT
BLUE DOT
GREEN BG
RED BG
BLUE BG
27-6 BLINK
2 18-12 CURSOR*

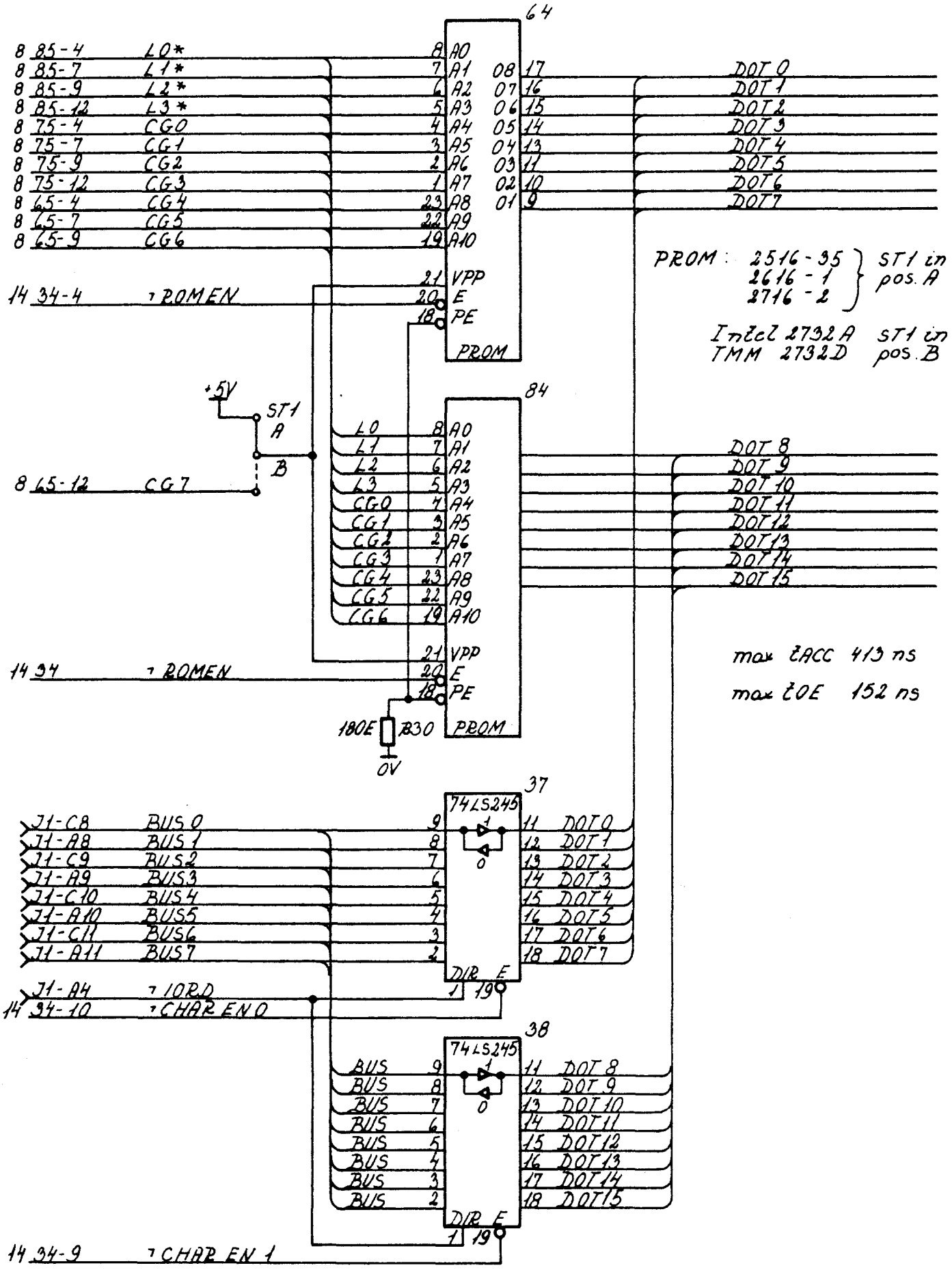
8112 21 PKA

Signal	Destination	Description
-,x	p2	Output of dot shifter. When x active a dot is displayed.

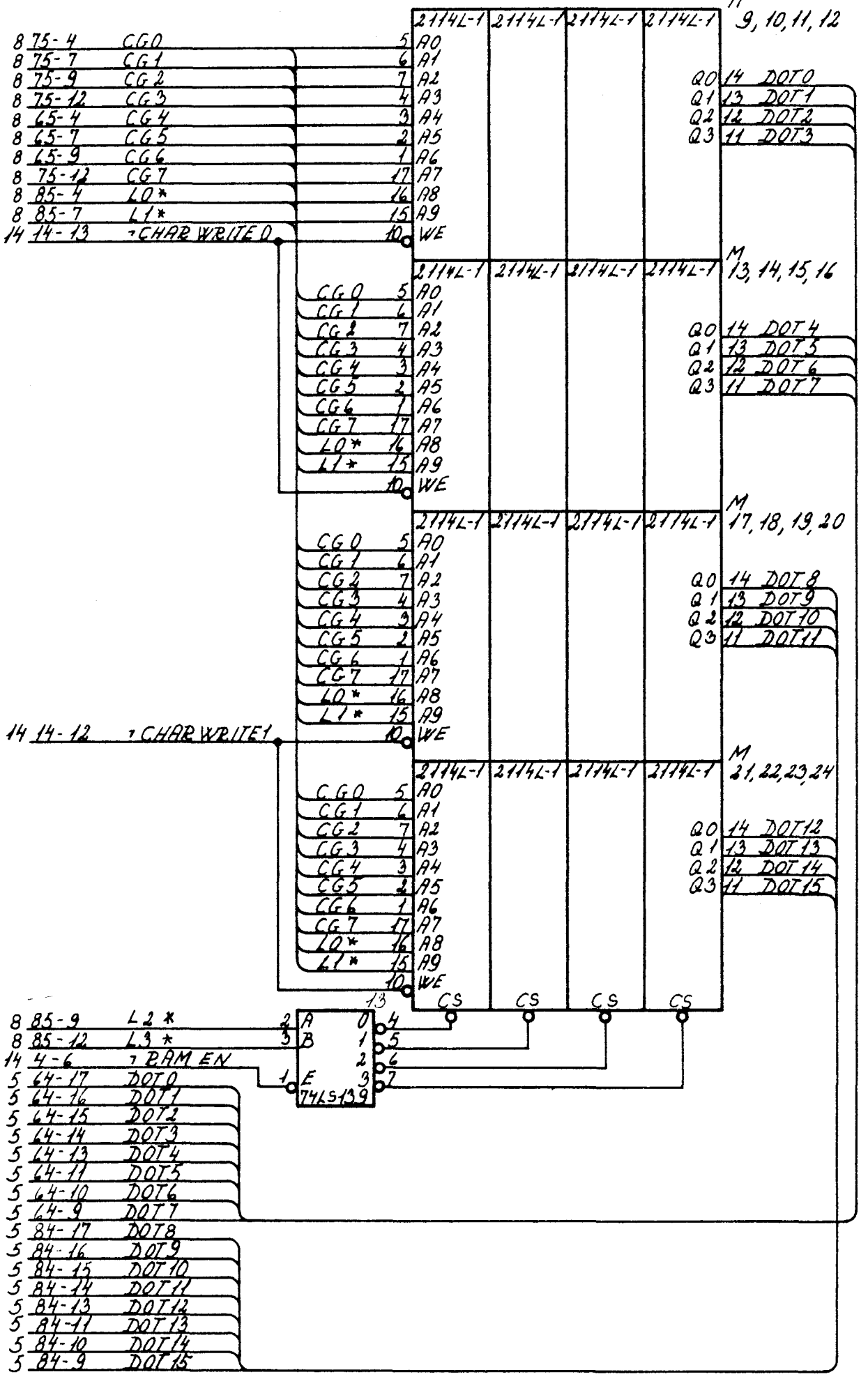


811221 PKA 820420 AGA

Signal	Destination	Description
DOT 0-15	p4, p5, p6	Tristate bus for input to dot shifter. Also accessible from MIC board thrugh U37 and U38. DOT 0-15 are sourced from the character ROM's U64 and U84 or the character RAM's p6.


64
8 85-4 LO*
8 85-7 L1*
8 85-9 L2*
8 85-12 L3*
8 75-4 CG0
8 75-7 CG1
8 75-9 CG2
8 75-12 CG3
8 65-4 CG4
8 65-7 CG5
8 65-9 CG6
14 34-4 ↑ROMEN
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
VPP E PE
PROM
08 07 06 05 04 03 02 01
DOT 0 DOT 1 DOT 2 DOT 3 DOT 4 DOT 5 DOT 6 DOT 7
PROM: 2516-35 2616-1 2716-2 } ST1 in pos. A
Intel 2732A TMM 2732D ST1 in pos. B
+5V
ST1
A
B
8 65-12 CG7
84
LO L1 L2 L3 CG0 CG1 CG2 CG3 CG4 CG5 CG6
DOT 8 DOT 9 DOT 10 DOT 11 DOT 12 DOT 13 DOT 14 DOT 15
max tACC 413 ns
max tOE 152 ns
14 34 ↑ROMEN
180E R30
0V
37
74LS245
J1-C8 BUS 0
J1-A8 BUS 1
J1-C9 BUS 2
J1-A9 BUS 3
J1-C10 BUS 4
J1-A10 BUS 5
J1-C11 BUS 6
J1-A11 BUS 7
DOT 0 DOT 1 DOT 2 DOT 3 DOT 4 DOT 5 DOT 6 DOT 7
D/R E
J1-A4 ↑IORD
14 34-10 ↑CHAR EN 0
38
74LS245
BUS 0 BUS 1 BUS 2 BUS 3 BUS 4 BUS 5 BUS 6 BUS 7
DOT 8 DOT 9 DOT 10 DOT 11 DOT 12 DOT 13 DOT 14 DOT 15
D/R E
14 34-9 ↑CHAR EN 1
AGA 820420
PKA 811221

Signal	Destination	Description
DOT 0-15	p4, p5	Tristate bus feeding the dot shifter.

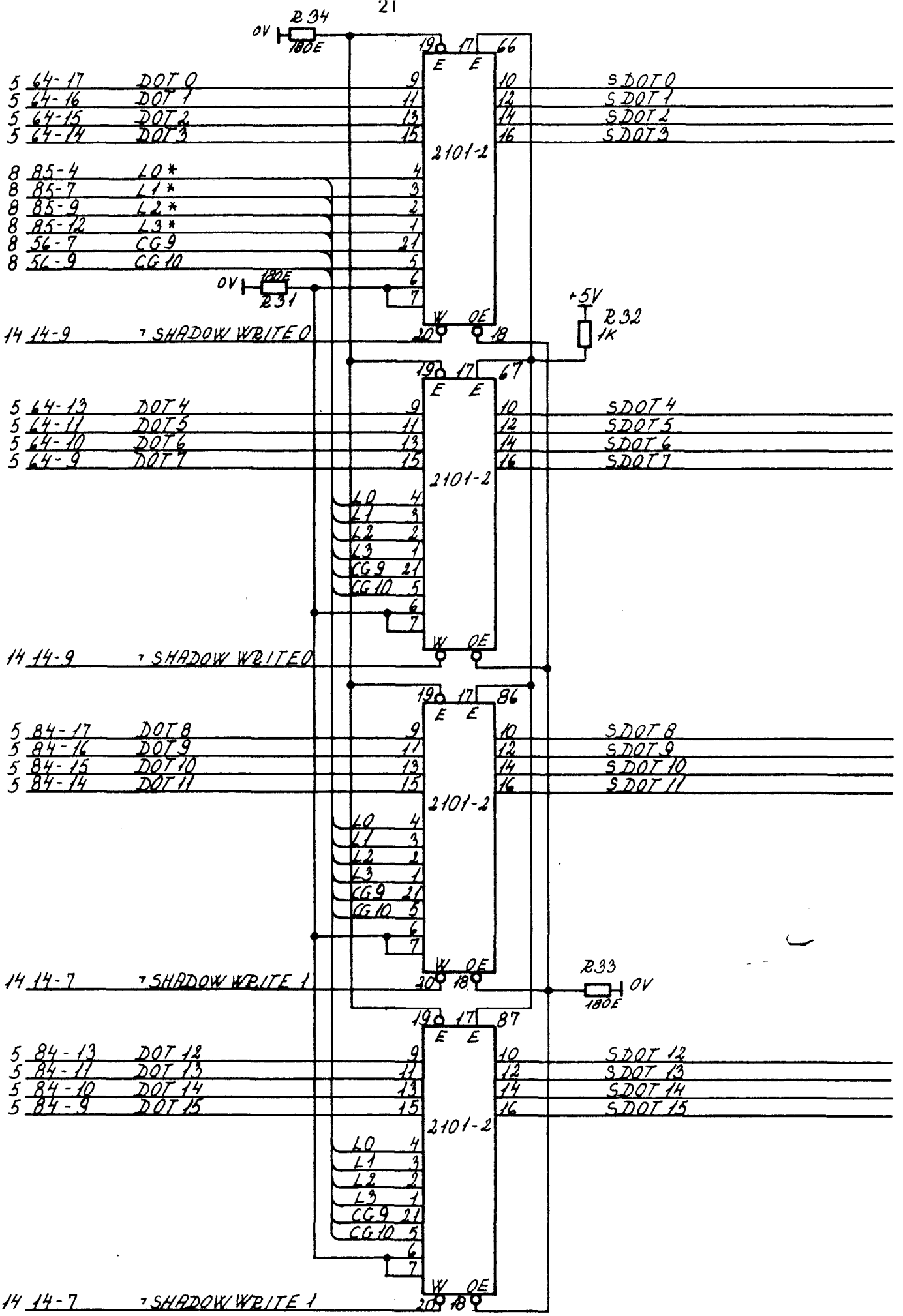


PKA 81221 AGA 820420

CRT 504 LOADABLE CHARACTER FONT 6

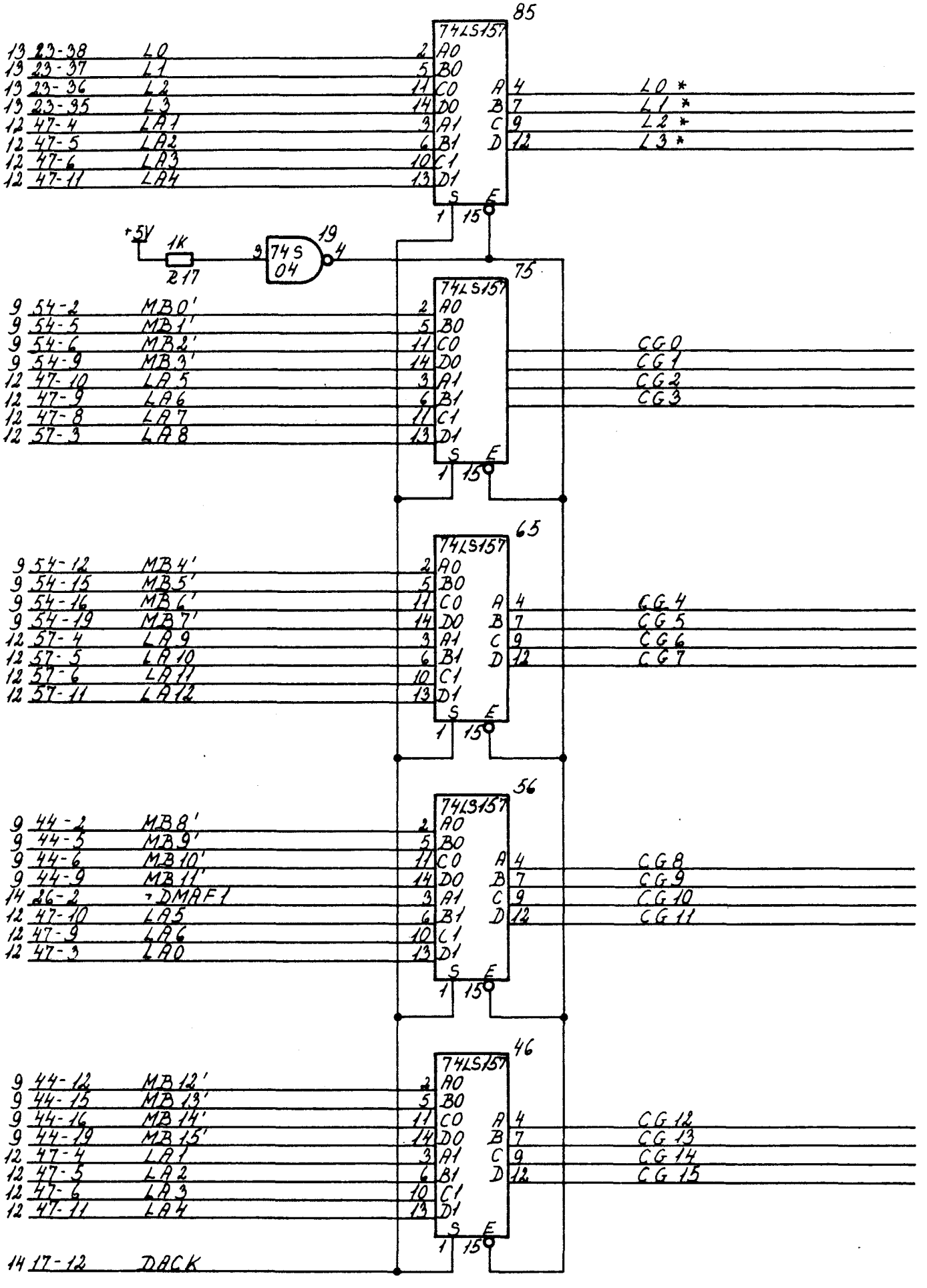
R 13345

Signal	Destination	Description
SDOT 0-15	p4	Are the dots of the shadow character.



81 12 21 PKA 820421 AGA

Signal	Destination	Description
L0-4*	p5, p6, p7	Used to address the video line number of the character generators.
CG0-7	p5, p6	Addresses a character in the character font (ROM or RAM).
CG 8	p14	Selects character ROM or RAM.
CG 9-10	p7	Selects shadow character.
CG 11-15	p3	Select attributes; CG15 also selects blink frequency.

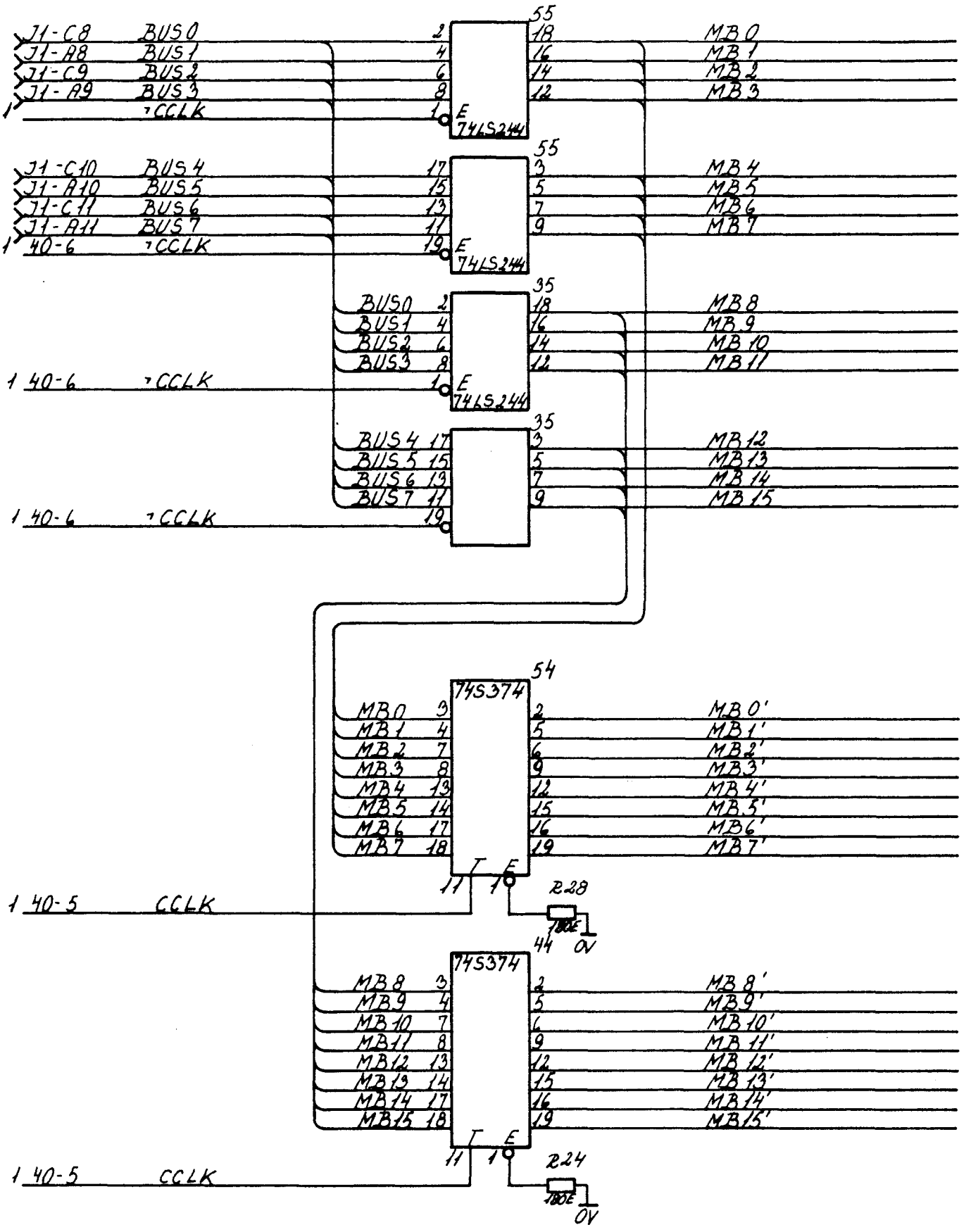


PKA 81 12 21 AGA 82 04 21

CRT 504
R 13347

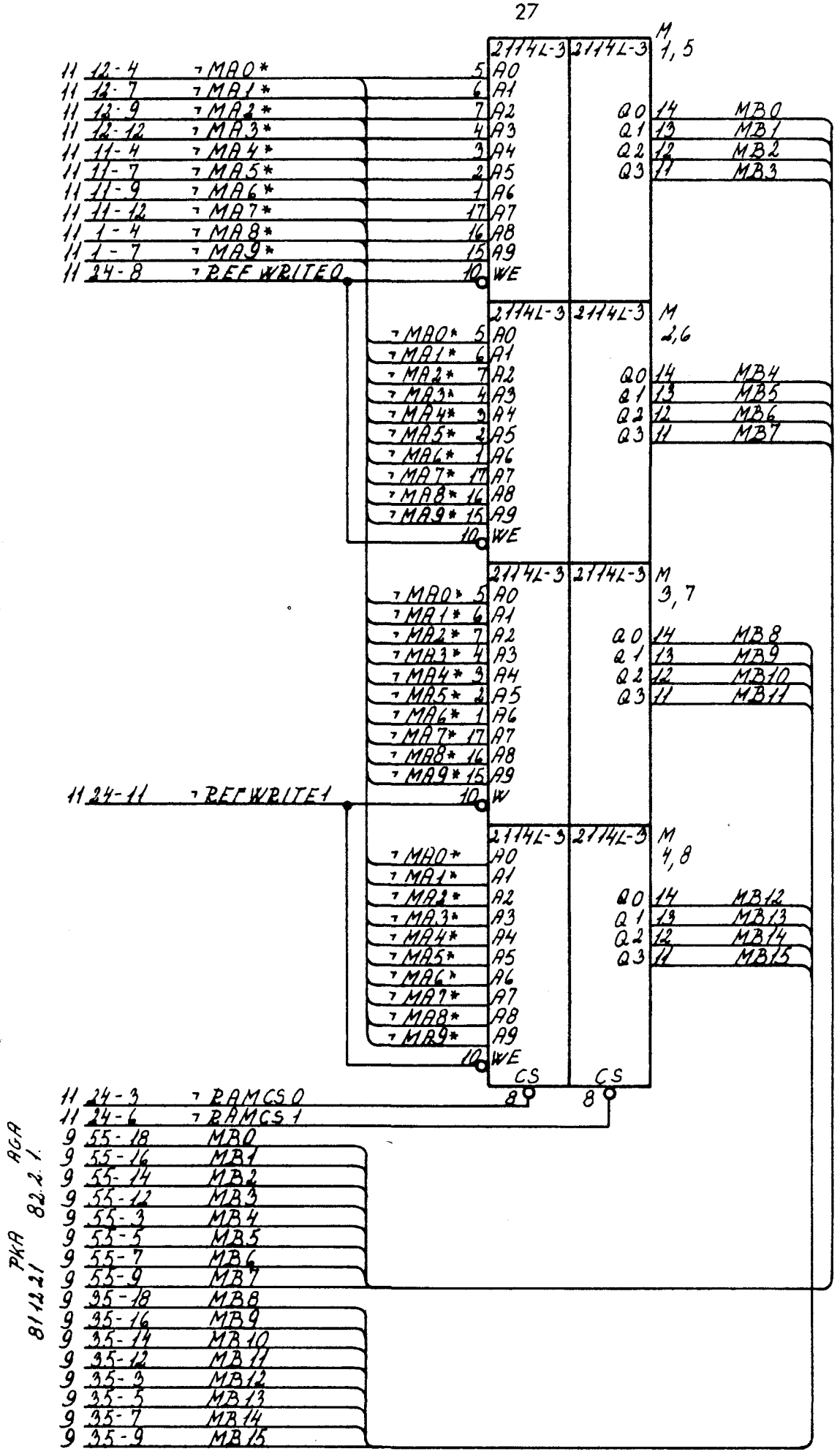
ADDRESS SWITCH for CHARACTER FONTS

Signal	Destination	Description
MB 0-15	p9, p10	Databus for refresh memory.
MB 0-15'	p8	Are gated to CG 0-15 during display time.

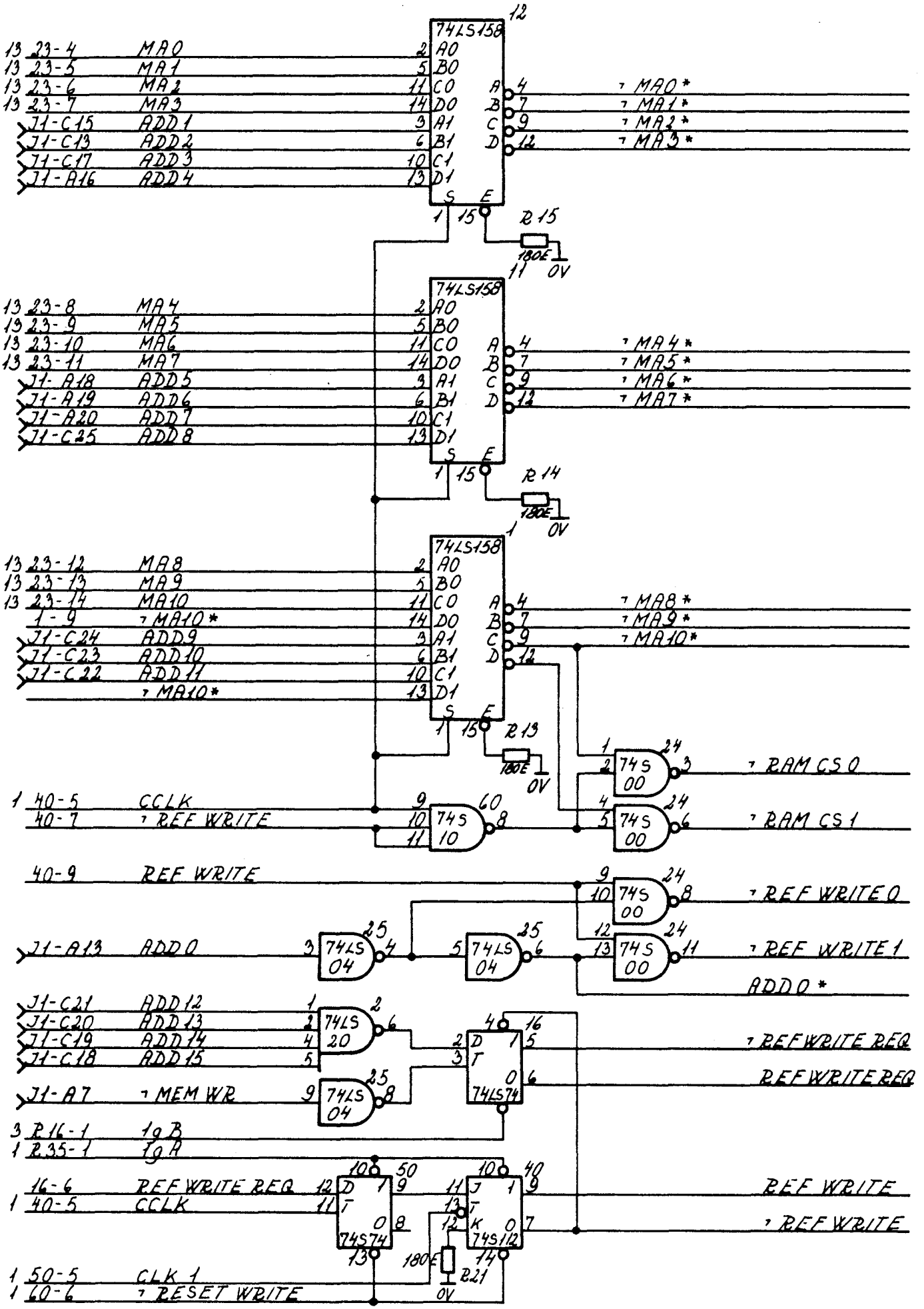


PKA 811221 82 21 AGA

Signal	Destination	Description
MB 0-15	p9	Databus for Refresh memory.


2114L-3
M 1,5
M 2,6
M 3,7
M 4,8
11 12-4 ¬MA0*
11 12-7 ¬MA1*
11 12-9 ¬MA2*
11 12-12 ¬MA3*
11 11-4 ¬MA4*
11 11-7 ¬MA5*
11 11-9 ¬MA6*
11 11-12 ¬MA7*
11 1-4 ¬MA8*
11 1-7 ¬MA9*
11 24-8 ¬REFWRITE0
11 24-11 ¬REFWRITE1
11 24-3 ¬RAMCS0
11 24-6 ¬RAMCS1
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 WE W CS
Q0 Q1 Q2 Q3
MB0 MB1 MB2 MB3 MB4 MB5 MB6 MB7 MB8 MB9 MB10 MB11 MB12 MB13 MB14 MB15
9 55-18 MB0
9 55-16 MB1
9 55-14 MB2
9 55-12 MB3
9 55-3 MB4
9 55-5 MB5
9 55-7 MB6
9 55-9 MB7
9 35-18 MB8
9 35-16 MB9
9 35-14 MB10
9 35-12 MB11
9 35-3 MB12
9 35-5 MB13
9 35-7 MB14
9 35-9 MB15
PKA 81.12.21 AGA 82.2.1.

Signal	Destination	Description
-,MA 0-10*	p10	Address lines to the refresh memory. during first character phase, -,MA 0-10* are derived from the MIC board-addressbus for writing in the refresh RAM, in the second character phase -,MA 0-10* are generated by the MC 6845 address sequencer for refresh of the character on the screen.
-,RAMCS 0-1	p10	Enable signals for refresh mem. controlled by -,MA 10*
-,REF WRITE 0-1	p10	Writepulse to frefresh memory, ADD 0 selects which byte.
ADD0*	p13	Buffered version of DD 0.
-,REFWRITE REQ	p13	The flip-flop is set when a memory write to the highest 4 k is issued by the CPU on the MIC board.
REFWRITE REQ	p11	
REF WRITE	p11	This pulse is generated if REF WRITE REQ is active, and falls entirely within the first character phase and has a guaranted minimum duration of 133 nanoseconds.
-,REF WRITE	p11	

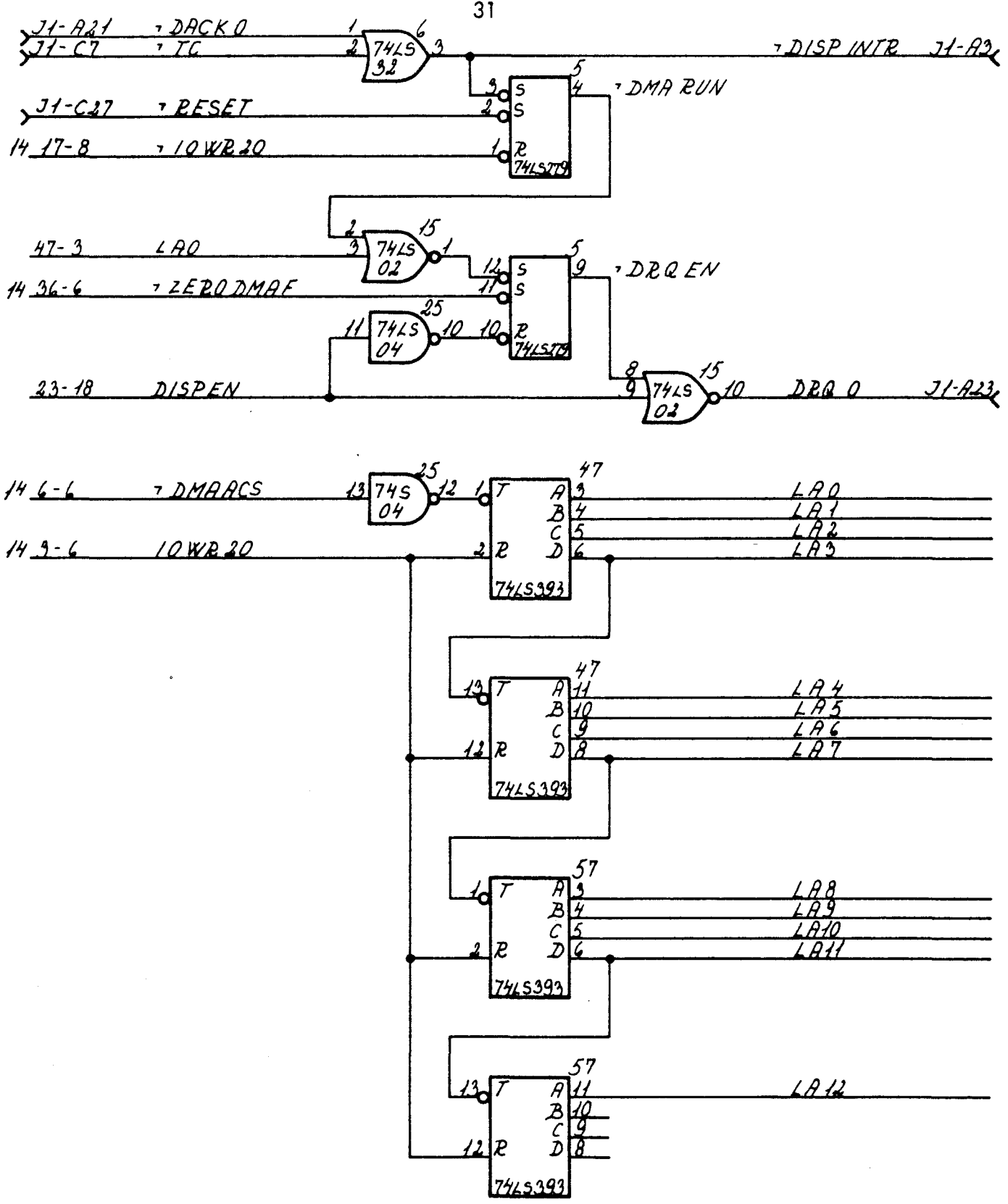


PKA 81121 AGA 82.2.2.

CRT 504
R 13350

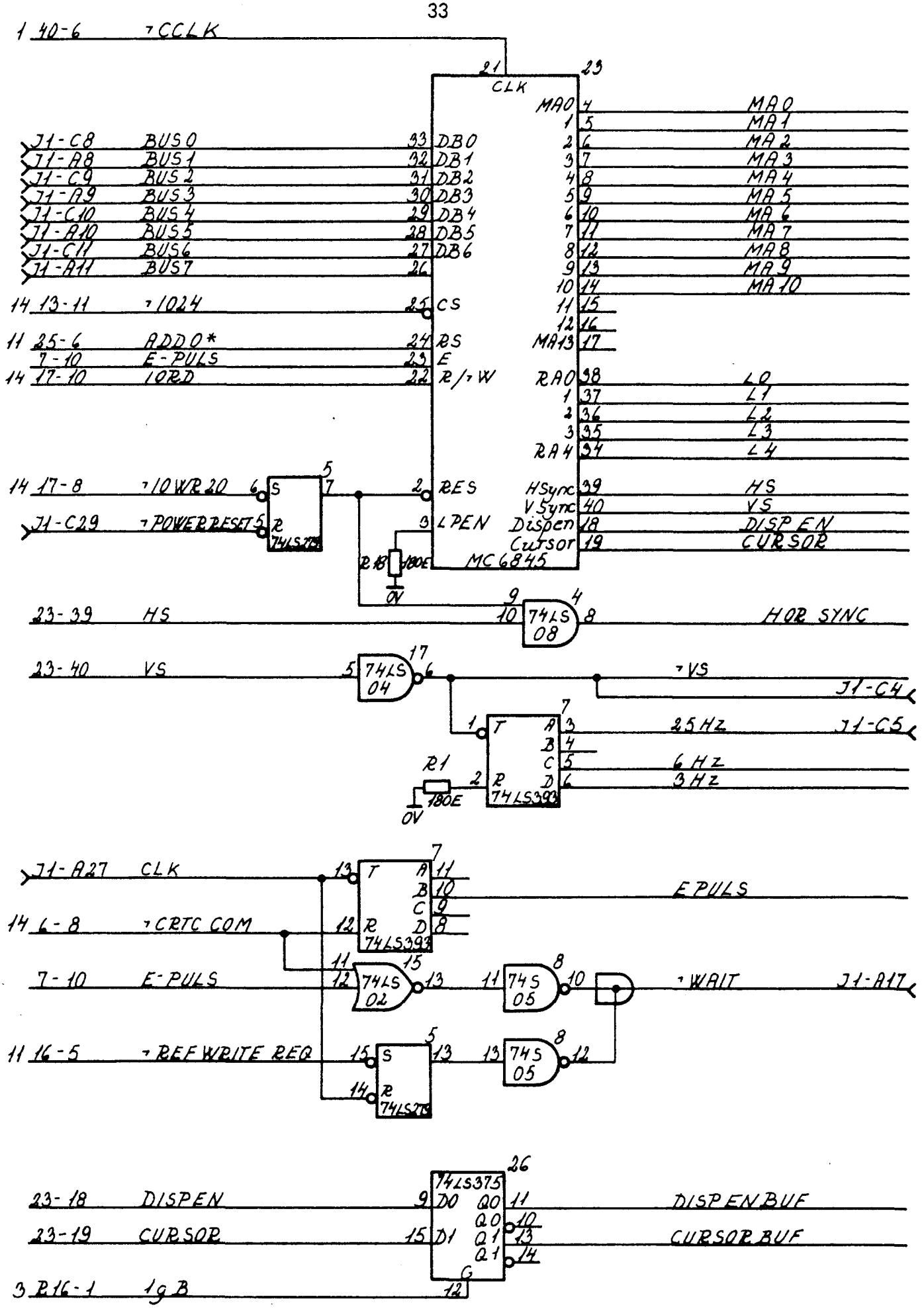
ADDRESS SWITCH for REFRESH MEMORY

Signal	Destination	Description
-,DISP INTR	MIC board	Active, when Dack 0 and -,Terminal count are active.
-,DMA RUN		Active from -,10WR20 to -,DISPINTR or -,RESET.
-,DRQ EN		Goes active when -,DMA RUN is low, if LA0 is low, -,ZERO DMAF is high and DISP EN is high. -,DRQ EN is reset by LA0 going high.
DRQ 0	MIC board	is set when DISPEN goes low, -,DRQ EN is active. Drops when one byte is transferred late enough to ensure that another DMA cycle is started.
LA 0-12	p8	Load Address counter for memories accessed by the MIC board via DMA.



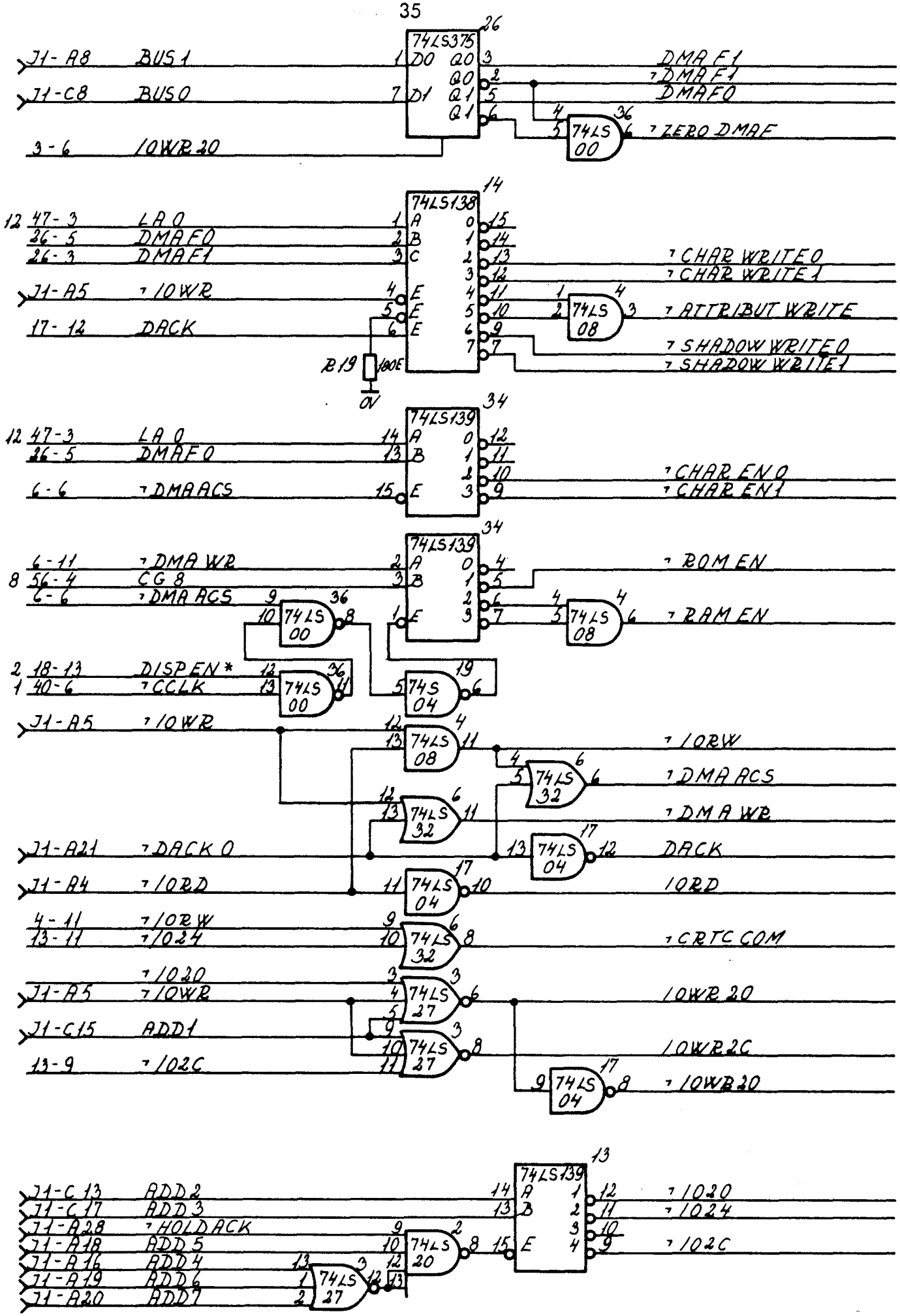
81 12 21 PKA 82.2.2. AGA

Signal	Destination	Description
MA 0-10	p11	Output of address sequence controller used for addressing the refresh memory for display.
L 0-3	p8	Video line number within the character line.
L4	p3	
HS	p13	Horizontal syncronization pulse.
VS	p13	Vertical syncronization pulse.
HOR SYNC	p1	Horsizontal sync gated with power up flip-flop.
-,VS	p1	
25 Hz	Mic board	Used for timer interrupt.
6 Hz	p3	Used for blink frequencies.
3 Hz	p3	
E Puls	p13	Enable pulse for programming of MC6845.
-,Wait	Micboard	Waitstates are inserted during memwrite in the refresh and programming of MC6845.
DISP EN BUF	p3	Display enable goes inactive during e-beam retrace.
CURSOR BUF	p3	



PKA 81121 AGA 82.2.2.

Signal	Destination	Description
DMA F1	p14	DMA function register.
-,DMA F1	p14	
DMA F0	p14	
-,ZERO DMAF	p12	Active when DMAF(0,1) = 0.
-,CHAR WRITE 0-1	p6	Write signal to character RAM.
-,ATTRIBUT WRITE	p3	Write signal to Attribut RAM.
-,SHADOWWRITE 0-1	p7	Write signal to shadow RAM.
-,CHAR EN 0-1	p5	Enables connection between DOT bus and MIC board data bus.
-,ROM EN	p5	Enables character ROM output.
-,RAM EN	p6	Enables Character RAM.
-,IORW	p14	-,(10 Read or 10 write).
-,DMA ACS	p12	IORW issued by DMA controller.
-,DMA WR	p14	Output by DMA.
DACK	p14	
IORD	p13	
-,CRTC COM	p13	10 port e4 addressed.
IOWR 20	p13, p14	10 port 20 addressed for write.
IOWR 2C	p3	
-,IOWR 20	p12	


J1-A8 BUS1
J1-C8 BUS0
3-6 /IOWR20
74LS375
DMAF1
¬DMAF1
DMAF0
74LS00
¬ZERO DMAF
12 47-3 LA0
26-5 DMAF0
26-3 DMAF1
J1-A5 ¬/IOWR
17-12 DACK
R19 100E
74LS138
¬CHAR WRITE0
¬CHAR WRITE1
74LS08
¬ATTRIBUT WRITE
¬SHADOW WRITE0
¬SHADOW WRITE1
12 47-3 LA0
26-5 DMAF0
6-6 ¬DMAACS
74LS139
¬CHAR EN0
¬CHAR EN1
6-11 ¬DMA WR
8 56-4 CG8
6-6 ¬DMA ACS
¬ROM EN
¬RAM EN
2 18-13 DISPEN*
1 40-6 ¬CCLK
74LS04
J1-A5 ¬/IOWR
¬/IORW
¬DMA ACS
¬DMA WR
J1-A21 ¬DACK0
DACK
J1-A4 ¬/IORD
/IORD
4-11 ¬/IORW
13-11 ¬/1024
74LS32
¬CRTC COM
¬/1020
J1-A5 ¬/IOWR
74LS27
/IOWR20
J1-C15 ADD1
13-9 ¬/102C
/IOWR2C
¬/IOWR20
J1-C13 ADD2
J1-C17 ADD3
J1-A28 ¬HOLDACK
J1-A18 ADD5
J1-A16 ADD4
J1-A19 ADD6
J1-A20 ADD7
74LS20
¬/1020
¬/1024
¬/102C
PKA AGA 82.2.3 81/1231

5. ATTRIBUTE ROM

5.

Blink on
Blink phase
CURSOR

Black & White
Color

F: Foreground
B: Background

output:
0 : White
1 : Yellow
2 : Turquoise
3 : Green
4 : Pink
5 : Red
6 : Blue
7 : Black

ADR	F B	ADR	F B	ADR	F B	ADR	F B	ADR	F B	ADR	F B	ADR	F B	ADR	F B
00	37	08	37	80	37	88	37	100	73	108	73	180	73	188	73
01	07	09	07	81	07	89	37	101	71	109	71	181	71	189	73
02	77	0A	37	82	77	8A	77	102	33	10A	73	182	33	18A	33
03	77	0B	07	83	77	8B	77	103	11	10B	71	183	11	18B	33
04	73	0C	73	84	73	8C	37	104	37	10C	37	184	37	18C	73
05	71	0D	71	85	71	8D	37	105	07	10D	07	185	07	18D	73
06	33	0E	73	86	33	8E	77	106	71	10E	31	186	71	18E	33
07	11	0F	71	87	11	8F	77	107	71	10F	01	187	71	18F	33
10	67	18	67	90	67	98	77	110	76	118	76	190	76	198	76
11	76	19	76	91	76	99	66	111	67	119	64	191	67	199	67
12	65	1A	65	92	65	9A	55	112	56	11A	56	192	56	19A	56
13	64	1B	64	93	64	9B	44	113	46	11B	46	193	46	19B	46
14	63	1C	63	94	63	9C	33	114	36	11C	36	194	36	19C	36
15	62	1D	62	95	62	9D	22	115	26	11D	26	195	26	19D	26
16	61	1E	61	96	61	9E	11	116	16	11E	16	196	16	19E	16
17	60	1F	60	97	60	9F	00	117	06	11F	06	197	06	19F	06
20	57	28	57	A0	57	A8	77	120	75	128	75	1A0	75	1A8	75
21	56	29	56	A1	56	A9	66	121	65	129	65	1A1	65	1A9	65
22	55	2A	55	A2	55	AA	55	122	57	12A	57	1A2	57	1AA	55
23	54	2B	54	A3	54	AB	44	123	45	12B	45	1A3	45	1AB	45
24	53	2C	53	A4	53	AC	33	124	35	12C	35	1A4	35	1AC	35
25	52	2D	52	A5	52	AD	22	125	25	12D	25	1A5	25	1AD	25
26	51	2E	51	A6	51	AE	11	126	15	12E	15	1A6	15	1AE	15
27	50	2F	50	A7	50	AF	00	127	05	12F	05	1A7	05	1AF	05
30	47	38	47	B0	77	B8	77	130	74	138	74	1B0	74	1B8	74
31	46	39	46	B1	66	B9	66	131	64	139	64	1B1	64	1B9	64
32	45	3A	45	B2	55	BA	55	132	54	13A	54	1B2	54	1BA	54
33	44	3B	44	B3	44	BB	44	133	47	13B	47	1B3	47	1BB	47
34	43	3C	43	B4	43	BC	33	134	34	13C	34	1B4	34	1BC	34
35	42	3D	42	B5	42	BD	22	135	24	13D	24	1B5	24	1BD	24
36	41	3E	41	B6	41	BE	11	136	14	13E	14	1B6	14	1BE	14
37	40	3F	40	B7	40	BF	00	137	04	13F	04	1B7	04	1BF	04
40	37	48	37	C0	37	C8	77	140	73	148	72	1C0	72	1C8	73
41	36	49	36	C1	36	C9	66	141	63	149	63	1C1	63	1C9	63
42	35	4A	35	C2	35	CA	55	142	53	14A	52	1C2	53	1CA	53
43	34	4B	34	C3	34	CB	44	143	43	14B	43	1C3	43	1CB	43
44	73	4C	73	C4	73	CC	33	144	37	14C	37	1C4	37	1CC	37
45	32	4D	32	C5	32	CD	22	145	23	14D	23	1C5	23	1CD	23
46	31	4E	31	C6	31	CE	11	146	13	14E	13	1C6	13	1CE	13
47	30	4F	30	C7	30	CF	00	147	03	14F	03	1C7	03	1CF	03
50	27	58	27	D0	27	D8	77	150	72	158	72	1D0	72	1D8	72
51	26	59	26	D1	26	D9	66	151	62	159	62	1D1	62	1D9	62
52	25	5A	25	D2	25	DA	55	152	52	15A	52	1D2	52	1DA	52
53	24	5B	24	D3	24	DB	44	153	42	15B	42	1D3	42	1DB	42
54	23	5C	23	D4	23	DC	33	154	32	15C	32	1D4	32	1DC	32
55	72	5D	72	D5	72	DD	22	155	27	15D	27	1D5	27	1DD	27
56	21	5E	21	D6	21	DE	11	156	12	15E	12	1D6	12	1DE	12
57	20	5F	20	D7	20	DF	00	157	02	15F	02	1D7	02	1DF	02
60	17	68	17	E0	17	E8	77	160	71	168	71	1E0	71	1E8	71
61	16	69	16	E1	16	E9	66	161	61	169	61	1E1	61	1E9	61
62	15	6A	15	E2	15	EA	55	162	51	16A	51	1E2	51	1EA	51
63	14	6B	14	E3	14	EB	44	163	41	16B	41	1E3	41	1EB	41
64	13	6C	13	E4	13	EC	33	164	31	16C	31	1E4	31	1EC	31
65	12	6D	12	E5	12	ED	22	165	21	16D	21	1E5	21	1ED	21
66	11	6E	11	E6	11	EE	11	166	17	16E	17	1E6	17	1EE	17
67	10	6F	10	E7	10	EF	00	167	01	16F	01	1E7	01	1EF	01
70	07	78	07	F0	07	F8	77	170	70	178	70	1F0	70	1F8	70
71	06	79	06	F1	06	F9	66	171	60	179	60	1F1	60	1F9	60
72	05	7A	05	F2	05	FA	55	172	50	17A	50	1F2	50	1FA	50
73	04	7B	04	F3	04	FB	44	173	40	17B	40	1F3	40	1FB	40
74	03	7C	03	F4	03	FC	33	174	30	17C	30	1F4	30	1FC	30
75	02	7D	02	F5	02	FD	22	175	20	17D	20	1F5	20	1FD	20
76	01	7E	01	F6	01	FE	11	176	10	17E	10	1F6	10	1FE	10
77	70	7F	70	F7	70	FF	00	177	07	17F	07	1F7	07	1FF	07

Contents of ROB046 type 74S472

6. CHARACTER ROM's 6.

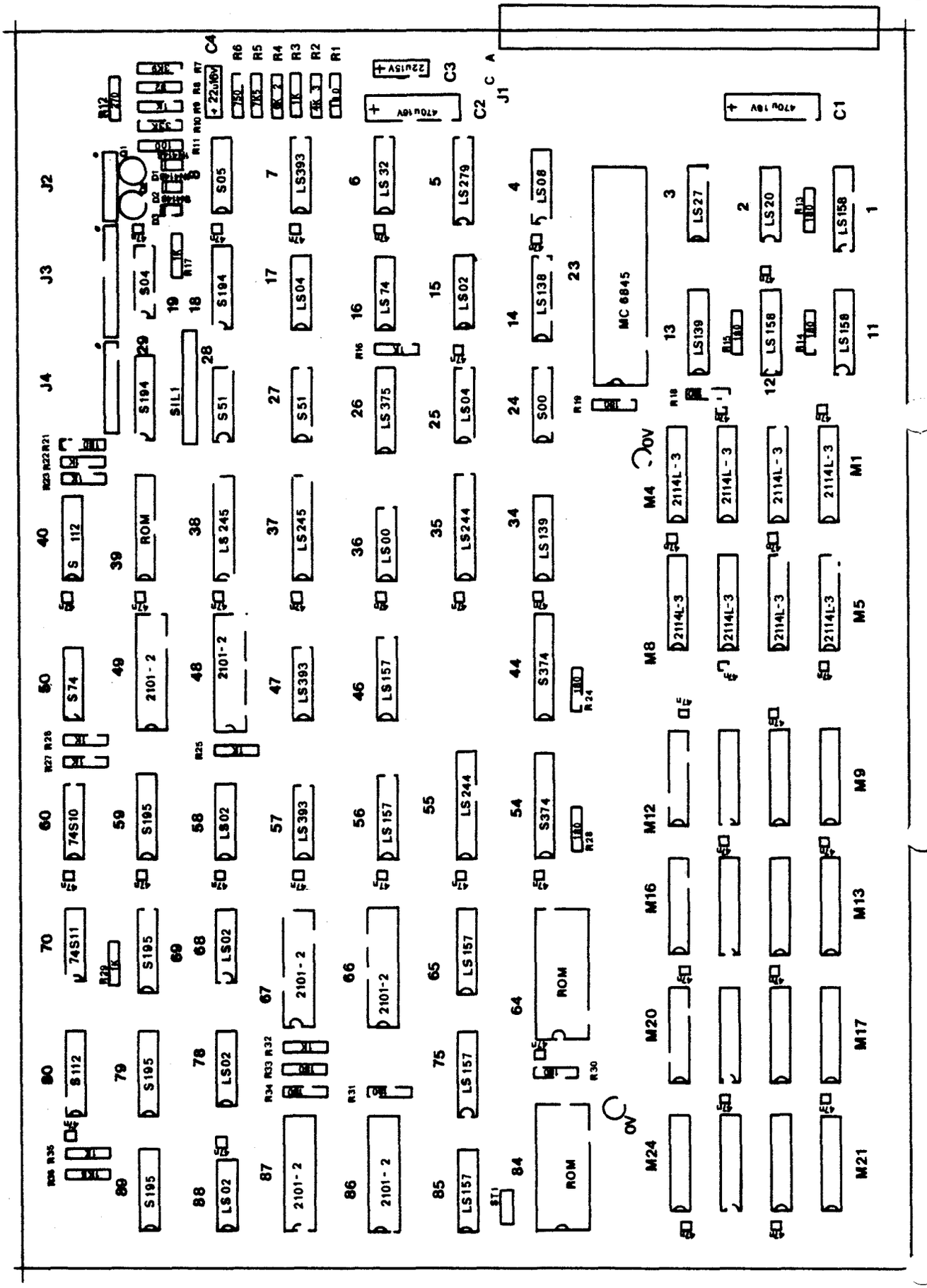
As character ROM's are used

U64 : ROA416

U84 : ROA417

7. ASSEMBLY DRAWING

7.



8. PLUGS

J1. pin	A	C
1		
2		
3	-,DISP INTR	-,VFO CLK
4	-,IORD	-,VS
5	-,IOWR	25Hz
6		
7	-,MEMWR	-,TC
8	BUS1	BUS0
9	BUS3	BUS2
10	BUS5	BUS4
11	BUS7	BUS6
12		
13	ADD0	ADD2
14	Chain	Chain
15		ADD1
16	ADD4	
17	-,WAIT	ADD3
18	ADD5	ADD15
19	ADD6	ADD14
20	ADD7	ADD13
21	-,DACK 0	ADD12
22		ADD11
23	DRQ 0	ADD10
24		ADD9
25		ADD8
26		
27	CLK	-,RESET
28	-,HOLD ACK	
29		-,POWER RESET
30		
31		
32	+12V	+12V

J2. pin

1	Contrast pot. max
2	Contrast pot. top
3	Contrast pot. min
4	Intensity pot. max
5	Intensity pot. tap
6	Intensity pot. min

J3. BW Monitor connected to CBL

pin

1	GND
2	Intensity max
3	Intensity min
4	Intensity top
5	Not used
6	Horizontal sync
7	Not used
8	Video
9	Vertical sync
10	GND

J4. Colour monitor

pin

1	
2	RED
3	GREEN
4	BLUE
5	GND
6	GND
7	-,Horizontal sync
8	-,Vertical sync

RETURN LETTER

Title: CRT504/506 - CRT Controller Technical Manual

RCSL No.: 44-RT2046

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