TEST AF 6710 IPC-KORT

Monter kort i test-IPC - Tænd for power.
Monter strap i S1 øverst (batteri til ur)
Juster clock-oscillator :
Forbind frekvenstæller til TP (yderst højre side) og juster til 32,768 Khz.
Monter strap i S1 næstøverst (debug on ved power on)
Forbind terminal (9600 baud) til DB9 stik (via adaptor)
Tænd IPC - Menu kommer frem på skærmen.
Tast : "OR [enter] Q"
Kald debugger med "D".

Test af DB9-stik(port1):
Udskriver kontinuerligt "U"

```
8000 : MVI A,55
8002 : 39ED
8004 : 0007
8006 : JMP 8000
```

Test af DB25-stik(port0):
Udskriver kontinuerligt "U"

```
8000 : MVI A,55
8002 : 39ED
8004 : 0006
8006 : JMP 8000
```

Test af ur.

Sekundskift på skærmen

```
8000 : MVI A,00
8002 : IN 86
8004 : 39ED
8006 : 0007
8008 : JMP 8000
```

Test temp.føler:

Check at værdi ændrer sig ved opvarmning:
under 70 gr. =DE (~)
over 70 gr. =DA (z) (bit 2 ændres)

```
8000 : MVI A,00
8002 : IN 66
8004 : 39ED
8006 : 0007
8008 : JMP 8000
```

Flyt næstøverste strap en position ned.
Tilslut terminal til port0 (DB25)
Power on. - Teksten "setup>>" vil vise sig på skærmen.
Tast "h" og check diverse faciliteter.

Test af 6710-kort med testprom IPC/2 TEST

Indeholder følgende testrutiner:

Terminal på port 1 (DB9)

adr.800 : Tester 6023-kort (adr.C3=sw.1-2-7 on)
Stop med CTRL/

adr.1000 : I : initialiser ur med fast værdi
R : læs ur
W : skriver en fast værdi (dato + tid)
R : læs ur igen

Tilslut terminal på port 0 (DB25)

adr.4000 : RS485 test på port 0 (ekko'er tegn på begge skærme)
afslut med CTRL/D.

adr.5000 : ekko'er tegn på modpart (hvis port 0 er forsynet med lus)

Test af IPC-system

Et IPC-rack med CPU (6710), digital input og digital output kort kan testes v.h.a.procescontrolsystemet på følgende måde.

IPC'en forsynes med power og tilsluttes madmax via kablet hos PKN. Endvidere skal DI-kort og DO-kort monteres med testtopconnectorer som forsynes med 12V DC via den røde og sorte ledning.
På en terminal logges ind på madmax med opl (opl1992) og understation ipct downloades med programmet `6741ny`.Derefter skal man i menuen `billeder` vælge programmet `6741test`.
Man skal derefter med funktionen `styring` starte enten kontinuerlig eller periodisk test.Derved testes relæer og optokoplere og kortenes øvrige funktion rimeligt.

Test af 6710-kort (ekstern bus)

Følgende rutine udfører relætest på 6026-kort (adr.50 = 2+4 on) :

```
8000 : MVI A,00
       LXI B,8650
       79ED
       PUSH PSW
       CALL 9000
       POP PSW
       ADI 01
       JMP 8003
```

```
9000 : LXI H,0000
       DCX H
       MOV A,H
       CPI 00
       RZ
       JMP 9003
```

Følgende rutine udfører relætest på 6019-kort (6732) adr.60 :

Som ovenstående bortset fra ... LXI B,8560

→ KK og LS.

Dansk Data Elektronik A/S

IPC 6710	Initials	Page
	Date 4/3-91	Project

Vedr. model for IPC 6710:

Hex stag ved DB25 og DB9 skal være længere; de monterede passer ikke til udvendig skrivemontering.

Tekst på forpladen aftales med IL.

Når kortet lægges på bagen, må batteri strappen (S1 pin 7-8) ikke være monteret. Monteres først øverste ved tilbagestilling af kortet; strappen er fjernet position på modellen.

På S1 EPROM (IC18) er normalt en 1MBit EPROM Programmering aftales med SLA.

M.v.h.

A.P.

Batterne (IC 16 og 17) skal egentlig være 22V10Z, CMOS men disse får ikke endnu, så foreløbig monteres GAL22V10.

MANUAL

for

IPC/1 6710 CPU II Processor modul

Dansk Data Elektronik A/S

Okt. 1990 / Feb. 1991.

Forfatter: Allan Petersen
Okt. 1990 / Feb. 1991.

Indholdsfortegnelse:

Introduktion.

IPC/1 6710 modulet er et andengenerations CPU kort til IPC systemet. Kortet er opbygget omkring en Hitachi 647180 microprocessor (software kompatibel med Z80 og 8085) og har desuden fået tilføjet faciliteter som urkreds og RS485 interface i forhold til det tidligere CPU kort. RAM og EPROM for processoren er nu ligeledes anbragt på selve CPU kortet istedet for som tidligere på et ekstra printkort. Memory arealet er væsentligt udvidet. Alt dette medvirker til en væsentlig højere performance end for det tidligere IPC 6000 kort.

Kortet indeholder skematisk følgende kredsløb:

- Hitachi 647180 processorkreds med CPU, MMU, DMA, timere, porte og bootprom med startprogram, debugger og testprogram.
- RAM (med batteri back-up), EPROM (med bankswitch) og EEPROM.
- Urkreds (National 8570) med batteri back-up).
- Businterface til IPC bus.
- Receivere og drivere for en RS232 port samt en valgbar RS232 eller RS485 port.
- Watchdog kredsløb.
- Kredsløb til reset og modeswitch for 647180 processor.
- LED's for portaktivitet og for processorstatus.
- Optional +- 12V DC/DC converter fra +5V (til RS232 porte).
- Detector for korttemperatur på over 70 C.

Kortet kan umiddelbart anvendes i forbindelse med alle tidligere IPC kort, undtagen 6041 kortet (300 bps Bell 103 modemkort), som i så fald skal have tilføjet en krystal oscillator på printet.

PS: Såfremt der anvendes et IPC 6092 kort (DC/DC converter i forbindelse med IPC 6016i kortet), må dette ikke strappes til at give -15 V på bussen, ligesom DMA, CSI port og TOUT2/TOUT3 ikke kan benyttes med IPC 6092 kortet monteret.

Funktionel beskrivelse:

Processor:

Hitachi 647180 processoren er en singlechip processor med indbygget RAM og EPROM, men kan også anvendes i en mode, hvor udvendig RAM og EPROM accesses. IPC 6710 kortet indeholder kredsløb til valg af disse modes, således at processoren ved power-on starter i den interne EPROM, hvor der findes programmer til initialisering samt check af den strap, der angiver, hvorvidt der herefter ønskes start af debugger/testprogrammer (i intern EPROM) eller umiddelbart skift af mode og start af userprogram i extern EPROM.

Memory og I/O:

På kortet findes 256 k bytes RAM, 128 - 512 k bytes EPROM og 8 - 32 k bytes EEPROM. Endvidere kan der adresseres memorymapped ud på IPC bussen, og bankswitch setting er også memory mapped. Processorens interne RAM (512 bytes) accesses normalt i området FFE00H til FFFFFH.

Der er på kortet anbragt 256 k bytes RAM med batteri back-up. Når 4Mbit SRAM kredse bliver tilgængelige, kan kortet forsynes med 512 k bytes RAM med batteri back-up.

Processorens I/O adresse område er på 64 k adresser, så den tidligere procedure med opsætning af typeadresse i register før acces kan nu udføres ved direkte adressering, jfr. I/O adresse oversigten.

Mode setting:

Modesetting foretages via to bits på port A (PA7 og PA6) samt ved mode-register strobe, og denne setting effektueres ved af give processoren en soft reset puls (skrivning til bestemt IO adresse).

Der kan specificeres tre forskellige modes:

- Intern mode (PA7/6=00), hvor den interne EPROM accesses

- System mode (PA7/6=10), hvor der startes programafvikling i den nederste del af EEPROM'en

- User mode (PA7/6=11), hvor der startes i den bankswitchede externe EPROM

Bemærk, at der ikke skal gives soft reset for at skifte mellem system-mode og user-mode, mens der skal gives soft reset ved skift til eller fra intern mode.

System-mode kan derfor anvendes til opsætning af specielle initialiserings parametre (valg af spec. user bankswitchsetting eller portopsætning el. lign) gemt i EEPROM inden start af user-mode. Sådanne settings vil ellers ødelægges af reset.

MMU:

Processoren kan via den indbyggede MMU adressere 1 Mbytes (16 pages a 64 k bytes; MMU'en kan foretage mapning af områder på 4 k bytes).

Der er på kortet plads til mellem 128 k og 512 k bytes EPROM, og dermed fra 4 til 16 banks a 32 k bytes, idet der regnes med et 32 k bytes vindue til EPROM lagerområdet.

Processorens interne RAM (512 bytes) og Bankswitch registeret acceses via MMU'en, ligesom man via MMU'en kan indvælge et memory vindue til IPC bussen. Et sådant vindue kan udnyttes til acces af memory på de tidligere IPC 6000 memorykort eller til acces af fælles (to port el. lign.) memory på evt. nye moduler.

Urkreds:

Kortet er forsynet med en urkreds, der også indeholder to timere, et RAM areal på 32 bytes, alarmkredsløb og power-fail detect kredsløb

med mulighed for automatisk at gemme det tidspunkt, hvor power forsvandt.
Osc. signalet fra urkredsen er ført ud via buffer til testpunktet TP til hjælp ved justering af uret. Når kortet har nået drifts-temperatur, justeres trimmekondsatoren til en osc. frekvens på 32,768 kHz.

Desuden er både ur og RAM forsynet med batteri back-up. Batteri status kan aflæses, dels via urkredsen selv, dels via et register i urkredsen, som sættes af initialiseringsprogrammet.

Bemærk, at registeret, som skrives via init, opdateres kun ved power on, mens statusbitten i urkredsen giver den aktuelle status. Init programmet tester hvorvidt RAM back-up controlleren har konstateret battery low siden sidste power-off og opdaterer et register (9E) i urkredsen i overensstemmelse hermed (9E=00 => ok, 9E=C3 => fail). Se desuden datablad for DS 1210 kredsen i appendix.

Back-up tid: Min. 1,5 år Typisk 3 - 5 år.
(typisk 3 års samlet back-up over periode på 10 år, d.v.s. mindst 7 års power-on i perioden. Jumper til batt. disable, hvis kort lægges på lager).

Bankswitch:

EPROM'en er bankswitched via en Dallas Semiconductor DS 1222 kreds for at muliggøre lagring af et antal forskellige programversioner i samme kreds og således kunne indvælge netop den ønskede version før opstart.

Hver bank er på 32k bytes; med en 1M bit EPROM fås da 4 banks og med en 4M bit EPROM fås 16 banks.

Valg af bank foregår ved skrivning af en bestemt sekvens til bank-switch kredsen, som accesses via memoryområdet omkring E0000H.

Der skal foretages skrivninger (ialt 16 efter initialize) til for-skellige adresser i området, jfr. datablad for DS 1222 kredsen i appendix.

F.eks: Skrivninger til adresserne E000F, E000A, E0005, E000A, E0005, E0005, E0005, E000A, E000A, E0005, E000A, E0005, E000A, E000A, E0002, E0005, og E0005 vil indvælge bank nr. 08.

Første skrivning sikrer, at kredsen er i rette start-tilstand.

Denne bankswitchmetode er valgt fremfor den simple register-skrivningsmetode, da det her sikres, at programfejl ikke vil kunne give utilsigtede skift af bank; dette er især vigtigt, når et watch-dog kredsløb skal kunne genstarte det ønskede program.

Waitstates:

Processoren kan programmeres til det ønskede antal waitstates for hhv. memory og IO som beskrevet i databogen for processoren.

Der er desuden som tidligere mulighed for at indsætte yderligere waitcycles ved brug af WAIT-signalet i bussen.

Med et CPU krystal på op til 12,3 Mhz kan der normalt anvendes 0 waitcycles til memoryacces på 6710 kortet, hvis der anvendes hurtige RAM/EPROM/EEPROM kredse.

Ved I/O acces over IPC bussen skal der anvendes mindst 2 waitstates (processoren anvender altid 0 waitstates ved acces af de interne I/O registre på kredsen) for de hidtidige I/O kort; det nødvendige antal waits afhænger generelt af såvel korttype som brug af bus-extender.

EEPROM skrivning:

Ved skrivning i EEPROM skal access altid foregå over adr. E0000H, ligesom de første 4k bytes kun kan skrives i intern- eller system-mode.

Der kan skrives på to måder, byte write eller page write:

Byte write: Der skrives een byte til kredsen, hvorefter der ventes i 10 mS eller ventes ved datapolling indtil skrivningen er tilendebragt.

Page write: Kredsen har en 64 byte page write mode, hvor op til 64 bytes (indenfor page addr.) kan skrives til kredsen umiddelbart efter hinanden, hvorefter der ventes 10mS eller polles, indtil page write er færdig. Page write skal foretages med disablet interruptsystem, da kredsen har bestemte krav til tidsafstanden mellem block write cycles.

Skrivningen udføres bekvemt med processorens "Load and repeat" instruktion; denne kan imidlertid afbrydes af interrupts, hvorfor interruptsystemet skal være disablet.

Se desuden databogen for Seeq DQ 28C64N EEPROM.

DMA:

Processoren har to DMA kanaler indbygget; kun den ene anvendes her (CH 0), idet kontrolsignalerne til DMA kanal 1 er konfigureret til brug for mode-setting i denne anvendelse. DMA kanal 0 kan derimod anvendes til alle DMA operationer (mem/\mem el. mem/IO), og request- og done signalerne er ført ud på bussen. Mht. opsætning henvises til databogen.

PS: DMA kan ikke benyttes, hvis der er monteret et IPC 6092 kort i kabinettet.

Clocked Serial I/O port:

Processoren indeholder foruden de to alm. serielle porte en clocked serial I/O port, der benytter tre signaler (Clock, data ud og data ind) til kommunikation med andre kredse. Disse signaler er ført ud på bussen, således at kredsen på CPU printet er master, mens evt. andre kredse er slaver (master leverer clock og slavers transmit-signal skal være open collector; slaver svarer kun ved poll). Mht. anvendelse af CSI port henvises til databogen.

Clockudgangen fra CSI porten er også forbundet til timer clock ind-gangen på urkredsen, og kan således benyttes til clockning af disse timere, hvis der i urkredsen vælges ekstern clock.

PS: CSI porten kan ikke benyttes, hvis der er monteret et IPC 6092 kort i kabinettet.

Timere:

Processoren indeholder:	To reload timere	T0 og T1
	En programmerbar timer	T2
Urkredsen indeholder:	To multimode timere	RTC0 og RTC1

Nogle af disse timere er her forbeholdt faste anvendelser:

- Processorkredsens T1 timer er forbeholdt watchdog anvendelse, idet udgangen fra denne timer TOUT1 er forbundet til watchdog triggerindgangen. Såfremt watchdog'en ikke ønskes benyttet, kan TOUT1 disables, og timer T1 kan anvendes som generel timer.

- Urkredsens RTC1 timer er forbeholdt for proces timer interrupt anvendelse, idet timerudgangen er forbundet til processorens højst prioriterede interrupt indgang, NMI. Forbindelsen kan dog disables via bit D7 i kontrolregisteret på adr. A0H, hvis denne facilitet ikke ønsket benyttet (eller indtil processkift igangsættes).

Timerne T0, T2 og RCT0 kan benyttes som generelle timere. Den programmerbare timer T2 har to udgange (TOUT2 og TOUT3), der kan benyttes i forskellige modes (timer compare, timer overflow m.m.). Udgangene kan via strap S6 føres ud på IPC bussen.

PS: Denne strapning må ikke foretages i et system, hvor IPC 6092 kortet anvendes.

Watchdog:

Udgangen fra timer T1 (TOUT1) er forbundet til reset kredsløbet via en one shot timer. Ved udløb af T1 kan der således gives reset til processoren. Programmet skal altså ved normal drift sørge for at skrive en ny tællerværdi til T1 inden udløb.

>>> Ved udløb resettes både processoren og periferikredse på bussen,
>> ligesom der startes i USER-MODE, d.v.s. bankswitch setting be-
> holdes, og boot programmet/system-mode overspringes.

Interrupts:

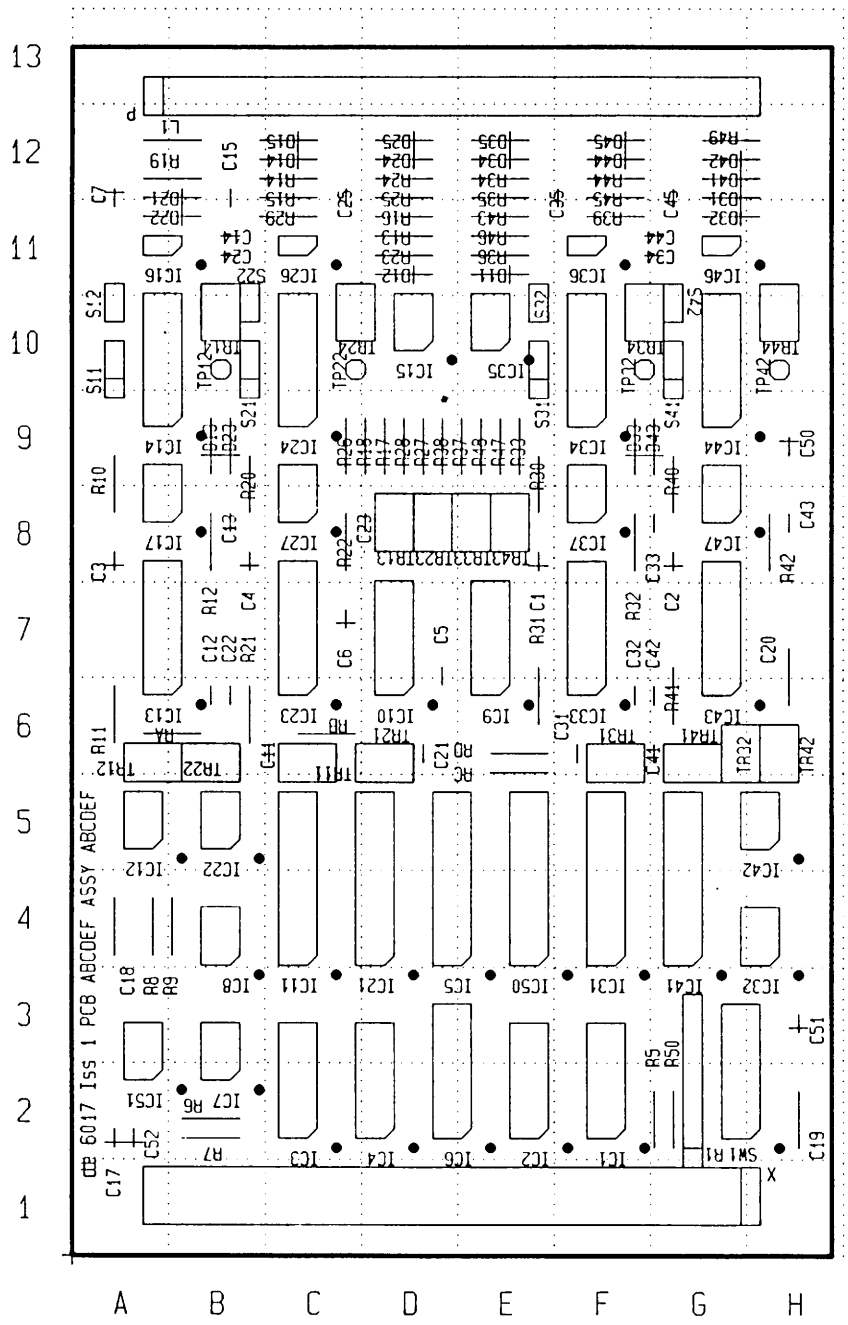
Prioritet:		Name:
(high)		
1	TRAP	Internt CPU interrupt
2	NMI	Periodisk tidsintr. fra urkreds, RTC1 (typ. 2 mS intr., kan ena/disa via reg)
3	INT0	"Call Debug" via DB9 pin 9
4	INT1	Bus interrupt RST 5.5
5	INT2	Bus interrupt INT
6	INPUT CAPT.	Alarm intr. (INTR) fra urkreds
7	OUTPUT COMP.	Intern) i forb. m.
8	TIMER 2 OVFL.	Intern) TOUT2 og TOUT3 på bus
9	TIMER 0	Intern
10	TIMER 1	Anv. til watchdog, TOUT1 giver reset
11	DMA CH0	DMA controller
12	DMA CH1	(anvendes ikke)
13	CSI	Clocked serial I/O port via bus
14	ASCI CH0	232/485 port på DB25 (alle handshakes)
15	ASCI CH1	232 port på DB9 (ingen handshakes)
(low)		

Pin 9 på DB9 stikket er via en RS232 receiver ført til INT0 interrupt-indgangen på processorkredsen; dette kan anvendes til at give CPU kortet et helt eksternt interrupt, f.eks. til debug call.

DC/DC converter option:

Såfremt kortet ønskes anvendt som singleboard computer med forsyning udelukkende fra +5 volt, kan der på kortet monteres (IC5) en DC/DC converter kreds, der fra +5 V leverer +-12 V til RS232 driverne (kun til RS232, ikke til +-12 V output på DB25).

Komponentplacering:



Temperatur detektor:

Der er på kortet anbragt en temperaturføler, der kan anvendes til at måle, hvorvidt omgivelsestemperaturen for kortet er over den maksimalt tilladelige, hvilket er 70 grader Celcius.

Føleren efterfølges af en open collector komparator, der er indstillet til et switchniveau på 70 C. Collector signalet er forbundet til pull-up modstanden for strap S1 pin 1, d.v.s. denne strap får to forskellige anvendelser:

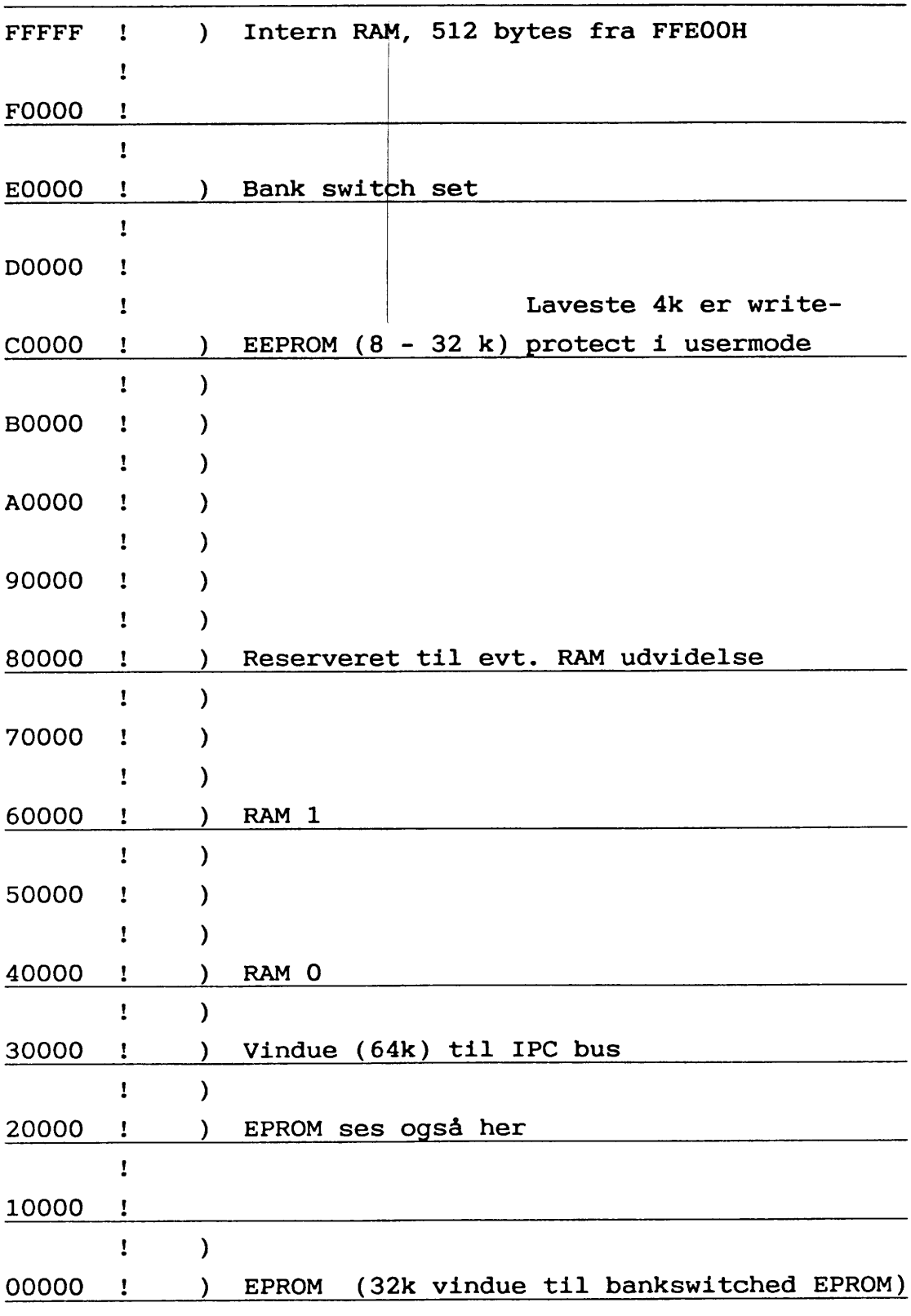
1) Når strappen ønskes anvendt som user defined input, monteres temperaturføleren ikke, og pin 2 til pin 3 på IC31's position kortsluttes.

2) Når indgangen ønskes anvendt som high temp detect, må strap S1 pin 1-2 ikke være kortsluttet, og temperaturføleren skal være monteret. Ved en omgivelsestemperatur på over 70 grader vil komparatorudgangen da sætte port G bit 2 lav, hvilket kan aflæses af processoren.

Om ønsket kan værdien af switchtemperaturen ændres ved at ændre på modstandsdelingen ved IC31.

Memory adressering:

I user-mode ser memoryområdet således ud:



I intern mode (f.eks. efter power-up):

I området 0 - 10000H selekteres EPROM ikke, men processorens interne EPROM (16k bytes) selekteres.
Resten af memoryområdet ses ligesom i usermode; dog er EEPROM ikke writeprotected i de første 4k.

I system mode:

I området 0 - 10000H selekteres ikke EPROM, men derimod EEPROM'en. EEPROM'en er dog her read only.
Resten af memoryområdet ses ligesom i usermode.

I/O adressering:

0000 til 007FH: Interne CPU I/O registre, se databog for Hitachi HD647180 processor kredsen.

0080 til 009FH: Registre 00 - 1FH i ur kredsen, se data for for National 8570A kredsen.

00A0: Control register (write only):

D7	NMI enable
D6	Select RS485
D5	RS485 Transmit enable
D4	RS485 Receiver disable
D3	DTR A0 (Active low)
D2	Gate 0 inp. på urkreds (act low)
D1	LED L2 Rød disable
D0	LED L2 Grøn disable

Control register after power-up: 00H

00A1 til 00BFH (Reserved)

00C0: Mode register strobe

Skrivning til denne adr. sætter mode flip-flops i overensstemmelse med data på PA7 og PA6:

PA7 = MP0/MP1N ; = 0 (mode 2) ved power-on
PA6 = USR/SYSN ; = 0 (system) ved power-on

00C1 til 00DFH (Reserved)

00E0: Soft reset strobe.

Skrivning til denne adresse giver reset til processoren, men ikke til periferi eller bus.

00E1 til 00FFH (Reserved)

0100 til 7FFFH Not used.

8000 til FFFFH Extern I/O:

Ved enhver extern adressering, d.v.s. adressering over IPC bussen, skal adresse bit 15 være sat. Den mindst betydende byte (A7 til A0) anvendes til port adressering på IPC kort (som tidligere). Adressebits A11 till A8 anvendes til IPC kort TYPE adressering, og bits A14 til A12 anvendes kun i forbindelse med nye typer kort, som udnytter "Advanced Modules" typen (type A) til udvidet type adresse.

A15:	Extern adresserings bit
A14 - A12:	Udvidet type adresse
A11 - A8:	Type adresse
A7 - A0:	Port adresse

Specielt vedrørende CPU port A og G:

Port A:	D7	PA7 til mode-set eller LCD DA ved test
	D6	PA6 til mode-set eller LCD EN ved test
	D5	config til CKS eller LCD CK ved test
	D4	config til RXS
	D3	config til TXS
	D2	config til TENDON
	D1	config til RxA1
	D0	config til TxA1
Port G:	D7	Undefined
(6 inp)	D6	Undefined
	D5	DSR fra DB25 stik
	D4	DCD fra DB25 stik
	D3	RI fra DB25 stik
	D2	Hightemp (aktiv lav), evt. user def. strap
	D1	USER DEF. STRAP
	D0	Debug option strap

Strapsettings: When strap mounted:

S1 :
.* * Batt. back-up enable
* * Debug select efter power on
* * (User definable)
* * (User definable eller temp detect)
Normal strapping: Ingen forb.
Batt. back-up enable ved
ibrugtagning af kortet.

S2 :
.* * P25 protective GND connected
to digital GND.
Normal strapping: Ingen forb.

Signals on strap pins:

S3 :
.* +5 V
* PA7 (DA) Extern test
* PA6 (EN) output conn
* PA5 (CK) option.
* GND
Normal strapping: Ingen forb.

S4 :
.* RAM VCC
* RAM pin 30
* A17

Pin 1-2 conn: 1Mbit kredse
Pin 2-3 conn: 4Mbit kreds.
Normal strapping: 1-2.

S5 :
.* Refresh pin fra 647180
* RAM pin 1
* A18

Pin 1-2 conn: 1Mbit kredse
Pin 2-3 conn: 4Mbit kreds.
Normal strapping: 1-2.

S6 :	.*	*	TOUT2 til bus
	*	*	TOUT3 til bus
			Normal strapping: Ingen forb.
S7 :	.*	*	-12 V til DB25 pin 9
			Normal strapping: Ingen forb.
S8 :	.*	*	+5 V til DB25 pin 18
			Normal strapping: Ingen forb.
S9 :	.*	*	+12 V til DB25 pin 21
			Normal strapping: Ingen forb.

Tilslutning til IPC bus:

Buskonnektoren er ligesom tidligere en 64 polet DIN konnektor (DIN 41612 C-form). Bussignalerne er kompatible med signalerne på det tidligere IPC 6000 CPU kort. Der er kommet enkelte tilføjelser, idet bl.a. DMA og Clocked Serial I/O nu er muligt.

Mht. signalbeskrivelser henvises til IPC/1 Systembeskrivelsen.

De enkelte signalers placering fremgår af næste side.

Forbindelser til bus:

Pin:	a	c
1	+ 5 V	+ 5 V
2	GND	GND
3	+ 12 V	+ 12 V
4	*RESET*	
5		
6		
7		
8		
9	A7	A6
10	A5	A4
11	A3	A2
12	A1	A0
13	IA3	IA2
14	IA1	IA0
15	D7	D6
16	D5	D4
17	D3	D2
18	D1	D0
19		
20	*INR*	*OUTR*
21		
22		
23		
24		
25		
26		
27	+ 15 V	+ 15 V
28	V strap	V strap
29	V+ strap	V+ strap
30	- 12 V	- 12 V
31	GND	GND
32	+ 5 V	+ 5 V

Forbindelser til bus: X konnector.

Pin:	a	c
1	+ 5 V	+ 5 V
2	GND	GND
3	+12 V	+12 V
4	*RESET*	CLK
5	A15	A14
6	A13	A12
7	A11	A10
8	A9	A8
9	A7	A6
10	A5	A4
11	A3	A2
12	A1	A0
13	IA3	IA2
14	IA1	IA0
15	D7	D6
16	D5	D4
17	D3	D2
18	D1	D0
19	*RR*	*WR*
20	*INR*	*OUTR*
21	*INT*	n.c.
22	*HOLD*	*HOLDA*
23	*RST 5.5*	*BUS DISABLE*
24	*WAIT*	*CKS*
25	*TXS*	*RXS*
26	*DMARQ*	*DMAEND*
27	*TOUT2*	*TOUT3*
28 (GND)	-24 V	-24 V
29 (+24 V)	GND (24V)	GND (24V)
30	-12 V	-12 V
31	GND	GND
32	+ 5 V	+ 5 V

* markerer, at signalet er active low.

Pin forbindelser til stik:

PORT 0 (DB25s):

Pin:	Signal:
1	Protective GND (forbindes til digital GND, hvis S2 conn)
2	RS232 TxData
3	RS232 RxData
4	RS232 RTS
5	RS232 CTS
6	RS232 DSR (via PG5)
7	Signal GND
8	RS232 DCD (via PG4)
9	-12 V via strap S7
10	RS485 Data +
11	nc
12	nc
13	nc
14	nc
15	nc
16	nc
17	nc
18	+5 V via strap S8
19	nc
20	RS232 DTR (via control register)
21	+12 V via strap S9
22	RS232 RI (via PG3)
23	nc
24	RS485 Data -
25	nc

Port 0 kan anvendes som enten en RS232 eller en RS485 forbindelse. Via kontrol registeret på I/O adr. A0H kan vælges den ønskede konfiguration, ligesom RX og TX for RS485 kan enables/disables via kontrolregisteret. RS485 forbindelsen er udført som en party line.

PORT 1 (DB9s):

Pin:	Signal:	(Pinforbindelser svarer til DB9 på PC'er)
1	nc	
2	RS232	RxData
3	RS232	TxData
4	RS232	DTR (pull-up via res. til +12 V)
5	Signal	GND
6	nc	
7	RS232	RTS (pull-up via res. til +12 V)
8	RS232	(CTS, not connected after receiver)
9	RS232	RI, Call Debug via INT0

Aktivitet på de to porte vises vha. en rød/grøn LED (L1). Receive aktivitet på en af de to porte giver grønt lys, transmit aktivitet giver rødt lys.

ures	MM58167A	MM58274C
	24 Hour 0.01 sec thru Months No Status Bit	12 or 24 Hr. 0.1 sec thru Years Yes Status Bit
	Parallel 5 8 1050 ns	Parallel 4 4 650 ns
ıts) Time Data Valid)		
	56 Bits (14 × 4)	No
e re e er	0.1 sec thru Months Yes Yes Yes	0.1, 0.5, 1, 5, 10, 30 and 60 sec No No Yes
quency illator Output	32.768 kHz No	32.768 kHz Yes
l l)D Max)	4.5–5.5V 2.2V min 5 mA 20 μA	4.5–5.5V 2.2V min 1 mA 10 μA
GY		
	CMOS	CMOS
	24 DIP 28 PCC	16 DIP 20 PCC

DP8570A Timer C Peripheral (TCP)

General Description

The DP8570A is intended for use in microprocessor based systems where information is required for multi-tasking, data logging or general time of day/date information. This device is implemented in low voltage silicon gate microCMOS technology to provide low standby power in battery back-up environments. The circuit's architecture is such that it looks like a contiguous block of memory or I/O ports. The address space is organized as 2 software selectable pages of 32 bytes. This includes the Control Registers, the Clock Counters, the Alarm Compare RAM, the Timers and their data RAM, and the Time Save RAM. Any of the RAM locations that are not being used for their intended purpose may be used as general purpose CMOS RAM.

Time and date are maintained from 1/100 of a second to year and leap year in a BCD format, 12 or 24 hour modes. Day of week, day of month and day of year counters are provided. Time is controlled by an on-chip crystal oscillator requiring only the addition of the crystal and two capacitors. The choice of crystal frequency is program selectable.

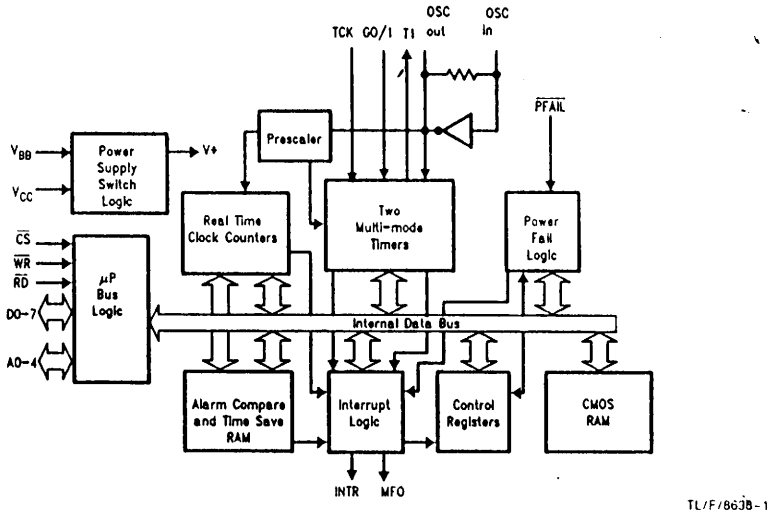
Two independent multifunction 10 MHz 16-bit timers are provided. These timers operate in four modes. Each has its own prescaler and can select any of 8 possible clock inputs. Thus, by programming the input clocks and the timer counter values a very wide range of timing durations can be achieved. The range is from about 400 ns (4.915 MHz oscillator) to 65,535 seconds (18 hrs., 12 min.).

Power failure logic and control functions have been integrated on chip. This logic is used by the TCP to issue a power fail interrupt, and lock out the μp interface. The time power fails may be logged into RAM automatically when $V_{BB} > V_{CC}$. Additionally, two supply pins are provided, and upon power failure detection, internal circuitry will automatically switch from the main supply to the battery supply. Status bits are provided to indicate initial application of battery power, system power, and low battery detect. (Continued)

Features

- Full function real time clock/calendar
  - 12/24 hour mode timekeeping
  - Day of week and day of years counters
  - Four selectable oscillator frequencies
  - Parallel Resonant Oscillator
- Two 16-bit timers
  - 10 MHz external clock frequency
  - Programmable multi-function output
  - Flexible re-trigger facilities
- Power fail features
  - Internal power supply switch to external battery
  - Power Supply Bus glitch protection
  - Automatic log of time into RAM at power failure
- On-chip interrupt structure
  - Periodic, alarm, timer and power fail interrupts
- Up to 44 bytes of CMOS RAM
- INTR/MFO pins programmable High/Low and push-pull or open drain

Block Diagram



TL/F/8638-1

FIGURE 1

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to V_{CC} +0.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation (PD)	500 mW
Lead Temperature (Soldering, 10 sec.)	260°C

Operation Conditions

	Min	Max	Unit
Supply Voltage (V_{CC}) (Note 3)	4.5	5.5	V
Supply Voltage (V_{BB}) (Note 3)	2.2	V_{CC} 0.4	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0.0	V_{CC}	V
Operation Temperature (T_A)	−40	+85	°C
Electr-Static Discharge Rating TBD		1	kV

DC Electrical Characteristics

V_{CC} = 5V ±10%, V_{BB} = 3V, V_{PFAIL} > V_{IH}, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage (Note 4)	Any Inputs Except OSC IN, OSC IN with External Clock	2.0 V_{BB} − 0.1		V V
V_{IL}	Low Level Input Voltage	All Inputs Except OSC IN OSC IN with External Clock		0.8 0.1	V V
V_{OH}	High Level Output Voltage (Excluding OSC OUT)	I_{OUT} = −20 μA I_{OUT} = −4.0 mA	V_{CC} −0.1 3.5		V V
V_{OL}	Low Level Output Voltage (Excluding OSC OUT)	I_{OUT} = 20 μA I_{OUT} = 4.0 mA		0.1 0.25	V V
I_{IN}	Input Current (Except OSC IN)	V_{IN} = V_{CC} or GND		±1.0	μA
I_{OZ}	Output TRI-STATE® Current	V_{OUT} = V_{CC} or GND		±5.0	μA
I_{LKG}	Output High Leakage Current T1, MFO, INTR Pins	V_{OUT} = V_{CC} or GND Outputs Open Drain		±5.0	μA
I_{CC}	Quiescent Supply Current (Note 7)	F_{OSC} = 32.768 kHz V_{IN} = V_{CC} or GND (Note 5) V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)		260 1.0 12.0	μA mA mA
		F_{OSC} = 4.194304 MHz or 4.9152 MHz V_{IN} = V_{CC} or GND (Note 6) V_{IN} = V_{IH} or V_{IL} (Note 6)		8 20	mA mA
I_{CC}	Quiescent Supply Current (Single Supply Mode) (Note 7)	V_{BB} = GND V_{IN} = V_{CC} or GND F_{OSC} = 32.768 kHz F_{OSC} = 4.9152 MHz or 4.194304 MHz		80 7.5	μA mA
I_{BB}	Standby Mode Battery Supply Current (Note 8)	V_{CC} = GND F_{OSC} = 32.768 kHz F_{OSC} = 4.9152 MHz or 4.194304 MHz		10 400	μA μA
I_{BLK}	Battery Supply Leakage	2.2V ≤ V_{BB} ≤ 4.0V	−5	1.5	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: For F_{OSC} = 4.194304 or 4.9152 MHz, V_{BB} minimum = 2.8V. In battery backed mode, V_{BB} = V_{CC} −0.4V.
Single Supply Mode: Data retention voltage is 2.2V min.
In single Supply Mode (Power connected to V_{CC} pin) 4.5V ≤ V_{CC} ≤ 5.5V.

Note 4: This parameter (V_{IH}) is not tested on all pins at the same time.

Note 5: This specification tests I_{CC} with all power fail circuitry disabled, by setting D7 of Interrupt Control Register 1 to 0.

Note 6: This specification tests I_{CC} with all power fail circuitry enabled, by setting D7 of Interrupt Control Register 1 to 1.

Note 7: This specification is tested with both the timers and OSC IN driven by a signal generator. Contents of the Test Register = 00(H), the MFO pin is not configured as buffered oscillator out and MFO, T1, INTR, are configured as open drain.

Note 8: This specification is tested with both the timers off, and only OSC IN is driven by a signal generator. Contents of the Test Register = 00(H) and the MFO pin is not configured as buffered oscillator out

AC Electrical Characteristics

V_{CC} = 5V ±10%, V_{BB} = 3V, V_{PFAIL} > V_{IH}, C_L = 100 pF (unless otherwise specified)

Symbol	Parameter	Min	Max	Units
READ TIMING				
t_{AR}	Address Valid Prior to Read Strobe	20		ns
t_{RW}	Read Strobe Width (Note 9)	80		ns
t_{CD}	Chip Select to Data Valid Time		80	ns
t_{RAH}	Address Hold after Read (Note 10)	3		ns
t_{RD}	Read Strobe to Valid Data		70	ns
t_{DZ}	Read or Chip Select to TRI-STATE		60	ns
t_{RCH}	Chip Select Hold after Read Strobe	0		ns
t_{DS}	Minimum Inactive Time between Read or Write Accesses	50		ns
WRITE TIMING				
t_{AW}	Address Valid before Write Strobe	20		ns
t_{WAH}	Address Hold after Write Strobe (Note 10)	3		ns
t_{CW}	Chip Select to End of Write Strobe	90		ns
t_{WW}	Write Strobe Width (Note 11)	80		ns
t_{DW}	Data Valid to End of Write Strobe	50		ns
t_{WDH}	Data Hold after Write Strobe (Note 10)	3		ns
t_{WCH}	Chip Select Hold after Write Strobe	0		ns
TIMER 0/TIMER 1 TIMING				
F_{TCK}	Input Frequency Range	DC	10	MHz
t_{CK}	Propagation Delay Clock to Output		120	ns
t_{GO}	Propagation Delay G0 to G1 to Timer Output (Note 12)		100	ns
t_{PGW}	Pulse Width G0 or G1	25		ns

Note 9: Read Strobe width as used in the read timing table is defined as the period when both chip select and read inputs are low. Hence read commences when both signals are low and terminates when either signal returns high.

Note 10: Hold time is guaranteed by design but not production tested. This limit is not used to calculate outgoing quality levels.

Note 11: Write Strobe width as used in the write timing table is defined as the period when both chip select and write inputs are low. Hence write commences when both signals are low and terminates when either signal returns high.

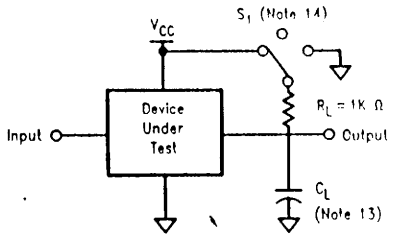
Note 12: Timers in Mode 3.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	6 ns (10%–90%)
Input and Output Reference Levels	1.3V
TRI-STATE Reference Levels (Note 14)	Active High +0.5V Active Low −0.5V

Note 13: C_L = 100 pF, includes jig and scope capacitance.

Note 14: S1 = V_{CC} for active low to high impedance measurements.
S1 = GND for active high to high impedance measurements.
S1 = open for all other timing measurements.



Capacitance (T_A = 25°C, f = 1 MHz)

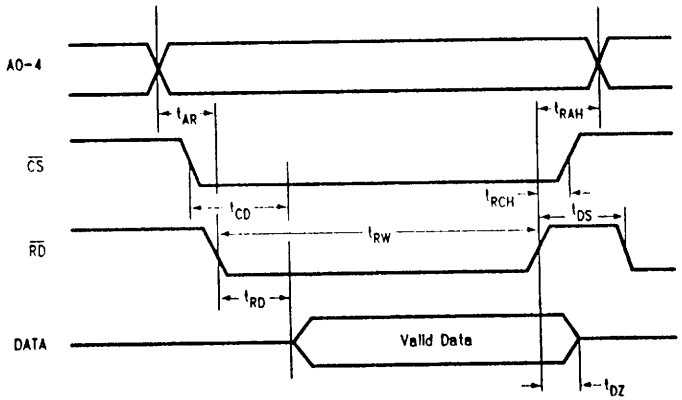
Symbol	Parameter (Note 15)	Typ	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	7	pF

Note 15: This parameter is not 100% tested.

Note 16: Output rise and fall times 25 ns max (10%–90%) with 100 pF load.

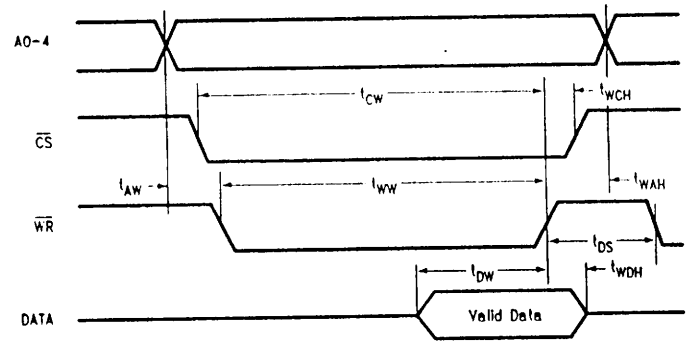
ning Wavefo

Read Timing Diagram



TL/F/8638-24

Write Timing Diagram



TL/F/8638-25

General Description (Continued)

The DP8570A's interrupt structure provides four basic types of interrupts: Periodic, Alarm/Compare, Timer, and Power Fail. Interrupt mask and status registers enable the masking and easy determination of each interrupt.

One dedicated general purpose interrupt output is provided. A second interrupt output is available on the Multiple Function Output (MFO) pin. Each of these may be selected to generate an interrupt from any source. Additionally, the MFO pin may be programmed to be either as oscillator output or Timer 0's output.

Pin Description

$\overline{CS}$, $\overline{RD}$, $\overline{WR}$ (Inputs): These pins interface to μP control lines. The $\overline{CS}$ pin is an active low enable for the read and write operations. Read and Write pins are also active low and enable reading or writing to the TCP. All three pins are disabled when power failure is detected. However, if a read or write is in progress at this time, it will be allowed to complete its cycle.

A0–A4 (Inputs): These 5 pins are for register selection. They individually control which location is to be accessed. These inputs are disabled when power failure is detected.

OSC IN (Input); OSC OUT (Output): These two pins are used to connect the crystal to the internal parallel resonant oscillator. The oscillator is always running when power is applied to V_{BB} and V_{CC}, and the correct crystal select bits in the Real Time Mode Register have been set.

MFO (Output): The multi-function output can be used as a second interrupt output for interrupting the μP. This pin can also provide an output for the oscillator or the internal Timer 0. The MFO output can be programmed active high or low, open drain or push-pull. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

INTR (Output): The interrupt output is used to interrupt the processor when a timing event or power fail has occurred and the respective interrupt has been enabled. The INTR output can be programmed active high or low, push-pull or open drain. If in battery backed mode and a pull-up resistor is attached, it should be connected to a voltage no greater than V_{BB}.

D0–D7 (Input/Output): These 8 bidirectional pins connect to the host μP's data bus and are used to read from and write to the TCP. When the $\overline{PFAIL}$ pin goes low and a write is not in progress, these pins are at TRI-STATE.

$\overline{PFAIL}$ (Input): In battery backed mode, this pin can have a digital signal applied to it via some external power detection logic. When $\overline{PFAIL}$ = logic 0 the TCP goes into a lockout mode, in a minimum of 30 μs or a maximum of 63 μs unless lockout delay is programmed. In the single power supply mode, this pin is not useable as an input and should be tied to V_{CC}. Refer to section on Power Fail Functional Description.

V_{BB} (Battery Power Pin): This pin is connected to a back-up power supply. This power supply is switched to the internal circuitry when the V_{CC} becomes lower than V_{BB}. Utilizing this pin eliminates the need for external logic to switch in and out the back-up power supply. If this feature is not to be used then this pin must be tied to ground, the TCP programmed for single power supply only, and power applied to the V_{CC} pin.

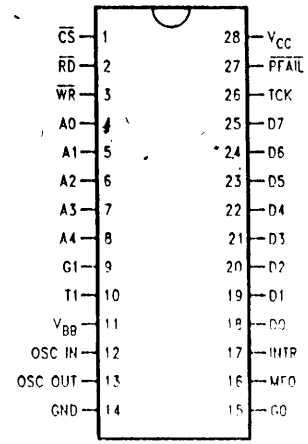
TCK, G1, G0, (Inputs), T1 (Output): TCK is the clock input to both timers when they have an external clock selected. G0 and G1 are active low enable inputs to timers 0 and 1 respectively. T1 is dedicated to the timer 1 output. The T1 output can be programmed active high or low, push-pull or open drain. Timer 0 output is available through MFO pin if desired. If in battery backed mode and a pull-up resistor is attached to T1, it should be connected to a voltage no greater than V_{BB}.

V_{CC}: This is the main system power pin.

GND: This is the common ground power pin for both V_{BB} and V_{CC}.

Connection Diagrams

Dual-In-Line

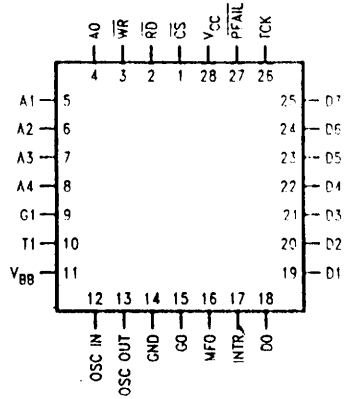


TL/F/8638-1

Top View

Order Number DP8570AJ or DP8570AN
See NS Package Number J28A or N28B

Plastic Chip Carrier



TL/F/8638-1

Top View

Order Number DP8570AV
See NS Package Number V28A

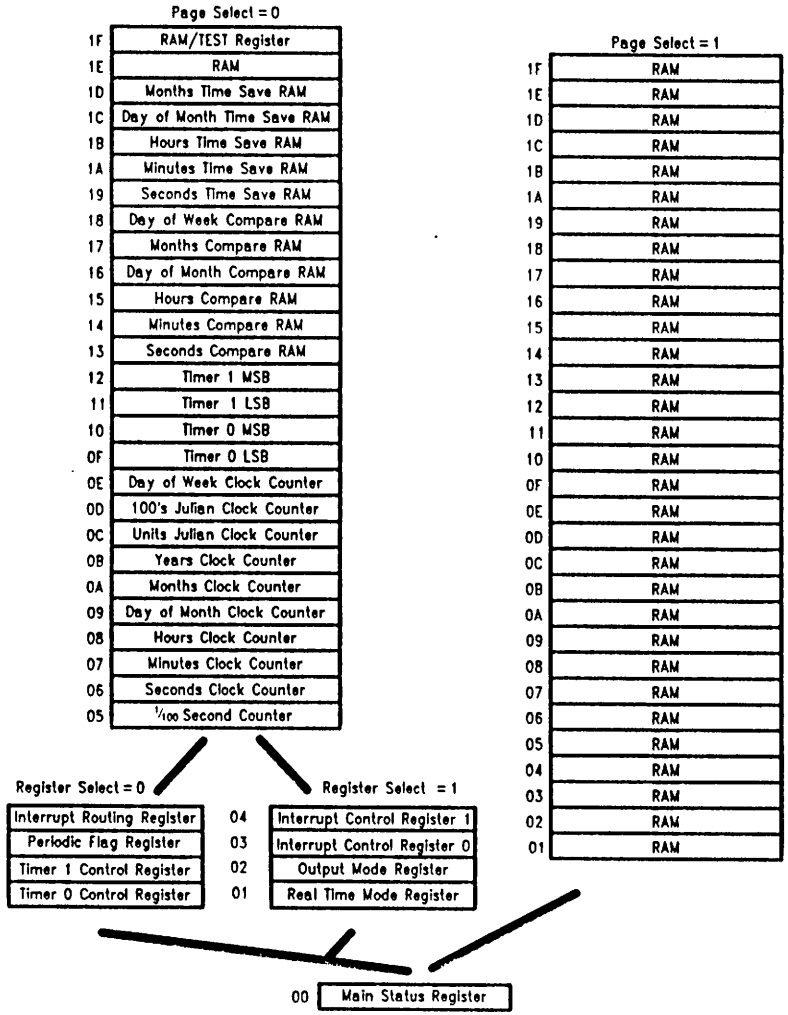
Functional Description

The DP8570A contains a fast access real time clock, two 10 MHz 16-bit timers, interrupt control logic, power fail detect logic, and CMOS RAM. All functions of the TCP are controlled by a set of nine registers. A simplified block diagram that shows the major functional blocks is given in *Figure 1*.

The blocks are described in the following sections:

1. Real Time Clock
2. Oscillator Prescaler
3. Interrupt Logic
4. Power Failure Logic
5. Additional Supply Management
6. Timers

The memory map of the TCP is shown in the memory addressing table. The memory map consists of two 31 byte pages with a main status register that is common to both pages. A control bit in the Main Status Register is used to select either page. *Figure 2* shows the basic concept. Page 0 contains all the clock timer functions, while page 1 has scratch pad RAM. The control registers are split into two separate blocks to allow page 1 to be used entirely as scratch pad RAM. Again a control bit in the Main Status Register is used to select either control register block.



TL/F/8638–4

FIGURE 2. DP8570A Internal Memory Map

Functional Description (Continued)

INITIAL POWER-ON of BOTH V_{BB} and V_{CC}

V_{BB} and V_{CC} may be applied in any sequence. In order for the power fail circuitry to function correctly, whenever power is off, the V_{CC} pin must see a path to ground through a maximum of 1 MΩ. The user should be aware that the control registers will contain random data. The first task to be carried out in an initialization routine is to start the oscillator by writing to the crystal select bits in the Real Time Mode Register. If the DP8570A is configured for single supply mode, an extra 50 µA may be consumed until the crystal select bits are programmed. The user should also ensure that the TCP is not in test mode (see register descriptions).

REAL TIME CLOCK FUNCTIONAL DESCRIPTION

As shown in *Figure 2*, the clock has 10 bytes of counters, which count from 1/100 of a second to years. Each counter counts in BCD and is synchronously clocked. The count sequence of the individual byte counters within the clock is shown later in Table VII. Note that the day of week, day of month, day of year, and month counters all roll over to 1. The hours counter in 12 hour mode rolls over to 1 and the AM/PM bit toggles when the hours rolls over to 12 (AM = 0, PM = 1). The AM/PM bit is bit D7 in the hours counter.

All other counters roll over to 0. Also note that the day of year counter is 12 bits long and occupies two addresses. Upon initial application of power the counters will contain random information.

READING THE CLOCK: VALIDATED READ

Since clocking of the counter occurs asynchronously to reading of the counter, it is possible to read the counter while it is being incremented (rollover). This may result in an incorrect time reading. Thus to ensure a correct reading of the entire contents of the clock (or that part of interest), it must be read without a clock rollover occurring. In general this can be done by checking a rollover bit. On this chip the periodic interrupt status bits can serve this function. The following program steps can be used to accomplish this.

1. Initialize program for reading clock.
2. Dummy read of periodic status bit to clear it.
3. Read counter bytes and store.
4. Read rollover bit, and test it.
5. If rollover occured go to 3.
6. If no rollover, done.

To detect the rollover, individual periodic status bits can be polled. The periodic bit chosen should be equal to the highest frequency counter register to be read. That is if only SECONDS through HOURS counters are read, then the SECONDS periodic bit should be used.

READING THE CLOCK: INTERRUPT DRIVEN

Enabling the periodic interrupt mask bits cause interrupts just as the clock rolls over. Enabling the desired update rate and providing an interrupt service routine that executes in less than 10 ms enables clock reading without checking for a rollover.

READING THE CLOCK: LATCHED READ

Another method to read the clock that does not require checking the rollover bit is to write a one into the Time Save Enable bit (D7) of the Interrupt Routing Register, and then to write a zero. Writing a one into this bit will enable the clock contents to be duplicated in the Time Save RAM. Changing the bit from a one to a zero will freeze and store the contents of the clock in Time Save RAM. The time then can be read without concern for clock rollover, since internal logic takes care of synchronization of the clock. Because only the bits used by the clock counters will be latched, the Time Save RAM should be cleared prior to use to ensure that random data stored in the unused bits do not confuse the host microprocessor. This bit can also provide time save at power failure, see the Additional Supply Management Functions section. With the Time Save Enable bit at a logical 0, the Time Save RAM may be used as RAM the latched read function is not necessary.

INITIALIZING AND WRITING TO THE CALENDAR-CLOCK

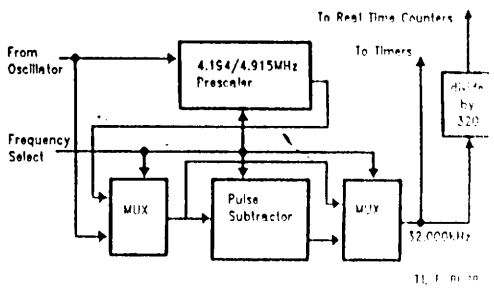
Upon initial application of power to the TCP or when making time corrections, the time must be written into the clock. To correctly write the time to the counters, the clock would normally be stopped by writing the Start/$\overline{\text{Stop}}$ bit in the Real Time Mode Register to a zero. This stops the clock from counting and disables the carry circuitry. When initializing the clock's Real Time Mode Register, it is recommended that first the various mode bits be written while maintaining the Start/$\overline{\text{Stop}}$ bit reset, and then writing to the register second time with the Start/$\overline{\text{Stop}}$ bit set.

The above method is useful when the entire clock is being corrected. If one location is being updated the clock need not be stopped since this will reset the prescaler, and time will be lost. An ideal example of this is correcting the hour for daylight savings time. To write to the clock "on the fly" the best method is to wait for the 1/100 of a second periodic interrupt. Then wait an additional 16 µs, and then write the data to the clock.

PRESCALER/OSCILLATOR FUNCTIONAL DESCRIPTION

Feeding the counter chain is a programmable prescaler which divides the crystal oscillator frequency to 32 kHz and further to 100 Hz for the counter chain (see *Figure 3*). The crystal frequency that can be selected are: 32 kHz, 32.76 kHz, 4.9152 MHz, and 4.194304 MHz.

Once 32 kHz is generated it feeds both timers and the clock. The clock and timer prescalers can be independently enabled by controlling the timer or clock Start/$\overline{\text{Stop}}$ bits.



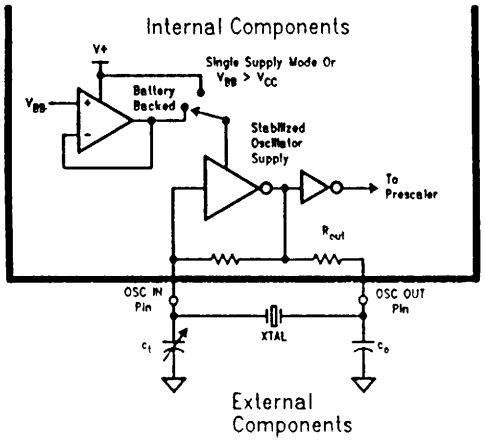
TL/F/8638–3

FIGURE 3. Programmable Clock Prescaler Block

Functional Description (Continued)

The oscillator is programmed via the Real Time Mode Register to operate at various frequencies. The crystal oscillator is designed to offer optimum performance at each frequency. Thus, at 32.768 kHz the oscillator is configured as a low frequency and low power oscillator. At the higher frequencies the oscillator inverter is reconfigured. In addition to the inverter, the oscillator feedback bias resistor is included on chip, as shown in *Figure 4*. The oscillator input may be driven from an external source if desired. Refer to test mode application note for details. The oscillator stability is enhanced through the use of an on chip regulated power supply.

The typical range of trimmer capacitor (as shown in Oscillator Circuit Diagram *Figure 4*, and in the typical application) at the oscillator input pin is suggested only to allow accurate tuning of the oscillator. This range is based on a typical printed circuit board layout and may have to be changed depending on the parasitic capacitance of the printed circuit board or fixture being used. In all cases, the load capacitance specified by the crystal manufacturer (nominal value 11 pF for the 32.768 crystal) is what determines proper oscillation. This load capcitance is the series combination of capacitance on each side of the crystal (with respect to ground).



TL/F/8638-3

FIGURE 4. Oscillator Circuit Diagram

XTAL	C_o	C_t	R_{OUT} (Switched Internally)
32/32.768 kHz	47 pF	2 pF–22 pF	150 kΩ to 350 kΩ
4.194304 MHz	68 pF	0 pF–80 pF	500Ω to 900Ω
4.9152 MHz	68 pF	29 pF–49 pF	500Ω to 900Ω

INTERRUPT LOGIC FUNCTIONAL DESCRIPTION

The TCP has the ability to coordinate processor timing activities. To enhance this, an interrupt structure has been implemented which enables several types of events to cause interrupts. Interrupts are controlled via two Control Registers in block 1 and two Status Registers in block 0. (See Register Description for notes on paging and also *Figure 5* and Table I.)

The interrupts are enabled by writing a one to the appropriate bits in Interrupt Control Register 0 and/or 1. Any of the interrupts can be routed to either the INTR pin or the MFO pin, depending on how the Interrupt Routing register is programmed. This, for example, enables the user to dedicate the MFO as a non-maskable interrupt pin to the CPU for power failure detection and enable all other interrupts to appear on the INTR pin. The polarity for the active interrupt can be programmed in the Output Mode Register for either active high or low, and open drain or push pull outputs.

TABLE I. Registers that are Applicable to Interrupt Control

Register Name	Register Select	Page Select	Address
Main Status Register	X	X	00H
Periodic Flag Register	0	0	03H
Interrupt Routing Register	0	0	04H
Interrupt Control Register 0	1	0	03H
Interrupt Control Register 1	1	0	04H
Output Mode Register	1	0	02H

The Interrupt Status Flag D0, in the Main Status Register, indicates the state of INTR and MFO outputs. It is set when either output becomes active and is cleared when all TCP interrupts have been cleared and no further interrupts are pending (i.e., both INTR and MFO are returned to their inactive state). This flag enables the TCP to be rapidly polled by the μP to determine the source of an interrupt in a wired—OR interrupt system.

Note that the Interrupt Status Flag will only monitor the state of the MFO output if it has been configured as an interrupt output (see Output Mode Register description). This is true, regardless of the state of the Interrupt Routing Register. Thus the Interrupt Status Flag provides a true reflection of all conditions routed to the external pins.

Status for the interrupts are provided by the Main Status Register and the Periodic Flag Register. Bits D1–D5 of the Main Status Register are the main interrupt bits.

These register bits will be set when their associated timing events occur. Enabled Alarm or Timer interrupts that occur will set its Main Status Register bit to a one. However, an external interrupt will only be generated if the appropriate Alarm or Timer interrupt enable bits are set (see *Figure 5*).

Disabling the periodic bits will mask the Main Status Register periodic bit, but not the Periodic Flag Register bits. The Power Fail Interrupt bit is set when the interrupt is enabled and a power fail event has occurred, and is not reset until the power is restored. If all interrupt enable bits are 0 no interrupt will be asserted. However, status still can be read from the Main Status Register in a polled fashion (see *Figure 5*).

To clear a flag in bits D2–D5 of the Main Status Register a 1 must be written back into the bit location that is to be cleared. For the Periodic Flag Register reading the status will reset all the periodic flags.

Functional Description (Continued)

Interrupts Fall Into Four Categories:

1. The Timer Interrupts: For description see Timer Section.
2. The Alarm Compare Interrupt: Issued when the value in the time compared RAM equals the counter.
3. The Periodic Interrupts: These are issued at every increment of the specific clock counter signal. Thus, an interrupt is issued every minute, second, etc. Each of these interrupts occurs at the roll-over of the specific counter.
4. The Power Fail Interrupt: Issued upon recognition of a power fail condition by the internal sensing logic. The power failed condition is determined by the signal on the $\overline{PFAIL}$ pin. The internal power fail signal is gated with the chip select signal to ensure that the power fail interrupt does not lock the chip out during a read or write.

ALARM COMPARE INTERRUPT DESCRIPTON

The alarm/time comparison interrupt is a special interrupt similar to an alarm clock wake up buzzer. This interrupt is generated when the clock time is equal to a value programmed into the alarm compare registers. Up to six bytes can be enabled to perform alarm time comparisons on the counter chain. These six bytes, or some subset thereof, would be loaded with the future time at which the interrupt will occur. Next, the appropriate bits in the Interrupt Control Register 1 are enabled or disabled (refer to detailed description of Interrupt Control Register 1). The TCP then compares these bytes with the clock time. When all the enabled compare registers equal the clock time an alarm interrupt is issued, but only if the alarm compare interrupt is enabled can the interrupt be generated externally. Each alarm compare bit in the Control Register will enable a specific byte for comparison to the clock. Disabling a compare byte is the same as setting its associated counter comparator to an "always equal" state. For example, to generate an interrupt at 3:15 AM of every day, load the hours compare with 0 3 (BCD), the minutes compare with 1 5 (BCD) and the faster counters with 0 0 (BCD), and then disable all other compare registers. So every day when the time rolls over from 3:14:59.99, an interrupt is issued. This bit may be reset by writing a one to bit D3 in the Main Status Register at any time after the alarm has been generated.

If time comparison for an individual byte counter is disabled, that corresponding RAM location can then be used as general purpose storage.

PERIODIC INTERRUPTS DESCRIPTION

The Periodic Flag Register contains six flags which are set by real-time generated "ticks" at various time intervals, see *Figure 5*. These flags constantly sense the periodic signals and may be used whether or not interrupts are enabled. These flags are cleared by any read or write operation performed on this register.

To generate periodic interrupts at the desired rate, the associated Periodic Interrupt Enable bit in Interrupt Control Register 0 must be set. Any combination of periodic interrupts may be enabled to operate simultaneously. Enabled periodic interrupts will now affect the Periodic Interrupt Flag in the Main Status Register. The Periodic Route bit in the Interrupt Routing Register is used to route the periodic interrupt events to either the INTR output or the MFO output.

When a periodic event occurs, the Periodic Interrupt Flag in the Main Status Register is set, causing an interrupt to be generated. The μP clears both flag and interrupt by writing a "1" to the Periodic Interrupt Flag. The individual flags in the periodic Interrupt Flag Register do not require clearing to cancel the interrupt.

If all periodic interrupts are disabled and a periodic interrupt is left pending (i.e., the Periodic Interrupt Flag is still set), the Periodic Interrupt Flag will still be required to be cleared to cancel the pending interrupt.

POWER FAIL INTERRUPTS DESCRIPTION

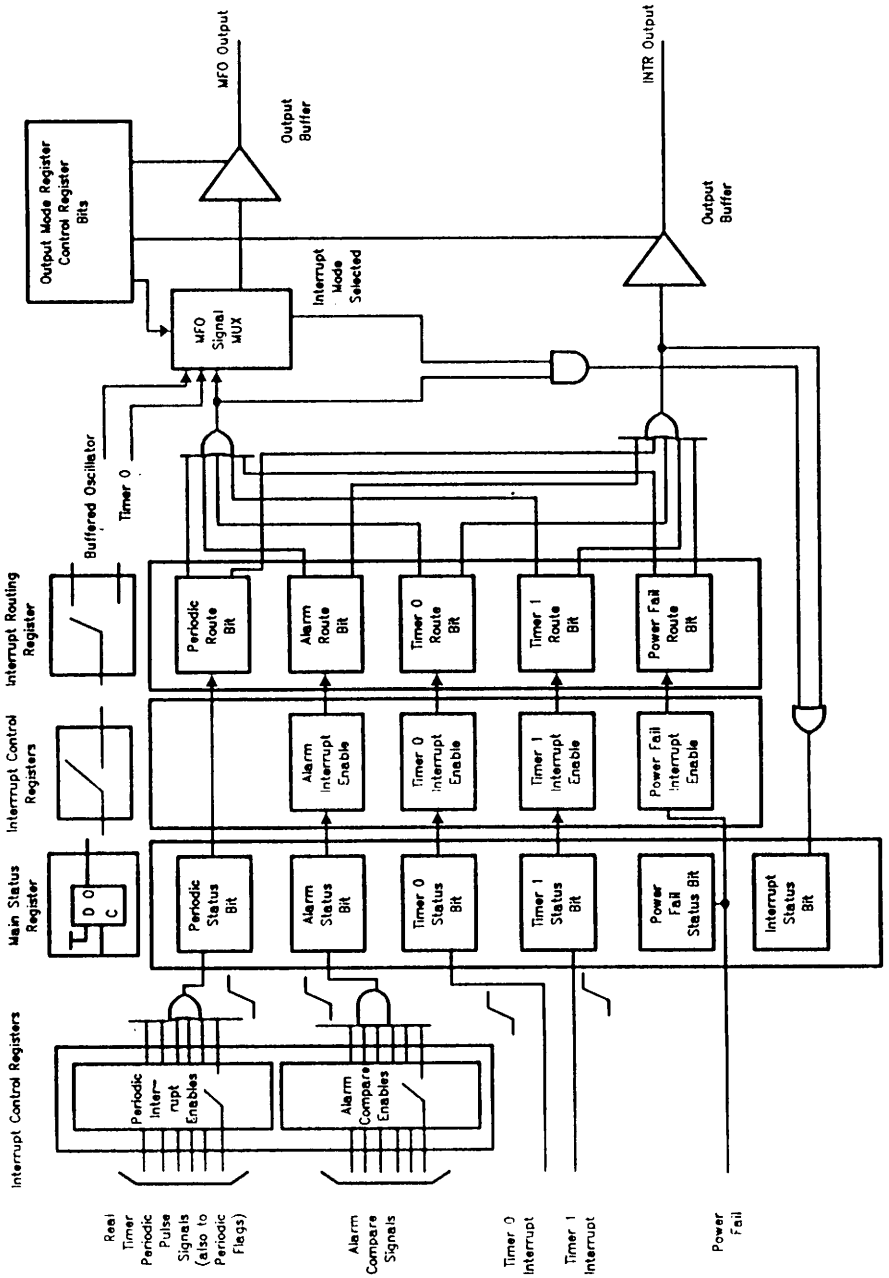
The Power Fail Status Flag in the Main Status Register monitors the state of the internal power fail signal. This flag may be interrogated by the μP, but it cannot be cleared; it is cleared automatically by the TCP when system power is restored. To generate an interrupt when the power fails, the Power Fail Interrupt Enable bit in Interrupt Control Register 1 is set.

The Power Fail Route bit determines which output the interrupt will appear on. Although this interrupt may not be cleared, it may be masked by clearing the Power Fail Interrupt Enable bit.

POWER FAILURE CIRCUITRY FUNCTIONAL DESCRIPTION

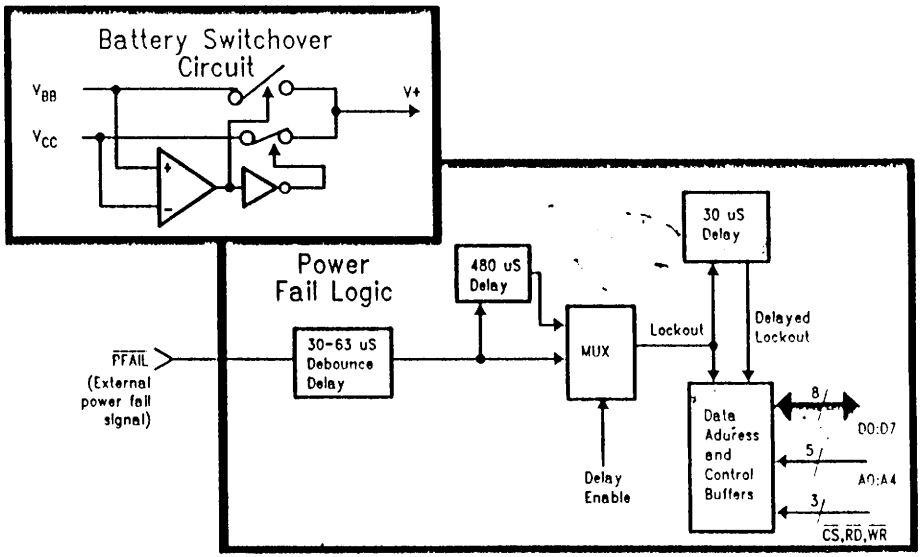
Since the clock must be operated from a battery when the main system supply has been turned off, the DP8570A provides circuitry to simplify design in battery backed systems. This circuitry switches over to the back up supply, and isolates the DP8570A from the host system. *Figure 6* shows a simplified block diagram of this circuitry, which consists of three major sections; 1) power loss logic; 2) battery switch over logic; and 3) isolation logic.

Detection of power loss occurs when $\overline{PFAIL}$ is low. Debounce logic provides a 30 μs–63 μs debounce time, which will prevent noise on the $\overline{PFAIL}$ pin from being interpreted as a system failure. After 30 μs–63 μs the debounce logic times out and a signal is generated indicating that system power is marginal and is failing. The Power Fail Interrupt will then be generated.



TL/F/8853-7

FIGURE 5. Interrupt Control Logic Overview



TL/F/8853-8

FIGURE 6. System-Battery Switchover (Upper Left), Power Fail and Lock-Out Circuits (Lower Right)

The user may choose to have this power failed signal lock-out the TCP's data bus within 30 μs min/63 μs max or to delay the lock-out to enable μP access after power failure is detected. This delay is enabled by setting the delay enable bit in the Routing Register. Also, if the lock-out delay was not enabled the TCP will disconnect itself from the bus within 30 μs min $\rightarrow$ 63 μs max. If chip select is low when a power failure is detected, a safety circuit will ensure that if a read or write is held active continuously for greater than 30 μs after the power fail signal is asserted, the lock-out will be forced. If a lock-out delay is enabled, the DP8570A will remain active for 480 μs after power fail is detected. This will enable the μP to perform last minute bookkeeping before total system collapse. When the host CPU is finished accessing the TCP it may force the bus lock-out before 480 μs has elapsed by resetting the delay enable bit.

The battery switch over circuitry is completely independent of the $\overline{PFAIL}$ pin. A separate circuit compares V_{CC} to the V_{BB} voltage. As the main supply fails, the TCP will continue to operate from the V_{CC} pin until V_{CC} falls below the V_{BB} voltage. At this time, the battery supply is switched in, V_{CC} is disconnected, and the device is now in the standby mode. If indeterminate operation of the battery switch over circuit is to be avoided, then the voltage at the V_{CC} pin must not be allowed to equal the voltage at the V_{BB} pin.

After the generation of a lock-out signal, and eventual switch in of the battery supply, the pins of the TCP will be configured as shown in Table II. Outputs that have a pull-up resistor should be connected to a voltage no greater than V_{BB}.

TABLE II. Pin Isolation during a Power Failure

Pin	$\overline{PFAIL}$ = Logic 0	Standby Mode V_{BB} > V_{CC}
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$	Locked Out	Locked Out
A0-A4	Locked Out	Locked Out
D0-D7	Locked Out	Locked Out
Oscillator	Not Isolated	Not Isolated
TCK, G0, G1	Not Isolated	Locked Out
$\overline{PFAIL}$	Not Isolated	Not Isolated
INTR, MFO T1	Not Isolated	Open Drain

The Timer and Interrupt Power Fail Operation bits in the Real-Time Mode Register determine whether or not the timers and interrupts will continue to function after a power fail event.

As power returns to the system, the battery switch over circuit will switch back to V_{CC} power as soon as it becomes greater than the battery voltage. The chip will remain in the locked out state as long as $\overline{PFAIL}$ = 0. When $\overline{PFAIL}$ = 1

Functional Description (Continued)

the chip is unlocked, but only after another 30 μs min → 63 μs max debounce time. The system designer must ensure that his system is stable when power has returned.

The power fail circuitry contains active linear circuitry that draws supply current from V_{CC}. In some cases this may be undesirable, so this circuit can be disabled by masking the power fail interrupt. The power fail input can perform all lock-out functions previously mentioned, except that no external interrupt will be issued. Note that the linear power fail circuitry is switched off automatically when using V_{BB} in standby mode.

LOW BATTERY, INITIAL POWER ON DETECT, AND POWER FAIL TIME SAVE

There are three other functions provided on the DP8570A to ease power supply control. These are an initial Power On detect circuit, which also can be used as a time keeping failure detect, a low battery detect circuit, and a time save on power failure.

On initial power up the Oscillator Fail Flag will be set to a one and the real time clock start bit reset to a zero. This indicates that an oscillator fail event has occurred, and time keeping has failed.

The Oscillator Fail flag will not be reset until the real-time clock is started. This allows the system to discriminate between an initial power-up and recovery from a power failure. If the battery backed mode is selected, then bit D6 of the Periodic Flag Register must be written low. This will not affect the contents of the Oscillator Fail Flag.

Another status bit is the low battery detect. This bit is set only when the clock is operating under the V_{CC} pin, and when the battery voltage is determined to be less than 2.1V (typical). When the power fail interrupt enable bit is low, it disables the power fail circuit and will also shut off the low battery voltage detection circuit as well.

To relieve CPU overhead for saving time upon power failure, the Time Save Enable bit is provided to do this automatically. (See also Reading the Clock: Latched Read.) The Time Save Enable bit, when set, causes the Time Save RAM to follow the contents of the clock. This bit can be reset by software, but if set before a power failure occurs, it will automatically be reset when the clock switches to the battery supply (not when a power failure is detected by the $\overline{PFAIL}$ pin). Thus, writing a one to the Time Save bit enables both a software write or power fail write.

SINGLE POWER SUPPLY APPLICATIONS

The DP8570A can be used in a single power supply application. To achieve this, the V_{BB} pin must be connected to ground, and the power connected to V_{CC}. The Oscillator Failed/Single Supply bit in the Periodic Flag Register should be set to a logic 1, which will disable the oscillator battery reference circuit. The power fail interrupt should also be disabled. This will turn off the linear power fail detection circuits, and will eliminate any quiescent power drawn through these circuits. Until the crystal select bits are initialized, the DP8570A may consume about 50 μA due to arbitrary oscillator selection at power on.

(This extra 50 μA is not consumed if the battery backed mode is selected).

TIMER FUNCTIONAL DESCRIPTION

The DP8570A contains 2 independent multi-mode timers. Each timer is composed of a 16-bit negative edge triggered binary down counter and associated control. The operation is similar to existing μP peripheral timers except that several features have been enhanced. The timers can operate in four modes, and in addition, the input clock frequency can be selected from a prescaler over a wide range of frequencies. Furthermore, these timers are capable of generating interrupts as well as hardware output signals, and both the interrupt and timer outputs are fully programmable active high, or low, open drain, or push-pull.

Figure 7 shows the functional block diagram of one of the timers. The timer consists of a 16-bit counter, two 8-bit input registers, two 8-bit output registers, clock prescaler, mode control logic, and output control logic. The timer and the data registers are organized as two bytes for each timer. Under normal operations a read/write to the timer locations will read or write to the data input register. The timer contents can be read by setting the counter Read bit (RD) in the timer control register.

TIMER INITIALIZATION

The timer's operation is controlled by a set of registers, as listed in Table III. These consist of 2 data input registers and one control register per timer. The data input registers contain the timers count down value. The Timer Control Register is used to set up the mode of operation and the input clock rate. The timer related interrupts can be controlled by programming the Interrupt Routing Register and Interrupt Control Register 0. The timer outputs are configured by the Output Mode Register.

TABLE III. Timer Associated Registers

Register Name	Register Select	Page Select	Address
Timer 0 Data MSB	X	0	10H
Timer 0 Data LSB	X	0	0FH
Timer 0 Control Register	0	0	01H
Timer 1 Data MSB	X	0	12H
Timer 1 Data LSB	X	0	11H
Timer 1 Control Register	0	0	02H
Interrupt Routing Register	0	0	04H
Interrupt Control Reg. 0	1	0	03H
Output Mode Register	1	0	02H

All these registers must be initialized prior to starting the timer(s). The Timer Control Register should first be set to select the timer mode with the timer start/$\overline{stop}$ bit reset. Then when the timer is to be started the control register should be rewritten identically but with the start/$\overline{stop}$ bit set.

TIMER OPERATION

Each timer is capable of operation in one of four modes. As mentioned, these modes are programmed in each timer's Control Register which is described later. All four modes operate in a similar manner. They operate on the two 8-bit data words stored into the Data Input Register. At the beginning of a counting cycle the 2 bytes are loaded into the timer and the timer commences counting down towards zero. The exact action taken when zero is reached depends on the

Functional Description (Continued)

INPUT CLOCK SELECTION

The input frequency to the timers may be selected. Each timer has a prescaler that gives a wide selection of clocking rates. In addition, the DP8570A has a single external clock input pin that can be selected for either of the timers. Table IV shows the range of programmable clocks available and the corresponding setting in the Timer Control Register.

TABLE IV. Programmable Timer Input Clocks

C2	C1	C0	Selected Clock
0	0	0	External
0	0	1	Crystal Oscillator
0	1	0	(Crystal Oscillator)/4
0	1	1	93.5 μs (10.7 kHz)
1	0	0	1 ms (1 kHz)
1	0	1	10 ms (100 Hz)
1	1	0	1/10 Second (10 Hz)
1	1	1	1 Second (1 Hz)

Note that the second and third selections are not fixed frequencies, but depend on the crystal oscillator frequency chosen.

Since the input clock frequencies are usually running asynchronously to the timer Start/$\overline{Stop}$ control bit, a 1 clock cycle error may result. This error results when the Start/Stop occurs just after the clock edge (max error). To minimize this error on all clocks an independent prescaler is used for each timer and is designed so that its Start/Stop error is less than 1 clock cycle.

The count hold/gate bit in the Timer Control Register and the external enable pins, G0/G1, can be used to suspend the timer operation in modes 0, 1, and 2 (in mode 3 it is the trigger input). The external pin and the register bit are OR'ed together, so that when either is high the timers are suspended. Suspending the timer causes the same synchronization error that starting the timer does. The range of errors specified in Table V.

TABLE V. Maximum Synchronization Errors

Clock Selected	Error
External	+ Ext. Clock Period
Crystal	+ 1 Crystal Clock Period
Crystal/4	+ 1 Crystal Clock Period
10.7 kHz	+ 32 μs
1 kHz	+ 32 μs
100 Hz	+ 32 μs
10 Hz	+ 32 μs
1 Hz	+ 32 μs

MODES OF OPERATION

Bits M0 and M1 in the Timer Control Registers are used to specify the modes of operation. The mode selection is described in Table VI.

TABLE VI. Programmable Timer Modes of Operation

M1	M0	Function	Modes
0	0	Single Pulse Generator	Mode 0
0	1	Rate Generator, Pulse Output	Mode 1
1	0	Square Wave Output	Mode 2
1	1	Retriggerable One Shot	Mode 3

MODE 0: SINGLE PULSE GENERATOR

When the timer is in this mode the output will be initially high if the Timer Start/$\overline{Stop}$ bit is low (stopped). When this mode is initiated the timer output will go high on the next falling edge of the prescaler's input clock, the contents

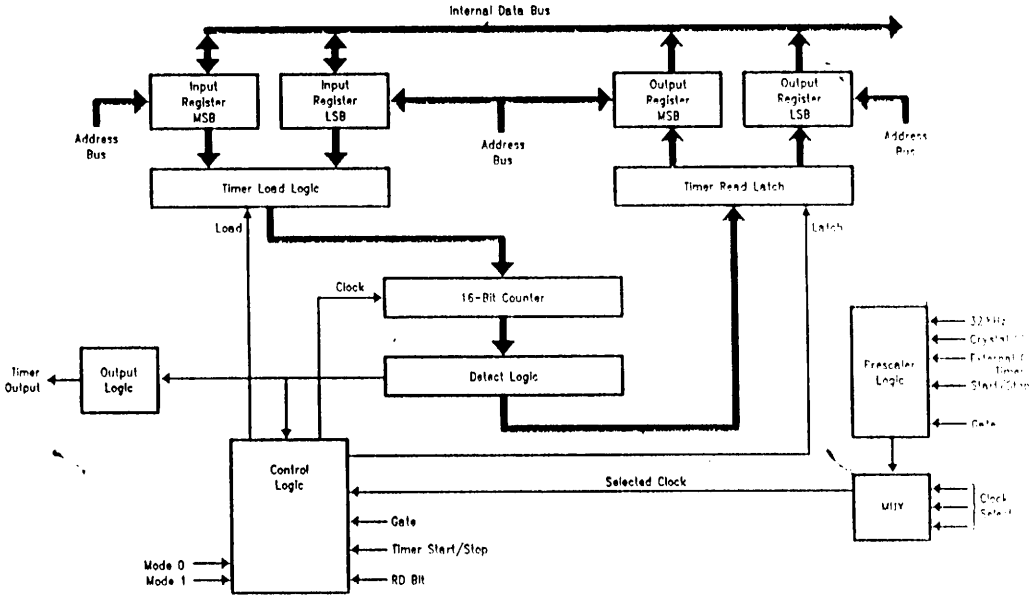


FIGURE 7. DP8570A Timer Block Diagram

Functional Description (Continued)

of the input data registers are loaded into the timer. The output will stay high until the counter reaches zero. At zero the output is reset. The result is an output pulse whose duration is equal to the input clock period times the count value (N) loaded into the input data register. This is shown in *Figure 8*.

Pulse Width = Clock Period × N

An interrupt is generated when the zero count is reached. This can be used for one-time interrupts that are set to occur a certain amount of time in the future. In this mode the Timer Start/$\overline{\text{Stop}}$ bit (TSS) is automatically reset upon zero detection. This removes the need to reset TSS before starting another operation.

The count down operation may be temporarily suspended either under software control by setting the Count Hold/Gate bit in the timer register high, or in hardware by setting the G0 or G1 pin high.

The above discussion assumes that the timer outputs were programmed to be non-inverting outputs (active high). If the polarity of the output waveform is wrong for the application the polarity can be reversed by configuring the Output Mode Register. The drive configuration can also be programmed to be push pull or open drain.

MODE 1: RATE GENERATOR

When operating in this mode the timer will operate continuously. Before the timer is started its output is low. When the timer is started the input data register contents are loaded into the counter on the negative clock edge and the output is set high (again assuming the Output Mode Register is programmed active high). The timer will then count down to zero. Once the zero count is reached the output goes low for one clock period of the timer clock. Then on the next clock the counter is reloaded automatically and the countdown repeats itself. The output, shown in *Figure 9*, is a waveform whose pulse width and period is determined by N, the input register value, and the input clock period:

Period = (N + 1) (Clock Period)

Pulse Width = Clock Period

The G0 or G1 pin and the count hold/gate bit can be used to suspend the appropriate timer countdown when either is high. Again, the output polarity is controllable as in mode 0. If enabled, an interrupt is generated whenever the zero count is reached. This can be used to generate a periodic interrupt.

MODE 2: SQUARE WAVE GENERATOR

This mode is also cyclic but in this case a square wave rather than a pulse is generated. The output square wave period is determined by the value loaded into the timer input register. This period and the duty cycle are:

Period = 2(N + 1) (Clock Period) Duty Cycle = 0.5

When the timer is stopped the output will be low, and when the Start/$\overline{\text{Stop}}$ bit is set high the timer's counter will be loaded on the next clock falling transition and the output will be set high.

The output will be toggled after the zero count is detected and the counter will then be reloaded, and the cycle will continue. Thus, every N + 1 counts the output gets toggled, as shown in *Figure 10*. Like the other modes the timer operation can be suspended either by software setting the count hold/gate bit (CHG) in the Timer Control Register or by using the gate pins. An interrupt will be generated every falling edge of the timer output, if enabled.

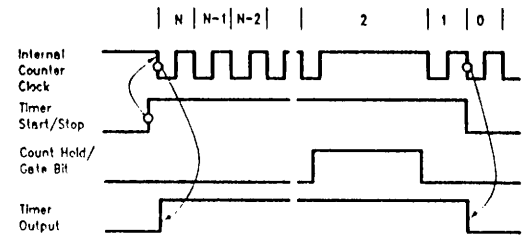


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FIGURE 8. Typical Waveforms for Timer Mode 0 (Timer Output Programmed Active High)

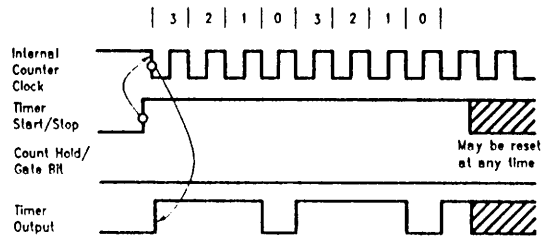

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FIGURE 9. Timing Waveforms for Timer Mode 1 (Timer Output Programmed Active High)

Functional Description (Continued)

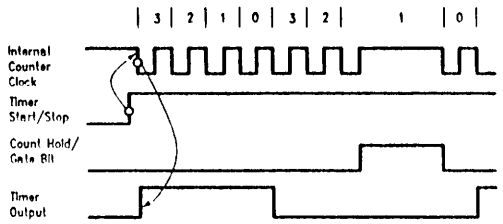

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FIGURE 10. Timing Waveforms for Timer Mode 2 (Timer Output Programmed Active High)

MODE 3: RETRIGGERABLE ONE SHOT

This mode is different from the previous three modes in that this is the only mode which uses the external gate to trigger the output. Once the timer Start/$\overline{\text{Stop}}$ bit is set the output stays inactive, and nothing happens until a positive transition is received on the G1 or G0 pins, or the Count Hold/Gate (CHG) bit is set in the timer control register. When a transition ocurs the one shot output is set active immediately; the counter is loaded with the value in the input register on the next transition of the input clock and the countdown begins. If a retrigger occurs, regardless of the current counter value, the counters will be reloaded with the value in the input register and the counter will be restarted without changing the output state. See *Figure 11*. A trigger count can occur at any time during the count cycle and can be a hardware or software signal (G0, G1 or CHG). In this mode the timer will output a single pulse whose width is determined by the value in the input data register (N) and the input clock period.

Pulse Width = Clock Period × N

Before entering mode 3, if a spurious edge has occurred on G0/G1 or the CHG bit is set to logic 1, then a pulse will appear at MFO or T1 or INTR output pin when the timer is started. To ensure this does not happen, do the following steps before entering mode 3: Configure the timer for mode 0, load a count of zero, then start the timer.

The timer will generate an interrupt only when it reaches a count of zero. This timer mode is useful for continuous "watch dog" timing, line frequency power failure detection etc.

READING THE TIMERS

Normally reading the timer data register addresses, (0FH and 10H for Timer 0 and 11H and 12H for Timer 1 will result in reading the input data register which contains the preset value for the timers. During timer operation it is often useful to read the contents of the 16-bit down counter. This reading may be an erroneous value of FFFFH.

To read a timer, the μP first sets the timer read bit in the appropriate Timer Control Register high. This will cause the counter's contents to be latched to 2-8 bit output registers and will enable these registers to be read if the μP reads the timer's input data register addresses. On reading the LSB byte the timer read bit is internally reset and subsequent reads of the timer locations will return the input register values.

DETAILED REGISTER DESCRIPTION

There are 5 external address bits: Thus, the host microprocessor has access to 32 locations at one time. An internal switching scheme provides a total of 67 locations.

This complete address space is organized into two pages. Page 0 contains two blocks of control registers, timers, real time clock counters, and special purpose RAM, while page 1 contains general purpose RAM. Using two blocks enables the 9 control registers to be mapped into 5 locations. The only register that does not get switched is the Main Status Register. It contains the page select bit and the register select bit as well as status information.

A memory map is shown in *Figure 2* and register addressing in Table VII. They show the name, address and page locations for the DP8570A.

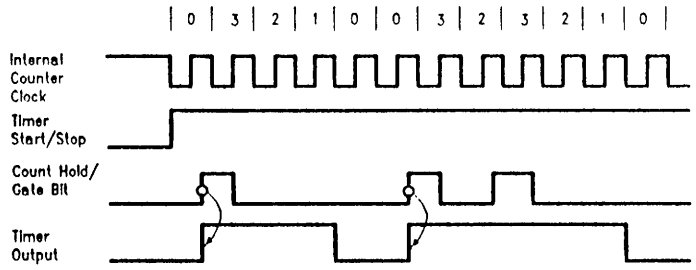

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FIGURE 11. Timing Waveforms for Timer Mode 3, Output Programmed Active High

Functional Description (Continued)

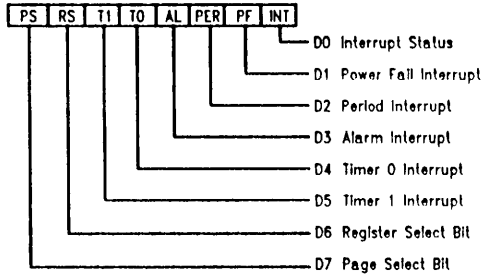
TABLE VII. Register/Counter/RAM Addressing for DP8570A

A0-4	PS (Note 1)	RS (Note 2)	Description	
CONTROL REGISTERS				
00	X	X	Main Status Register	
01	0	0	Timer 0 Control Register	
02	0	0	Timer 1 Control Register	
03	0	0	Periodic Flag Register	
04	0	0	Interrupt Routing Register	
01	0	1	Real Time Mode Register	
02	0	1	Output Mode Register	
03	0	1	Interrupt Control Register 0	
04	0	1	Interrupt Control Register 1	
COUNTERS (CLOCK CALENDAR)				
05	0	X	1/100, 1/10 Seconds	(0-99)
06	0	X	Seconds	(0-59)
07	0	X	Minutes	(0-59)
08	0	X	Hours	(1-12, 0-23)
09	0	X	Days of Month	(1-28/29/30/31)
0A	0	X	Months	(1-12)
0B	0	X	Years	(0-99)
0C	0	X	Julian Date (LSB)	(1-99)
0D	0	X	Julian Date	(0-3)
0E	0	X	Day of Week	(1-7)
TIMER DATA REGISTERS				
0F	0	X	Timer 0 LSB	
10	0	X	Timer 0 MSB	
11	0	X	Timer 1 LSB	
12	0	X	Timer 1 MSB	
TIMER COMPARE RAM				
13	0	X	Sec Compare RAM	(0-59)
14	0	X	Min Compare RAM	(0-59)
15	0	X	Hours Compare RAM	(1-12, 0-23)
16	0	X	DOM Compare RAM	(1-28/29/30/31)
17	0	X	Months Compare RAM	(1-12)
18	0	X	DOW Compare RAM	(1-7)
TIME SAVE RAM				
19	0	X	Seconds Time Save RAM	
1A	0	X	Minutes Time Save RAM	
1B	0	X	Hours Time Save RAM	
1C	0	X	Day of Month Time Save RAM	
1D	0	X	Months Time Save RAM	
1E	0	1	RAM	
1F	0	X	RAM/Test Mode Register	
01-1F	1	X	2nd Page General Purpose RAM	

1 PS—Page Select (Bit D7 of Main Status Register)
2 RS—Register Select (Bit D6 of Main Status Register)

4 0
80 01XX XXXX
81 0 0

MAIN STATUS REGISTER



TL/F/8638-14

The Main Status Register is always located at address 0 regardless of the register block or the page selected.

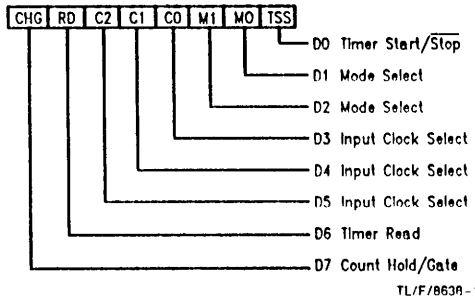
D0: This read only bit is a general interrupt status bit that is taken directly from the interrupt pins. The bit is a one when an interrupt is pending on either the INTR pin or the MFO pin (when configured as an interrupt). This is unlike D3-D5 which can be set by an internal event but may not cause an interrupt. This bit is reset when the interrupt status bits in the Main Status Register are cleared.

D1-D5: These five bits of the Main Status Register are the main interrupt status bits. Any bit may be a one when any of the interrupts are pending. Once an interrupt is asserted the μP will read this register to determine the cause. These interrupt status bits are not reset when read. Except for D1, to reset an interrupt a one is written back to the corresponding bit that is being tested. D1 is reset whenever the $\overline{PFAIL}$ pin = logic 1. This prevents loss of interrupt status when reading the register in a polled mode. D1, D3-D5 are set regardless of whether these interrupts are masked or not by bits D6 and D7 of Interrupt Control Registers 0 and 1.

D6 and D7: These bits are Read/Write bits that control which register block or RAM page is to be selected. Bit D6 controls the register block to be accessed (see memory map). The memory map of the clock is further divided into two memory pages. One page is the registers, clock and timers, and the second page contains 31 bytes of general purpose RAM. The page selection is determined by bit D7.

Functional Description (Continued)

TIMER 0 AND 1 CONTROL REGISTER



TL/F/8638-15

These registers control the operation of the timers. Each timer has its own register.

D0: This bit will Start (1) or Stop (0) the timer. When the timer is stopped the timer's prescaler and counter are reset, and the timer will restart from the beginning when started again. In mode 0 on time out the TSS bit is internally reset.

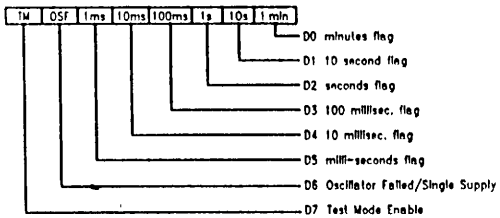
D1 and D2: These control the count mode of the timers. See Table VI.

D3-D5: These bits control which clock signal is applied to the timer's counter input. There is one external clock input pin (TCK) and either (or both) timer(s) can be selected to run off this pin: refer to Table IV for details.

D6: This is the read bit. If a one is written into this location it will cause the contents of the timer to be latched into a holding register, which can be read by the μP at any time. Reading the least significant byte of the timer will reset the RD bit. The timer read cycle can be aborted by writing RD to zero.

D7: The CHG bit has two mode dependent functions. In modes 0 through 2 writing a one to this bit will suspend the timer operation (without resetting the timer prescaler). However, in mode 3 this bit is used to trigger or re-trigger the count sequence as with the gate pins. If retriggering is desired using the CHG bit, it is not necessary to write a zero to this location prior to the re-trigger. The action of further writing a one to this bit will re-trigger the count.

PERIODIC FLAG REGISTER



TL/F/8638-16

The Periodic Flag Register has the same bit for bit correspondence as Interrupt Control Register 0 except for D6 and D7. For normal operation (i.e., not a single supply application) this register must be written to on initial power up or after an oscillator fail event. D0-D5 are read only bits, D6 and D7 are read/write.

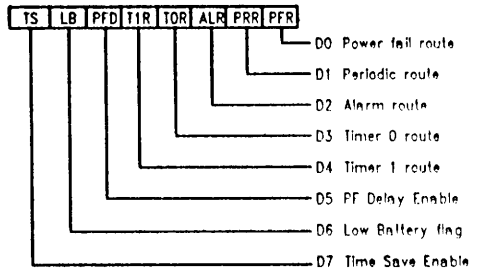
D0-D5: These bits are set by the real time rollover events (Time Change = 1). The bits are reset when the register is read and can be used as selective data change flags.

D6: This bit performs a dual function. When this bit is read, a one indicates that an oscillator failure has occurred and the time information may have been lost. This bit is automatically set on initial power-up or an oscillator fail event. The oscillator fail flag is reset by writing a one to the clock start/stop bit in the Real Time Mode Register, with the crystal oscillating.

When D6 is written to, it defines whether the TCP is being used in battery standby (normal) or in a single supply mode application. When set to a one this bit configures the TCP for single supply mode applications. This bit is automatically set on initial power-up or an oscillator fail event. This disables the oscillator reference circuit, and requires that V_{BB} is connected to ground, and the single supply mode connected to V_{CC}. When this bit is set to zero, the oscillator reference is enabled. This allows operation in standard battery standby application.

D7: Writing a one to this bit enables the test mode register at location 1F (see Table VII). This bit should be forced to zero during initialization for normal operation. If the test mode has been entered, clear the test mode register before leaving test mode. (See separate test mode application note for further details.)

INTERRUPT ROUTING REGISTER



TL/F/8638-17

D0-D4: The lower 5 bits of this register are associated with the main interrupt sources created by this chip. The purpose of this register is to route the interrupts to either the MFO (multi-function pin), or to the main interrupt pin. When any bit is set the associated interrupt signal will be sent to the MFO pin, and when zero it will be sent to the INTR pin.

Functional Description (Continued)

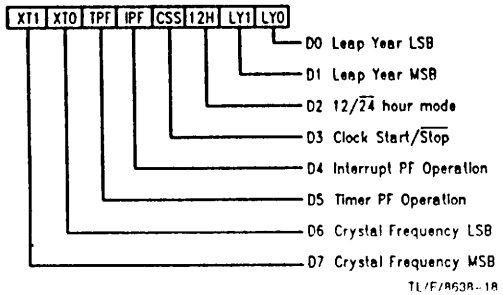
D5: The Delay Enable bit is used when a power fail occurs. If this bit is set, a 480 μs delay is generated internally before the μP interface is locked out. This will enable the μP to access the registers for up to 480 μs after it receives a power fail interrupt. After a power failure is detected but prior to the 480 μs delay timing out, the host μP may force immediate lock out by resetting the Delay Enable bit. Note if this bit is a 0 when power fails then after a delay of 30 μs min/63 μs max the μP cannot read the chip.

D6: This read only bit is set and reset by the voltage at the V_{BB} pin. It can be used by the μP to determine whether the battery voltage at the V_{BB} pin is getting too low. A comparator monitors the battery and when the voltage is lower than 2.1V (typical) this bit is set. The power fail interrupt must be enabled to check for a low battery voltage.

D7: Time Save Enable bit controls the loading of real-time-clock data into the Time Save RAM. When a one is written to this bit the Time Save RAM will follow the corresponding clock registers, and when a zero is written to this bit the time in the Time Save RAM is frozen. This eliminates any synchronization problems when reading the clock, thus negating the need to check for a counter rollover during a read cycle.

This bit must be set to a one prior to power failing to enable the Time Save feature. When the power fails this bit is automatically reset and the time is saved in the Time Save RAM.

REAL TIME MODE REGISTER



TL/F/8638-18

D0–D1: These are the leap year counter bits. These bits are written to set the number of years from the previous leap year. The leap year counter increments on December 31st and it internally enables the February 29th counter state. This method of setting the leap year allows leap year to occur whenever the user wishes to, thus providing flexibility in implementing Japanese leap year function.

LY1	LY0	Leap Year Counter
0	0	Leap Year Current Year
0	1	Leap Year Last Year
1	0	Leap Year 2 Years Ago
1	1	Leap Year 3 Years Ago

D2: The count mode for the hours counter can be set to either 24 hour mode or 12 hour mode with AM/PM indicator. A one will place the clock in 12 hour mode.

D3: This bit is the master Start/$\overline{\text{Stop}}$ bit for the clock. When a one is written to this bit the real time counter's prescaler and counter chain are enabled. When this bit is reset to zero the contents of the real time counter is stopped and the prescaler is cleared. When the TCP is initially powered up this bit will be held at a logic 0 until the oscillator starts functioning correctly after which this bit may be modified. If an oscillator fail event occurs, this bit will be reset to logic 0.

D4: This bit controls the operation of the interrupt output in standby mode. If set to a one it allows Alarm, Periodic, and Power Fail interrupts to be functional in standby mode. Timer interrupts will also be functional provided that bit D5 is also set. Note that the MFO and INTR pins are configured as open drain in standby mode.

If bit D4 is set to a zero then interrupt control register 0 and bits D6 and D7 of interrupt control register 1 will be reset when the TCP enters the standby mode. They will have to be re-configured when system (V_{CC}) power is restored.

D5: This bit controls the operation of the timers in standby mode. If set to a one the timers will continue to function when the TCP is in standby mode. The input pins TCK, G0, G1 are locked out in standby mode, and cannot be used.

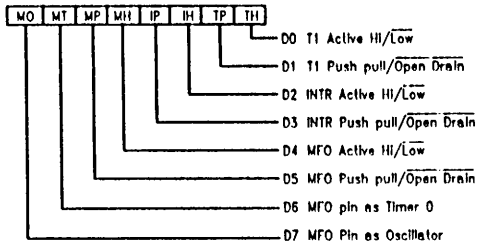
Therefore external control of the timers is not possible in standby mode. Note also that MFO and T1 pins are automatically reconfigured open drain during standby.

D6 and D7: These two bits select the crystal clock frequency as per the following table:

XT1	XT0	Crystal Frequency
0	0	32.768 kHz
0	1	4.194304 MHz
1	0	4.9152 MHz
1	1	32.000 kHz

All bits are Read/Write, and any mode written into this register can be determined by reading the register. On initial power up these bits are random.

OUTPUT MODE REGISTER



TL/F/8638-19

Functional Description (Continued)

D0: This bit, when set to a one makes the T1 (timer 1) output pin active high, and when set to a zero, it makes this pin active low.

D1: This bit controls whether the T1 pin is an open drain or push-pull output. A one indicates push pull.

D2: This bit, when set to a one makes the INTR output pin active high, and when set to a zero, it makes this pin active low.

D3: This bit controls whether the INTR pin is an open drain or push-pull output. A one indicates push-pull.

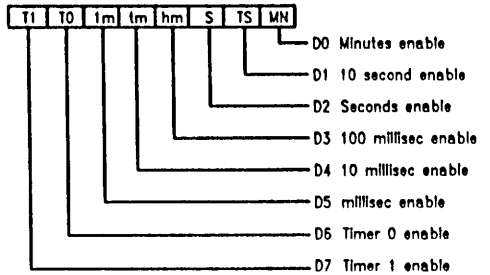
D4: This bit, when set to a one makes the MFO output pin active high, and when set to a zero, it makes this pin active low.

D5: This bit controls whether the MFO pin is an open drain or push-pull output. A one indicates push-pull.

D6 and D7: These bits are used to program the signal appearing at the MFO output, as follows:

D7	D6	MFO Output Signal
0	0	2nd Interrupt
0	1	Timer 0 Waveform
1	X	Buffered Crystal Oscillator

INTERRUPT CONTROL REGISTER 0

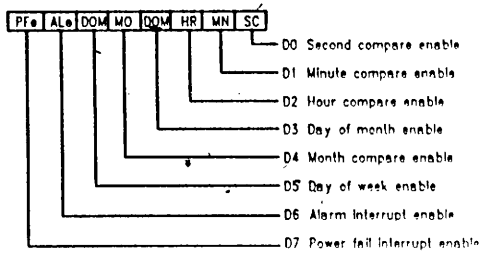


TL/F/8638-20

D0–D5: These bits are used to enable one of the selected periodic interrupts by writing a one into the appropriate bit. These interrupts are issued at the rollover of the clock. For example, the minutes interrupt will be issued whenever the minutes counter increments. In all likelihood the interrupt will be enabled asynchronously with the real time change. Therefore, the very first interrupt will occur in less than the periodic time chosen, but after the first interrupt all subsequent interrupts will be spaced correctly. These interrupts are useful when minute, second, real time reading, or task switching is required. When all six bits are written to a 0 this disables periodic interrupts from the Main Status Register and the interrupt pin.

D6 and D7: These are individual timer enable bits. A one written to these bits enable the timers to generate interrupts to the μP.

INTERRUPT CONTROL REGISTER 1



D0–D5: Each of these bits are enable bits which will enable a comparison between an individual clock counter and its associated compare RAM. If any bit is a zero then that clock-RAM comparator is set to the "always equal" state and the associated TIME COMPARE RAM byte can be used as general purpose RAM. However, to ensure that an alarm interrupt is not generated at bit D3 of the Main Status Register, all bits must be written to a logic zero.

D6: In order to generate an external alarm compare interrupt to the μP from bit D3 of the Main Status Register, this bit must be written to a logic 1.

D7: The MSB of this register is the enable bit for the Power Fail Interrupt. When this bit is set to a one an interrupt will be generated to the μP when $\overline{\text{PFAIL}} = 0$.

This bit also enables the low battery detection analog circuitry.

If the user wishes to mask the power fail interrupt, but utilize the analog circuitry, this bit should be enabled, and the Routing Register can be used to route the interrupt to the MFO pin. The MFO pin can then be left open or configured as the Timer 0 or buffered oscillator output.

Control and Status Register Address Bit Map

Main Status Register PS = 0 RS = 0 ADDRESS = 00H

D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R[1]	R[1]	R[1]	R[1]	R[2]	R[3]
Page Select	Register Select	Timer 1 Interrupt	Timer 0 Interrupt	Alarm Interrupt	Periodic Interrupt	Power Fail Interrupt	Interrupt Status

1. Reset by writing 1 to bit.
2. Set/reset by voltage at $\overline{PFAIL}$ pin.
3. Reset when all pending interrupts are removed

Timer 0 Control Register PS = 0 RS = 0 Address = 01H

Count Hold Gate	Timer Read	Input Clock Select C2	Input Clock Select C1	Input Clock Select C0	Mode Select M1	Mode Select M0	Timer Start/$\overline{Stop}$

All Bits R/W

Timer 1 Control Register PS = 0 RS = 0 Address = 02H

Count Hold Gate	Timer Read	Input Clock Select C2	Input Clock Select C1	Input Clock Select C0	Mode Select M1	Mode Select M0	Timer Start/$\overline{Stop}$

All Bits R/W

Periodic Flag Register PS = 0 RS = 0 Address = 03H

R/W	R/W[4]	R[5]	R[5]	R[5]	R[5]	R[5]	R[5]
Test Mode	Osc. Fail/ Single Supply	1 ms Flag	10 ms Flag	100 ms Flag	Seconds Flag	10 Second Flag	Minute Flag

4. Read Osc fa
Write 0 Batt-
Backed Mod
Write 1 Singl
Supply Mode
5. Reset by positive edge of read.

Interrupt Routing Register PS = 0 RS = 0 Address = 04H

R/W	R[6]	R/W	R/W	R/W	R/W	R/W	R/W
Time Save Enable	Low Battery Flag	Power Fail Delay Enable	Timer 1 Int. Route MFO/$\overline{INT}$	Timer 0 Int. Route MFO/$\overline{INT}$	Alarm Int. Route MFO/$\overline{INT}$	Periodic Int. Route MFO/$\overline{INT}$	Power Fail Int. Route MFO/$\overline{INT}$

6. Set and rese
by V_{BB}
voltage.

Real Time Mode Register PS = 0 RS = 1 Address = 01H

Crystal Freq. XT1	Crystal Freq. XT0	Timers EN on Back-Up	Interrupt EN on Back-Up	Clock Start/$\overline{Stop}$	12/$\overline{24}$ Hr. Mode	Leap Year MSB	Leap Year LSB

All Bits R/W

Output Mode Register PS = 0 RS = 1 Address = 02H

MFO as Crystal	MFO as Timer 0	MFO PP/$\overline{OD}$	MFO Active HI/$\overline{LO}$	INTR PP/$\overline{OD}$	INTR Active HI/$\overline{LO}$	T1 PP/$\overline{OD}$	T1 Active HI/$\overline{LO}$

All Bits R/W

Interrupt Control Register 0 PS = 0 RS = 1 Address = 03H

Timer 1 Interrupt Enable	Timer 0 Interrupt Enable	1 ms Interrupt Enable	10 ms Interrupt Enable	100 ms Interrupt Enable	Seconds Interrupt Enable	10 Second Interrupt Enable	Minute Interrupt Enable

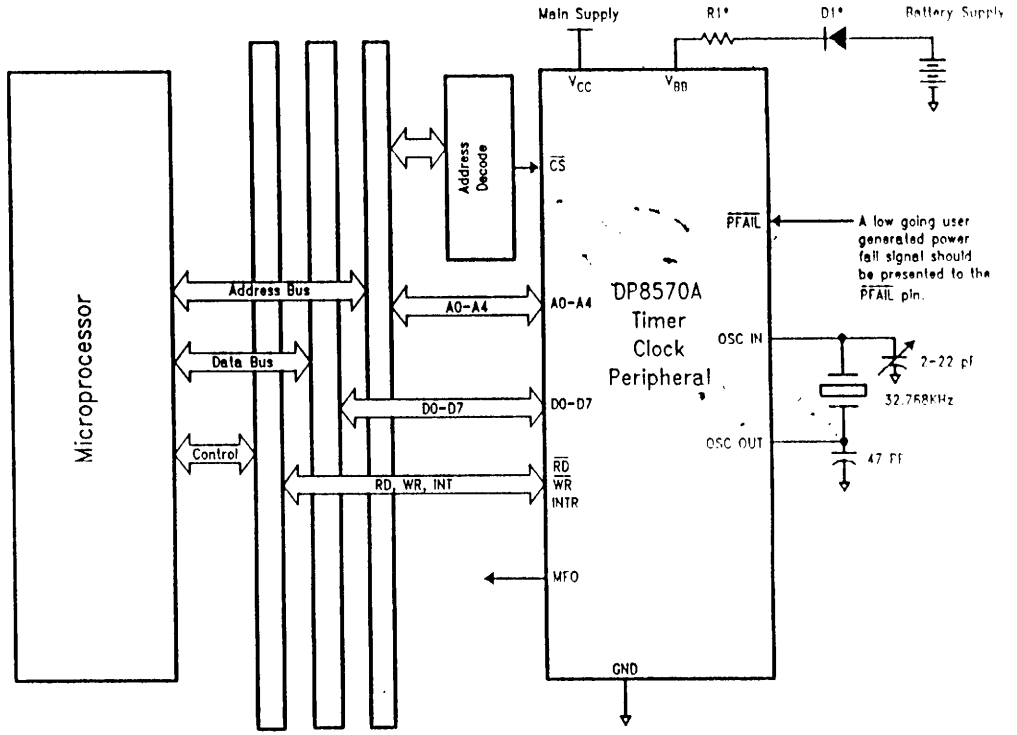
All Bits R/W

Interrupt Control Register 1 PS = 0 RS = 1 Address = 04H

Power Fail Interrupt Enable	Alarm Interrupt Enable	DOW Interrupt Enable	Month Interrupt Enable	DOM Interrupt Enable	Hours Interrupt Enable	Minute Interrupt Enable	Second Interrupt Enable

All Bits R/W

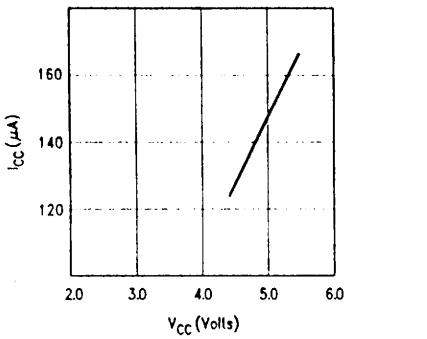
Typical Application



*These components may be necessary to meet UL requirements for lithium batteries. Consult battery manufacturer.

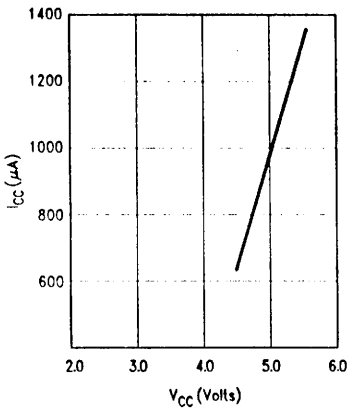
Typical Performance Characteristics

Operating Current vs Supply Voltage (Single Supply Mode Fosc = 32.768 kHz)



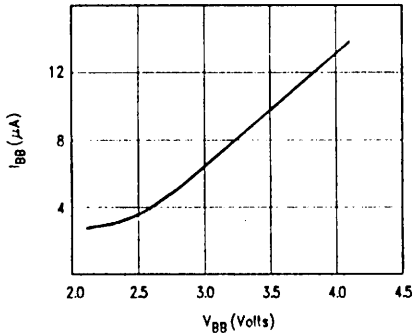
TL/F/8638–26

Operating Current vs Supply Voltage (Battery Backed Mode Fosc = 32.768 kHz)



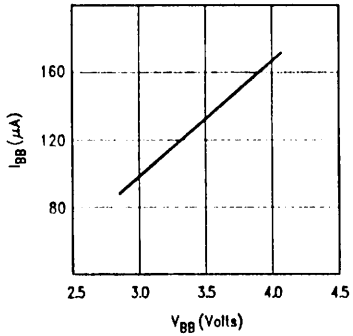
TL/F/8638–27

Standby Current vs Power Supply Voltage (Fosc = 32.768 kHz)



TL/F/8638–28

Standby Current vs Power Supply Voltage Fosc = 4.194304 MHz



TL/F/8638–29

PRELIMINARY

National Semiconductor

DP8571A Timer Clock Peripheral (TCP)

General Description

The DP8571A is intended for use in microprocessor based systems where information is required for multi-tasking, data logging or general time of day/date information. This device is implemented in low voltage silicon gate microCMOS technology to provide low standby power in battery back-up environments. The circuit's architecture is such that it looks like a contiguous block of memory or I/O ports. The address space is organized as 2 software selectable pages of 32 bytes. This includes the Control Registers, the Clock Counters, the Alarm Compare RAM, the Timers and their data RAM, and the Time Save RAM. Any of the RAM locations that are not being used for their intended purpose may be used as general purpose CMOS RAM.

Time and date are maintained from 1/100 of a second to year and leap year in a BCD format, 12 or 24 hour modes. Day of week, day of month and day of year counters are provided. Time is controlled by an on-chip crystal oscillator requiring only the addition of the crystal and two capacitors. The choice of crystal frequency is program selectable.

Two independent multifunction 10 MHz 16-bit timers are provided. These timers operate in four modes. Each has its own prescaler and can select any of 7 possible clock inputs. Thus, by programming the input clocks and the timer counter values a very wide range of timing durations can be achieved. The range is from about 400 ns (4.915 MHz oscillator) to 65,535 seconds (18 hrs., 12 min.).

Power failure logic and control functions have been integrated on chip. This logic is used by the TCP to issue a power fail interrupt, and lock out the μp interface. The time power fails may be logged into RAM automatically when V_{BB} V_{CC}. Additionally, two supply pins are provided, and upon power failure detection, internal circuitry will automatically switch from the main supply to the battery supply. Status bits are provided to indicate initial application of battery power, system power, and low battery detect. (Continued)

Features

- Full function real time clock/calendar
  - 12/24 hour mode timekeeping
  - Day of week and day of years counters
  - Four selectable oscillator frequencies
  - Parallel resonant oscillator
- Two 16-bit timers
  - 10 MHz external clock frequency
  - Programmable multi-function output
  - Flexible re-trigger facilities
- Power fail features
  - Internal power supply switch to external battery
  - Power Supply Bus glitch protection
  - Automatic log of time into RAM at power failure
- On-chip interrupt structure
  - Periodic, alarm, timer and power fail interrupts
- Up to 44 bytes of CMOS RAM
- INTR/MFO pins programmable High/Low and push-pull or open drain

Block Diagram

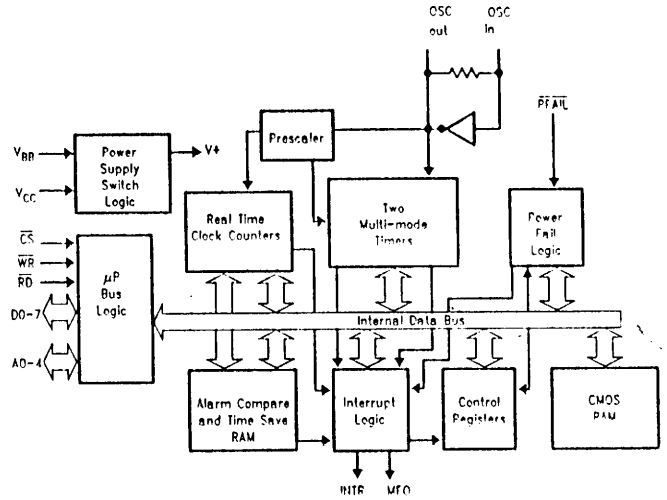


FIGURE 1

FUJITSU

POWER SUPPLY MONITOR

MB 3771

September 1986
Edition 1.0

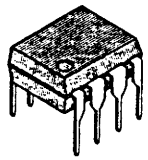
POWER SUPPLY MONITOR

The Fujitsu MB 3771 is designed to monitor the voltage level of one or two power supplies (+5V and an arbitrary voltage) in a microprocessor circuit, memory board in large-size computer, for example.

If the circuit's power supply deviates more than a specified amount, then the MB 3771 generates a reset signal to the microprocessor. Thus, the computer data is protected from accidental erasure.

Using the MB 3771 requires few external components. To monitor only a +5V supply, the MB 3771 requires the connection of one external capacitor. The level of an arbitrary dectection voltage is determined by two external resistors.

The MB 3771 is available in an 8-pin Dual In-Line, Signal In-Line Package or space saving Flat Package.



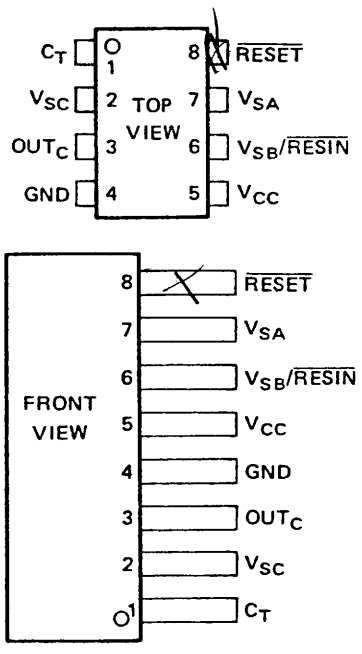
PLASTIC PACKAGE
DIP-08P-M01

PLASTIC PACKAGE
DIP-08P-M02

FPT-08P-M01: See page 20

- Precision voltage detection (V_{SA} = 4.1 to 4.3 V)
- User selectable threshold level with hysterisis ($V_{SB} \geqq 1.24$ V)
- Monitors the voltage of one or two power supplies (5 V and an arbitrary voltage, $\geqq 1.23$ V)
- Low voltage output for reset signal (V_{CC} = 0.8 V typ.)
- Minimal number of external components (one capacitor min.)
- Low power dissipation (I_{CC} = 0.35 mA typ., V_{CC} = 5 V)
- Available in a variety of packages
  - 8-pin Dual In-Line Package
  - 8-pin Single In-Line Package
  - 8-pin Flat Package

PIN ASSIGNMENT



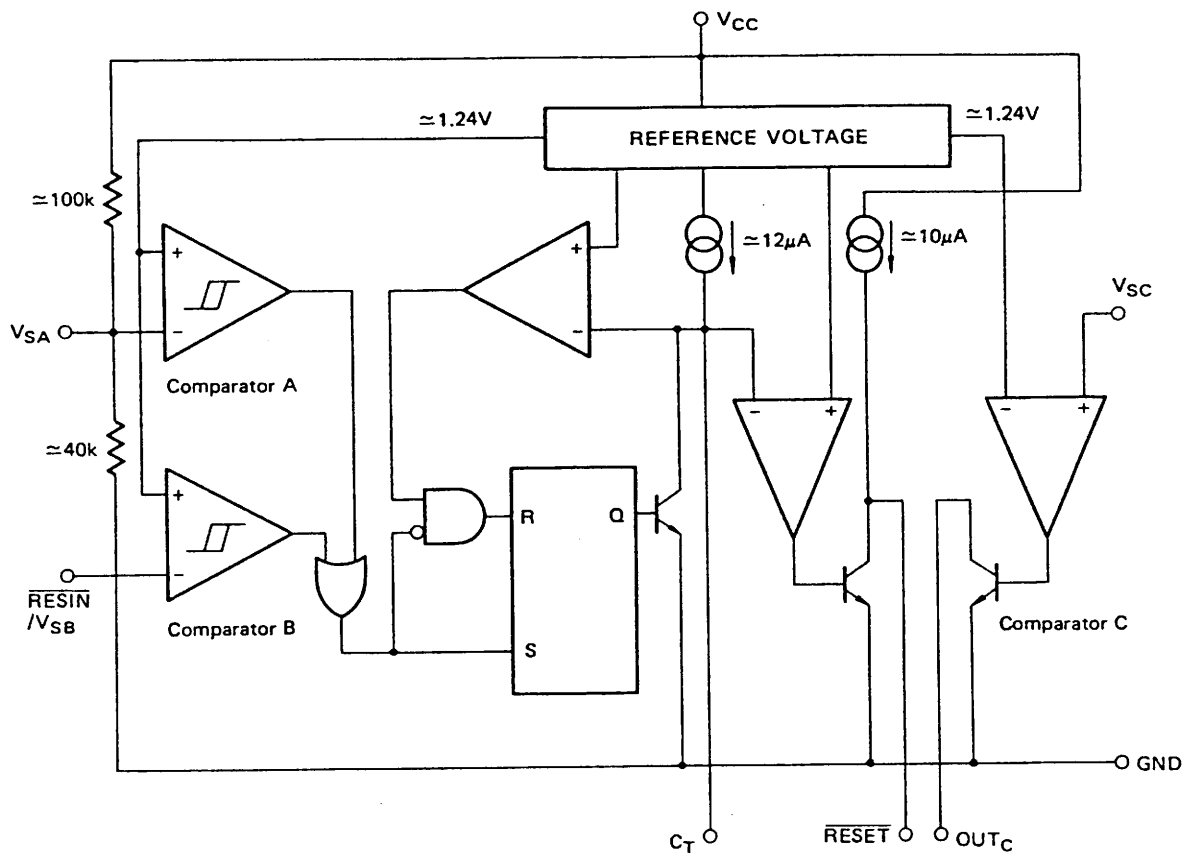
ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +20	V
Input Voltage A	V_{SA}	-0.3 to V_{CC}+0.3 (<+20)	V
Input Voltage B	V_{SB}	-0.3 to +20	V
Input Voltage C	V_{SC}	-0.3 to +20	V
Power Dissipation	P_D	200 ($T_A \leqq 85°C$)	mW
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM OF MB 3771



FUNCTIONAL EXPLANATIONS

Detection voltage inputs A and B are connected to the inverting input of Comparators A and B respectively. Both comparators have built-in hysterisis. If either V_{SA} or V_{SB} drops lower than about 1.23V, then $\overline{RESET}$ goes low.

Comparator B is used for the arbitrary preset voltage detection (See Example 3), or as forced reset input for TTL logic level input. (See Example 6)

Comparator C is designed as an open-collector output with inverted polarity input/output characteristics. Comparator C has no hysteresis. It can be used for over-voltage detection (See Example 11), generation of $\overline{RESET}$ signal by positive logic (See Example 7), and generation of reference voltage (See Example 10).

Note that V_{SB} and V_{SC} should be connected with V_{CC} and GND respectively. (See Example 1.)

The MB 3771 can detect about 2μs voltage sag/surge of the power supply. The user can add delayed trigger capacity by connecting a capacitor between inputs V_{SA} and V_{SB}. (See Example 8)

Internal pull-up resistor on the $\overline{RESET}$ line provides for high impedance loading (i.e. CMOS logic).

RECOMMENDED OPERATING CONDITIONS

parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+3.5 to +18	V
Output Current ($\overline{RESET}$)	I_{RESET}	0 to 20	mA
Output Current (OUT_C)	I_{OUTC}	0 to 6	mA
Operating Ambient Temperature	T_A	−40 to +85	°C

ELECTORICAL CHARACTERISTICS

DC Characteristics (V_{CC} = 5V, T_A = 25°C)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Supply Current	V_{SB} = 5V, V_{SC} = 0V	I_{CC1}		350	500	μA
	V_{SB} = 0V, V_{SC} = 0V	I_{CC2}		400	600	μA
Sagging Detection Voltage Falling	V_{CC}	V_{SAL}	4.10	4.20	4.30	V
	V_{CC}, T_A = −40 to +85°C		4.05	4.20	4.35	V
Rising	V_{CC}	V_{SAH}	4.20	4.30	4.40	V
	V_{CC}, T_A = −40 to +85°C		4.15	4.30	4.45	V
Hysterisis Width		V_{HYSA}	50	100	150	mV
Sagging Detection Voltage	V_{SB}	V_{SB}	1.212	1.230	1.248	V
	V_{SB}, T_A = −40 to +85°C		1.200	1.230	1.260	V
Deviation of Detection Voltage	V_{CC} = 3.5 to 18V	ΔV_{SB}		3	10	mV
Hysterisis Width		V_{HYSB}	14	28	42	mV
Input Current	V_{SB} = 5V	I_{IHB}		0	250	nA
	V_{SB} = 0V	I_{ILB}		20	250	nA
High-level Output Voltage	I_{RESET} = −5μA, V_{SB} = 5V	V_{OHR}	4.5	4.9		V
Output Saturation Voltage	I_{RESET} = 3mA, V_{SB} = 0V	V_{OLR}		0.28	0.4	V
	I_{RESET} = 10mA, V_{SB} = 0V			0.38	0.5	V
Output Sink Current	V_{OLR} = 1.0V, V_{SB} = 0V	I_{RESET}	20	40		mA
C_T Charge Current	V_{SB} = 5V, V_{CT} = 0.5V	I_{CT}	9	12	16	μA

ELECTORICAL CHARACTERISTICS (Cont'd)

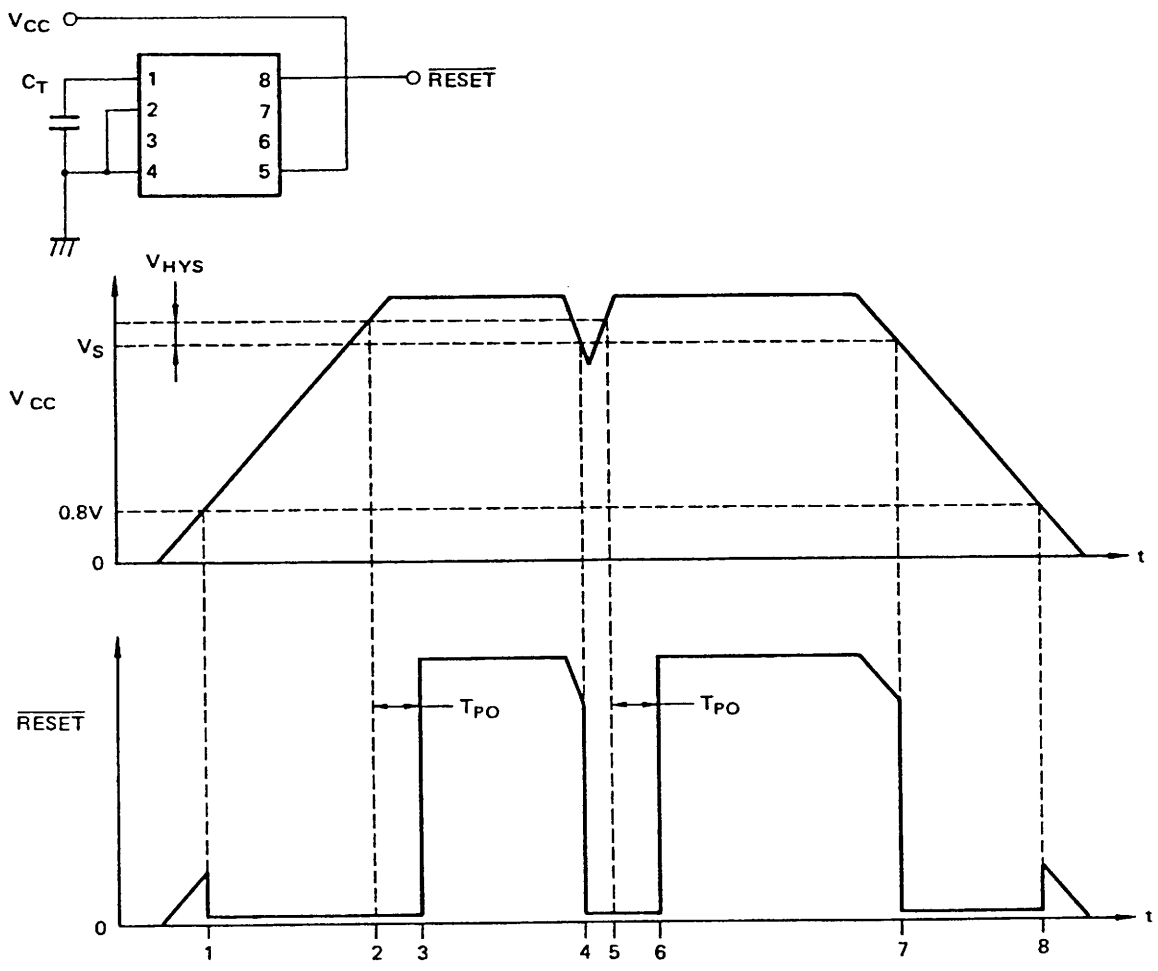
DC Characteristics (V_{CC} = 5V, T_A = 25°C)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Input Current	V_{SC} = 5V	I_{IHC}		0	500	nA
	V_{SC} = 0V	I_{ILC}		50	500	nA
Detection Voltage	V_{SC}	V_{SC}	1.225	1.245	1.265	V
	V_{SC}, T_A = −40 to +85°C		1.205	1.245	1.285	V
Deviation of Detection Voltage	V_{CC} = 3.5 to 18V	ΔV_{SC}		3	10	mV
Output Leakage Current	V_{OHC} = 18V	I_{OHC}		0	1	μA
Output Saturation Voltage	I_{OUTC} = 4mA, V_{SC} = 5V	V_{OLC}		0.15	0.4	V
Output Sink Current	V_{OLC} = 1.0V, V_{SC} = 5V	I_{OUTC}	6	15		mA
Reset Operation Minimum Supply Voltage	V_{OLR}=0.4V, I_{RESET}=200μA	V_{CCL}		0.8	1.2	V

AC Characteristics (V_{CC} = 5V, T_A = 25°C, C_T = 0.01μF)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Input Pulse Width	V_{SA}, V_{SB}	t_{PI}	5.0			μs
RESET Output Pulse Width		t_{PO}	0.5	1.0	1.5	ms
RESET Rising Time	R_L = 2.2kΩ, C_L = 100pF	t_R		1.0	1.5	μs
RESET Falling Time	R_L = 2.2kΩ, C_L = 100pF	t_F		0.1	0.5	μs
Propagation Delay Time	V_{SB}	t_{PD}		2	10	μs
	V_{SC}, R_L = 2.2kΩ, C_L = 100pF	t_{PHL}		0.5		μs
	V_{SC}, R_L = 2.2kΩ, C_L = 100pF	t_{PLH}		1.0		μs

FUNCTION EXPLANATION



Point 1: When V_{CC} rises to about 0.8V, $\overline{RESET}$ goes low.

Point 2: When V_{CC} reaches $V_S + V_{HYS}$, C_T then begins charging. $\overline{RESET}$ remains low during this time.

Point 3: $\overline{RESET}$ goes high when C_T begins charging.

$$T_{OP} \simeq C_T \times 10^5 \text{ [ms]}$$

Point 4: When V_{CC} level drops lower then V_S, then $\overline{RESET}$ goes low and C_T starts discharging.

Point 5: When V_{CC} level reaches $V_S + V_{HYS}$, then C_T starts charging.

In the case of voltage sagging, if the period from the time V_{CC} goes lower than or equal to V_S to the time V_{CC} reaches $V_S + V_{HYS}$ again, is longer than t_{P1}, (as speicified in the AC Characteristics), C_T is discharged and charged successively.

Point 6: After T_{PO} passes, and V_{CC} level exceeds $V_S + V_{HYS}$, then $\overline{RESET}$ goes high.

Point 7: Same as Point 4.

Point 8: $\overline{RESET}$ remains low until V_{CC} drops below 0.8V.

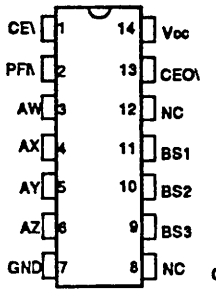
DALLAS SEMICONDUCTOR

DS1222
BankSwitch Chip

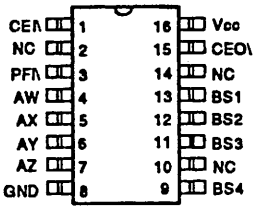
FEATURES

- Provides bank switching for 16 banks of memory
- Bank switching is software-controlled by a pattern recognition sequence on four address inputs
- Automatically sets all 16 banks off on power-up
- Bank switching logic allows only one bank on at a time
- Custom recognition patterns are available to prevent unauthorized access
- Full ± 10% operating range
- Low-power CMOS circuitry
- Can be used to expand the address range of microprocessors and decoders
- Optional 16-pin SOIC surface mount package

PIN DESCRIPTION



DS1222 14-Pin DIP (300 Mil.)



DS1222S16-Pin SOIC (300 Mil.)

PIN NAMES (\ Denotes Condition Low)

A_W-A_Z	Address Inputs
CE\	Chip Enable Input
CEO\	Chip Enable Output
NC	No Connection
BS1,BS2,	Bank Select Outputs
BS3,BS4	Bank Select Outputs
PFI\	Power Fail Input
V_{CC}	+5 Volts
GND	Ground

DESCRIPTION

The DS1222 BankSwitch Chip is a CMOS circuit designed to select one of sixteen memory banks under software control. Memory bank switching allows for an increase in memory capacity without additional address lines. Continuous blocks of memory are enabled by selecting the proper memory bank through a pattern recognition sequence on four address inputs. Custom patterns available from Dallas Semiconductor can provide security through uniqueness and prevent unauthorized access. By combining the DS1222 with the DS1212 Nonvolatile Controller x16 Chip, up to 16 banks of static RAMs can be selected.

OPERATION-BANK SWITCHING

Initially, on power-up all four bank select outputs are low and the chip enable output (CEO\) is held high. (Note: the power fail input [PFI\] must be low prior to power-up to assure proper initialization.) Bank switching is achieved by matching a predefined pattern stored within the DS1222 with a 16-bit sequence received on four address inputs. Prior to entering the 16-bit pattern, which sets the bank switch, a read cycle of 1111 on address inputs A_W through A_Z should be executed to guarantee that pattern entry starts with bit 0. Each set of address inputs is clocked into the DS1222 when CEI\ is driven low. All 16 inputs must be consecutive read cycles. The first eleven cycles must match the exact bit pattern as shown in Table 1. The last five cycles must match the exact bit pattern as shown for addresses A_X, A_Y, and A_Z. However, address line A_W defines the bank number to be enabled as per Table 2.

Switching to a selected bank of memory occurs on the rising edge of CEI\ when the last set of bits is input and a match has been established. After bank selection CEO\ always follows CEI\ with a maximum propagation delay of 15ns. The bank selected is determined by the levels set on Bank Select 1 through Bank Select 4 as per Table 2. These levels are held constant for all memory cycles until a new memory bank is selected.

	BIT SEQUENCE															
ADDRESS INPUTS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A_W	1	0	1	0	0	0	1	1	0	1	0	x	x	x	x	x
A_X	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A_Y	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A_Z	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X See Table 2

BANK SELECT CONTROL Table 2

Bank Selected	A_W Bit Sequence 11	12	13	14	15	Outputs BS1	BS2	BS3	BS4
*Banks Off	0	X	X	X	X	Low	Low	Low	Low
Bank 0	1	0	0	0	0	Low	Low	Low	Low
Bank 1	1	0	0	0	1	High	Low	Low	Low
Bank 2	1	0	0	1	0	Low	High	Low	Low
Bank 3	1	0	0	1	1	High	High	Low	Low
Bank 4	1	0	1	0	0	Low	Low	High	Low
Bank 5	1	0	1	0	1	High	Low	High	Low
Bank 6	1	0	1	1	0	Low	High	High	Low
Bank 7	1	0	1	1	1	High	High	High	Low
Bank 8	1	1	0	0	0	Low	Low	Low	High
Bank 9	1	1	0	0	1	High	Low	Low	High
Bank 10	1	1	0	1	0	Low	High	Low	High
Bank 11	1	1	0	1	1	High	High	Low	High
Bank 12	1	1	1	0	0	Low	Low	High	High
Bank 13	1	1	1	0	1	High	Low	High	High
Bank 14	1	1	1	1	0	Low	High	High	High
Bank 15	1	1	1	1	1	High	High	High	High

*CEO\ = V_{IH} independent of CE\

ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground -0.3V to +7.0V
Operating Temperature 0°C to 70°C
Storage Temperature -55°C to +125°C

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Logic 1	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V +/- 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	uA	
I/O Leakage Current	I_{LO}	-1.0		+1.0	uA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	2
Output Current @ 0.4V	I_{OL}			+4.0	mA	2
Operating Current	I_{CC}			15	mA	

CAPACITANCE

(t_A=25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5	10	pF	
Input/Output Capacitance	$C_{I/O}$		5	10	pF	

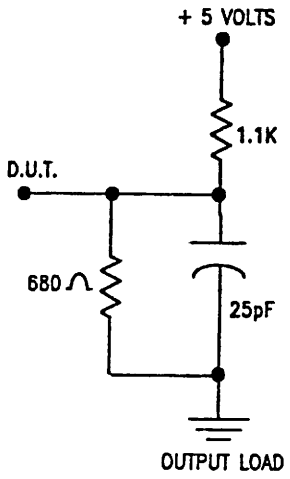
AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC}=5V+/- 10%)

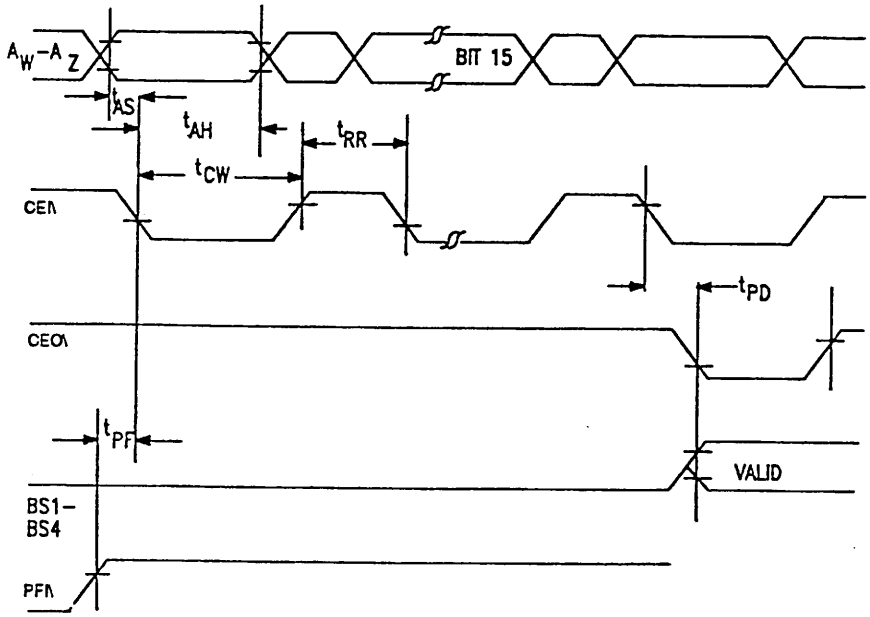
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Address Setup	t_{AS}	5			ns	
Address Hold	t_{AH}	50			ns	
Read Recovery	t_{RR}	40			ns	
Propagation Delay	t_{PD}			15	ns	2
Power Fail Input to First CE\	t_{PF}	50			ns	
Chip Enable Low	t_{CW}	110			ns	

NOTES: 1. All voltages are referenced to ground.
2. Measured with a load as shown in Figure 1.

OUTPUT LOAD FIGURE 1



TIMING DIAGRAM-ACCESS TO BANK SWITCH



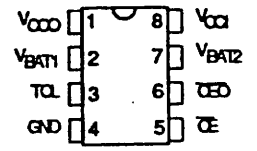
DALLAS SEMICONDUCTOR

DS1210
Nonvolatile Controller Chip

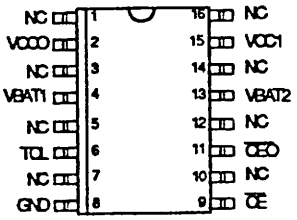
FEATURES

- Converts CMOS RAMs into nonvolatile memories
- Unconditionally write protects when V_{CC} Is out of tolerance
- Automatically switches to battery when power fail occurs
- Space saving 8-pin DIP
- Consumes less than 100 nA of battery current
- Tests battery condition on power up
- Provides for redundant batteries
- Optional 5% or 10% power fail detection
- Low forward voltage drop on the V_{CC} switch
- Optional 16-pin SOIC surface mount package

PIN DESCRIPTION



DS1210 8-Pin DIP
(300 Mil.)



DS1210S 16-Pin SOIC
(300 Mil.)

PIN NAMES (\ Denotes Condition Low)

VCCO	RAM Supply
VBAT1	+ Battery 1
TOL	Power Supply Tolerance
GND	Ground
CE\	Chip Enable Input
CEO\	Chip Enable Output
VBAT2	+ Battery 2
VCCI	+ Supply
NC	No Connect

DESCRIPTION

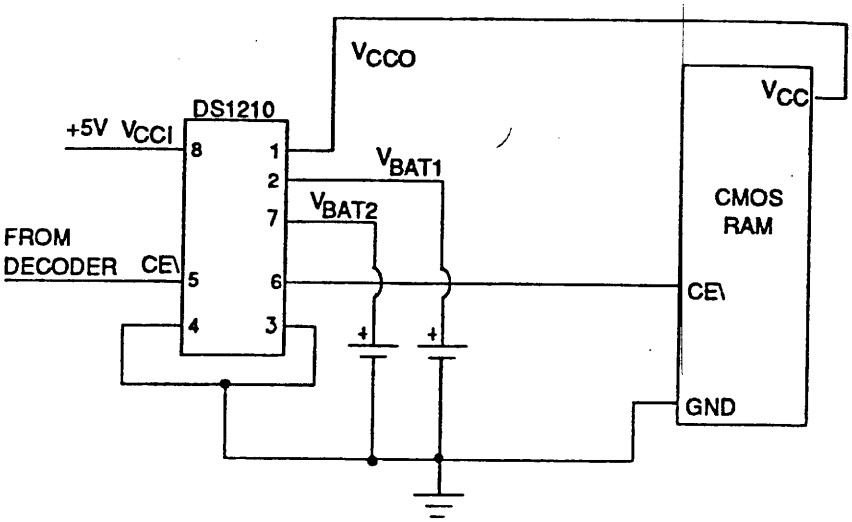
The DS1210 Nonvolatile Controller Chip is a CMOS circuit which solves the application problem of converting CMOS RAM into nonvolatile memory. Incoming power is monitored for an out- of-tolerance condition. When such a condition is detected, chip enable is inhibited to accomplish write protection and the battery is switched on to supply the RAM with uninterrupted power. Special circuitry uses a low-leakage CMOS process which affords precise voltage detection at extremely low battery consumption. The 8-pin DIP package keeps PC board real estate requirements to a minimum. By combining the DS1210 Nonvolatile Controller Chip with a CMOS memory and batteries, nonvolatile RAM operation can be achieved.

OPERATION

The DS1210 nonvolatile controller performs five circuit functions required to battery back up a RAM. First, a switch is provided to direct power from the battery or the incoming supply (V_{CCI}) depending on which is greater. This switch has a voltage drop of less than 0.3V. The second function which the nonvolatile controller provides is power fail detection. The DS1210 constantly monitors the incoming supply. When the supply goes out of tolerance a precision comparator detects power fail and inhibits chip enable (CEO\). The third function of write protection is accomplished by holding the CEO\ output signal to within 0.2 volts of the V_{CCI} or battery supply. If CE\ input is low at the time power fail detection occurs, the CEO\ output is kept in its present state until CE\ is returned high. The delay of write protection until the current memory cycle is completed prevents the corruption of data. Power fail detection occurs in the range of 4.75 volts to 4.5 volts with the tolerance Pin 3 grounded. If Pin 3 in connected to V_{CCO}, then power fail detection occurs in the range of 4.5 volts to 4.25 volts. During nominal supply conditions CEO\ will follow CE\ with a maximum propagation delay of 20ns. The fourth function the DS1210 performs is a battery status warning so that potential data loss is avoided. Each time that the circuit is powered up the battery voltage is checked with a precision comparator. If the battery voltage is less than 2.0 volts, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, verifying that memory location content. A subsequent write cycle can then be executed to the same memory location altering the data. If the next read cycle fails to verify the written data, then the batteries are less than 2.0V and data is in danger of being corrupted. The fifth function of the nonvolatile controller provides for battery redundancy. In many applications, data integrity is paramount. In these applications it is often desirable to use two batteries to ensure reliability. The DS1210 controller provides an internal isolation switch which allows the connection of two batteries. During battery backup operation the battery with the highest voltage is selected for use. If one battery should fail, the other will take over the load. The switch to a redundant battery is transparent to circuit operation and to the user. A battery status warning will occur when the battery in use falls below 2.0 volts. A grounded V_{BAT2} pin will not activate a battery fail warning. In applications where battery redundancy is not required, a single battery should be connected to the BAT1 pin. The BAT2 battery pin must be grounded. The nonvolatile controller contains circuitry to turn off the battery back-up. This is to maintain the battery(s) at its highest capacity until the equipment is powered up and valid data is written to the SRAM. While in the freshness seal mode the CEO\ and V_{CCO} will be forced to V_{OL}. When the batteries are first attached to one or both of the V_{BAT} pins, V_{CCO} will not provide battery back-up until V_{CCI} exceeds V_{CCTP}, as set by the T_{OL} pin, and then falls below V_{BAT}.

Figure 1 shows a typical application incorporating the DS1210 in a microprocessor-based system. Section A shows the connections necessary to write protect the RAM when V_{CC} is less than 4.75 volts and to back up the supply with batteries. Section B shows the use of the DS1210 to halt the processor when V_{CC} is less than 4.75 volts and to delay its restart on power-up to prevent spurious writes.

SECTION A - BATTERY BACKUP Figure 1

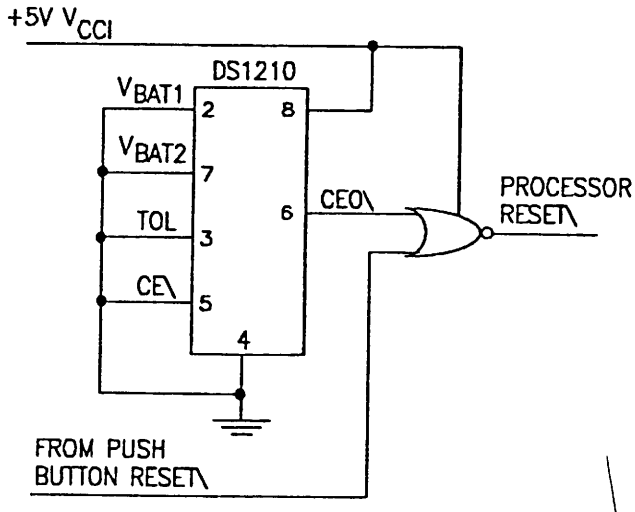


BATTERY BACKUP CURRENT DRAIN EXAMPLE

CONSUMPTION

DS1210 I_{BAT}	100 nA
RAM I_{CCO2}	10 uA
Total Drain	10.1 uA

SECTION B - PROCESOR RESET



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 3 = GND Supply Voltage	V_{CCI}	4.75	5.0	5.5	V	1
Pin 3 = V_{CCO} Supply Voltage	V_{CCI}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.2		V_{CC}+0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1
Battery Input	V_{BAT1}, V_{BAT2}	2.0		4.0	V	1,2

(0°C to 70°C, V_{CCI} = 4.75V to 5.5V, Pin 3 = GND)

DC ELECTRICAL CHARACTERISTICS

(V_{CCI} = 4.5 to 5.5V, Pin 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current	I_{CCI}			5	mA	3
Supply Voltage	V_{CCO}	V_{CC} -0.2			V	1
Supply Current	I_{CCO1}			80	mA	4
Input Leakage	I_{IL}	-1.0		+1.0	uA	
Output Leakage	I_{LO}	-1.0		+1.0	uA	
CEO\ Output @2.4V	I_{OH}	-1.0			mA	5
CEO\ Output @0.4V	I_{OL}			4.0	mA	5
V_{CC} Trip Point (TOL=GND)	V_{CCTP}	4.50	4.62	4.74	V	1
V_{CC} Trip Point (TOL=V_{CC})	V_{CCTP}	4.25	4.37	4.49	V	1

(0°C to 70°C, V_{CCI} = < V_{BAT})

CEO\ Output	V_{OHL}	V_{BAT} - 0.2			V	
V_{BAT1} or V_{BAT2} Battery Current	I_{BAT}			100	nA	2,3
Battery Backup Current @ V_{cco} = V_{BAT} - 0.3V	I_{CCO2}			50	uA	6,7

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	
Output Capacitance	C_{OUT}			7	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CCI} = 4.75V to 5.5V, Pin 3 = GND)
(V_{CCI} = 4.5 to 5.5V, Pin3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
CE\ Propagation Delay	t_{PD}	5	10	20	ns	5
CE\ High to Power Fail	t_{PF}			0	ns	

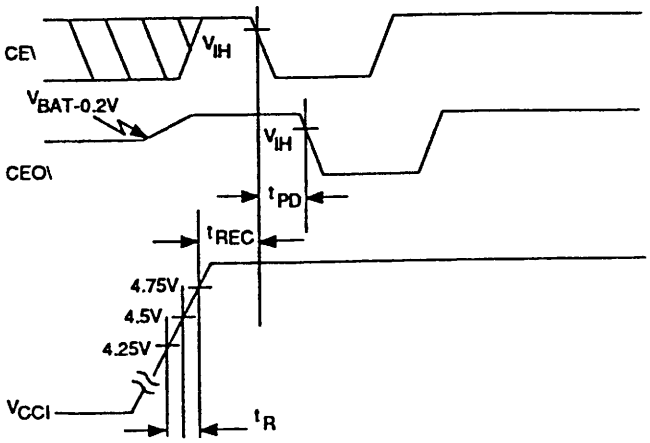
(0°C to 70°C, V_{CCI} <4.75V , Pin 3 = GND)
(V_{CCI} < 4.5 , Pin 3 = V_{CCO})

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Recovery at Power Up	t_{REC}	2	80	125	ms	
V_{CC} Slew Rate Power Down	t_F	300			us	
V_{CC} Slew Rate Power Down	t_{FB}	10			us	
V_{CC} Slew Rate Power Up	t_R	0			us	
CE\ Pulse Width	t_{CE}			1.5	us	7,8

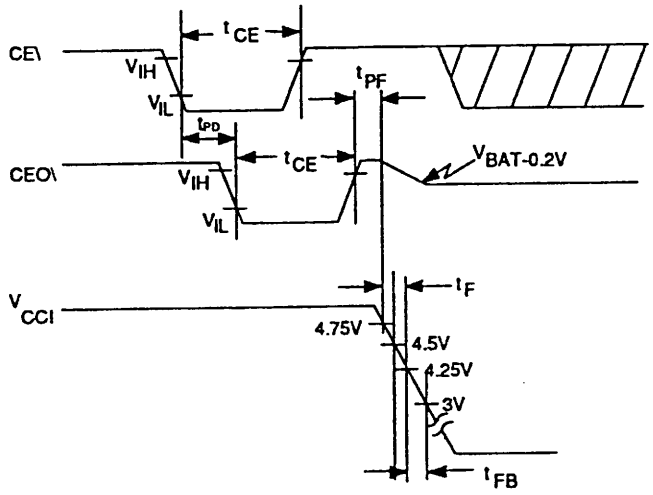
NOTES

1. All voltages are referenced to ground.
2. Only one battery input is required.
3. Measured with V_{CCO} and CEO\ open.
4. I_{CCO1} is the maximum average load which the DS1210 can supply to the memories.
5. Measured with a load as shown in Figure 2.
6. I_{CCO2} is the maximum average load current which the DS1210 can supply to the memories in the battery backup mode.
7. t_{CE} max. must be met to ensure data integrity on power loss.
8. CEO\ can only sustain leakage current in the battery backup mode.

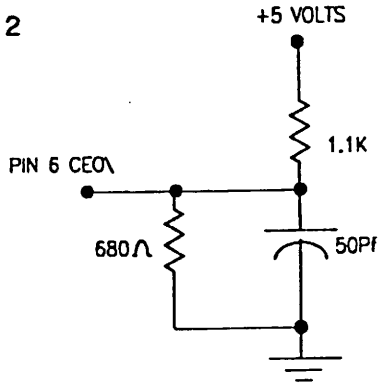
TIMING DIAGRAM - POWER UP



TIMING DIAGRAM - POWER DOWN



OUTPUT LOAD Figure 2



```
module ipcp16adrdec
flag '-r0';
title 'ipccpu ip16 addr decode
ap 1990  31 aug'
ip16p    device 'P22V10';
a19,a18,a17,a16,a15,a13,a12,mpo,usr,men,rdn,wrn
                                pin 1,2,3,4,5,6,7,8,9,10,11,13;
nwrb,nrdb,nwrc,nrdc,ne2wr,nepcs,nra0cs,nra1cs,ne2cs,nbscs
                                pin 14,15,16,17,18,19,20,21,22,23;
c,x,z = .C.,.X.,.Z.;

equations


!nbscs  = !rdn & !men & a19 & a18 & a17 & !a16 & !a15 & !a13 & !a12
        # !wrn & !men & a19 & a18 & a17 & !a16 & !a15 & !a13 & !a12;

!ne2cs  = !rdn& !men& a19& a18& !a17& !a16& !a15
        # !wrn& !men& a19& a18& !a17& !a16& !a15& !a13&  a12
        # !wrn& !men& a19& a18& !a17& !a16& !a15&  a13& !a12
        # !wrn& !men& a19& a18& !a17& !a16& !a15&  a13&  a12
        # !wrn& !men& a19& a18& !a17& !a16& !a15& !a13& !a12& !usr
        # !rdn& !men&!a19&!a18& !a17& !a16& !a15&  mpo& !usr;

!nra1cs = !men & !a19 & a18 & a17 & !a16
        # !men & !a19 & a18 & a17 &  a16;

!nra0cs = !men & !a19 & a18 & !a17 & !a16
        # !men & !a19 & a18 & !a17 &  a16;

!nepcs  = !men & !rdn & !a19 & !a18 &  a17 & !a16
        # !men & !rdn & !a19 & !a18 & !a17 & !a16 & mpo & usr;

!ne2wr  = !wrn & !men & a19 & a18 & !a17 & !a16 & !a15 & !a13 &  a12
        # !wrn & !men & a19 & a18 & !a17 & !a16 & !a15 &  a13 & !a12
        # !wrn & !men & a19 & a18 & !a17 & !a16 & !a15 &  a13 &  a12
        # !wrn& !men& a19& a18& !a17& !a16& !a15& !a13& !a12 & !usr;


!nrdc   = !men & !rdn & !a19 & !a18 & !a17
        # !men & !rdn & !a19 & !a18 &  a17 & !a16
        # !men & !rdn & !a19 &  a18 & !a17
        # !men & !rdn & !a19 &  a18 &  a17
```

```
        # !men & !rdn &  a19 & !a18 & !a17
        # !men & !rdn &  a19 & !a18 &  a17
        # !men & !rdn &  a19 &  a18 & !a16;

!nwrc   = !men & !wrn & !a19 &  a18
        # !men & !wrn &  a19 & !a18;

!nrdb   = !men & !rdn & !a19 & !a18 & a17 & a16;

!nwrb   = !men & !wrn & !a19 & !a18 & a17 & a16;


end ipcp16adrdec;
```

```
module ipcp17ioadr
flag '-r0';
title 'ipccpu ip17 io addr decode
ap 1990  03 sep'
ip17p    device 'P22V10';
a15,a9,a8,a7,a6,a5,a4,a3,a2,ioen,rdn,wrn,nrdb
                                pin 1,2,3,4,5,6,7,8,9,10,11,13,23;
niowb,niorb,niowu,nioru,ndbdir,nsrcs,nmrcs,ngprcs,nurcs
                                pin 14,15,16,17,18,19,20,21,22;
c,x,z = .C.,.X.,.Z.;

equations


!nurcs  = !ioen & !a15 & !a9 & !a8 & a7 & !a6 & !a5;

!ngprcs = !ioen& !wrn& !a15& !a9& !a8& a7& !a6& a5& !a4& !a3 & !a2;

!nmrcs  = !ioen& !wrn& !a15& !a9& !a8& a7& a6& !a5& !a4& !a3& !a2;

!nsrcs  = !ioen& !wrn& !a15& !a9& !a8& a7& a6&  a5& !a4& !a3& !a2;

!ndbdir = !ioen & !rdn & a15   #   !nrdb;

!nioru  = !ioen & !rdn & !a15 & !a9 & !a8 & a7 & !a6 & !a5;

!niowu  = !ioen & !wrn & !a15 & !a9 & !a8 & a7 & !a6 & !a5;

!niorb  = !ioen & !rdn &  a15;

!niowb  = !ioen & !wrn &  a15;

end ipcp17ioadr;
```

Name	Type	Pos
B1	Lith. batt. B-400	H2
C1	Cap.1uF/40V Sol.Al	D9
C2	Cap. 100nF ker.	C9
C3	Cap. 100nF ker.	C9
C4	Cap.10uF/16V Sol.Al	G11
C5	Cap. 33pF ker. P150	F11
C6	Cap. 2-22pF trim	F10
C7	Cap.10uF/16V Sol.Al	D4
C8	Cap.10uF/16V Sol.Al	H11
C9	Cap.10uF/16V Sol.Al	H11
C10	Cap. 22pF ker. NPO	A7
C11	Cap. 22pF ker. NPO	A7
C12	Cap. 100nF ker.	A6
C13	Cap. 100nF ker.	D6
C14	Cap. 100nF ker.	D6
C15	Cap. 100nF ker.	H5
C16	Cap. 100nF ker.	H4
C17	Cap. 100nF ker.	A8
C18	Cap. 100nF ker.	H1
C19	Cap.10uF/16V Sol.Al	A1
C20	Cap. 100nF ker.	A2
C21	Cap. 100nF ker.	A3
C22	Cap. 100nF ker.	A4
C23	Cap. 100nF ker.	A5
C24	Cap. 100nF ker.	H10
C25	Cap. 100nF ker.	H5
C26	Cap. 100nF ker.	A9
C27	Cap. 100nF ker.	A10
C28	Cap. 100nF ker.	A11
C29	Cap. 100nF ker.	H7
C30	Cap. 100nF ker.	H12
C31	Cap. 100nF ker.	H8
C32	Cap. 100nF ker.	H7
C33	Cap. 100nF ker.	H9
C34	Cap. 100nF ker.	H11
C35	Cap. 100nF ker.	H3
C36	Cap. 100nF ker.	H2
IC1	MB3771	D9
IC2	PC74HCT74P	B10
IC3	PC74HCT221P	C9
IC4	DP8570AV	G10
IC5	NMA0512D OPTION	B11
IC6	PC74HCT00P	E11
IC7	74AS1000AN	F11
IC8	PC74HCT00P	D11
IC9	LTC485	D10
IC10	SN75C189AN	C11
IC11	SN75C189AN	G11
IC12	SN75C188N	C11
IC13	PC74HCT273P	E8
IC14	DS1222	F8
IC15	HD647180X0CP6	A8
IC16	GAL22V10	C4
IC17	GAL22V10	E4
IC18	HN27C101G-25	H8
IC19	HM628128LP-12	H6
IC20	HM628128LP-12	H5
IC21	NQ28C64-250	H8
IC22	DS1210	B4
IC23	DS1210	C4
IC24	74ALS541N	F2
IC25	74ALS541N	E2
IC26	74ALS541N	D2
IC27	74ALS(N 645	D2
IC28	74ALS541N	B2
IC29	74ALS541N	C2
IC30	PC74HCT04P	C10
IC31	LM35DZ	F11
L1	LED LD100-7	E13
L2	LED LD100-7	E13
P9	DB9S conn	G13
P25	DB25S conn	A13
R1	Res. 22k	E10
R2	Res. 22k	E9
R3	Res. 22k	D10
R4	Res. 47R	D8
R5	Res. 47k	E10
R6	Res. 47k	E10

Name	Type	Pos
R7	Res. 47k	E10
R8	Res. SIL 4x 120R	F11
R10	Res. 47k	E10
R11	Res. 47k	D9
R12	Res. 1k	F13
R13	Res. 1k	F12
R16	Res. SIL 9x10k	C2
R17	Res. SIL 9x10k	F2
R18	Res. SIL 9x10k	G2
R19	Res. SIL 9x10k	E2
R20	Res. SIL 9x10k	D7
R21	Res. SIL 9x10k	D4
R22	Res. 4k42 1%	F11
R23	Res. 511R 1%	F12
S1	Strap	E8
S2	Strap	A12
S3	Strap	B9
S4	Strap	H4
S5	Strap	H6
S6	Strap	B5
S7	Strap	E13
S8	Strap	E13
S9	Strap	D13
TP	Test point	H10
V1	Supp.diode SICTE-12	G11
V2	Supp.diode SICTE-12	H11
V3	Supp.diode SICTE-5	B6
X	EURO conn	H1
XT1	XTAL 12.288 MHz	B6
XT2	XTAL 32.768 kHz CX-1	F10

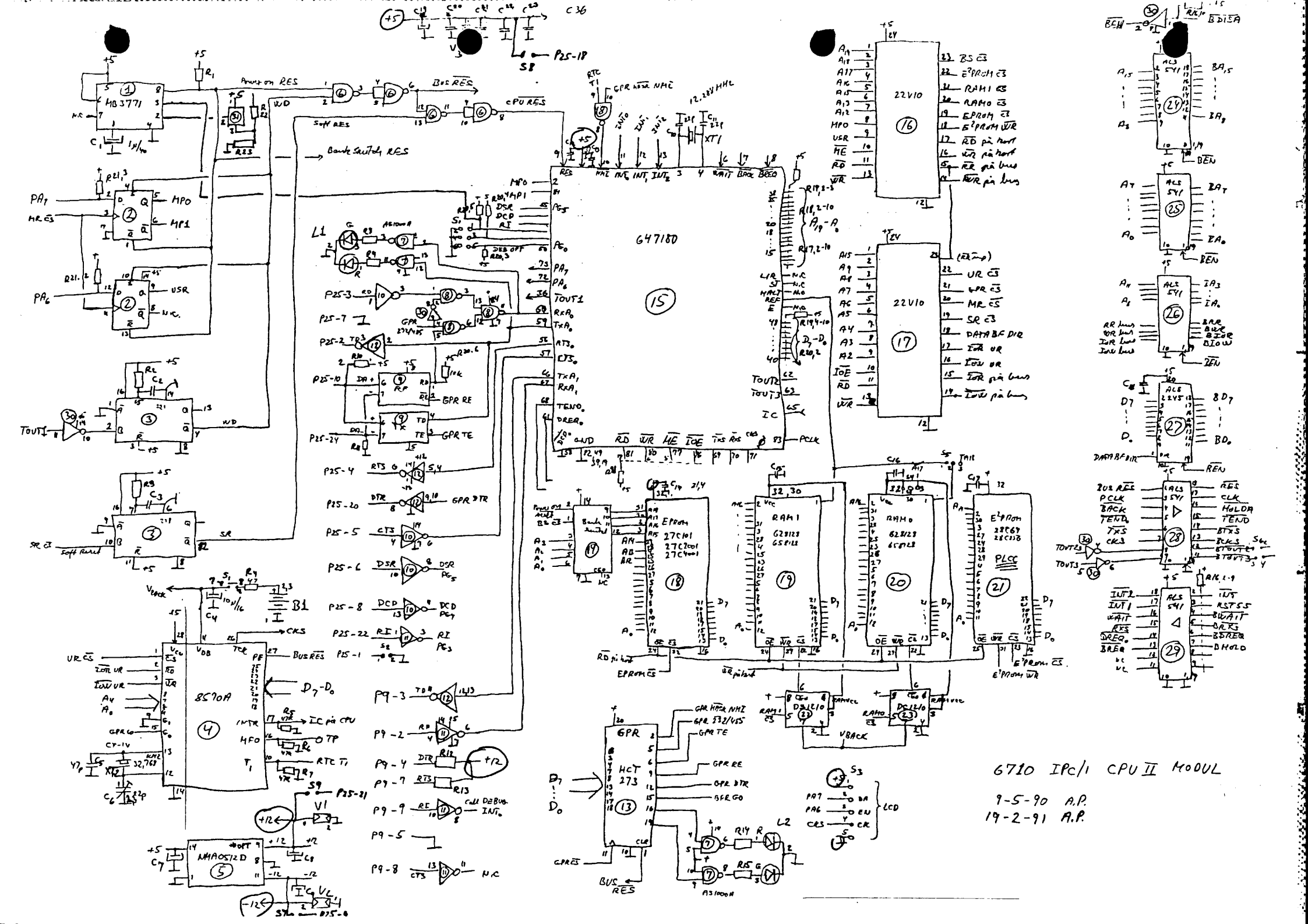
Name	Type	Pos

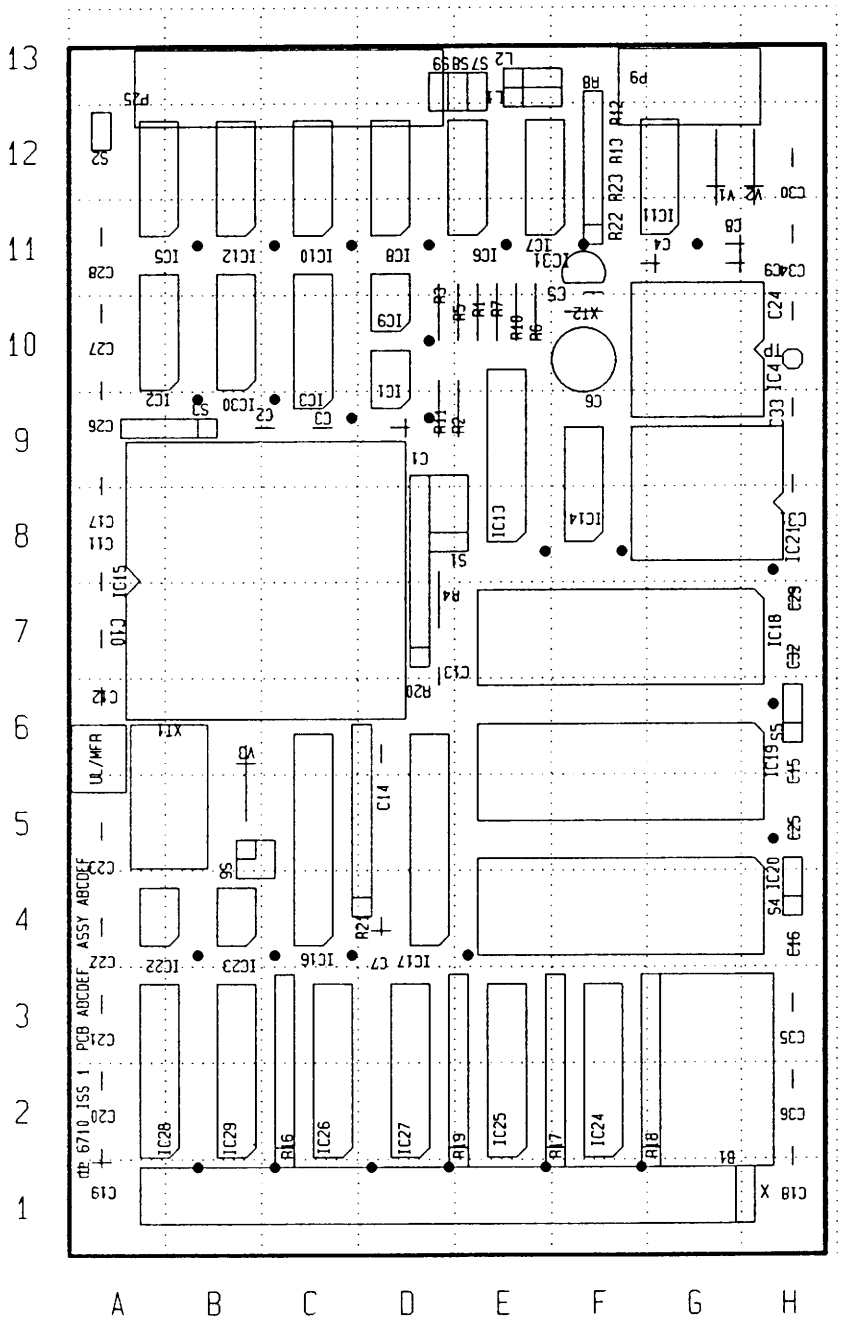
ALTERNATIV FOR IC 19/20: SRM20100LC/10

Component locations

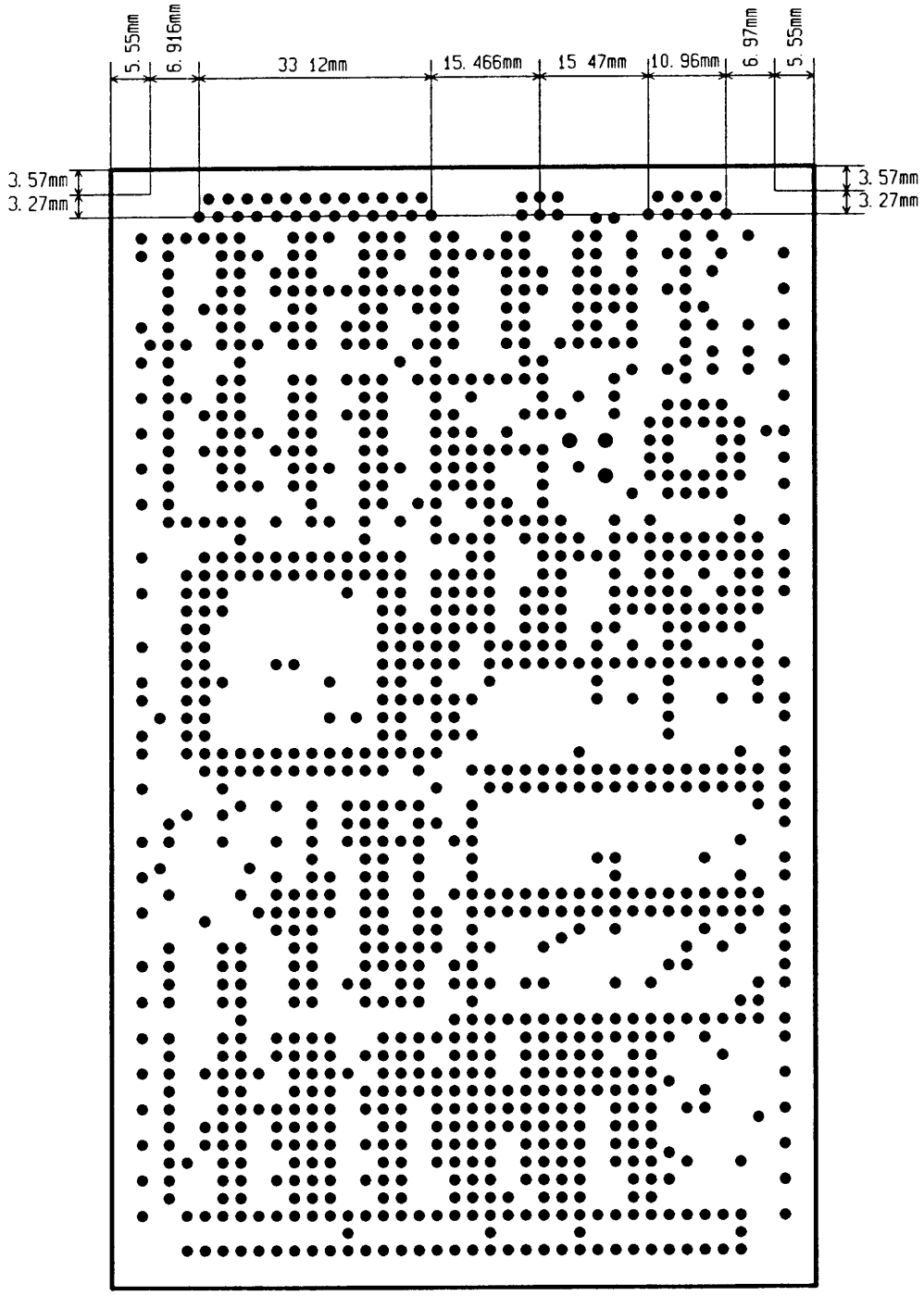
PCB: 6710 / IPC CPU | Issue: 1 | Date: 910131

dansk data elektronik a/s
herlev hovedgade 199, 2730 herlev, tlf 42-84 50 11


6710 IPc/1 CPU II MODUL
9-5-90 A.P.
19-2-91 A.P.



Component locations				
PCB: 6710 / IPC CPU	Issue: 1	Date: 910131	dansk data elektronik a/s	herlev hovedgade 199, 2730 herlev, tlf. 42-84 50 11


5. 55mm
6. 916mm
33 12mm
15. 466mm
15 47mm
10. 96mm
6. 97mm
5. 55mm
3. 57mm
3. 27mm
3. 57mm
3. 27mm

Jedec PAL list for IPL 6710 module

Pal name	Pal position	Pal type	Checksum	Comment
IP160	IC16	G22V10-25(22V10)	C8B0	
IP170	IC17	G22V10-25(22V10)	6414	

Date: 91/05/08 13:55:56
Revision: 1.1
File name: ipc6710

Varenumre (med forbehold)

2 ch:

3500	:	0-10 V
3510	:	0-20 mA
3520	:	4-20 mA

4 ch:

3600	:	0-10 V
3610	:	0-20 mA
3620	:	4-20 mA

6751 TEST 4-kanal Analog Output

```
;                       TEST AF 6751-KORT
BADR:   EQU 70
        JMP EXEC

DATAOO: MVI A,40
        SIM
        MVI A,00
        CALL OUTXX
        RET

DATAFF: MVI A,40
        SIM
        MVI A,0FF
        CALL OUTXX
        RET

OUTXX:  OUT BADR+1
        OUT BADR+0
        OUT BADR+2
        OUT BADR+5
        OUT BADR+4
        OUT BADR+6
        OUT BADR+9
        OUT BADR+8
        OUT BADR+0A
        OUT BADR+0D
        OUT BADR+0C
        OUT BADR+0E
        RET

PRINT:  LN 085
        MAR
        JNC PRINT
        MOV A,M
        CPI 00
        RZ
        OUT 0B4
        INX H
        JMP PRINT

STEP:   MVI A,40                ;EXTERN I/O
        SIM
        LXI H,0000
STEP1:  CALL CHXX
        CALL VENT
        MOV A,H
        ADI 02
        CPI 0FE
        JZ VALG
        MOV H,A
        JMP STEP1

CHXX:   MOV A,H
        OUT BADR+1
        OUT BADR+5
        OUT BADR+9
        OUT BADR+0D
        MOV A,L
        OUT BADR+0
        OUT BADR+2
        OUT BADR+4
        OUT BADR+6
        OUT BADR+8
        OUT BADR+0A
        OUT BADR+0C
        OUT BADR+0E
        RET
```

```
VENT1:  DCX D
        MOV A,D
        ORA E
        NOP
        NOP
        JNZ VENT1
        RET

VALG:   MVI A,0C0
        SIM
        IN 0B5
        RAR
        RAR
        JNC VALG
        IN 0B4
        CPI 31
        CZ DATA00
        CPI 32
        CZ DATAFF
        CPI 33
        JZ STEP
        CPI 34
        JZ 0F008
        JMP VALG

TEXT:   DB 1A,'                                    TEST AF 6751-KORT'
        DB 0D,0A,0A,'STIL ADR.SWITCH P; ADR.70 (SWITCH 2,3,4 ON )'
        DB 0D,0A,0A,' TAST 1 FOR UDL7SNING AF DAT
' 2 FOR UDL7SNING AF DATAV7RDI FFF P; CH 1-4'
0B 0D,0A,0A,' TAST 3 FOR UDL7SNING AF STE
 HCP TIL DEBUG'
B 0D,0A,0A,' :',00

XI H,TEXT
        CALL PRINT
        MVI A,09                    ;KORTTYPE
        OUT 0BF
        JMP VALG
        END EXEC
```

dde Dansk Data Elektronik A/S

Initials | Page 1.
Date | Project

Count	Skal give [V]	Målt CH0	% afv.	Målt CH1	% afv.
1FF	0,2496	0,251	0,07	0,249	0,03
3FF	0,4996	0,500	~~0,05~~	0,~~498~~	0,08
5FF	0,7497	0,750	0,015	0,749	
7FF	0,9998	0,999		1,000	
9FF	1,2498	1,249		1,249	
BFF	1,4999	1,499		1,499	X
DFF	1,7499	1,749		1,749	
FFF	2,000				

MSB

Mat. fejl = 0,4 %

1800 : MVI B, XX (MSB)

[redacted]

MVI A, 40

SIM (30)

[redacted] MOV A,B

OUT 71
MVI A, F0
OUT 70
OUT 72
} CH1

[redacted] MOV A,B

OUT 75
MVI A, F0
OUT 74
OUT 76
} CH2

JMP F000

Tilføjes 6751 test for måling af linearitet, jvf. skema næste side

Varenummer: 6751

IPC 6017

Analog Output

KANAL	Råværdi	Signal mA
0	0	0,00
0	6553	3,88
0	16380	9,89
0	32760	18,70
1	0	0.00
1	6553	3.92
1	16380	9,92
1	32760	10,30

KORT TYPE: AO

Kanal 0 defekt

Kanal 1 defekt

KANAL	Råværdi	Signal mA
0	0	0,00
0	6553	3,94
0	16380	9,93
0	32760	19,90
1	0	0,00
1	6553	3,83
1	16380	9.82
1	32760	10,28

KORT TYPE: AO

Kanal 1 defekt

KANAL	Råverdi	Signal mA
0	0	6,00
0	6553	4,08
0	16380	9,99
0	32760	19,99
1	0	0,03
1	6553	4,11
1	16380	9,97
1	32760	10,28

KORT TYPE: AO

Kanal 1. dekket

KANAL	Råverd	
0	0	0
0	6553	3,96
0	16380	9,97
0	32760	20,07
1	0	0
1	6553	3,91
1	16380	9,96
1	32760	10,0

KORT TYPE: AO

Kanal 1 defekt

KANAL	Råværdi	Signal mA
0	0	0,00
0	6553	3,91
0	16380	9,91
0	32760	20.01
1	0	0,00
1	6553	3,93
1	16380	9,93
1	32760	10.50

KORT TYPE: AO

Kanal 1 defekt.

KANAL	Råværdi	Signal mA
0	0	0,00
0	6553	3,89
0	16380	9,89
0	32760	20,02
1	0	0,00
1	6553	3,86
1	16380	9,90
1	32760	10,50

KORT TYPE: AO

Kanal 1 defekt

Dansk Data Elektronik A/S

Initials | Page | Date | Project

IPC 6757 Linearitet, Prototypeboard

counts HEX			counts	output ideel [mA]	MÅLT CH0	afv. µA	afv %	CH 1	afv µA	afv %
0	0	0	0	0	2 µA	+2 µA	+0,01%	2 µA	+2 µA	+0,01%
0	7	F	127	620,3 µA	606 µA	-14		632 µA	+12	
0	F	F	255	1245 µA	1240 µA	-5		1256 µA	+11	
1	7	F	383	1871 µA	1855 µA	-16 *	-0,08%	1883 µA	+12 *	+0,06%
1	F	F	511	2,496 mA	2,489 mA	-10		2,503 mA	+7	
2	7	F	639	3,121 mA	3,107	-14		3,130	+9	
2	F	F	767	3,746	3,732	-14		3,753	+7	
3	7	F	895	4,371	4,358	-13		4,381	+10	
3	F	F	1023	4,996	4,991	-5		5,001	+5	
4	7	F	1151	5,621	5,609	-12		5,631	+10	
4	F	F	1279	6,247	6,236	-11		6,255	+8	
5	7	F	1407	6,872	6,860	-12		6,882	+10	
5	F	F	1535	7,497	7,493	-4		7,502	+5	
6	7	F	1663	8,122	8,111	-11		8,129	+7	
6	F	F	1791	8,747	8,745	-2		8,753	+6	
7	7	F	1919	9,372	9,366	-6		9,382	+10	
7	F	F	2047	9,998	9,996	-2		10,001	+3	
8	7	F	2175	10,623	10,611	-12		10,630	+7	
8	F	F	2303	11,248	11,238	-10		11,253	+5	
9	7	F	2431	11,873	11,860	-13		11,881	+8	
9	F	F	2559	12,498	12,494	-4		12,502	+4	
A	7	F	2687	13,123	13,112	-11		13,128	+5	
A	F	F	2815	13,748	13,739	-9		13,752	+4	
B	7	F	2943	14,374	14,363	-11		14,380	+6	
B	F	F	3071	14,999	14,996	-3		15,000	+1	
C	7	F	3199	15,624	15,614	-10		15,630	+6	
C	F	F	3327	16,249	16,241	-8		16,254	+5	
D	7	F	3455	16,874	16,864	-10		16,882	+8	
D	F	F	3583	17,499	17,498	-1		17,503	+4	
E	7	F	3711	18,125	18,116	-9		18,130	+5	
E	F	F	3839	18,750	18,743	-7		18,753	+3	
F	7	F	3967	19,375	19,367	-8		19,382	+8	
F	F	F	4095	20,000 mA	19,999	-1	-0,005%	20,002	+2	+0,01%

MSB | altid FO_H i LSB

På lab. just kort:

Gain, offset. typ ± 0,01% FSR } ± 0,1% FSR.

Ulinearitet, typ ± 0,08% FSR

Beregnet max. iflg datablade er ± 0,3% FSR

Ref: målt af kunden:

KANAL	Råværdi	Signal mA	
0	0	0,00	0
0	6553	3,78	4 ← skal være 4 mA ÷ 5,5 %
0	16380	9,85	10 ÷ 1,5 %
0	32760	20,05	20
1	0	0,06	
1	6553	4,14	
1	16380	10,10	
1	32760	10,70	(2)

KORT TYPE: AD

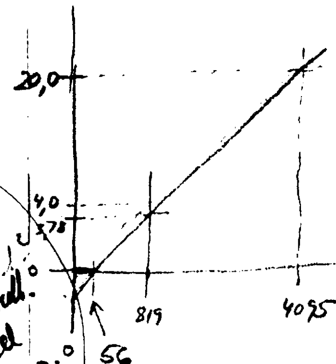
Kanal 0 defekt

Kanal 1 defekt

Ved modtagelse af kort

målt:

	målt:	skal være:	Efter justering: målt:	afvigelse:
CH0: 0 (0 counts) ~	0,000	0,000	0,002	2 μA
440 (55 counts) ~	0,005	0,269	0,230	-39 μA
6552 (819 counts) ~	3,781	4,000	3,953	-47 μA $\frac{50 \mu A}{20 mA}$ = 0,25 %
16380 (2048 counts) ~	9,920	10,000	10,009	+9 μA
32760 (4095 counts) ~	20,047	20,000	20,000	0
CH1: 0 ~	0,000	0,000	0,001	1 μA
448 ~	0,259	0,274	0,320	46 μA
6552 ~	4,025	4,000	4,078	78 μA $\frac{78 \mu A}{20 mA}$ = 0,39 %
16380 ~	9,995	10,000	9,989	-11 μA
32760 ~	20,050	20,000	20,000	0



spænding out:

CH0:	Før	Efter	CH1:	Før	Efter
	2 mV	2 mV		-13 mV	0
0			0		
55 counts	0,1888	0,115	56	0,1408	0,161
819	2,0035	1,975	819	2,0267	2,042
2048	5,011	5,002	2048	5,017	5,002
4095	10,130	9,992	4095	10,053	10,015

undersøgelse viser at: offset på kanal 0 ikke var justeret; ulineariteten på typ 0,3 % er normalt. kundens måling på kanal 1 ved full scale kan ikke reproduceres; fejl fundet på kanal 1. 19/3-91

Afvigelser måles altid i forhold til full scale output!

Varenummer	Beskrivelse	ABC Kls	Typ Kod	Bestilt Antal	På lag.	I ordre	Allok	Reserv.	Disponibel
Hovedvarenummer									
99746752	ANALOG OUTPUT 4CH 12 BIT			1	Kontrakt:				
Varenummer									
9899001000	* TEX. SN74ALS00AN	C	4	1.0000	368	0	0	0	368
9899002810	* TEX. SN75447P	C	4	1.0000	8	0	0	0	8
9899005019	* LF 356 N	C	4	5.0000	15	0	0	0	15
9899005020	* LM 358 N	C	4	2.0000	35	0	0	0	35
9899012002	* ISO 122 P	C	4	4.0000	0	0	0	0	0
9899012014	* 1403	C	4	1.0000	10	0	0	0	10
9899012057	* HSSR-8200	C	4	4.0000	22	0	0	0	22
9899020040	* RES. 820 OHM 1/4W 5%	C	4	4.0000	4696	0	0	0	4696
9899020201	* RES. 1 K 1/4W 1%	C	4	8.0000	942	0	0	0	942
9899022206	* NETVÆRK 4609X/R-101-103	C	4	1.0000	58	0	0	0	58
99000423	TI SN74LS136N	C	4	2.0000	0	0	0	0	0
99001007	* TI SN74ALS74AN	C	4	1.0000	656	0	0	0	656
99001010	+ TI SN74ALS138N	C	4	1.0000	14	0	0	0	14
99001021	+ TI SN74ALS573CN	B	4	1.0000	0	0	0	0	0
99001028	* TI SN74ALS642AN	C	4	1.0000	309	0	0	0	309
99012001	* XTR 110 KP	C	4	4.0000	6	0	0	0	6
99012013	* 12 BIT UP COMP DAC	C	4	4.0000	45	0	0	0	45
99012023	* NMA 2415 D	C	4	2.0000	8	0	0	0	8
99012070	* HEXDIP	C	4	4.0000	95	0	0	0	95
99020007	RES. 270 OHM 1/4W 5%	C	4	4.0000	2450	0	0	0	2450
99020008	RES. 330 OHM 1/4W 5%	C	4	8.0000	473	0	0	0	473
99020013	RES. 1 K 1/4W 5%	C	4	2.0000	2368	0	0	0	2368
99020030	RES. 100 K 1/4W 5%	C	4	4.0000	936	0	0	0	936
99020038	RES. 47 OHM 1/4W 5%	C	4	4.0000	1283	0	0	0	1283
99020203	RES. 10 K 1/4W 1%	C	4	11.0000	729	0	0	0	729
99020225	* RES. 200 OHM 1%	C	4	1.0000	1014	0	0	0	1014
99020803	KOND.104K 2 MODUL	C	4	8.0000	4292	0	0	0	4292
99020811	* KOND. 3.3 UF 5%	C	4	8.0000	492	0	0	0	492
99020812	* KOND. 470 NF 5%	C	4	5.0000	501	0	0	0	501
99020835	KOND.POLY. 100V	C	4	3.0000	269	0	0	0	269
99020950	METAL KON. 10uF/16V	C	4	7.0000	107	0	0	0	107

36 stk

99020952	METAL KON. 1uF/40V	C	4	4.0000	660	0	0	660
99021208	DIODE 1N4148	C	4	16.0000	2028	0	50	1978
99021218	* ZENER BZX 79-C16	C	4	4.0000	146	0	0	146
99022400	* POOTM. 3266W-20K	C	4	12.0000	114	0	0	114
99022404	* POTM. 3266W-1-102	C	4	4.0000	72	0	0	72
99022805	8 BIT SWITCH	C	4	1.0000	15	0	0	15
99025000	FERRITSPOLE	C	4	1.0000	327	0	0	327
99030807	* IPC 6017	C	4	1.0000	8	0	0	8
99041002	100-964-053 IPC	C	4	1.0000	577	0	0	577
99041003	100-064-053 IPC	C	4	1.0000	282	0	0	282

Varenummer	Beskrivelse	ABC Kls	Typ Kod	Bestilt Antal	På lag.	I ordre	Allok	Reserv.	Disponibel
Hovedvarenummer									
99746752	ANALOG OUTPUT 4CH 12 BIT			1	Kontrakt:				
Varenummer									
99061613	* IPC FORPLADE 6751	C	4	1.0000	4	0	0	0	4

*** Slut på rapport ***

IKKE ALLE KOMPONENTER MONTERES I STANDARD VERSIONEN, SE TEKST.

Name	Type	Pos
C1	10uF/16V Sol.Al	E8
C2	10uF/16V Sol.Al	G8
C3	10uF/16V Sol.Al	A8
C4	10uF/16V Sol.Al	B8
C5	470nF ker.	D6
C6	1uF/40V Sol.Al	C7
C7	1uF/40V Sol.Al	A12
C11	3n3 ker.	C6
C12	3n3 ker.	B7
C13	470nF ker.	B8
C14	100 nF	B11
C15	100 nF	B11
C17	10uF/16V Sol.Al	A2
C18	100 nF	A4
C19	100 nF	H2
C20	100 nF	H6
C21	3n3 ker.	D6
C22	3n3 ker.	B7
C23	470nF ker.	D8
C24	100 nF	B11
C25	100 nF	C11
C31	3n3 ker.	F6
C32	3n3 ker.	F7
C33	470nF ker.	G8
C34	100 nF	F11
C35	100 nF	F11
C41	3n3 ker.	G6
C42	3n3 ker.	G7
C43	470nF ker.	H8
C44	100 nF	F11
C45	100 nF	G11
C50	1uF/40V Sol.Al	H9
C51	10uF/16V Sol.Al	H3
C52	10uF/16V Sol.Al	A2
D11	1N4148	E11
D12	1N4148	D11
D13	BZX85C16	B9
D14	1N4148	C12
D15	1N4148	C12
D21	1N4148	B12
D22	1N4148	B11
D23	BZX85C16	B9
D24	1N4148	D12
D25	1N4148	D12
D31	1N4148	H12
D32	1N4148	H11
D33	BZX85C16	F9
D34	1N4148	E12
D35	1N4148	E12
D41	1N4148	H12
D42	1N4148	H12
D43	BZX85C16	G9
D44	1N4148	G12
D45	1N4148	G12
IC1	74LS136N	F2
IC2	74LS136N	F2
IC3	74ALS00N	C2
IC4	74ALS74AN	D2
IC5	74ALS573N	E4
IC6	74ALS138N	E2
IC7	AD1403N	B2
IC8	LF356N	B4
IC9	NMA2415D	E6
IC10	NMA2415D	D6
IC11	DAC1230LCJ-1	C4
IC12	LF356N	B5
IC13	ISO122P	B6
IC14	XTR110P	B9
IC15	LM358N	D10
IC16	IRFD9110	B11
IC17	HSSR-8200	B8
IC21	DAC1230LCJ-1	D4
IC22	LF356N	B5
IC23	ISO122P	C6
IC24	XTR110P	C9
IC26	IRFD9110	C11
IC27	HSSR-8200	C8
IC31	DAC1230LCJ-1	F4

Name	Type	Pos
IC32	LF356N	H4
IC33	ISO122P	F6
IC34	XTR110P	F9
IC35	LM358N	E10
IC36	IRFD9110	F11
IC37	HSSR-8200	F8
IC41	DAC1230LCJ-1	G4
IC42	LF356N	H5
IC43	ISO122P	H6
IC44	XTR110P	H9
IC46	IRFD9110	H11
IC47	HSSR-8200	H8
IC50	74ALS642	F4
IC51	75447	B2
L1	Inductor	A12
P	EURO conn	A13
RA	196k MR25 1% (option	A6
RB	196k MR25 1% (option	C6
RC	196k MR25 1% (option	F6
RD	196k MR25 1% (option	F6
R1	8x10k	G2
R5	1k	G2
R6	10k MR25 1%	B2
R7	10k MR25 1%	B2
R8	10k MR25 1%	A4
R9	~~332R~~ MR25 1% 200R	B4
R10	~~1k~~ 820R	A9
R11	1k00 MR25 1%	A6
R12	1k00 MR25 1%	B8
R13	10k MR25 1%	D11
R14	330R	B12
R15	47R	B12
R16	10k MR25 1%	D11
R17	330R	D9
R18	100K	D9
R19	270R	A12
R20	~~1k~~ 820R	B9
R21	1k00 MR25 1%	B6
R22	1k00 MR25 1%	C8
R23	10k MR25 1%	D11
R24	330R	D12
R25	47R	D12
R26	10k MR25 1%	C9
R27	330R	D9
R28	100K	D9
R29	270R	B11
R30	~~1k~~ 820R	E9
R31	1k00 MR25 1%	E6
R32	1k00 MR25 1%	F8
R33	10k MR25 1%	E9
R34	330R	E12
R35	47R	E12
R36	10k MR25 1%	E11
R37	330R	E9
R38	100K	D9
R39	270R	G11
R40	~~1k~~ 820R	G9
R41	1k00 MR25 1%	G6
R42	1k00 MR25 1%	H8
R43	10k MR25 1%	E11
R44	330R	F12
R45	47R	F12
R46	10k MR25 1%	E11
R47	330R	E9
R48	100K	E9
R49	270R	H12
R50	1k	G2
SW1	DIL switch 4 el. 8	H2
S11	Strap	A10
S12	Strap	A11
S21	Strap	B10
S22	Strap	B11
S31	Strap	E10
S32	Strap	E11
S41	Strap	G10
S42	Strap	G11
TP12	Test point	B10
TP22	Test point	C10

Name	Type	Pos
TP32	Test point	F10
TP42	Test point	H10
TR11	Trimmepotm. 1k	C6
TR12	Trimmepotm. 20k	B6
TR13	Trimmepotm. 20k	D8
TR14	Trimmepotm. 20k	B10
TR21	Trimmepotm. 1k	D6
TR22	Trimmepotm. 20k	B6
TR23	Trimmepotm. 20k	D8
TR24	Trimmepotm. 20k	D10
TR31	Trimmepotm. 1k	F6
TR32	Trimmepotm. 20k	H6
TR33	Trimmepotm. 20k	E8
TR34	Trimmepotm. 20k	G10
TR41	Trimmepotm. 1k	G6
TR42	Trimmepotm. 20k	H6
TR43	Trimmepotm. 20k	E8
TR44	Trimmepotm. 20k	H10
X	EURO conn	H1

87718-3

Component locations

PCB: 6017 / D-A | Issue: 1 | Date: 900228

dansk data elektronik a/s
herlev hovedgade 199, 2730 herlev, tlf 02-84 58 11

MANUAL

for

IPC/1 6751 Analog Output modul.

Dansk Data Elektronik A/S

Oktober 1989 / Marts 1990.

Forfatter: Allan Petersen

Oktober 1989. Revideret Marts 1990.

Dansk Data Elektronik A/S

Test af 6751 + 6752	Initials	Page
	Date	Project

Addr. sw: 2+3+4 ON = adr. 70

Start konvertering med output = 00

```
4200: MVI A,00          4000: output high
      SIM (30)
      MVI A,09
      OUT BF
      MVI A,40
      SIM (30)
      MVI A,00    (FF → output high)
      OUT 71
      MVI A,00    ( ——— " ——— )
      OUT 70
      OUT 72
      MVI A,00    ( ——— " ——— )
      OUT 75
      MVI A,00    ( ——— " ——— )
      OUT 74
      OUT 76
      MVI A,00    ( ——— " ——— )
      OUT 79
      MVI A,00    ( ——— " ——— )
      OUT 78
      OUT 7A
      MVI A,00    ( ——— " ——— )
      OUT 7D
      MVI A,00    ( ——— " ——— )
      OUT 7C
      OUT 7E
4034  JMP F000
```

4. Justering

De fire kanaler justeres hver for sig. For hver kanal findes fire trimmepotmetre, TRx1, TRx2, TRx3 og TRx4, hvor x står for kanal 1 til 4.

Først udlæses (f.eks med TEST I/O eller Ladder-Logic) en dataværdi = 0 til den pågældende kanal.

Med digitalvoltmeter på TPx2 trimmes på TRx2 til offset er mindre end ± 1 mV. Dernæst trimmes TRx3 til offset er mindre end ± 2 mV på spændingsudgangen for den pågældende kanal.

Med en modstand på 100,0 Ohm (0,1 %) forbundet mellem kanalens strømudgang og stel trimmes TRx4 til en visning på mellem 0 mV og 0,5 mV over målemodstanden (for område 0 - 20 mA).

Dernæst udlæses dataværdi = 32767 decimalt (TEST I/O) til den pågældende kanal.

Med digitalvoltmeter på spændingsudgangen trimmes på TRx1 til en spænding på 10,00 V. Det kontrolleres, at der nu er en spænding på 2,000 V over strømmålemodstanden (svarende til 20,00 mA).

Med Ladder-Logic udlæses derefter en step-spænding, med step af 255 decimalt for hver gennemløb af koden, på den pågældende kanal. Såvel strøm- som spændingsudgangen betragtes med et oscilloscop. Det kontrolleres, at signalets indsvingninger og trinstørrelser er ensartede.

Justering:

Standardudgaven har strapning til 0 - 20 mA strømudgang.
De fire kanaler justeres hver for sig. For hver kanal findes fire trimmepotmetre, TRx1, TRx2, TRx3 og TRx4, hvor x står for kanal 1 til 4.

Først udlæses (med debugger eller testprogram) dataværdi = 0 til den pågældende kanal og konverteringen startes.

Med digitalvoltmeter på TPx2 trimmes på TRx2 til offset mindre end +- 1 mV. Dernæst trimmes TRx3 til offset mindre end +- 2 mV på spændingsudgangen for den pågældende kanal.

Isolationsforstærkeren har typisk et offset på mindre end 10 mV (kan måles på TPx2 med pin 15 og 16 kortsluttet på ICx3); hvis offset er større end 20 mV, kan det være svært at justere udgangen på kortet til nul. Da bør isolationsforstærkeren skiftes (kan dog også løses med en ekstra biasmodstand svarende til RA).

Med en modstand på 100,0 ohm (0,1 %) forbundet mellem kanalens strømudgang og stel trimmes TRx4 til en visning på mellem 0 mV og 0,5 mV over målemodstanden (for område 0 - 20 mA).

P.S.: Strømudgangen kan ikke levere negativ udgangsstrøm; justering foretages ved at justere til en positiv værdi for derefter at dreje potm. tilbage til netop 0.

Dernæst udlæses dataværdi = FFF hex (full scale output) til den pågældende kanal og konverteringen startes.

(typisk til 0,2 mV svarer => 2 µA

Se bagsiden

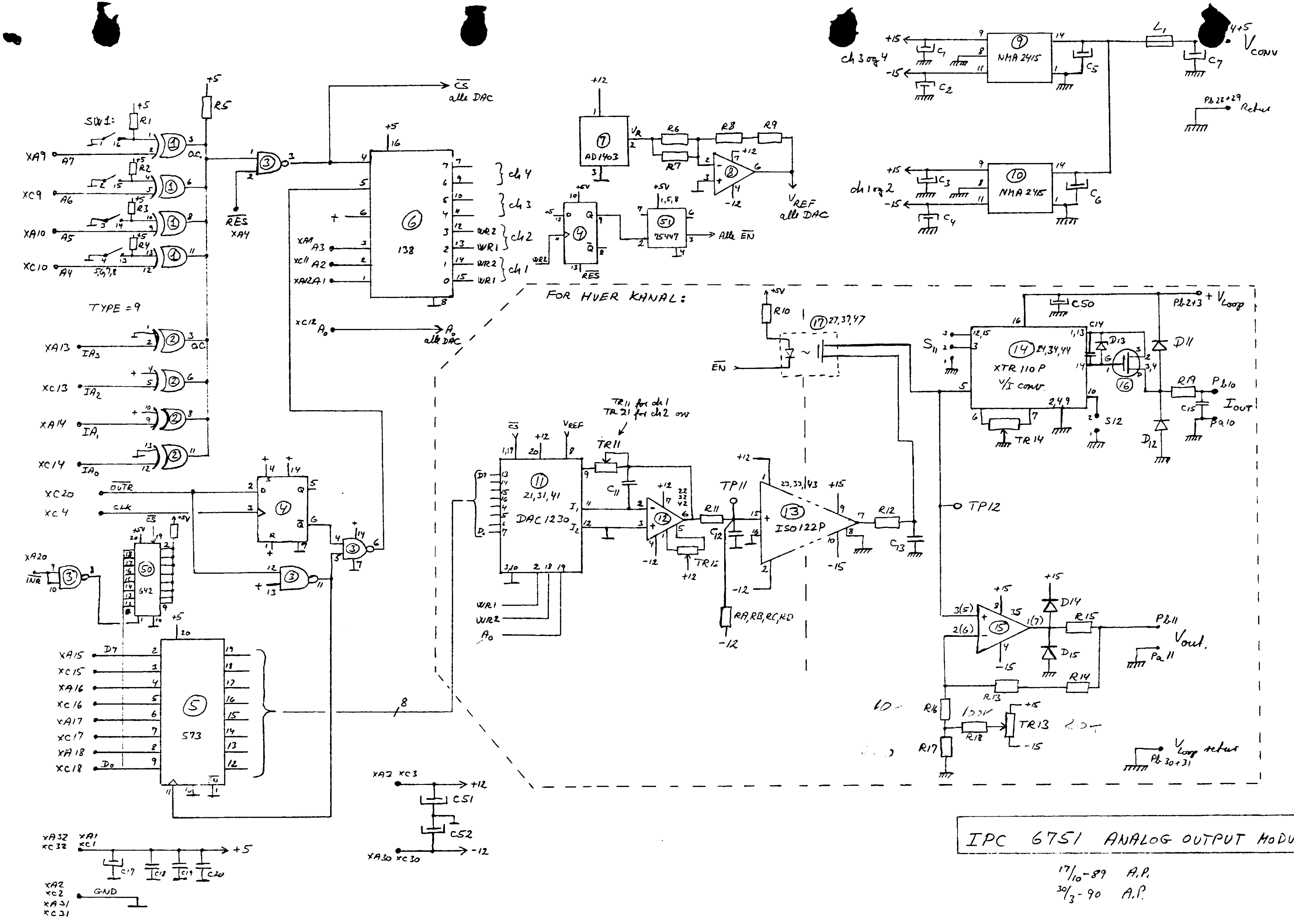
Med digitalvoltmeter på spændingsudgangen trimmes på TRx1 til en spændingsvisning på 10,00 volt. Det kontrolleres, at der nu er en spænding på 2,000 volt over strømmålemodstanden (svarende til 20,00 mA).

Med debuggeren udlæses derefter en step-spænding (optæl f.eks. dataværdien med 200h for hvert gennemløb af loop'en) på den pågældende kanal, og såvel strøm- som spændingsudgangen betragtes med et oscilloskop. Det kontrolleres, at signalets indsvingninger er dæmpede, og at trinstørrelserne er ensartede.

Justering af offset:

Udlæs data 00 til kanal 1+2 (+3+4)

Drej potm TR14 (+ TR24) højre om og bemærk den minimale visning der kan forekomme. Drej derefter potm venstre om til en højere værdi. Drej derefter højre om indtil den minimale værdi netop nås.



IPC 6751 ANALOG OUTPUT MODUL

17/10-89 A.P.
30/3-90 A.P.

Indholdsfortegnelse:

Introduktion.

IPC/1 6751 modulet er et analog output kort med op til fire separate kanaler, hvor hver kanal kan give såvel et 0 - 10 V spændingssignal som et 0 - 20 mA eller 4 - 20 mA current loop signal.
Standardudgaven har to kanaler og giver et 0 - 10 V spændingssignal samt et 0 - 20 mA current loop signal for hver kanal.

D/A konverteringen for hver kanal foretages med en 12 bit D/A konverter.

Udgangssiden er galvanisk adskilt (isolation 1500 V DC) fra processor siden. Udgangssiden skal have en ekstern (fælles) strømforsyning.

Kortet indeholder skematisk følgende kredsløb:

- D/A konverter, isolationsforstærker, V/I konverter og analog udgangsforstærker for hver kanal.

- Fælles spændingsreferance for D/A konverterne.

- DC/DC konverter til udgangskredsløbene, så kortet kan forsynes fra een fælles ekstern forsyning.

- Adressedekodning og enabling for tilslutning til IPC/1 datamat.

Udgangene har beskyttelsesdioder og -modstande til beskyttelse mod almindeligt forekommende transienter. Udgangene og den eksterne strømforsyning har fælles stel.

Funktionel beskrivelse.

Kortet kan bestykkes med op til fire analog output kanaler. Standard versionen af kortet har monteret de to første kanaler, mens den udvidede version af kortet har monteret alle fire kanaler.

Hver kanal er opbygget omkring tre hovedkomponenter: En 12 bit D/A konverter DAC 1230, en isolationsforstærker ISO122P og en spænding til strømsløjfe konverter XTR110P.
På kortet findes også en fælles spændingsreferance til D/A konverterne.

Konverteringstid: 10 mS max. (fra start af konvertering).

V/I konverteren har en ekstern MOSFET til styring af udgangs-strømmen. Strømudgangen kan strappes til enten 0 - 20 mA eller til 4 - 20 mA (dog skal kortet justeres på ny efter strap-ændring).
For hver kanal er der foruden V/I konverteren anbragt en operations-forstærker, der leverer et spændingsoutput.
Offset og gain kan trimmes separat for strøm- og spændingsudgangen for hver kanal.

Alle udgange (såvel spænding som strøm) har fælles stel; dette gælder også den eksterne strømforsyning. Forsyningen til kredsene på udgangssiden skal være 24 V DC (+- 2V) og forbruget er max. 250 mA for hvert kort. Dog er forsyningen til strømsløjferne ført ud separat (men normalt forbundet til den faste eksterne forsyning).

Ved læsning fra en vilkårlig af kortets adresser vil der svares med data = 00h som indikering af, at kortet er monteret.

Efter power-up er alle udgange på kortet disablede, svarende til udlæst dataværdi = 00h. Ved første konv. start kommando på kanal 1 enables alle udgange på kortet. Der kan således udlæses initial dataværdier til kanalernes dataregistre og konverteres, inden alle udgange samtidig åbnes ved start af konvertering på kanal 1.

Ved power-off for IPC datamaten disables kortets udgange, svarende til udlæsning af dataværdi = 00h, uanset om den eksterne forsyning til kortets udgangsside er on eller off.

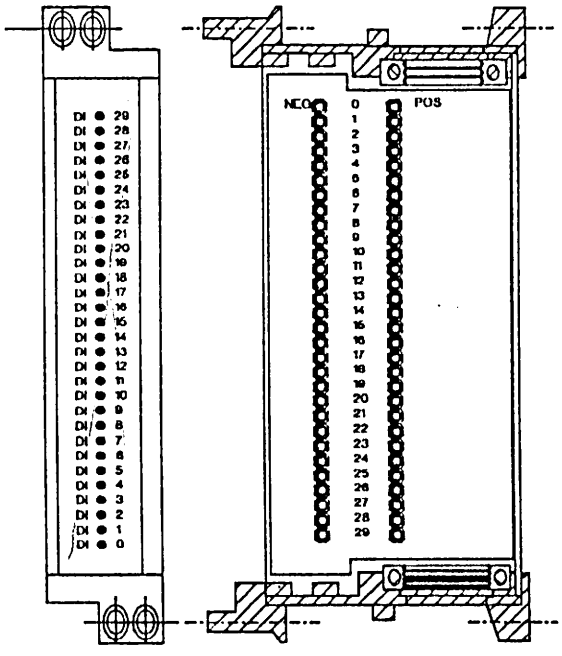
Strapsettings:

S11 (21,31,41):	For 4 - 20 mA:	.* *--*
	For 0 - 20 mA:	.*--* *
S12 (22,32,42):	For 4 - 20 mA:	.* *
	For 0 - 20 mA:	.*--*

Tilslutning til periferien foretages via en Europakonnektor DIN 41612, byggeform B, 64 polet hanstik, som er monteret på kortet.

I stikket sættes en adaptor (også kaldet et periferistik), der er påmonteret to specielle flanger, der dels muliggør fastspænding i IPC/1 rack, dels muliggør fastspænding af periferistikket.

Tilslutning af signalledningerne (samt ekstern strømforsyning) sker i periferistikket (varenummer 6751c), der er forsynet med loddeterminaler:



Connections:

Channel #:	Name:	Channel #:	Name:
0 (minus)	NEG_0	15 (minus)	NEG 15
0 (plus)	POS_0	15 (plus)	POS 15
1 (minus)	NEG_1	16 (minus)	NEG_16
1 (plus)	POS_1	16 (plus)	POS_16
2 (minus)	NEG_2	17 (minus)	NEG_17
2 (plus)	POS_2	17 (plus)	POS_17
3 (minus)	NEG_3	18 (minus)	NEG 18
3 (plus)	POS_3	18 (plus)	POS 18
4 (minus)	NEG 4	19 (minus)	NEG 19
4 (plus)	POS 4	19 (plus)	POS 19
5 (minus)	NEG 5	20 (minus)	NEG_20
5 (plus)	POS 5	20 (plus)	POS_20
6 (minus)	NEG 6	21 (minus)	NEG_21
6 (plus)	POS 6	21 (plus)	POS_21
7 (minus)	NEG 7	22 (minus)	NEG 22
7 (plus)	POS 7	22 (plus)	POS 22
8 (minus)	NEG_8	23 (minus)	NEG 23
8 (plus)	POS_8	23 (plus)	POS 23
9 (minus)	NEG_9	24 (minus)	NEG 24
9 (plus)	POS_9	24 (plus)	POS 24
10 (minus)	NEG 10	25 (minus)	NEG 25
10 (plus)	POS 10	25 (plus)	POS 25
11 (minus)	NEG 11	26 (minus)	NEG_26
11 (plus)	POS 11	26 (plus)	POS_26
12 (minus)	NEG 12	27 (minus)	NEG_27
12 (plus)	POS_12	27 (plus)	POS_27
13 (minus)	NEG 13	28 (minus)	NEG_28
13 (plus)	POS 13	28 (plus)	POS_28
14 (minus)	NEG 14	29 (minus)	NEG_29
14 (plus)	POS 14	29 (plus)	POS_29

Adressering.

Kortet optager 16 I/O adresser; basisadressen sættes på kortet på et switch register. Den til kortet hørende type-adresse (TYPE = 9) er fast kodet i printet.

OUT:

+0F		
+0E	tilsv. for kanal 4	
+0D		(hvis
+0C		monteret)
+0B		
+0A	tilsv. for kanal 3	
+09		
+08		
+07	(ikke benyttet)	
+06	konv. start	tilsv. for kanal 2
+05	8 MSB data.....	
+04	4 LSB data	
+03	(ikke benyttet)	for kanal 1
+02	konv. start (og enable alle outputs).	
+01	8 MSB data.....	
Base adr. +00	4 LSB data	

7 6 5 4 3 2 1 0
Databit

IN: Alle adr.: Svarer med data = 00h.

Set up data:

Skriv data til Adr.1 (8 MSB), derefter data til Adr.0 (4 LSB).

Start konvertering:

Konvertering foretages først, når der udføres en skrivning til Adr.2 (data ligegyldig).

99020952	METAL KON. 1uF/40V	C	4	4.0000	660	0	0	0	660
99021208	DIODE 1N4148	C	4	16.0000	2028	0	50	50	1978
99021218	* ZENER BZX 79-C16	C	4	4.0000	146	0	0	0	146
99022400	* POOTM. 3266W-20K	C	4	12.0000	114	0	0	0	114
99022404	* POTM. 3266W-1-102	C	4	4.0000	72	0	0	0	72
99022805	8 BIT SWITCH	C	4	1.0000	15	0	0	0	15
99025000	FERRITSPOLE	C	4	1.0000	327	0	0	0	327
99030807	* IPC 6017	C	4	1.0000	8	0	0	0	8
99041002	100-964-053 IPC	C	4	1.0000	577	0	0	0	577
99041003	100-064-053 IPC	C	4	1.0000	282	0	0	0	282

Varenummer	Beskrivelse	ABC Kls	Typ Kod	Bestilt Antal	På lag.	I ordre	Allok	Reserv.	Disponibel
Hovedvarenummer									
99746752	ANALOG OUTPUT 4CH 12 BIT			1	Kontrakt:				
Varenummer									
99061613	* IPC FORPLADE 6751	C	4	1.0000	4	0	0	0	4

*** Slut på rapport ***

Hovedvarenummer

99746752 ANALOG OUTPUT 4CH 12 BIT — Bestilt Antal: 1 — Kontrakt:

Varenummer

Varenummer	Beskrivelse	ABC Kls	Typ Kod	Bestilt Antal	På lag.	I ordre	Allok	Reserv.	Disponibel
9899001000	* TEX. SN74ALS00AN	C	4	1.0000	368	0	0	0	368
9899002810	* TEX. SN75447P	C	4	1.0000	8	0	0	0	8
9899005019	* LF 356 N	C	4	5.0000	15	0	0	0	15
9899005020	* LM 358 N	C	4	2.0000	35	0	0	0	35
9899012002	* ISO 122 P	C	4	4.0000	0	0	0	0	0
9899012014	* 1403	C	4	1.0000	10	0	0	0	10
9899012057	* HSSR-8200	C	4	4.0000	22	0	0	0	22
9899020040	* RES. 820 OHM 1/4W 5%	C	4	4.0000	4696	0	0	0	4696
9899020201	* RES. 1 K 1/4W 1%	C	4	8.0000	942	0	0	0	942
9899022206	* NETVÆRK 4609X/R-101-103	C	4	1.0000	58	0	0	0	58
99000423	TI SN74LS136N	C	4	2.0000	0	0	0	0	0
99001007	* TI SN74ALS74AN	C	4	1.0000	656	0	0	0	656
99001010	+ TI SN74ALS138N	C	4	1.0000	14	0	0	0	14
99001021	+ TI SN74ALS573CN	B	4	1.0000	0	0	0	0	0
99001028	* TI SN74ALS642AN	C	4	1.0000	309	0	0	0	309
99012001	* XTR 110 KP	C	4	4.0000	6	0	0	0	6
99012013	* 12 BIT UP COMP DAC	C	4	4.0000	45	0	0	0	45
99012023	* NMA 2415 D	C	4	2.0000	8	0	0	0	8
99012070	* HEXDIP	C	4	4.0000	95	0	0	0	95
99020007	RES. 270 OHM 1/4W 5%	C	4	4.0000	2450	0	0	0	2450
99020008	RES. 330 OHM 1/4W 5%	C	4	8.0000	473	0	0	0	473
99020013	RES. 1 K 1/4W 5%	C	4	2.0000	2368	0	0	0	2368
99020030	RES. 100 K 1/4W 5%	C	4	4.0000	936	0	0	0	936
99020038	RES. 47 OHM 1/4W 5%	C	4	4.0000	1283	0	0	0	1283
99020203	RES. 10 K 1/4W 1%	C	4	11.0000	729	0	0	0	729
99020225	* RES. 200 OHM 1%	C	4	1.0000	1014	0	0	0	1014
99020803	KOND.104K 2 MODUL	C	4	8.0000	4292	0	0	0	4292
99020811	* KOND. 3.3 UF 5%	C	4	8.0000	492	0	0	0	492
99020812	* KOND. 470 NF 5%	C	4	5.0000	501	0	0	0	501
99020835	KOND.POLY. 100V	C	4	3.0000	269	0	0	0	269
99020950	METAL KON. 10uF/16V	C	4	7.0000	107	0	0	0	107

IKKE ALLE KOMPONENTER MONTERES I STANDARD VERSIONEN, SE TEKST.

Name	Type	Pos
C1	10uF/16V Sol.Al	E8
C2	10uF/16V Sol.Al	G8
C3	10uF/16V Sol.Al	A8
C4	10uF/16V Sol.Al	B8
C5	470nF ker.	D6
C6	1uF/40V Sol.Al	C7
C7	1uF/40V Sol.Al	A12
C11	3n3 ker.	C6
C12	3n3 ker.	B7
C13	470nF ker.	B8
C14	100 nF	B11
C15	100 nF	B11
C17	10uF/16V Sol.Al	A2
C18	100 nF	A4
C19	100 nF	H2
C20	100 nF	H6
C21	3n3 ker.	D6
C22	3n3 ker.	B7
C23	470nF ker.	D8
C24	100 nF	B11
C25	100 nF	C11
C31	3n3 ker.	F6
C32	3n3 ker.	F7
C33	470nF ker.	G8
C34	100 nF	F11
C35	100 nF	F11
C41	3n3 ker.	G6
C42	3n3 ker.	G7
C43	470nF ker.	H8
C44	100 nF	F11
C45	100 nF	G11
C50	1uF/40V Sol.Al	H9
C51	10uF/16V Sol.Al	H3
C52	10uF/16V Sol.Al	A2
D11	1N4148	E11
D12	1N4148	D11
D13	BZX85C16	B9
D14	1N4148	C12
D15	1N4148	C12
D21	1N4148	B12
D22	1N4148	B11
D23	BZX85C16	B9
D24	1N4148	D12
D25	1N4148	D12
D31	1N4148	H12
D32	1N4148	H11
D33	BZX85C16	F9
D34	1N4148	E12
D35	1N4148	E12
D41	1N4148	H12
D42	1N4148	H12
D43	BZX85C16	G9
D44	1N4148	G12
D45	1N4148	G12
IC1	74LS136N	F2
IC2	74LS136N	F2
IC3	74ALS00N	C2
IC4	74ALS74AN	D2
IC5	74ALS573N	E4
IC6	74ALS138N	E2
IC7	AD1403N	B2
IC8	LF356N	B4
IC9	NMA2415D	E6
IC10	NMA2415D	D6
IC11	DAC1230LCJ-1	C4
IC12	LF356N	B5
IC13	ISO122P	B6
IC14	XTR110P	B9
IC15	LM358N	D10
IC16	IRFD9110	B11
IC17	HSSR-8200	B8
IC21	DAC1230LCJ-1	D4
IC22	LF356N	B5
IC23	ISO122P	C6
IC24	XTR110P	C9
IC26	IRFD9110	C11
IC27	HSSR-8200	C8
IC31	DAC1230LCJ-1	F4

Name	Type	Pos
IC32	LF356N	H4
IC33	ISO122P	F6
IC34	XTR110P	F9
IC35	LM358N	E10
IC36	IRFD9110	F11
IC37	HSSR-8200	F8
IC41	DAC1230LCJ-1	G4
IC42	LF356N	H5
IC43	ISO122P	H6
IC44	XTR110P	H9
IC46	IRFD9110	H11
IC47	HSSR-8200	H8
IC50	74ALS642	F4
IC51	75447	B2
L1	Inductor	A12
P	EURO conn	A13
RA	196k MR25 1% (option	A6
RB	196k MR25 1% (option	C6
RC	196k MR25 1% (option	F6
RD	196k MR25 1% (option	F6
R1	8x10k	G2
R5	1k	G2
R6	10k MR25 1%	B2
R7	10k MR25 1%	B2
R8	10k MR25 1%	A4
R9	~~332R~~ MR25 1% 200R	B4
R10	~~1k~~ 820R	A9
R11	1k00 MR25 1%	A6
R12	1k00 MR25 1%	B8
R13	10k MR25 1%	D11
R14	330R	B12
R15	47R	B12
R16	10k MR25 1%	D11
R17	330R	D9
R18	100K	D9
R19	270R	A12
R20	~~1k~~ 820R	B9
R21	1k00 MR25 1%	B6
R22	1k00 MR25 1%	C8
R23	10k MR25 1%	D11
R24	330R	D12
R25	47R	D12
R26	10k MR25 1%	C9
R27	330R	D9
R28	100K	D9
R29	270R	B11
R30	~~1k~~ 820R	E9
R31	1k00 MR25 1%	E6
R32	1k00 MR25 1%	F8
R33	10k MR25 1%	E9
R34	330R	E12
R35	47R	E12
R36	10k MR25 1%	E11
R37	330R	E9
R38	100K	D9
R39	270R	G11
R40	~~1k~~ 820R	G9
R41	1k00 MR25 1%	G6
R42	1k00 MR25 1%	H8
R43	10k MR25 1%	E11
R44	330R	F12
R45	47R	F12
R46	10k MR25 1%	E11
R47	330R	E9
R48	100K	E9
R49	270R	H12
R50	1k	G2
SW1	DIL switch 4 el. 8	H2
S11	Strap	A10
S12	Strap	A11
S21	Strap	B10
S22	Strap	B11
S31	Strap	E10
S32	Strap	E11
S41	Strap	G10
S42	Strap	G11
TP12	Test point	B10
TP22	Test point	C10

Name	Type	Pos
TP32	Test point	F10
TP42	Test point	H10
TR11	Trimmepotm. 1k	C6
TR12	Trimmepotm. 20k	B6
TR13	Trimmepotm. 20k	D8
TR14	Trimmepotm. 20k	B10
TR21	Trimmepotm. 1k	D6
TR22	Trimmepotm. 20k	B6
TR23	Trimmepotm. 20k	D8
TR24	Trimmepotm. 20k	D10
TR31	Trimmepotm. 1k	F6
TR32	Trimmepotm. 20k	H6
TR33	Trimmepotm. 20k	E8
TR34	Trimmepotm. 20k	G10
TR41	Trimmepotm. 1k	G6
TR42	Trimmepotm. 20k	H6
TR43	Trimmepotm. 20k	E8
TR44	Trimmepotm. 20k	H10
X	EURO conn	H1

Component locations

PCB: 6017 / D-A | Issue: 1 | Date: 900228

dansk data elektronik a/s
herlev hovedgade 199, 2730 herlev, tlf 02-84 50 11

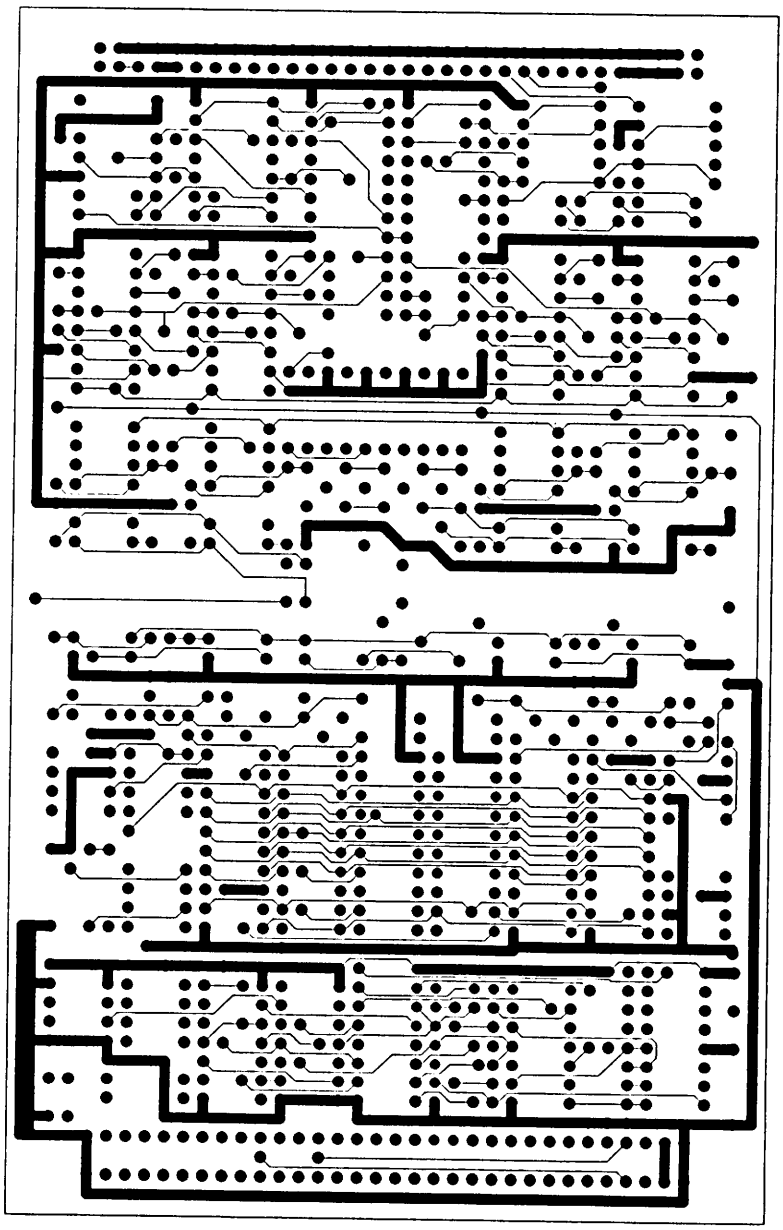
M/Can

1373 MIK

V/Can 1325

11104 – MK

Printlayout: Komponentside



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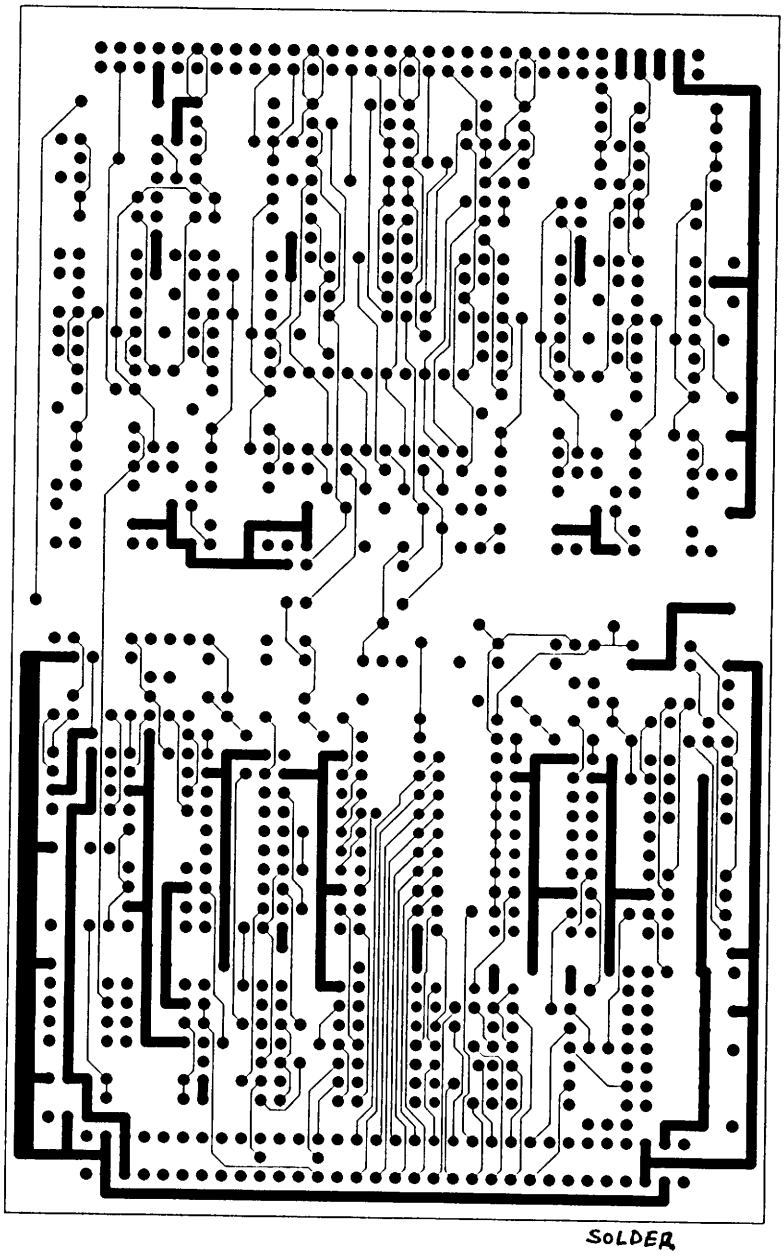


Forbindelser til bus: X konnector.

Pin:	a	c
1	+ 5 V	+ 5 V
2	GND	GND
3	+12 V	+12 V
4	*RESET*	CLK
5		
6		
7		
8		
9	A7	A6
10	A5	A4
11	A3	A2
12	A1	A0
13	IA3	IA2
14	IA1	IA0
15	D7	D6
16	D5	D4
17	D3	D2
18	D1	D0
19		
20	*INR*	*OUTR*
21		
22		
23		
24		
25		
26		
27		
28		
29		
30	-12 V	-12 V
31	GND	GND
32	+ 5 V	+ 5 V

Forbindelser til stik: P konnector.

Pin:	a	b
1		
2	GND	+V Loop
3	GND	+V Loop
4	GND	+V Conv.
5	GND	+V conv.
6	GND	
7	GND	
8	GND	
9	GND	
10	GND	I out ch 1
11	GND	V out ch 1
12	GND	
13	GND	
14	GND	I out ch 2
15	GND	V out ch 2
16	GND	
17	GND	
18	GND	I out ch 3
19	GND	V out ch 3
20	GND	
21	GND	
22	GND	I out ch 4
23	GND	V out ch 4
24	GND	
25	GND	
26	GND	
27	GND	
28	GND	GND (Conv. retur)
29	GND	GND (Conv. retur)
30	GND	GND (Loop retur)
31	GND	GND (Loop retur)
32		

National Semiconductor Corporation

MICRO-DAC™ DAC1208, DAC1209, DAC1210, DAC1230, DAC1231, DAC1232 12-Bit, μP Compatible, Double-Buffered D to A Converters

General Description

The DAC1208 and the DAC1230 series are 12-bit multiplying D to A converters designed to interface directly with a wide variety of microprocessors (8080, 8048, 8085, Z-80, etc.). Double buffering input registers and associated control lines allow these DACs to appear as a two-byte "stack" in the system's memory or I/O space with no additional interfacing logic required.

The DAC1208 series provides all 12 input lines to allow single buffering for maximum throughput when used with 16-bit processors. These input lines can also be externally configured to permit an 8-bit data interface. The DAC1230 series can be used with an 8-bit data bus directly as it internally formulates the 12-bit DAC data from its 8 input lines. All of these DACs accept left-justified data from the processor.

The analog section is a precision silicon-chromium (Si-Cr) R-2R ladder network and twelve CMOS current switches. An inverted R-2R ladder structure is used with the binary weighted currents switched between the I_{OUT1} and I_{OUT2} maintaining a constant current in each ladder leg independent of the switch state. Special circuitry provides TTL logic input voltage level compatibility.

The DAC1208 series and DAC1230 series are the 12-bit members of a family of microprocessor compatible DACs (MICRO-DACs™). For applications requiring other resolutions, the DAC1000 series for 10-bit and DAC0830 series for 8-bit are available alternatives.

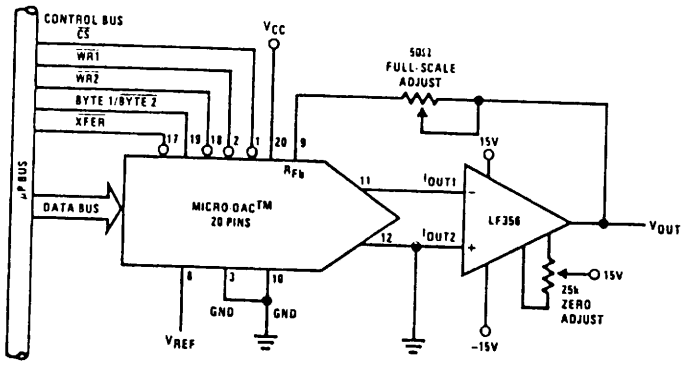
Features

- Linearity specified with zero and full-scale adjust only
- Direct interface to all popular microprocessors
- Double-buffered, single-buffered or flow through digital data inputs
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Works with ±10V reference—full 4-quadrant multiplication
- Operates stand-alone (without μP) if desired
- All parts guaranteed 12-bit monotonic
- DAC1230 series is pin compatible with the DAC0830 series 8-bit MICRO-DACs

Key Specifications

■ Current Settling Time	1 μs
■ Resolution	12 Bits
■ Linearity (Guaranteed over temperature)	10, 11, or 12 Bits of FS
■ Gain Tempco	1.3 ppm/°C
■ Low Power Dissipation	20 mW
■ Single Power Supply	5 V_{DC} to 15 V_{DC}

Typical Application



TL/H/5690–1

Absolute Maxim

If Military/Aerospace sp
contact the National S
Distributors for availabili
(Notes 1 and 2)
Supply Voltage (V_{CC})
Voltage at Any Digital Inpu
Voltage at V_{REF} Input
Storage Temperature Ran
Package Dissipation at T_A
(Note 3)
DC Voltage Applied to I_{OU}
(Note 4)
ESD Susceptability

Electrical Chara

V_{REF} = 10.000 V_{DC}, V_{CC}
Note 13); all other limits

Parameter
Resolution
Linearity Error (End Point Linearity)
Differential Non-Linearity
Monotonicity
Gain Error (Min)
Gain Error (Max)
Gain Error Tempco
Power Supply Rejection
Reference Input Resistar
Reference Input Resistar
Output Feedthrough Erro
Output Capacitance
Supply Current Drain
Output Leakage Current I_{OUT1}
I_{OUT2}
Digital Input Threshold
Digital Input Currents

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Notes 1 and 2)

Supply Voltage (V_{CC})	17 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND
Voltage at V_{REF} Input	±25V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C (Note 3)	500 mW
DC Voltage Applied to I_{OUT1} or I_{OUT2} (Note 4)	−100 mV to V_{CC}
ESD Susceptability	800V

Operating Conditions

Lead Temperature (Soldering, 10 seconds)	300°C
Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC1208LCJ, DAC1209LCJ, DAC1210LCJ, DAC1230LCJ, DAC1231LCJ, DAC1232LCJ	$-40°C \le T_A \le +85°C$
DAC1208LCJ-1, DAC1209LCJ-1, DAC1210LCJ-1, DAC1230LCJ-1, DAC1231LCJ-1, DAC1232LCJ-1	$0°C \le T_A \le +70°C$
Range of V_{CC}	4.75 V_{DC} to 16 V_{DC}
Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics

V_{REF} = 10.000 V_{DC}. V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted. **Boldface limits apply from T_{MIN} to T_{MAX} (see Note 13);** all other limits $T_A = T_J$ = 25°C.

Parameter	Conditions	Notes	Typ (Note 10)	Tested Limit (Note 5)	Design Limit (Note 6)	Units
Resolution			12	**12**	**12**	Bits
Linearity Error (End Point Linearity)	Zero and Full-Scale Adjusted DAC1208, DAC1230 DAC1209, DAC1231 DAC1210, DAC1232	4, 7, 13		 **0.012** **0.024** **0.050**	 **0.012** **0.024** **0.05**	 % of FSR % of FSR % of FSR
Differential Non-Linearity	Zero and Full-Scale Adjusted DAC1208, DAC1230 DAC1209, DAC1231 DAC1210, DAC1232	4, 7, 13		 **0.018** **0.024** **0.050**	 **0.018** **0.024** **0.05**	 % of FSR % of FSR % of FSR
Monotonicity		4	12	**12**	**12**	Bits
Gain Error (Min)	Using Internal R_{Fb} V_{ref} = ±10V, ±1V	7	−0.1	0.0		% of FSR
Gain Error (Max)		7	−0.1	−0.2		% of FSR
Gain Error Tempco		7	±1.3		**±6.0**	ppm of FS/°C
Power Supply Rejection	All Digital Inputs Latched High	7	±3.0	±30		ppm of FSR/V
Reference Input Resistance (Min) Reference Input Resistance (Max)		13	15 15	**10** **20**	**10** **20**	kΩ
Output Feedthrough Error	V_{REF} = 20 Vp-p, f = 100 kHz All Data Inputs Latched Low	9	3.0			mVp-p
Output Capacitance	All Data Inputs Latched High I_{OUT1} All Data Inputs Latched High I_{OUT2} All Data Inputs Latched Low I_{OUT1} All Data Inputs Latched Low I_{OUT2}				200 70 70 200	pF pF pF pF
Supply Current Drain		13		2.0	**2.5**	mA
Output Leakage Current I_{OUT1}	All Data Inputs Latched Low	11, 13	0.1	**15**	**15**	nA
Output Leakage Current I_{OUT2}	All Data Inputs Latched High	11, 13	0.1	**15**	**15**	nA
Digital Input Threshold	Low Threshold High Threshold	13 13		**0.8** **2.2**	**0.8** **2.2**	V_{DC} V_{DC}
Digital Input Currents	Digital Inputs <0.8V Digital Inputs >2.2V	13 13		**−200** **10**	**−200** **10**	μA_{DC} μA_{DC}

Electrical Characteristics (Continued)

V_{REF} = 10.000 V_{DC}, V_{CC} = 11.4 V_{DC} to 15.75 V_{DC} unless otherwise noted. **Boldface limits apply from T_{MIN} to T_{MAX} (see Note 13);** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	See Note	Typ (Note 10)	Tested Limit (Note 5)	Design Limit (Note 6)	Units
AC CHARACTERISTICS							
t_s	Current Setting Time	V_{IL} = 0V, V_{IH} = 5V		1.0			µs
t_W	Write and XFER Pulse Width Min.	V_{IL} = 0V, V_{IH} = 5V	8	50		320 **320**	ns
t_{DS}	Data Setup Time Min.	V_{IL} = 0V, V_{IH} = 5V		70		320 **320**	ns
t_{DH}	Data Hold Time Min.	V_{IL} = 0V, V_{IH} = 5V		30		90 **90**	ns
t_{CS}	Control Setup Time Min.	V_{IL} = 0V, V_{IH} = 5V		60		320 **320**	ns
t_{CH}	Control Hold Time Min.	V_{IL} = 0V, V_{IH} = 5V		0		10	ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: This 500 mW specification applies for all packages. The low intrinsic power dissipation of this part (and the fact that there is no way to significantly modify the power dissipation) removes concern for heat sinking.

Note 4: Both I_{OUT1} and I_{OUT2} must go to ground or the virtual ground of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if V_{REF} = 10V then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.

Note 5: Tested and guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 6: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels. Guaranteed for V_{CC} = 11.4V to 15.75V and V_{REF} = −10V to +10V.

Note 7: The unit FSR stands for full-scale range. Linearity Error and Power Supply Rejection specs are based on this unit to eliminate dependence on a particular V_{REF} value to indicate the true performance of the part. The Linearity Error specification of the DAC1208 is 0.012% of FSR(max). This guarantees that after performing a zero and full-scale adjustment, the plot of the 4096 analog voltage outputs will each be within 0.012% × V_{REF} of a straight line which passes through zero and full-scale. The unit ppm of FSR(parts per million of full-scale range) and ppm of FS(parts per million of full-scale) are used for convenience to define specs of very small percentage values, typical of higher accuracy converters. In this instance, 1 ppm of FSR = $V_{REF}/10^6$ is the conversion factor to provide an actual output voltage quantity. For example, the gain error tempco spec of ±6 ppm of FS/°C represents a worst-case full-scale gain error change with temperature from −40°C to +85°C of ±(6)($V_{REF}/10^6$)(125°C) or ±0.75 (10^{-3}) V_{REF} which is ±0.075% of V_{REF}.

Note 8: This spec implies that all parts are guaranteed to operate with a write pulse or transfer pulse width (t_W) of 320 ns. A typical part will operate with t_W of only 100 ns. The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH} and t_S to apply.

Note 9: To achieve this low feedthrough in the D package, the user must ground the metal lid. If the lid is left floating the feedthrough is typically 6 mV.

Note 10: Typicals are at 25°C and represent the most likely parametric norm.

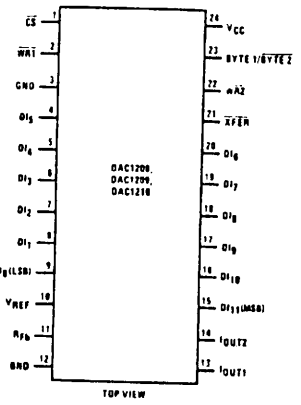
Note 11: A 10 nA leakage current with R_{Fb} = 20k and V_{REF} = 10V corresponds to a zero error of (10 × 10^{-9} × 20 × 10^3) × 100% 10V or 0.002% of FS.

Note 12: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

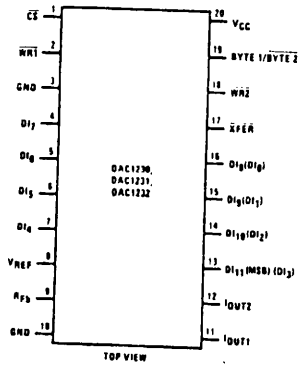
Note 13: Tested limit for −1 suffix parts applies only at 25°C.

Connection Diagrams

Dual-In-Line Package



Dual-In-Line Package



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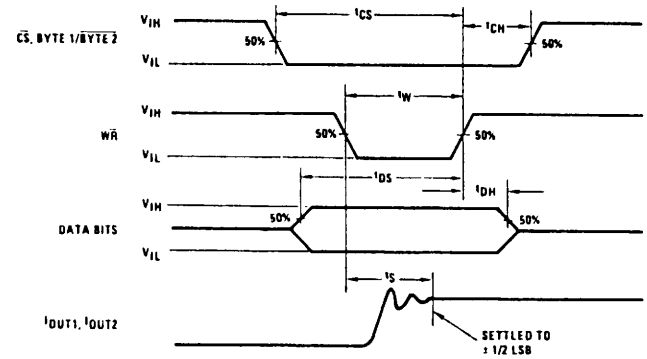
See Ordering Information

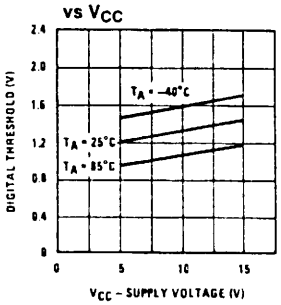
Switching Waveforms



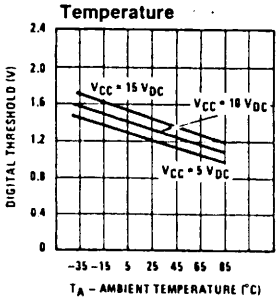
TL/H/5690-3

Typical Performance Characteristics

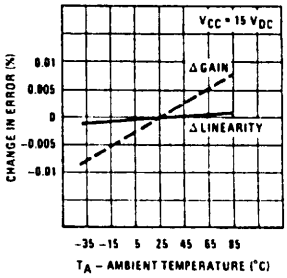
Digital Input Threshold vs V_{CC}



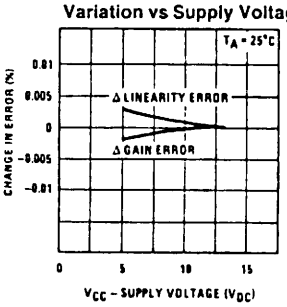
Digital Input Threshold vs Temperature



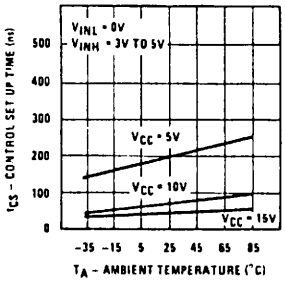
Gain and Linearity Error Variation vs Temperature



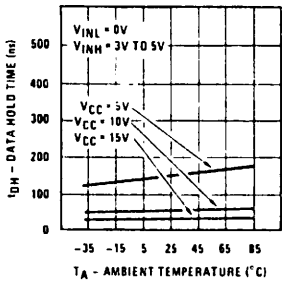
Gain and Linearity Error Variation vs Supply Voltage



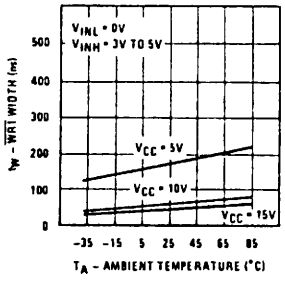
Control Set-Up Time, t_{CS}



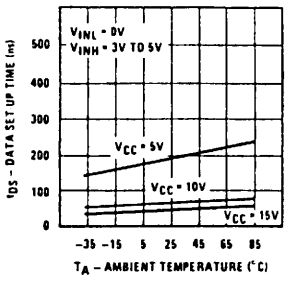
Data Hold Time, t_{DH}



Write Pulse Width, t_W



Data Set-Up Time, t_{DS}



TL/H/5690-4

Definition of Package Pinouts

CONTROL SIGNALS (all control signals are level actuated)

$\overline{CS}$: Chip Select (active low). The $\overline{CS}$ will enable $\overline{WR1}$.

$\overline{WR1}$: Write 1. The active low $\overline{WR1}$ is used to load the digital data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR1}$ is high. The 12-bit input latch is split into two latches. One holds the first 8 bits, while the other holds 4 bits. The Byte 1/$\overline{\text{Byte 2}}$ control pin is used to select both latches when Byte 1/$\overline{\text{Byte 2}}$ is high or to overwrite the 4-bit input latch when in the low state.

Byte 1/$\overline{\text{Byte 2}}$: Byte Sequence Control. When this control is high, all 12 locations of the input latch are enabled. When low, only the four least significant locations of the input latch are enabled.

$\overline{WR2}$: Write 2 (active low). The $\overline{WR2}$ will enable $\overline{XFER}$.

$\overline{XFER}$: Transfer Control Signal (active low). This signal, in combination with $\overline{WR2}$, causes the 12-bit data which is available in the input latches to transfer to the DAC register.

DI_0 to DI_{11}: Digital Inputs. DI_0 is the least significant digital input (LSB) and DI_{11} is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital code of all 1s in the DAC register, and is zero for all 0s in the DAC register.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1}, or $I_{OUT1} + I_{OUT2} = \text{constant}$ (for a fixed reference voltage). This constant current is

$$V_{REF} \times \left(1 - \frac{1}{4096}\right)$$

divided by the reference input resistance.

R_{Fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of 10V to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from 5 V_{DC} to 15 V_{DC}. Operation is optimum for 15 V_{DC}.

GND: Pins 3 and 12 of the DAC1208, DAC1209, and DAC1210 must be connected to ground. Pins 3 and 10 of the DAC1230, DAC1231, and DAC1232 must be connected to ground. It is important that I_{OUT_1} and I_{OUT_2} are at ground potential for current switching applications. Any difference of potential (V_{OS} on these pins) will result in a linearity change of

$$\frac{V_{OS}}{3\,V_{REF}}$$

For example, if V_{REF} = 10V and these ground pins are 3 mV offset from I_{OUT_1} and I_{OUT_2}, the linearity change will be 0.03%.

Definition of Terms

Resolution: Resolution is defined as the reciprocal of the number of discrete steps in the DAC output. It is directly related to the number of switches or bits within the DAC. For example, the DAC1208 has 2^{12} or 4096 steps and therefore has 12-bit resolution.

Linearity Error: Linearity error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic.* It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

National's linearity test (a) and the best straight line test (b) used by other suppliers are illustrated below. The best straight line (b) requires a special zero and FS adjustment for each part, which is almost impossible for the user to determine. The end point test uses a standard zero FS adjustment procedure and is a much more stringent test for DAC linearity.

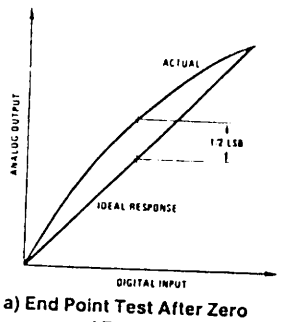
Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Full-scale current settling time requires zero to full-scale or full-scale to zero output change. Settling time is the time required from a code transition until the DAC output reaches within ± ½ LSB of the final output value.

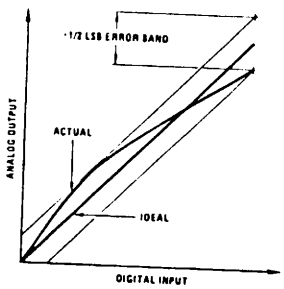
Full-Scale Error: Full-scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC1208 or DAC1230 series, full-scale is $V_{REF} - 1$ LSB. For V_{REF} = 10V and unipolar operation, $V_{FULL\text{-}SCALE} = 10.0000V - 2.44\ mV = 9.9976V$. Full-scale error is adjustable to zero.

Differential Non-Linearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB is differential non-linearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. A 12-bit DAC which is monotonic to 12 bits simply means that input increasing digital input codes will produce an increasing analog output.



a) End Point Test After Zero and FS Adjust



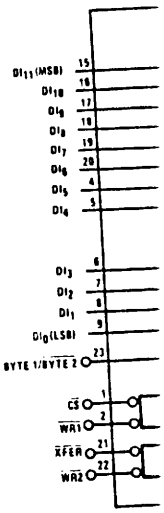
b) Shifting FS Adjust to Pass Best Straight Line Test

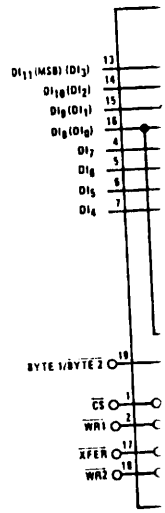
TL/H/5690-5

Application Hints

DIGITAL INTERFACE

These DACs are designed to pro
digital input circuitry to permit a
variety of microprocessor system
of convention of the input control
be treated as a typical memory de
no external logic required in n
these DACs can be mapped as a
(or I/O space) to receive their 1
successive 8-bit data writing seq
also is intended for use in syste
The DAC1208 series provides all
can be externally configured to
bus or can be driven directly fro





BURR-BROWN®

ISO122P

ADVANCE INFORMATION
SUBJECT TO CHANGE

Precision Lowest Cost ISOLATION AMPLIFIER

FEATURES

- 100 % TESTED FOR HIGH-VOLTAGE BREAKDOWN
- RATED 1500 Vrms
- HIGH IMR: 140dB at 60Hz
- BIPOLAR OPERATION: V_O = ±10V
- SINGLE-WIDE 16-PIN PLASTIC DIP
- EASE OF USE: Fixed Unity Gain Configuration

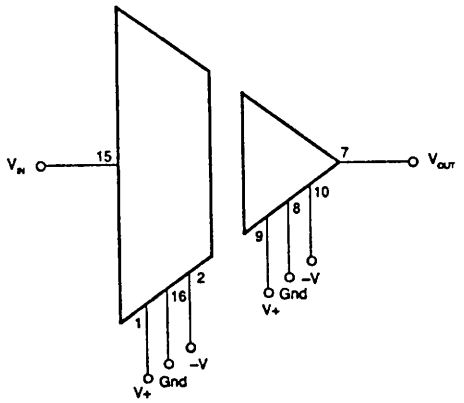
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL: Transducer Isolator, Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4mA to 20mA Loop Isolation
- GROUND LOOP ELIMINATION
- MOTOR AND SCR CONTROL
- POWER MONITORING
- PC-BASED DATA ACQUISITION
- TEST EQUIPMENT
- VENDING MACHINES

DESCRIPTION

The ISO122P is a precision isolation amplifier incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2pF differential capacitive barrier. With digital modulation the barrier characteristics do not affect signal integrity, resulting in excellent reliability and good high frequency transient immunity across the barrier. Both barrier capacitors are imbedded in the plastic body of the package.

The ISO122P is easy to use. No external components are required for operation. The key specification of 0.01% max nonlinearity is guaranteed, with up to 50kHz signal bandwidth and 200µV/°C max V_{OS} drift typical. A power supply range of ±4.5V to ±18V and quiescent current of ±4.5mA on V_{S1} and ±4.5mA on V_{S2} make these amplifiers ideal for a wide range of applications.



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Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491 • FAX: (602) 889-1510

PDS-857

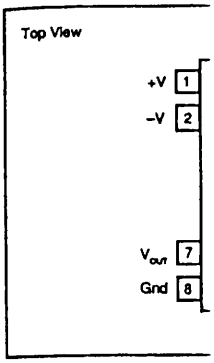
SPECIFICATIONS

At T_A = 25°C and V_s1 = V_s2 = ±15V unless otherwise noted.

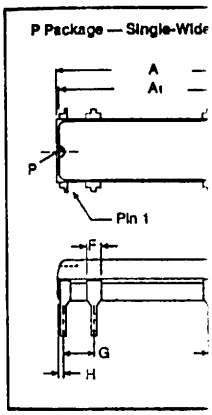
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ISOLATION					
Voltage Rated Continuous AC 60Hz		1500			VAC
100% Test 1	1s, 5pc PD	2400			VAC
Isolation Mode Rejection			140		dB
Barrier Impedance			10^{14} || 2		Ω || pF
Leakage Current at 60Hz	V_{iso} = 240Vrms		0.18	0.5	µArms
GAIN	V_o = ±10V				
Nominal Gain			1		V/V
Gain Error			±.05	±.30	%FSR
Gain vs Temperature			±10		ppm/°C
Nonlinearity			±.008	±.015	%FSR
INPUT OFFSET VOLTAGE					
Initial Offset			±5	±50	mV
vs Temperature			±200		µV/°C
vs Supply			±2		mV/V
Noise			4		µV/√Hz
INPUT					
Voltage Range		±10			V
Resistance			200		kΩ
OUTPUT					
Voltage Range		±10	±12		V
Current Drive		±5	±15		mA
Capacitive Load Drive			1000		pF
Ripple Voltage[2]			10		mVp-p
FREQUENCY RESPONSE					
Small Signal Bandwidth			50		kHz
Slew Rate	V_o = ±10V		1.5		V/µs
Settling Time					
0.1%			50		µs
0.01%			150		µs
Overload Recover Time			150		µs
POWER SUPPLIES					
Rated Voltage			15		V
Voltage Range		±4.5		±18	V
Quiescent Current: V_{s1}			±4.5	±6.5	mA
V_{s2}			±4.5	±6.5	mA
TEMPERATURE RANGE					
Specification		0		70	°C
Operating		–25		85	°C
Storage		–25		85	°C
θ_{JA}			100		°C/W

NOTES: (1) Tested at 1.4 X rated, fail on 5pC partial discharge leakage current on five successive pulses. (2) Ripple frequency is at carrier frequency (500kHz).

CONNECTION DIAGR



MECHANICAL



THEORY OF

The ISO122P isolation a
section galvanically iso
pacitors built into the
cycle modulated and tra
The output section rece
it back to an analog volta
inherent in the demodul
fabricated, then laser trin
ing common to both in
are then mounted on o
isolating capacitors m

MODULATOR

An input amplifier (A1
between the input curren
current source. This c
switchable 200µA sour

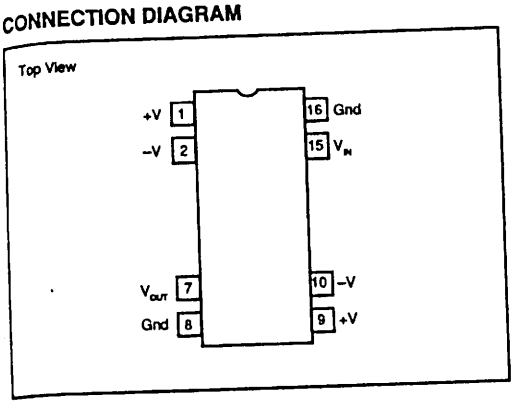
CHANGE

UNITS
VAC
VAC
dB
Ω || pF
µArms
V/V
%FSR
ppm/°C
%FSR
mV
µV/°C
mV/V
µV/√Hz
V
V
mA
pF
mVp-p
kHz
V/µs
µs
µs
µs
V
V
mA
mA
°C
°C
°C
°C/W

2) Ripple frequency

ADVANCE INFORMATION SUBJECT TO CHANGE

CONNECTION DIAGRAM

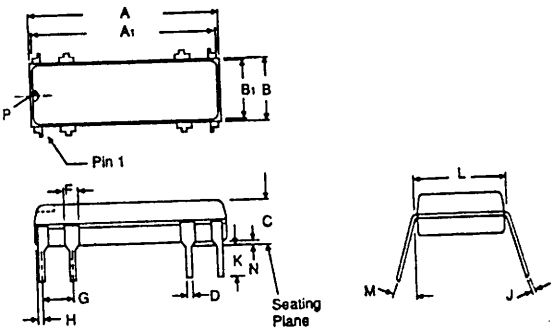


ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
V_{IN}	±100V
Continuous Isolation Voltage	1500Vrms
V_{ISO} dv/dt	20kV/µs
Junction Temperature	+150°C
Storage Temperature	+85°C
Lead Temperature (soldering, 10s)	+300°C
Output Short to Common	Continuous

MECHANICAL

P Package — Single-Wide 16-Pin Plastic DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.740	.800	18.80	20.32
A1	.725	.785	18.42	19.94
B	.230	.290	5.85	7.38
B1	.200	.250	5.09	6.36
C	.120	.200	3.05	5.09
D	.015	.023	0.38	0.59
F	.030	.070	0.76	1.78
G	.100 BASIC		2.54 BASIC	
H	0.20	.050	0.51	1.27
J	.008	.015	0.20	0.38
K	.070	.150	1.78	3.82
L	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.010	.030	0.25	0.76
P	.025	.050	0.64	1.27

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane. Pin numbers shown for reference only. Numbers may not be marked on package.

THEORY OF OPERATION

The ISO122P isolation amplifier uses an input and an output section galvanically isolated by matched 1pF isolating capacitors built into the plastic package. The input is duty-cycle modulated and transmitted digitally across the barrier. The output section receives the modulated signal, converts it back to an analog voltage and removes the ripple component inherent in the demodulation. Input and output sections are fabricated, then laser trimmed for exceptional circuitry matching common to both input and output sections. The sections are then mounted on opposite ends of the package with the isolating capacitors mounted between the two sections.

MODULATOR

An input amplifier (A1, Figure 1) integrates the difference between the input current (V_{IN}/200kΩ) and a switched ±100µA current source. This current source is implemented by a switchable 200µA source and a fixed 100µA current sink.

To understand the basic operation of the modulator, assume that V_{IN} = 0.0V. The integrator will ramp in one direction until the comparator threshold is exceeded. The comparator and sense amp will force the current source to switch; the resultant signal is a triangular waveform with a 50% duty cycle. The internal oscillator forces the current source to switch at the 500kHz frequency. If V_{IN} changes, the duty cycle of the integrator will change to keep the average DC value at the output of A1 near zero volts

DEMODULATOR

The sense amplifier drives a switched current source into integrator A2. The output stage balances the duty-cycle modulated current against the feedback current through the 200kΩ feedback resistor, resulting in an average value at the V_{OUT} pin equal to V_{IN}. The sample and hold amplifiers in the output feedback loop serve to remove undesired ripple voltages inherent in the demodulation process.

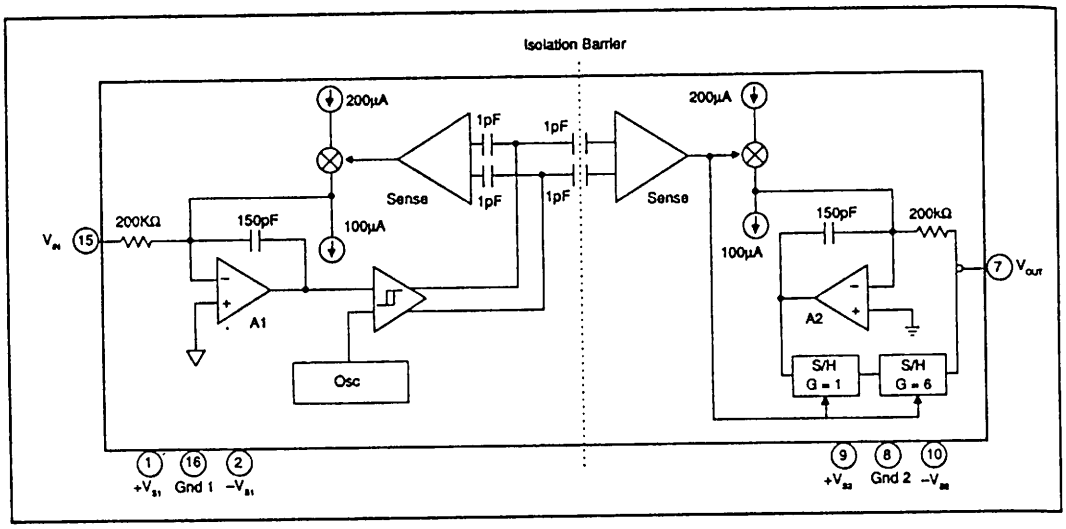


FIGURE 1. Block Diagram.

BASIC OPERATION

SIGNAL AND POWER CONNECTIONS

Each power supply pin should be bypassed with 1µF tantalum capacitors located as close to the amplifier as possible. The internal frequency of the modulator/demodulator is set at 500kHz by an internal oscillator. Therefore if it is desired to minimize any feedthrough noise (beat frequencies) from a DC/DC converter, use a pie filter on the supplies (See Figure 2).

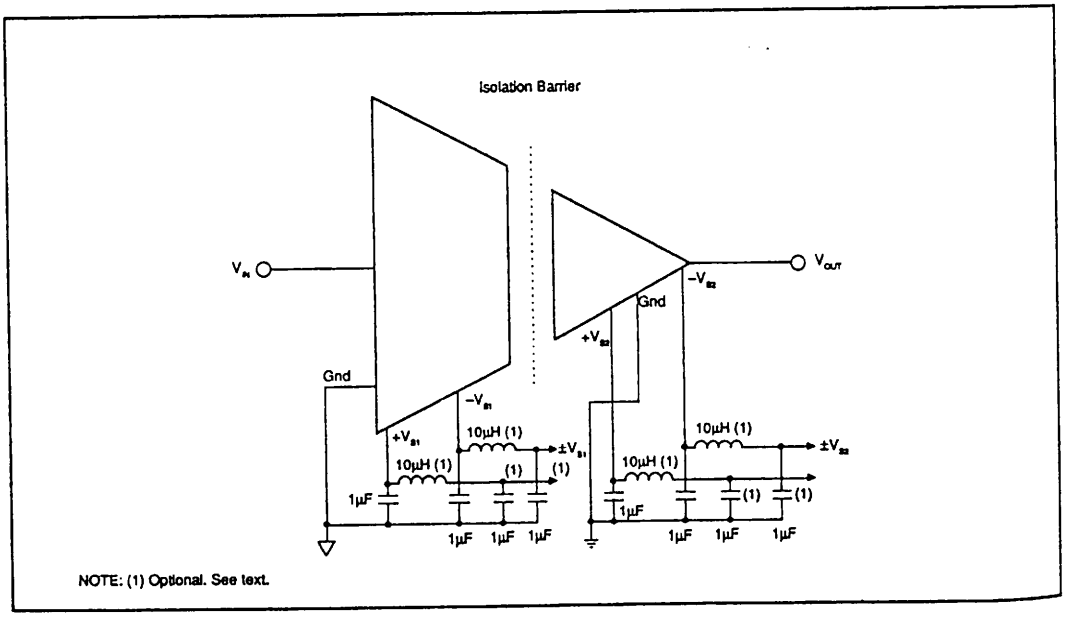


FIGURE 2. Applications Figure.

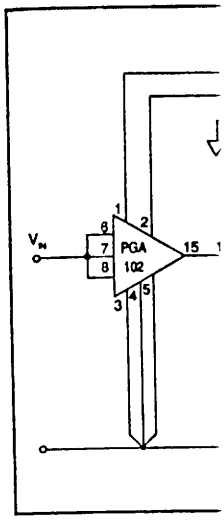


FIGURE 3. Programmat
Gains of 1, 1

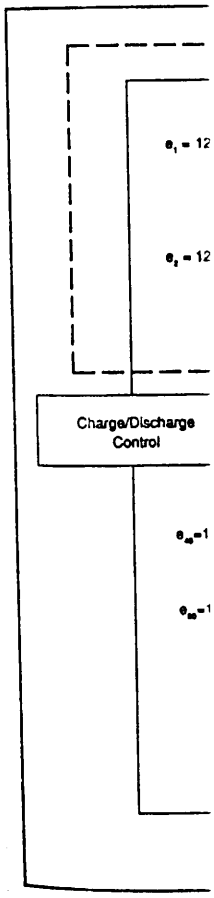
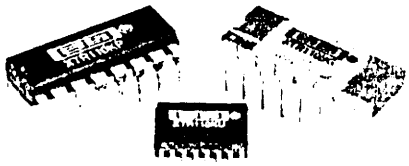


FIGURE 4. Battery M

BURR-BROWN®

XTR110



PRECISION VOLTAGE-TO-CURRENT CONVERTER/TRANSMITTER

FEATURES

- 4mA TO 20mA TRANSMITTER
- SELECTABLE INPUT/OUTPUT RANGES:
  0V to +5V, 0V to +10V Inputs
  0mA to 20mA, 5mA to 25mA Outputs
  Other Ranges
- 0.005% MAX NONLINEARITY, 14 BIT
- PRECISION +10V REFERENCE OUTPUT
- SINGLE SUPPLY OPERATION
- CURRENT SOURCING TO COMMON
- WIDE SUPPLY RANGE, 13.5V TO 40V

APPLICATIONS

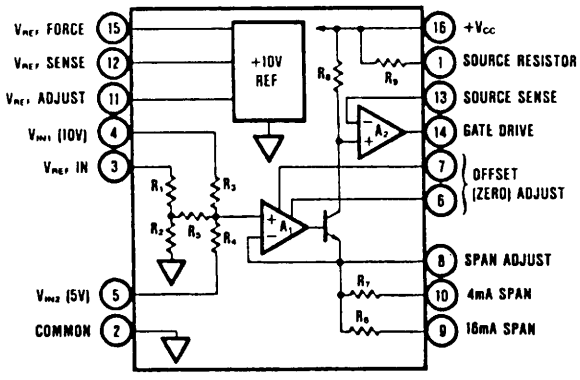
- INDUSTRIAL PROCESS CONTROL
- PRESSURE/TEMPERATURE TRANSMITTERS
- CURRENT-MODE BRIDGE EXCITATION
- GROUNDED TRANSDUCER CIRCUITS
- CURRENT SOURCE REFERENCE FOR DATA ACQUISITION
- PROGRAMMABLE CURRENT SOURCE FOR TEST EQUIPMENT
- AUTOMATED MANUFACTURING
- POWER PLANT/ENERGY SYSTEM MONITORING

DESCRIPTION

The XTR110 is a monolithic precision voltage-to-current converter. It can convert standard 0V to +10V or 0V to +5V inputs into 4mA to 20mA, or 5mA to 25mA outputs. The required external MOS transistor keeps heat outside the XTR110 package to optimize performance under all output conditions.

A precision +10V reference output can drive 10mA. An external transistor can be added for more current, e.g. 33mA for 300Ω bridges.

The XTR110 is a key data acquisition component, designed for high noise immunity current-mode transmission. It is also ideal as a precision programmable current source for transducer circuits and test equipment.



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PDS-555C

SPECIFICATIONS

ELECTRICAL

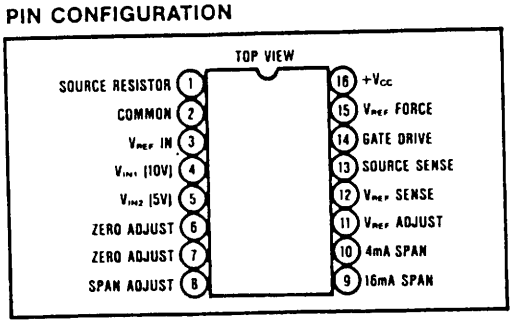
At T_A = +25°C and V_{CC} = +24V and R_L = 250Ω† unless otherwise specified.

PARAMETER	CONDITIONS	XTR110AG/KP/KU MIN	XTR110AG/KP/KU TYP	XTR110AG/KP/KU MAX	XTR110BG MIN	XTR110BG TYP	XTR110BG MAX	UNITS
TRANSMITTER								
Transfer Function			$I_O = 10\,[(V_{REF}IN/16) + (V_{IN1}/4) + (V_{IN2}/2)]/R_{SPAN}$					
Input Range: V_{IN1}[5]	Specified performance	0		+10	•	•	•	V
V_{IN2}	Specified performance	0		+5	•		•	V
Current, I_O	Specified performance[1]	4		20	•		•	mA
	Derated performance[1]	0		40	•		•	mA
Nonlinearity	16mA/20mA span[2]		0.01	0.025		0.002	0.005	% of span
Offset Current, I_{OS}	I_O = 4mA[1]		0.2	0.4		0.02	0.1	% of span
Initial	[1]		0.0003	0.005		•	0.003	% of span/°C
vs Temp	[1]		0.0005	0.005		•	•	% of span/V
vs Supply, V_{CC}	[1]							
Span Error	I_O = 20mA		0.3	0.6		0.05	0.2	% of span
Initial	[1]		0.0025	0.005		0.0009	0.003	% of span/°C
vs Temp	[1]		0.003	0.005		•	•	% of span/V
vs Supply, V_{CC}	[1]		$10 \times 10^{[9]}$			•		Ω
Output Resistance	From drain of FET (Q_{EXT})[3]		27			•		kΩ
Input Resistance	V_{IN1}		22			•		kΩ
	V_{IN2}		19			•		kΩ
	V_{REF} IN							
Dynamic Response						•		µsec
Settling Time	To 0.1% of span		15			•		µsec
	To 0.01% of span		20			•		µsec
Slew Rate			1.3			•		mA/µsec
VOLTAGE REFERENCE								
Output Voltage		+9.95	+10	+10.05	+9.98	•	+10.02	V
vs Temp			35	50		15	30	ppm/°C
vs Supply, V_{CC}	Line regulation		0.0002	0.005		•	•	%/V
vs Output Current	Load regulation		0.0005	0.01		•	•	%/mA
vs Time			100			•		ppm/1k hrs
Trim Range		−0.100		+0.25	•		•	V
Output Current	Specified performance	10			•		•	mA
POWER SUPPLY								
Input Voltage, V_{CC}		+13.5		+40	•	•	•	V
Quiescent Current	Excluding I_O		3	4.5				mA
TEMPERATURE RANGE								
Specification: AG, BG		−40		+85	•		•	°C
KP, KU		0		+70				°C
Operating: AG, BG		−55		+125	•		•	°C
KP, KU		−25		+85				°C

* Specification same as AG/KP grades. † Specifications apply to the range of R_L shown in Typical Performance Curves.

NOTES: (1) Including internal reference. (2) Span is the change in output current resulting from a full-scale change in input voltage. (3) Within compliance range limited by (+V_{CC} − 2V) +V_{DS} required for linear operation of the FET. (4) For V_{REF} adjustment circuit see Figure 4. (5) For extended I_{REF} drive circuit see Figure 8. (5) Unit may be damaged. See "Input Voltage Range" on next page.

PIN CONFIGURATION

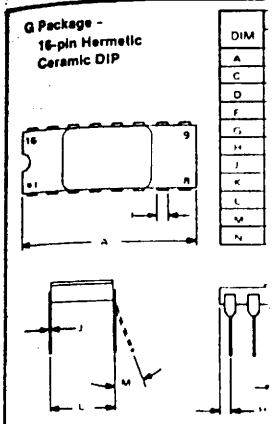


ABSOLUTE MAXIMUM RATINGS

Power Supply, +V_{CC}	40V
Input Voltage, $V_{IN\,1}$, $V_{IN\,2}$, $V_{REF\,IN}$	+V_{CC}
Storage Temperature Range: A, B	−55°C to +125°C
K, U	−40°C to +85°C
Lead Temperature (soldering, 10s) G, P	300°C
(wave soldering, 3s) U	260°C
Output Short-Circuit Duration, Gate Drive and V_{REF} Force	Continuous to common and +V_{CC}
Output Current Using Internal 50Ω Resistor	40mA

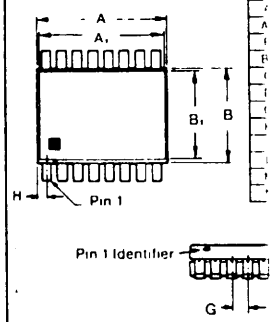
MECHANICAL

G Package - 16-pin Hermetic Ceramic DIP



NOTE: Leads in true po
(.25mm) R at MMC at s
Pin numbers shown for
Numbers may not be m

U Package - 16-pin SOIC



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane

Pin numbers shown for reference only. Numbers are not marked on package.

BURN-IN SCREENING

Burn-in screening is an option
and ceramic-packaged XTR
160 hours at the temperature s
combination of time and temp

Plastic "-BI" models: +85
Ceramic "-BI" models: +

All units are tested after bur
specifications are met. To orde
base model number.

3110BG		
TYP	MAX	UNITS
R_{SPAN}		V
		V
		mA
		mA
002	0.005	% of span
0.02	0.1	% of span
	0.003	% of span/°C
		% of span/V
0.05	0.2	% of span
0.0009	0.003	% of span/°C
		% of span/V
		Ω
		kΩ
		kΩ
		kΩ
		µsec
		µsec
		mA/µsec
	+10.02	V
6	30	ppm/°C
		%/V
		%/mA
		ppm/1k hrs
		V
		mA
		V
		mA
		°C
		°C
		°C
		°C

Curves.

change in input voltage. (3) Within circuit see Figure 4. (5) For extended

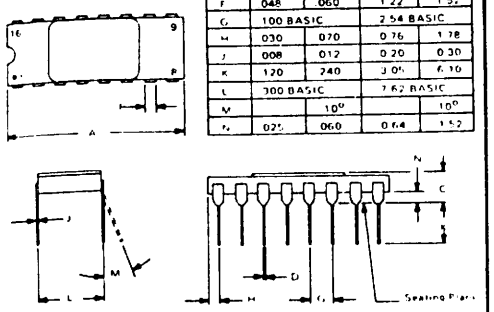
RATI

	40V
	+Vcc
B	-55°C to +125°C
U	-40°C to +85°C
	300°C
	260°C
Gate Drive	
	Continuous to common and +Vcc
00 Resistor	40mA

MECHANICAL

G Package - 16-pin Hermetic Ceramic DIP

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	790	810	20.07	20.57
C	105	170	2.67	4.32
D	015	021	0.38	0.53
F	048	060	1.22	1.52
G	100 BASIC		2.54 BASIC	
H	030	070	0.76	1.78
J	008	012	0.20	0.30
K	120	240	3.04	6.10
L	300 BASIC		7.62 BASIC	
M		10°		10°
N	025	060	0.64	1.52

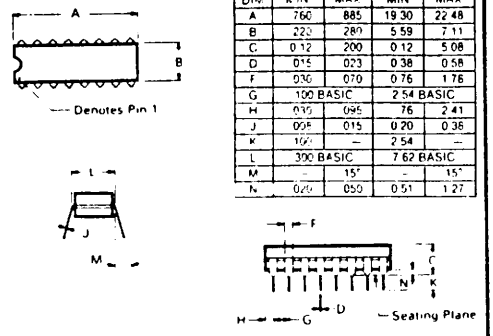


NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

P Package - 16-pin Plastic DIP

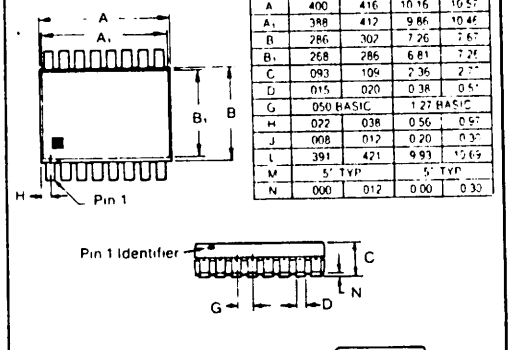
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	760	885	19.30	22.48
B	220	280	5.59	7.11
C	0.12	200	0.12	5.08
D	015	023	0.38	0.58
F	030	070	0.76	1.78
G	100 BASIC		2.54 BASIC	
H	030	095	.76	2.41
J	008	015	0.20	0.38
K	100	–	2.54	–
L	300 BASIC		7.62 BASIC	
M	–	15°	–	15°
N	020	050	0.51	1.27



NOTE
Leads in true position within 0.01" (0.25mm) R at MMC at seating plane

U Package - 16-pin SOIC

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	400	416	10.16	10.57
A_1	398	412	9.86	10.46
B	286	302	7.26	7.67
B_1	268	286	6.81	7.26
C	093	109	2.36	2.77
D	015	020	0.38	0.51
G	050 BASIC		1.27 BASIC	
H	022	038	0.56	0.97
J	008	012	0.20	0.30
L	391	421	9.93	10.69
M	5° TYP		5° TYP	
N	000	012	0.00	0.30



NOTE: Leads in true position within .010" (.25mm) R at MMC at seating plane

Pin numbers shown for reference only. Numbers are not marked on package

ORDERING INFORMATION

Model	Package	Temperature Range
XTR110AG	Ceramic DIP	-40°C to +85°C
XTR110BG	Ceramic DIP	-40°C to +85°C
XTR110KP	Plastic DIP	0°C to +70°C
XTR110KU	Plastic SOIC	0°C to +70°C

BURN-IN SCREENING OPTION
See text for details

Model	Package	Burn-In Temp. (160h)[1]
XTR110AG-BI	Ceramic DIP	+125°C
XTR110BG-BI	Ceramic DIP	+125°C
XTR110KP-BI	Plastic DIP	+85°C
XTR110KU-BI	Plastic SOIC	+85°C

NOTE: (1) Or equivalent combination. See text

BURN-IN SCREENING

Burn-in screening is an option available for both plastic- and ceramic-packaged XTR110s. Burn-in duration is 160 hours at the temperature shown below (or equivalent combination of time and temperature).

Plastic "-BI" models: +85°C
Ceramic "-BI" models: +125°C

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.

INPUT VOLTAGE RANGE

The XTR110 can be damaged if the inputs are taken below pin 2 (COMMON). Under carefully controlled conditions, the input can be allowed to go below system ground. To determine the allowable range for the input, use the following equation:

$$(V_{REF}\,IN/16) + (V_{IN1}/4) + (V_{IN2}/2) = 0$$

For example, assume that the standard configuration of Figure 1 is being used. In this case, $V_{REF}IN = 10V$ and $V_{IN2} = 0V$. The equation now becomes:

$$(10/16) + (V_{IN1}/4) + (0/2) = 0$$

Rearranging gives:

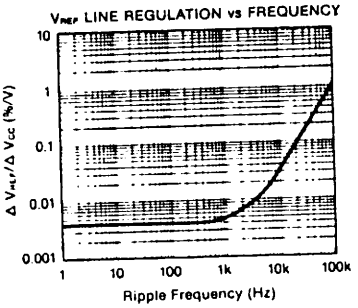
$$V_{IN1} = -2.5V$$

which is the maximum negative voltage that the input can be taken to. Note, however, that this applies only as long as there is 10V at $V_{REF}IN$. If, for example, the supply for the XTR110 is interrupted, the 10V will no longer be generated and any negative input at V_{IN1} could damage the unit.

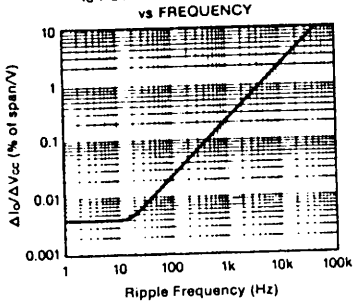
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{CC} = 24VDC, R_L = 250Ω unless otherwise noted.

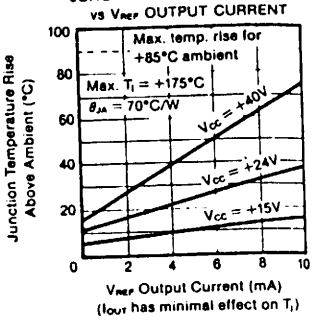
V_{REF} LINE REGULATION vs FREQUENCY



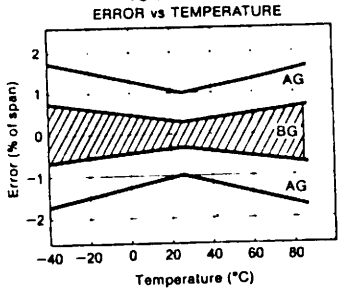
I_O POWER SUPPLY REJECTION vs FREQUENCY



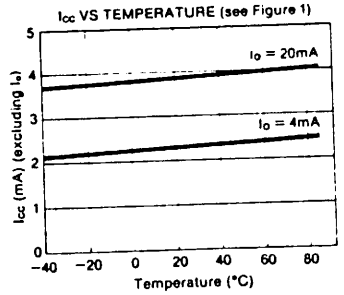
JUNCTION TEMPERATURE RISE vs V_{REF} OUTPUT CURRENT



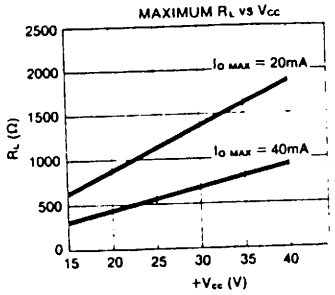
TOTAL OUTPUT ERROR vs TEMPERATURE



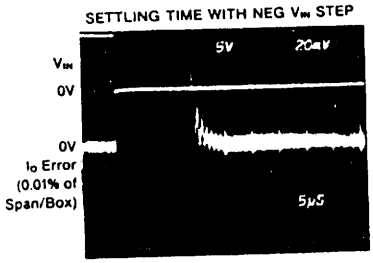
I_{CC} VS TEMPERATURE (see Figure 1)



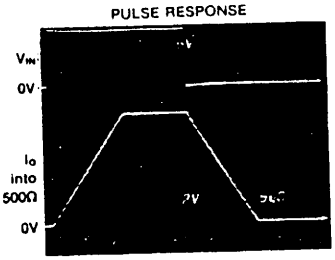
MAXIMUM R_L vs V_{CC}



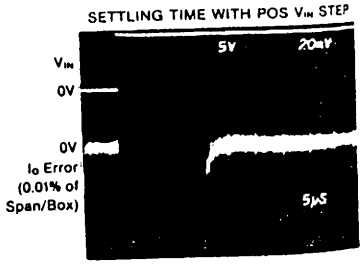
SETTLING TIME WITH NEG V_{IN} STEP



PULSE RESPONSE



SETTLING TIME WITH POS V_{IN} STEP



THEORY OF O

The XTR110 is designed t
voltage into a positive outp

A block diagram of the X
The circuit contains four
precision resistor divider n
to-current converter (A_1,
current converter (A_2, R_8,
+10V reference.

The precision divider netw
to the noninverting input
scale), V_{IN2} (5V full scale),

In the voltage-to-current c
ces its input voltage across
and R_7. Since Q_1 is a high
error is negligible and all c
current converter (into R_8)
ing input divider is as follo

$$I_{R8} = [(V_{REF}\ IN/16) + ($$

where R_{SPAN} is the resista
mon.

The current-to-current co
the XTR110 transmitter.
resistor (R_8) is forced acr

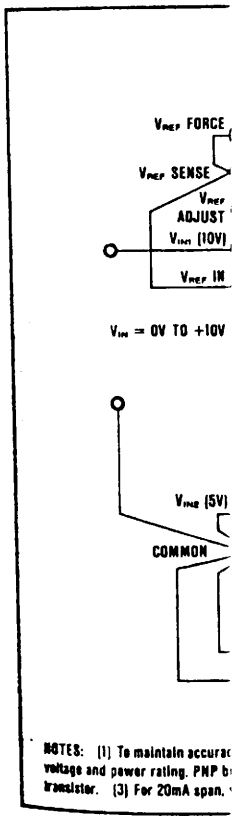
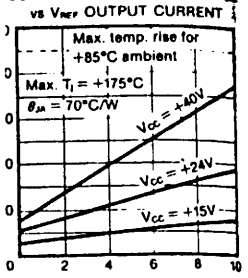


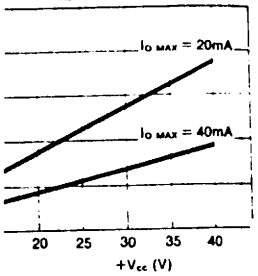
FIGURE 1. Block Diag

JUNCTION TEMPERATURE RISE vs V_{REF} OUTPUT CURRENT



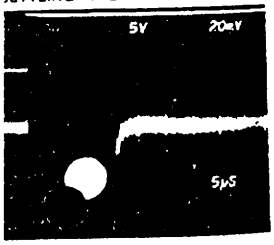
V_{REF} Output Current (mA)
(I_{OUT} has minimal effect on T_j)

MAXIMUM R_L vs V_{CC}



+V_{CC} (V)

SETTLING TIME WITH POS V_{IN} STEP



THEORY OF OPERATION

The XTR110 is designed to convert a high level input voltage into a positive output current.

A block diagram of the XTR110 is shown in Figure 1. The circuit contains four main functional blocks: (1) a precision resistor divider network (R_1–R_5), (2) a voltage-to-current converter (A_1, Q_1, R_6, R_7), (3) a current-to-current converter (A_2, R_8, R_9, Q_{EXT}), and (4) a precision +10V reference.

The precision divider network sums three input voltages to the noninverting input of A_1. These are V_{IN1} (10V full scale), V_{IN2} (5V full scale), and V_{REF} IN (for offsetting).

In the voltage-to-current converter, the op amp, A_1, forces its input voltage across the span setting resistors, R_6 and R_7. Since Q_1 is a high gain Darlington, base current error is negligible and all current flows to the current-to-current converter (into R_8). The transfer function including input divider is as follows:

$$I_{RR} = [(V_{REF}\ IN/16) + (V_{IN1}/4) + (V_{IN2}/2)]/R_{SPAN}$$

where R_{SPAN} is the resistance from Q_1 emitter to common.

The current-to-current converter is the output section of the XTR110 transmitter. The voltage across the 500Ω resistor (R_8) is forced across the 50Ω resistor (R_9) by A_2 and the external MOSFET (Q_{EXT}). Since no current flows in the gate of the MOSFET, all current is delivered to the output. This current (I_{OUT}) is ten times the internal current through R_8. Use of the external transistor keeps power out of the precision IC to maintain accuracy.

The overall transfer function for the XTR110 transmitter is:

$$I_O = 10[(V_{REF}\ IN/16) + (V_{IN1}/4) + (V_{IN2}/2)]/R_{SPAN}.$$

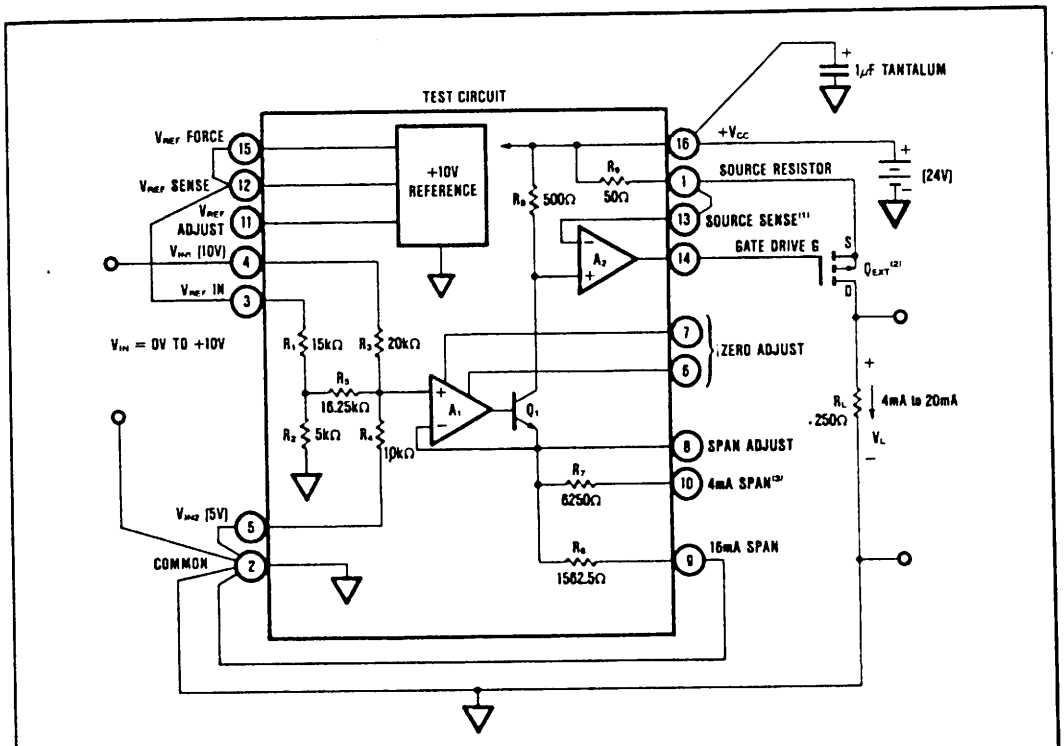
For output currents beyond 40mA an external resistor can be used in place of R_9.

The +10V reference provides input offsetting, e.g. 4mA offset for the 4ma to 20mA output configuration. The reference can deliver 10mA and is protected from shorts to common. Higher current can be provided for other applications by using an external NPN transistor connected to the sense and force pins.

INSTALLATION AND OPERATING INSTRUCTIONS

BASIC CONNECTION

The basic connection of the XTR110 is the standard 0V to +10V input; 4mA to 20mA output configuration is shown in Figure 1.



NOTES: (1) To maintain accuracy, make a separate direct connection between pins 1 and 13. (2) Q_{EXT} is any P-channel enhancement-mode power MOSFET with appropriate voltage and power rating. PNP bipolar transistors can be used with slight degradation in end-point accuracy and linearity. For recommended devices see section on external transistor. (3) For 20mA span, strap 4mA and 16mA pins together to common.

FIGURE 1. Block Diagram of the XTR110 in Basic Connection: 0V to +10V in, 4mA to 20mA out.

$+V_{CC}$ may originate at the XTR110 site or may be brought in as part of a three-wire twisted line. Be sure to use sufficient bypassing close to the XTR110 on the $+V_{CC}$ line.

EXTERNAL TRANSISTOR

Connections to the MOSFET are gate drive (pin 14) and source resistor (pin 1). To eliminate errors due to resistance in the connection between pin 1 and the source of the external transistor, connect pin 13 directly to pin 1 as shown in Figure 1.

The output of A2, pin 14, is intended to drive a MOSFET or PNP external pass transistor, and for that reason, is atypical of op amp outputs. The output stage can be visualized as a 300μA current source in parallel with an NPN collector. The NPN is the active element that, through feedback, determines where the gate drive should be set. It is capable of sinking over 15mA.

External MOSFET

The XTR110 can operate with a variety of output transistors having appropriate breakdown voltage and power rating which is influenced by package type. Some general observations on package thermal characteristics are listed in Table I.

TABLE I. External Transistor Package Type and Dissipation.

Package Type	Allowable Power Dissipation
TO-92	Lowest. Use minimum supply and at +25°C.
TO-237	Acceptable. Trade-off supply and temperature.
TO-39	Good. Adequate for majority of designs
TO-220	Excellent. For prolonged maximum stress
TO-3	Overkill. If nothing else is available

Maximum power dissipation of the external transistor can be derived from the derating curve. It can also be calculated from the thermal characteristics using the equation below:

$$P_A = P_D - (T_A - 25)/\theta_{JA}$$

P_A = Power to be dissipated at T_A
T_A = Maximum ambient temperature
P_D = Maximum continuous power dissipation at +25°C ($I_D V_{DS}$)
θ_{JA} = Junction to ambient thermal resistance

(Refer to the manufacturer's data sheet for required numbers.)

Table II shows suitable MOSFET output transistors.

Summary of points to consider for selecting the transistor are:

1. Power rating—Equal to 1.5 × P_A if possible, or at least equal to P_A.
2. Drain-source breakdown—Greater than maximum expected V_{DS}. This includes any additional voltage that may exist between the transmitter and receiver grounds.
3. Gate-source breakdown—Greater than $+V_{CC}$, because V_{CC} will be applied gate-to-source, under the condition of an open drain line (V_{GATE} then = 0V). Most MOSFETS will tolerate only 20V, but a zener (12V or more) connected gate-to-source will clamp the junction and remain off during normal operation.

TABLE II. Available P-Channel MOSFETs.

Manufacturer	Part No.	BV_{DSS}*	BV_{GS}*	Package
Ferranti	ZVP1304A	−40V	20V	TO-92
	ZVP1304B	−40V	20V	TO-39
	ZVP1306A	−60V	20V	TO-92
	ZVP1306B	−60V	20V	TO-39
International Rectifier	IRF9513	−60V	20V	TO-220
Motorola	MTP8P08	−80V	20V	TO-220
RCA	RFL1P08	−80V	20V	TO-39
	RFT2P08	−80V	20V	TO-220
Siliconix (preferred)	VP0300B	−30V	40V	TO-39
	VP0300L	−30V	40V	TO-92
	VP0300M	−30V	40V	TO-237
	VP0808B	−80V	40V	TO-39
	VP0808L	−80V	40V	TO-92
	VP0808M	−80V	40V	TO-237
Supertex	VP1304N2	−40V	20V	TO-220
	VP1304N3	−40V	20V	TO-92
	VP1306N2	−60V	20V	TO-220
	VP1306N3	−60V	20V	TO-92

*BV_{DSS}—Drain-source breakdown voltage. BV_{GS}—Gate-source breakdown voltage.

External PNP Transistor

A PNP bipolar transistor can also be used for the output but it will result in a slight drop in end-point accuracy and linearity. A TN2905 in a TO-237 package performs adequately. The end point shifts can be calculated if the beta of the PNP is known. The offset shift is I_{OS} beta and the span shift is I_{SPAN}/beta. For example, if the transistor's beta is 250 and the output range is 4mA to 20mA, the calculations are as follows:

$dI_{OS} = 4mA/250 = 16\mu A$ (0.1% of span)
$dI_{SPAN} = 16mA/250 = 64\mu A$ (0.4% of span)

The offset error can be corrected by using the offset correction circuitry of Figure 5. The span error due to base current loss can be compensated by connecting an external resistor, R_{PAD}, in parallel with the internal resistor as shown in Figure 2. R_{PAD} can be calculated with the following formula:

$$R_{PAD} = 50 \text{ (beta + 1)}$$

Any span error due to the XTR110 itself can be corrected with the span adjust circuitry of Figure 5. Use a nominal beta to calculate the value of R_{PAD} if individual transistor measurements are not made. There should be enough range in the span adjust circuit to compensate for normal tolerances.

Small nonlinearity degradation (0.01% typical at $24V_{CC}$) results from changes in beta caused by changes in power as collector current varies from 4mA to 20mA. A heat sink can be added to minimize the heat dissipation effect.

A Darlington configuration (two separate PNPs) can also be used with no degradation in end-point accuracy and linearity. A 0.047μF capacitor across pins 13 and 14 is required for stability as shown in Figure 3. Single-packaged Darlingtons with in
not recommended since th
accuracy.

To select a bipolar transistor.
for MOSFETs. Note, howeve
down is not considered becau
biased should the collector o

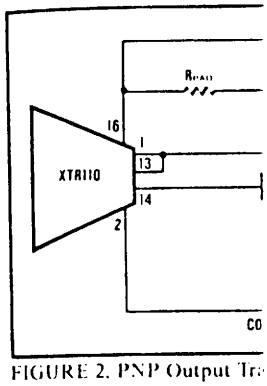


FIGURE 2. PNP Output Tra
span error cause

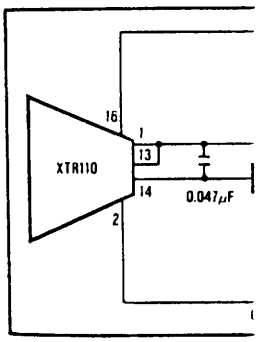


FIGURE 3. Darlington Out
Transistors.

COMMONS

Careful attention should be
nection of the commons. A
at one point as close to pin
The exception is the I_{OUT}
any place where it will not
2.

VOLTAGE REFERENCE

The reference voltage is a
(V_{REF} sense). To preserve
pin 3 should be connected
The circuit in Figure 4 shov
of the voltage reference.

e only 20V, but a zener (12V or
o-source will clamp the junc-
ing normal operation.

-Channel MOSFETs.

	BV_{DSS}*	BV_{GS}*	Package
A	−40V	20V	TO-92
B	−40V	20V	TO-39
A	−60V	20V	TO-92
B	−60V	20V	TO-39
	−60V	20V	TO-220
	−80V	20V	TO-220
	−80V	20V	TO-39
	−80V	20V	TO-220
	−30V	40V	TO-39
	−30V	40V	TO-92
	−30V	40V	TO-237
	−80V	40V	TO-39
	−80V	40V	TO-92
	−80V	40V	TO-237
	–	20V	TO-220
	–	20V	TO-92
		20V	TO-220
		20V	TO-92

wn voltage. BV_{GS}—Gate-source break-

or

r can also be used for the output
ght drop in end-point accuracy
5 in a TO-237 package performs
nt shifts can be calculated if the
wn. The offset shift is I_{OS}/beta
SPAN/beta. For example, if the
and the output range is 4mA to
re as follows:

16μA (0.1% of span)
0 = 64μA (0.4% of span)

corrected by using the offset
Figure 5. The span error due to
compensated by connecting an
in parallel with the internal
gure 2. R_{PAD} can be calculated
ila:

= 50 (+ 1)

e XT itself can be corrected
uitry gure 5. Use a nominal
e of R_{PAD} if individual transistor
nade. There should be enough
ust circuit to compensate for

dation (0.01% typical at 24V_{CC})
eta caused by changes in power
es from 4mA to 20mA. A heat
mize the heat dissipation effect.
tion (two separate PNPs) can
radation in end-point accuracy
capacitor across pins 13 and 14
as shown in Figure 3. Single-

packaged Darlingtons with internal bleeder resistors are not recommended since they will severly degrade accuracy.

To select a bipolar transistor, follow the same points as for MOSFETs. Note, however, the base-emitter breakdown is not considered because this junction is forward biased should the collector open.

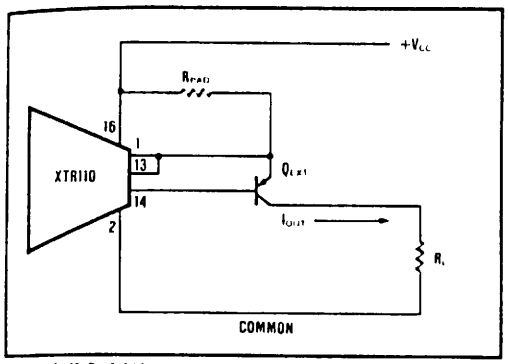


FIGURE 2. PNP Output Transistor (R_{PAD} corrects for span error caused by beta).

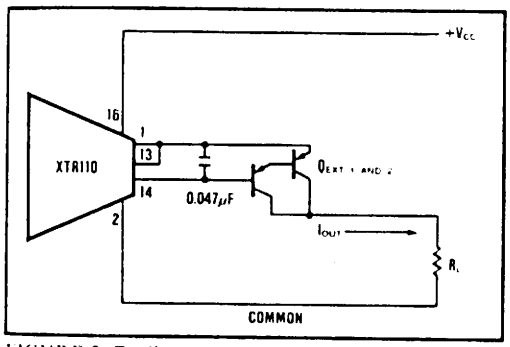


FIGURE 3. Darlington Output Composed of Two PNP Transistors.

COMMONS

Careful attention should be directed toward proper connection of the commons. All commons should be joined at one point as close to pin 2 of the XTR110 as possible. The exception is the I_{OUT} return. It can be returned to any place where it will not modulate the common at pin 2.

VOLTAGE REFERENCE

The reference voltage is accurately regulated at pin 12 (V_{REF} sense). To preserve accuracy, any load including pin 3 should be connected to this point.

The circuit in Figure 4 shows coarse and fine adjustment of the voltage reference.

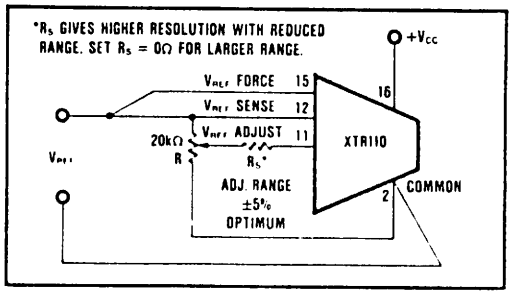


FIGURE 4. Optional Adjustment of Reference Voltage.

OFFSET (ZERO) ADJUSTMENT

The offset current can be adjusted by using the potentiometer, R_1, shown in Figure 5. The procedure is to set the input voltage to zero and then adjust R_1 to give 4mA at the output. For spans starting at 0mA, the following special procedure is recommended: set the input to a small nonzero value and then adjust R_1 to the proper output current. When the input is zero the output will be zero. Figures 6 and 7 show graphically how offset is adjusted.

SPAN ADJUSTMENT

The span is adjusted at the full-scale output current using the potentiometer, R_2, shown in Figure 5. This adjustment is interactive with the offset adjustment, and a few iterations may be necessary. For the circuit shown, set the input voltage to +10V full scale and then adjust R_2 to give 20mA full-scale output. Figures 6 and 7 show graphically how span is adjusted.

The values of R_2, R_3, and R_4 for adjusting the span are determined as follows: choose R_4 in series to slightly decrease the span; then choose R_2 and R_3 to increase the span to be adjustable about the center value.

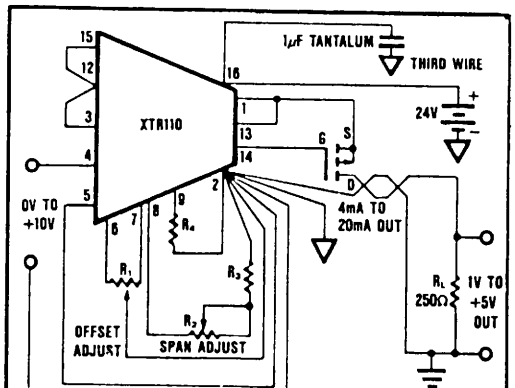


FIGURE 5. Offset and Span Adjustment Circuit for 0V to +10V Input, 4mA to 20mA Output.

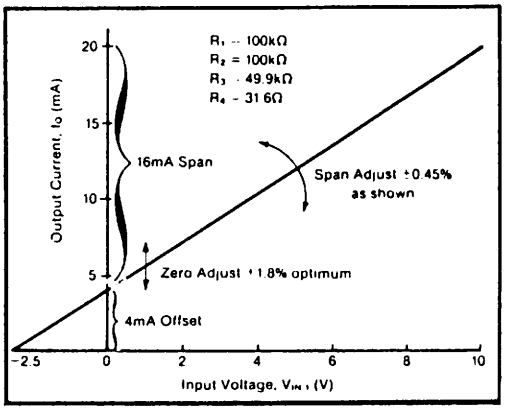


FIGURE 6. Zero and Span of 0V to +10V Input, 4mA to 20mA Output Configuration (see Figure 5).

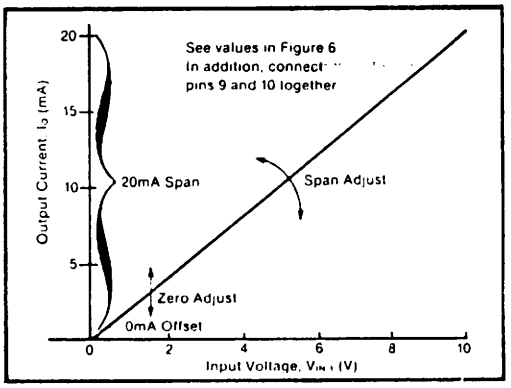


FIGURE 7. Zero and Span of 0V to +10V$_{IN}$, 0mA to 20mA Output Configuration (see Figure 5).

ERROR CALCULATIONS

Errors can be calculated by considering these key parameters:

1. Offset Current (Initial, vs Temperature, vs Supply)
2. Span Error (Initial, vs Temperature, vs Supply)
3. Nonlinearity

Lower errors can readily be obtained by externally adjusting the initial offset and span errors to zero (see Performance Curves).

EXTENDED REFERENCE CURRENT DRIVE

The current drive capability of the XTR110's internal reference is 10mA. This can be extended if desired by adding an external NPN transistor shown in Figure 8.

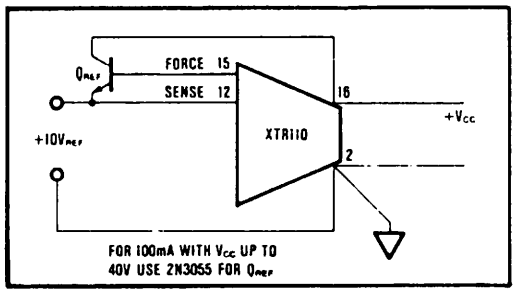


FIGURE 8. Extended Reference Current Drive.

LOW TEMPERATURE COEFFICIENT (TC) OPERATION

Although the precision resistors in the XTR110 track within 1ppm °C, the output current depends upon the absolute temperature coefficient of any one of the resistors, R_A, R_B, R_S, and R_N. Since the absolute TC of the resistors is 20ppm/°C, maximum, the TC of the output current can have 20ppm °C drift. For low TC operation, zero TC resistors can be substituted for either the span resistors (R_A or R_B) or for the source resistor (R_N) but not both.

EXTENDED SPAN

For spans beyond 40mA, the internal 50Ω resistor (R_N) may be replaced by an external resistor connected between pins 13 and 16.

Its value can be calculated as follows:

$$R_{EXT} = R_N (Span_{OLD}/Span_{NEW})$$

Since the internal thin-film resistors have a 20% absolute value tolerance, measure R_N before determining the final value of R_{EXT}. Self-heating of R_{EXT} can cause nonlinearity. Therefore, choose one with a low TC and adequate power rating. See Figure 14 for application.

STANDARD CURRENT RANGES OR SPANS

Table III shows the pin connections for standard XTR110 current ranges.

TABLE III. Pin Connections for Standard Ranges.

Input Range (V)	Output Range (mA)	Pin 3	Pin 4	Pin 5	Pin 9	Pin 10
0 - 10	0 - 20	Com	Input	Com	Com	Com
2 - 10	4 - 20	Com	Input	Com	Com	Com
0 - 10	4 - 20	+10V Ref	Input	Com	Com	Open
0 - 10	5 - 25	+10V Ref	Input	Com	Com	Com
0 - 5	0 - 20	Com	Com	Input	Com	Com
1 - 5	4 - 20	Com	Com	Input	Com	Com
0 - 5	4 - 20	+10V Ref	Com	Input	Com	Open
0 - 5	5 - 25	+10V Ref	Com	Input	Com	Com

TYPICAL AP

The XTR110 is ideal fo
ing high noise immuni
sion. The precision +10
be exciting for bridges a
make it very useful as a

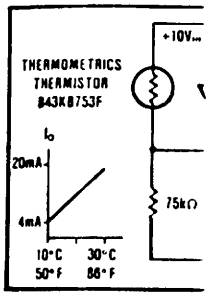


FIGURE 9. 4mA to 20

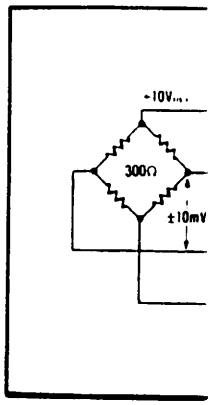


FIGURE 10. 4mA to 2

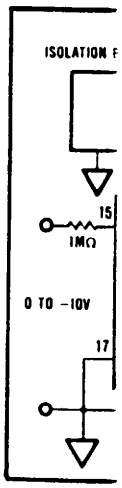


FIGURE 11.

Step spændings på 6757
(RAM fra 1000 - 1FFF)

```
start: 1100:  MVI A, C0   } [illegible]
              SIM
              MVI A, 09
              OUT BF
              MVI A, 40   } [illegible]
              SIM
              LXI SP, 2000
              LXI H, 0
       1110 → CALL CH1  (1120)
              CALL CH2  (1129)
              CALL vent (1132)
              MOV A, H
              ADI 02
              MOV H, A
              JMP 1110

CH1:          MOV A, H
1120          OUT BASE+01
              MOV A, L
              OUT BASE+00
              OUT BASE+02
              RET

CH2:          MOV A, H
1129          OUT BASE+05
              MOV A, L
              OUT BASE+04
              OUT BASE+06
              RET

vent:         LXI D, 1FF
1132   1135 → DCX D
              MOV A, D
              ORA E
              NOP
              NOP
              JNZ 1135
              MVI A, C0
              SIM
              IN B5       }
              ANI 020     } [illegible]
              CNZ F008    }
              MVI A, 40
              SIM
114B          RET
```

Test 6757 på IPC/1 v. 4.9. debugger
RAM fra 1000 – 1FFF

```
1000:   MVI A, C0   } set = 1
        SIM (30)
        MVI A, 09   } card
        OUT BF      } set type
        MVI A, 40   } set = 0
        SIM (30)
```

output 0000 på begge kanaler

```
→       MVI A, 00
        OUT BASE+01   ← MSB adress
→       MVI A, 00     } set kanal 1
        OUT BASE+00   ← LSB adress
        OUT BASE+02   ← start
```

dvs ett sätta output til FFFF på begge kanaler

```
→       MVI A, 00
        OUT BASE+05
→       MVI A, 00     } set kanal 2
        OUT BASE+04
        OUT BASE+06   ← start
        JMP 0000
```

BASE = switch adds

4000 → FF

4200 → 00

ADR 70 → switch 2+3+4 ON

Manual for

IPC/1 Analog Output Modul

Varenummer 6751

Dansk Data Elektronik A/S
Februar 1991

Indholdsfortegnelse

1. Introduktion

IPC/1 modulet type 6751 er et analogt output kort med 2/4 udgange, hvor hver kanal kan give såval et 0 - 10 V spændingssignal, som et 0 - 20mA eller 4 - 20 mA current loop signal.

D/A konverteringen for hver kanal foretages med en 12 bit D/A konverter.

Udgangssiden er galvanisk adskilt (isolation 1500 V DC) fra processor siden. Udgangssiden skal have en extern (fælles) strømforsyning.

Kortet indeholder skematisk følgende kredsløb:

- D/A konverter, isolationsforstærker, V/I konverter og analog udgangsforstærker for hver kanal.

- Fælles spændingsreferance for D/A konverterne.

- DC/DC konverter til udgangskredsløbene, så kortet kan forsynes fra een sælles ekstern forsyning.

Udgangene har beskyttelsesdioder og -modstande til beskyttelse mod almindeligt forekommende transienter. Udgangene og den eksterne strømforsyning har fælles stel.

2. Funktionsbeskrivelse

Kortet kan bestykkes med op til 4 analog output kanaler. Standard versionen af kortet har monteret de to første kanaler, mens den udvidede version af kortet har monteret alle 4 kanaler.

Hver kanal er opbygget omkring tre hovedkomponenter: En 12 bit D/A konverter DAC1230, en isolationsforstærker ISO122P og en spændings til strømsløjfe konverter.
Konverteringstid: 10 mS max. (fra start af konvertering).
V/I konverteren har en ekstern MOSFET til styring af udgangsstrømmen. Strømudgangen kan strappes til enten 0 - 20 mA eller til 4 - 20 mA (dog skal kortet justeres på ny efter strapændring).
For hver kanal er der foruden V/I konverteren anbragt en operationsforstærker, der leverer et spændingsoutput.
Offset og gain kan trimmes separat for strøm- og spændingsudgangen for hver kanal.

Alle udgange (såvel spænding som strøm) har fælles stel; dette gælder også den eksterne strømforsyning. Forsyningen til kredsene på udgangssiden skal være 24 V DE (±2 V) og forbruget er max. 250 mA for hver kort. Dog er forsyningen til strømsløjferne ført ud separat (men normalt forbundet til den faste eksterne forsyning).

På kortet findes også en fælles spændingsreferance til D/A konverterne.

Efter power-up er alle udgange på kortet disablede, svarende til udlæst dataværdi = 00h. Ved første konv. start kommando på kanal 1 enables alle udgange på kortet. Der kan således udlæses initial dataværdier til kanalernes dataregistre og konverteres, inden alle udgange samtidigt åbnes ved start af konvertering på kanal 1.

Ved power-off for IPC datamaten disables kortes udgange, svarende til udlæsning af dataværdi = 00h, uanset om den eksterne for-

syning til kortets udgangsside er on eller off.

Adressering

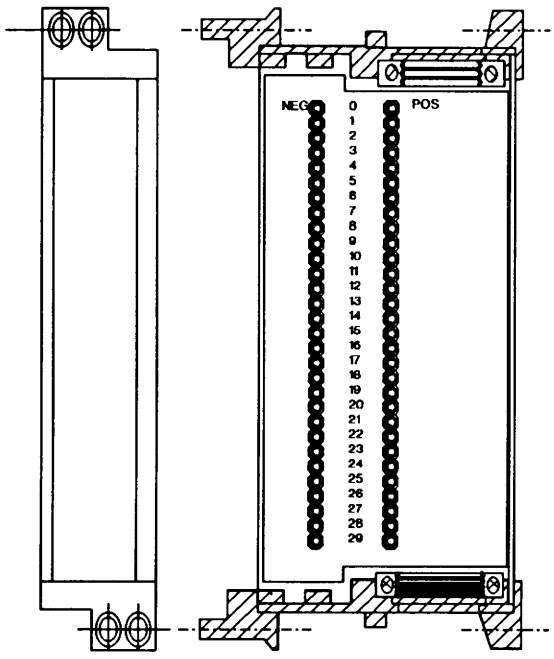
Kortet optager 16 I/O adresser, hvorfor basisadressen skal sættes i step af 16. De 4 switche på kortet er derfor de 4 mest betydende bit. I nedenstående tabel er de 4 0'er i invers altså fast kodet i printet.

Switch SW:	Analog output kanal #:
0000**0000** binært = 0 decimalt	0, 1, (2 og 3)
0001**0000** binært = 16 decimalt	4, 5, (6 og 7)
0010**0000** binært = 32 decimalt	8, 9, (10 og 11)
XXXX**0000** binært = 16n decimalt	4n, 4n+1, (4n+2, 4n+3)

3. Mekanisk beskrivelse af board og stik

IPC/1 modulet 6751 består af et board (standard europakort format) samt et periferistik.
Boardet er afsluttet i en 64-polet DIN-konnektor påmonteret en aluminiums forplolade, der dels muliggør fastspænding i IPC/1 rack, dels muliggør fastspænding af periferistikket.

Signal tilslutningen sker via et medfølgende stik (varenummer 6751c) forsynet med loddeterminaler:



Connections:

Signal	Name:	Signal	Name:
	NEG 0		NEG 15
V-loop (+)	POS 0		POS 15
	NEG 1		NEG 16
V-loop (+)	POS 1	I Chan. 2	POS 16
	NEG 2		NEG 17
V-konv (+)	POS 2	V Chan. 2	POS 17
	NEG 3		NEG 18
V-konv (+)	POS 3		POS 18
	NEG 4		NEG 19
	POS 4		POS 19
	NEG 5		NEG 20
	POS 5	I Chan. 3	POS 20
	NEG 6		NEG 21
	POS 6	V Chan. 3	POS 21
	NEG 7		NEG 22
	POS 7		POS 22
	NEG 8		NEG 23
I Chan. 0	POS 8		POS 23
	NEG 9		NEG 24
V Chan. 0	POS 9		POS 24
	NEG 10		NEG 25
	POS 10		POS 25
	NEG 11		NEG 26
	POS 11	V-konv (-)	POS 26
	NEG 12		NEG 27
I Chan. 1	POS 12	V-konv (-)	POS 27
	NEG 13		NEG 28
V Chan. 1	POS 13	V-loop (-)	POS 28
	NEG 14		NEG 29
	POS 14	V-loop (-)	POS 29

→ Poul Knudsen, S&W

X-Sender: jwj@ariane.dde.dk
X-Mailer: QUALCOMM Windows Eudora Pro Version 4.1
Date: Mon, 11 Jan 1999 16:09:45 +0100
To: sgf
From: Jesper Wolf Jespersen <jwj@dde.dk>
Subject: beskrivelse af modifikation til 6027c kort i forbindelse med 6751 kortet

Hej Søren.

Jeg har gennemgået kortforbindelserne og den gamle dokumentation på 6751c pin-outet og har forfattet følgende modificationsbeskrivelse til 6027c kortets standard bestykning.

Generelt må det bemærkes at lysdioderne ingen funktion har i forbindelse med 6751 AO kortet.

Lysdioderne er, i AO sammnehæng, forspændt forkert og vil, hvis de ikke kortsluttes, forhindre at kortets signaler er tilgængelige på de tilsigtede udgange.

Derfor er det nødvendigt at kortslutte/luse lysdioderne i forbindelse med følgende ledere, her er angivet stik forbindelser såvel som pin numre og logiske signaler:

ben	række-a	række-b	DI-no
2	gnd	Vloop +	0
3	gnd	Vloop +	1
4	gnd	Vconv +	2
5	gnd	Vconv +	3
10	gnd	Iout 1 +	8
11	gnd	Vout 1 +	9
14	gnd	Iout 2 +	12
15	gnd	Vout 2 +	13
18	gnd	Iout 3 +	16
19	gnd	Vout 3 +	17
22	gnd	Iout 4 +	20
23	gnd	Vout 4 +	21
28	gnd	gnd (Vconv -)	26
29	gnd	gnd (Vconv -)	27
30	gnd	gnd (Vloop -)	28
31	gnd	gnd (Vloop -)	29

Hvis man sidder med et bart 6027C kort er det meget simplere at montere lus i ovenstående lysdiodepositioner, det gør det også meget simpelt at se at man har fat i det rigtige miniprint.

Har man et færdigbestykket kort kan man også bare luse de ovenfor nævnte lysdioder og så huske at skrive korrekt type på stik'et. Det er ret frustrerende at skulle skille stikket af for at se om det er den rette type. Eventuelt kan man udlodde lysdioderne så man udefra kan se at stikket er modificeret.

Med venlig hilsen
Jesper Wolf Jespersen

+-----------------------------+-------------------------+
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Process Control Development	d d
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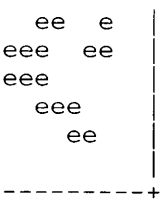

Manual for

IPC/1 Analog Output Modul

Varenummer 296436x0

Dansk Data Elektronik A/S
September 1995

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Hver kanal er opbygget omkring tre hovedkomponenter: En 12 bit D/A konverter DAC1230, en isolationsforstærker ISO122P og en spændings til strømsløjfe konverter.
Konverteringstid: 10 mS max. (fra start af konvertering).
V/I konverteren har en ekstern MOSFET til styring af udgangsstrømmen. Strømudgangen kan strappes til enten 0 - 20 mA eller til 4 - 20 mA (dog skal kortet justeres på ny efter strapændring).
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Ved power-off for IPC datamaten disables kortes udgange, svarende til udlæsning af dataværdi = 00h, uanset om den eksterne forsyning til kortets udgangsside er on eller off.

Adressering

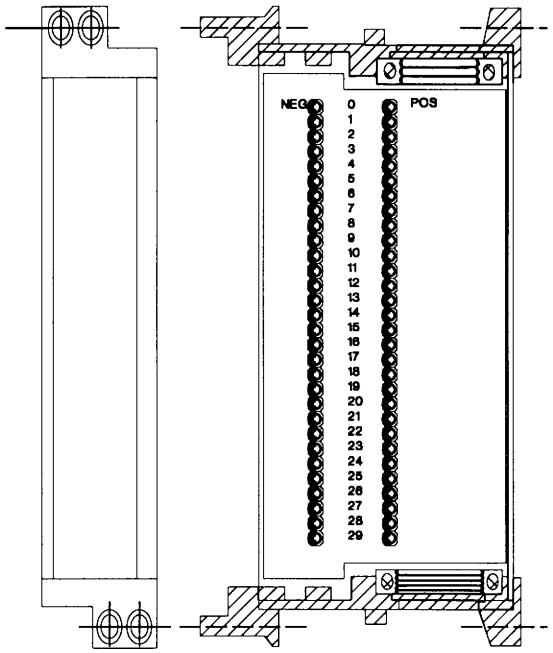
Kortet optager 16 I/O adresser, hvorfor basisadressen skal sættes i step af 16. De 4 switche på kortet er derfor de 4 mest betydende bit. I nedenstående tabel er de 4 0'er i invers altså fast kodet i printet.

Switch SW:	Analog output kanal #:
0000**0000** binært = 0 decimalt	0, 1, (2 og 3)
0001**0000** binært = 16 decimalt	4, 5, (6 og 7)
0010**0000** binært = 32 decimalt	8, 9, (10 og 11)
XXXX**0000** binært = 16n decimalt	4n, 4n+1, (4n+2, 4n+3)

3. Mekanisk beskrivelse af board og stik

IPC/1 modulet 6751 består af et board (standard europakort format) samt et periferistik.
Boardet er afsluttet i en 64-polet DIN-konnektor påmonteret en aluminiums forplolade, der dels muliggør fastspænding i IPC/1 rack, dels muliggør fastspænding af periferistikket.

Signal tilslutningen sker via et medfølgende stik (varenummer 6751c) forsynet med loddeterminaler:



Connections:

Signal	Name:	Signal	Name:
	NEG 0		NEG 15
V-loop (+)	POS 0		POS 15
	NEG 1		NEG 16
V-loop (+)	POS 1	I Chan. 2	POS 16
	NEG 2		NEG 17
V-konv (+)	POS 2	V Chan. 2	POS 17
	NEG 3		NEG 18
V-konv (+)	POS 3		POS 18
	NEG 4		NEG 19
	POS 4		POS 19
	NEG 5		NEG 20
	POS 5	I Chan. 3	POS 20
	NEG 6		NEG 21
	POS 6	V Chan. 3	POS 21
	NEG 7		NEG 22
	POS 7		POS 22
	NEG 8		NEG 23
I Chan. 0	POS 8		POS 23
	NEG 9		NEG 24
V Chan. 0	POS 9		POS 24
	NEG 10		NEG 25
	POS 10		POS 25
	NEG 11		NEG 26
	POS 11	V-konv (-)	POS 26
	NEG 12		NEG 27
I Chan. 1	POS 12	V-konv (-)	POS 27
	NEG 13		NEG 28
V Chan. 1	POS 13	V-loop (-)	POS 28
	NEG 14		NEG 29
	POS 14	V-loop (-)	POS 29

V-loop (+): Forsyning til strømsløjfe (+24 V). Frobindes kun hvis der anvendes strømsløjfe.

V-loop (-): Forsyning til strømsløjfe (stel).
V-conv (+): Forsyning til konverter (+24 V).
V-conv (-): Forsyning til konverter (stel).
I Chan. x: Strøm-output for kanal x.
V Chan. x: Spændingsoutput for kanal x.

4. Justering

De fire kanaler justeres hver for sig. For hver kanal findes fire trimmepotmetre, TRx1, TRx2, TRx3 og TRx4, hvor x står for kanal 1 til 4.

Først udlæses (f.eks med TEST I/O eller Ladder-Logic) en dataværdi = 0 til den pågældende kanal.

Med digitalvoltmeter på TPx2 trimmes på TRx2 til offset er mindre end ± 1 mV. Dernæst trimmes TRx3 til offset er mindre end ± 2 mV på spændingsudgangen for den pågældende kanal.

Med en modstand på 100,0 Ohm (0,1 %) forbundet mellem kanalens strømudgang og stel trimmes TRx4 til en visning på mellem 0 mV og 0,5 mV over målemodstanden (for område 0 - 20 mA).

Dernæst udlæses dataværdi = 32767 decimalt (TEST I/O) til den pågældende kanal.

Med digitalvoltmeter på spændingsudgangen trimmes på TRx1 til en spænding på 10,00 V. Det kontrolleres, at der nu er en spænding på 2,000 V over strømmålemodstanden (svarende til 20,00 mA).

Med Ladder-Logic udlæses derefter en step-spænding, med step af 255 decimalt for hver gennemløb af koden, på den pågældende kanal. Såvel strøm- som spændingsudgangen betragtes med et oscilloscop. Det kontrolleres, at signalets indsvingninger og trinstørrelser er ensartede.

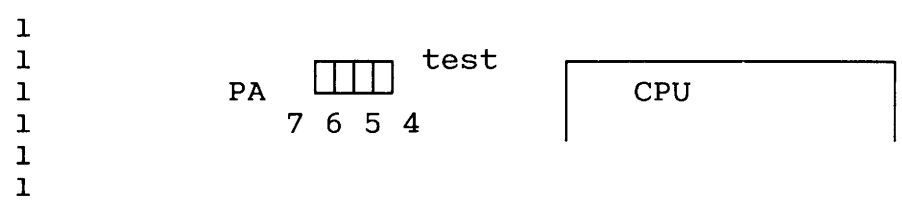
Test af 6055X Iss 4 print.

Kortet kan dels testes med original CPU 6055X version 2.0 19-11-91
og dels med CPU 6055X 10.10.91 med indbygget testprom.

Med original 6055X CPU :

Kortet forsynes med 5V og tilsluttes seriel port på en PC'er via det specielle kabel med optokoblere for interface konvertering.Derefter køres testen 'hdlc' ~~som findes på diskette.~~ Jvf.nærmere beskrivelse i 'Manual for IPC/1 6055X' Testen bruger delvis programmet 'Supermax Vejebod' LCD display tilsluttes connector L - Trimmer PT1 drejes max. mod uret.Når der isættes strap i strapfelt 'TEST' PA4 vil der ved power on komme tekst i display. (Vægtinterface 2.00)

Strapoversigt for strapfelt 'TEST' (PA4-PA5-PA6-PA7)

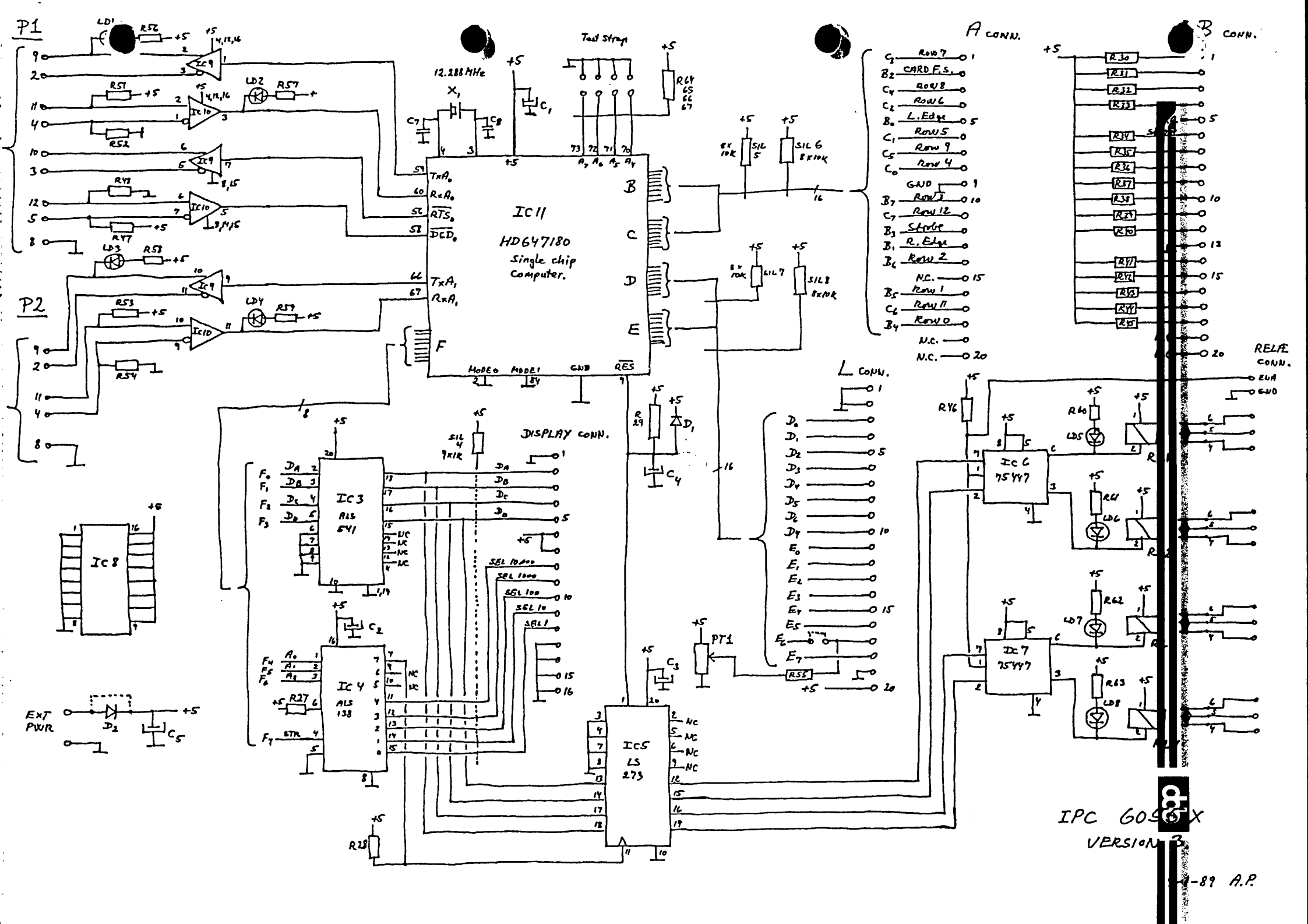


Med CPU 6055X 10.10.91 med indbygget testprom :

Kortet tilsluttes en terminal via det ovennævnte kabel. LCD display tilsluttes. Derefter kan følgende tests køres efter power on :

Alle straps monteret (PA4-PA7) :	LCD test (This is a test... Hitachi LCD 20 x 2)
Strap PA7 ikke monteret :	kortlæsertest
Strap PA6 ikke monteret :	ekkotest CH0 (P1)
Strap PA5 ikke monteret :	ekkotest CH1 (P2)
Strap PA4 ikke monteret :	relætest

Husk 8801 kabel (88001050) til terminal


P1
P2
IC11
HD647180
Single chip
Computer.
12.288 MHz
X1
Test Strip
A CONN.
B CONN.
L CONN.
DISPLAY CONN.
RELAY CONN.
IC 8
IC 3
ALS 641
IC 4
ALS 138
IC5
LS 273
IC 6
75477
IC 7
75477
EXT PWR
PT1
IPC 6096X
VERSION 3
-89 A.P.

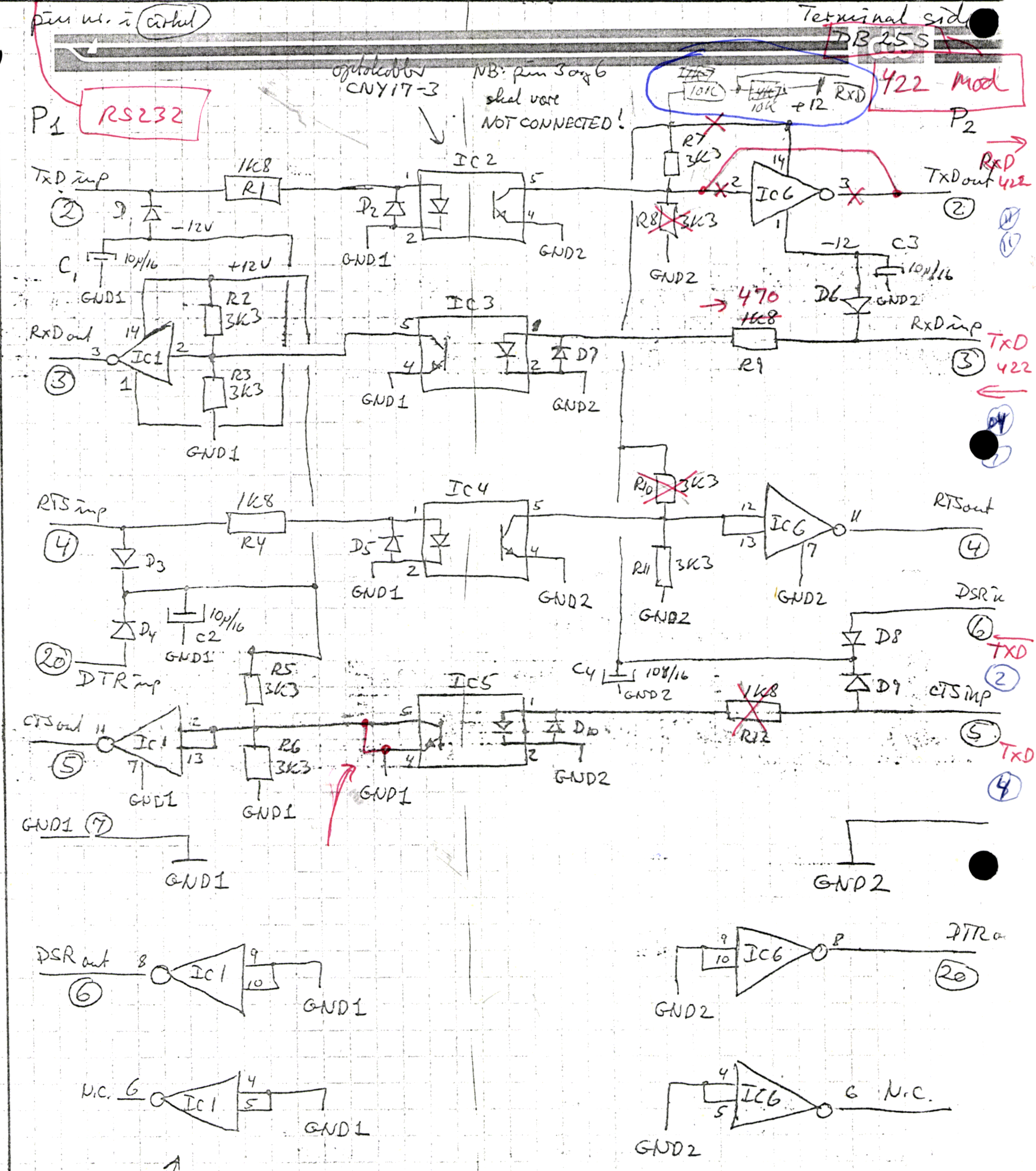
dansk data elektronik a/s

Initialer/dato	Side
AP 4/5 -88	
Revideret	**Projekt**
	Isolator

UTC port side

DB25P

422 OPTO

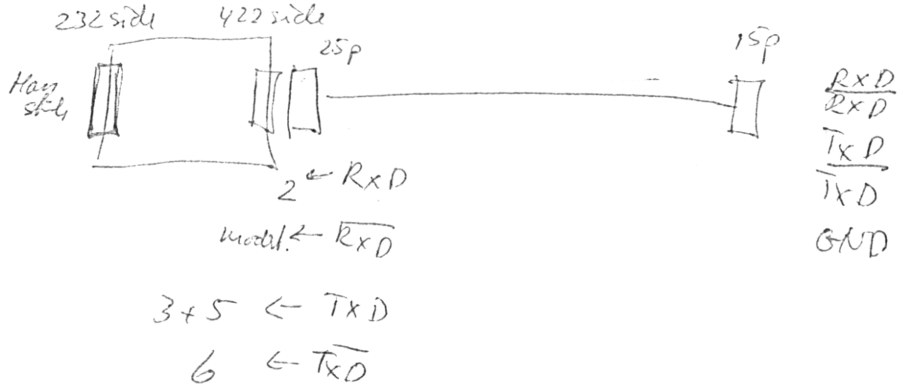


Driver IC er DS 14C88 N

GND1 og GND2 er galvanisk adskilt

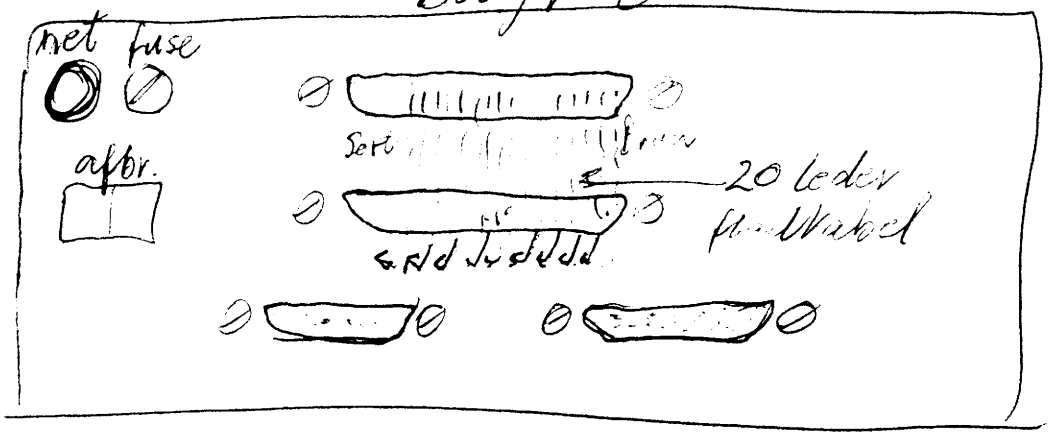
Alle dioder 1N4148

→ LS, KLOKKERHOLM

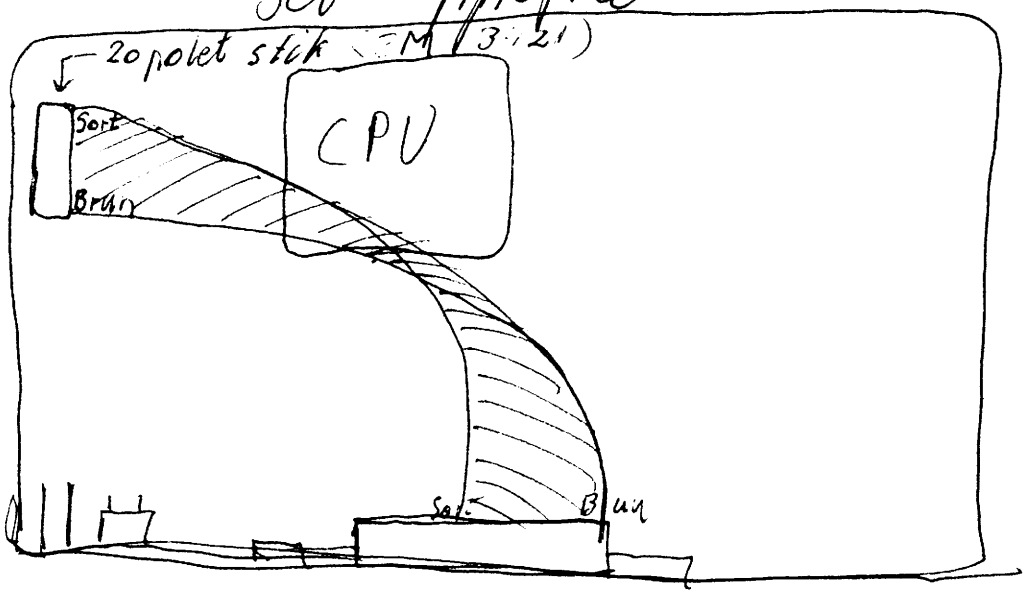

232 side
422 side
25P
15P
Hanger side
2 ← RxD
module ← $\overline{RxD}$
3+5 ← TxD
6 ← $\overline{TxD}$
RxD
$\overline{RxD}$
TxD
$\overline{TxD}$
GND

Beskrivelse af flad kabel for 6055 X vejebod.

Bagfra



Set oppefra



1.3 Pin Assignment

Figure 1-2. shows a top view of the HD647180X packages. Table 1-1. shows the pin functions in the four modes.

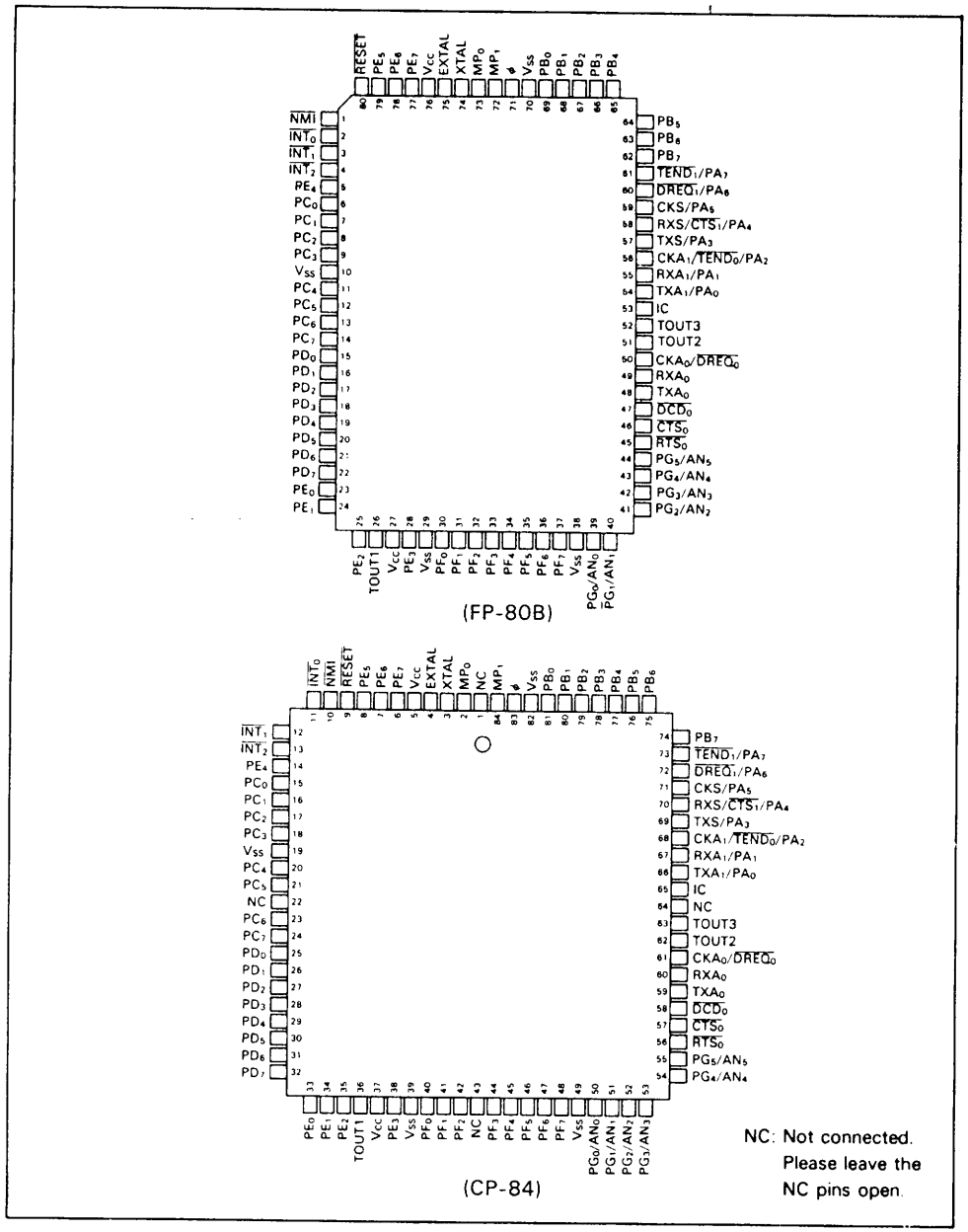


Figure 1-2. Pin Assignment

Table 1-1. Pin Function

Pin No.		Mode 0	Mode 1	Mode 2	Mode 3
FP-80B	CP-84				
1	10	$\overline{NMI}$	←	←	A_9
2	11	$\overline{INT_0}$	←	←	–
3	12	$\overline{INT_1}$	←	←	–
4	13	$\overline{INT_2}$	←	←	–
5	14	PE_4	ST	←	–
6	15	PC_0	A_0	←	←
7	16	PC_1	A_1	←	←
8	17	PC_2	A_2	←	←
9	18	PC_3	A_3	←	←
10	19	V_{SS}	←	←	←
11	20	PC_4	A_4	←	←
12	21	PC_5	A_5	←	←
13	23	PC_6	A_6	←	←
14	24	PC_7	A_7	←	←
15	25	PD_0	A_8	A_8/PD_0	A_8
16	26	PD_1	A_9	A_9/PD_1	–
17	27	PD_2	A_{10}	A_{10}/PD_2	A_{10}
18	28	PD_3	A_{11}	A_{11}/PD_3	A_{11}
19	29	PD_4	A_{12}	A_{12}/PD_4	A_{12}
20	30	PD_5	A_{13}	A_{13}/PD_5	A_{13}
21	31	PD_6	A_{14}	A_{14}/PD_6	A_{14}
22	32	PD_7	A_{15}	A_{15}/PD_7	$\overline{OE}$
23	33	PE_0	A_{16}	A_{16}/PE_0	$\overline{CE}$
24	34	PE_1	A_{17}	A_{17}/PE_1	–
25	35	PE_2	A_{18}	A_{18}/PE_2	–
26	36	TOUT1	←	←	–
27	37	V_{CC}	←	←	←
28	38	PE_3	A_{19}	A_{19}/PE_3	–
29	39	V_{SS}	←	←	←
30	40	PF_0	D_0	←	O_0
31	41	PF_1	D_1	←	O_1
32	42	PF_2	D_2	←	O_2
33	44	PF_3	D_3	←	O_3
34	45	PF_4	D_4	←	O_4
35	46	PF_5	D_5	←	O_5
36	47	PF_6	D_6	←	O_6
37	48	PF_7	D_7	←	O_7
38	49	V_{SS}	←	←	←
39	50	PG_0/AN_0	←	←	–
40	51	PG_1/AN_1	←	←	–

Notes: ← Same as previous column
– No function

IC 11:

p 68 = PA_2

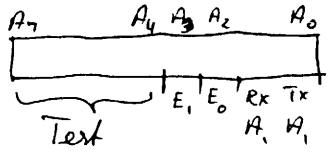
p 69 = PA_3

$\overline{INT}_0$ = p 11

IC 9:

p 4 control for 2-3 or 5C (A_0)

p 12 —"— 10-11 or 12-13 (A_1)



~~DS~~

6055x Version 4

IC 9 pin 4 ikke til +5 men til IC 11 p 68

IC 9 pin 12 ikke til +5 men til IC 11 p 69

CS flytter, så siden af power skiftet er fri (eller power skift flytter)

IC 11 p 10 ikke direkte til +5, men pull-up til +5V R68

NMI

Henrik Stig Larsen
Christian/Christian Hammeren/

MANUAL

for

IPC/1 6055X Kortlæserprint f. Indvejningssystem.

Dansk Data Elektronik A/S

Januar 1989.

Forfatter: Allan Petersen

Januar 1989.

Indholdsfortegnelse:

Introduktion:

IPC/1 6055X modulet er et interfacekort mellem selve kortlæseren og IPC datamaten til anvendelse i indvejningssystemer. Kortet findes i tre versioner. Den ældste version (version 1) har udelukkende TTL logik til interface mellem kortlæser, LED display, relæer og et 6018 parallel I/O kort, mens de senere versioner (version 2 og version 3) er forsynet med en single chip microcomputer til indlæsning fra kortlæser og til aktivering af LEDs og relæer; kommunikationen til IPC datamaten foregår da serielt direkte til CPU kortet.

Der er endvidere på version 2 og 3 yderligere mulighed for at tilslutte et LCD display (evt. med LED backlight).

Kortet kan desuden anvendes som et generelt microkomputer kort (m. 16 k EPROM og 512 bytes RAM) med 32 digitale I/O kanaler, 4 relæ kanaler, 5 multiplexede BCD kanaler samt to serielle RS422 kommunikationskanaler.

Forskellen mellem version 2 og 3 er hovedsagelig, at version 3 har fået tilføjet lysdiodeindikeringer ved kommunikationskanalerne og ved relæerne samt nogle teststraps til valg af interne testrutiner.

Kortet indeholder følgende kredsløb:

- Formodstande til kortlæser lysdioder og inputs for detektorer i kortlæser.
- Driverkredsløb til multiplexet LED syvsegment display modul.
- Fire relæer og tilhørende drivere.
- Singlechip microkomputer m. 16k EPROM og 512 b RAM
- To serielle RS422 kanaler.
- Tilslutning for LCD displaymodul.
- Mulighed for valg af testprogrammer via straps.

Funktionsbeskrivelse:

Kortet er opbygget omkring en Hitachi HD647180X single chip microcomputer med 16k intern programlager (EPROM) og 512 bytes intern RAM, to programmerbare serielle kommunikations kanaler, 3 timere og 54 I/O pins.

B konnektoren strømforsyner lysdioderne i kortlæseren, og A konnektoren anvendes til aflæsning af kortlæserens detektorer. Lysdiode formodstandene (R30 - R45) kan monteres på en komponent sokkel for at muliggøre udskiftning/værdiændring. Modstanden R34 er formodstand for strobe lysdioden, og har derfor oftest en anden værdi end de øvrige modstande.

L konnektoren er forbundet til processorens D og E port og kan da benyttes som generelle I/O kanaler; men stikket er udlagt således, at det direkte er muligt at forbinde et fladkabel til et LCD modul, f.eks. Hitachi LM091LN (el. LM038L) 2 x 20 character displaymodul.

I så fald monteres R55, mens strappen til E6 udelades; da kan PT1 give en variabel spænding til LCD modulet til indstilling af synsvinkel.

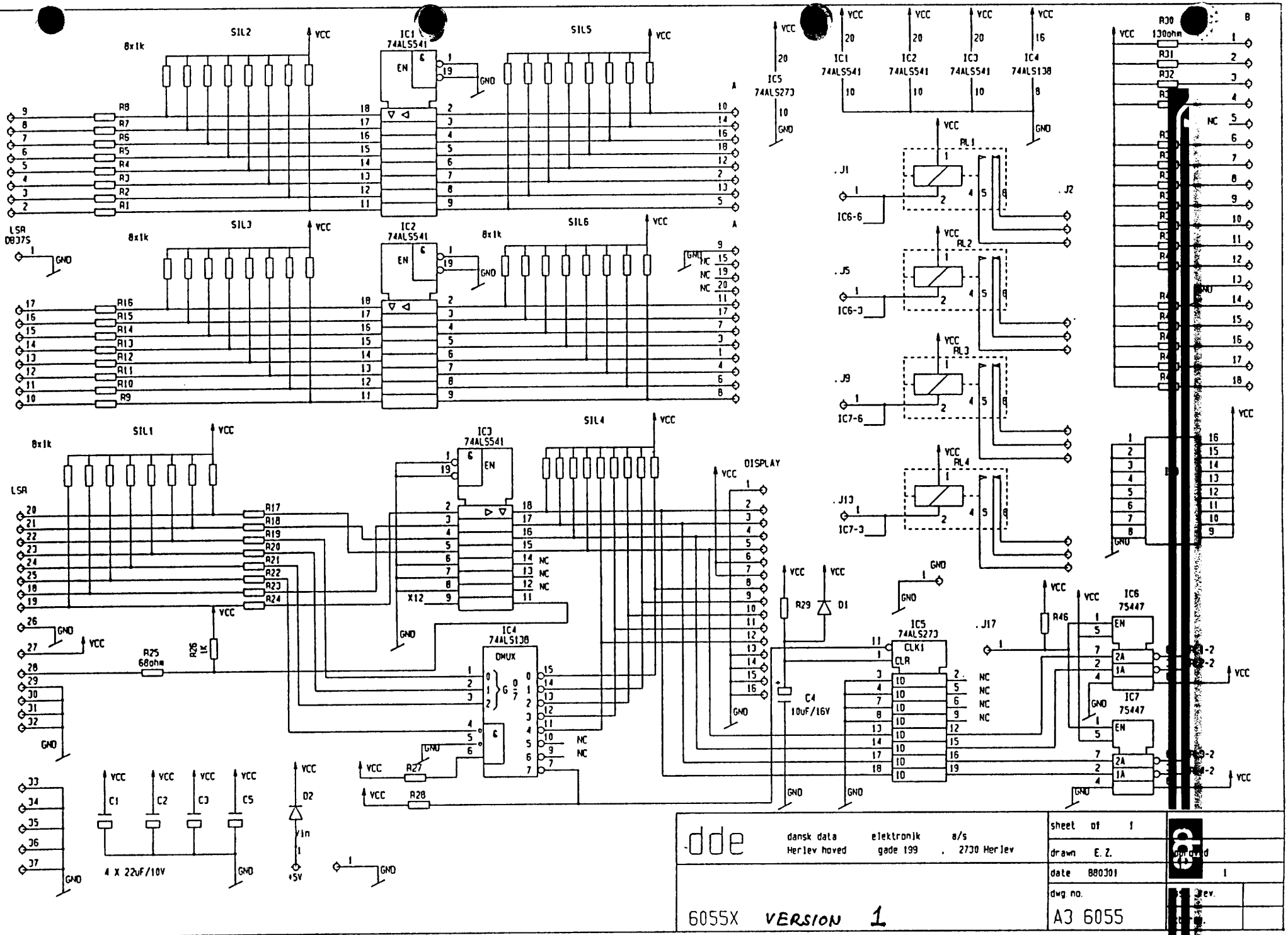
De fire relæer RL1 til RL4 har både slutte og brydekontakter ført ud til konnektoren. Alle relæerne kan disables ved at forbinde terminal ENA til GND.

Data til relæerne latches m. IC5 via en strobepuls fra dekoderen IC4, der også leverer strobe til de 5 select udgange på DISPLAY konnectoren.

P1 og P2 er to RS422 serielle kanaler. På P1 (kanal 0 på 647180) er både TxD, RxD, RTS og DCD ført ud, mens på P2 (kanal 1 på 647180) er kun TxD og RxD ført ud.

For begge kanaler er TxD og RxD forsynet med lysdioder til overvågning af kommunikationen.

Indgangene A7-A4 på processoren er normalt pull-up high, men kan strappes low til valg af eventuelle testrutiner i softwaren.



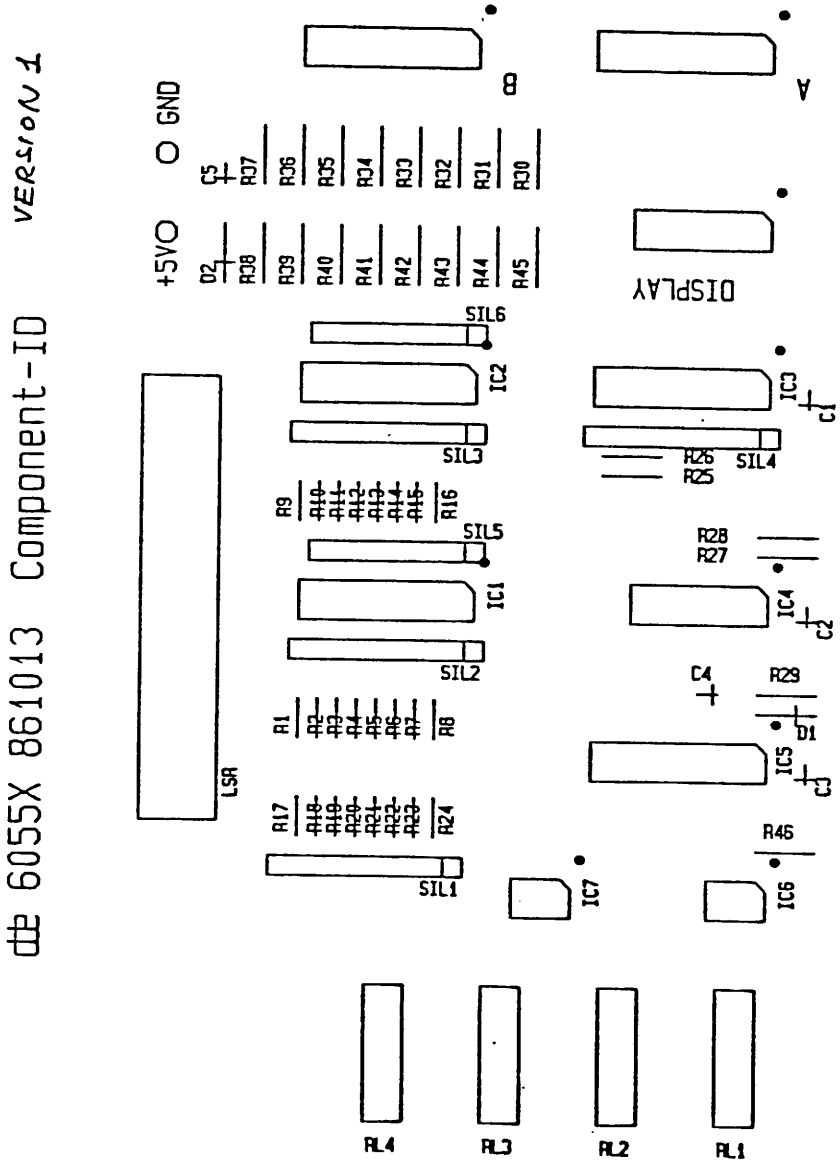
dde dansk data elektronik a/s
Herlev hoved gade 199 . 2730 Herlev

sheet	of 1
drawn	E. Z.
date	880301
dwg no.	A3 6055

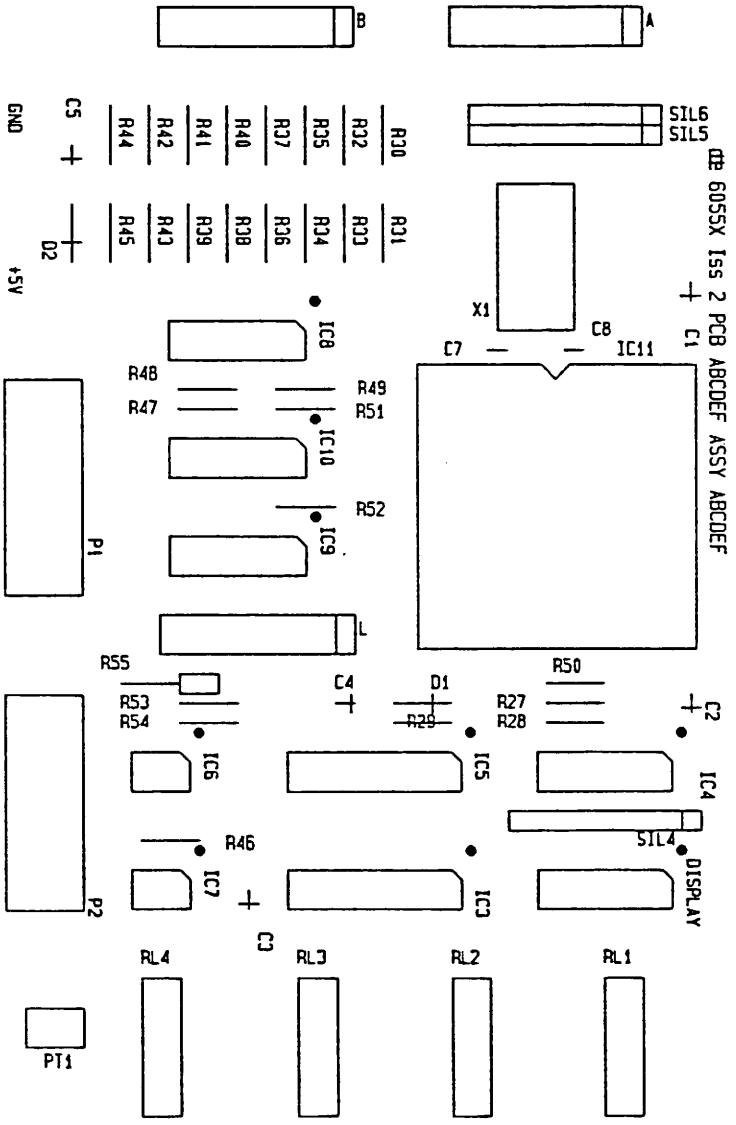
6055X VERSION 1

6055X Date: 09.01.1989 Time: 08:17:09 Scale: 1.00

Komponentplacering, version 1

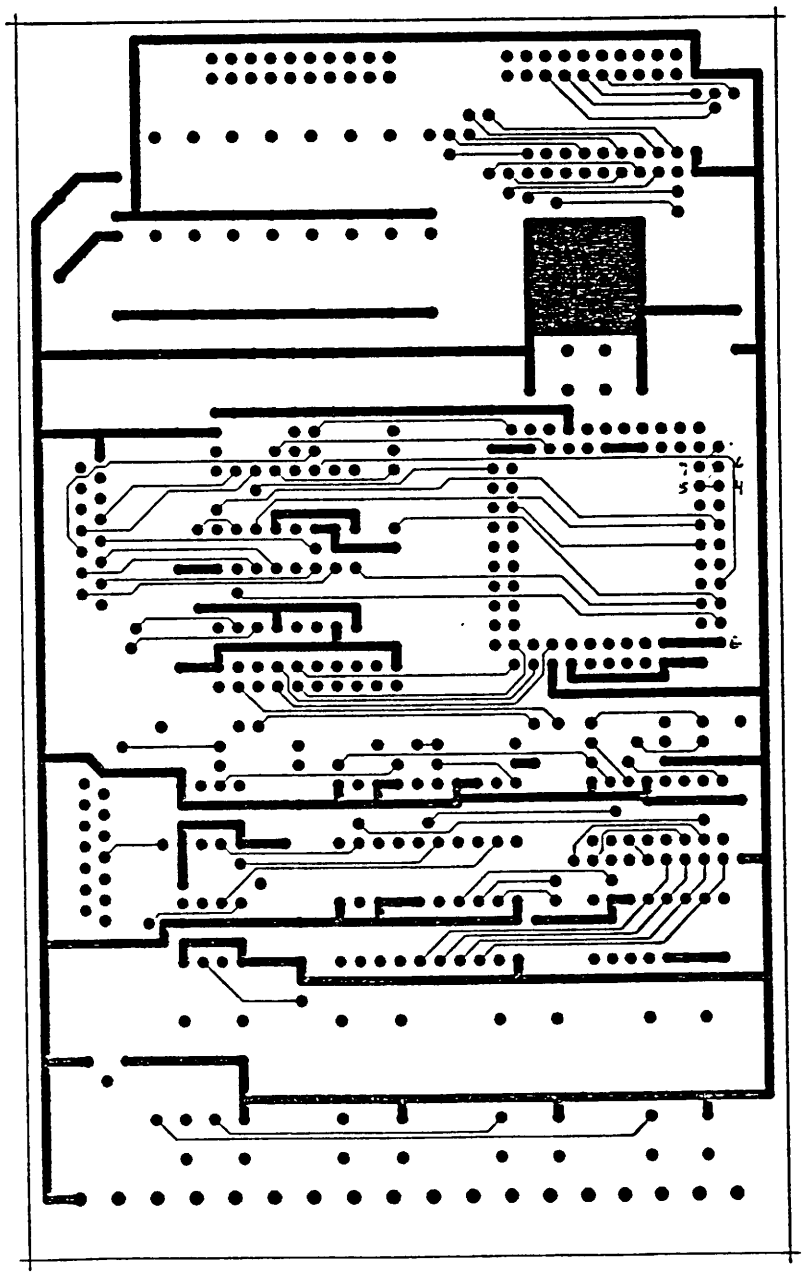


Komponentplacering, version 2



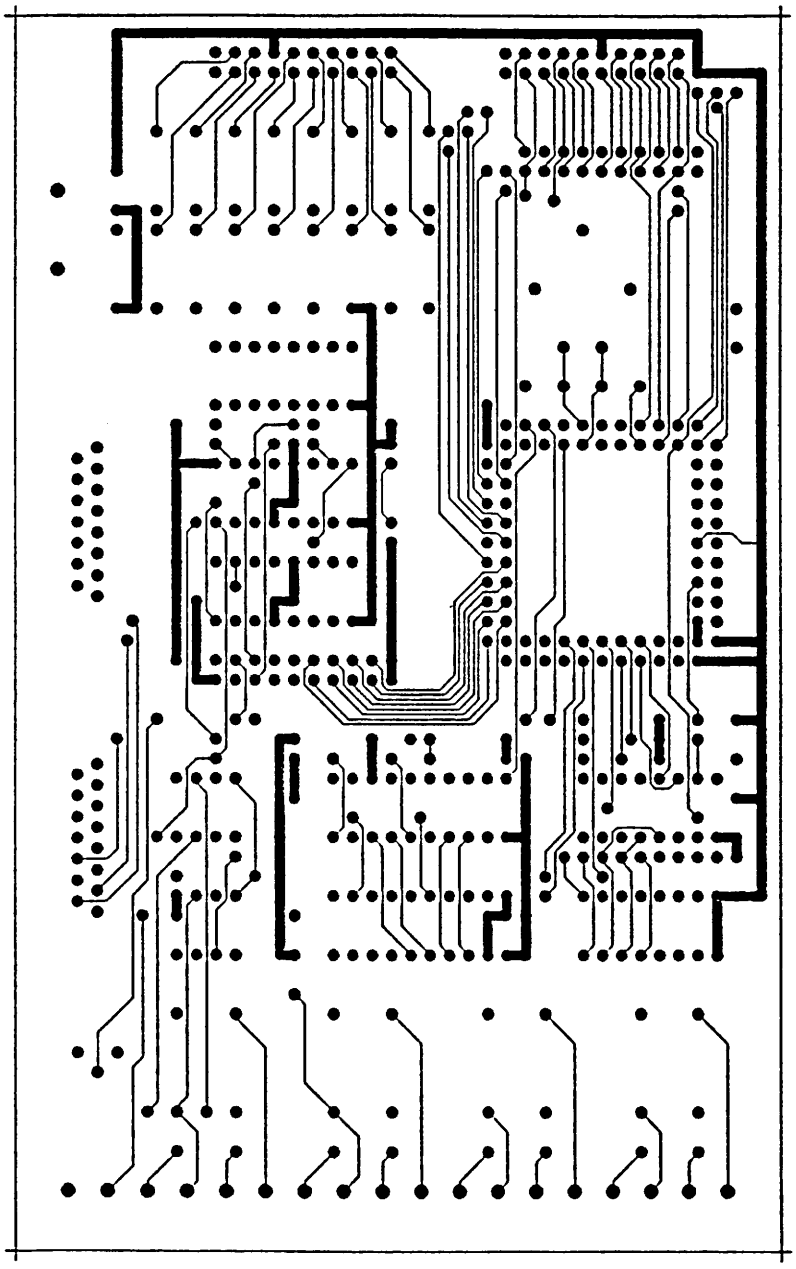
		dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf. 02-84 50 11	
Issue	Date	6055X VERSION 2.	
0	861013		
1	870601		
2	881017	Component-ID	
3			
4		Parts no.	
5		Dwg. no.	

Printlayout, version 2 (komp.side)



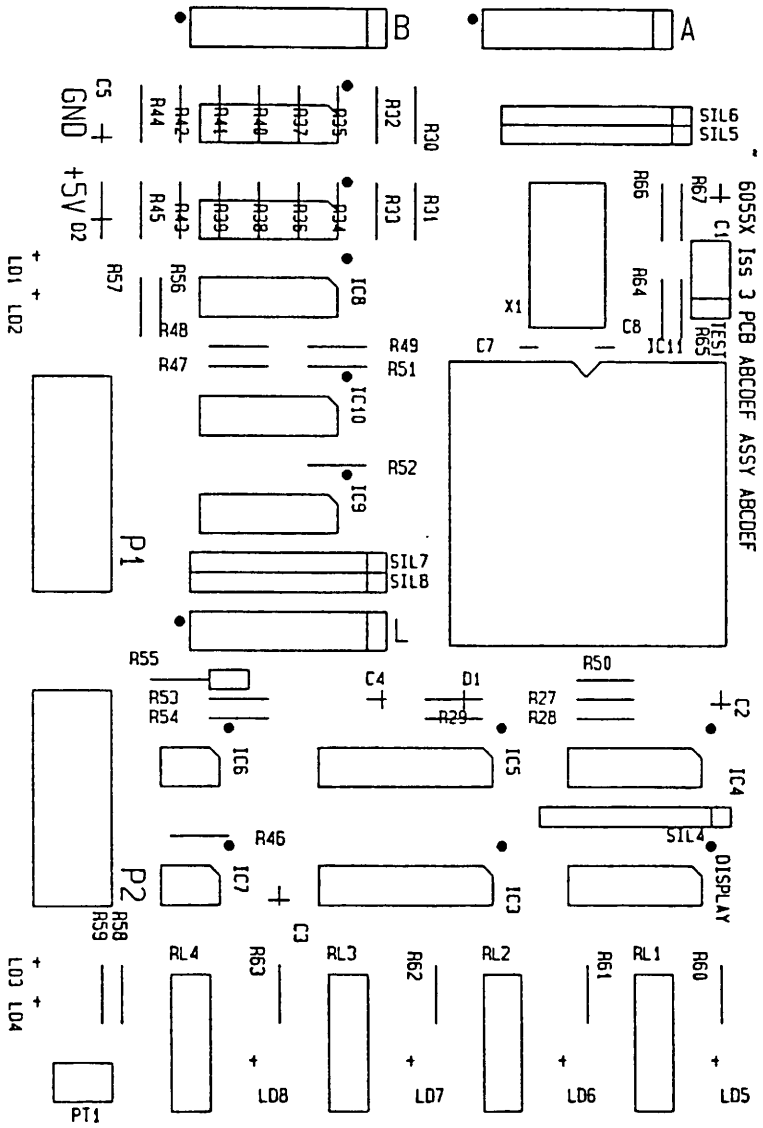
		dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf. 02-84 50 11	
Issue	Date	6055X -2	
0	861013		
1	870601		
2	881017	Layer no: 1 / Componentside	
3			
4		Parts no.	
5		Dwg. no.	

Printlayout, version 2 (solder side)



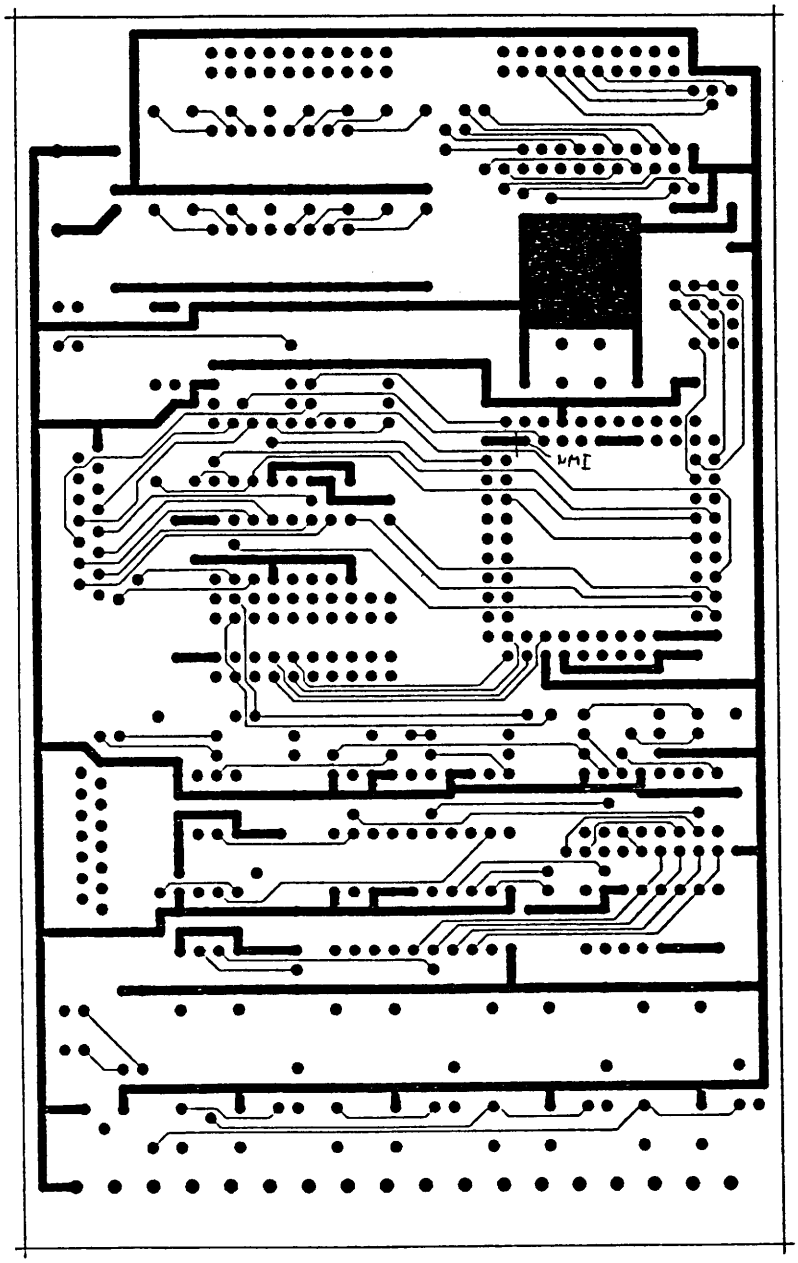
		dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf. 02-84 50 11	
Issue	Date	6055X -2	
0	861013		
1	870601		
2	881017	Layer no: 2 / Solderside	
3			
4		Parts no.	
5		Dwg. no.	

Komponentplacering, version 3



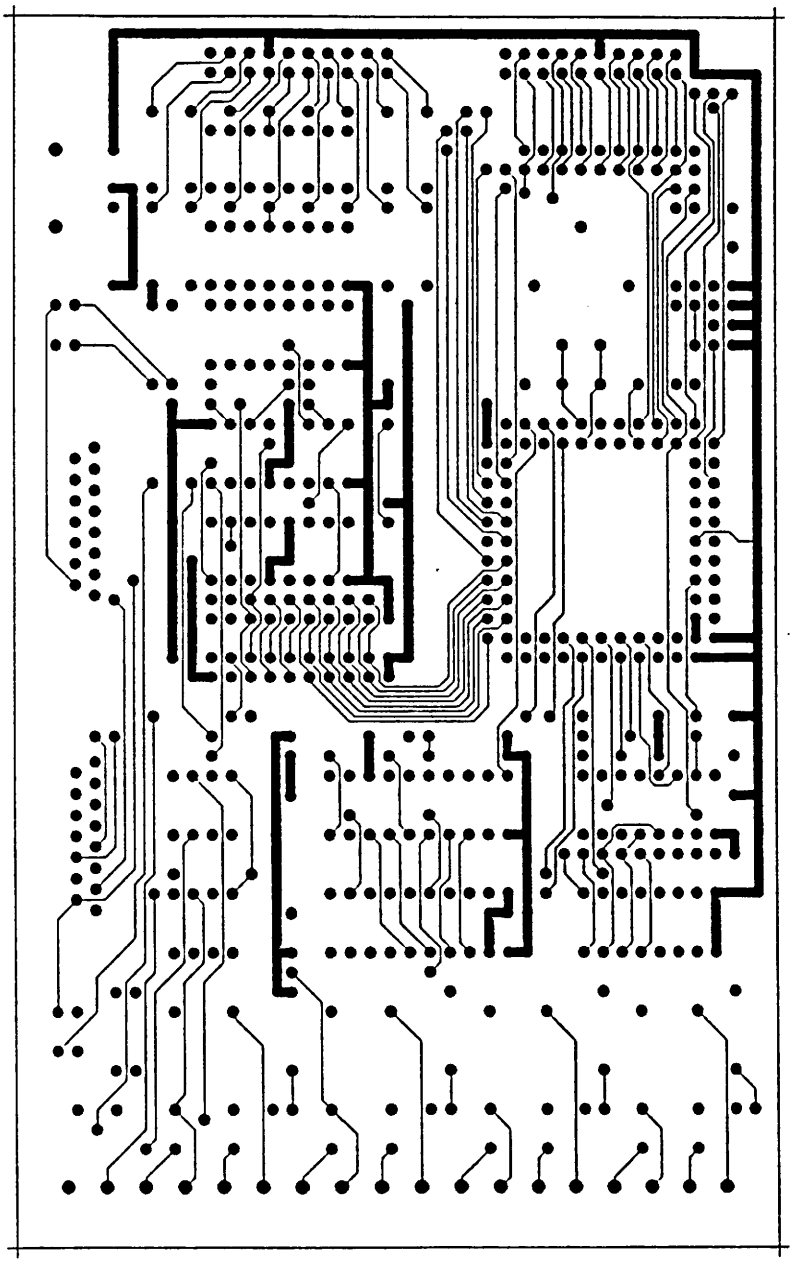
		dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf. 02-84 50 11	
Issue	Date	6055X VERSION 3	
0	861013		
1	870601		
2	881017	Component-ID	
3	890118		
4		Parts no	
5		Dwg. no.	

Printlayout, version 3 (komp.side)



		dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf. 02-84 50 11	
Issue	Date	6055X -3	
0	861013		
1	870601		
2	881017	Layer no: 1 / Componentside	
3	890118		
4		Parts no.	
5		Dwg. no.	

Printlayout, version 3 (solder side)



		dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf. 02-84 50 11	
Issue	Date	6055X -3	
0	861013		
1	870601		
2	881017	Layer no: 2 / Solderside	
3	890118		
4		Parts no.	
5		Dwg. no.	

Komponentliste: IPC 6055X version 3 !!

Navn	Komponent	Fabrikat	Pins
IC 3	SN74ALS541N	Texas	20 pin
IC 4	SN74ALS138N	Texas	16 pin
IC 5	SN74LS273N	Texas	20 pin
IC 6	SN75447N	Texas	8 pin
IC 7	SN75447N	Texas	8 pin
IC 8	(Her isættes kun sokkel)		16 pin
IC 9	DS34C87N	National	16 pin
IC 10	DS34C86N	National	16 pin
IC 11	HD647180XCP6 OTP (i sokkel)	Hitachi	84 pin PLCC
D1	Diode 1N4002		
D2	(Her monteres strap i stedet for diode)		
LD1	Lysdiode, Rød		
LD2	Lysdiode, Grøn		
LD3	Lysdiode, Rød		
LD4	Lysdiode, Grøn		
LD5	Lysdiode, Rød; Små 1e enkelte, modulstakbar type		
LD6	Lysdiode, Rød; Små 1e enkelte, modulstakbar type		
LD7	Lysdiode, Rød; Små 1e enkelte, modulstakbar type		
LD8	Lysdiode, Rød; Små 1e enkelte, modulstakbar type		
X1	Krystal 12.288 MHz	NDK	
RL1	RELÆ V23040-A0001-D201	Siemens	
RL2	RELÆ V23040-A0001-D201	Siemens	
RL3	RELÆ V23040-A0001-D201	Siemens	
RL4	RELÆ V23040-A0001-D201	Siemens	
R27	Modstand 1k		
R28	Modstand 1k		
R29	Modstand 10k		
R30	Modstand 150 ohm		
R31	Modstand 150 ohm		

R32	Modstand	150 ohm	
R33	Modstand	150 ohm	
R34	Modstand	270 ohm	<<<<<<<<<
R35	Modstand	150 ohm	
R36	Modstand	150 ohm	
R37	Modstand	150 ohm	
R38	Modstand	150 ohm	
R39	Modstand	150 ohm	
R40	Modstand	150 ohm	
R41	Modstand	150 ohm	
R42	Modstand	150 ohm	
R43	Modstand	150 ohm	
R44	Modstand	150 ohm	
R45	Modstand	150 ohm	
R46	Modstand	1k	
R47	Modstand	47k	
R48	Modstand	47k	
R49	Modstand	1k	
R50	Modstand	1k	
R51	Modstand	47k	
R52	Modstand	47k	
R53	Modstand	47k	
R54	Modstand	47k	
R55	Modstand	150 ohm	
R56	Modstand	470 ohm	
R57	Modstand	~~470 ohm~~ 330 Ω	
R58	Modstand	470 ohm	
R59	Modstand	~~470 ohm~~ 330 Ω	
R60	Modstand	470 ohm	
R61	Modstand	470 ohm	
R62	Modstand	470 ohm	
R63	Modstand	470 ohm	
R64	Modstand	10k	
R65	Modstand	10k	
R66	Modstand	10k	
R67	Modstand	10k	
SIL4	SIL Modstand	9 x 1k	
SIL5	SIL Modstand	9 x 10k	

R68 = Modst 1k

SIL6	SIL Modstand 9 x 10k	
SIL7	SIL Modstand 9 x 10k	
SIL8	SIL Modstand 9 x 10k	
PT1	Trimmepotentiometer SPECTROL 63P-103T010 (10k)	
C1	El.lyt, Sol.Al. 10 uF/16V	Philips
C2	Konds. 100 nF afkobling.	
C3	Konds. 100 nF afkobling.	
C4	El.lyt, Sol.Al. 22 uF/16V	Philips
C5	El.lyt, Sol.Al. 22 uF/16V	Philips
C7	Konds. 15 pF Ker.	
C8	Konds. 15 pF Ker.	
P1	DSUB konn. DB 15 S (vinkel)	SOURIAU
P2	DSUB konn. DB 15 S (vinkel)	—"—
A	3M20 (dobbelt pin række)	
B	3M20 (dobbelt pin række)	
L	3M20 (dobbelt pin række)	
DISPLAY	16 pin IC sokkel.	

Connektorer ved relæer er EURO-DIP terminalblok ED500/2DS.

Forbindelser til stik:

	A konnektor:	B konnector:	L konnektor:
1	Row 7	Modst.	GND
2	Card f. s.	Modst.	GND
3	Row 8	Modst.	D0
4	Row 6	Modst.	D1
5	Left edge	n.c.	D2
6	Row 5	Modst. ST	D3
7	Row 9	Modst.	D4
8	Row 4	Modst.	D5
9	GND	Modst.	D6
10	Row 3	Modst.	D7
11	Row 12	Modst.	E0
12	Strobe	Modst.	E1
13	Right edge	GND	E2
14	Row 2	Modst.	E3
15	n.c.	Modst.	E4
16	Row 1	Modst.	E5
17	Row 11	Modst.	E6/PT1
18	Row 0	Modst.	E7
19	n.c.	n.c.	GND
20	n.c.	n.c.	+ 5 V

Teststraps:

A7	*	*	GND
A6	*	*	GND
A5	*	*	GND
A4	*	*	GND

Forbindelser til stik:

	DISPLAY konn:	P1 konnector:	P2 konnektor:
1	GND	n.c.	n.c.
2	Da	TxA0N	TxA1N
3	Db	RTS0	n.c.
4	Dc	RxA0N	RxA1N
5	Dd	DCD0	n.c.
6	+5 V	n.c.	n.c.
7	+5 V	n.c.	n.c.
8	Sel 10.000	GND	GND
9	Sel 1.000	TxA0	TxA1
10	Sel 100	RTS0N	n.c.
11	Sel 10	RxA0	RxA1
12	Sel 1	DCD0N	n.c.
13	GND	n.c.	n.c.
14	GND	n.c	n.c.
15	GND	n.c.	n.c.
16	GND		

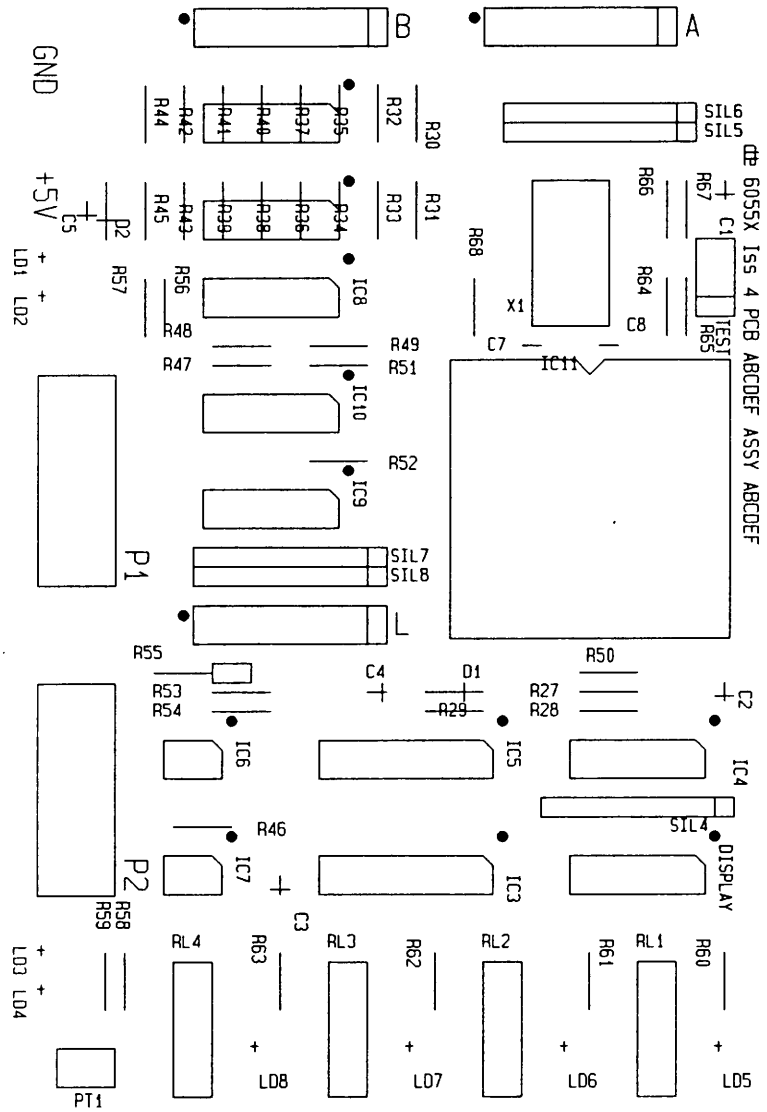
dde Dansk Data Elektronik A/S

	Initials	Page
	Date	Project

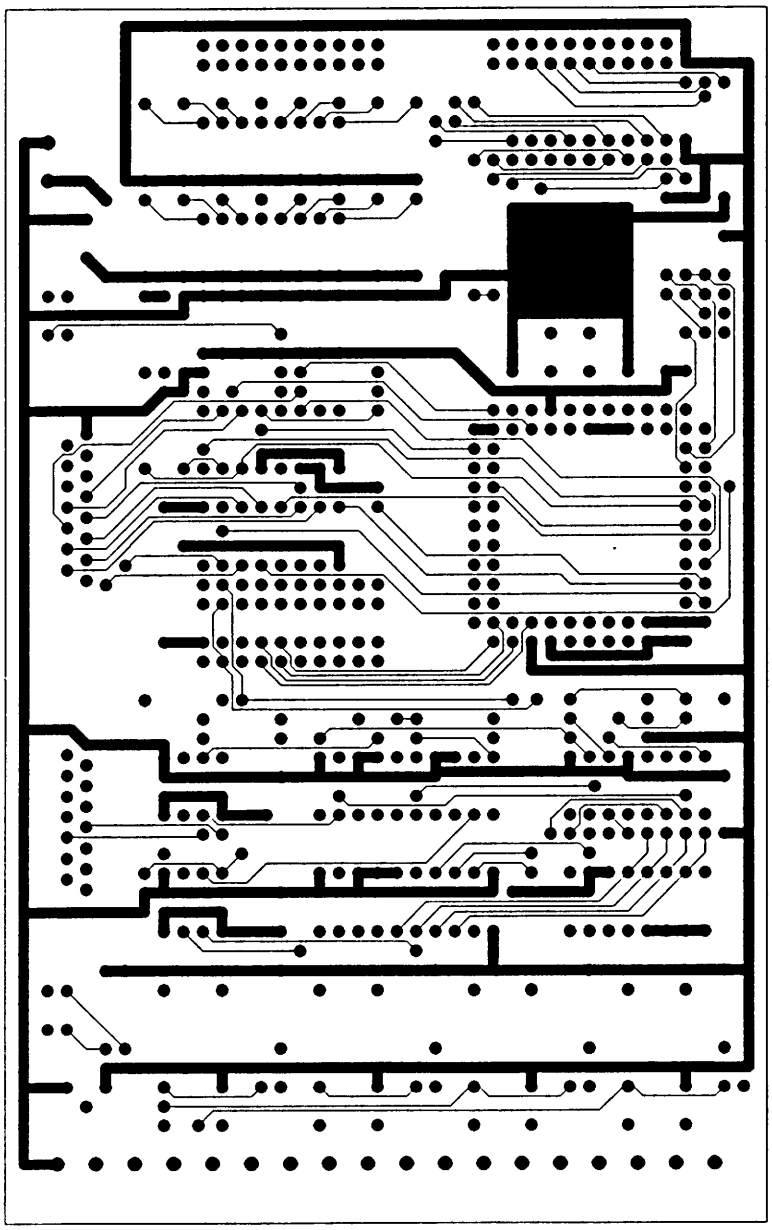
NB:

1/ På et print fra repair var der monteret en 10K Ω modst mellem p4 - p12 på IC 9. Dette er ikke standard.

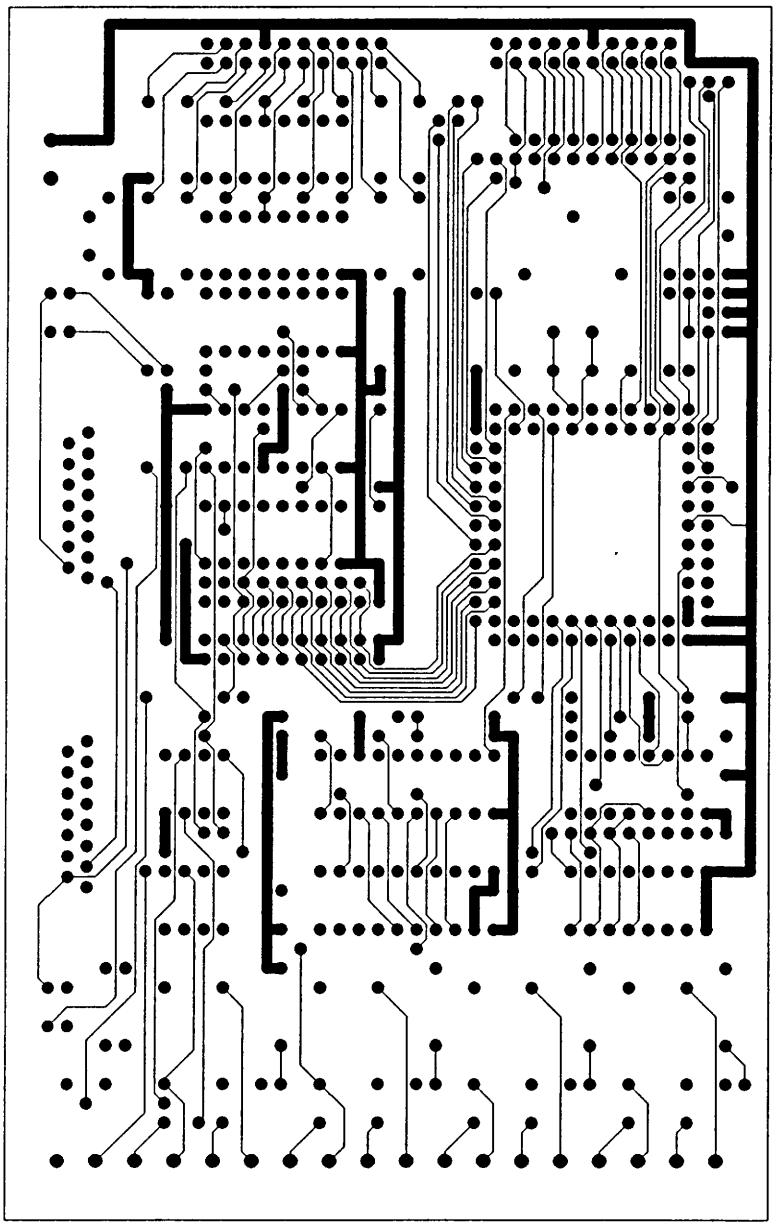
2/ For eftertiden skal reset-kond. C4 have monteret en parallelt på 22µF (= C4) (mont. på loddeside.) i.f.g. Allan P.



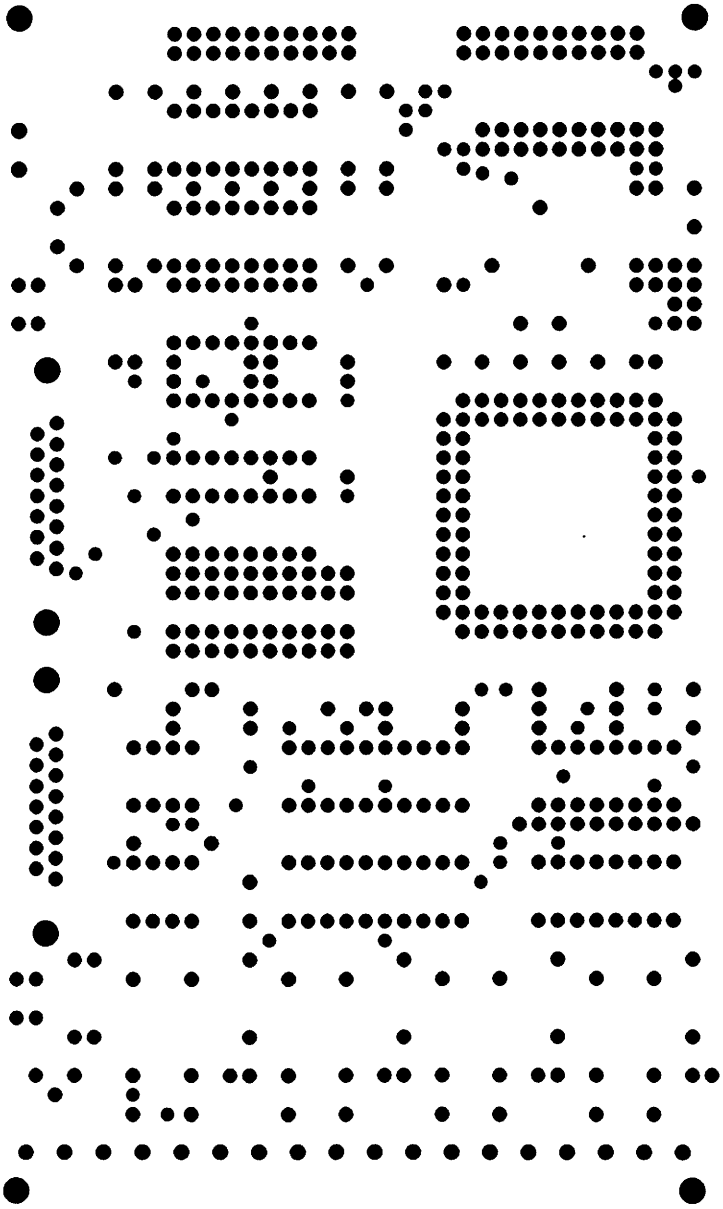
	dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf. 02-84 50 11	
Issue	Date	6055X
0	861013	
1	870601	
2	881017	Component-ID
3	890118	
4	890628	Parts no
5		Dwg. no.



	dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf. 02-84 50 11	
Issue	Date	6055X
0	861013	
1	870601	
2	881017	Layer no: 1 / Componentside
3	890118	
4	890628	Parts no.
5		Dwg. no.



		dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf. 02-84 50 11	
Issue	Date	6055X	
0	861013		
1	870601		
2	881017	Layer no: 2 / Solderside	
3	890118		
4	890628	Parts no.	
5		Dwg. no.	



		dansk data elektronik a/s herlev hovedgade 199, 2730 herlev, tlf. 02-84 50 11	
Issue	Date	6055X	
0	861013		
1	870601		
2	881017	Solder/Isolation mask	
3	890118		
4	890628	Parts no	
5		Dwg. no.	

6055 x Bolts

DSUB25 forbindelse:

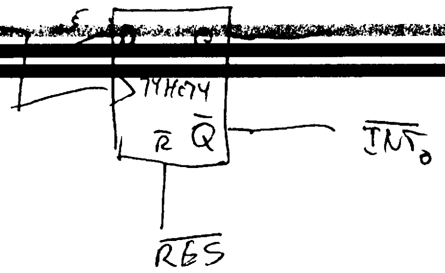
1	N.C.
2	B4
3	B5
4	B6
5	B3
6	B7
7	C0
8	C1
9	C2
10	B2
11	N.C.
12	N.C.
13	N.C.
14	N.C.
15	C6
16	N.C.
17	B1
18	C7
19	GND
20	C5
21	B0
22	C4
23	C3
24	N.C.
25	N.C.

pladekabel til A connector

(intern 10K pull-up til +5V
transient beskyttelse via
elektronik filterstik)

→ IC 8

P1 og P2
pin 1 kan strappes til +5V



til mogn. kontakt

R... el. GND eller +5V

CB flyttes

pin 4 og 12 på IC 9 til R68, C9

INT0 frigøres og får pull up. samt ϕ (R49)

NMI frigøres og får pull up → R68
til timerinterrupt ved operativsyst.

	max
IC 11	50 mA
IC 9	15 mA (85)
IC 10	1 mA (80)
IC 6	25 mA
IC 7	25 mA
Relæ	64 mA
IC 3	25 mA
IC 4	10 mA
LED	20 mA
Rv	5 mA
	240 (389) typ. 150

Lcd lys 200 mA ? 200

350

max 500 mA ~ 2,5W max

150 - 500

Poul Hermansen
DDE, Klokkerholm

Herlev, den 25. september 1990

Test Program til 6055 mark 3 kort

Hermed et test program til 6055 kortet. Programmet er ikke udelukkende beregnet til at teste det kort. Det kan måske derfor godt være lidt underligt at bruge.

Hvis du har nogen forslag til hvordan du vil have programmet til at virke skal jeg se velvilligt på sagen.

Med venlig hilsen
Dansk Data Elektronik A/S

Henrik Christensen

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DK 2730 Herlev, Denmark

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Telex: 35258 dde dk
Fax: (+45) 42 84 52 20

Reg.no. 65.295
Giro: 5 29 73 70
Bank: Handelsbanken

Test program til 6055 mark 3 kort

Dette er en kort beskrivelse af test programmet hdlctst der bruges til at teste 6055 kort med. Programmet er skrevet i forbindelse med udviklingen af PC vejebdodssystemet. Det bærer det også præg af.

Programmet kører på en PC hvor man forbinder 6055 til com1 porten. De fleste com1 porte kører efter RS232 standarden, mens 6055 kortet kører RS485 (En afart af RS422). Det betyder at man skal bruge en konverter mellem de to standarder.

Protokol

På linien mellem PC og 6055 kort benyttes en hdlc lignende protokol. Denne protokol er beskrevet i "Beskrivelse af kommunikationsprotokol i DV9800 apparatserien".

Installation

Før man kan benytte tesprogrammet skal der installeres en driver på PC'en. driveren hedder hdlc.bin og installeres ved at tilføje en linie i config.sys: device=hdlc.bin

Adresser

6055 kortet har en adresse. Denne vælges ved hjælp af de 4 straps der sidder lige ved siden af CPU'en. Ingen strap svarer til 0 og en strap svarer til 1. Strappen nærmest CPU'en er mindst betydende bit. Når der ikke er monteret nogen strap svarer det til adresse 1 (første kortlæser i vores system). De straps man monterer bliver lagt til adressen således at en strap nærmest CPU'en giver adresse 2 (første vægt i vores system).

Kommandoer

Test programmet har en række kommandoer som alle består af et enkelt bogstav og evt. en parameter. Output sendes altid til kortet der har adresse 1, mens vægtaflæsning foregår fra den enhed der har adresse 2.

Kommandoer:

t <antal> send tekster til alfadisplay
1 aflæs input fra enhed 1
2 aflæs input fra enhed 2
s skift til den anden vægt
v aflæs vægt
k kontinuert send/læs
h læs hulkort

```
m <len> længde af besked kø
f <fil> send fil
l <nr> tænd lys ( Relæ )
q quit
? denne vejledning
>
```

Vægttyper

Man vælger hvilken vægt man vil benytte ved hjælp af vsetup programmet. Det format de forskellige vægte sender er beskrevet i bilag 2. Bemærk at type 0 og 1 er parallele vægte, der kan afprøves ved at montere nogle lus i det 25 polede stik mens resten er serielle og kræver at man kan levere et signal der svarer til beskrivelsen.

Supermax programmet bro kan benyttes til at simulere de serielle vægte.

TEST AF 6056 med PC.

1/ Husk at vælge vægttype i Vsetup.
2/ hdlctst
3/ V
vægttype 0 : Vægt (null) -7
vægttype 1 : Vægt (null) 7

Husk ... prg.sys i device=hdlc.bin

En evt. mode com1 i autoexec.bat fjernes.

1. Konfiguration

Der findes en lang række parametre der kan stilles ved hjælp af setup programmet vsetup. Når man starter det kommer man ind i denne menu:

```
 Vejebod setup program
Firma oplysninger
Generelle oplysninger
Fortryd
```

Vælger man firmaoplsyninger får man dette skærmbillede:

```
 Firma oplysninger
Selskabets kortnr                          [2730                    ]
Forbogstaver til indvejningsnumre          [RFB                     ]
Tilladte pladsnumre                        [1 2                     ]
Antal adresse linier                       [2                       ]
Minimum containervægt                      [000                     ]
Momsprocent                                [22.00                   ]
Kontantgebyr                               [0.00                    ]
Foreslået felt nr                          [6                       ]
Program flag   1 - 10                      [0 0 0 1 0 0 0 0 2 2     ]
Program flag  11 - 20                      [2 0 0 1 1 2 1 0 0 0     ]
Program flag  21 - 30                      [1 0 0 0 0 0 0 0 0 0     ]
```

Vælger man punktet generelle oplysninger får man dette skærmbillde:

```
Generelle oplysninger
Timeout til Supermax ( send og modtag )    [7  30                   ]
Sekunder mellem opkaldsforsøg              [20                      ]
Databits                                   [8                       ]
Modem forbindelse                          [0                       ]
Supermax interrupt nr ( default 0xb0 )     [0xb0                    ]
Kortstander kommunikation navn             [com1                    ]
Printer navn                               [lpt1                    ]
Overførselstidspunkt for kartoteker        [04:20                   ]
Timeout for automatiske vejninger          [2                       ]
Antal vægte                                [1                       ]
Vægttype(r)                                [3  (0)                  ]
Lys type                                   [1                       ]
Vægtgrænse 1 ( Sluk kørelys )              [600                     ]
Vægtgrænse 2 ( 2 signaler, tænder rødt lys)[600                     ]
Sluk kørelys bits                          [0                       ]
Tænd rødt kørelys, bits                    [1                       ]
Tænd grønt lys, bits                       [2                       ]
Kartoteks størrelser                       [140 700 400 150 1500 10 ]
```

Kartoteks størrelserne defineres i denne rækkefølge:

Tekster, kort, kunder, priser, containere og containertyper.
Tekster indeholder tekster til pladser, områder og typer.
Det er foreløbig kun Amager forbrænding og ESØ der har container register.
Man bevæger sig rundt mellem felterne med piltasterne og kommer ud af billederne med f1. Når programmet forlades gemmes de nye oplysninger automatisk. Hvis man fortryder sine ændringer vælger man punktet fortryd. Det bevirker at programmet forlades uden at man gemmer oplysningerne.

1.1 Program flag

Man kan ændre programmets virkemåde ved at ændre på nogle parametre med setup programmet. Disse parametre kaldes program flag. I setup programmet optræder parametrene med 10 på hver linie.

Fejltyper				
nr	Beskrivelse	Værdi		
		0	1	2
1	Forkert komm. område	ignorer	logisk	fatal
2	Følgeseddel ved auto vejning	altid	debitorkode	
3	Indtast totalvægt	umuligt	muligt	
4	Slut funktion	PC stopper	DOS	
5	SEnr bruges	nej	ja	
6	Altid auto	nej	ja	
7	Curser	understreg	blok	
8	Debug kommunikation	nej	ja	
9	Container vægt udfyldt	ingen	logisk	fatal
10	Ingen bilag til Kontant kunder	ingen	logisk	fatal
11	Bilagstype 4 spærrer kunde	nej	advarsel	spærret
12	Hop til felt	fast	ledigt	
13	Adressen skal være udfyldt på kontant bilag	nej	ja	
14	Indtast bilvægt	umuligt	muligt	
15	Indtast gebyr	umuligt	muligt	
16	Pris beregningsmetode	Se nedenfor		
17	Bilag ved fremvejning	nej	ja	
18	Automatisk udskrift af bilag	nej	ja	
19	Bil kontrol	nej	logisk	fatal
20	Container kontrol	nej	logisk	fatal
21	Printer type	7 bit	PC	
22	Maks. telegram kø		antal	
23	Klokke ved vægtbelastning	nej	ja	

Parameter 16, pris beregningsmetode, angiver hvordan priskartoteket benyttes. Priskartoteket har en nøgle til hver pris. Denne nøgle består af tre tal. Betydningen af disse tal kan variere med beregningsmetoden. I øjeblikket er der følgende

metoder:

1. Nøglen bruges til plads, område og type. Det er standard metoden og den der er beskrevet i manualerne.
2. Nøglen bruges til plads og type. Man benytter altid prisen for område 0. Det betyder at prisen ikke afhænger af området.
   Bruges hos RENO Nord
3. Nøglen bruges til plads kundegruppe og type.
   Bruges hos Amagerforbrænding.

Parameter 22, maks. telegram kø, angiver hvor mange beskeder der kan stå i kø til kortstanderen. Danvægt kortstandere kan håndtere 6 telegrammer, mens andre typer normalt kun kan håndtere 1.

BISCO Vægt- og vejeindikator AFVG21

FASAN 1
FASAN 3
REFA 1
REFA 2
REFA 3

Type : '3'

600 baud even 7 bit 1 stop

Sekvens fra vægt er opdelt i:

1) STX = (1) Start på vægtsekvens
2) VÆGT 1 = (5) Første vægt
7) STATUS 1 = (1) Første status
8) VÆGT 2 = (5) Anden vægt
13) STATUS 2 = (1) Anden status

Status er opdelt på følgende måde:

0011 0--- Vægt i ro ------> Vægt i ro
0011 -1-- Anvendes ikke ?????
0011 --1- Vægt positiv - Acceptabel
0011 ---1 Vægt indenfor vejeområde ------> Vægt overbelastet (inverteret)
(vægtens arbejdsområde)

Vægtstatus i ro : 7 (0011 0111)
Vægtstatus ikke i ro : ? (0011 1111)
Vægtstatus negativ : < (0011 1100)

TYPE C NORMAL B
4800 BAUD 7 BIT EVEN 1 STOP

JBM / MITA Vægt- og vejeindikator AFVG22

ESØ 1
Vestfyn 1
RENO SYD 2

Type : '4'

9600 baud odd 7 bit 1 stop

Sekvens fra vægt er opdelt i:

1)	STX	=	(1) Start på vægtsekvens	
2)	VÆGT	=	(5) Vægtangivelse	
7)	POLARITET	=	(1) + / -	
8)	EXPONENT	=	(1)	
9)	VÆGT I RO	=	(1) V / 0 (FEJL)	---> Vægt i ro
10)	TARA	=	(1) T / 0	---> Vægt tareret
11)	OVERFLOW	=	(1) O (FEJL) / 0	---> Vægt overbelastet
12)	POWERFAIL	=	(1) P (FEJL) / 0	
13)	CHECKSUM	=	(1)	
14)	ETX	=	(1) Slut på vægtsekvens	

Type : '2'

2400 baud even 7 bit 1 stop

Sekvens fra vægt er opdelt i:

1) b = (1) Start på vægtsekvens
2) STATUS = (1) Vægtstatus
3) VÆGT = (5) Vægtsignal
4) CHECKSUM = (1) XOR checksum

Status er opdelt på følgende måde:

-1-- ---1	Vægt i ro	----> Vægt i ro
-1-- --1-	Vægt overbelastet	----> Vægt overbelas
-1-- -1--	Vægt fastholder ikke nulpunkt	----> Vægt fastholder ikke nulpunkt
-1-- 1---	Lovlig vejning igang	----> Lovlig vejning i gang
-1-1 ----	Vægt tareret	----> Vægt tareret
-11- ----	Vejeresultat negativt	

TOLEDO Vægt- og vejeindikator AFVG25 RENO NORD 1

Type : '0'

Vægtdata består af 5 cifre i BCD kode.

Der indlæses 4 cifre, idet sidste ciffer altid nul. Vejeindikatorens mindste interval er 20 kg. Mest betydende bit i mest betydende ciffer angiver fortegnet, idet '1' betyder negativt fortegn.

Type : '1'

Vægtdata består af 5 cifre i BCD kode.

Der indlæses 4 cifre, idet sidste ciffer altid nul. Vejeindikatorens mindste interval er 20 kg. Mest betydende bit i mest betydende ciffer angiver fortegnet, idet '1' betyder positivt fortegn.

Type : '5'

1200 baud even 7 bit 1 stop

Sekvens fra vægt er opdelt i:

1)	STX	=	(1) Start på vægtsekvens
2)	STATUS A	=	(1) '1'
3)	STATUS B	=	(1) a)
4)	STATUS C	=	(1) ' '
5)	VÆGT	=	(6) ' 12345'
11)	TARA	=	(6) ' 00000'
17)	CR	=	(1)

ad a)

----X---	0: vægt i ro 1: vægt ej i ro
------X-	0: positivt fortegn på vægtfelt 1: negativt fortegn på vægtfelt

		Initialer/dato AP 4/5 -88	Side
		Revideret	Projekt Isolator

PC port side

DB25P

pin nr. i cirkel

4/2 OPTO

Terminal side

DB25S

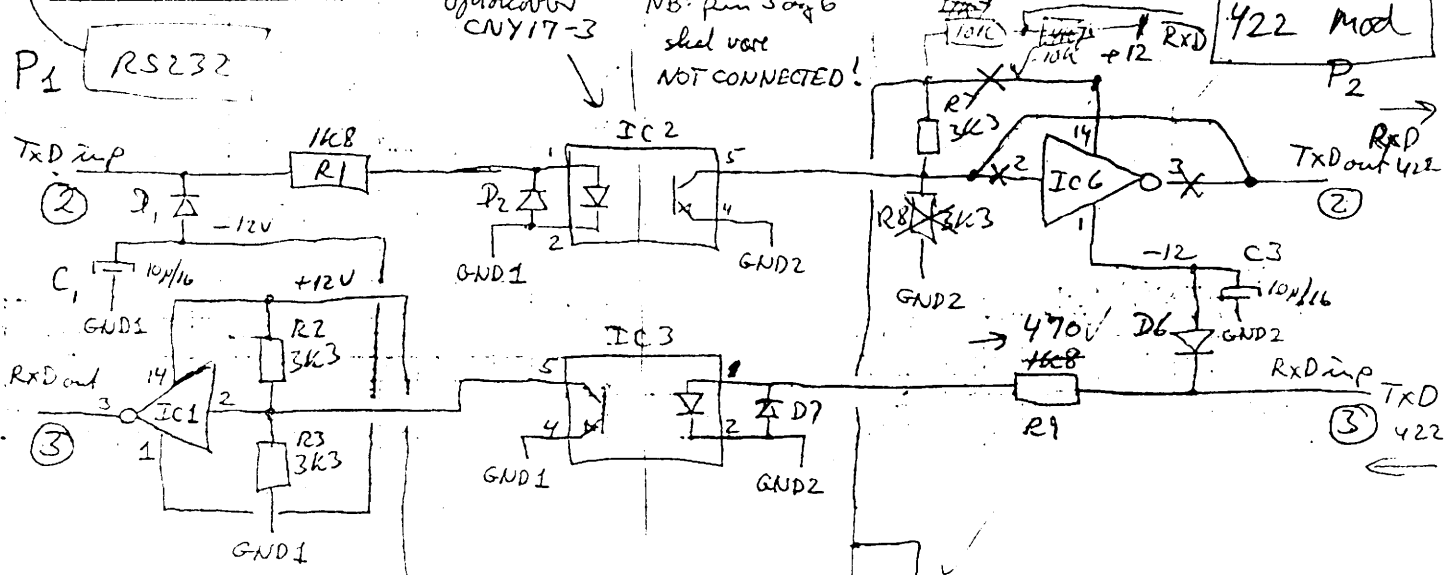
P1 RS232

opto CNY17-3

NB: pin 3 og 6 skal vare NOT CONNECTED!

422 mod

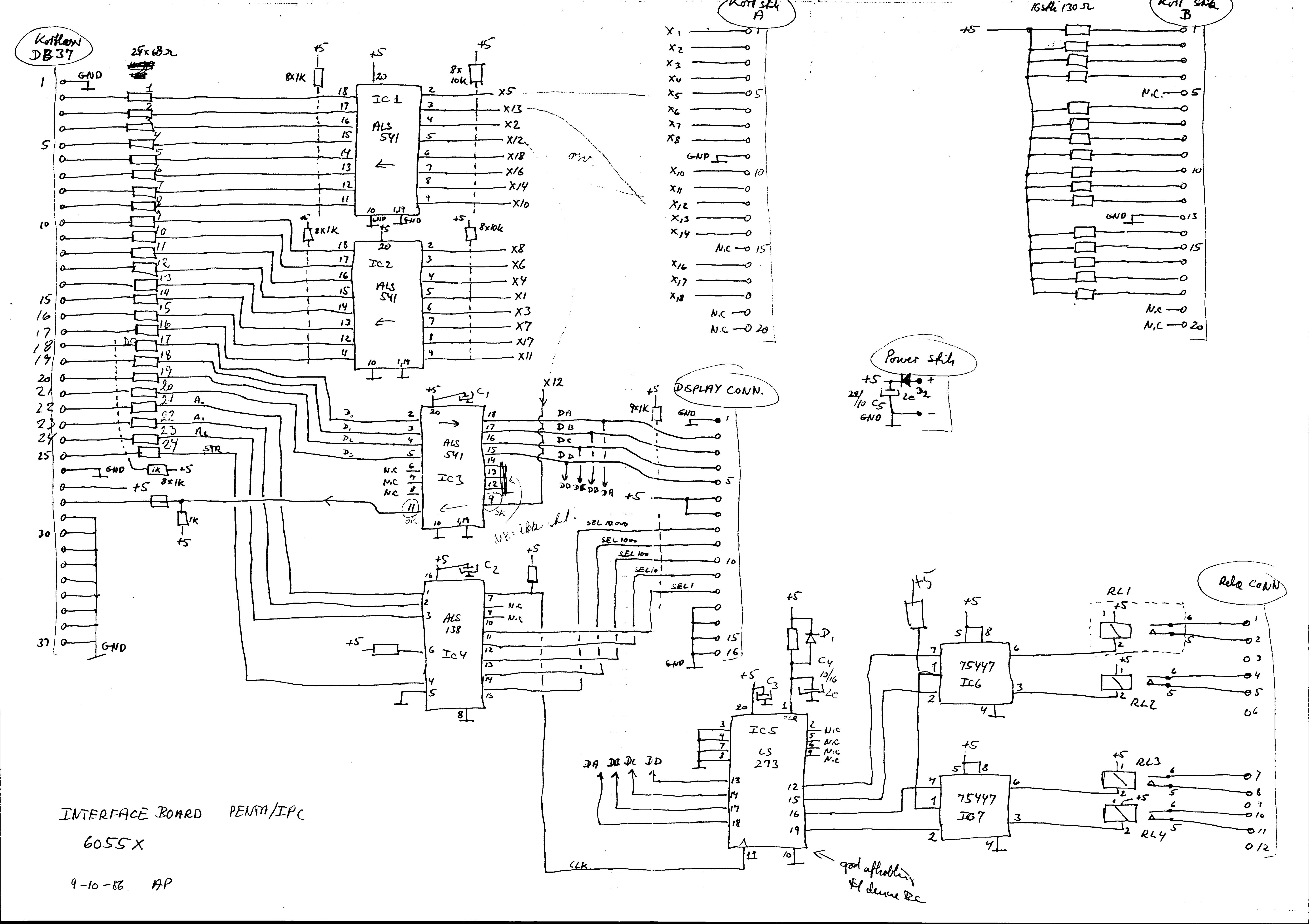
P2



GND1 og GND2 er galvanisk adskilt

Alle dioder 1N4148

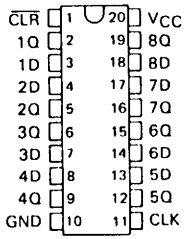
Driver IC er DS 14C88N


Kotlow DB37
25x68Ω
8x1K
8x10K
IC1 ALS 541
IC2 ALS 541
IC3 ALS 541
IC4 ALS 138
IC5 LS 273
75447 IC6
75447 IC7
Kontakt A
Kontakt B
16stk 130Ω
Power stik
DISPLAY CONN.
Rele CONN
RL1
RL2
RL3
RL4
SEL 10.000
SEL 1000
SEL 100
SEL 10
SEL 1
CLK
STR
GND
+5
N.C
INTERFACE BOARD PENTA/IPC
6055X
9-10-86 AP

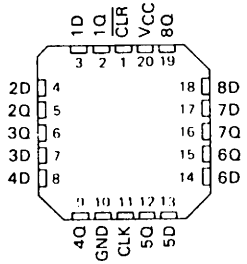
AUGUST 1983

- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS273 . . . J PACKAGE
SN74ALS273 . . . N PACKAGE
(TOP VIEW)



SN54ALS273 . . . FH PACKAGE
SN74ALS273 . . . FN PACKAGE
(TOP VIEW)



description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

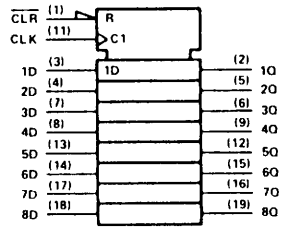
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The SN54ALS273 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS273 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

logic symbol

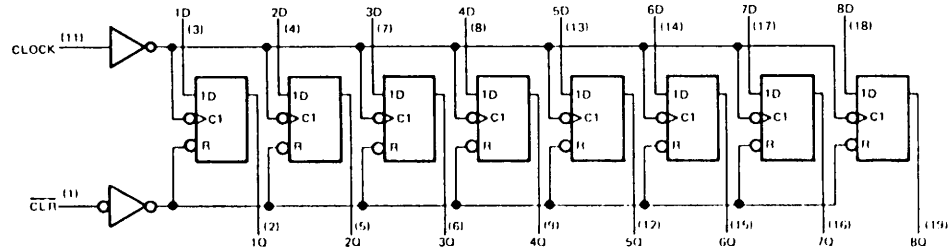


Pin numbers shown are for J and N packages.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS273 . . . . . −55°C to 125°C
SN74ALS273 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

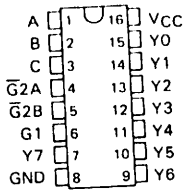
			SN54ALS273			SN74ALS273			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High level input voltage		2			2			V
V_{IL}	Low level input voltage				0.8			0.8	V
I_{OH}	High level output current				−1			−2.6	mA
I_{OL}	Low level output current				12			24	mA
f_{clock}	Clock frequency		0		30	0		35	MHz
t_w	Pulse duration	$\overline{CLR}$ low	10			10			ns
		CLK high	16.5			14			
		CLK low	16.5			14			
t_{su}	Setup time before CLK	Data	10			10			ns
		Clear inactive state	10			10			
t_h	Hold time, data after CLK		0			0			ns
T_A	Operating free air temperature		55		125	0		70	°C

Additional information on these products can be obtained from the factory as it becomes available.

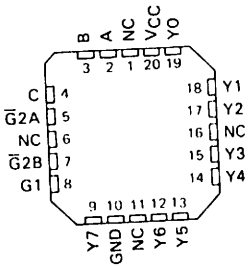
D2661, APRIL 1982

- Designed Specifically for High-Speed Memory Decoders and Data Transmission Systems
- Incorporates 3 Enable Inputs to Simplify Cascading and/or Data Reception
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS138 . . . J PACKAGE
SN74ALS138 . . . N PACKAGE
(TOP VIEW)



SN54ALS138 . . . FH PACKAGE
SN74ALS138 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

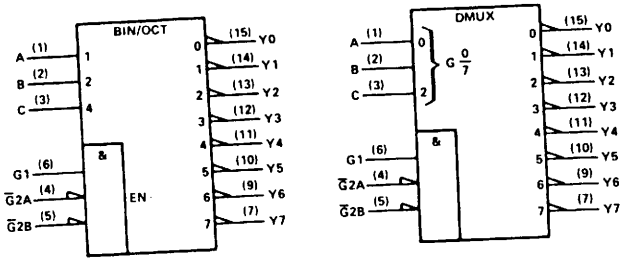
description

The 'ALS138 circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

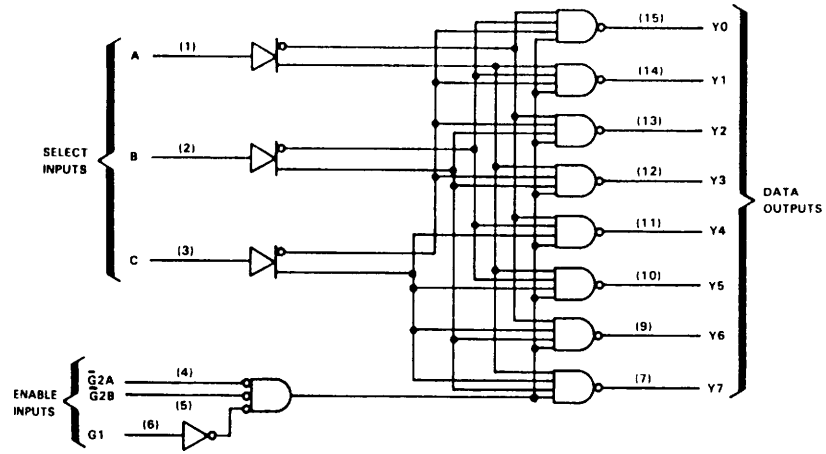
The SN54ALS138 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS138 is characterized for operation from 0°C to 70°C.

logic symbols (alternatives)



Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

FUNCTION TABLE

ENABLE INPUTS		SELECT INPUTS			OUTPUTS							
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

Absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free air temperature range: SN54ALS138 . . . . . −55°C to 125°C
SN74ALS138 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

switching characteristics (see note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS539			SN74ALS539			
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y							ns
t_{PHL}									
t_{PLH}	$\overline{G}$	Y							ns
t_{PHL}									
t_{PLH}	P	Y							ns
t_{PHL}									
t_{PZH}	$\overline{OC}$	Y							ns
t_{PZL}									
t_{PHZ}	$\overline{OC}$	Y							ns
t_{PLZ}									

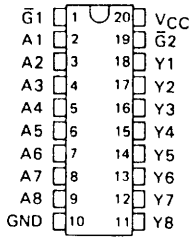
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

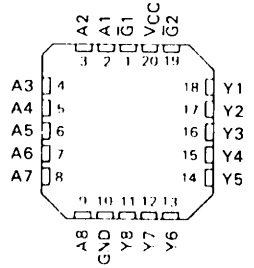
D2661 APRIL 1982

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Data Flow-Thru Pinout (All Inputs on Opposite Side from Outputs)
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

SN54ALS540, SN54ALS541 . . . J PACKAGE
SN74ALS540, SN74ALS541 . . . N PACKAGE
(TOP VIEW)



SN54ALS540, SN54ALS541 . . . FH PACKAGE
SN74ALS540, SN74ALS541 . . . FN PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed to have the performance of the popular SN54ALS240/SN74ALS240 series and, at the same time, offer a pinout with inputs and outputs on opposite sides of the package. This arrangement greatly enhances printed circuit board layout.

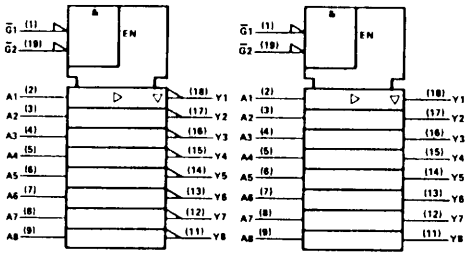
The three-state control gate is a 2-input NOR such that if either $\overline{G}1$ or $\overline{G}2$ is high, all eight outputs are in the high-impedance state.

The 'ALS540 provides inverted data and the 'ALS541 provides true data at the outputs.

The SN54ALS540 and SN54ALS541 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS540 and SN74ALS541 are characterized for operation from 0°C to 70°C.

logic symbols

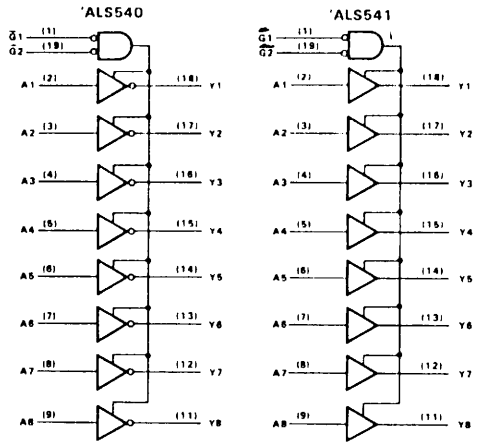
'ALS540 'ALS541



Pin numbers shown are for J and N packages.

logic diagrams (positive logic)

'ALS540 'ALS541



ADVANCE INFORMATION

This page contains information on a new product. Specifications are subject to change without notice.

SERIES 75446
DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 12630, DECEMBER 1978 – REVISED NOVEMBER 1980

- Very Low Power Requirements
- Very Low Input Current
- Characterized for Use to 350 mA
- No Output Latch-Up at 50 V (After Conducting 300 mA)
- High-Voltage Outputs (70 V Min)
- Output Clamp Diodes for Transient Suppression (350 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications

description

The '75446 dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching times. The SN75446, SN75447, SN75448, and SN75449 provide AND, NAND, OR, and NOR drivers, respectively. These devices have diode-clamped inputs as well as high-current, high-voltage inductive-clamp diodes on the outputs.

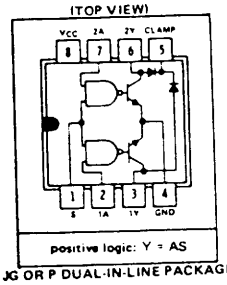
The '75446 drivers are characterized for operation from 0°C to 70°C.

SN75446
FUNCTION TABLE
(EACH AND DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

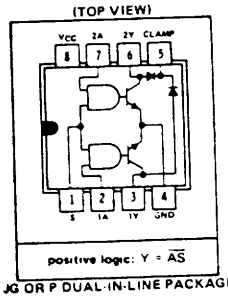


SN75447
FUNCTION TABLE
(EACH NAND DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

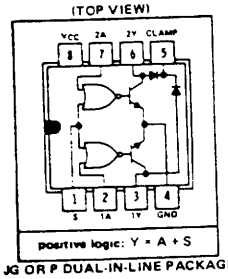


SN75448
FUNCTION TABLE
(EACH OR DRIVER)

INPUTS		OUTPUT
A	S	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)

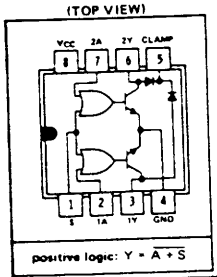


SN75449
FUNCTION TABLE
(EACH NOR DRIVER)

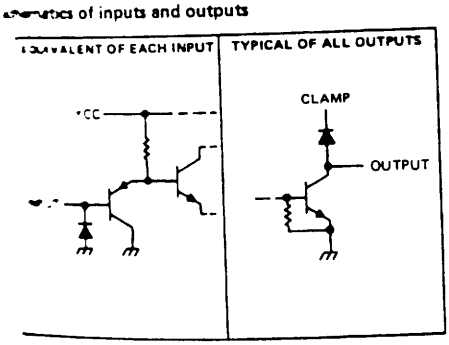
INPUTS		OUTPUT
A	S	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = high level
L = low level

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



schematics of inputs and outputs



Version 1.1

Supermax Vejebod

Brugervejledning

Dansk Data Elektronik a/s
09.03.89

INDHOLD

1. Indhold

Denne vejledning indeholder en meget kort introduktion til betjening af Supermax datamater og en mere tilbundsgående gennemgang af programmet *Supermax Vejebod.*

Gennemgangen af programmet er af to dele. Første del indeholder en beskrivelse af hvordan man generelt betjener terminalen og anden del beskriver nogle normale situationer.

2. Generelt

Betjeningen af progammet *Supermax Vejebod* minder om den måde andre Supermax programmer betjenes på. Her tænkes især på begreberne hårde og bløde funktionstaster.

De hårde funktionstaster er tasterne fra f1 til f8. De har (stort set) den samme betydning i alle programmer. Deres betydning fremgår af en strimmel der er monteret på keyboardet.

De bløde funktionstaster er tasterne fra f9 til f16. Deres betydning er forskellig fra program til program, og fremgår af det *skakbrædt* der vises på den nederste del af skærmen.

2.1 Start af programmet

Programmet startes ved at man logger ind på Supermaxen under brugernavnet **vejebod.**

På skærmen vil der efter et kort øjeblik vise sig et skærmbillede der ser nogenlunde således ud:

```
                                                  Hukommelse
          Veje nr.                    Huk nr.
         1 Kundenr
           Område
         2 Type
           Totalvægt
         3 Bil vægt
         4 Container vægt
         5 Container nr
           Affaldsvægt
Deponering
Statsafgift
      Netto
       Moms
      Total

                                6

       Indtast nr
Vægt                  Faktura                          Hent opl.            Gentegn
Vægt+kort Vejebilag Følgesed. Fremvej.  TilbagevejVis log   Beregn    Godkend
```

2.2 Flytning af markøren

Markøren vil stå lige ved siden af teksten 'Indtast nr'. Når man står i dette felt kan man springe til et andet felt ved at indtaste feltets nr efterfulgt af et tryk på return tasten. Ved trykke på pil-op og pil-ned kan man også flytte mellem de forskellige felter. Return tasten bevirker at markøren flytter til det næste felt.

2.3 Kontrol af data

Når et felt forlades, undersøges det om det der står i feltet er lovligt. Hvis det ikke er det skrives øverst til venstre på skærmen hvad der er galt, og markøren bliver i feltet. Der er i denne situation to måder at komme ud af feltet på. Enten taster man lovlige data ind, eller også sletter man indvejningen ved at trykke på SHIFT F1.

Kundenr Når feltet *kundenr* forlades vises kundens navn nederst til højre på skærmen.

kundeoplysningerne overføres kun fra administrationen når man beder om det. Hvis administrationen har ændret i kundeoplysningerne må man derfor overføre oplysningerne inden de bruges.

Affaldstype Når feltet *Type* forlades vises navnet på affaldstypen nederst til højre på skærmen.

Vægtfelter I vægtfelterne undersøges om vægten er negativ.

2.4 Hårde funktionstaster

Det er kun nogle få af de faste funktionstaster der har nogen betydning i vejebods programmet.

Slut f1 bruges til at forlade programmet. når man trykker på denne tast kommer man ud til velkomst billedet.

Fortryd SHIFT F1 fortyder en indvejning. Det vil sige at den bliver markeret som slettet og sendt til administrationen som en slettet indvejning. Indvejningen bliver dog først sendt næste gang man godkender en vejning.

Hjælp f2 bevirker at de nederste to linier der viser de bløde funktions tasters betydning bliver slået til eller fra.

Indsæt tegn f6 indsætter et tegn på markørens plads. Den er egentlig kun relevant i forbindelse med indtastning af adresser.

Slet tegn SHIFT F6 sletter et tegn på markørens plads.

f7 f7 flytter markøren hen til slutningen af et felt, mens SHIFT F7 flytter markøren hen til begyndelsen af et felt.

f8 f8 sletter et felt fra markørens position og hen til resten af feltet, mens SHIFT F8 sletter hele feltet.

2.5 Bløde funktionstaster

De nederste to linier på skærmen viser de bløde funktionstasters betydning. Den nederste linie viser betydningen hvis man blot trykker på funktionstasten, mens den næstnederste viser betydningen hvis man trykker på SHIFT tasten samtidigt.

Det første felt svarer til f9 og det sidste felt svarer til f16. De felter der er vist i negativ, svarer til de taster der er markeret med mørkt på strimlen.

Vægt+kort f9 bruges til at overføre kortdata fra kortlæseren og vægten fra brovægten. I modsætning til IPC udstyret aflæses disse data ikke automatisk, men kun når man trykker på f9.

Det har den fordel at indholdet af felterne ikke pludselig ændres inden man godkender en vejning.

Der kan gå op til et par sekunder fra kortet puttes i kortlæseren og til det kan aflæses af Supermaxen. Supermaxen vil vente op til 10 sekunder på at der kommer data fra kortlæseren.

Hvis kortet er aflæst forkert vises det øverst på skærmen.

Markøren placeres i container vægt feltet efter funktionen.

Vægt SHIFT F9 aflæser brovægten, men ikke kortlæseren. Funktionen bruges hvis man laver en vejning uden kort, eller hvis man vil aflæse en ny vægt, men bibeholde kort oplysningerne.

Hvis det blæser kan brovægten stå og svinge. Hvis vægten ikke er i ro skrives det øverst på skærmen. Det er ment som en advarsel, man kan godt lave en vejning alligevel.

Markøren placeres i container vægt feltet efter funktionen.

Vejebilag f10 udskriver et vejebilag. Det kan man altid gøre.

Følgeseddel f10 udskriver en følgeseddel.

Faktura SHIFT F11 udskriver en faktura. Denne funktion benyttes kun i forbindelse med kontant betaling.

Fremvej f12 laver en fremvejning. Det bruges hvis man ikke kender bilens tomvægt, normalt fordi bilen ikke har noget kundekort.

Funktionen bevirker at totalvægten og kundeoplysninger gemmes til senere brug. Vægt og eventuelle kortdata skal være læst inden funktionen benyttes. For at lette betjeningen vises oplysningerne hele tiden øverst til højre på skærmen. Samtidigt skrives et vejebilag.

Tilbagevej f13 laver en tilbagevejning. Efter et tryk på tasten, flyttes markøren op i feltet 'Huk nr.' Her vælges den ønskede linie ved at angive det nummer der står i det første felt i området med fremvejninger. Samtidigt hermed aflæses brovægten, og det største tal af den nye totalvægt og den gamle vægt bruges som totalvægt og det andet tal bruges som bilvægt.

Vis log f14 viser de sidste 20 vejninger på skærmen. Hver linie indeholder dato, klokkeslet, pladsnr, affaldstype, indvejningsnr, kundenr, totalvægt, bilvægt, containervægt, containrnr, affaldsvægt, kontantnr og et statusfelt. I status feltet betyder K kontant, O offline, og S slettet.

Hver linie ser således ud:

```
09.03.89 14:03 1 2 RFB00173 30001 47770 15580 1440 3 30750   O
```

Hent Oplysninger SHIFT F14 henter oplysninger om affaldstyper, priser og kunder fra administrationens Supermax.

Denne funktion behøver man kun benytte hvis der ændres priser, eller hvis der ændres i kundeoplysningerne. Alle oplysningerne lagres på vejebodens Supermax, så det er altså ikke nødvendigt at udføre funktionen efter f.eks. en strømafbrydelse.

Beregn f15 beregner prisen for affaldet. Man kan benytte funktionen hvis man gerne vil se hvad prisen bliver, men i forbindelse med udskrivning af følgesedler og godkendelse af indvejninger bliver funktionen udført automatisk, så man behøver egentlig ikke bruge den.

Godkend f16 godkender en vejning. Det kontroleres at indvejningen er lovlig, prisen beregnes og vejningen sendes til administrationen. Herefter gøres klar til næste vejning.

Gentegn SHIFT F16 bevirker at skærmbilledet tegnes på ny. Denne funktion benyttes hvis skærmen har været slukket eller der er kommet til at stå noget på skærmen som kommer fra andre programmer.

3. Betjeningsforløb

I dette afsnit beskrives hvordan man laver de almindelige indvejninger.

3.1 Vejning med kundekort

Vejning med kundekort er den almindligste og hurtigste måde at veje på. Det skyldes at man kan nøjes med at veje bilen en gang, da bilens tomvægt fremgår af kundekortet.

Proceduren er følgende:

1. Bilen kører op på vægten.
2. Chaufføren stikker kundekortet i kortlæseren og tager det ud igen.
3. I vejeboden aflæses brovægten og oplysningerne fra kundekortet ved at trykke på f9 (Vægt + Kort).
4. Bilen kører ned af vægten.
5. På skærmen kan man nu se kundens navn, området og affaldstypen.
6. Hvis affaldstypen er en anden end den der fremgår af kortet ændres denne.
7. Hvis kunden vil have en følgeseddel skrives denne ved at trykke på f11.
8. Vejningen godkendes ved tryk på f16.

3.2 Vejning med kundekort og container

Biler med container vejes på samme måde, men man er nødt til at udfylde feltet med containervægt. Den nemmeste måde at komme ind i feltet med container vægt er ved at skrive 5 i linienr feltet. Hvis man ikke kender container vægten må man lave en to gangs vejning.

3.3 To gangs vejninger

Det er nødvendigt at veje både før og efter aflæsning hvis man ikke kender bilens tomvægt. Det kan f.eks. være fordi bilen ikke har noget kundekort eller fordi containervægten ikke fremgår af containeren.

Proceduren er følgende:

1. Bilen kører op på vægten.
2. Vægten aflæses med et tryk på f9.
3. Bilen kører ned og læsser af.
4. Felterne med kundenr og affaldstype udfyldes.
5. Tryk på fremvejning, f12. Oplysningerne overføres nu til et ledigt felt til højre på skærmen. Samtidigt udskrives et vejebilag. På vejebilaget står hukkommelses nummeret. Det er et tal mellem 1 og 9.
6. Når bilen har læsset af kører den op på vægten igen.
7. Nu trykkes på f13, tilbagevejning.
8. Hukkommelses nummeret angives. Når dette er sket aflæses vægten automatisk.

9. Bilen kører ned af vægten.
10. De oplysninger der blev gemt ved den første vejning hentes nu frem.
11. Hvis der er nogen felter der ikke blev udfyldt før udfyldes de nu.
12. Der skrives eventuelt en følgeseddel ud.
13. Vejningen godkendes.

4. Systemadministration

4.1 Start af Supermax

Supermaxen tændes ved at dreje nøglen på forsiden af maskinen så nøglen står lodret. Der kommer nu lys i displayet på forsiden. Når der efter ca 30 sekunder står -3 i displayet på forsiden skal der komme noget tekst ud på skærmen.

Maskinen finder ud af om den er blevet lukket på en kontrolleret måde eller om der har været strømafbrydelse. Hvis der har været strømafbrydelse undersøges det om disken er i orden. Hvis det ikke er tilfældet skrives **BOOT UNIX** på skærmen. Man skal så dreje nøglen over i vandret (slukke for strømmen) og tænde igen.

Når disken er kontrolleret skal man angive dato og klokkeslet når man bliver bedt om det.

Efter ca 1 minut, hvor der bliver skrevet forskellige ting på skærmen er Supermaxen klar.

På skærmen er der nu et velkomst billede og nederst står der **Login:**

Man skriver nu brugernavnet **vejebod** efterfulgt af return og kommer ind i vejebodsprogrammet.

4.2 Nedlukning af Supermax

Inden man slukker for strømmen til Supermaxen skal man gå ud af vejebodsprogrammet og logge på med brugernavnet **powerdown.**

Man kommer ind i et program der stopper Supermaxen. Programmet spørger om man vil lave en *Express powerdown.* Det besvares med **y.** Hvis man fortryder nedlukningen svarer man q.

Når der på skærmen står **system is down** kan man slukke for strømmen ved at dreje nøglen over i vandret stilling.

4.3 Backup

De eneste filer der ændres under kørslen, er filen med sekvensnumre og filen med indvejninger der ikke har kunnet overføres til administrationen. Der er derfor ikke nogen grund til at lave jævnlig backup.

5. Ændringer i forhold til IPC udstyret

Supermaxen har langt større lager kapacitet en IPC'en og har derfor plads til alle kunderne lokalt. Det medfører at det ikke er nødvendigt at kalde administrationens

computer op for at finde ud af om et kundenummer er gyldigt. Kundenumre testes derfor så snart de tastes ind. Det medfører på den anden side at man må overføre alle oplysninger hver gang der bliver ændret i kundeoplysningerne.

Den store lagerkapacitet betyder også at man kan gemme mere end 5000 vejninger lokalt. Der er derfor ingen grund til at holde øje med hvor mange vejninger der ligger lokalt.

Aflæsning af kort og brovægt foregår ikke løbende, med kun på anmodning fra operatøren. Det har den fordel at vægten ikke står og ændrer sig mens man er igang med en vejning, og kundeoplysningerne ikke pludselig forsvinder fordi den næste chauffør stikker et kort i kortlæseren.

Programmet indeholder ikke nogen tælleværker. Alle de oplysninger der ligger i tælleværkerne kan man få ved at lave nogle statistik udskrifter på administrationens maskine.

Man kan ikke ændre i setup af f.eks. indvejningsnumre fra vejebods programmet. Det gøres ved at redigere nogle filer med en editor.