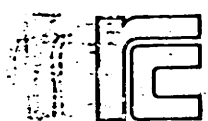


Title:

HPS 802

SEQUENCE ANALYZER

GENERAL DESCRIPTION

 A REGNECENTRALEN

RC SYSTEM LIBRARY: FALKONERALLE 1 DK-2000 COPENHAGEN F

RCSL No: 44-RT 1471

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CONTENTS

PAGE

1.	GENERAL DESCRIPTION	1
2.	OPERATIONAL DESCRIPTION	2
3.	FRONTPANEL	3
4.	ELECTRICAL CHARACTERISTICS	4

1. GENERAL DESCRIPTION

1.

The HPS 802 is a general sequence analyzer with a storing capacity of 64 words by 9 bits.

It is usefull for debugging microprograms, examining sequences which for reasons of speed-demands cannot be stepped though at a slow rate, etc.

2. OPERATIONAL DESCRIPTION

2.

HPS 801 records 9 bit words at times defined by the clock input.

When clocked, HPS 802 writes the contents of the 9 input lines into a 64 by 9 bit RAM, and counts the address register controlling the RAM. The address counting is modulo 64, that is when running, the RAM holds the latest 64 steps in the sequence.

When the contents at the inputs, at clocktime, corresponds to the comperat⁰er switch setting, the HPS 802 proceeds recording 31 more steps and then halts, turning on the pointer digits. Hence when halted, the HPS 802 holds a picture of 32 steps before the stop condition occurred and 31 after, and it is now possible by means of the 'stepup' and 'stepdown' push bottoms to examine this picture.

The stop condition comperat⁰er is besides the 9 recorded inputs expanded by 3 non recorded inputs, which contributes to the condition in the same way as the 9 data inputs. To fullfill the stop condition, all inputs should equal the corresponding switch settings; that is, if a switch is set to 1, the data input must be 1 to meet the condition, if the switch is in the X setting, this partial condition is a don't care, i.e. the data input does not contribute to the stop condition.

When stopped, the pointer digits indicate 00, and point at the first word in the sequence, that satisfied the programmed stop condition, stepping up will bring the succeeding words on the led display, and stepping down will display the preceding words, if you are looking back in time, the $\div$ lamp will light. It is possible that the stop condition occurs before 32 clock pulses have been received since start, then of course not all 32 preceding words in the RAM can be defined. This situation is indicated when it is not possible to 'stepdown' beyond a certain point (the first word recorded).

If the pointer digits show a 01 after you have depressed the 'startbutton', the HPS does not receive any clock pulses.

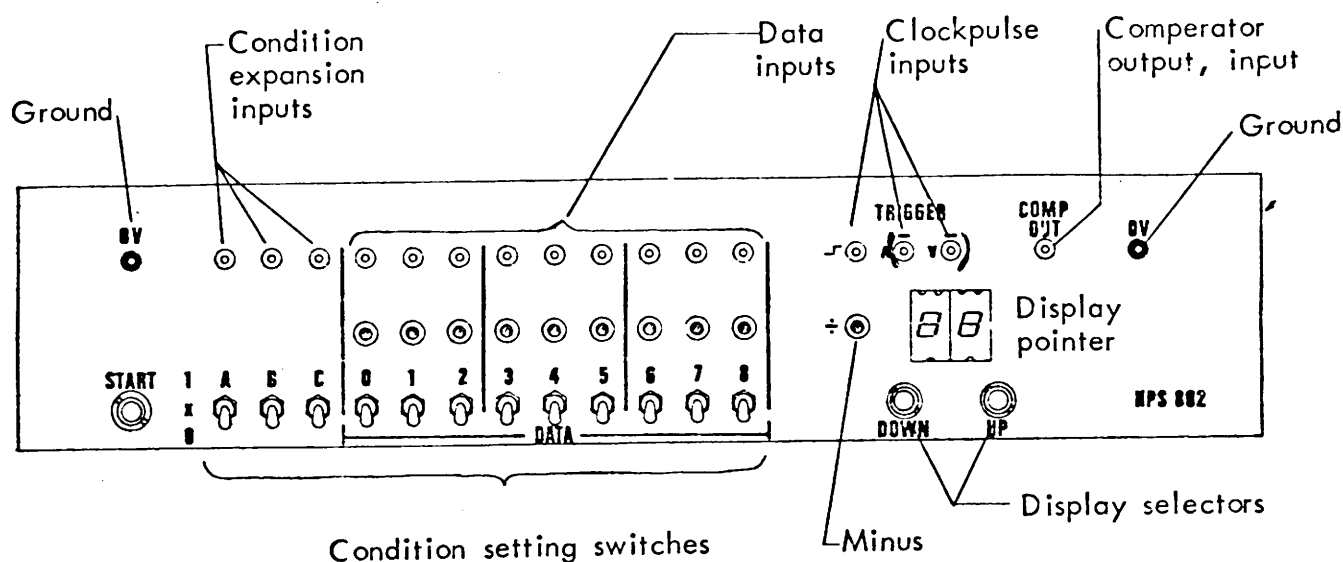
The clock pulse inputs are labelled with a boolean expression, preceded by a $\leq$ sign. The meaning of this is, that clocktime is defined as the moment, at which the value of the expression (with the three inputs as variables) transits from 0 to 1.

For proper operation it is recommended that the data inputs are stable from 2 nanosecs to 15 nanosecs after the clocktime, as the recorded word is the state of the datainputs during this interval.

If the clock frequency is greater than appr. 11 MHz, not all steps in the sequence will be recorded.

3. FRONTPANEL

3.



- | | | |
|-------------------------------|--|---|
| Data inputs : | Data to be recorded | } Fed into 'stop condition' comparator. |
| Condition expansion inputs : | | |
| Data display : | Display the values of the recorded bits. | |
| Display pointer : | Indicates the displayed step no. in octal representation, relative to the stop condition word. Is off while running. | |
| Minus lamp : | Part of display pointer, lights if events before the stop condition are displayed. | |
| Stepup push button : | Steps forwards in the recorded data. | |
| Stepdown push button : | Steps backwards in the recorded data. | |
| Comparator setting switches : | Have three positions each : 1, X, and 0; in X-position does the corresponding input not contribute to the stop condition. | |
| Comp out connector : | Is 'wireanded' with all comparator outputs, may be used for triggering a scope on the set conditions or expanding with one more HPS 802. | |
| Clock input connectors : | The 'low' to 'high' transition of the inputs combined in the way printed on the frontplate, defines the moment of recording. | |

4. ELECTRICAL CHARACTERISTICS

4.

Power requirements : 220V AC 50 Hz 20W

All inputs are fully TTL compatible.

Recognition as a low input : $U \leq 0,8 \text{ V}$

Recognition as a high input : $U \geq 2,0 \text{ V}$

(Maximum input voltages : -1 low,
5,5 high)

Datainputs 0-8, A, B, and C :

Input current low: max -250 μA

Input current high ($U_i = 2,7 \text{ V}$) max 50 μA

($U_i = 5,5 \text{ V}$) max 1 m A

Clock inputs

Input current low max - 2 mA

Input current high ($U_i = 2,7 \text{ V}$) max 50 μA

($U_i = 5,5 \text{ V}$) max 1 mA

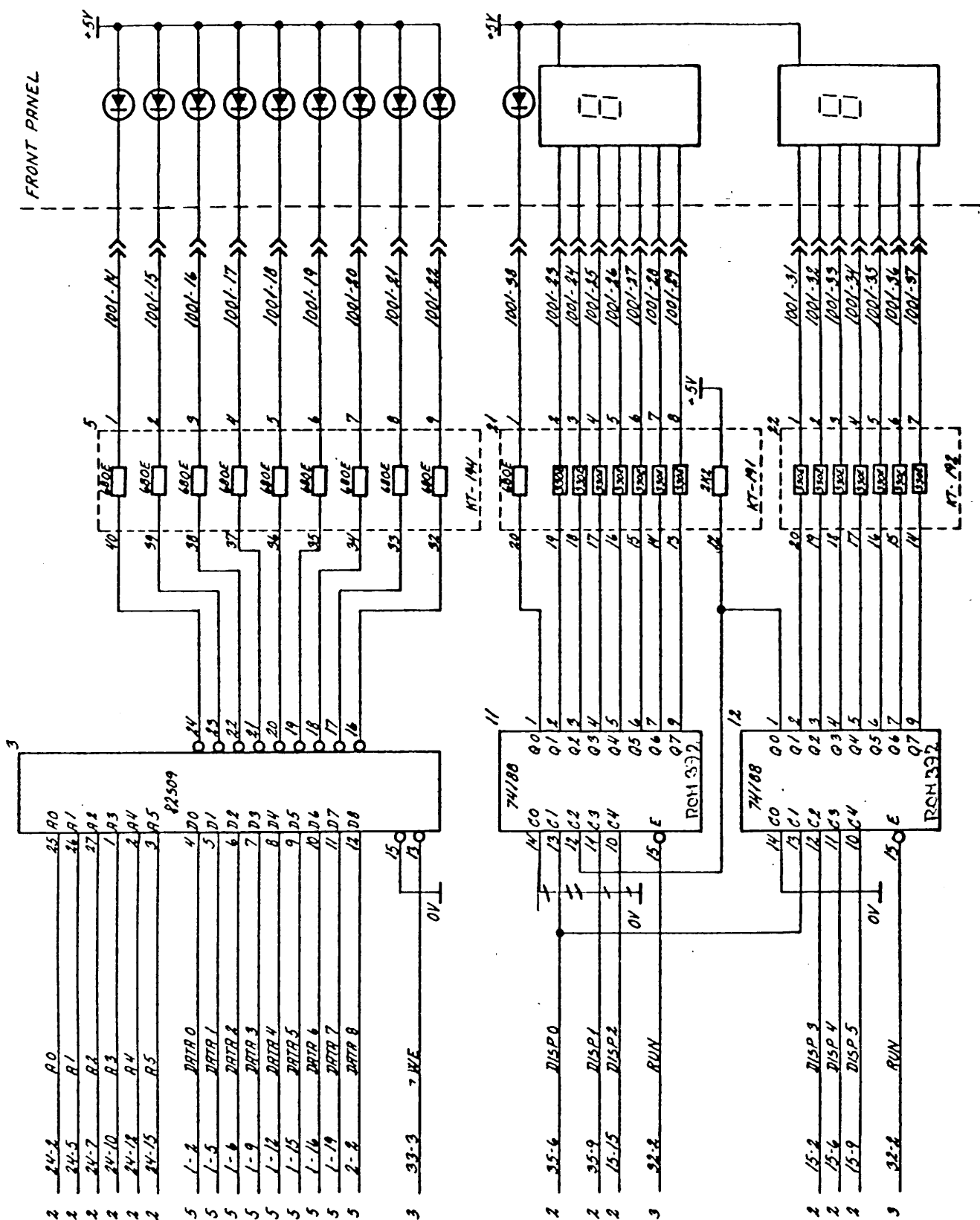
For proper operation:

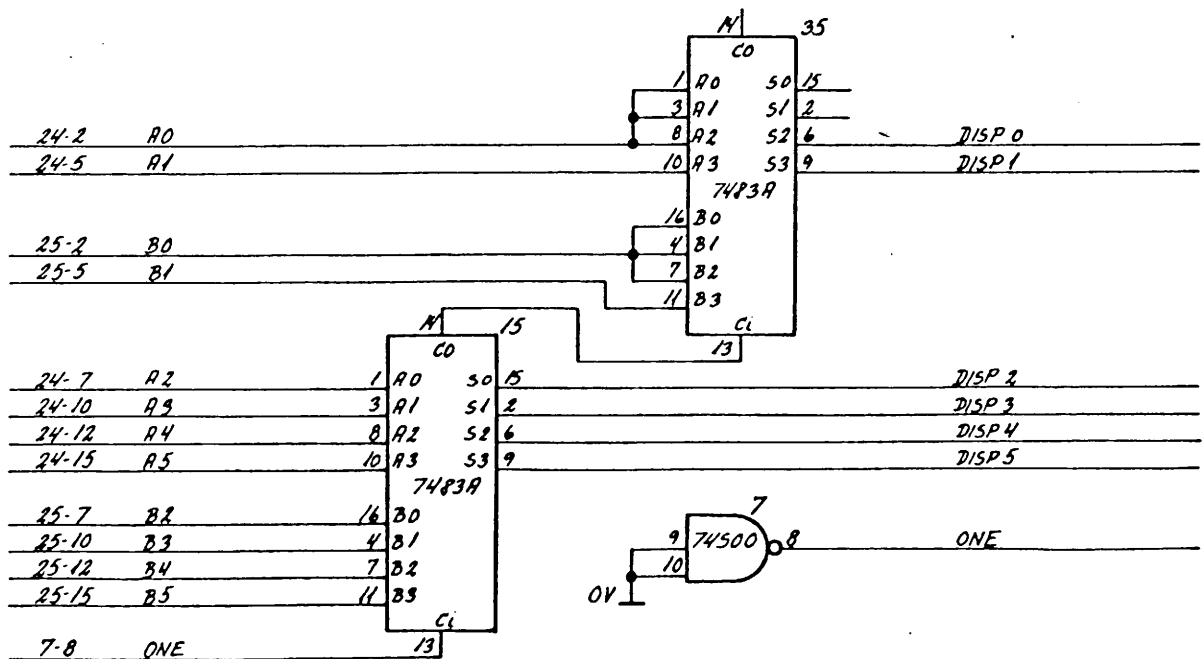
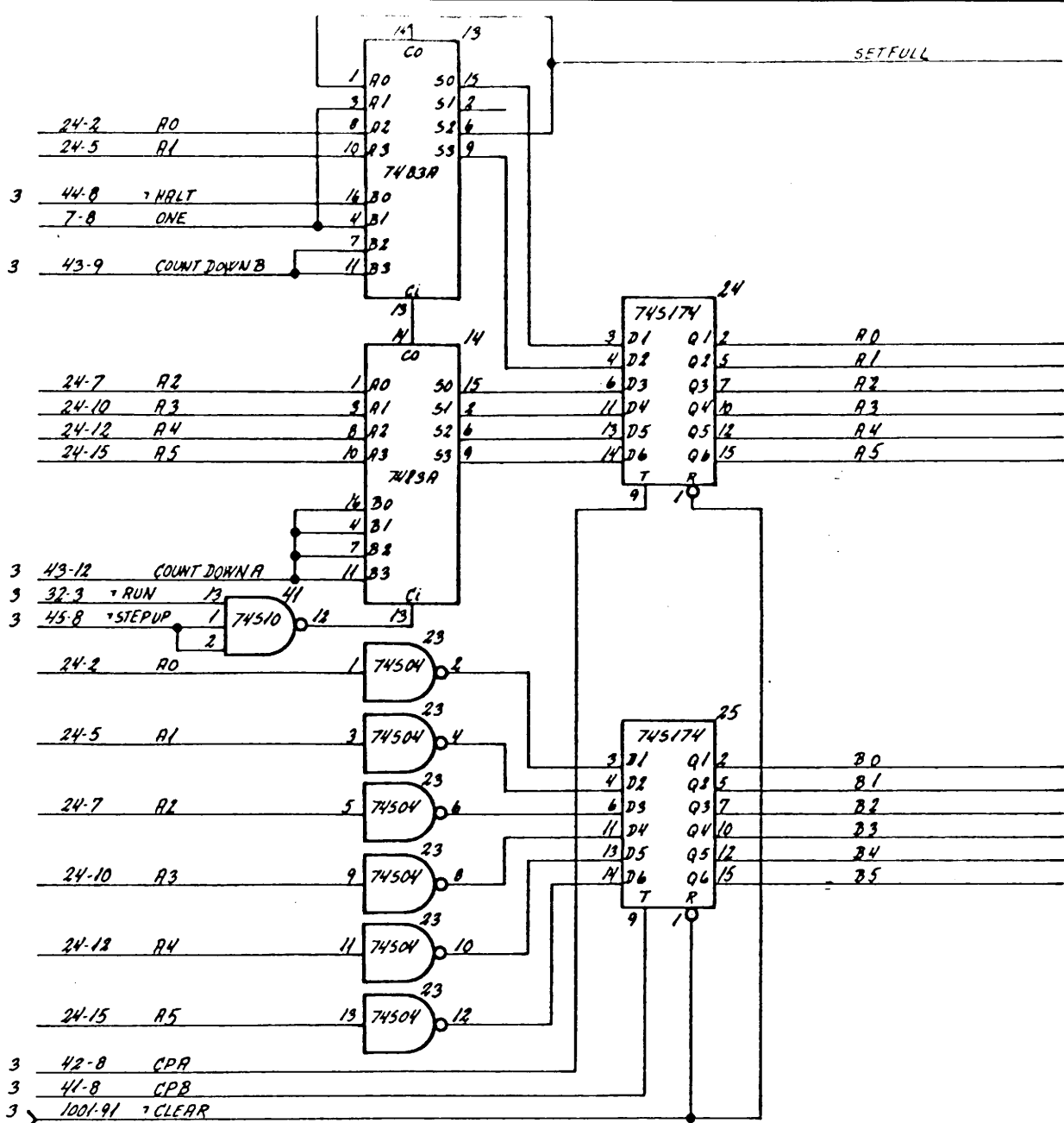
Data should be stable in the interval 2 - 15 nanosec's after the clock time.

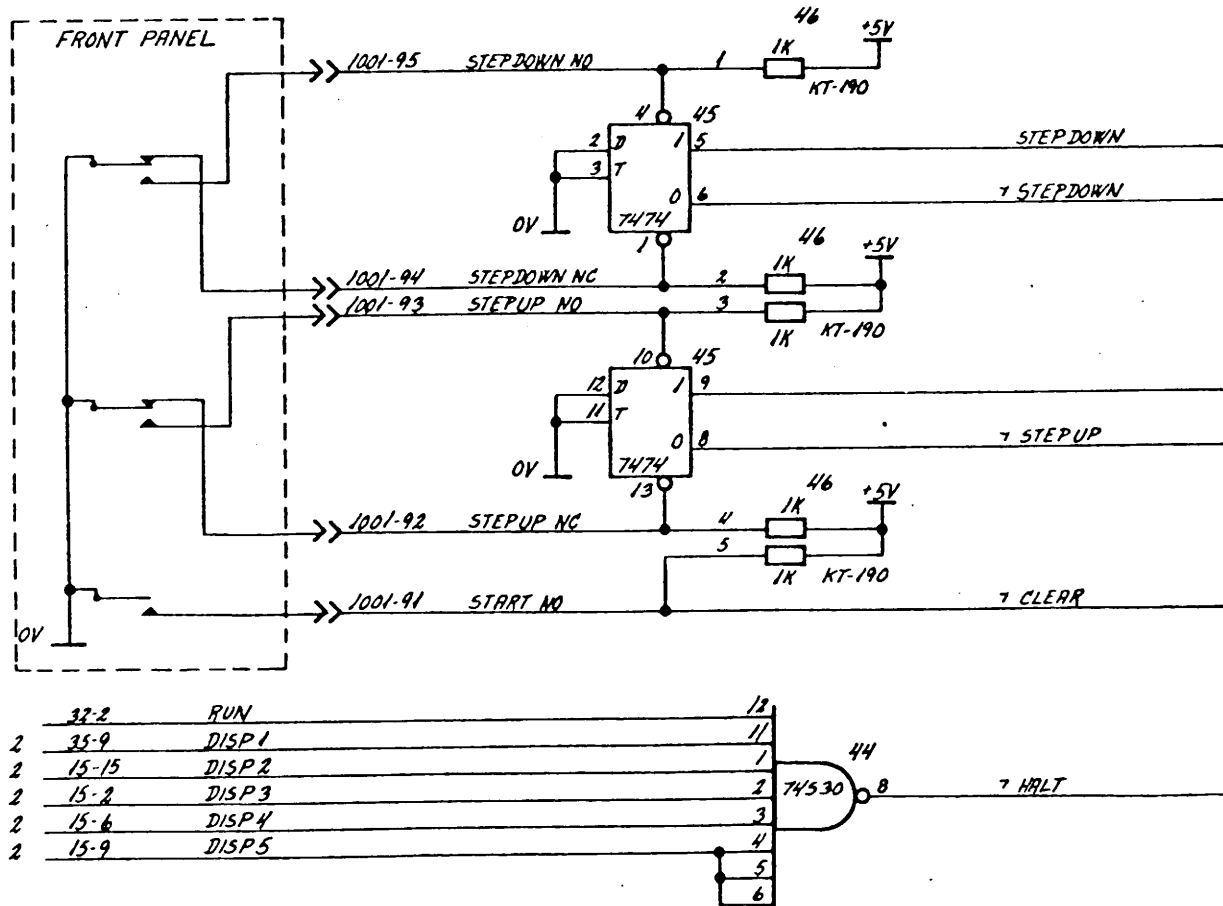
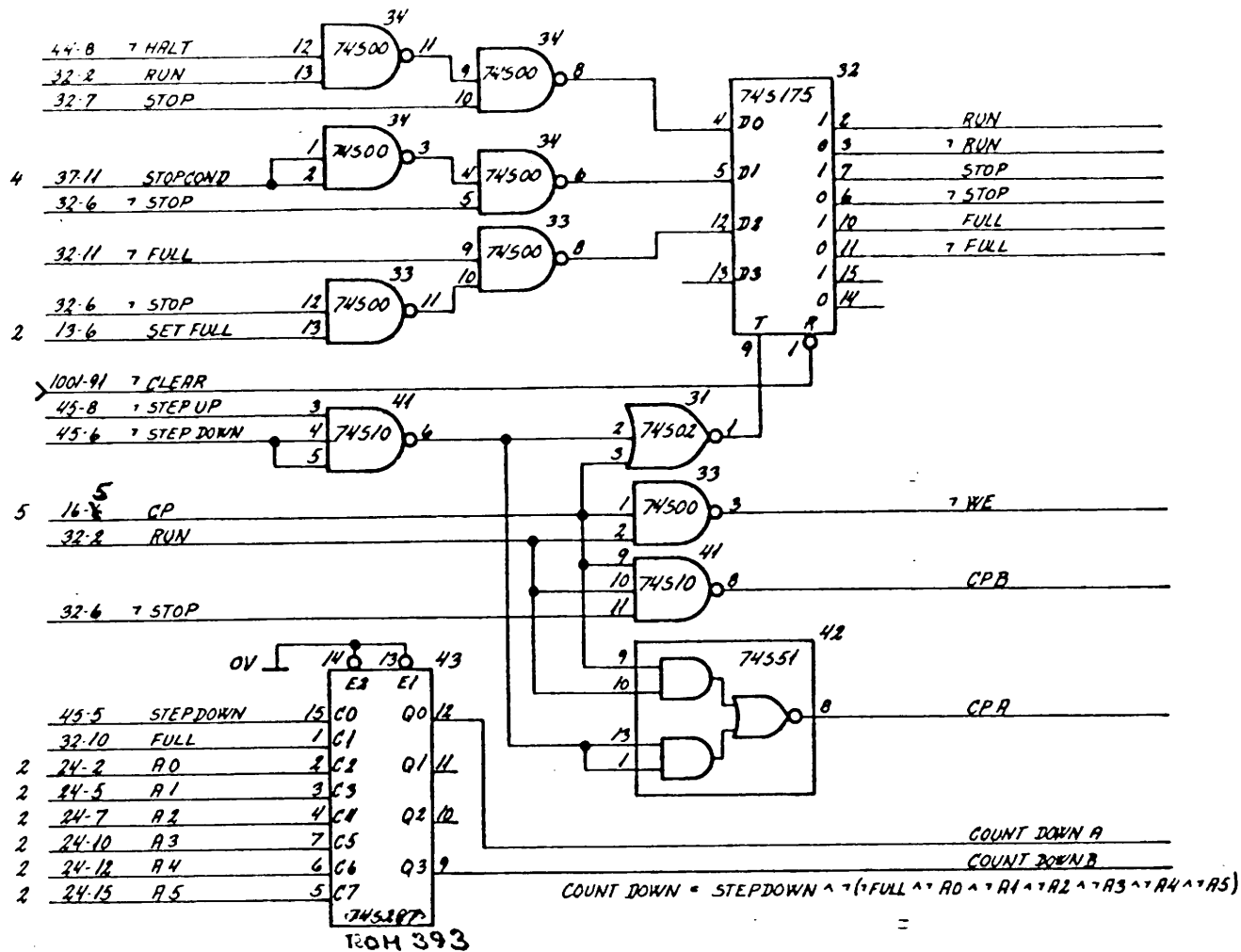
Minimum low-time for CP = 10 nSec.

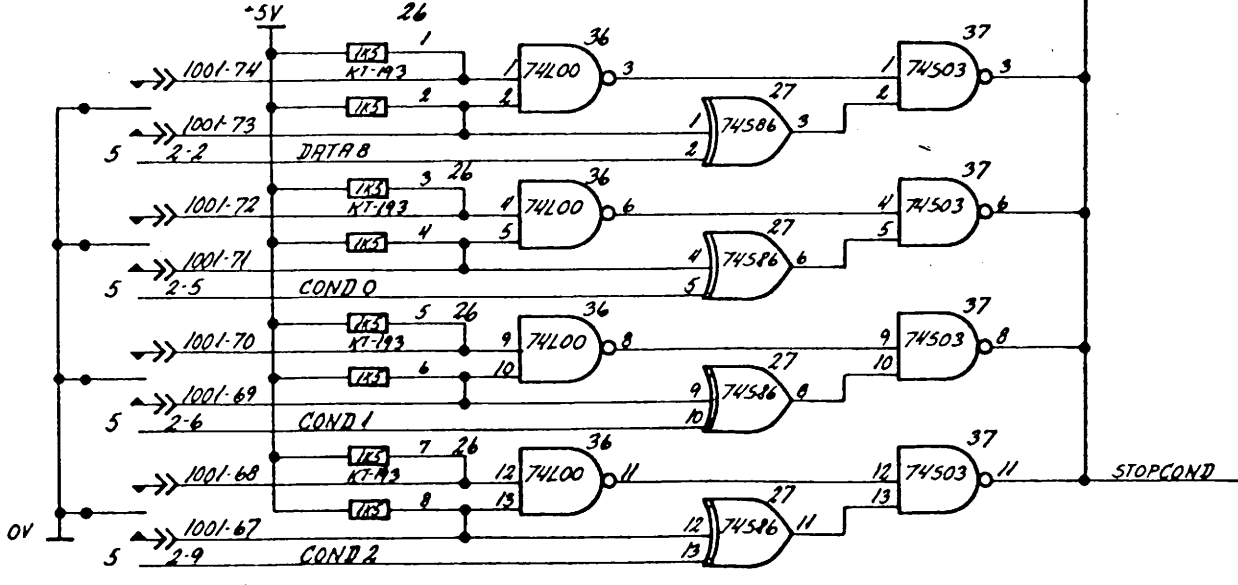
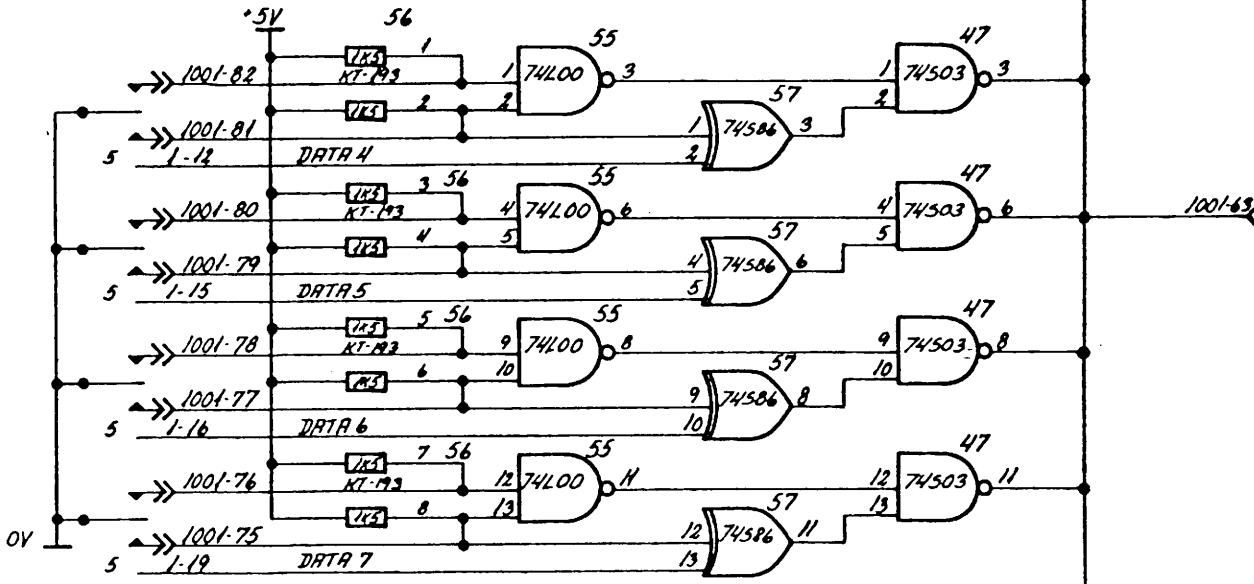
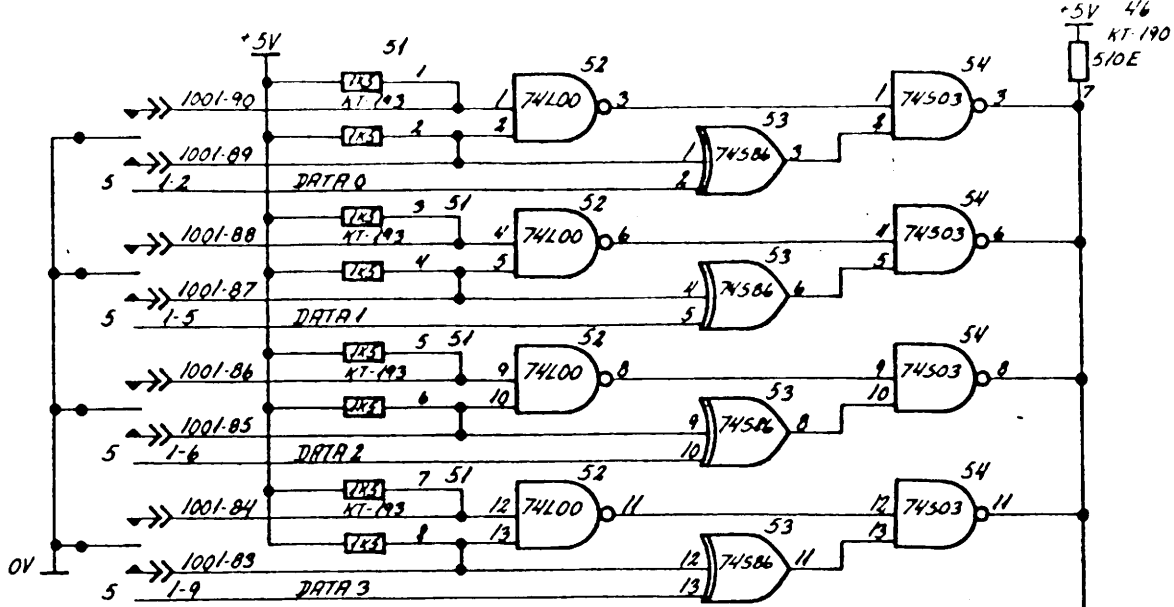
Minimum high-time for CP = 15 nSec.

Maximum recordable CP frequency = 11 MHz.

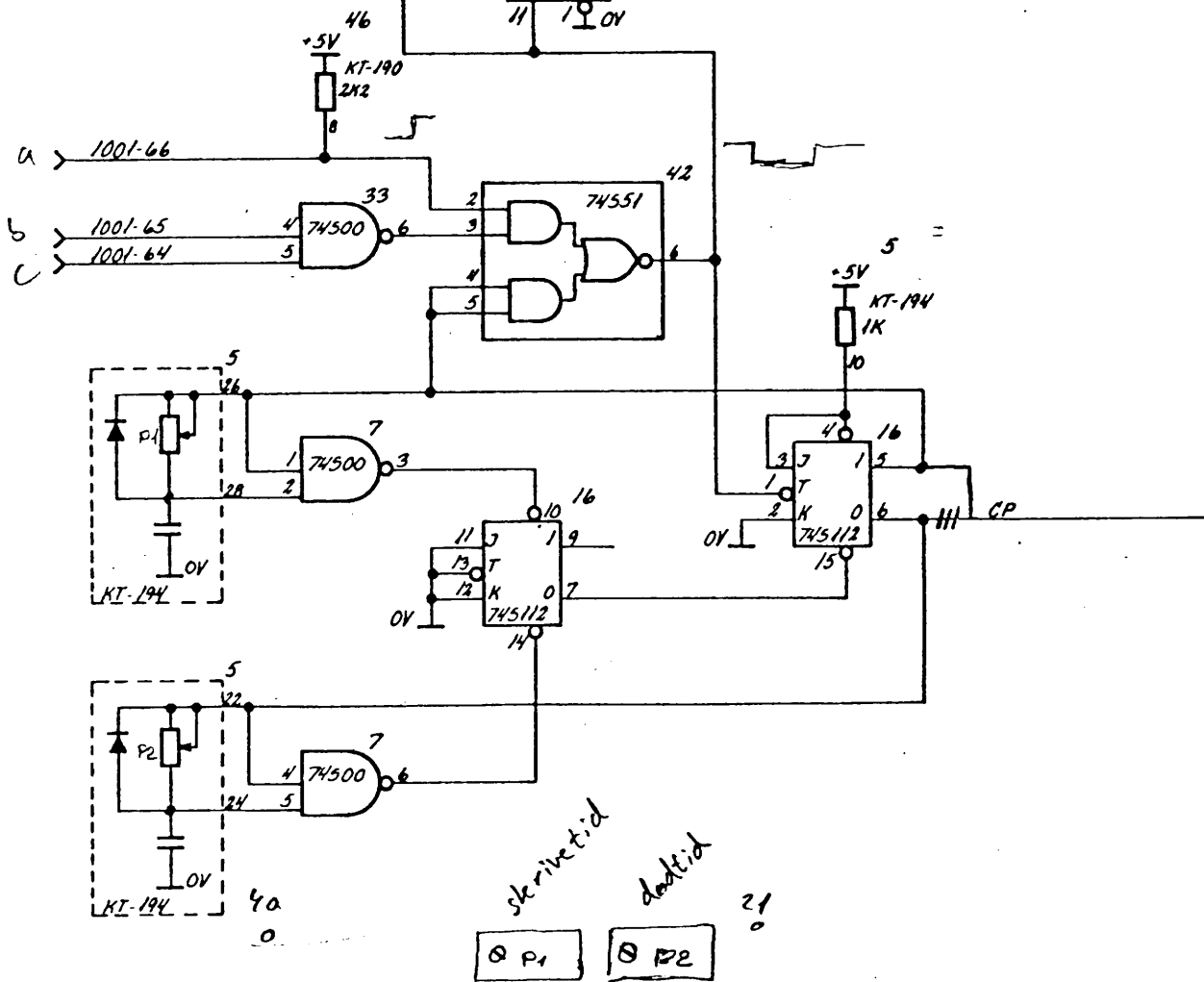
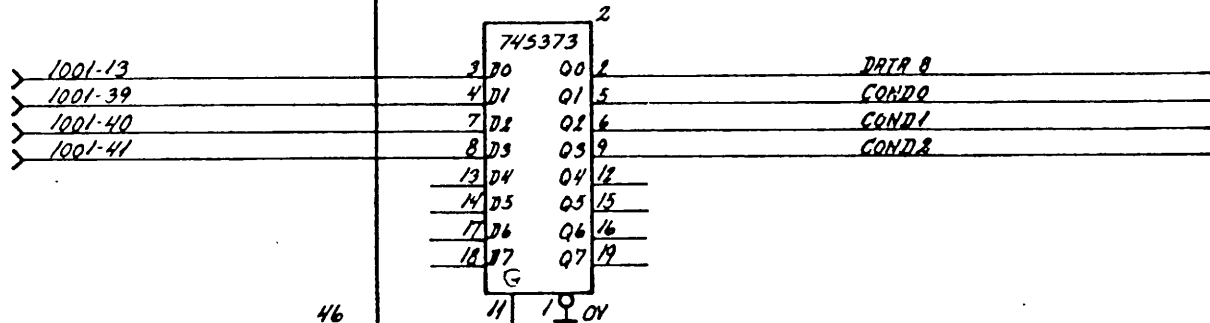
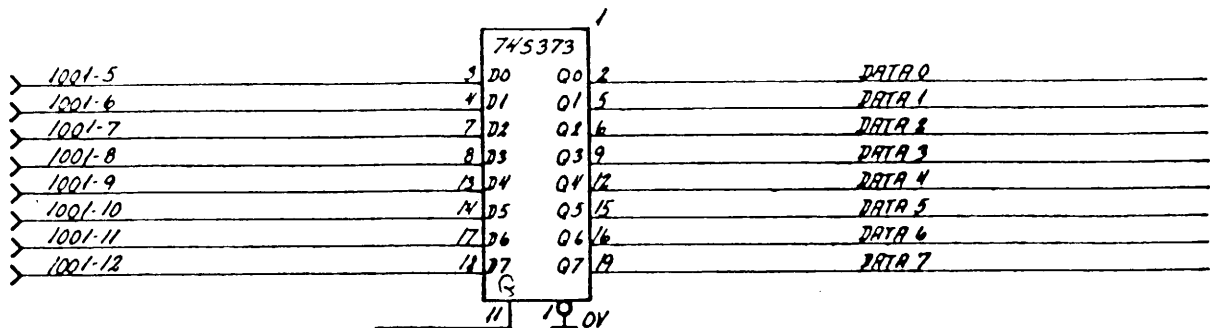






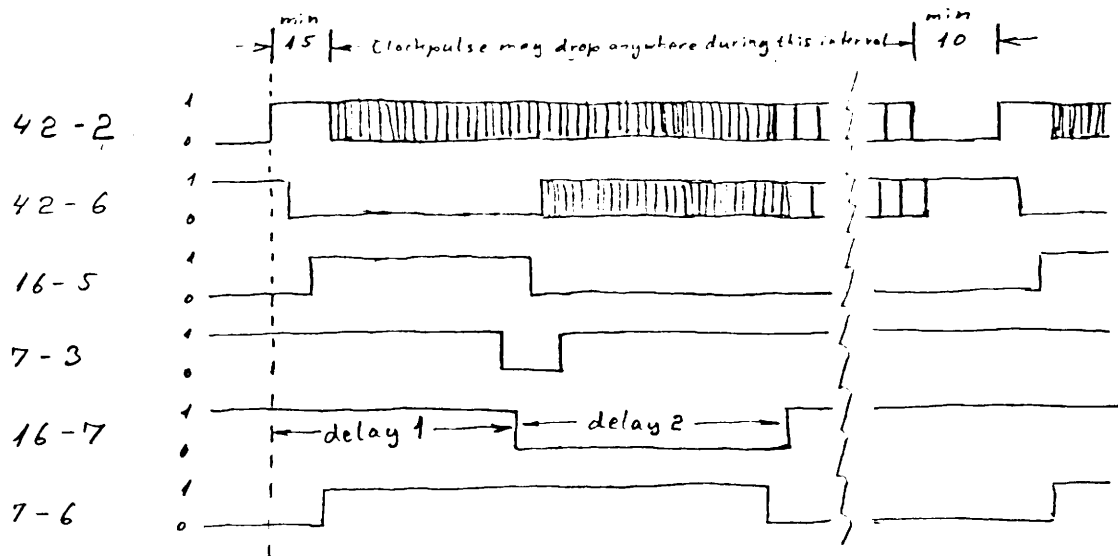


011276 PHA 030177 ROB



011276 PHA 030177 AOB

Timing diagrammet for clockshaping kredsløbet (diagram 5) er som følger:



Delay 1 er skrive tiden i RAM og beslutningstid for comparator.

Delay 2 er dødtid inden næste klokkepuls vil blive registreret.

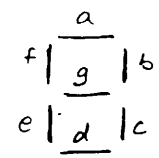
Ved hjælp af pulsgenerator på klokkeindgang og oscilloskop på pos. 42-2 og pos. 16-7 og skruetrækker

justeres Delay 1 på P1 til 60 ns og

Delay 2 på P2 til 30 ns.

Q 97654321
76543210

addr.	g f e d c b a s	Display picture
0:	1 0 0 0 0 0 0 0	0
1:	1 1 1 1 0 0 1 0	1
2:	0 1 0 0 1 0 0 0	2
3:	0 1 1 0 0 0 0 0	3
4:	0 0 1 1 0 0 1 0	4
5:	0 0 1 0 0 1 0 0	5
6	0 0 0 0 0 1 0 0	6
7	1 1 1 1 0 0 0 0	7
10	1 0 0 0 0 0 0 1	0
11	1 1 1 1 0 0 0 0	7
12	0 0 0 0 0 1 0 0	6
13	0 0 1 0 0 1 0 0	5
14	0 0 1 1 0 0 1 0	4
15	0 1 1 0 0 0 0 0	3
16	0 1 0 0 1 0 0 0	2
17	1 1 1 1 0 0 1 0	1
20	1 0 0 0 0 0 0 1	0
21	1 1 1 1 0 0 1 1	1
22	0 1 0 0 1 0 0 1	2
23	0 1 1 0 0 0 0 1	3
24	1 0 0 0 0 0 0 1	0
25	1 1 1 1 0 0 1 1	1
26	0 1 0 0 1 0 0 1	2
27	0 1 1 0 0 0 0 1	3
30	0 1 1 0 0 0 0 0	- 3
31	0 1 0 0 1 0 0 0	- 2
32	1 1 1 1 0 0 1 0	- 1
33	1 0 0 0 0 0 0 0	- 0
34	0 0 1 1 0 0 1 0	- 4
35	0 1 1 0 0 0 0 0	- 3
36	0 1 0 0 1 0 0 0	- 2
37	1 1 1 1 0 0 1 0	- 1

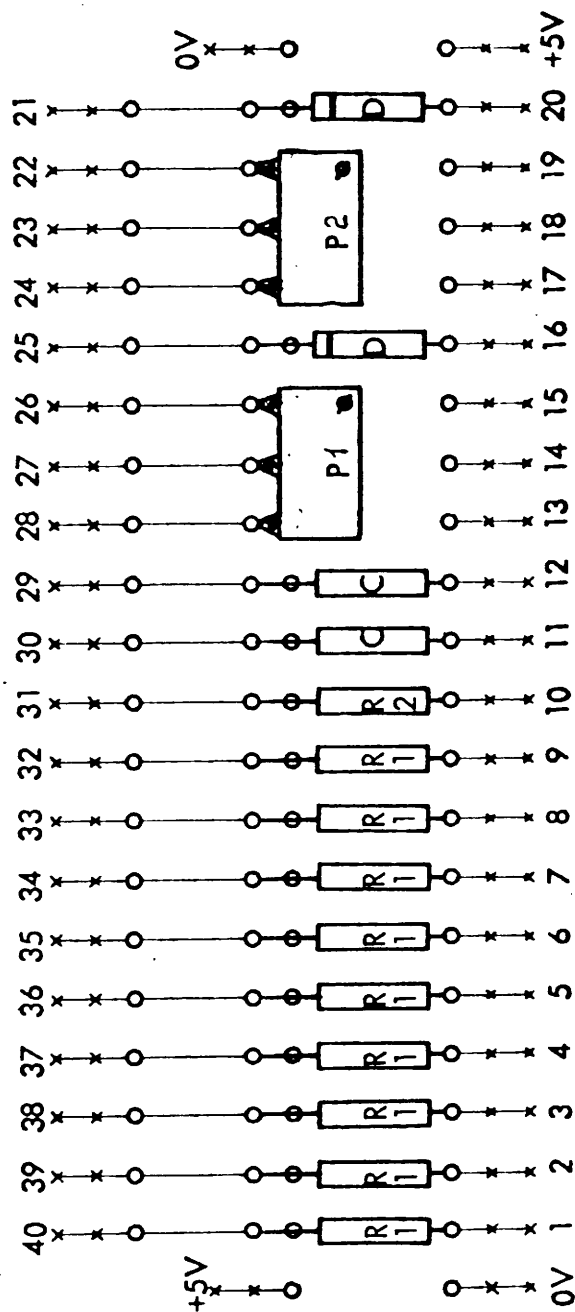


7/12-76

KREDSLØB: KT - 194 Div. Komp.

MONTAGE: SET FRA KOMPONENTSIDENINTERN TRÅDNING:

+5V	-	31
0V	-	11
11	-	12
30	-	28
27	-	26
29	-	24
23	-	22
30	-	16
27	-	25
20	-	29
23	-	21

KOMPONENTER:

P1, P2: Potentiometer 2K Bourns
 C: Kondensator 150pF
 R1: Modstand 680E 5% 1/8W
 R2: Modstand 1K 5% 1/8W
 D: Diode 1N914