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PROGRAM

NOVA 2 LOGIC TEST

TAPE

095-000141-03

ABSTRACT

THE NOVA 2 LOGIC TEST IS A MAINTENANCE PROGRAM DESIGNED TO TEST THE NOVA 2 CENTRAL PROCESSING UNIT. IT IS A GATE-BY-GATE TEST OF THE LOGIC USED TO IMPLEMENT THE NOVA 2 INSTRUCTION SET. ALSO INCLUDED IS A MINIMAL LEVEL TEST OF THE CPU I/O AND PROGRAM INTERRUPT.

```
0001 N2LOG MACRO REV 03.00              12:42:59 06/11/76
01
02
03
04
05
06
07              ;*****************************************************************
08              ;
09              ; NAME: N2LGCTST.SR                          PART NUMBER: 094-000505
10              ;
11              ;
12              ; DESCRIPTION: NOVA 2 LOGIC TEST
13              ;
14              ;
15              ; REVISION HISTORY:
16              ;
17              ;       REV.            DATE
18              ;
19              ;       00              07/19/73
20              ;       01              02/15/74
21              ;       02              06/07/74
22              ;       03              06/11/76
23              ;
24              ;
25              ; COPYRIGHT (C) DATA GENERAL CORPORATION, 1973, 1974, 1976
26              ; ALL RIGHTS RESERVED.
27              ;*****************************************************************
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0000 N2LOG
01              ;               NOVA 2 LOGIC TEST
02              ;1.     ABSTRACT
03              ;               THE NOVA 2 LOGIC TEST IS A MAINTENANCE PROGRAM
04              ;               DESIGNED TO TEST THE NOVA 2 CENTRAL PROCESSING
05              ;               UNIT.  IT IS A GATE BY GATE TEST OF THE LOGIC
06              ;               USED TO IMPLEMENT THE NOVA 2 INSTRUCTION SET.
07              ;               ALSO INCLUDED IS A MINIMUM LEVEL TEST OF THE
08              ;               CPU I/O INSTRUCTIONS,TELETYPE I/O AND PRO-
09              ;               GRAM INTERRUPT.
10              ;
11              ;2.     MACHINE REQUIREMENTS
12              ;2.1            NOVA 2 PROCESSOR
13              ;2.2            4K OF READ/WRITE MEMORY
14              ;2.3            BASIC I/O TELETYPE INTERFACE
15              ;
16              ;4.     OPERATING PROCEDURE
17              ;4.1            VERIFY THAT THE NOVA 2 WILL PERFORM ALL
18              ;               CONSOLE FUNCTIONS, I.E. EXAMINE/EXAMINE NEXT
19              ;               DEPOSIT/DEPOSIT NEXT AC'S EXAMINE/DEPOSIT
20              ;4.2            LOAD THE PROGRAM VIA THE BINARY LOADER.
21              ;4.3            SET THE SWITCHES EQUAL TO 500
22              ;4.4            PRESS START
23              ;4.5            MACHINE SHOULD HALT M/A=501, PRESS CONTINUE
24              ;4.6            PROCESSOR SHOUL CONTINUE TO RUN WITHOUT HALTING
25              ;               TELETYPE SHOULD STUTTER FOR 60 CHARACTERS
26              ;               THE TYPEOUT "PASS" SHOULD OCCUR AND THE TEST
27              ;               SHOULD CONTINUE TO LOOP WITH THE TELETYPE RUNNIN
28              ;               AT A SLOWER RATE.
29              ;
30              ;5.     ERROR DESCRIPTION
31              ;5.1            DETECTED ERRORS WILL BE MANIFESTED BY A PROCESSO
32              ;               HALT
33              ;5.2            RECORD THE STATE OF THE PROCESSOR AND REGISTERS
34              ;               AT THE TIME OF THE HALT.  CONSULT THE LISTING
35              ;               AT THE ADDRESS OF THE ERROR HALT FOR PROB-
36              ;               ABLE CAUSES OF THE FAILURE. CONSTRUCT A LOOP
37              ;               THAT WILL REPEAT THE FAILURE AND SCOPE AS REQUIR
38              ;
39              ;6.     PROGRAM DESCRIPTION
40              ;               THIS PROGRAM IS A COLLECTION OF SMALL TESTS,
41              ;               EACH TEST IN SEQUENCE BASED ON PREVIOUS TESTS
42              ;               WORKING AND DESIGNED TO TEST AS SMALL AN ADDI-
43              ;               TIONAL PIECE OF THE LOGIC AS POSSIBLE.
```

```
0003 N2LOG
01                              .TITL N2LOG
02
03          000000              .LOC    0
04 000000 027560                DIRT                    ;DTOS DIRT BLOCK POINTER
05
06          000045              .LOC    45
07 000045 000046                EGGS                    ;DTOS EGGS BLK PNTR
08 000046 000000 EGGS:  0                               ;DTOS AUTO MODE SW
09 000047 000000        0                               ;DEVICE CODE
10 000050 000000        0                               ;CAT SWITCH
11 000051 000000        0                               ;# OF PASSES THIS RUN
12 000052 000000        0                               ;DTOS RTN ADDR
13 000053 000000        0                               ;SWITCH REGISTER
14
15 000054 000001 K1: 1
16 000055 000002 K2: 2
17 000056 000004 K4: 4
18 000057 000010 K10: 10
19 000060 000020 K20: 20
20 000061 000040 K40: 40
21 000062 000100 K100: 100
22 000063 000200 K200: 200
23 000064 000400 K400: 400
24 000065 001000 K1000: 1000
25 000066 002000 K2000: 2000
26 000067 004000 K4000: 4000
27 000070 010000 K10K: 10000
28 000071 020000 K20K: 20000
29 000072 040000 K40K: 40000
30 000073 100000 K100K: 100000
31 000074 020400 KLDA,: 20400   ;= TO AN LDA 0,, OFF PAGE0
32 000075 000005 K5:    5
33 000076 000007 K7:    7
34 000077 000300 K300:  300
35 000100 000017 KD17:  #17
36 000101 177770 KM8:   -8.
37 000102 000021 KD21:  #21
38 000103 000037 KD37:  #37
39 000104 125251 KCBE:  125251  ;EVEN # BITS
40 000105 052525 KCBO:  052525  ;ODD # BITS
41 000106 000420 K420:  420
42 000107 001400 KJRET: JMP 0,3 ;JSR RETURNS TYPE JMP
43 000110 000000 K0:    0
44 000111 000074 K60:   60.
45 000112 000074 TESTK: 060.
46 000113 000215 K215:  215
47 000114 000212 K212:  212
48 000115 000323 K323:  323
49 000116 000011 KTTO:  TTO
50 000117 000320 K320:  320
51 000120 023300 JMPJK: JMP @300
52 000121 000001 PKR00: 1
53 000122 000001 PKR01: 1
54
55          002000              .LOC    200
56
57                  ;
58                  ; STANDARD START AT 200
59                  ;
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```
0004 N2LOG
01 002201 002201 DTOSR:  JMP @.+1
02 002201 027561         &1A
```

```
0025 N2LOG
                .LOC 500
000500 063077   HALT    ;TO TEST CPU HALT
                ;DEFINE SKIP TEST MACRO FOR FIRST TEST SERIES
                ;THIS SERIES WILL VERIFY THAT EACH ALC
                ;INSTRUCTION WILL NOT SKIP/THEN SKIP UNCONDITIONALLY
                        .MACRO STES1
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A1:
                        A2 0,0          ;A2 SHD NOT CAUSE SKIP IR13,14,15=000
                        A2 0,0,SKP      ;A2 SKIP ALWAYS IR13,14,15=001
                        HALT
                %
                        .MACRO STES2
                        STES1   A1A     A2
                        STES1   A1B     A27
                        STES1   A1C     A2D
                        STES1   A1D     A2C
                        STES1   A1E     A2L
                        STES1   A1F     A2R
                        STES1   A1G     A2S
                %

                        STES2   1       COM
                        STES1   1A      COM
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A1A:
000501 104000           COM 0,0         ;COM SHD NOT CAUSE SKIP IR13,14,15=000
000502 104001           COM 0,0,SKP     ;COM SKIP ALWAYS IR13,14,15=001
000503 063077           HALT
                        STES1   1B      COMZ
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A1B:
000504 104020           COMZ 0,0                ;COMZ SHD NOT CAUSE SKIP IR13,14
000505 104021           COMZ 0,0,SKP    ;COMZ SKIP ALWAYS IR13,14,15=001
000506 063077           HALT
                        STES1   1C      COMO
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A1C:
000507 104040           COMO 0,0                ;COMO SHD NOT CAUSE SKIP IR13,14
000510 104041           COMO 0,0,SKP    ;COMO SKIP ALWAYS IR13,14,15=001
000511 063077           HALT
                        STES1   1D      COMC
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A1D:
000512 104060           COMC 0,0                ;COMC SHD NOT CAUSE SKIP IR13,14
000513 104061           COMC 0,0,SKP    ;COMC SKIP ALWAYS IR13,14,15=001
000514 063077           HALT
                        STES1   1E      COML
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A1E:
000515 104100           COML 0,0                ;COML SHD NOT CAUSE SKIP IR13,14
000516 104101           COML 0,0,SKP    ;COML SKIP ALWAYS IR13,14,15=001
000517 063077           HALT
                        STES1   1F      COMR
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A1F:
000520 104200           COMR 0,0                ;COMR SHD NOT CAUSE SKIP IR13,14
000521 104201           COMR 0,0,SKP    ;COMR SKIP ALWAYS IR13,14,15=001
000522 063077           HALT
                        STES1   1G      COMS
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0026 N2LOG
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A1G:
000523 104300           COMS 0,0                ;COMS SHD NOT CAUSE SKIP IR13,14
000524 104301           COMS 0,0,SKP    ;COMS SKIP ALWAYS IR13,14,15=001
000525 063077           HALT
                        STES2   2       NEG
                        STES1   2A      NEG
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A2A:
000526 104400           NEG 0,0         ;NEG SHD NOT CAUSE SKIP IR13,14,15=000
000527 104401           NEG 0,0,SKP     ;NEG SKIP ALWAYS IR13,14,15=001
000530 063077           HALT
                        STES1   2B      NEGZ
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A2B:
000531 104420           NEGZ 0,0                ;NEGZ SHD NOT CAUSE SKIP IR13,14
000532 104421           NEGZ 0,0,SKP    ;NEGZ SKIP ALWAYS IR13,14,15=001
000533 063077           HALT
                        STES1   2C      NEGO
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A2C:
000534 104440           NEGO 0,0                ;NEGO SHD NOT CAUSE SKIP IR13,14
000535 104441           NEGO 0,0,SKP    ;NEGO SKIP ALWAYS IR13,14,15=001
000536 063077           HALT
                        STES1   2D      NEGC
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A2D:
000537 104460           NEGC 0,0                ;NEGC SHD NOT CAUSE SKIP IR13,14
000540 104461           NEGC 0,0,SKP    ;NEGC SKIP ALWAYS IR13,14,15=001
000541 063077           HALT
                        STES1   2E      NEGL
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A2E:
000542 104500           NEGL 0,0                ;NEGL SHD NOT CAUSE SKIP IR13,14
000543 104501           NEGL 0,0,SKP    ;NEGL SKIP ALWAYS IR13,14,15=001
000544 063077           HALT
                        STES1   2F      NEGR
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A2F:
000545 104600           NEGR 0,0                ;NEGR SHD NOT CAUSE SKIP IR13,14
000546 104601           NEGR 0,0,SKP    ;NEGR SKIP ALWAYS IR13,14,15=001
000547 063077           HALT
                        STES1   2G      NEGS
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A2G:
000550 104700           NEGS 0,0                ;NEGS SHD NOT CAUSE SKIP IR13,14
000551 104701           NEGS 0,0,SKP    ;NEGS SKIP ALWAYS IR13,14,15=001
000552 063077           HALT
                        STES2   3       MOV
                        STES1   3A      MOV
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A3A:
000553 105000           MOV 0,0         ;MOV SHD NOT CAUSE SKIP IR13,14,15=000
000554 105001           MOV 0,0,SKP     ;MOV SKIP ALWAYS IR13,14,15=001
000555 063077           HALT
                        STES1   3B      MOVZ
                ;ERR HALT INDICATES EXTRANEOUS SKIP
                A3B:
000556 105020           MOVZ 0,0                ;MOVZ SHD NOT CAUSE SKIP IR13,14
000557 105021           MOVZ 0,0,SKP    ;MOVZ SKIP ALWAYS IR13,14,15=001
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0007 N2LOG
01 00560 063077          HALT
02                       STES1   3C      MOVO
03                  ;ERR HALT INDICATES EXTRANEOUS SKIP
04                  A3C:
05 00561 101040          MOVO 0,0                ;MOVO SHD NOT CAUSE SKIP IR13,14
06 00562 101041          MOVO 0,0,SKP    ;MOVO SKIP ALWAYS IR13,14,15=001
07 00563 063077          HALT
08                       STES1   3D      MOVC
09                  ;ERR HALT INDICATES EXTRANEOUS SKIP
10                  A3D:
11 00564 101060          MOVC 0,0                ;MOVC SHD NOT CAUSE SKIP IR13,14
12 00565 101061          MOVC 0,0,SKP    ;MOVC SKIP ALWAYS IR13,14,15=001
13 00566 063077          HALT
14                       STES1   3E      MOVL
15                  ;ERR HALT INDICATES EXTRANEOUS SKIP
16                  A3E:
17 00567 101100          MOVL 0,0                ;MOVL SHD NOT CAUSE SKIP IR13,14
18 00570 101101          MOVL 0,0,SKP    ;MOVL SKIP ALWAYS IR13,14,15=001
19 00571 063077          HALT
20                       STES1   3F      MOVR
21                  ;ERR HALT INDICATES EXTRANEOUS SKIP
22                  A3F:
23 00572 101200          MOVR 0,0                ;MOVR SHD NOT CAUSE SKIP IR13,14
24 00573 101201          MOVR 0,0,SKP    ;MOVR SKIP ALWAYS IR13,14,15=001
25 00574 063077          HALT
26                       STES1   3G      MOVS
27                  ;ERR HALT INDICATES EXTRANEOUS SKIP
28                  A3G:
29 00575 101300          MOVS 0,0                ;MOVS SHD NOT CAUSE SKIP IR13,14
30 00576 101301          MOVS 0,0,SKP    ;MOVS SKIP ALWAYS IR13,14,15=001
31 00577 063077          HALT
32                       STES2   4       INC
33                       STES1   4A      INC
34                  ;ERR HALT INDICATES EXTRANEOUS SKIP
35                  A4A:
36 00600 101400          INC 0,0                 ;INC SHD NOT CAUSE SKIP IR13,14,15=000
37 00601 101401          INC 0,0,SKP     ;INC SKIP ALWAYS IR13,14,15=001
38 00602 063077          HALT
39                       STES1   4B      INCZ
40                  ;ERR HALT INDICATES EXTRANEOUS SKIP
41                  A4B:
42 00603 101420          INCZ 0,0                ;INCZ SHD NOT CAUSE SKIP IR13,14
43 00604 101421          INCZ 0,0,SKP    ;INCZ SKIP ALWAYS IR13,14,15=001
44 00605 063077          HALT
45                       STES1   4C      INCO
46                  ;ERR HALT INDICATES EXTRANEOUS SKIP
47                  A4C:
48 00606 101440          INCO 0,0                ;INCO SHD NOT CAUSE SKIP IR13,14
49 00607 101441          INCO 0,0,SKP    ;INCO SKIP ALWAYS IR13,14,15=001
50 00610 063077          HALT
51                       STES1   4D      INCC
52                  ;ERR HALT INDICATES EXTRANEOUS SKIP
53                  A4D:
54 00611 101460          INCC 0,0                ;INCC SHD NOT CAUSE SKIP IR13,14
55 00612 101461          INCC 0,0,SKP    ;INCC SKIP ALWAYS IR13,14,15=001
56 00613 063077          HALT
57                       STES1   4E      INCL
58                  ;ERR HALT INDICATES EXTRANEOUS SKIP
59                  A4E:
60 00614 101500          INCL 0,0                ;INCL SHD NOT CAUSE SKIP IR13,14
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0008 N2LOG
01 00615 101501          INCL 0,0,SKP    ;INCL SKIP ALWAYS IR13,14,15=001
02 00616 063077          HALT
03                       STES1   4F      INCM
04                  ;ERR HALT INDICATES EXTRANEOUS SKIP
05                  A4F:
06 00617 101600          INCM 0,0                ;INCM SHD NOT CAUSE SKIP IR13,14
07 00620 101601          INCM 0,0,SKP    ;INCM SKIP ALWAYS IR13,14,15=001
08 00621 063077          HALT
09                       STES1   4G      INCS
10                  ;ERR HALT INDICATES EXTRANEOUS SKIP
11                  A4G:
12 00622 101700          INCS 0,0                ;INCS SHD NOT CAUSE SKIP IR13,14
13 00623 101701          INCS 0,0,SKP    ;INCS SKIP ALWAYS IR13,14,15=001
14 00624 063077          HALT
15                       STES2   5       ADC
16                       STES1   5A      ADC
17                  ;ERR HALT INDICATES EXTRANEOUS SKIP
18                  A5A:
19 00625 102000          ADC 0,0                 ;ADC SHD NOT CAUSE SKIP IR13,14,15=000
20 00626 102001          ADC 0,0,SKP     ;ADC SKIP ALWAYS IR13,14,15=001
21 00627 063077          HALT
22                       STES1   5B      ADCZ
23                  ;ERR HALT INDICATES EXTRANEOUS SKIP
24                  A5B:
25 00630 102020          ADCZ 0,0                ;ADCZ SHD NOT CAUSE SKIP IR13,14
26 00631 102021          ADCZ 0,0,SKP    ;ADCZ SKIP ALWAYS IR13,14,15=001
27 00632 063077          HALT
28                       STES1   5C      ADCO
29                  ;ERR HALT INDICATES EXTRANEOUS SKIP
30                  A5C:
31 00633 102040          ADCO 0,0                ;ADCO SHD NOT CAUSE SKIP IR13,14
32 00634 102041          ADCO 0,0,SKP    ;ADCO SKIP ALWAYS IR13,14,15=001
33 00635 063077          HALT
34                       STES1   5D      ADCC
35                  ;ERR HALT INDICATES EXTRANEOUS SKIP
36                  A5D:
37 00636 102060          ADCC 0,0                ;ADCC SHD NOT CAUSE SKIP IR13,14
38 00637 102061          ADCC 0,0,SKP    ;ADCC SKIP ALWAYS IR13,14,15=001
39 00640 063077          HALT
40                       STES1   5E      ADCL
41                  ;ERR HALT INDICATES EXTRANEOUS SKIP
42                  A5E:
43 00641 102100          ADCL 0,0                ;ADCL SHD NOT CAUSE SKIP IR13,14
44 00642 102101          ADCL 0,0,SKP    ;ADCL SKIP ALWAYS IR13,14,15=001
45 00643 063077          HALT
46                       STES1   5F      ADCR
47                  ;ERR HALT INDICATES EXTRANEOUS SKIP
48                  A5F:
49 00644 102200          ADCR 0,0                ;ADCR SHD NOT CAUSE SKIP IR13,14
50 00645 102201          ADCR 0,0,SKP    ;ADCR SKIP ALWAYS IR13,14,15=001
51 00646 063077          HALT
52                       STES1   5G      ADCS
53                  ;ERR HALT INDICATES EXTRANEOUS SKIP
54                  A5G:
55 00647 102300          ADCS 0,0                ;ADCS SHD NOT CAUSE SKIP IR13,14
56 00650 102301          ADCS 0,0,SKP    ;ADCS SKIP ALWAYS IR13,14,15=001
57 00651 063077          HALT
58                       STES2   6       SUB
59                       STES1   6A      SUB
60                  ;ERR HALT INDICATES EXTRANEOUS SKIP
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0009 N2LOG
01                      A6A:
02 00652 102400                 SUB 0,0                 ;SUB SHD NOT CAUSE SKIP IR13,14,15=000
03 00653 102401                 SUB 0,0,SKP             ;SUB SKIP ALWAYS IR13,14,15=001
04 00654 063077                 HALT
05                              STES1   6B      SUBZ
06                      ;ERR HALT INDICATES EXTRANEOUS SKIP
07                      A6B:
08 00655 102420                 SUBZ 0,0                ;SUBZ SHD NOT CAUSE SKIP IR13,14
09 00656 102421                 SUBZ 0,0,SKP            ;SUBZ SKIP ALWAYS IR13,14,15=001
10 00657 063077                 HALT
11                              STES1   6C      SUBO
12                      ;ERR HALT INDICATES EXTRANEOUS SKIP
13                      A6C:
14 00660 102440                 SUBO 0,0                ;SUBO SHD NOT CAUSE SKIP IR13,14
15 00661 102441                 SUBO 0,0,SKP            ;SUBO SKIP ALWAYS IR13,14,15=001
16 00662 063077                 HALT
17                              STES1   6D      SUBC
18                      ;ERR HALT INDICATES EXTRANEOUS SKIP
19                      A6D:
20 00663 102460                 SUBC 0,0                ;SUBC SHD NOT CAUSE SKIP IR13,14
21 00664 102461                 SUBC 0,0,SKP            ;SUBC SKIP ALWAYS IR13,14,15=001
22 00665 063077                 HALT
23                              STES1   6E      SUBL
24                      ;ERR HALT INDICATES EXTRANEOUS SKIP
25                      A6E:
26 00666 102500                 SUBL 0,0                ;SUBL SHD NOT CAUSE SKIP IR13,14
27 00667 102501                 SUBL 0,0,SKP            ;SUBL SKIP ALWAYS IR13,14,15=001
28 00670 063077                 HALT
29                              STES1   6F      SUBR
30                      ;ERR HALT INDICATES EXTRANEOUS SKIP
31                      A6F:
32 00671 102600                 SUBR 0,0                ;SUBR SHD NOT CAUSE SKIP IR13,14
33 00672 102601                 SUBR 0,0,SKP            ;SUBR SKIP ALWAYS IR13,14,15=001
34 00673 063077                 HALT
35                              STES1   6G      SUBS
36                      ;ERR HALT INDICATES EXTRANEOUS SKIP
37                      A6G:
38 00674 102700                 SUBS 0,0                ;SUBS SHD NOT CAUSE SKIP IR13,14
39 00675 102701                 SUBS 0,0,SKP            ;SUBS SKIP ALWAYS IR13,14,15=001
40 00676 063077                 HALT
41                              STES2   7       ADD
42                              STES1   7A      ADD
43                      ;ERR HALT INDICATES EXTRANEOUS SKIP
44                      A7A:
45 00677 103000                 ADD 0,0                 ;ADD SHD NOT CAUSE SKIP IR13,14,15=000
46 00700 103001                 ADD 0,0,SKP             ;ADD SKIP ALWAYS IR13,14,15=001
47 00701 063077                 HALT
48                              STES1   7B      ADDZ
49                      ;ERR HALT INDICATES EXTRANEOUS SKIP
50                      A7B:
51 00702 103020                 ADDZ 0,0                ;ADDZ SHD NOT CAUSE SKIP IR13,14
52 00703 103021                 ADDZ 0,0,SKP            ;ADDZ SKIP ALWAYS IR13,14,15=001
53 00704 063077                 HALT
54                              STES1   7C      ADDO
55                      ;ERR HALT INDICATES EXTRANEOUS SKIP
56                      A7C:
57 00705 103040                 ADDO 0,0                ;ADDO SHD NOT CAUSE SKIP IR13,14
58 00706 103041                 ADDO 0,0,SKP            ;ADDO SKIP ALWAYS IR13,14,15=001
59 00707 063077                 HALT
60                              STES1   7D      ADDC
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0010 N2LOG
01                      ;ERR HALT INDICATES EXTRANEOUS SKIP
02                      A7D:
03 00710 103060                 ADDC 0,0                ;ADDC SHD NOT CAUSE SKIP IR13,14
04 00711 103061                 ADDC 0,0,SKP            ;ADDC SKIP ALWAYS IR13,14,15=001
05 00712 063077                 HALT
06                              STES1   7E      ADDL
07                      ;ERR HALT INDICATES EXTRANEOUS SKIP
08                      A7E:
09 00713 103100                 ADDL 0,0                ;ADDL SHD NOT CAUSE SKIP IR13,14
10 00714 103101                 ADDL 0,0,SKP            ;ADDL SKIP ALWAYS IR13,14,15=001
11 00715 063077                 HALT
12                              STES1   7F      ADDR
13                      ;ERR HALT INDICATES EXTRANEOUS SKIP
14                      A7F:
15 00716 103200                 ADDR 0,0                ;ADDR SHD NOT CAUSE SKIP IR13,14
16 00717 103201                 ADDR 0,0,SKP            ;ADDR SKIP ALWAYS IR13,14,15=001
17 00720 063077                 HALT
18                              STES1   7G      ADDS
19                      ;ERR HALT INDICATES EXTRANEOUS SKIP
20                      A7G:
21 00721 103300                 ADDS 0,0                ;ADDS SHD NOT CAUSE SKIP IR13,14
22 00722 103301                 ADDS 0,0,SKP            ;ADDS SKIP ALWAYS IR13,14,15=001
23 00723 063077                 HALT
24                              STES2   8       AND
25                              STES1   8A      AND
26                      ;ERR HALT INDICATES EXTRANEOUS SKIP
27                      A8A:
28 00724 103400                 AND 0,0                 ;AND SHD NOT CAUSE SKIP IR13,14,15=000
29 00725 103401                 AND 0,0,SKP             ;AND SKIP ALWAYS IR13,14,15=001
30 00726 063077                 HALT
31                              STES1   8B      ANDZ
32                      ;ERR HALT INDICATES EXTRANEOUS SKIP
33                      A8B:
34 00727 103420                 ANDZ 0,0                ;ANDZ SHD NOT CAUSE SKIP IR13,14
35 00730 103421                 ANDZ 0,0,SKP            ;ANDZ SKIP ALWAYS IR13,14,15=001
36 00731 063077                 HALT
37                              STES1   8C      ANDO
38                      ;ERR HALT INDICATES EXTRANEOUS SKIP
39                      A8C:
40 00732 103440                 ANDO 0,0                ;ANDO SHD NOT CAUSE SKIP IR13,14
41 00733 103441                 ANDO 0,0,SKP            ;ANDO SKIP ALWAYS IR13,14,15=001
42 00734 063077                 HALT
43                              STES1   8D      ANDC
44                      ;ERR HALT INDICATES EXTRANEOUS SKIP
45                      A8D:
46 00735 103460                 ANDC 0,0                ;ANDC SHD NOT CAUSE SKIP IR13,14
47 00736 103461                 ANDC 0,0,SKP            ;ANDC SKIP ALWAYS IR13,14,15=001
48 00737 063077                 HALT
49                              STES1   8E      ANDL
50                      ;ERR HALT INDICATES EXTRANEOUS SKIP
51                      A8E:
52 00740 103500                 ANDL 0,0                ;ANDL SHD NOT CAUSE SKIP IR13,14
53 00741 103501                 ANDL 0,0,SKP            ;ANDL SKIP ALWAYS IR13,14,15=001
54 00742 063077                 HALT
55                              STES1   8F      ANDR
56                      ;ERR HALT INDICATES EXTRANEOUS SKIP
57                      A8F:
58 00743 103600                 ANDR 0,0                ;ANDR SHD NOT CAUSE SKIP IR13,14
59 00744 103601                 ANDR 0,0,SKP            ;ANDR SKIP ALWAYS IR13,14,15=001
60 00745 063077                 HALT
```

```
 0011 N2LOG
01                      STES1   8G      ANDS
02                  ;ERR HALT INDICATES EXTRANEOUS SKIP
03                  A8G:
04 00746 103700             ANDS 0,0                ;ANDS SHD NOT CAUSE SKIP IR13,14
05 00747 103701             ANDS 0,0,SKP    ;ANDS SKIP ALWAYS IR13,14,15=001
06 00750 063077             HALT
```

```
 0012 N2LOG
01
02
03                  ;TEST CARRY (CRY FLOP) AND SKIP LOGIC
04
05 00751 102422 A9A:        ADCZ 0,0,SZC    ;ZC,IR14,NOT IR15
06 00752 063077             HALT            ;ZERO INPUT TO CARRY FAILED
07
08 00753 102023             ADCZ 0,0,SNC    ;SNC NOT SEE CALC,IR15
09 00754 102002             ADC 0,0,SZC     ;ALSO TEST ZERO HOLD OF CRY
10 00755 063077             HALT            ;IF CRY=1 SEE NOT IR12 OR
11                  ;ABOVE FAILURE IF CRY=1 MIGHT BE IN "NOT SCI" NOT IR10
12 00756 102426 A9B:        ADCZ 0,0,SEZ    ;CARRY=0 ZC,IR14,NOT IR15
13 00757 063077             HALT            ;INVOLVES SAME GATES AS SZC (?)
14
15 00760 102043             ADCO 0,0,SNC    ;TEST FOR TRUE CALC=IR15
16 00761 063077             HALT            ;1'S INPUT TO CRY CALC WAS NOT 1
17
18 00762 102042             ADCO 0,0,SZC    ;TEST FOR CALC,IR15 FALSE
19 00763 102003             ADC 0,0,SNC     ;ALSO TEST ONES HOLD OF CRY
20 00764 063077             HALT            ;IF CRY=0 SEE NOT IR12
21                  ;ABOVE FAILURE IF CRY=0 MIGHT BE IN "NOT SCI" IR11
22
23 00765 102046 A9C:        ADCO 0,0,SEZ    ;AGAIN TEST NOT ZC,IR14,NOT IR15
24 00766 102003             ADC 0,0,SNC     ;SAME GATES AS LAST TEST (SZC)
25 00767 063077             HALT            ;EXCEPT FOR ZR,IR13
26
27                  ;CARRY SHOULD=1 COMING INTO NEXT TEST CHECK
28                  ;OF TRANSITION TO 0 ON ZC
29 00770 102022 A9D:        ADCZ 0,0,SZC    ;SKIP ON ZC,IR14,NOT IR15
30 00771 063077             HALT            ;SEE CRY,IR11 THROUGH NOT SCI
31
32 00772 102040             ADCO 0,0        ;SET CRY=1
33 00773 102023             ADCZ 0,0,SNC    ;TRANSITION CRY TO 0
34 00774 102002             ADC 0,0,SZC     ;CHECK 0 REALLY GOT THERE
35 00775 063077             HALT            ;CRY=0 IS SNC FAILED
36                  ;CRY=1 SEE CRY,IR11 IN "NOT SCI" GATES OR ZC,LOAD CARRY
37
38                  ;CARRY=0 COMING INTO NEXT TEST CHECK NOT CRY,NOT IR10
39 00776 102023 A9E:        ADCZ 0,0,SNC    ;ALSO NOT (CRY,IR11)
40 00777 102002             ADC 0,0,SZC     ;CRY SHD HAVE STAYED 0
41 01000 063077             HALT            ;ALSO ZC AND LOAD CARRY USED
```

```
;0013 N2LOG
01
02
03                      ;TEST CARRY TO TRANSITION FROM 0 TO 1
04 01001 102020 A9F:    ADCZ 0,0,       ;SET CRY=1
05 01002 102042         ADCO 0,0,SZC    ;MAKE IT=1 AGAIN NOT CRY,IR10
06 01003 102003         ADC 0,0,SNC     ;DID 1 REALLY GET TO CRY
07 01004 063077         HALT            ;IF CRY=1 SZC FAILED
08                      ;IF CRY=0 SEE CALC,NOT IR12
09
10                      ;TEST COMPLIMENT OF CARRY IR11,IR10
11 01005 102020 A9G:    ADCZ 0,0        ;SET CRY=0
12 01006 102062         ADCC 0,0,SZC    ;TRANS CRY 0 TO 1 (SZC NOT)
13 01007 102003         ADC 0,0,SNC     ;CRY SHD=1
14 01010 063077         HALT            ;CRY=0 SEE CALC,LOAD CARRY
15                      ;CARRY=0 SEE NOT SCI
16
17 01011 102040 A9H:    ADCO 0,0        ;SET CRY=1
18 01012 102063         ADCC 0,0,SNC    ;ZC SHD BE TRUE (NOT SNC)
19 01013 102002         ADC 0,0,SZC     ;CARRY SHD REALLY=0
20 01014 063077         HALT            ;CRY=1 SEE ZC AND LOAD CARRY
21
22                      ;TEST CARRY NO LOAD IR12=1 TO PREVENT CARRY CHANGE
23
24 01015 102020 A9I:    ADCZ 0,0
25 01016 102052         ADCO# 0,0,SZC   ;NO LOAD CRY IR12=1
26 01017 102002         ADC 0,0,SZC
27 01020 063077         HALT            ;CALC,IR12
28
29 01021 102040 A9J:    ADCO 0,0
30 01022 102033         ADCZ# 0,0,SNC   ;CRY SHD STAY=1 IR12=1
31 01023 102003         ADC 0,0,SNC
32 01024 063077         HALT            ;ZC,NOT LOAD CARRY
```

```
;0014 N2LOG
01
02
03                      ;TEST FOR ADC TO SET AC0=MOSTLY 1'S AND SNR TO SKIP
04                      ;START BUILDING INSTRUCTIONS TO CREATE CONSTANTS
05                      ;VERY LITTLE LOGIC IS VERIFIED YET
06 01025 102005 A20:    ADC 0,0,SNR     ;ANY RESULT IN AC0 SHD CAUSE SKP
07 01026 063077         HALT            ;AC0 ANYTHING BUT 0 IS SNR FAILED
08                  ;AC0 NOT=0 SEE IR15 IN SKIP CONTROL AND ZR AND GATES
09                  ;AC0=0 ADC MAY=SUB SEE ALU ROM NOT IR7 INPUT
10
11                  ;SZR SHOULD NOT SKIP WHEN AC0 NOT=0
12 01027 102004 A21:    ADC 0,0,SZR     ;TEST A2 INDICATES AC0 NOT=0
13 01030 102005         ADC 0,0,SNR     ;AS RESULT OF AN ADC
14 01031 063077         HALT            ;SZR SKIPPED IF AC0 NOT=0
15
16                  ;ATTEMPT TO GENERATE AN ALL 0'S CONSTANT VIA ADC+COM
17                  ;ALSO TESTS SZR TO SKIP IN GROSS CASE
18 01032 102000 A22:    ADC 0,0         ;ADC MAY NOT YET=-1
19 01033 100004         COM 0,0,SZR     ;OR COM MAY ALSO FAIL
20                  ; RESULT DOES NOT=0
21 01034 063077         HALT            ;RESULT IN AC0 SHOULD HELP TO
22                  ;ISOLATE PROBLEM TO A BIT OR CARRY GATE THROUGH THE ALU
23                  ;AC0=0 IS SZR FAILED TO SKIP IR15=0 IN SKIP LOGIC
24                  ;IF COM 0,0,=-1 THEN COM MAY=MOV OR ADC IR5+IR6
25
26                  ;TEST ZERO CARRY SKIP FROM COM 0,0
27 01035 102020 A23:    ADCZ 0,0        ;0 TO CARRY=1 TO AC0
28 01036 100002         COM 0,0,SZC     ;CARRY SHD STILL=0
29 01037 063077         HALT
30
31                  ;TEST SKIP EITHER ZERO WITH BOTH AC AND CARRY=0
32
33 01040 102020 A24:    ADCZ 0,0
34 01041 100006         COM 0,0,SEZ     ;BOTH RESULT AND CARRY=0
35 01042 063077         HALT            ;SEZ FAILED BOTH=0
36                  ;SEE IR13,ZR+IR14,ZC,NOT IR15 ((NEG AND) SKIP CONTROL)
37
38                  ;TEST SKIP EITHER ZERO WITH AC=0 AND CARRY=1
39
40 01043 102040 A25:    ADCO 0,0
41 01044 100006         COM 0,0,SEZ     ;RES=0 BUT CARRY=1
42 01045 063077         HALT            ;SEE ZR,IR13,NOT IR15
```

```
0015 N2LOG
01
02                ;THE NEXT SERIES OF TESTS VERIFY
03                ;THAT REFERENCING ONE AC DOES NOT DISTURB THE OTHERS
04                .MACRO ACITS    ;AC ISOLATION TEST^1
05              ;ACI^1:
06                      ADC ^2,^2
07                      COM ^2,^2       ;SET AC^2 TO 0
08                      ADC ^3,^3       ;SET AC^3 TO -1
09                      MOV ^2,^2,SZR   ;TEST AC^2 TO STILL=0
10                      HALT            ;AC^3 DESTINATION DISTURBED AC^2
11              %
12
13                      ACITS   00      0       1
14              ;ACI00:
15 01046 102000         ADC 0,0
16 01047 100000         COM 0,0 ;SET AC0 TO 0
17 01050 126000         ADC 1,1 ;SET AC1 TO -1
18 01051 101004         MOV 0,0,SZR     ;TEST AC0 TO STILL=0
19 01052 063077         HALT            ;AC1 DESTINATION DISTURBED AC0
20                      ACITS   01      0       2
21              ;ACI01:
22 01053 102000         ADC 0,0
23 01054 100000         COM 0,0 ;SET AC0 TO 0
24 01055 152000         ADC 2,2 ;SET AC2 TO -1
25 01056 101004         MOV 0,0,SZR     ;TEST AC0 TO STILL=0
26 01057 063077         HALT            ;AC2 DESTINATION DISTURBED AC0
27                      ACITS   02      0       3
28              ;ACI02:
29 01060 102000         ADC 0,0
30 01061 100000         COM 0,0 ;SET AC0 TO 0
31 01062 176000         ADC 3,3 ;SET AC3 TO -1
32 01063 101004         MOV 0,0,SZR     ;TEST AC0 TO STILL=0
33 01064 063077         HALT            ;AC3 DESTINATION DISTURBED AC0
34                      ACITS   03      1       0
35              ;ACI03:
36 01065 126000         ADC 1,1
37 01066 124000         COM 1,1 ;SET AC1 TO 0
38 01067 102000         ADC 0,0 ;SET AC0 TO -1
39 01070 125004         MOV 1,1,SZR     ;TEST AC1 TO STILL=0
40 01071 063077         HALT            ;AC0 DESTINATION DISTURBED AC1
41                      ACITS   04      1       2
42              ;ACI04:
43 01072 126000         ADC 1,1
44 01073 124000         COM 1,1 ;SET AC1 TO 0
45 01074 152000         ADC 2,2 ;SET AC2 TO -1
46 01075 125004         MOV 1,1,SZR     ;TEST AC1 TO STILL=0
47 01076 063077         HALT            ;AC2 DESTINATION DISTURBED AC1
48                      ACITS   05      1       3
49              ;ACI05:
50 01077 126000         ADC 1,1
51 01100 124000         COM 1,1 ;SET AC1 TO 0
52 01101 176000         ADC 3,3 ;SET AC3 TO -1
53 01102 125004         MOV 1,1,SZR     ;TEST AC1 TO STILL=0
54 01103 063077         HALT            ;AC3 DESTINATION DISTURBED AC1
55                      ACITS   06      2       0
56              ;ACI06:
57 01104 152000         ADC 2,2
58 01105 150000         COM 2,2 ;SET AC2 TO 0
59 01106 102000         ADC 0,0 ;SET AC0 TO -1
60 01107 151004         MOV 2,2,SZR     ;TEST AC2 TO STILL=0
```

```
0016 N2LOG
01 01110 063077         HALT            ;AC0 DESTINATION DISTURBED AC2
02                      ACITS   07      2       1
03              ;ACI07:
04 01111 152000         ADC 2,2
05 01112 150000         COM 2,2 ;SET AC2 TO 0
06 01113 126000         ADC 1,1 ;SET AC1 TO -1
07 01114 151004         MOV 2,2,SZR     ;TEST AC2 TO STILL=0
08 01115 063077         HALT            ;AC1 DESTINATION DISTURBED AC2
09                      ACITS   08      2       3
10              ;ACI08:
11 01116 152000         ADC 2,2
12 01117 150000         COM 2,2 ;SET AC2 TO 0
13 01120 176000         ADC 3,3 ;SET AC3 TO -1
14 01121 151004         MOV 2,2,SZR     ;TEST AC2 TO STILL=0
15 01122 063077         HALT            ;AC3 DESTINATION DISTURBED AC2
16                      ACITS   09      3       0
17              ;ACI09:
18 01123 176000         ADC 3,3
19 01124 174000         COM 3,3 ;SET AC3 TO 0
20 01125 102000         ADC 0,0 ;SET AC0 TO -1
21 01126 175004         MOV 3,3,SZR     ;TEST AC3 TO STILL=0
22 01127 063077         HALT            ;AC0 DESTINATION DISTURBED AC3
23                      ACITS   10      3       1
24              ;ACI10:
25 01130 176000         ADC 3,3
26 01131 174000         COM 3,3 ;SET AC3 TO 0
27 01132 126000         ADC 1,1 ;SET AC1 TO -1
28 01133 175004         MOV 3,3,SZR     ;TEST AC3 TO STILL=0
29 01134 063077         HALT            ;AC1 DESTINATION DISTURBED AC3
30                      ACITS   11      3       2
31              ;ACI11:
32 01135 176000         ADC 3,3
33 01136 174000         COM 3,3 ;SET AC3 TO 0
34 01137 152000         ADC 2,2 ;SET AC2 TO -1
35 01140 175004         MOV 3,3,SZR     ;TEST AC3 TO STILL=0
36 01141 063077         HALT            ;AC2 DESTINATION DISTURBED AC3
```

```
;0017 N2LOG
01
02
03                ;THE FOLLOWING TESTS INSURE 0'S ISOLATION
04                ;OF AC TO AC
05
06                      .MACRO ACIT2    ;0'S ISOLATION TEST
07                ;ACI^1:
08                      ADC ^2,^2       ;SET AC^2=-1
09                      COM ^2,^3       ;SET 0'S TO AC^3
10                      COM ^2,^2,SZR   ;AC^2 SHD STILL=-1
11                      HALT            ;0'S TO AC^3 DISTURBED AC^2
12                %
13                      ACIT2   12      0       1
14                ;ACI12:
15 01142 102000         ADC 0,0 ;SET AC0=-1
16 01143 104000         COM 0,1 ;SET 0'S TO AC1
17 01144 100004         COM 0,0,SZR     ;AC0 SHD STILL=-1
18 01145 063077         HALT            ;0'S TO AC1 DISTURBED AC0
19                      ACIT2   13      0       2
20                ;ACI13:
21 01146 102000         ADC 0,0 ;SET AC0=-1
22 01147 110000         COM 0,2 ;SET 0'S TO AC2
23 01150 100004         COM 0,0,SZR     ;AC0 SHD STILL=-1
24 01151 063077         HALT            ;0'S TO AC2 DISTURBED AC0
25                      ACIT2   14      0       3
26                ;ACI14:
27 01152 102000         ADC 0,0 ;SET AC0=-1
28 01153 114000         COM 0,3 ;SET 0'S TO AC3
29 01154 100004         COM 0,0,SZR     ;AC0 SHD STILL=-1
30 01155 063077         HALT            ;0'S TO AC3 DISTURBED AC0
31                      ACIT2   15      1       0
32                ;ACI15:
33 01156 126000         ADC 1,1 ;SET AC1=-1
34 01157 120000         COM 1,0 ;SET 0'S TO AC0
35 01160 124004         COM 1,1,SZR     ;AC1 SHD STILL=-1
36 01161 063077         HALT            ;0'S TO AC0 DISTURBED AC1
37                      ACIT2   16      1       2
38                ;ACI16:
39 01162 126000         ADC 1,1 ;SET AC1=-1
40 01163 130000         COM 1,2 ;SET 0'S TO AC2
41 01164 124004         COM 1,1,SZR     ;AC1 SHD STILL=-1
42 01165 063077         HALT            ;0'S TO AC2 DISTURBED AC1
43                      ACIT2   17      1       3
44                ;ACI17:
45 01166 126000         ADC 1,1 ;SET AC1=-1
46 01167 134000         COM 1,3 ;SET 0'S TO AC3
47 01170 124004         COM 1,1,SZR     ;AC1 SHD STILL=-1
48 01171 063077         HALT            ;0'S TO AC3 DISTURBED AC1
49                      ACIT2   18      2       0
50                ;ACI18:
51 01172 152000         ADC 2,2 ;SET AC2=-1
52 01173 140000         COM 2,0 ;SET 0'S TO AC0
53 01174 150004         COM 2,2,SZR     ;AC2 SHD STILL=-1
54 01175 063077         HALT            ;0'S TO AC0 DISTURBED AC2
55                      ACIT2   19      2       1
56                ;ACI19:
57 01176 152000         ADC 2,2 ;SET AC2=-1
58 01177 144000         COM 2,1 ;SET 0'S TO AC1
59 01200 150004         COM 2,2,SZR     ;AC2 SHD STILL=-1
60 01201 063077         HALT            ;0'S TO AC1 DISTURBED AC2
```

```
;0018 N2LOG
01                      ACIT2   20      2       3
02                ;ACI20:
03 01202 152000         ADC 2,2 ;SET AC2=-1
04 01203 154000         COM 2,3 ;SET 0'S TO AC3
05 01204 150004         COM 2,2,SZR     ;AC2 SHD STILL=-1
06 01205 063077         HALT            ;0'S TO AC3 DISTURBED AC2
07                      ACIT2   21      3       0
08                ;ACI21:
09 01206 176000         ADC 3,3 ;SET AC3=-1
10 01207 160000         COM 3,0 ;SET 0'S TO AC0
11 01210 174004         COM 3,3,SZR     ;AC3 SHD STILL=-1
12 01211 063077         HALT            ;0'S TO AC0 DISTURBED AC3
13                      ACIT2   22      3       1
14                ;ACI22:
15 01212 176000         ADC 3,3 ;SET AC3=-1
16 01213 164000         COM 3,1 ;SET 0'S TO AC1
17 01214 174004         COM 3,3,SZR     ;AC3 SHD STILL=-1
18 01215 063077         HALT            ;0'S TO AC1 DISTURBED AC3
19                      ACIT2   23      3       2
20                ;ACI23:
21 01216 176000         ADC 3,3 ;SET AC3=-1
22 01217 170000         COM 3,2 ;SET 0'S TO AC2
23 01220 174004         COM 3,3,SZR     ;AC3 SHD STILL=-1
24 01221 063077         HALT            ;0'S TO AC2 DISTURBED AC3
25
26
27
```

```
10019 N2LOG
01                  ;AT THIS POINT IN THE TEST THE FOLLOWING
02                  ;ITEMS HAVE BEEN VERIFIED
03                  ;1. NONE OF THE ALC INSTRUCTIONS SKIP EXTRANEOUSLY
04                  ;2. CRY CAN BE SET TO 1 OR 0 AND CRY SKIPS
05                        ;FUNCTION CORRECTLY
06                  ;3. A CONSTANT OTHER THAN 0 CAN BE GENERATED
07                        ;BY AN ADC ANY AC TO ITSELF
08                  ;4. A CONSTANT THAT AT LEAST APPEARS TO=0 CAN
09                        ;BE GENERATED BY AN ADC+COM ANY AC TO ITSELF
10                  ;5. ANY AC MAY BE REFERENCED BY EITHER
11                        ;AN ADC OR COM WITHOUT DISTURBING THE OTHERS
12                  ;6. SNR SKIPS ON -1 DOES NOT SKIP ON 0
13                  ;7. SZR SKIPS ON 0 DOES NOT SKIP ON -1
14                  ;8. NO TRANSFER (IR 12=1) INHIBITS CARRY CHANGE
15
16                  ;TEST LEFT SHIFT OF A 1 INTO 0 CRY
17 01222 102020 A40:    ADCZ 0,0
18 01223 101102         MOVL 0,0,SZC      ;MAKE LEFT SHIFT CRY IN=1
19 01224 101003         MOV 0,0,SNC       ;TEST FOR CRY REALLY=1
20 01225 063077         HALT              ;LEFT SHIFT IR9 FAILED
21                  ;IF GATE IR8=1 AND CALC IS TRUE TEST WILL ALSO FAIL (SWAP)
22                  ;TEST LEFT SHIFT OF A 0 INTO A 1 CRY
23
24 01226 102040 A41:    ADCO 0,0
25 01227 100103         COML 0,0,SNC      ;CRY INPUT (ZC)
26 01230 101002         MOV 0,0,SZC       ;DID 0 REALLY GET TO CRY
27 01231 063077         HALT              ;LEFT SHIFT (IR9) 0 INTO CRY
28
29
```

```
10020 N2LOG
01
02                  ;TEST FOR NO BITS TO PICK UP ON SHIFT LEFT
03
04 01232 102020 A42:    ADCZ 0,0          ;AC0=-1  CRY=0
05 01233 100105         COML 0,0,SNR      ;TEST RESULT LEVELS=0
06 01234 101004         MOV 0,0,SZR       ;AND ACTUAL RESULT=0
07 01235 063077         HALT              ;AC0 L SHOULD=0
08                  ;TEST THE TRANSFER OF A CRY=1 INTO BIT 15 AC 0
09 01236 102040 A43:    ADCO 0,0
10 01237 100105         COML 0,0,SNR      ;CRY SHOULD=1 TO AC 15
11 01240 063077         HALT              ;IF AC0=0 SEE ALU 15
12                  ;IF AC0=+1 SEE NOT SUM 15 INTO SKIP LOGIC
13                  ;IN ABOVE TEST ALU LEVEL INPUT IS NOT SCI (FALSE)
14                  ;NOT SUM 15 GOES LOW FOR LEFT SHIFT ALSO
15                  ;TEST BIT 15=1 STRAIGHT TRANSFER THROUGH
16
17 01241 102040 A44:    ADCO 0,0
18 01242 100104         COML 0,0,SZR      ;IN CASE LEVEL NOT SUM 15 FAILS
19 01243 101005         MOV 0,0,SNR       ;AC0=+1 RESULT IS NON ZERO
20 01244 063077         HALT
21                  ;ABOVE FAILURE IS MOST PROBABLY "NOT ALU 15" FALSE WAS TRUE
22                  ;OR "NOT SUM 15" FALSE INTO ZR AND'S IN SKP LOGIC
23
24                  ;TEST RIGHT SHIFT LOGIC INTO CRY
25                  ;TEST ONES SHIFT INTO A 0 CRY
26                  ;TEST OF IR8=1 ENABLES RIGHT SHIFT INPUTS
27 01245 102223 A45:    ADCZR 0,0,SNC     ;TEST INPUT TO CRY=1
28 01246 063077         HALT
29                  ;IF IR9 AND CALC GATE IS TRUE TEST WILL ALSO FAIL (SWAP)
30
31 01247 102222 A46:    ADCZR 0,0,SZC     ;INPUT TO CRY=1
32 01250 100003         COM 0,0,SNC       ;CRY RIGHT SHD STILL=1
33 01251 063077         HALT
34                  ;TEST RIGHT 0 INPUT TO CRY=1
35
36 01252 102040 A47:    ADCO 0,0
37 01253 100203         COMM 0,0,SNC
38 01254 100002         COM 0,0,SZC
39 01255 063077         HALT              ;CRY SHOULD=0
40                  ;TEST OF NOT ALU0 INPUT TO ZC AND IR88=1
41                  ;
```

```
!0021 N2LOG
01
02                  ;TEST FOR NO BITS TO PICK UP ON RIGHT SHIFT
03
04 01256 102020 A48:    ADCZ 0,0            ;(AC0)=-1 CRY=0
05 01257 100205         COMR 0,0,SNR        ;SHIFT 0'S RIGHT
06 01260 101004         MOV 0,0,SZR         ;RESULT SHOULD REMAIN=0
07 01261 063077         HALT                ;RIGHT SHIFT ALL 0'S FAILED
08                  ;EXAMINE AC0 TO DETERMINE BITS PICKED SHIFT RIGHT
09                  ;SHIFT CRY=1 RIGHT INTO BIT 0
10                  ;ALSO TEST BIT 0=1 INTO NOT ZR
11 01262 102040 A49:    ADCO 0,0            ;CRY=1 AC0=-1
12 01263 100204         COMR 0,0,SZR        ;RIGHT SHIFT 0'S CRY=1 TO BIT 0
13 01264 101205         MOVR 0,0,SNR        ;TEST RESULT TO REALLY HOLD
14 01265 063077         HALT                ;RIGHT SHIFT CRY=1 FAILED
15                  ;ABOVE HALT CAN BE NOT SCI INTO NOT SUM 0 (AC0 WILL=0)
16                  ;OR NOT SUM 0 INTO ZR AND GATES IN SKIP LOGIC (AC0=100000)
17
18                  ;TEST RIGHT SHIFT OF AC0=0'S INTO AC1
19                  ;START BUILDING DOUBLE REGISTERS FOR TEST USAGE
20
21 01266 102000 A50:    ADC 0,0
22 01267 125020         ADCZ 1,1
23 01270 100200         COMR 0,1
24 01271 125004         MOV 1,1,SZR
25 01272 063077         HALT                ;RIGHT SHIFT ALL 0'S TO AC1
26
27                  ;TRANSFER CRY=1 INTO AC1 BIT 0 SHIFT RIGHT
28 01273 102000 A51:    ADC 0,0             ;AC0=-1
29 01274 100040         COMO 0,1            ;AC1=0  CRY=1
30 01275 100200         COMR 0,1            ;RIGHT SHIFT NOT(0) TO AC1
31 01276 125005         MOV 1,1,SNR         ;RESULT SHD=NOT 0 BIT 0=1
32 01277 063077         HALT                ;AC1 SHD=100000
33                  ;ABOVE TESTS WERE TO VERIFY TRANSFER OF AC0 TO AC OCCURS
34                  ;RIGHT SHIFT OR CRY=1 TO BIT 0 WAS PREV. VERIFIED
```

```
!0022 N2LOG
01
02                  ;DEFINE MACRO TO TEST SHIFTS OF
03                  ;A SINGLE ONE BIT INTO THE NEXT POSITION
04                      .MACRO SHIFT
05                  ;THIS IS A A5 SHIFT TEST OF BIT A2 TO BIT A3
06                  ;AC0 SHD=A4 COMING INTO THE TEST
07                  ;ASA1:
08                      MOVA5 0,1,SZR   ;TEST NOT ALUA2 INTO SUMA3
09                      MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
10                      HALT            ;RESULT IN AC1 SHD=A6
11                      MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
12                      HALT            ;STRAIGHT TRANSFER BIT A3 FAILED
13                  ;BIT A3 A5 SHIFT FAILED IF AC1=0 IF=A6 BA3 INTO ZR AND GATES
14                  %
15                  ;SETUP NEXT SERIES OF RIGHT SHIFT TESTS
16 01300 102040         ADCO 0,0
17 01301 100200         COMR 0,0
18 01302 101005         MOV 0,0,SNR
19 01303 063077         HALT            ;BIT 0 SETUP FAILED
20
21                      SHIFT R00,0,1,100000,R,040000
22                  ;THIS IS A R SHIFT TEST OF BIT 0 TO BIT 1
23                  ;AC0 SHD=100000 COMING INTO THE TEST
24                  ;ASR00:
25 01304 102004         MOVR 0,1,SZR    ;TEST NOT ALU0 INTO SUM1
26 01305 125005         MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
27 01306 063077         HALT            ;RESULT IN AC1 SHD=040000
28 01307 121005         MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
29 01310 063077         HALT            ;STRAIGHT TRANSFER BIT 1 FAILED
30                  ;BIT 1 R SHIFT FAILED IF AC1=0 IF=040000 B1 INTO ZR AND GATES
31                      SHIFT R01,1,2,040000,R,020000
32                  ;THIS IS A R SHIFT TEST OF BIT 1 TO BIT 2
33                  ;AC0 SHD=040000 COMING INTO THE TEST
34                  ;ASR01:
35 01311 102004         MOVR 0,1,SZR    ;TEST NOT ALU1 INTO SUM2
36 01312 125005         MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
37 01313 063077         HALT            ;RESULT IN AC1 SHD=020000
38 01314 121005         MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
39 01315 063077         HALT            ;STRAIGHT TRANSFER BIT 2 FAILED
40                  ;BIT 2 R SHIFT FAILED IF AC1=0 IF=020000 B2 INTO ZR AND GATES
41                      SHIFT R02,2,3,020000,R,010000
42                  ;THIS IS A R SHIFT TEST OF BIT 2 TO BIT 3
43                  ;AC0 SHD=020000 COMING INTO THE TEST
44                  ;ASR02:
45 01316 102004         MOVR 0,1,SZR    ;TEST NOT ALU2 INTO SUM3
46 01317 125005         MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
47 01320 063077         HALT            ;RESULT IN AC1 SHD=010000
48 01321 121005         MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
49 01322 063077         HALT            ;STRAIGHT TRANSFER BIT 3 FAILED
50                  ;BIT 3 R SHIFT FAILED IF AC1=0 IF=010000 B3 INTO ZR AND GATES
51                      SHIFT R03,3,4,010000,R,004000
52                  ;THIS IS A R SHIFT TEST OF BIT 3 TO BIT 4
53                  ;AC0 SHD=010000 COMING INTO THE TEST
54                  ;ASR03:
55 01323 102004         MOVR 0,1,SZR    ;TEST NOT ALU3 INTO SUM4
56 01324 125005         MOV 1,1,SNR     ;STRAIGHT TRANSFER COULD ALSO FAIL
57 01325 063077         HALT            ;RESULT IN AC1 SHD=004000
58 01326 121005         MOV 1,0,SNR     ;MOVE RESULT BACK TO AC0 NXT TST
59 01327 063077         HALT            ;STRAIGHT TRANSFER BIT 4 FAILED
60                  ;BIT 4 R SHIFT FAILED IF AC1=0 IF=004000 B4 INTO ZR AND GATES
```

```
01                      SHIFT R04,4,5,004000,R,002000
02                    ;THIS IS A R SHIFT TEST OF BIT 4 TO BIT 5
03                    ;AC0 SHD=004000 COMING INTO THE TEST
04                  ;ASR04:
05 01330 105204             MOVR 0,1,SZR     ;TEST NOT ALU4 INTO SUM5
06 01331 125005             MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
07 01332 063077             HALT             ;RESULT IN AC1 SHD=002000
08 01333 121005             MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
09 01334 063077             HALT             ;STRAIGHT TRANSFER BIT 5 FAILED
10                    ;BIT 5 R SHIFT FAILED IF AC1=0 IF=002000 B5 INTO ZR AND GATES
11                      SHIFT R05,5,6,002000,R,001000
12                    ;THIS IS A R SHIFT TEST OF BIT 5 TO BIT 6
13                    ;AC0 SHD=002000 COMING INTO THE TEST
14                  ;ASR05:
15 01335 105204             MOVR 0,1,SZR     ;TEST NOT ALU5 INTO SUM6
16 01336 125005             MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
17 01337 063077             HALT             ;RESULT IN AC1 SHD=001000
18 01340 121005             MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
19 01341 063077             HALT             ;STRAIGHT TRANSFER BIT 6 FAILED
20                    ;BIT 6 R SHIFT FAILED IF AC1=0 IF=001000 B6 INTO ZR AND GATES
21                      SHIFT R06,6,7,001000,R,000400
22                    ;THIS IS A R SHIFT TEST OF BIT 6 TO BIT 7
23                    ;AC0 SHD=001000 COMING INTO THE TEST
24                  ;ASR06:
25 01342 105204             MOVR 0,1,SZR     ;TEST NOT ALU6 INTO SUM7
26 01343 125005             MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
27 01344 063077             HALT             ;RESULT IN AC1 SHD=000400
28 01345 121005             MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
29 01346 063077             HALT             ;STRAIGHT TRANSFER BIT 7 FAILED
30                    ;BIT 7 R SHIFT FAILED IF AC1=0 IF=000400 B7 INTO ZR AND GATES
31                      SHIFT R07,7,8,000400,R,000200
32                    ;THIS IS A R SHIFT TEST OF BIT 7 TO BIT 8
33                    ;AC0 SHD=000400 COMING INTO THE TEST
34                  ;ASR07:
35 01347 105204             MOVR 0,1,SZR     ;TEST NOT ALU7 INTO SUM8
36 01350 125005             MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
37 01351 063077             HALT             ;RESULT IN AC1 SHD=000200
38 01352 121005             MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
39 01353 063077             HALT             ;STRAIGHT TRANSFER BIT 8 FAILED
40                    ;BIT 8 R SHIFT FAILED IF AC1=0 IF=000200 B8 INTO ZR AND GATES
41                      SHIFT R08,8,9,000200,R,000100
42                    ;THIS IS A R SHIFT TEST OF BIT 8 TO BIT 9
43                    ;AC0 SHD=000200 COMING INTO THE TEST
44                  ;ASR08:
45 01354 105204             MOVR 0,1,SZR     ;TEST NOT ALU8 INTO SUM9
46 01355 125005             MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
47 01356 063077             HALT             ;RESULT IN AC1 SHD=000100
48 01357 121005             MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
49 01360 063077             HALT             ;STRAIGHT TRANSFER BIT 9 FAILED
50                    ;BIT 9 R SHIFT FAILED IF AC1=0 IF=000100 B9 INTO ZR AND GATES
51                      SHIFT R09,9,10,000100,R,000040
52                    ;THIS IS A R SHIFT TEST OF BIT 9 TO BIT 10
53                    ;AC0 SHD=000100 COMING INTO THE TEST
54                  ;ASR09:
55 01361 105204             MOVR 0,1,SZR     ;TEST NOT ALU9 INTO SUM10
56 01362 125005             MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
57 01363 063077             HALT             ;RESULT IN AC1 SHD=000040
58 01364 121005             MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
59 01365 063077             HALT             ;STRAIGHT TRANSFER BIT 10 FAILED
60                    ;BIT 10 R SHIFT FAILED IF AC1=0 IF=000040 B10 INTO ZR AND GATE
```



```
01                      SHIFT R10,10,11,000040,R,000020
02                    ;THIS IS A R SHIFT TEST OF BIT 10 TO BIT 11
03                    ;AC0 SHD=000040 COMING INTO THE TEST
04                  ;ASR10:
05 01366 105204             MOVR 0,1,SZR     ;TEST NOT ALU10 INTO SUM11
06 01367 125005             MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
07 01370 063077             HALT             ;RESULT IN AC1 SHD=000020
08 01371 121005             MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
09 01372 063077             HALT             ;STRAIGHT TRANSFER BIT 11 FAILED
10                    ;BIT 11 R SHIFT FAILED IF AC1=0 IF=000020 B11 INTO ZR AND GATE
11                      SHIFT R11,11,12,000020,R,000010
12                    ;THIS IS A R SHIFT TEST OF BIT 11 TO BIT 12
13                    ;AC0 SHD=000020 COMING INTO THE TEST
14                  ;ASR11:
15 01373 105204             MOVR 0,1,SZR     ;TEST NOT ALU11 INTO SUM12
16 01374 125005             MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
17 01375 063077             HALT             ;RESULT IN AC1 SHD=000010
18 01376 121005             MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
19 01377 063077             HALT             ;STRAIGHT TRANSFER BIT 12 FAILED
20                    ;BIT 12 R SHIFT FAILED IF AC1=0 IF=000010 B12 INTO ZR AND GATE
21                      SHIFT R12,12,13,000010,R,000004
22                    ;THIS IS A R SHIFT TEST OF BIT 12 TO BIT 13
23                    ;AC0 SHD=000010 COMING INTO THE TEST
24                  ;ASR12:
25 01400 105204             MOVR 0,1,SZR     ;TEST NOT ALU12 INTO SUM13
26 01401 125005             MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
27 01402 063077             HALT             ;RESULT IN AC1 SHD=000004
28 01403 121005             MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
29 01404 063077             HALT             ;STRAIGHT TRANSFER BIT 13 FAILED
30                    ;BIT 13 R SHIFT FAILED IF AC1=0 IF=000004 B13 INTO ZR AND GATE
31                      SHIFT R13,13,14,000004,R,000002
32                    ;THIS IS A R SHIFT TEST OF BIT 13 TO BIT 14
33                    ;AC0 SHD=000004 COMING INTO THE TEST
34                  ;ASR13:
35 01405 105204             MOVR 0,1,SZR     ;TEST NOT ALU13 INTO SUM14
36 01406 125005             MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
37 01407 063077             HALT             ;RESULT IN AC1 SHD=000002
38 01410 121005             MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
39 01411 063077             HALT             ;STRAIGHT TRANSFER BIT 14 FAILED
40                    ;BIT 14 R SHIFT FAILED IF AC1=0 IF=000002 B14 INTO ZR AND GATE
41                      SHIFT R14,14,15,000002,R,000001
42                    ;THIS IS A R SHIFT TEST OF BIT 14 TO BIT 15
43                    ;AC0 SHD=000002 COMING INTO THE TEST
44                  ;ASR14:
45 01412 105204             MOVR 0,1,SZR     ;TEST NOT ALU14 INTO SUM15
46 01413 125005             MOV 1,1,SNR      ;STRAIGHT TRANSFER COULD ALSO FAIL
47 01414 063077             HALT             ;RESULT IN AC1 SHD=000001
48 01415 121005             MOV 1,0,SNR      ;MOVE RESULT BACK TO AC0 NXT TST
49 01416 063077             HALT             ;STRAIGHT TRANSFER BIT 15 FAILED
50                    ;BIT 15 R SHIFT FAILED IF AC1=0 IF=000001 B15 INTO ZR AND GATE
51
52 01417 105205 ASR15:  MOVR 0,1,SNR     ;TEST BIT 15=1 R TO CRY
53 01420 125004             MOV 1,1,SZR      ;AC1 SHD=0'S
54 01421 063077             HALT
55 01422 125003             MOV 1,1,SNC      ;AND CRY SHD=1
56 01423 063077             HALT
```

```
0025 N2LOG
01
02                ;LEFT SHIFT SINGLE BIT TESTS
03                ;SET UP A 1 IN BIT 15
04
05 01424 102040         ADCO 0,0
06 01425 100104         COML 0,0,SZR
07 01426 101005         MOV 0,0,SNR
08 01427 063077         HALT                ;AC0 SHO=1 SETUP FAILED
09
10                      SHIFT L00,15,14,000001,L,000002
11                ;THIS IS A L SHIFT TEST OF BIT 15 TO BIT 14
12                ;AC0 SHO=000001 COMING INTO THE TEST
13              ;ASL00:
14 01430 105104         MOVL 0,1,SZR        ;TEST NOT ALU15 INTO SUM14
15 01431 125005         MOV 1,1,SNR         ;STRAIGHT TRANSFER COULD ALSO FAIL
16 01432 063077         HALT                ;RESULT IN AC1 SHO=000002
17 01433 121005         MOV 1,0,SNR         ;MOVE RESULT BACK TO AC0 NXT TST
18 01434 063077         HALT                ;STRAIGHT TRANSFER BIT 14 FAILED
19                ;BIT 14 L SHIFT FAILED IF AC1=0 IF=000002 B14 INTO ZR AND GATE
20                      SHIFT L01,14,13,000002,L,000004
21                ;THIS IS A L SHIFT TEST OF BIT 14 TO BIT 13
22                ;AC0 SHO=000002 COMING INTO THE TEST
23              ;ASL01:
24 01435 105104         MOVL 0,1,SZR        ;TEST NOT ALU14 INTO SUM13
25 01436 125005         MOV 1,1,SNR         ;STRAIGHT TRANSFER COULD ALSO FAIL
26 01437 063077         HALT                ;RESULT IN AC1 SHO=000004
27 01440 121005         MOV 1,0,SNR         ;MOVE RESULT BACK TO AC0 NXT TST
28 01441 063077         HALT                ;STRAIGHT TRANSFER BIT 13 FAILED
29                ;BIT 13 L SHIFT FAILED IF AC1=0 IF=000004 B13 INTO ZR AND GATE
30                      SHIFT L02,13,12,000004,L,000010
31                ;THIS IS A L SHIFT TEST OF BIT 13 TO BIT 12
32                ;AC0 SHO=000004 COMING INTO THE TEST
33              ;ASL02:
34 01442 105104         MOVL 0,1,SZR        ;TEST NOT ALU13 INTO SUM12
35 01443 125005         MOV 1,1,SNR         ;STRAIGHT TRANSFER COULD ALSO FAIL
36 01444 063077         HALT                ;RESULT IN AC1 SHO=000010
37 01445 121005         MOV 1,0,SNR         ;MOVE RESULT BACK TO AC0 NXT TST
38 01446 063077         HALT                ;STRAIGHT TRANSFER BIT 12 FAILED
39                ;BIT 12 L SHIFT FAILED IF AC1=0 IF=000010 B12 INTO ZR AND GATE
40                      SHIFT L03,12,11,000010,L,000020
41                ;THIS IS A L SHIFT TEST OF BIT 12 TO BIT 11
42                ;AC0 SHO=000010 COMING INTO THE TEST
43              ;ASL03:
44 01447 105104         MOVL 0,1,SZR        ;TEST NOT ALU12 INTO SUM11
45 01450 125005         MOV 1,1,SNR         ;STRAIGHT TRANSFER COULD ALSO FAIL
46 01451 063077         HALT                ;RESULT IN AC1 SHO=000020
47 01452 121005         MOV 1,0,SNR         ;MOVE RESULT BACK TO AC0 NXT TST
48 01453 063077         HALT                ;STRAIGHT TRANSFER BIT 11 FAILED
49                ;BIT 11 L SHIFT FAILED IF AC1=0 IF=000020 B11 INTO ZR AND GATE
50                      SHIFT L04,11,10,000020,L,000040
51                ;THIS IS A L SHIFT TEST OF BIT 11 TO BIT 10
52                ;AC0 SHO=000020 COMING INTO THE TEST
53              ;ASL04:
54 01454 105104         MOVL 0,1,SZR        ;TEST NOT ALU11 INTO SUM10
55 01455 125005         MOV 1,1,SNR         ;STRAIGHT TRANSFER COULD ALSO FAIL
56 01456 063077         HALT                ;RESULT IN AC1 SHO=000040
57 01457 121005         MOV 1,0,SNR         ;MOVE RESULT BACK TO AC0 NXT TST
58 01460 063077         HALT                ;STRAIGHT TRANSFER BIT 10 FAILED
59                ;BIT 10 L SHIFT FAILED IF AC1=0 IF=000040 B10 INTO ZR AND GATE
60                      SHIFT L05,10,09,000040,L,000100
```

```
0026 N2LOG
01                ;THIS IS A L SHIFT TEST OF BIT 10 TO BIT 09
02                ;AC0 SHO=000040 COMING INTO THE TEST
03              ;ASL05:
04 01461 105104         MOVL 0,1,SZR        ;TEST NOT ALU10 INTO SUM09
05 01462 125005         MOV 1,1,SNR         ;STRAIGHT TRANSFER COULD ALSO FAIL
06 01463 063077         HALT                ;RESULT IN AC1 SHO=000100
07 01464 121005         MOV 1,0,SNR         ;MOVE RESULT BACK TO AC0 NXT TST
08 01465 063077         HALT                ;STRAIGHT TRANSFER BIT 09 FAILED
09                ;BIT 09 L SHIFT FAILED IF AC1=0 IF=000100 B09 INTO ZR AND GATE
10                      SHIFT L06,09,08,000100,L,000200
11                ;THIS IS A L SHIFT TEST OF BIT 09 TO BIT 08
12                ;AC0 SHO=000100 COMING INTO THE TEST
13              ;ASL06:
14 01466 105104         MOVL 0,1,SZR        ;TEST NOT ALU09 INTO SUM08
15 01467 125005         MOV 1,1,SNR         ;STRAIGHT TRANSFER COULD ALSO FAIL
16 01470 063077         HALT                ;RESULT IN AC1 SHO=000200
17 01471 121005         MOV 1,0,SNR         ;MOVE RESULT BACK TO AC0 NXT TST
18 01472 063077         HALT                ;STRAIGHT TRANSFER BIT 08 FAILED
19                ;BIT 08 L SHIFT FAILED IF AC1=0 IF=000200 B08 INTO ZR AND GATE
20                      SHIFT L07,08,07,000200,L,000400
21                ;THIS IS A L SHIFT TEST OF BIT 08 TO BIT 07
22                ;AC0 SHO=000200 COMING INTO THE TEST
23              ;ASL07:
24 01473 105104         MOVL 0,1,SZR        ;TEST NOT ALU08 INTO SUM07
25 01474 125005         MOV 1,1,SNR         ;STRAIGHT TRANSFER COULD ALSO FAIL
26 01475 063077         HALT                ;RESULT IN AC1 SHO=000400
27 01476 121005         MOV 1,0,SNR         ;MOVE RESULT BACK TO AC0 NXT TST
28 01477 063077         HALT                ;STRAIGHT TRANSFER BIT 07 FAILED
29                ;BIT 07 L SHIFT FAILED IF AC1=0 IF=000400 B07 INTO ZR AND GATE
30                      SHIFT L08,07,06,000400,L,001000
31                ;THIS IS A L SHIFT TEST OF BIT 07 TO BIT 06
32                ;AC0 SHO=000400 COMING INTO THE TEST
33              ;ASL08:
34 01500 105104         MOVL 0,1,SZR        ;TEST NOT ALU07 INTO SUM06
35 01501 125005         MOV 1,1,SNR         ;STRAIGHT TRANSFER COULD ALSO FAIL
36 01502 063077         HALT                ;RESULT IN AC1 SHO=001000
37 01503 121005         MOV 1,0,SNR         ;MOVE RESULT BACK TO AC0 NXT TST
38 01504 063077         HALT                ;STRAIGHT TRANSFER BIT 06 FAILED
39                ;BIT 06 L SHIFT FAILED IF AC1=0 IF=001000 B06 INTO ZR AND GATE
40                      SHIFT L09,06,05,001000,L,002000
41                ;THIS IS A L SHIFT TEST OF BIT 06 TO BIT 05
42                ;AC0 SHO=001000 COMING INTO THE TEST
43              ;ASL09:
44 01505 105104         MOVL 0,1,SZR        ;TEST NOT ALU06 INTO SUM05
45 01506 125005         MOV 1,1,SNR         ;STRAIGHT TRANSFER COULD ALSO FAIL
46 01507 063077         HALT                ;RESULT IN AC1 SHO=002000
47 01510 121005         MOV 1,0,SNR         ;MOVE RESULT BACK TO AC0 NXT TST
48 01511 063077         HALT                ;STRAIGHT TRANSFER BIT 05 FAILED
49                ;BIT 05 L SHIFT FAILED IF AC1=0 IF=002000 B05 INTO ZR AND GATE
50                      SHIFT L10,05,04,002000,L,004000
51                ;THIS IS A L SHIFT TEST OF BIT 05 TO BIT 04
52                ;AC0 SHO=002000 COMING INTO THE TEST
53              ;ASL10:
54 01512 105104         MOVL 0,1,SZR        ;TEST NOT ALU05 INTO SUM04
55 01513 125005         MOV 1,1,SNR         ;STRAIGHT TRANSFER COULD ALSO FAIL
56 01514 063077         HALT                ;RESULT IN AC1 SHO=004000
57 01515 121005         MOV 1,0,SNR         ;MOVE RESULT BACK TO AC0 NXT TST
58 01516 063077         HALT                ;STRAIGHT TRANSFER BIT 04 FAILED
59                ;BIT 04 L SHIFT FAILED IF AC1=0 IF=004000 B04 INTO ZR AND GATE
60                      SHIFT L11,04,03,004000,L,010000
```

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 0027 N2LOG
01                      ;THIS IS A L SHIFT TEST OF BIT 04 TO BIT 03
02                      ;AC0 SHD=004000 COMING INTO THE TEST
03                    ;ASL11:
04 01517 105104               MOVL 0,1,SZR      ;TEST NOT ALU04 INTO SUM03
05 01520 125005               MOV 1,1,SNR       ;STRAIGHT TRANSFER COULD ALSO FAIL
06 01521 063077               HALT              ;RESULT IN AC1 SHD=010000
07 01522 121005               MOV 1,0,SNR       ;MOVE RESULT BACK TO AC0 NXT TST
08 01523 063077               HALT              ;STRAIGHT TRANSFER BIT 03 FAILED
09                      ;BIT 03 L SHIFT FAILED IF AC1=0 IF=010000 B03 INTO ZR AND GATE
10                            SHIFT L12,03,02,010000,L,020000
11                      ;THIS IS A L SHIFT TEST OF BIT 03 TO BIT 02
12                      ;AC0 SHD=010000 COMING INTO THE TEST
13                    ;ASL12:
14 01524 105104               MOVL 0,1,SZR      ;TEST NOT ALU03 INTO SUM02
15 01525 125005               MOV 1,1,SNR       ;STRAIGHT TRANSFER COULD ALSO FAIL
16 01526 063077               HALT              ;RESULT IN AC1 SHD=020000
17 01527 121005               MOV 1,0,SNR       ;MOVE RESULT BACK TO AC0 NXT TST
18 01530 063077               HALT              ;STRAIGHT TRANSFER BIT 02 FAILED
19                      ;BIT 02 L SHIFT FAILED IF AC1=0 IF=020000 B02 INTO ZR AND GATE
20                            SHIFT L13,02,01,020000,L,040000
21                      ;THIS IS A L SHIFT TEST OF BIT 02 TO BIT 01
22                      ;AC0 SHD=020000 COMING INTO THE TEST
23                    ;ASL13:
24 01531 105104               MOVL 0,1,SZR      ;TEST NOT ALU02 INTO SUM01
25 01532 125005               MOV 1,1,SNR       ;STRAIGHT TRANSFER COULD ALSO FAIL
26 01533 063077               HALT              ;RESULT IN AC1 SHD=040000
27 01534 121005               MOV 1,0,SNR       ;MOVE RESULT BACK TO AC0 NXT TST
28 01535 063077               HALT              ;STRAIGHT TRANSFER BIT 01 FAILED
29                      ;BIT 01 L SHIFT FAILED IF AC1=0 IF=040000 B01 INTO ZR AND GATE
30                            SHIFT L14,01,00,040000,L,100000
31                      ;THIS IS A L SHIFT TEST OF BIT 01 TO BIT 00
32                      ;AC0 SHD=040000 COMING INTO THE TEST
33                    ;ASL14:
34 01536 105104               MOVL 0,1,SZR      ;TEST NOT ALU01 INTO SUM00
35 01537 125005               MOV 1,1,SNR       ;STRAIGHT TRANSFER COULD ALSO FAIL
36 01540 063077               HALT              ;RESULT IN AC1 SHD=100000
37 01541 121005               MOV 1,0,SNR       ;MOVE RESULT BACK TO AC0 NXT TST
38 01542 063077               HALT              ;STRAIGHT TRANSFER BIT 00 FAILED
39                      ;BIT 00 L SHIFT FAILED IF AC1=0 IF=100000 B00 INTO ZR AND GATE
40
41 01543 105105 ASL15:  MOVL 0,1,SNR      ;AC0=100000
42 01544 125004               MOV 1,1,SZR       ;RESULT LEFT SHD=0'S
43 01545 063077               HALT              ;PICKED UP EXTRA BITS LEFT
44 01546 125003               MOV 1,1,SNC
45 01547 063077               HALT              ;LOST CARRY LAST LEFT SHIFT
```

```
 0028 N2LOG
01                      ;SHIFT A 0 BIT IN FIELD OF ONES
02                      ;DEFINITION OF MACRO FOR TESTING SAME
03                            .MACRO7 SHIFZ
04                      ;THIS IS A ^5 SHIFT TEST OF NOT BIT ^2 TO NOT BIT ^3
05                    ;AS^1:
06                            MOVO^5 0,1        ;AC0 SHD=^4 COMING INTO TEST
07                            COMZ^5 0,2,SNR    ;AC2 SHD=COM OF ^6
08                            HALT
09                            COM 2,2           ;AC2 SHD NOW=AC1
10                            ADC 1,2           ;THE ADDITION OF COM SHD=-1
11                            COM 2,2,SZR       ;AND RESULT SHD=0 ALL SHIFTS OK
12                            HALT              ;BIT ^2 ^5 TO BIT ^3 FAILED
13                      ;AC0=^4 ORIGINAL TO ^6 IN AC1 AC2 WAS COM OF AC1
14                      ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
15                      ;WAS PREVIOUSLY VERIFIED SEE NOT ALU^2 INTO NOT SUM^3
16                            MOV 1,0           ;SET UP NEXT TEST
17                    %
18                      ;SET UP SERIES OF RIGHT SHIFT TESTS
19                      ;BY SETTING AC0 TO 077777
20 01550 102000               ADC 0,0
21 01551 100240               COMOR 0,0         ;SEQUENCE MUST LIKELY TO
22 01552 100000               COM 0,0           ;SET AC0=077777
23 01553 110005               COM 0,2,SNR
24 01554 063077               HALT              ;SETUP FAILED CRY=0 TO BIT 0
25 01555 105000               MOV 0,1
26 01556 150000               COM 2,2           ;RETEST INSTRUCTION
27 01557 132000               ADC 1,2           ;CHECK SEQUENCE
28 01560 150004               COM 2,2,SZR       ;JUST TO MAKE SURE IT WORKS
29 01561 063077               HALT              ;COMPARE OF AC0=077777 FAILED
```

```
10029 N2LOG
01
02                      SHIFZ R16,0,1,077777,R,137777
03                  ;THIS IS A R SHIFT TEST OF NOT BIT 0 TO NOT BIT 1
04                ;ASR16:
05 01562 105240         MOVOR 0,1           ;AC0 SHD=077777 COMING INTO TEST
06 01563 110225         COMZR 0,2,SNR       ;AC2 SHD=COM OF 137777
07 01564 063077         HALT
08 01565 150000         COM 2,2             ;AC2 SHD NOW=AC1
09 01566 132000         ADC 1,2             ;THE ADDITION OF COM SHD=-1
10 01567 150004         COM 2,2,SZR         ;AND RESULT SHD=0 ALL SHIFTS OK
11 01570 063077         HALT                ;BIT 0 R TO BIT 1 FAILED
12                  ;AC0=077777 ORIGINAL TO 137777 IN AC1 AC2 WAS COM OF AC1
13                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
14                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU0 INTO NOT SUM1
15 01571 121000         MOV 1,0             ;SET UP NEXT TEST
16                      SHIFZ R17,1,2,137777,R,157777
17                  ;THIS IS A R SHIFT TEST OF NOT BIT 1 TO NOT BIT 2
18                ;ASR17:
19 01572 105240         MOVOR 0,1           ;AC0 SHD=137777 COMING INTO TEST
20 01573 110225         COMZR 0,2,SNR       ;AC2 SHD=COM OF 157777
21 01574 063077         HALT
22 01575 150000         COM 2,2             ;AC2 SHD NOW=AC1
23 01576 132000         ADC 1,2             ;THE ADDITION OF COM SHD=-1
24 01577 150004         COM 2,2,SZR         ;AND RESULT SHD=0 ALL SHIFTS OK
25 01600 063077         HALT                ;BIT 1 R TO BIT 2 FAILED
26                  ;AC0=137777 ORIGINAL TO 157777 IN AC1 AC2 WAS COM OF AC1
27                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
28                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU1 INTO NOT SUM2
29 01601 121000         MOV 1,0             ;SET UP NEXT TEST
30                      SHIFZ R18,2,3,157777,R,167777
31                  ;THIS IS A R SHIFT TEST OF NOT BIT 2 TO NOT BIT 3
32                ;ASR18:
33 01602 105240         MOVOR 0,1           ;AC0 SHD=157777 COMING INTO TEST
34 01603 110225         COMZR 0,2,SNR       ;AC2 SHD=COM OF 167777
35 01604 063077         HALT
36 01605 150000         COM 2,2             ;AC2 SHD NOW=AC1
37 01606 132000         ADC 1,2             ;THE ADDITION OF COM SHD=-1
38 01607 150004         COM 2,2,SZR         ;AND RESULT SHD=0 ALL SHIFTS OK
39 01610 063077         HALT                ;BIT 2 R TO BIT 3 FAILED
40                  ;AC0=157777 ORIGINAL TO 167777 IN AC1 AC2 WAS COM OF AC1
41                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
42                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU2 INTO NOT SUM3
43 01611 121000         MOV 1,0             ;SET UP NEXT TEST
44                      SHIFZ R19,3,4,167777,R,173777
45                  ;THIS IS A R SHIFT TEST OF NOT BIT 3 TO NOT BIT 4
46                ;ASR19:
47 01612 105240         MOVOR 0,1           ;AC0 SHD=167777 COMING INTO TEST
48 01613 110225         COMZR 0,2,SNR       ;AC2 SHD=COM OF 173777
49 01614 063077         HALT
50 01615 150000         COM 2,2             ;AC2 SHD NOW=AC1
51 01616 132000         ADC 1,2             ;THE ADDITION OF COM SHD=-1
52 01617 150004         COM 2,2,SZR         ;AND RESULT SHD=0 ALL SHIFTS OK
53 01620 063077         HALT                ;BIT 3 R TO BIT 4 FAILED
54                  ;AC0=167777 ORIGINAL TO 173777 IN AC1 AC2 WAS COM OF AC1
55                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
56                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU3 INTO NOT SUM4
57 01621 121000         MOV 1,0             ;SET UP NEXT TEST
58                      SHIFZ R20,4,5,173777,R,175777
59                  ;THIS IS A R SHIFT TEST OF NOT BIT 4 TO NOT BIT 5
60                ;ASR20:
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0030 N2LOG
01 01622 105240         MOVOR 0,1           ;AC0 SHD=173777 COMING INTO TEST
02 01623 110225         COMZR 0,2,SNR       ;AC2 SHD=COM OF 175777
03 01624 063077         HALT
04 01625 150000         COM 2,2             ;AC2 SHD NOW=AC1
05 01626 132000         ADC 1,2             ;THE ADDITION OF COM SHD=-1
06 01627 150004         COM 2,2,SZR         ;AND RESULT SHD=0 ALL SHIFTS OK
07 01630 063077         HALT                ;BIT 4 R TO BIT 5 FAILED
08                  ;AC0=173777 ORIGINAL TO 175777 IN AC1 AC2 WAS COM OF AC1
09                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
10                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU4 INTO NOT SUM5
11 01631 121000         MOV 1,0             ;SET UP NEXT TEST
12                      SHIFZ R21,5,6,175777,R,176777
13                  ;THIS IS A R SHIFT TEST OF NOT BIT 5 TO NOT BIT 6
14                ;ASR21:
15 01632 105240         MOVOR 0,1           ;AC0 SHD=175777 COMING INTO TEST
16 01633 110225         COMZR 0,2,SNR       ;AC2 SHD=COM OF 176777
17 01634 063077         HALT
18 01635 150000         COM 2,2             ;AC2 SHD NOW=AC1
19 01636 132000         ADC 1,2             ;THE ADDITION OF COM SHD=-1
20 01637 150004         COM 2,2,SZR         ;AND RESULT SHD=0 ALL SHIFTS OK
21 01640 063077         HALT                ;BIT 5 R TO BIT 6 FAILED
22                  ;AC0=175777 ORIGINAL TO 176777 IN AC1 AC2 WAS COM OF AC1
23                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
24                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU5 INTO NOT SUM6
25 01641 121000         MOV 1,0             ;SET UP NEXT TEST
26                      SHIFZ R22,6,7,176777,R,177377
27                  ;THIS IS A R SHIFT TEST OF NOT BIT 6 TO NOT BIT 7
28                ;ASR22:
29 01642 105240         MOVOR 0,1           ;AC0 SHD=176777 COMING INTO TEST
30 01643 110225         COMZR 0,2,SNR       ;AC2 SHD=COM OF 177377
31 01644 063077         HALT
32 01645 150000         COM 2,2             ;AC2 SHD NOW=AC1
33 01646 132000         ADC 1,2             ;THE ADDITION OF COM SHD=-1
34 01647 150004         COM 2,2,SZR         ;AND RESULT SHD=0 ALL SHIFTS OK
35 01650 063077         HALT                ;BIT 6 R TO BIT 7 FAILED
36                  ;AC0=176777 ORIGINAL TO 177377 IN AC1 AC2 WAS COM OF AC1
37                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
38                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU6 INTO NOT SUM7
39 01651 121000         MOV 1,0             ;SET UP NEXT TEST
40                      SHIFZ R23,7,8,177377,R,177577
41                  ;THIS IS A R SHIFT TEST OF NOT BIT 7 TO NOT BIT 8
42                ;ASR23:
43 01652 105240         MOVOR 0,1           ;AC0 SHD=177377 COMING INTO TEST
44 01653 110225         COMZR 0,2,SNR       ;AC2 SHD=COM OF 177577
45 01654 063077         HALT
46 01655 150000         COM 2,2             ;AC2 SHD NOW=AC1
47 01656 132000         ADC 1,2             ;THE ADDITION OF COM SHD=-1
48 01657 150004         COM 2,2,SZR         ;AND RESULT SHD=0 ALL SHIFTS OK
49 01660 063077         HALT                ;BIT 7 R TO BIT 8 FAILED
50                  ;AC0=177377 ORIGINAL TO 177577 IN AC1 AC2 WAS COM OF AC1
51                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
52                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU7 INTO NOT SUM8
53 01661 121000         MOV 1,0             ;SET UP NEXT TEST
54                      SHIFZ R24,8,9,177577,R,177677
55                  ;THIS IS A R SHIFT TEST OF NOT BIT 8 TO NOT BIT 9
56                ;ASR24:
57 01662 105240         MOVOR 0,1           ;AC0 SHD=177577 COMING INTO TEST
58 01663 110225         COMZR 0,2,SNR       ;AC2 SHD=COM OF 177677
59 01664 063077         HALT
60 01665 150000         COM 2,2             ;AC2 SHD NOW=AC1
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0031 N2LOG
01 01666 132000          ADC 1,2          ;THE ADDITION OF COM SHD=-1
02 01667 150004          COM 2,2,SZR      ;AND RESULT SHD=0 ALL SHIFTS OK
03 01670 063077          HALT             ;BIT 8 R TO BIT 9 FAILED
04                  ;AC0=177577 ORIGINAL TO 177677 IN AC1 AC2 WAS COM OF AC1
05                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
06                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU8 INTO NOT SUM9
07 01671 121000          MOV 1,0          ;SET UP NEXT TEST
08                       SHIFZ R25,9,10,177677,R,177737
09                  ;THIS IS A R SHIFT TEST OF NOT BIT 9 TO NOT BIT 10
10                ;ASR25:
11 01672 105240          MOVOR 0,1        ;AC0 SHD=177677 COMING INTO TEST
12 01673 110225          COMZR 0,2,SNR    ;AC2 SHD=COM OF 177737
13 01674 063077          HALT
14 01675 150000          COM 2,2          ;AC2 SHD NOW=AC1
15 01676 132000          ADC 1,2          ;THE ADDITION OF COM SHD=-1
16 01677 150004          COM 2,2,SZR      ;AND RESULT SHD=0 ALL SHIFTS OK
17 01700 063077          HALT             ;BIT 9 R TO BIT 10 FAILED
18                  ;AC0=177677 ORIGINAL TO 177737 IN AC1 AC2 WAS COM OF AC1
19                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
20                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU9 INTO NOT SUM10
21 01701 121000          MOV 1,0          ;SET UP NEXT TEST
22                       SHIFZ R26,10,11,177737,R,177757
23                  ;THIS IS A R SHIFT TEST OF NOT BIT 10 TO NOT BIT 11
24                ;ASR26:
25 01702 105240          MOVOR 0,1        ;AC0 SHD=177737 COMING INTO TEST
26 01703 110225          COMZR 0,2,SNR    ;AC2 SHD=COM OF 177757
27 01704 063077          HALT
28 01705 150000          COM 2,2          ;AC2 SHD NOW=AC1
29 01706 132000          ADC 1,2          ;THE ADDITION OF COM SHD=-1
30 01707 150004          COM 2,2,SZR      ;AND RESULT SHD=0 ALL SHIFTS OK
31 01710 063077          HALT             ;BIT 10 R TO BIT 11 FAILED
32                  ;AC0=177737 ORIGINAL TO 177757 IN AC1 AC2 WAS COM OF AC1
33                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
34                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU10 INTO NOT SUM11
35 01711 121000          MOV 1,0          ;SET UP NEXT TEST
36                       SHIFZ R27,11,12,177757,R,177767
37                  ;THIS IS A R SHIFT TEST OF NOT BIT 11 TO NOT BIT 12
38                ;ASR27:
39 01712 105240          MOVOR 0,1        ;AC0 SHD=177757 COMING INTO TEST
40 01713 110225          COMZR 0,2,SNR    ;AC2 SHD=COM OF 177767
41 01714 063077          HALT
42 01715 150000          COM 2,2          ;AC2 SHD NOW=AC1
43 01716 132000          ADC 1,2          ;THE ADDITION OF COM SHD=-1
44 01717 150004          COM 2,2,SZR      ;AND RESULT SHD=0 ALL SHIFTS OK
45 01720 063077          HALT             ;BIT 11 R TO BIT 12 FAILED
46                  ;AC0=177757 ORIGINAL TO 177767 IN AC1 AC2 WAS COM OF AC1
47                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
48                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU11 INTO NOT SUM12
49 01721 121000          MOV 1,0          ;SET UP NEXT TEST
50                       SHIFZ R28,12,13,177767,R,177773
51                  ;THIS IS A R SHIFT TEST OF NOT BIT 12 TO NOT BIT 13
52                ;ASR28:
53 01722 105240          MOVOR 0,1        ;AC0 SHD=177767 COMING INTO TEST
54 01723 110225          COMZR 0,2,SNR    ;AC2 SHD=COM OF 177773
55 01724 063077          HALT
56 01725 150000          COM 2,2          ;AC2 SHD NOW=AC1
57 01726 132000          ADC 1,2          ;THE ADDITION OF COM SHD=-1
58 01727 150004          COM 2,2,SZR      ;AND RESULT SHD=0 ALL SHIFTS OK
59 01730 063077          HALT             ;BIT 12 R TO BIT 13 FAILED
60                  ;AC0=177767 ORIGINAL TO 177773 IN AC1 AC2 WAS COM OF AC1
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0032 N2LOG
01                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
02                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU12 INTO NOT SUM13
03 01731 121000          MOV 1,0          ;SET UP NEXT TEST
04                       SHIFZ R29,13,14,177773,R,177775
05                  ;THIS IS A R SHIFT TEST OF NOT BIT 13 TO NOT BIT 14
06                ;ASR29:
07 01732 105240          MOVOR 0,1        ;AC0 SHD=177773 COMING INTO TEST
08 01733 110225          COMZR 0,2,SNR    ;AC2 SHD=COM OF 177775
09 01734 063077          HALT
10 01735 150000          COM 2,2          ;AC2 SHD NOW=AC1
11 01736 132000          ADC 1,2          ;THE ADDITION OF COM SHD=-1
12 01737 150004          COM 2,2,SZR      ;AND RESULT SHD=0 ALL SHIFTS OK
13 01740 063077          HALT             ;BIT 13 R TO BIT 14 FAILED
14                  ;AC0=177773 ORIGINAL TO 177775 IN AC1 AC2 WAS COM OF AC1
15                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
16                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU13 INTO NOT SUM14
17 01741 121000          MOV 1,0          ;SET UP NEXT TEST
18                       SHIFZ R30,14,15,177775,R,177776
19                  ;THIS IS A R SHIFT TEST OF NOT BIT 14 TO NOT BIT 15
20                ;ASR30:
21 01742 105240          MOVOR 0,1        ;AC0 SHD=177775 COMING INTO TEST
22 01743 110225          COMZR 0,2,SNR    ;AC2 SHD=COM OF 177776
23 01744 063077          HALT
24 01745 150000          COM 2,2          ;AC2 SHD NOW=AC1
25 01746 132000          ADC 1,2          ;THE ADDITION OF COM SHD=-1
26 01747 150004          COM 2,2,SZR      ;AND RESULT SHD=0 ALL SHIFTS OK
27 01750 063077          HALT             ;BIT 14 R TO BIT 15 FAILED
28                  ;AC0=177775 ORIGINAL TO 177776 IN AC1 AC2 WAS COM OF AC1
29                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
30                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU14 INTO NOT SUM15
31 01751 121000          MOV 1,0          ;SET UP NEXT TEST
32
33 01752 105240 ASR31:   MOVOR 0,1        ;TEST 177776 TO -1
34 01753 130004          COM 1,2,SZR      ;ALSO RETEST ABOVE SEQ
35 01754 063077          HALT             ;AN R16 TO R30 MAY HAVE LOST
36 01755 101002          MOV 0,0,SZC
37 01756 063077          HALT             ;CRY SHD=0 FROM LAST MOVOR
38
39                  ;SETUP SERIES OF LEFT SHIFT TESTS SET AC0=177776
40 01757 102000          ADC 0,0          ;AC0=-1
41 01760 101140          COMOL 0,0        ;SHD NOW=+1
42 01761 100000          CUM 0,0
43 01762 104224          COMZR 0,1,SZR
44 01763 063077          HALT             ;LEFT SHIFT SETUP FAILED
45 01764 125003          MOV 1,1,SNC
46 01765 063077          HALT             ;LEFT SHIFT SETUP FAILED
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10033 N2LOG
01                ;LEFT SHIFT SINGLE 0 BIT TESTS
02                        SHIFZ L16,15,14,177776,L,177775
03                  ;THIS IS A L SHIFT TEST OF NOT BIT 15 TO NOT BIT 14
04                ;ASL16:
05 01766 105140           MOVOL 0,1         ;AC0 SHD=177776 COMING INTO TEST
06 01767 110125           COMZL 0,2,SNR     ;AC2 SHD=COM OF 177775
07 01770 063077           HALT
08 01771 150000           COM 2,2           ;AC2 SHD NOW=AC1
09 01772 132000           ADC 1,2           ;THE ADDITION OF COM SHD=-1
10 01773 150004           COM 2,2,SZR       ;AND RESULT SHD=0 ALL SHIFTS OK
11 01774 063077           HALT              ;BIT 15 L TO BIT 14 FAILED
12                  ;AC0=177776 ORIGINAL TO 177775 IN AC1 AC2 WAS COM OF AC1
13                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
14                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU15 INTO NOT SUM14
15 01775 121000           MOV 1,0           ;SET UP NEXT TEST
16                        SHIFZ L17,14,13,177775,L,177773
17                  ;THIS IS A L SHIFT TEST OF NOT BIT 14 TO NOT BIT 13
18                ;ASL17:
19 01776 105140           MOVOL 0,1         ;AC0 SHD=177775 COMING INTO TEST
20 01777 110125           COMZL 0,2,SNR     ;AC2 SHD=COM OF 177773
21 02000 063077           HALT
22 02001 150000           COM 2,2           ;AC2 SHD NOW=AC1
23 02002 132000           ADC 1,2           ;THE ADDITION OF COM SHD=-1
24 02003 150004           COM 2,2,SZR       ;AND RESULT SHD=0 ALL SHIFTS OK
25 02004 063077           HALT              ;BIT 14 L TO BIT 13 FAILED
26                  ;AC0=177775 ORIGINAL TO 177773 IN AC1 AC2 WAS COM OF AC1
27                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
28                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU14 INTO NOT SUM13
29 02005 121000           MOV 1,0           ;SET UP NEXT TEST
30                        SHIFZ L18,13,12,177773,L,177767
31                  ;THIS IS A L SHIFT TEST OF NOT BIT 13 TO NOT BIT 12
32                ;ASL18:
33 02006 105140           MOVOL 0,1         ;AC0 SHD=177773 COMING INTO TEST
34 02007 110125           COMZL 0,2,SNR     ;AC2 SHD=COM OF 177767
35 02010 063077           HALT
36 02011 150000           COM 2,2           ;AC2 SHD NOW=AC1
37 02012 132000           ADC 1,2           ;THE ADDITION OF COM SHD=-1
38 02013 150004           COM 2,2,SZR       ;AND RESULT SHD=0 ALL SHIFTS OK
39 02014 063077           HALT              ;BIT 13 L TO BIT 12 FAILED
40                  ;AC0=177773 ORIGINAL TO 177767 IN AC1 AC2 WAS COM OF AC1
41                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
42                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU13 INTO NOT SUM12
43 02015 121000           MOV 1,0           ;SET UP NEXT TEST
44                        SHIFZ L19,12,11,177767,L,177757
45                  ;THIS IS A L SHIFT TEST OF NOT BIT 12 TO NOT BIT 11
46                ;ASL19:
47 02016 105140           MOVOL 0,1         ;AC0 SHD=177767 COMING INTO TEST
48 02017 110125           COMZL 0,2,SNR     ;AC2 SHD=COM OF 177757
49 02020 063077           HALT
50 02021 150000           COM 2,2           ;AC2 SHD NOW=AC1
51 02022 132000           ADC 1,2           ;THE ADDITION OF COM SHD=-1
52 02023 150004           COM 2,2,SZR       ;AND RESULT SHD=0 ALL SHIFTS OK
53 02024 063077           HALT              ;BIT 12 L TO BIT 11 FAILED
54                  ;AC0=177767 ORIGINAL TO 177757 IN AC1 AC2 WAS COM OF AC1
55                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
56                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU12 INTO NOT SUM11
57 02025 121000           MOV 1,0           ;SET UP NEXT TEST
58                        SHIFZ L20,11,10,177757,L,177737
59                  ;THIS IS A L SHIFT TEST OF NOT BIT 11 TO NOT BIT 10
60                ;ASL20:
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0034 N2LOG
01 02026 105140           MOVOL 0,1         ;AC0 SHD=177757 COMING INTO TEST
02 02027 110125           COMZL 0,2,SNR     ;AC2 SHD=COM OF 177737
03 02030 063077           HALT
04 02031 150000           COM 2,2           ;AC2 SHD NOW=AC1
05 02032 132000           ADC 1,2           ;THE ADDITION OF COM SHD=-1
06 02033 150004           COM 2,2,SZR       ;AND RESULT SHD=0 ALL SHIFTS OK
07 02034 063077           HALT              ;BIT 11 L TO BIT 10 FAILED
08                  ;AC0=177757 ORIGINAL TO 177737 IN AC1 AC2 WAS COM OF AC1
09                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
10                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU11 INTO NOT SUM10
11 02035 121000           MOV 1,0           ;SET UP NEXT TEST
12                        SHIFZ L21,10,09,177737,L,177677
13                  ;THIS IS A L SHIFT TEST OF NOT BIT 10 TO NOT BIT 09
14                ;ASL21:
15 02036 105140           MOVOL 0,1         ;AC0 SHD=177737 COMING INTO TEST
16 02037 110125           COMZL 0,2,SNR     ;AC2 SHD=COM OF 177677
17 02040 063077           HALT
18 02041 150000           COM 2,2           ;AC2 SHD NOW=AC1
19 02042 132000           ADC 1,2           ;THE ADDITION OF COM SHD=-1
20 02043 150004           COM 2,2,SZR       ;AND RESULT SHD=0 ALL SHIFTS OK
21 02044 063077           HALT              ;BIT 10 L TO BIT 09 FAILED
22                  ;AC0=177737 ORIGINAL TO 177677 IN AC1 AC2 WAS COM OF AC1
23                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
24                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU10 INTO NOT SUM09
25 02045 121000           MOV 1,0           ;SET UP NEXT TEST
26                        SHIFZ L22,09,08,177677,L,177577
27                  ;THIS IS A L SHIFT TEST OF NOT BIT 09 TO NOT BIT 08
28                ;ASL22:
29 02046 105140           MOVOL 0,1         ;AC0 SHD=177677 COMING INTO TEST
30 02047 110125           COMZL 0,2,SNR     ;AC2 SHD=COM OF 177577
31 02050 063077           HALT
32 02051 150000           COM 2,2           ;AC2 SHD NOW=AC1
33 02052 132000           ADC 1,2           ;THE ADDITION OF COM SHD=-1
34 02053 150004           COM 2,2,SZR       ;AND RESULT SHD=0 ALL SHIFTS OK
35 02054 063077           HALT              ;BIT 09 L TO BIT 08 FAILED
36                  ;AC0=177677 ORIGINAL TO 177577 IN AC1 AC2 WAS COM OF AC1
37                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
38                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU09 INTO NOT SUM08
39 02055 121000           MOV 1,0           ;SET UP NEXT TEST
40                        SHIFZ L23,08,07,177577,L,177377
41                  ;THIS IS A L SHIFT TEST OF NOT BIT 08 TO NOT BIT 07
42                ;ASL23:
43 02056 105140           MOVOL 0,1         ;AC0 SHD=177577 COMING INTO TEST
44 02057 110125           COMZL 0,2,SNR     ;AC2 SHD=COM OF 177377
45 02060 063077           HALT
46 02061 150000           COM 2,2           ;AC2 SHD NOW=AC1
47 02062 132000           ADC 1,2           ;THE ADDITION OF COM SHD=-1
48 02063 150004           COM 2,2,SZR       ;AND RESULT SHD=0 ALL SHIFTS OK
49 02064 063077           HALT              ;BIT 08 L TO BIT 07 FAILED
50                  ;AC0=177577 ORIGINAL TO 177377 IN AC1 AC2 WAS COM OF AC1
51                  ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
52                  ;WAS PREVIOUSLY VERIFIED SEE NOT ALU08 INTO NOT SUM07
53 02065 121000           MOV 1,0           ;SET UP NEXT TEST
54                        SHIFZ L24,07,06,177377,L,176777
55                  ;THIS IS A L SHIFT TEST OF NOT BIT 07 TO NOT BIT 06
56                ;ASL24:
57 02066 105140           MOVOL 0,1         ;AC0 SHD=177377 COMING INTO TEST
58 02067 110125           COMZL 0,2,SNR     ;AC2 SHD=COM OF 176777
59 02070 063077           HALT
60 02071 150000           COM 2,2           ;AC2 SHD NOW=AC1
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0035 N2LOG
01 02072 132000          ADC 1,2          ;THE ADDITION OF COM SHD=-1
02 02073 150004          COM 2,2,SZR      ;AND RESULT SHD=0 ALL SHIFTS OK
03 02074 063077          HALT             ;BIT 07 L TO BIT 06 FAILED
04                    ;AC0=177377 ORIGINAL TO 176777 IN AC1 AC2 WAS COM OF AC1
05                    ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
06                    ;WAS PREVIOUSLY VERIFIED SEE NOT ALU07 INTO NOT SUM06
07 02075 121000          MOV 1,0          ;SET UP NEXT TEST
08                       SHIFZ L25,06,05,176777,L,175777
09                    ;THIS IS A L SHIFT TEST OF NOT BIT 06 TO NOT BIT 05
10                 ;ASL25:
11 02076 105140          MOVOL 0,1        ;AC0 SHD=176777 COMING INTO TEST
12 02077 110125          COMZL 0,2,SNR    ;AC2 SHD=COM OF 175777
13 02100 063077          HALT
14 02101 150000          COM 2,2          ;AC2 SHD NOW=AC1
15 02102 132000          ADC 1,2          ;THE ADDITION OF COM SHD=-1
16 02103 150004          COM 2,2,SZR      ;AND RESULT SHD=0 ALL SHIFTS OK
17 02104 063077          HALT             ;BIT 06 L TO BIT 05 FAILED
18                    ;AC0=176777 ORIGINAL TO 175777 IN AC1 AC2 WAS COM OF AC1
19                    ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
20                    ;WAS PREVIOUSLY VERIFIED SEE NOT ALU06 INTO NOT SUM05
21 02105 121000          MOV 1,0          ;SET UP NEXT TEST
22                       SHIFZ L26,05,04,175777,L,173777
23                    ;THIS IS A L SHIFT TEST OF NOT BIT 05 TO NOT BIT 04
24                 ;ASL26:
25 02106 105140          MOVOL 0,1        ;AC0 SHD=175777 COMING INTO TEST
26 02107 110125          COMZL 0,2,SNR    ;AC2 SHD=COM OF 173777
27 02110 063077          HALT
28 02111 150000          COM 2,2          ;AC2 SHD NOW=AC1
29 02112 132000          ADC 1,2          ;THE ADDITION OF COM SHD=-1
30 02113 150004          COM 2,2,SZR      ;AND RESULT SHD=0 ALL SHIFTS OK
31 02114 063077          HALT             ;BIT 05 L TO BIT 04 FAILED
32                    ;AC0=175777 ORIGINAL TO 173777 IN AC1 AC2 WAS COM OF AC1
33                    ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
34                    ;WAS PREVIOUSLY VERIFIED SEE NOT ALU05 INTO NOT SUM04
35 02115 121000          MOV 1,0          ;SET UP NEXT TEST
36                       SHIFZ L27,04,03,173777,L,167777
37                    ;THIS IS A L SHIFT TEST OF NOT BIT 04 TO NOT BIT 03
38                 ;ASL27:
39 02116 105140          MOVOL 0,1        ;AC0 SHD=173777 COMING INTO TEST
40 02117 110125          COMZL 0,2,SNR    ;AC2 SHD=COM OF 167777
41 02120 063077          HALT
42 02121 150000          COM 2,2          ;AC2 SHD NOW=AC1
43 02122 132000          ADC 1,2          ;THE ADDITION OF COM SHD=-1
44 02123 150004          COM 2,2,SZR      ;AND RESULT SHD=0 ALL SHIFTS OK
45 02124 063077          HALT             ;BIT 04 L TO BIT 03 FAILED
46                    ;AC0=173777 ORIGINAL TO 167777 IN AC1 AC2 WAS COM OF AC1
47                    ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
48                    ;WAS PREVIOUSLY VERIFIED SEE NOT ALU04 INTO NOT SUM03
49 02125 121000          MOV 1,0          ;SET UP NEXT TEST
50                       SHIFZ L28,03,02,167777,L,157777
51                    ;THIS IS A L SHIFT TEST OF NOT BIT 03 TO NOT BIT 02
52                 ;ASL28:
53 02126 105140          MOVOL 0,1        ;AC0 SHD=167777 COMING INTO TEST
54 02127 110125          COMZL 0,2,SNR    ;AC2 SHD=COM OF 157777
55 02130 063077          HALT
56 02131 150000          COM 2,2          ;AC2 SHD NOW=AC1
57 02132 132000          ADC 1,2          ;THE ADDITION OF COM SHD=-1
58 02133 150004          COM 2,2,SZR      ;AND RESULT SHD=0 ALL SHIFTS OK
59 02134 063077          HALT             ;BIT 03 L TO BIT 02 FAILED
60                    ;AC0=167777 ORIGINAL TO 157777 IN AC1 AC2 WAS COM OF AC1
```

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0036 N2LOG
01                    ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
02                    ;WAS PREVIOUSLY VERIFIED SEE NOT ALU03 INTO NOT SUM02
03 02135 121000          MOV 1,0          ;SET UP NEXT TEST
04                       SHIFZ L29,02,01,157777,L,137777
05                    ;THIS IS A L SHIFT TEST OF NOT BIT 02 TO NOT BIT 01
06                 ;ASL29:
07 02136 105140          MOVOL 0,1        ;AC0 SHD=157777 COMING INTO TEST
08 02137 110125          COMZL 0,2,SNR    ;AC2 SHD=COM OF 137777
09 02140 063077          HALT
10 02141 150000          COM 2,2          ;AC2 SHD NOW=AC1
11 02142 132000          ADC 1,2          ;THE ADDITION OF COM SHD=-1
12 02143 150004          COM 2,2,SZR      ;AND RESULT SHD=0 ALL SHIFTS OK
13 02144 063077          HALT             ;BIT 02 L TO BIT 01 FAILED
14                    ;AC0=157777 ORIGINAL TO 137777 IN AC1 AC2 WAS COM OF AC1
15                    ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
16                    ;WAS PREVIOUSLY VERIFIED SEE NOT ALU02 INTO NOT SUM01
17 02145 121000          MOV 1,0          ;SET UP NEXT TEST
18                       SHIFZ L30,01,00,137777,L,077777
19                    ;THIS IS A L SHIFT TEST OF NOT BIT 01 TO NOT BIT 00
20                 ;ASL30:
21 02146 105140          MOVOL 0,1        ;AC0 SHD=137777 COMING INTO TEST
22 02147 110125          COMZL 0,2,SNR    ;AC2 SHD=COM OF 077777
23 02150 063077          HALT
24 02151 150000          COM 2,2          ;AC2 SHD NOW=AC1
25 02152 132000          ADC 1,2          ;THE ADDITION OF COM SHD=-1
26 02153 150004          COM 2,2,SZR      ;AND RESULT SHD=0 ALL SHIFTS OK
27 02154 063077          HALT             ;BIT 01 L TO BIT 00 FAILED
28                    ;AC0=137777 ORIGINAL TO 077777 IN AC1 AC2 WAS COM OF AC1
29                    ;PROBABILITY OF SHIFT FAILURE TO AC2 IS LOW AS ONES SHIFT
30                    ;WAS PREVIOUSLY VERIFIED SEE NOT ALU01 INTO NOT SUM00
31 02155 121000          MOV 1,0          ;SET UP NEXT TEST
32                    ;IF AC0 DOES NOT=077777 HERE SOME L16 TO L30 FAILED
33 02156 105140 ASL31:   MOVOL 0,1        ;SHD RESULT IN AC1=-1
34 02157 130004          COM 1,2,SZR      ;TEST FOR AC2 RESULT=0
35 02160 063077          HALT             ;COULD HAVE FAILED L16 TO L30
36 02161 151002          MOV 2,2,SZC      ;CRY SHD=0 FROM BIT 0
37 02162 063077          HALT             ;BIT 0 TO CRY FAILED
38
39
40
```

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10037 N2LOG
01
02                ;SINGLE BIT ADD WITHOUT CARRY TESTS
03                ;DEFINE MACRO ENCOMPASSING SOURCE OR DEST=NON ZERO
04
05                      .MACRO ADDT1
06                ;TEST ADD INSTRUCTION NO CARRY WHEN A1 IS NON ZERO
07                ;A2 IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
08                ;AC0=A3 COMING INTO THE TEST
09              ;ANCA7:
10                      MOV 0,A4          ;SET UP A1 ACA4
11                      ADC A5,A5
12                      COM A5,A5         ;SET ACA5 A2=0
13                      ADD 1,2           ;PERFORM ADD WITH NO CARRIES
14                      MOV 2,3           ;THE A1 AC WAS NON ZERO
15                      ADC 0,3           ;AC3 SHD NOW=-1
16                      COM 3,3,SZR       ;WITH COM=0
17                      HALT              ;ADD WITHOUT CARRY FAILED
18                      MOVZL 0,0         ;SET UP NEXT TEST
19                ;AC2 SHD=A3 AS A RESULT OF ABOVE TEST
20                %
21                ;TEST ADD OF ALL 0'S TO GENERATE NO CARRIES
22 02163 102000 ANC00:  ADC 0,0
23 02164 100000         COM 0,0           ;SETS AC0=0
24 02165 103004         ADD 0,0,SZR       ;RESULT OF ADD SHD STILL=0
25 02166 063077         HALT              ;ADD 0+0 GENERATED A CARRY
26 02167 101002         MOV 0,0,SZC       ;ABOVE ADD SHD LVE CRY=0
27 02170 063077         HALT              ;INTO CRY SEE CARRY OUT
28
29                ;SET UP AC0 TO=+1 FOR FIRST TEST
30 02171 102000         ADC 0,0
31 02172 100145         COMOL 0,0,SNR
32 02173 063077         HALT              ;SETUP FAILED
```

```
10038 N2LOG
01
02                      ADDT1 SRC,DEST,1,1,2,Z,A1
03                ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
04                ;DEST IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
05                ;AC0=1 COMING INTO THE TEST
06              ;ANC01:
07 02174 105000         MOV 0,1 ;SET UP SRC AC1
08 02175 152000         ADC 2,2
09 02176 150000         COM 2,2 ;SET AC2 DEST=0
10 02177 133000         ADD 1,2           ;PERFORM ADD WITH NO CARRIES
11 02200 155000         MOV 2,3           ;THE SRC AC WAS NON ZERO
12 02201 116000         ADC 0,3           ;AC3 SHD NOW=-1
13 02202 174004         COM 3,3,SZR       ;WITH COM=0
14 02203 063077         HALT              ;ADD WITHOUT CARRY FAILED
15 02204 101120         MOVZL 0,0         ;SET UP NEXT TEST
16                ;AC2 SHD=1 AS A RESULT OF ABOVE TEST
17                      ADDT1 SRC,DEST,2,1,2,Z,02
18                ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
19                ;DEST IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
20                ;AC0=2 COMING INTO THE TEST
21              ;ANC02:
22 02205 105000         MOV 0,1 ;SET UP SRC AC1
23 02206 152000         ADC 2,2
24 02207 150000         COM 2,2 ;SET AC2 DEST=0
25 02210 133000         ADD 1,2           ;PERFORM ADD WITH NO CARRIES
26 02211 155000         MOV 2,3           ;THE SRC AC WAS NON ZERO
27 02212 116000         ADC 0,3           ;AC3 SHD NOW=-1
28 02213 174004         COM 3,3,SZR       ;WITH COM=0
29 02214 063077         HALT              ;ADD WITHOUT CARRY FAILED
30 02215 101120         MOVZL 0,0         ;SET UP NEXT TEST
31                ;AC2 SHD=2 AS A RESULT OF ABOVE TEST
32                      ADDT1 SRC,DEST,4,1,2,Z,03
33                ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
34                ;DEST IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
35                ;AC0=4 COMING INTO THE TEST
36              ;ANC03:
37 02216 105000         MOV 0,1 ;SET UP SRC AC1
38 02217 152000         ADC 2,2
39 02220 150000         COM 2,2 ;SET AC2 DEST=0
40 02221 133000         ADD 1,2           ;PERFORM ADD WITH NO CARRIES
41 02222 155000         MOV 2,3           ;THE SRC AC WAS NON ZERO
42 02223 116000         ADC 0,3           ;AC3 SHD NOW=-1
43 02224 174004         COM 3,3,SZR       ;WITH COM=0
44 02225 063077         HALT              ;ADD WITHOUT CARRY FAILED
45 02226 101120         MOVZL 0,0         ;SET UP NEXT TEST
46                ;AC2 SHD=4 AS A RESULT OF ABOVE TEST
47                      ADDT1 SRC,DEST,10,1,2,Z,04
48                ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
49                ;DEST IS EQUAL TO 0=RESULT SHD BE SAME AS MOVE
50                ;AC0=10 COMING INTO THE TEST
51              ;ANC04:
52 02227 105000         MOV 0,1 ;SET UP SRC AC1
53 02230 152000         ADC 2,2
54 02231 150000         COM 2,2 ;SET AC2 DEST=0
55 02232 133000         ADD 1,2           ;PERFORM ADD WITH NO CARRIES
56 02233 155000         MOV 2,3           ;THE SRC AC WAS NON ZERO
57 02234 116000         ADC 0,3           ;AC3 SHD NOW=-1
58 02235 174004         COM 3,3,SZR       ;WITH COM=0
59 02236 063077         HALT              ;ADD WITHOUT CARRY FAILED
60 02237 101120         MOVZL 0,0         ;SET UP NEXT TEST
```

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0039 N2LOG
01                ;AC2 SHD=10 AS A RESULT OF ABOVE TEST
02                      ADDT1 SRC,DEST,20,1,2,Z,05
03                ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
04                ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
05                ;AC0=20 COMING INTO THE TEST
06              ;ANC05:
07 02240 105000         MOV 0,1 ;SET UP SRC AC1
08 02241 152000         ADC 2,2
09 02242 150000         COM 2,2 ;SET AC2 DEST=0
10 02243 133000         ADD 1,2          ;PERFORM ADD WITH NO CARRIES
11 02244 155000         MOV 2,3          ;THE SRC AC WAS NON ZERO
12 02245 116000         ADC 0,3          ;AC3 SHD NOW=-1
13 02246 174004         COM 3,3,SZR      ;WITH COM=0
14 02247 063077         HALT             ;ADD WITHOUT CARRY FAILED
15 02250 101120         MOVZL 0,0        ;SET UP NEXT TEST
16                ;AC2 SHD=20 AS A RESULT OF ABOVE TEST
17                      ADDT1 SRC,DEST,40,1,2,Z,06
18                ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
19                ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
20                ;AC0=40 COMING INTO THE TEST
21              ;ANC06:
22 02251 105000         MOV 0,1 ;SET UP SRC AC1
23 02252 152000         ADC 2,2
24 02253 150000         COM 2,2 ;SET AC2 DEST=0
25 02254 133000         ADD 1,2          ;PERFORM ADD WITH NO CARRIES
26 02255 155000         MOV 2,3          ;THE SRC AC WAS NON ZERO
27 02256 116000         ADC 0,3          ;AC3 SHD NOW=-1
28 02257 174004         COM 3,3,SZR      ;WITH COM=0
29 02260 063077         HALT             ;ADD WITHOUT CARRY FAILED
30 02261 101120         MOVZL 0,0        ;SET UP NEXT TEST
31                ;AC2 SHD=40 AS A RESULT OF ABOVE TEST
32                      ADDT1 SRC,DEST,100,1,2,Z,07
33                ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
34                ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
35                ;AC0=100 COMING INTO THE TEST
36              ;ANC07:
37 02262 105000         MOV 0,1 ;SET UP SRC AC1
38 02263 152000         ADC 2,2
39 02264 150000         COM 2,2 ;SET AC2 DEST=0
40 02265 133000         ADD 1,2          ;PERFORM ADD WITH NO CARRIES
41 02266 155000         MOV 2,3          ;THE SRC AC WAS NON ZERO
42 02267 116000         ADC 0,3          ;AC3 SHD NOW=-1
43 02270 174004         COM 3,3,SZR      ;WITH COM=0
44 02271 063077         HALT             ;ADD WITHOUT CARRY FAILED
45 02272 101120         MOVZL 0,0        ;SET UP NEXT TEST
46                ;AC2 SHD=100 AS A RESULT OF ABOVE TEST
47                      ADDT1 SRC,DEST,200,1,2,Z,08
48                ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
49                ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
50                ;AC0=200 COMING INTO THE TEST
51              ;ANC08:
52 02273 105000         MOV 0,1 ;SET UP SRC AC1
53 02274 152000         ADC 2,2
54 02275 150000         COM 2,2 ;SET AC2 DEST=0
55 02276 133000         ADD 1,2          ;PERFORM ADD WITH NO CARRIES
56 02277 155000         MOV 2,3          ;THE SRC AC WAS NON ZERO
57 02300 116000         ADC 0,3          ;AC3 SHD NOW=-1
58 02301 174004         COM 3,3,SZR      ;WITH COM=0
59 02302 063077         HALT             ;ADD WITHOUT CARRY FAILED
60 02303 101120         MOVZL 0,0        ;SET UP NEXT TEST
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0040 N2LOG
01                ;AC2 SHD=200 AS A RESULT OF ABOVE TEST
02                      ADDT1 SRC,DEST,400,1,2,Z,09
03                ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
04                ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
05                ;AC0=400 COMING INTO THE TEST
06              ;ANC09:
07 02304 105000         MOV 0,1 ;SET UP SRC AC1
08 02305 152000         ADC 2,2
09 02306 150000         COM 2,2 ;SET AC2 DEST=0
10 02307 133000         ADD 1,2          ;PERFORM ADD WITH NO CARRIES
11 02310 155000         MOV 2,3          ;THE SRC AC WAS NON ZERO
12 02311 116000         ADC 0,3          ;AC3 SHD NOW=-1
13 02312 174004         COM 3,3,SZR      ;WITH COM=0
14 02313 063077         HALT             ;ADD WITHOUT CARRY FAILED
15 02314 101120         MOVZL 0,0        ;SET UP NEXT TEST
16                ;AC2 SHD=400 AS A RESULT OF ABOVE TEST
17                      ADDT1 SRC,DEST,1000,1,2,Z,10
18                ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
19                ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
20                ;AC0=1000 COMING INTO THE TEST
21              ;ANC10:
22 02315 105000         MOV 0,1 ;SET UP SRC AC1
23 02316 152000         ADC 2,2
24 02317 150000         COM 2,2 ;SET AC2 DEST=0
25 02320 133000         ADD 1,2          ;PERFORM ADD WITH NO CARRIES
26 02321 155000         MOV 2,3          ;THE SRC AC WAS NON ZERO
27 02322 116000         ADC 0,3          ;AC3 SHD NOW=-1
28 02323 174004         COM 3,3,SZR      ;WITH COM=0
29 02324 063077         HALT             ;ADD WITHOUT CARRY FAILED
30 02325 101120         MOVZL 0,0        ;SET UP NEXT TEST
31                ;AC2 SHD=1000 AS A RESULT OF ABOVE TEST
32                      ADDT1 SRC,DEST,2000,1,2,Z,11
33                ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
34                ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
35                ;AC0=2000 COMING INTO THE TEST
36              ;ANC11:
37 02326 105000         MOV 0,1 ;SET UP SRC AC1
38 02327 152000         ADC 2,2
39 02330 150000         COM 2,2 ;SET AC2 DEST=0
40 02331 133000         ADD 1,2          ;PERFORM ADD WITH NO CARRIES
41 02332 155000         MOV 2,3          ;THE SRC AC WAS NON ZERO
42 02333 116000         ADC 0,3          ;AC3 SHD NOW=-1
43 02334 174004         COM 3,3,SZR      ;WITH COM=0
44 02335 063077         HALT             ;ADD WITHOUT CARRY FAILED
45 02336 101120         MOVZL 0,0        ;SET UP NEXT TEST
46                ;AC2 SHD=2000 AS A RESULT OF ABOVE TEST
47                      ADDT1 SRC,DEST,4000,1,2,Z,12
48                ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
49                ;DEST IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
50                ;AC0=4000 COMING INTO THE TEST
51              ;ANC12:
52 02337 105000         MOV 0,1 ;SET UP SRC AC1
53 02340 152000         ADC 2,2
54 02341 150000         COM 2,2 ;SET AC2 DEST=0
55 02342 133000         ADD 1,2          ;PERFORM ADD WITH NO CARRIES
56 02343 155000         MOV 2,3          ;THE SRC AC WAS NON ZERO
57 02344 116000         ADC 0,3          ;AC3 SHD NOW=-1
58 02345 174004         COM 3,3,SZR      ;WITH COM=0
59 02346 063077         HALT             ;ADD WITHOUT CARRY FAILED
60 02347 101120         MOVZL 0,0        ;SET UP NEXT TEST
```

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0041 N2LOG
01                      ;AC2 SHO=4000 AS A RESULT OF ABOVE TEST
02                          ADDT1 SRC,DEST,10000,1,2,Z,13
03                      ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
04                      ;DEST IS EQUAL TO 0-RESULT SHO BE SAME AS MOVE
05                      ;AC0=10000 COMING INTO THE TEST
06                    ;ANC13:
07 02350 105000             MOV 0,1 ;SET UP SRC AC1
08 02351 152000             ADC 2,2
09 02352 150000             COM 2,2 ;SET AC2 DEST=0
10 02353 133000             ADD 1,2         ;PERFORM ADD WITH NO CARRIES
11 02354 155000             MOV 2,3         ;THE SRC AC WAS NON ZERO
12 02355 116000             ADC 0,3         ;AC3 SHO NOW=-1
13 02356 174004             COM 3,3,SZR     ;WITH COM=0
14 02357 063077             HALT            ;ADD WITHOUT CARRY FAILED
15 02360 101120             MOVZL 0,0       ;SET UP NEXT TEST
16                      ;AC2 SHO=10000 AS A RESULT OF ABOVE TEST
17                          ADDT1 SRC,DEST,20000,1,2,Z,14
18                      ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
19                      ;DEST IS EQUAL TO 0-RESULT SHO BE SAME AS MOVE
20                      ;AC0=20000 COMING INTO THE TEST
21                    ;ANC14:
22 02361 105000             MOV 0,1 ;SET UP SRC AC1
23 02362 152000             ADC 2,2
24 02363 150000             COM 2,2 ;SET AC2 DEST=0
25 02364 133000             ADD 1,2         ;PERFORM ADD WITH NO CARRIES
26 02365 155000             MOV 2,3         ;THE SRC AC WAS NON ZERO
27 02366 116000             ADC 0,3         ;AC3 SHO NOW=-1
28 02367 174004             COM 3,3,SZR     ;WITH COM=0
29 02370 063077             HALT            ;ADD WITHOUT CARRY FAILED
30 02371 101120             MOVZL 0,0       ;SET UP NEXT TEST
31                      ;AC2 SHO=20000 AS A RESULT OF ABOVE TEST
32                          ADDT1 SRC,DEST,40000,1,2,Z,15
33                      ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
34                      ;DEST IS EQUAL TO 0-RESULT SHO BE SAME AS MOVE
35                      ;AC0=40000 COMING INTO THE TEST
36                    ;ANC15:
37 02372 105000             MOV 0,1 ;SET UP SRC AC1
38 02373 152000             ADC 2,2
39 02374 150000             COM 2,2 ;SET AC2 DEST=0
40 02375 133000             ADD 1,2         ;PERFORM ADD WITH NO CARRIES
41 02376 155000             MOV 2,3         ;THE SRC AC WAS NON ZERO
42 02377 116000             ADC 0,3         ;AC3 SHO NOW=-1
43 02400 174004             COM 3,3,SZR     ;WITH COM=0
44 02401 063077             HALT            ;ADD WITHOUT CARRY FAILED
45 02402 101120             MOVZL 0,0       ;SET UP NEXT TEST
46                      ;AC2 SHO=40000 AS A RESULT OF ABOVE TEST
47                          ADDT1 SRC,DEST,100000,1,2,Z,16
48                      ;TEST ADD INSTRUCTION NO CARRY WHEN SRC IS NON ZERO
49                      ;DEST IS EQUAL TO 0-RESULT SHO BE SAME AS MOVE
50                      ;AC0=100000 COMING INTO THE TEST
51                    ;ANC16:
52 02403 105000             MOV 0,1 ;SET UP SRC AC1
53 02404 152000             ADC 2,2
54 02405 150000             COM 2,2 ;SET AC2 DEST=0
55 02406 133000             ADD 1,2         ;PERFORM ADD WITH NO CARRIES
56 02407 155000             MOV 2,3         ;THE SRC AC WAS NON ZERO
57 02410 116000             ADC 0,3         ;AC3 SHO NOW=-1
58 02411 174004             COM 3,3,SZR     ;WITH COM=0
59 02412 063077             HALT            ;ADD WITHOUT CARRY FAILED
60 02413 101120             MOVZL 0,0       ;SET UP NEXT TEST
```

```
0042 N2LOG
01                      ;AC2 SHO=100000 AS A RESULT OF ABOVE TEST
02
03                      ;RESET UP AC0 FOR DEST NOT=0 ADD TEST
04 02414 102000             ADC 0,0
05 02415 100145             COMOL 0,0,SNR
06 02416 063077             HALT
07
08                          ADDT1 DEST,SRC,1,2,1,Z,17
09                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
10                      ;SRC IS EQUAL TO 0-RESULT SHO BE SAME AS MOVE
11                      ;AC0=1 COMING INTO THE TEST
12                    ;ANC17:
13 02417 111000             MOV 0,2 ;SET UP DEST AC2
14 02420 126000             ADC 1,1
15 02421 124000             COM 1,1 ;SET AC1 SRC=0
16 02422 133000             ADD 1,2         ;PERFORM ADD WITH NO CARRIES
17 02423 155000             MOV 2,3         ;THE DEST AC WAS NON ZERO
18 02424 116000             ADC 0,3         ;AC3 SHO NOW=-1
19 02425 174004             COM 3,3,SZR     ;WITH COM=0
20 02426 063077             HALT            ;ADD WITHOUT CARRY FAILED
21 02427 101120             MOVZL 0,0       ;SET UP NEXT TEST
22                      ;AC2 SHO=1 AS A RESULT OF ABOVE TEST
23                          ADDT1 DEST,SRC,2,2,1,Z,18
24                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
25                      ;SRC IS EQUAL TO 0-RESULT SHO BE SAME AS MOVE
26                      ;AC0=2 COMING INTO THE TEST
27                    ;ANC18:
28 02430 111000             MOV 0,2 ;SET UP DEST AC2
29 02431 126000             ADC 1,1
30 02432 124000             COM 1,1 ;SET AC1 SRC=0
31 02433 133000             ADD 1,2         ;PERFORM ADD WITH NO CARRIES
32 02434 155000             MOV 2,3         ;THE DEST AC WAS NON ZERO
33 02435 116000             ADC 0,3         ;AC3 SHO NOW=-1
34 02436 174004             COM 3,3,SZR     ;WITH COM=0
35 02437 063077             HALT            ;ADD WITHOUT CARRY FAILED
36 02440 101120             MOVZL 0,0       ;SET UP NEXT TEST
37                      ;AC2 SHO=2 AS A RESULT OF ABOVE TEST
38                          ADDT1 DEST,SRC,4,2,1,Z,19
39                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
40                      ;SRC IS EQUAL TO 0-RESULT SHO BE SAME AS MOVE
41                      ;AC0=4 COMING INTO THE TEST
42                    ;ANC19:
43 02441 111000             MOV 0,2 ;SET UP DEST AC2
44 02442 126000             ADC 1,1
45 02443 124000             COM 1,1 ;SET AC1 SRC=0
46 02444 133000             ADD 1,2         ;PERFORM ADD WITH NO CARRIES
47 02445 155000             MOV 2,3         ;THE DEST AC WAS NON ZERO
48 02446 116000             ADC 0,3         ;AC3 SHO NOW=-1
49 02447 174004             COM 3,3,SZR     ;WITH COM=0
50 02450 063077             HALT            ;ADD WITHOUT CARRY FAILED
51 02451 101120             MOVZL 0,0       ;SET UP NEXT TEST
52                      ;AC2 SHO=4 AS A RESULT OF ABOVE TEST
53                          ADDT1 DEST,SRC,10,2,1,Z,20
54                      ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
55                      ;SRC IS EQUAL TO 0-RESULT SHO BE SAME AS MOVE
56                      ;AC0=10 COMING INTO THE TEST
57                    ;ANC20:
58 02452 111000             MOV 0,2 ;SET UP DEST AC2
59 02453 126000             ADC 1,1
60 02454 124000             COM 1,1 ;SET AC1 SRC=0
```

```
 0043 N2LOG
01 02455 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
02 02456 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
03 02457 116000          ADC 0,3          ;AC3 SHD NOW=-1
04 02460 174004          COM 3,3,SZR      ;WITH COM=0
05 02461 063077          HALT             ;ADD WITHOUT CARRY FAILED
06 02462 101120          MOVZL 0,0        ;SET UP NEXT TEST
07                  ;AC2 SHD=10 AS A RESULT OF ABOVE TEST
08                       ADDT1 DEST,SRC,20,2,1,Z,21
09                  ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
10                  ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
11                  ;AC0=20 COMING INTO THE TEST
12                 ;ANC21:
13 02463 111000          MOV 0,2 ;SET UP DEST AC2
14 02464 126000          ADC 1,1
15 02465 124000          COM 1,1 ;SET AC1 SRC=0
16 02466 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
17 02467 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
18 02470 116000          ADC 0,3          ;AC3 SHD NOW=-1
19 02471 174004          COM 3,3,SZR      ;WITH COM=0
20 02472 063077          HALT             ;ADD WITHOUT CARRY FAILED
21 02473 101120          MOVZL 0,0        ;SET UP NEXT TEST
22                  ;AC2 SHD=20 AS A RESULT OF ABOVE TEST
23                       ADDT1 DEST,SRC,40,2,1,Z,22
24                  ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
25                  ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
26                  ;AC0=40 COMING INTO THE TEST
27                 ;ANC22:
28 02474 111000          MOV 0,2 ;SET UP DEST AC2
29 02475 126000          ADC 1,1
30 02476 124000          COM 1,1 ;SET AC1 SRC=0
31 02477 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
32 02500 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
33 02501 116000          ADC 0,3          ;AC3 SHD NOW=-1
34 02502 174004          COM 3,3,SZR      ;WITH COM=0
35 02503 063077          HALT             ;ADD WITHOUT CARRY FAILED
36 02504 101120          MOVZL 0,0        ;SET UP NEXT TEST
37                  ;AC2 SHD=40 AS A RESULT OF ABOVE TEST
38                       ADDT1 DEST,SRC,100,2,1,Z,23
39                  ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
40                  ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
41                  ;AC0=100 COMING INTO THE TEST
42                 ;ANC23:
43 02505 111000          MOV 0,2 ;SET UP DEST AC2
44 02506 126000          ADC 1,1
45 02507 124000          COM 1,1 ;SET AC1 SRC=0
46 02510 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
47 02511 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
48 02512 116000          ADC 0,3          ;AC3 SHD NOW=-1
49 02513 174004          COM 3,3,SZR      ;WITH COM=0
50 02514 063077          HALT             ;ADD WITHOUT CARRY FAILED
51 02515 101120          MOVZL 0,0        ;SET UP NEXT TEST
52                  ;AC2 SHD=100 AS A RESULT OF ABOVE TEST
53                       ADDT1 DEST,SRC,200,2,1,Z,24
54                  ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
55                  ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
56                  ;AC0=200 COMING INTO THE TEST
57                 ;ANC24:
58 02516 111000          MOV 0,2 ;SET UP DEST AC2
59 02517 126000          ADC 1,1
60 02520 124000          COM 1,1 ;SET AC1 SRC=0
```

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 0044 N2LOG
01 02521 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
02 02522 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
03 02523 116000          ADC 0,3          ;AC3 SHD NOW=-1
04 02524 174004          COM 3,3,SZR      ;WITH COM=0
05 02525 063077          HALT             ;ADD WITHOUT CARRY FAILED
06 02526 101120          MOVZL 0,0        ;SET UP NEXT TEST
07                  ;AC2 SHD=200 AS A RESULT OF ABOVE TEST
08                       ADDT1 DEST,SRC,400,2,1,Z,25
09                  ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
10                  ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
11                  ;AC0=400 COMING INTO THE TEST
12                 ;ANC25:
13 02527 111000          MOV 0,2 ;SET UP DEST AC2
14 02530 126000          ADC 1,1
15 02531 124000          COM 1,1 ;SET AC1 SRC=0
16 02532 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
17 02533 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
18 02534 116000          ADC 0,3          ;AC3 SHD NOW=-1
19 02535 174004          COM 3,3,SZR      ;WITH COM=0
20 02536 063077          HALT             ;ADD WITHOUT CARRY FAILED
21 02537 101120          MOVZL 0,0        ;SET UP NEXT TEST
22                  ;AC2 SHD=400 AS A RESULT OF ABOVE TEST
23                       ADDT1 DEST,SRC,1000,2,1,Z,26
24                  ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
25                  ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
26                  ;AC0=1000 COMING INTO THE TEST
27                 ;ANC26:
28 02540 111000          MOV 0,2 ;SET UP DEST AC2
29 02541 126000          ADC 1,1
30 02542 124000          COM 1,1 ;SET AC1 SRC=0
31 02543 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
32 02544 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
33 02545 116000          ADC 0,3          ;AC3 SHD NOW=-1
34 02546 174004          COM 3,3,SZR      ;WITH COM=0
35 02547 063077          HALT             ;ADD WITHOUT CARRY FAILED
36 02550 101120          MOVZL 0,0        ;SET UP NEXT TEST
37                  ;AC2 SHD=1000 AS A RESULT OF ABOVE TEST
38                       ADDT1 DEST,SRC,2000,2,1,Z,27
39                  ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
40                  ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
41                  ;AC0=2000 COMING INTO THE TEST
42                 ;ANC27:
43 02551 111000          MOV 0,2 ;SET UP DEST AC2
44 02552 126000          ADC 1,1
45 02553 124000          COM 1,1 ;SET AC1 SRC=0
46 02554 133000          ADD 1,2          ;PERFORM ADD WITH NO CARRIES
47 02555 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
48 02556 116000          ADC 0,3          ;AC3 SHD NOW=-1
49 02557 174004          COM 3,3,SZR      ;WITH COM=0
50 02560 063077          HALT             ;ADD WITHOUT CARRY FAILED
51 02561 101120          MOVZL 0,0        ;SET UP NEXT TEST
52                  ;AC2 SHD=2000 AS A RESULT OF ABOVE TEST
53                       ADDT1 DEST,SRC,4000,2,1,Z,28
54                  ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
55                  ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
56                  ;AC0=4000 COMING INTO THE TEST
57                 ;ANC28:
58 02562 111000          MOV 0,2 ;SET UP DEST AC2
59 02563 126000          ADC 1,1
60 02564 124000          COM 1,1 ;SET AC1 SRC=0
```

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0045 N2LOG
01 02565 133000          ADC 1,2          ;PERFORM ADD WITH NO CARRIES
02 02566 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
03 02567 116000          ADC 0,3          ;AC3 SHD NOW=-1
04 02570 174004          COM 3,3,SZR      ;WITH COM=0
05 02571 063077          HALT             ;ADD WITHOUT CARRY FAILED
06 02572 101120          MOVZL 0,0        ;SET UP NEXT TEST
07                  ;AC2 SHD=4000 AS A RESULT OF ABOVE TEST
08                       ADDT1 DEST,SRC,10000,2,1,Z,29
09                  ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
10                  ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
11                  ;AC0=10000 COMING INTO THE TEST
12                  ;ANC29:
13 02573 111000          MOV 0,2 ;SET UP DEST AC2
14 02574 126000          ADC 1,1
15 02575 124000          COM 1,1 ;SET AC1 SRC=0
16 02576 133000          ADC 1,2          ;PERFORM ADD WITH NO CARRIES
17 02577 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
18 02600 116000          ADC 0,3          ;AC3 SHD NOW=-1
19 02601 174004          COM 3,3,SZR      ;WITH COM=0
20 02602 063077          HALT             ;ADD WITHOUT CARRY FAILED
21 02603 101120          MOVZL 0,0        ;SET UP NEXT TEST
22                  ;AC2 SHD=10000 AS A RESULT OF ABOVE TEST
23                       ADDT1 DEST,SRC,20000,2,1,Z,30
24                  ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
25                  ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
26                  ;AC0=20000 COMING INTO THE TEST
27                  ;ANC30:
28 02604 111000          MOV 0,2 ;SET UP DEST AC2
29 02605 126000          ADC 1,1
30 02606 124000          COM 1,1 ;SET AC1 SRC=0
31 02607 133000          ADC 1,2          ;PERFORM ADD WITH NO CARRIES
32 02610 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
33 02611 116000          ADC 0,3          ;AC3 SHD NOW=-1
34 02612 174004          COM 3,3,SZR      ;WITH COM=0
35 02613 063077          HALT             ;ADD WITHOUT CARRY FAILED
36 02614 101120          MOVZL 0,0        ;SET UP NEXT TEST
37                  ;AC2 SHD=20000 AS A RESULT OF ABOVE TEST
38                       ADDT1 DEST,SRC,40000,2,1,Z,31
39                  ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
40                  ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
41                  ;AC0=40000 COMING INTO THE TEST
42                  ;ANC31:
43 02615 111000          MOV 0,2 ;SET UP DEST AC2
44 02616 126000          ADC 1,1
45 02617 124000          COM 1,1 ;SET AC1 SRC=0
46 02620 133000          ADC 1,2          ;PERFORM ADD WITH NO CARRIES
47 02621 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
48 02622 116000          ADC 0,3          ;AC3 SHD NOW=-1
49 02623 174004          COM 3,3,SZR      ;WITH COM=0
50 02624 063077          HALT             ;ADD WITHOUT CARRY FAILED
51 02625 101120          MOVZL 0,0        ;SET UP NEXT TEST
52                  ;AC2 SHD=40000 AS A RESULT OF ABOVE TEST
53                       ADDT1 DEST,SRC,100000,2,1,Z,32
54                  ;TEST ADD INSTRUCTION NO CARRY WHEN DEST IS NON ZERO
55                  ;SRC IS EQUAL TO 0-RESULT SHD BE SAME AS MOVE
56                  ;AC0=100000 COMING INTO THE TEST
57                  ;ANC32:
58 02626 111000          MOV 0,2 ;SET UP DEST AC2
59 02627 126000          ADC 1,1
60 02630 124000          COM 1,1 ;SET AC1 SRC=0
```

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0046 N2LOG
01 02631 133000          ADC 1,2          ;PERFORM ADD WITH NO CARRIES
02 02632 155000          MOV 2,3          ;THE DEST AC WAS NON ZERO
03 02633 116000          ADC 0,3          ;AC3 SHD NOW=-1
04 02634 174004          COM 3,3,SZR      ;WITH COM=0
05 02635 063077          HALT             ;ADD WITHOUT CARRY FAILED
06 02636 101120          MOVZL 0,0        ;SET UP NEXT TEST
07                  ;AC2 SHD=100000 AS A RESULT OF ABOVE TEST
```

```
;0047 N2LOG
01
02                ;SINGLE BIT CARRY TESTS DEFINE MACRO
03                ;CONSTANTS ARE SET UP BY ALREADY TESTED SHIFT
04
05                      .MACRO ADDT0
06                ;TEST SINGLE BIT CARRY ADD BIT A2 TO ITSELF
07                ;LOOK FOR RESULTANT CARRY INTO NEXT BIT A3
08                ;AND SUM BIT A2 TO GO TO 0 RESULT SHD=A5
09              ;ACA1:
10                      MOV 0,1         ;AC0=A4 COMING INTO TEST
11                      ADD 1,1         ;USE IT TO SET UP AC1+AC1
12                      MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
13                      ADC 1,2         ;AC2 SHD NOW=-1
14                      COM 2,2,SZR     ;NOT 0 IS BIT A2 CARRY FAILED
15                      HALT            ;BIT A2+A2 FAILED ADD SEE ALUA3
16                ;AND ALUA2
17                      MOVZL 0,0       ;SET UP NEXT TEST
18              %
19                ;SET UP BIT 15 FOR ADD TESTS
20 02637 102000         ADC 0,0
21 02640 102145         COMOL 0,0,SNR
22 02641 063077         HALT            ;AC0 SHD=+1
23
24                      ADDT0 00,15,14,1,2
25                ;TEST SINGLE BIT CARRY ADD BIT 15 TO ITSELF
26                ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 14
27                ;AND SUM BIT 15 TO GO TO 0 RESULT SHD=2
28              ;AC00:
29 02642 105000         MOV 0,1         ;AC0=1 COMING INTO TEST
30 02643 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
31 02644 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
32 02645 132000         ADC 1,2         ;AC2 SHD NOW=-1
33 02646 150004         COM 2,2,SZR     ;NOT 0 IS BIT 15 CARRY FAILED
34 02647 063077         HALT            ;BIT 15+15 FAILED ADD SEE ALU14
35                ;AND ALU15
36 02650 101120         MOVZL 0,0       ;SET UP NEXT TEST
37                      ADDT0 01,14,13,2,4
38                ;TEST SINGLE BIT CARRY ADD BIT 14 TO ITSELF
39                ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 13
40                ;AND SUM BIT 14 TO GO TO 0 RESULT SHD=4
41              ;AC01:
42 02651 105000         MOV 0,1         ;AC0=2 COMING INTO TEST
43 02652 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
44 02653 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
45 02654 132000         ADC 1,2         ;AC2 SHD NOW=-1
46 02655 150004         COM 2,2,SZR     ;NOT 0 IS BIT 14 CARRY FAILED
47 02656 063077         HALT            ;BIT 14+14 FAILED ADD SEE ALU13
48                ;AND ALU14
49 02657 101120         MOVZL 0,0       ;SET UP NEXT TEST
50                      ADDT0 02,13,12,4,10
51                ;TEST SINGLE BIT CARRY ADD BIT 13 TO ITSELF
52                ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 12
53                ;AND SUM BIT 13 TO GO TO 0 RESULT SHD=10
54              ;AC02:
55 02660 105000         MOV 0,1         ;AC0=4 COMING INTO TEST
56 02661 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
57 02662 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
58 02663 132000         ADC 1,2         ;AC2 SHD NOW=-1
59 02664 150004         COM 2,2,SZR     ;NOT 0 IS BIT 13 CARRY FAILED
60 02665 063077         HALT            ;BIT 13+13 FAILED ADD SEE ALU12
```

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;0048 N2LOG
01                ;AND ALU13
02 02666 101120         MOVZL 0,0       ;SET UP NEXT TEST
03                      ADDT0 03,12,11,10,20
04                ;TEST SINGLE BIT CARRY ADD BIT 12 TO ITSELF
05                ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 11
06                ;AND SUM BIT 12 TO GO TO 0 RESULT SHD=20
07              ;AC03:
08 02667 105000         MOV 0,1         ;AC0=10 COMING INTO TEST
09 02670 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
10 02671 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
11 02672 132000         ADC 1,2         ;AC2 SHD NOW=-1
12 02673 150004         COM 2,2,SZR     ;NOT 0 IS BIT 12 CARRY FAILED
13 02674 063077         HALT            ;BIT 12+12 FAILED ADD SEE ALU11
14                ;AND ALU12
15 02675 101120         MOVZL 0,0       ;SET UP NEXT TEST
16                ;IF ABOVE TEST FAILS ALSO SEE CN2 IF AC1=0
17                      ADDT0 04,11,10,20,40
18                ;TEST SINGLE BIT CARRY ADD BIT 11 TO ITSELF
19                ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 10
20                ;AND SUM BIT 11 TO GO TO 0 RESULT SHD=40
21              ;AC04:
22 02676 105000         MOV 0,1         ;AC0=20 COMING INTO TEST
23 02677 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
24 02700 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
25 02701 132000         ADC 1,2         ;AC2 SHD NOW=-1
26 02702 150004         COM 2,2,SZR     ;NOT 0 IS BIT 11 CARRY FAILED
27 02703 063077         HALT            ;BIT 11+11 FAILED ADD SEE ALU10
28                ;AND ALU11
29 02704 101120         MOVZL 0,0       ;SET UP NEXT TEST
30                      ADDT0 05,10,9,40,100
31                ;TEST SINGLE BIT CARRY ADD BIT 10 TO ITSELF
32                ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 9
33                ;AND SUM BIT 10 TO GO TO 0 RESULT SHD=100
34              ;AC05:
35 02705 105000         MOV 0,1         ;AC0=40 COMING INTO TEST
36 02706 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
37 02707 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
38 02710 132000         ADC 1,2         ;AC2 SHD NOW=-1
39 02711 150004         COM 2,2,SZR     ;NOT 0 IS BIT 10 CARRY FAILED
40 02712 063077         HALT            ;BIT 10+10 FAILED ADD SEE ALU9
41                ;AND ALU10
42 02713 101120         MOVZL 0,0       ;SET UP NEXT TEST
43                      ADDT0 06,9,8,100,200
44                ;TEST SINGLE BIT CARRY ADD BIT 9 TO ITSELF
45                ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 8
46                ;AND SUM BIT 9 TO GO TO 0 RESULT SHD=200
47              ;AC06:
48 02714 105000         MOV 0,1         ;AC0=100 COMING INTO TEST
49 02715 127000         ADD 1,1         ;USE IT TO SET UP AC1+AC1
50 02716 111120         MOVZL 0,2       ;AC2 SHD NOW=RESULT OF ADD
51 02717 132000         ADC 1,2         ;AC2 SHD NOW=-1
52 02720 150004         COM 2,2,SZR     ;NOT 0 IS BIT 9 CARRY FAILED
53 02721 063077         HALT            ;BIT 9+9 FAILED ADD SEE ALU8
54                ;AND ALU9
55 02722 101120         MOVZL 0,0       ;SET UP NEXT TEST
56                      ADDT0 07,8,7,200,400
57                ;TEST SINGLE BIT CARRY ADD BIT 8 TO ITSELF
58                ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 7
59                ;AND SUM BIT 8 TO GO TO 0 RESULT SHD=400
60              ;AC07:
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0049 N2LOG
01 02723 105000          MOV 0,1          ;AC0=200 COMING INTO TEST
02 02724 127000          ADD 1,1          ;USE IT TO SET UP AC1+AC1
03 02725 111120          MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
04 02726 132000          ADC 1,2          ;AC2 SHD NOW=-1
05 02727 150004          COM 2,2,SZR      ;NOT 0 IS BIT 8 CARRY FAILED
06 02730 063077          HALT             ;BIT 8+8 FAILED ADD SEE ALU7
07                    ;AND ALU8
08 02731 101120          MOVZL 0,0        ;SET UP NEXT TEST
09                    ;IF ABOVE TEST FAILS ALSO SEE CN1 IF AC1=0
10                       ADDT0 08,7,5,400,1000
11                    ;TEST SINGLE BIT CARRY ADD BIT 7 TO ITSELF
12                    ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 6
13                    ;AND SUM BIT 7 TO GO TO 0 RESULT SHD=1000
14                 ;AC08:
15 02732 105000          MOV 0,1          ;AC0=400 COMING INTO TEST
16 02733 127000          ADD 1,1          ;USE IT TO SET UP AC1+AC1
17 02734 111120          MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
18 02735 132000          ADC 1,2          ;AC2 SHD NOW=-1
19 02736 150004          COM 2,2,SZR      ;NOT 0 IS BIT 7 CARRY FAILED
20 02737 063077          HALT             ;BIT 7+7 FAILED ADD SEE ALU6
21                    ;AND ALU7
22 02740 101120          MOVZL 0,0        ;SET UP NEXT TEST
23                       ADDT0 09,6,5,1000,2000
24                    ;TEST SINGLE BIT CARRY ADD BIT 6 TO ITSELF
25                    ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 5
26                    ;AND SUM BIT 6 TO GO TO 0 RESULT SHD=2000
27                 ;AC09:
28 02741 105000          MOV 0,1          ;AC0=1000 COMING INTO TEST
29 02742 127000          ADD 1,1          ;USE IT TO SET UP AC1+AC1
30 02743 111120          MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
31 02744 132000          ADC 1,2          ;AC2 SHD NOW=-1
32 02745 150004          COM 2,2,SZR      ;NOT 0 IS BIT 6 CARRY FAILED
33 02746 063077          HALT             ;BIT 6+6 FAILED ADD SEE ALU5
34                    ;AND ALU6
35 02747 101120          MOVZL 0,0        ;SET UP NEXT TEST
36                       ADDT0 10,5,4,2000,4000
37                    ;TEST SINGLE BIT CARRY ADD BIT 5 TO ITSELF
38                    ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 4
39                    ;AND SUM BIT 5 TO GO TO 0 RESULT SHD=4000
40                 ;AC10:
41 02750 105000          MOV 0,1          ;AC0=2000 COMING INTO TEST
42 02751 127000          ADD 1,1          ;USE IT TO SET UP AC1+AC1
43 02752 111120          MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
44 02753 132000          ADC 1,2          ;AC2 SHD NOW=-1
45 02754 150004          COM 2,2,SZR      ;NOT 0 IS BIT 5 CARRY FAILED
46 02755 063077          HALT             ;BIT 5+5 FAILED ADD SEE ALU4
47                    ;AND ALU5
48 02756 101120          MOVZL 0,0        ;SET UP NEXT TEST
49                       ADDT0 11,4,3,4000,10000
50                    ;TEST SINGLE BIT CARRY ADD BIT 4 TO ITSELF
51                    ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 3
52                    ;AND SUM BIT 4 TO GO TO 0 RESULT SHD=10000
53                 ;AC11:
54 02757 105000          MOV 0,1          ;AC0=4000 COMING INTO TEST
55 02760 127000          ADD 1,1          ;USE IT TO SET UP AC1+AC1
56 02761 111120          MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
57 02762 132000          ADC 1,2          ;AC2 SHD NOW=-1
58 02763 150004          COM 2,2,SZR      ;NOT 0 IS BIT 4 CARRY FAILED
59 02764 063077          HALT             ;BIT 4+4 FAILED ADD SEE ALU3
60                    ;AND ALU4
```

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0050 N2LOG
01 02765 101120          MOVZL 0,0        ;SET UP NEXT TEST
02                    ;IF ABOVE TEST FAILS SEE ALSO CN0 IF AC1=0
03                       ADDT0 12,3,2,10000,20000
04                    ;TEST SINGLE BIT CARRY ADD BIT 3 TO ITSELF
05                    ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 2
06                    ;AND SUM BIT 3 TO GO TO 0 RESULT SHD=20000
07                 ;AC12:
08 02766 105000          MOV 0,1          ;AC0=10000 COMING INTO TEST
09 02767 127000          ADD 1,1          ;USE IT TO SET UP AC1+AC1
10 02770 111120          MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
11 02771 132000          ADC 1,2          ;AC2 SHD NOW=-1
12 02772 150004          COM 2,2,SZR      ;NOT 0 IS BIT 3 CARRY FAILED
13 02773 063077          HALT             ;BIT 3+3 FAILED ADD SEE ALU2
14                    ;AND ALU3
15 02774 101120          MOVZL 0,0        ;SET UP NEXT TEST
16                       ADDT0 13,2,1,20000,40000
17                    ;TEST SINGLE BIT CARRY ADD BIT 2 TO ITSELF
18                    ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 1
19                    ;AND SUM BIT 2 TO GO TO 0 RESULT SHD=40000
20                 ;AC13:
21 02775 105000          MOV 0,1          ;AC0=20000 COMING INTO TEST
22 02776 127000          ADD 1,1          ;USE IT TO SET UP AC1+AC1
23 02777 111120          MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
24 03000 132000          ADC 1,2          ;AC2 SHD NOW=-1
25 03001 150004          COM 2,2,SZR      ;NOT 0 IS BIT 2 CARRY FAILED
26 03002 063077          HALT             ;BIT 2+2 FAILED ADD SEE ALU1
27                    ;AND ALU2
28 03003 101120          MOVZL 0,0        ;SET UP NEXT TEST
29                       ADDT0 14,1,0,40000,100000
30                    ;TEST SINGLE BIT CARRY ADD BIT 1 TO ITSELF
31                    ;LOOK FOR RESULTANT CARRY INTO NEXT BIT 0
32                    ;AND SUM BIT 1 TO GO TO 0 RESULT SHD=100000
33                 ;AC14:
34 03004 105000          MOV 0,1          ;AC0=40000 COMING INTO TEST
35 03005 127000          ADD 1,1          ;USE IT TO SET UP AC1+AC1
36 03006 111120          MOVZL 0,2        ;AC2 SHD NOW=RESULT OF ADD
37 03007 132000          ADC 1,2          ;AC2 SHD NOW=-1
38 03010 150004          COM 2,2,SZR      ;NOT 0 IS BIT 1 CARRY FAILED
39 03011 063077          HALT             ;BIT 1+1 FAILED ADD SEE ALU0
40                    ;AND ALU1
41 03012 101120          MOVZL 0,0        ;SET UP NEXT TEST
42
43                    ;TEST ADD BIT 0 TO BIT0 AC0=100000
44                    ;SEE THAT CRYOUT GETS TO CRY
45 03013 105000       AC15:  MOVZ 0,1
46 03014 127004          ADD 1,1,SZR      ;ADD BIT 0 TO 0 FAILED
47 03015 063077          HALT
48 03016 125003          MOV 1,1,SNC      ;BIT 0+BIT 0 DID NOT CRY OUT
49 03017 063077          HALT
```

```
1@@51 N2LOG
01
02                  ;TEST AND INSTRUCTION AND VARIATIONS
03                  ;FIRST TEST GROSS CASE AND -1 TO -1
04
05 03020 102000 AND00:  ADC 0,0             ;SET AC0=-1
06 03021 103405         AND 0,0,SNR         ;FIRST USE OF "AND"
07 03022 063077         HALT                ;RESULT SHD STILL BE NON 0
08                  ;IF RESULT=0 "AND" LOOKS LIKE "SUB" OR "INC"
09                  ;SEE NOT IR16 OR NOT IR15 AT ALU ROM
10 03023 104004         COM 0,1,SZR
11 03024 063077         HALT                ;RESULT OF PREV AND NOT=-1
12                  ;IF RESULT IN AC0=-2 "AND" LOOKS LIKE "ADD"
13                  ;SEE NOT IR7 AT ALU ROM
14
15                  ;TEST AND 0'S TO 0'S RESULT SHD REMAIN=0
16 03025 102002 AND01:  ADC 0,0
17 03026 100002         COM 0,0             ;AC0=0
18 03027 103404         AND 0,0,SZR         ;RESULT OF AND SHD=0
19 03030 063077         HALT
20 03031 101004         MOV 0,0,SZR         ;RECHECK RESULT
21 03032 063077         HALT
22                  ;SEE RESULT IN AC0 TO DETERMINE ALU BIT(S) IN ERR
23
24                  ;AND -1 TO 0 WITH 0 AS DESTINATION
25                  ;RESULT SHOULD AGAIN=0'S
26 03033 102000 AND02:  ADC 0,0
27 03034 104000         COM 0,1
28 03035 107404         AND 0,1,SZR         ;DEST REG AC1=0'S
29 03036 063077         HALT                ;RESULT OF ABOVE AND NOT=0
30 03037 125004         MOV 1,1,SZR         ;RECHECK RESULT
31 03040 063077         HALT
32                  ;EXAMINE AC1 TO DETERMINE ALU BIT(S) IN ERROR
33
34                  ;TEST AND OF 0 TO -1 WITH -1 ORIGINAL DESTINATION
35 03041 102000 AND03:  ADC 0,0
36 03042 104000         COM 0,1
37 03043 123404         AND 1,0,SZR         ;DEST=-1  SRC=0  RES SHD=0
38 03044 063077         HALT
39 03045 101004         MOV  0,0,SZR        ;RECHECK RESULT
40 03046 063077         HALT
41                  ;EXAMINE AC0 TO DETERMINE ALU BIT(S) IN ERROR
```

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1@@52 N2LOG
01
02                  ;DEFINE BIT TEST MACRO FOR AND INSTRUCTION
03                      .MACRO ANDTS
04                  ;THE NEXT SERIES IS AN AND TST OF BIT A2
05                  ;AC0=A3 COMING INTO THE TEST
06                ;ANDA1:
07                      MOV 0,1             ;AC0=A3
08                      AND 0,1,SNR         ;BIT A2 SHD REMAIN=1
09                      HALT
10                      MOV 1,2
11                      ADC 0,2
12                      COM 2,2,SZR         ;TEST FOR EXTRA BITS
13                      HALT                ;MORE THAN 1 BIT IN AND OF A3
14                  ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=A3
15                  ;NOW TEST AND OF COMPLIMENTS
16                  ;SOURCE WILL=A3 DEST WILL=COMPLIMENT
17                ;ANA1A:
18                      COM 0,1
19                      AND 0,1,SZR
20                      HALT                ;AND OF A3 AND ITS COM FAILED
21                  ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
22                  ;TEST AND OF COMPLIMENTS WITH DEST=A3 AND SRC=COM
23                ;ANA1M:
24                      MOV 0,1
25                      COM 1,2
26                      AND 2,1,SZR
27                      HALT                ;AND OF A3 AND ITS COM FAILED
28                  ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
29                      MOVZL 0,0           ;SET UP NEXT TEST
30                %
31
32
33                  ;SET UP AC0=1 FOR FIRST AND TEST
34
35 03047 102000         ADC 0,0
36 03050 107145         COMOL 0,0,SNR
37 03051 063077         HALT
```

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0053 N2LOG

                        ANDTS 04,15,1
                    ;THE NEXT SERIES IS AN AND TST OF BIT 15
                    ;AC0=1 COMING INTO THE TEST
                ;AND04:
03052 105000            MOV 0,1             ;AC0=1
03053 107405            AND 0,1,SNR         ;BIT 15 SHD REMAIN=1
03054 063077            HALT
03055 131000            MOV 1,2
03056 112000            ADC 0,2
03057 150004            COM 2,2,SZR         ;TEST FOR EXTRA BITS
03060 063077            HALT                ;MORE THAN 1 BIT IN AND OF 1
                    ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=1
                    ;NOW TEST AND OF COMPLIMENTS
                    ;SOURCE WILL=1 DEST WILL=COMPLIMENT
                ;AN04A:
03061 104000            COM 0,1
03062 107404            AND 0,1,SZR
03063 063077            HALT                ;AND OF 1 AND ITS COM FAILED
                    ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
                    ;TEST AND OF COMPLIMENTS WITH DEST=1 AND SRC=COM
                ;AN04B:
03064 105000            MOV 0,1
03065 130000            COM 1,2
03066 147404            AND 2,1,SZR
03067 063077            HALT                ;AND OF 1 AND ITS COM FAILED
                    ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
03070 101120            MOVZL 0,0           ;SET UP NEXT TEST
                        ANDTS 05,14,2
                    ;THE NEXT SERIES IS AN AND TST OF BIT 14
                    ;AC0=2 COMING INTO THE TEST
                ;AND05:
03071 105000            MOV 0,1             ;AC0=2
03072 107405            AND 0,1,SNR         ;BIT 14 SHD REMAIN=1
03073 063077            HALT
03074 131000            MOV 1,2
03075 112000            ADC 0,2
03076 150004            COM 2,2,SZR         ;TEST FOR EXTRA BITS
03077 063077            HALT                ;MORE THAN 1 BIT IN AND OF 2
                    ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=2
                    ;NOW TEST AND OF COMPLIMENTS
                    ;SOURCE WILL=2 DEST WILL=COMPLIMENT
                ;AN05A:
03100 104000            COM 0,1
03101 107404            AND 0,1,SZR
03102 063077            HALT                ;AND OF 2 AND ITS COM FAILED
                    ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
                    ;TEST AND OF COMPLIMENTS WITH DEST=2 AND SRC=COM
                ;AN05B:
03103 105000            MOV 0,1
03104 130000            COM 1,2
03105 147404            AND 2,1,SZR
03106 063077            HALT                ;AND OF 2 AND ITS COM FAILED
                    ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
03107 101120            MOVZL 0,0           ;SET UP NEXT TEST
                        ANDTS 06,13,4
                    ;THE NEXT SERIES IS AN AND TST OF BIT 13
                    ;AC0=4 COMING INTO THE TEST
                ;AND06:
03110 105000            MOV 0,1             ;AC0=4
```

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0054 N2LOG

03111 107405            AND 0,1,SNR         ;BIT 13 SHD REMAIN=1
03112 063077            HALT
03113 131000            MOV 1,2
03114 112000            ADC 0,2
03115 150004            COM 2,2,SZR         ;TEST FOR EXTRA BITS
03116 063077            HALT                ;MORE THAN 1 BIT IN AND OF 4
                    ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=4
                    ;NOW TEST AND OF COMPLIMENTS
                    ;SOURCE WILL=4 DEST WILL=COMPLIMENT
                ;AN06A:
03117 104000            COM 0,1
03120 107404            AND 0,1,SZR
03121 063077            HALT                ;AND OF 4 AND ITS COM FAILED
                    ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
                    ;TEST AND OF COMPLIMENTS WITH DEST=4 AND SRC=COM
                ;AN06B:
03122 105000            MOV 0,1
03123 130000            COM 1,2
03124 147404            AND 2,1,SZR
03125 063077            HALT                ;AND OF 4 AND ITS COM FAILED
                    ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
03126 101120            MOVZL 0,0           ;SET UP NEXT TEST
                        ANDTS 07,12,10
                    ;THE NEXT SERIES IS AN AND TST OF BIT 12
                    ;AC0=10 COMING INTO THE TEST
                ;AND07:
03127 105000            MOV 0,1             ;AC0=10
03130 107405            AND 0,1,SNR         ;BIT 12 SHD REMAIN=1
03131 063077            HALT
03132 131000            MOV 1,2
03133 112000            ADC 0,2
03134 150004            COM 2,2,SZR         ;TEST FOR EXTRA BITS
03135 063077            HALT                ;MORE THAN 1 BIT IN AND OF 10
                    ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=10
                    ;NOW TEST AND OF COMPLIMENTS
                    ;SOURCE WILL=10 DEST WILL=COMPLIMENT
                ;AN07A:
03136 104000            COM 0,1
03137 107404            AND 0,1,SZR
03140 063077            HALT                ;AND OF 10 AND ITS COM FAILED
                    ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
                    ;TEST AND OF COMPLIMENTS WITH DEST=10 AND SRC=COM
                ;AN07B:
03141 105000            MOV 0,1
03142 130000            COM 1,2
03143 147404            AND 2,1,SZR
03144 063077            HALT                ;AND OF 10 AND ITS COM FAILED
                    ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
03145 101120            MOVZL 0,0           ;SET UP NEXT TEST
                        ANDTS 08,11,20
                    ;THE NEXT SERIES IS AN AND TST OF BIT 11
                    ;AC0=20 COMING INTO THE TEST
                ;AN08B:
03146 105000            MOV 0,1             ;AC0=20
03147 107405            AND 0,1,SNR         ;BIT 11 SHD REMAIN=1
03150 063077            HALT
03151 131000            MOV 1,2
03152 112000            ADC 0,2
03153 150004            COM 2,2,SZR         ;TEST FOR EXTRA BITS
03154 063077            HALT                ;MORE THAN 1 BIT IN AND OF 20
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0055 N2LOG
01                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=20
02                      ;NOW TEST AND OF COMPLIMENTS
03                      ;SOURCE WILL=20 DEST WILL=COMPLIMENT
04                    ;AN00A:
05 03155 104000                 COM 0,1
06 03156 107404                 AND 0,1,SZR
07 03157 063077                 HALT                    ;AND OF 20 AND ITS COM FAILED
08                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
09                      ;TEST AND OF COMPLIMENTS WITH DEST=20 AND SRC=COM
10                    ;AN00B:
11 03160 105000                 MOV 0,1
12 03161 130000                 COM 1,2
13 03162 147404                 AND 2,1,SZR
14 03163 063077                 HALT                    ;AND OF 20 AND ITS COM FAILED
15                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
16 03164 101120                 MOVZL 0,0               ;SET UP NEXT TEST
17                              ANDTS 09,10,40
18                      ;THE NEXT SERIES IS AN AND TST OF BIT 10
19                      ;AC0=40 COMING INTO THE TEST
20                    ;AND09:
21 03165 105000                 MOV 0,1                 ;AC0=40
22 03166 107405                 AND 0,1,SNR             ;BIT 10 SHD REMAIN=1
23 03167 063077                 HALT
24 03170 131000                 MOV 1,2
25 03171 112000                 ADC 0,2
26 03172 150004                 COM 2,2,SZR             ;TEST FOR EXTRA BITS
27 03173 063077                 HALT                    ;MORE THAN 1 BIT IN AND OF 40
28                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=40
29                      ;NOW TEST AND OF COMPLIMENTS
30                      ;SOURCE WILL=40 DEST WILL=COMPLIMENT
31                    ;AN09A:
32 03174 104000                 COM 0,1
33 03175 107404                 AND 0,1,SZR
34 03176 063077                 HALT                    ;AND OF 40 AND ITS COM FAILED
35                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
36                      ;TEST AND OF COMPLIMENTS WITH DEST=40 AND SRC=COM
37                    ;AN09B:
38 03177 105000                 MOV 0,1
39 03200 130000                 COM 1,2
40 03201 147404                 AND 2,1,SZR
41 03202 063077                 HALT                    ;AND OF 40 AND ITS COM FAILED
42                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
43 03203 101120                 MOVZL 0,0               ;SET UP NEXT TEST
44                              ANDTS 10,9,100
45                      ;THE NEXT SERIES IS AN AND TST OF BIT 9
46                      ;AC0=100 COMING INTO THE TEST
47                    ;AND10:
48 03204 105000                 MOV 0,1                 ;AC0=100
49 03205 107405                 AND 0,1,SNR             ;BIT 9 SHD REMAIN=1
50 03206 063077                 HALT
51 03207 131000                 MOV 1,2
52 03210 112000                 ADC 0,2
53 03211 150004                 COM 2,2,SZR             ;TEST FOR EXTRA BITS
54 03212 063077                 HALT                    ;MORE THAN 1 BIT IN AND OF 100
55                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=100
56                      ;NOW TEST AND OF COMPLIMENTS
57                      ;SOURCE WILL=100 DEST WILL=COMPLIMENT
58                    ;AN10A:
59 03213 104000                 COM 0,1
60 03214 107404                 AND 0,1,SZR
```

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0056 N2LOG
01 03215 063077                 HALT                    ;AND OF 100 AND ITS COM FAILED
02                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
03                      ;TEST AND OF COMPLIMENTS WITH DEST=100 AND SRC=COM
04                    ;AN10B:
05 03216 105000                 MOV 0,1
06 03217 130000                 COM 1,2
07 03220 147404                 AND 2,1,SZR
08 03221 063077                 HALT                    ;AND OF 100 AND ITS COM FAILED
09                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
10 03222 101120                 MOVZL 0,0               ;SET UP NEXT TEST
11                              ANDTS 11,8,200
12                      ;THE NEXT SERIES IS AN AND TST OF BIT 8
13                      ;AC0=200 COMING INTO THE TEST
14                    ;AND11:
15 03223 105000                 MOV 0,1                 ;AC0=200
16 03224 107405                 AND 0,1,SNR             ;BIT 8 SHD REMAIN=1
17 03225 063077                 HALT
18 03226 131000                 MOV 1,2
19 03227 112000                 ADC 0,2
20 03230 150004                 COM 2,2,SZR             ;TEST FOR EXTRA BITS
21 03231 063077                 HALT                    ;MORE THAN 1 BIT IN AND OF 200
22                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=200
23                      ;NOW TEST AND OF COMPLIMENTS
24                      ;SOURCE WILL=200 DEST WILL=COMPLIMENT
25                    ;AN11A:
26 03232 104000                 COM 0,1
27 03233 107404                 AND 0,1,SZR
28 03234 063077                 HALT                    ;AND OF 200 AND ITS COM FAILED
29                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
30                      ;TEST AND OF COMPLIMENTS WITH DEST=200 AND SRC=COM
31                    ;AN11B:
32 03235 105000                 MOV 0,1
33 03236 130000                 COM 1,2
34 03237 147404                 AND 2,1,SZR
35 03240 063077                 HALT                    ;AND OF 200 AND ITS COM FAILED
36                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
37 03241 101120                 MOVZL 0,0               ;SET UP NEXT TEST
38                              ANDTS 12,7,400
39                      ;THE NEXT SERIES IS AN AND TST OF BIT 7
40                      ;AC0=400 COMING INTO THE TEST
41                    ;AND12:
42 03242 105000                 MOV 0,1                 ;AC0=400
43 03243 107405                 AND 0,1,SNR             ;BIT 7 SHD REMAIN=1
44 03244 063077                 HALT
45 03245 131000                 MOV 1,2
46 03246 112000                 ADC 0,2
47 03247 150004                 COM 2,2,SZR             ;TEST FOR EXTRA BITS
48 03250 063077                 HALT                    ;MORE THAN 1 BIT IN AND OF 400
49                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=400
50                      ;NOW TEST AND OF COMPLIMENTS
51                      ;SOURCE WILL=400 DEST WILL=COMPLIMENT
52                    ;AN12A:
53 03251 104000                 COM 0,1
54 03252 107404                 AND 0,1,SZR
55 03253 063077                 HALT                    ;AND OF 400 AND ITS COM FAILED
56                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
57                      ;TEST AND OF COMPLIMENTS WITH DEST=400 AND SRC=COM
58                    ;AN12B:
59 03254 105000                 MOV 0,1
60 03255 130000                 COM 1,2
```

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0057 N2LOG
03256 147404            AND 2,1,SZR
03257 063077            HALT                    ;AND OF 400 AND ITS COM FAILED
                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
03260 101120            MOVZL 0,0               ;SET UP NEXT TEST
                        ANDTS 13,6,1000
                      ;THE NEXT SERIES IS AN AND TST OF BIT 6
                      ;AC0=1000 COMING INTO THE TEST
                    ;AND13:
03261 105000            MOV 0,1                 ;AC0=1000
03262 107405            AND 0,1,SNR             ;BIT 6 SHD REMAIN=1
03263 063077            HALT
03264 131000            MOV 1,2
03265 112000            ADC 0,2
03266 150004            COM 2,2,SZR             ;TEST FOR EXTRA BITS
03267 063077            HALT                    ;MORE THAN 1 BIT IN AND OF 1000
                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=1000
                      ;NOW TEST AND OF COMPLIMENTS
                      ;SOURCE WILL=1000 DEST WILL=COMPLIMENT
                    ;AN13A:
03270 104000            COM 0,1
03271 107404            AND 0,1,SZR
03272 063077            HALT                    ;AND OF 1000 AND ITS COM FAILED
                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
                      ;TEST AND OF COMPLIMENTS WITH DEST=1000 AND SRC=COM
                    ;AN13B:
03273 105000            MOV 0,1
03274 130000            COM 1,2
03275 147404            AND 2,1,SZR
03276 063077            HALT                    ;AND OF 1000 AND ITS COM FAILED
                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
03277 101120            MOVZL 0,0               ;SET UP NEXT TEST
                        ANDTS 14,5,2000
                      ;THE NEXT SERIES IS AN AND TST OF BIT 5
                      ;AC0=2000 COMING INTO THE TEST
                    ;AND14:
03300 105000            MOV 0,1                 ;AC0=2000
03301 107405            AND 0,1,SNR             ;BIT 5 SHD REMAIN=1
03302 063077            HALT
03303 131000            MOV 1,2
03304 112000            ADC 0,2
03305 150004            COM 2,2,SZR             ;TEST FOR EXTRA BITS
03306 063077            HALT                    ;MORE THAN 1 BIT IN AND OF 2000
                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=2000
                      ;NOW TEST AND OF COMPLIMENTS
                      ;SOURCE WILL=2000 DEST WILL=COMPLIMENT
                    ;AN14A:
03307 104000            COM 0,1
03310 107404            AND 0,1,SZR
03311 063077            HALT                    ;AND OF 2000 AND ITS COM FAILED
                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
                      ;TEST AND OF COMPLIMENTS WITH DEST=2000 AND SRC=COM
                    ;AN14B:
03312 105000            MOV 0,1
03313 130000            COM 1,2
03314 147404            AND 2,1,SZR
03315 063077            HALT                    ;AND OF 2000 AND ITS COM FAILED
                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
03316 101120            MOVZL 0,0               ;SET UP NEXT TEST
                        ANDTS 15,4,4000
                      ;THE NEXT SERIES IS AN AND TST OF BIT 4
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0058 N2LOG
                      ;AC0=4000 COMING INTO THE TEST
                    ;AND15:
03317 105000            MOV 0,1                 ;AC0=4000
03320 107405            AND 0,1,SNR             ;BIT 4 SHD REMAIN=1
03321 063077            HALT
03322 131000            MOV 1,2
03323 112000            ADC 0,2
03324 150004            COM 2,2,SZR             ;TEST FOR EXTRA BITS
03325 063077            HALT                    ;MORE THAN 1 BIT IN AND OF 4000
                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=4000
                      ;NOW TEST AND OF COMPLIMENTS
                      ;SOURCE WILL=4000 DEST WILL=COMPLIMENT
                    ;AN15A:
03326 104000            COM 0,1
03327 107404            AND 0,1,SZR
03330 063077            HALT                    ;AND OF 4000 AND ITS COM FAILED
                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
                      ;TEST AND OF COMPLIMENTS WITH DEST=4000 AND SRC=COM
                    ;AN15B:
03331 105000            MOV 0,1
03332 130000            COM 1,2
03333 147404            AND 2,1,SZR
03334 063077            HALT                    ;AND OF 4000 AND ITS COM FAILED
                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
03335 101120            MOVZL 0,0               ;SET UP NEXT TEST
                        ANDTS 16,3,10000
                      ;THE NEXT SERIES IS AN AND TST OF BIT 3
                      ;AC0=10000 COMING INTO THE TEST
                    ;AND16:
03336 105000            MOV 0,1                 ;AC0=10000
03337 107405            AND 0,1,SNR             ;BIT 3 SHD REMAIN=1
03340 063077            HALT
03341 131000            MOV 1,2
03342 112000            ADC 0,2
03343 150004            COM 2,2,SZR             ;TEST FOR EXTRA BITS
03344 063077            HALT                    ;MORE THAN 1 BIT IN AND OF 10000
                      ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=10000
                      ;NOW TEST AND OF COMPLIMENTS
                      ;SOURCE WILL=10000 DEST WILL=COMPLIMENT
                    ;AN16A:
03345 104000            COM 0,1
03346 107404            AND 0,1,SZR
03347 063077            HALT                    ;AND OF 10000 AND ITS COM FAILED
                      ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
                      ;TEST AND OF COMPLIMENTS WITH DEST=10000 AND SRC=COM
                    ;AN16B:
03350 105000            MOV 0,1
03351 130000            COM 1,2
03352 147404            AND 2,1,SZR
03353 063077            HALT                    ;AND OF 10000 AND ITS COM FAILED
                      ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
03354 101120            MOVZL 0,0               ;SET UP NEXT TEST
                        ANDTS 17,2,20000
                      ;THE NEXT SERIES IS AN AND TST OF BIT 2
                      ;AC0=20000 COMING INTO THE TEST
                    ;AND17:
03355 105000            MOV 0,1                 ;AC0=20000
03356 107405            AND 0,1,SNR             ;BIT 2 SHD REMAIN=1
03357 063077            HALT
03360 131000            MOV 1,2
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0059 N2LOG
01 03361 112000          ADC 0,2
02 03362 150004          COM 2,2,SZR      ;TEST FOR EXTRA BITS
03 03363 063077          HALT             ;MORE THAN 1 BIT IN AND OF 20000
04                     ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=20000
05                     ;NOW TEST AND OF COMPLIMENTS
06                     ;SOURCE WILL=20000 DEST WILL=COMPLIMENT
07                   ;AN17A:
08 03364 104000          COM 0,1
09 03365 107404          AND 0,1,SZR
10 03366 063077          HALT             ;AND OF 20000 AND ITS COM FAILED
11                     ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
12                     ;TEST AND OF COMPLIMENTS WITH DEST=20000 AND SRC=COM
13                   ;AN17B:
14 03367 105000          MOV 0,1
15 03370 130000          COM 1,2
16 03371 147404          AND 2,1,SZR
17 03372 063077          HALT             ;AND OF 20000 AND ITS COM FAILED
18                     ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
19 03373 101120          MOVZL 0,0        ;SET UP NEXT TEST
20                       ANDTS 18,1,40000
21                     ;THE NEXT SERIES IS AN AND TST OF BIT 1
22                     ;AC0=40000 COMING INTO THE TEST
23                   ;AND18:
24 03374 105000          MOV 0,1          ;AC0=40000
25 03375 107405          AND 0,1,SNR      ;BIT 1 SHD REMAIN=1
26 03376 063077          HALT
27 03377 131000          MOV 1,2
28 03400 112000          ADC 0,2
29 03401 150004          COM 2,2,SZR      ;TEST FOR EXTRA BITS
30 03402 063077          HALT             ;MORE THAN 1 BIT IN AND OF 40000
31                     ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=40000
32                     ;NOW TEST AND OF COMPLIMENTS
33                     ;SOURCE WILL=40000 DEST WILL=COMPLIMENT
34                   ;AN18A:
35 03403 104000          COM 0,1
36 03404 107404          AND 0,1,SZR
37 03405 063077          HALT             ;AND OF 40000 AND ITS COM FAILED
38                     ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
39                     ;TEST AND OF COMPLIMENTS WITH DEST=40000 AND SRC=COM
40                   ;AN18B:
41 03406 105000          MOV 0,1
42 03407 130000          COM 1,2
43 03410 147404          AND 2,1,SZR
44 03411 063077          HALT             ;AND OF 40000 AND ITS COM FAILED
45                     ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
46 03412 101120          MOVZL 0,0        ;SET UP NEXT TEST
47                       ANDTS 19,0,100000
48                     ;THE NEXT SERIES IS AN AND TST OF BIT 0
49                     ;AC0=100000 COMING INTO THE TEST
50                   ;AND19:
51 03413 105000          MOV 0,1          ;AC0=100000
52 03414 107405          AND 0,1,SNR      ;BIT 0 SHD REMAIN=1
53 03415 063077          HALT
54 03416 131000          MOV 1,2
55 03417 112000          ADC 0,2
56 03420 150004          COM 2,2,SZR      ;TEST FOR EXTRA BITS
57 03421 063077          HALT             ;MORE THAN 1 BIT IN AND OF 100000
58                     ;EXAMINE AC1 TO DETERMINE BIT(S) IN ERROR IT SHD=100000
59                     ;NOW TEST AND OF COMPLIMENTS
60                     ;SOURCE WILL=100000 DEST WILL=COMPLIMENT
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0060 N2LOG
01                   ;AN19A:
02 03422 104000          COM 0,1
03 03423 107404          AND 0,1,SZR
04 03424 063077          HALT             ;AND OF 100000 AND ITS COM FAILED
05                     ;EXAMINE AC1 TO DETERMINE BIT(S) FAILED IT SHD=0
06                     ;TEST AND OF COMPLIMENTS WITH DEST=100000 AND SRC=COM
07                   ;AN19B:
08 03425 105000          MOV 0,1
09 03426 130000          COM 1,2
10 03427 147404          AND 2,1,SZR
11 03430 063077          HALT             ;AND OF 100000 AND ITS COM FAILED
12                     ;EXAMINE AC1 TO DETERMINE BITS FAILED IT SHD=0
13 03431 101120          MOVZL 0,0        ;SET UP NEXT TEST
```

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10061 N2LOG
01
02                ;THE NEXT SERIES OF TESTS VERIFY THAT "AND"
03                ;DOES NOT EFFECT "CRY"
04
05 03432 102020 AND20:  ADCZ 0,0          ;CRY=0  AC0=-1
06 03433 103402         AND 0,0,SZC       ;CRY SHD STILL=0
07 03434 063077         HALT              ;AND SET CRY=1
08                ;SEE "NOT AND" AND WITH CRY OUT
09
10 03435 102040 AND21:  ADCO 0,0          ;AND=1 WITH CRY=1
11 03436 103403         AND 0,0,SNC       ;CRY SHD STILL=1
12 03437 063077         HALT              ;AND OF -1-1 CLRD CRY
13
14                ;TEST AND WITH 00 TO NOT CHNG CRY 0 TO 1
15
16 03440 102000 AND22:  ADC 0,0
17 03441 100020         COMZ 0,0
18 03442 103402         AND 0,0,SZC
19 03443 063077         HALT
20                ;TEST AND WITH 00 TO NOT CHNG CRY 1 TO 0
21 03444 102000 AND23:  ADC 0,0
22 03445 100040         COMO 0,0
23 03446 103403         AND 0,0,SNC
24 03447 063077         HALT
25
26                ;REPEAT TESTS CHANGING STATE OF CRY DURING AND
27
28 03450 102040 AND24:  ADCO 0,0
29 03451 103422         ANDZ 0,0,SZC
30 03452 063077         HALT              ;SEE IR11 NOT IR10 IN NOT SCI
31                ;POSSIBLY TRANSITION TIMING AS AND DID NOT PREV CHNG CRY
32 03453 102020 AND25:  ADCZ 0,0
33 03454 103443         ANDO 0,0,SNC      ;SEE NOT OF ABOVE TEST IR10=11
34 03455 063077         HALT              ;CRY WENT TO 0 AND -1 TO -1
35
36 03456 102000 AND26:  ADC 0,0
37 03457 100040         COMO 0,0
38 03460 103422         ANDZ 0,0,SZC      ;FURTHER TEST AND IN SCI LOGIC
39 03461 063077         HALT              ;CRY WENT TO 1 AND 0 TO 0
40
41 03462 102000 AND27:  ADC 0,0
42 03463 100020         COMZ 0,0
43 03464 103443         ANDO 0,0,SNC
44 03465 063077         HALT              ;CRY WENT 1 TO 0 AND OF 0 TO 0
45
46
```

```
10062 N2LOG
01                ;VERIFY THE EXISTENCE OF INC INSTRUCTION
02                ;FIRST TIME FOR "INC" INSTRUCTION
03 03466 102000 INC00:  ADC 0,0
04 03467 100000         COM 0,0
05 03470 101005         INC 0,0,SNR       ;RESULT=0 POSSIBLY ALU CRY NOT
06 03471 063077         HALT              ;AC0 SHD=+1
07 03472 101005         MOV 0,0,SNR
08 03473 063077         HALT              ;MAKE SURE RESULT GOT BACK TO 0
09 03474 105224         MOVZR 0,1,SZR     ;MAKE SURE ONLY +1 NO EXTRAS
10 03475 063077         HALT              ;EXAMINE AC0 FOR EXTRA BITS INC
11                ;AC0=0 POSSIBLY "NOT" IR6 INC LOOKS LIKE NEG
12                ;OR "NOT" IR7 INC LOOKS LIKE MOV SEE ALU ROM
13                ;OR IR5 INTO ID ALC ROM INC LOOKS LIKE AND
14
15                ;TEST INC OF +1 TO +2 (2ND TIME FOR INC)
16 03476 102000 INC01:  ADC 0,0
17 03477 104140         COMOL 0,0         ;AC0=+1
18 03500 105120         MOVZL 0,1         ;AC1=+2
19 03501 101405         INC 0,0,SNR       ;1+1 SHD=2
20 03502 063077         HALT              ;BIT 15 CARRY TO BIT 14(?)
21 03503 100000         ADC 0,1           ;AC1 SHD NOW=-1 (IF INC WORKED)
22 03504 124404         COM 1,1,SZR       ;AND COM SHD BE 0
23 03505 063077         HALT              ;AC0 INC'D+1 INCORRECT
24                ;EXAMINE AC0 FOR ALU FAILURE IT SHD=+2
25                ;IF AC0 DOES=+2 EXAMINE AC1 FOR ADC+COM FAILURE
26
27                ;TEST TO INSURE ONLY SRC REG IS INVOLVED IN INC
28 03506 102000 INC02:  ADC 0,0
29 03507 100000         COM 0,0           ;AC0=0
30 03510 104140         COMOL 0,1         ;AC1=1
31 03511 125140         MOVOL 1,1         ;=3
32 03512 105405         INC 0,1,SNR       ;0+1 SHD=1
33 03513 063077         HALT              ;ALU CRY FAILED (?) ALRDY TESTED
34 03514 131224         MOVZR 1,2,SZR     ;AC1 SHD ONLY=1
35 03515 063077         HALT              ;PROBABLY DESTINATION REG ALSO ADDED
36                ;SEE 2 REN ID ALC ROM INC ALSO CAUSES ADD OR AND
```

```
0063 N2LOG
01
02                ;TEST INC TO CARRY THROUGH ALL 1 BITS
03                ;DEFINE MACRO FOR CARRY TESTS
04                      .MACRO INCTS
05                ;AC0=-4 COMING INTO TEST,+1=AC1=-5
06                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
07                ;BIT-2 INTO BIT-3 WITH RESULT=AC1
08              ;INC-1:
09                      INC 0,2,SNR       ;AC0=-4+1 AND BE NON ZERO
10                      HALT              ;INC RESULT SHD=-5
11                      MOV 2,3
12                      ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
13                      COM 3,3,SZR       ;THEN 0
14                      HALT
15                      MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
16                      MOVZL 1,1         ;SET UP RESULT NEXT TEST
17              %
18
19                ;SET UP FIRST CARRY TEST
20 03516 102000         ADC 0,0
21 03517 100000         COM 0,0
22 03520 105140         MOVOL 0,1
23
24                      INCTS 03,ALUCRY,15,0,1
25                ;AC0=0 COMING INTO TEST,+1=AC1=1
26                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
27                ;BITALUCRY INTO BIT15 WITH RESULT=AC1
28              ;INC03:
29 03521 111405         INC 0,2,SNR       ;AC0=0+1 AND BE NON ZERO
30 03522 063077         HALT              ;INC RESULT SHD=1
31 03523 155000         MOV 2,3
32 03524 136000         ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
33 03525 174004         COM 3,3,SZR       ;THEN 0
34 03526 063077         HALT
35 03527 101140         MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
36 03530 125120         MOVZL 1,1         ;SET UP RESULT NEXT TEST
37                      INCTS 04,15,14,1,2
38                ;AC0=1 COMING INTO TEST,+1=AC1=2
39                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
40                ;BIT15 INTO BIT14 WITH RESULT=AC1
41              ;INC04:
42 03531 111405         INC 0,2,SNR       ;AC0=1+1 AND BE NON ZERO
43 03532 063077         HALT              ;INC RESULT SHD=2
44 03533 155000         MOV 2,3
45 03534 136000         ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
46 03535 174004         COM 3,3,SZR       ;THEN 0
47 03536 063077         HALT
48 03537 101140         MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
49 03540 125120         MOVZL 1,1         ;SET UP RESULT NEXT TEST
50                      INCTS 05,14,13,3,4
51                ;AC0=3 COMING INTO TEST,+1=AC1=4
52                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
53                ;BIT14 INTO BIT13 WITH RESULT=AC1
54              ;INC05:
55 03541 111405         INC 0,2,SNR       ;AC0=3+1 AND BE NON ZERO
56 03542 063077         HALT              ;INC RESULT SHD=4
57 03543 155000         MOV 2,3
58 03544 136000         ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
59 03545 174004         COM 3,3,SZR       ;THEN 0
60 03546 063077         HALT
```

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0064 N2LOG
01 03547 101140         MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
02 03550 125120         MOVZL 1,1         ;SET UP RESULT NEXT TEST
03                      INCTS 06,13,12,7,10
04                ;AC0=7 COMING INTO TEST,+1=AC1=10
05                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
06                ;BIT13 INTO BIT12 WITH RESULT=AC1
07              ;INC06:
08 03551 111405         INC 0,2,SNR       ;AC0=7+1 AND BE NON ZERO
09 03552 063077         HALT              ;INC RESULT SHD=10
10 03553 155000         MOV 2,3
11 03554 136000         ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
12 03555 174004         COM 3,3,SZR       ;THEN 0
13 03556 063077         HALT
14 03557 101140         MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
15 03560 125120         MOVZL 1,1         ;SET UP RESULT NEXT TEST
16                      INCTS 07,12,11,17,20
17                ;AC0=17 COMING INTO TEST,+1=AC1=20
18                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
19                ;BIT12 INTO BIT11 WITH RESULT=AC1
20              ;INC07:
21 03561 111405         INC 0,2,SNR       ;AC0=17+1 AND BE NON ZERO
22 03562 063077         HALT              ;INC RESULT SHD=20
23 03563 155000         MOV 2,3
24 03564 136000         ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
25 03565 174004         COM 3,3,SZR       ;THEN 0
26 03566 063077         HALT
27 03567 101140         MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
28 03570 125120         MOVZL 1,1         ;SET UP RESULT NEXT TEST
29                      INCTS 08,11,10,37,40
30                ;AC0=37 COMING INTO TEST,+1=AC1=40
31                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
32                ;BIT11 INTO BIT10 WITH RESULT=AC1
33              ;INC08:
34 03571 111405         INC 0,2,SNR       ;AC0=37+1 AND BE NON ZERO
35 03572 063077         HALT              ;INC RESULT SHD=40
36 03573 155000         MOV 2,3
37 03574 136000         ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
38 03575 174004         COM 3,3,SZR       ;THEN 0
39 03576 063077         HALT
40 03577 101140         MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
41 03600 125120         MOVZL 1,1         ;SET UP RESULT NEXT TEST
42                      INCTS 09,10,9,77,100
43                ;AC0=77 COMING INTO TEST,+1=AC1=100
44                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
45                ;BIT10 INTO BIT9 WITH RESULT=AC1
46              ;INC09:
47 03601 111405         INC 0,2,SNR       ;AC0=77+1 AND BE NON ZERO
48 03602 063077         HALT              ;INC RESULT SHD=100
49 03603 155000         MOV 2,3
50 03604 136000         ADC 1,3           ;ADC SUM OF 1+3 SHD=-1
51 03605 174004         COM 3,3,SZR       ;THEN 0
52 03606 063077         HALT
53 03607 101140         MOVOL 0,0         ;SET UP CONSTANTS NEXT TEST
54 03610 125120         MOVZL 1,1         ;SET UP RESULT NEXT TEST
55                      INCTS 10,9,8,177,200
56                ;AC0=177 COMING INTO TEST,+1=AC1=200
57                ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
58                ;BIT9 INTO BIT8 WITH RESULT=AC1
59              ;INC10:
60 03611 111405         INC 0,2,SNR       ;AC0=177+1 AND BE NON ZERO
```

```
0065 N2LOG
01 03612 063077          HALT                ;INC RESULT SHD=200
02 03613 155000          MOV 2,3
03 03614 136000          ADC 1,3             ;ADC SUM OF 1+3 SHD=-1
04 03615 174004          COM 3,3,SZR         ;THEN 0
05 03616 063077          HALT
06 03617 101140          MOVOL 0,0           ;SET UP CONSTANTS NEXT TEST
07 03620 125120          MOVZL 1,1           ;SET UP RESULT NEXT TEST
08                       INCTS 11,8,7,377,400
09                    ;AC0=377 COMING INTO TEST,+1=AC1=400
10                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
11                    ;BIT8 INTO BIT7 WITH RESULT=AC1
12                 ;INC11:
13 03621 111405          INC 0,2,SNR         ;AC0=377+1 AND BE NON ZERO
14 03622 063077          HALT                ;INC RESULT SHD=400
15 03623 155000          MOV 2,3
16 03624 136000          ADC 1,3             ;ADC SUM OF 1+3 SHD=-1
17 03625 174004          COM 3,3,SZR         ;THEN 0
18 03626 063077          HALT
19 03627 101140          MOVOL 0,0           ;SET UP CONSTANTS NEXT TEST
20 03630 125120          MOVZL 1,1           ;SET UP RESULT NEXT TEST
21                       INCTS 12,7,6,777,1000
22                    ;AC0=777 COMING INTO TEST,+1=AC1=1000
23                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
24                    ;BIT7 INTO BIT6 WITH RESULT=AC1
25                 ;INC12:
26 03631 111405          INC 0,2,SNR         ;AC0=777+1 AND BE NON ZERO
27 03632 063077          HALT                ;INC RESULT SHD=1000
28 03633 155000          MOV 2,3
29 03634 136000          ADC 1,3             ;ADC SUM OF 1+3 SHD=-1
30 03635 174004          COM 3,3,SZR         ;THEN 0
31 03636 063077          HALT
32 03637 101140          MOVOL 0,0           ;SET UP CONSTANTS NEXT TEST
33 03640 125120          MOVZL 1,1           ;SET UP RESULT NEXT TEST
34                       INCTS 13,6,5,1777,2000
35                    ;AC0=1777 COMING INTO TEST,+1=AC1=2000
36                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
37                    ;BIT6 INTO BIT5 WITH RESULT=AC1
38                 ;INC13:
39 03641 111405          INC 0,2,SNR         ;AC0=1777+1 AND BE NON ZERO
40 03642 063077          HALT                ;INC RESULT SHD=2000
41 03643 155000          MOV 2,3
42 03644 136000          ADC 1,3             ;ADC SUM OF 1+3 SHD=-1
43 03645 174004          COM 3,3,SZR         ;THEN 0
44 03646 063077          HALT
45 03647 101140          MOVOL 0,0           ;SET UP CONSTANTS NEXT TEST
46 03650 125120          MOVZL 1,1           ;SET UP RESULT NEXT TEST
47                       INCTS 14,5,4,3777,4000
48                    ;AC0=3777 COMING INTO TEST,+1=AC1=4000
49                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
50                    ;BIT5 INTO BIT4 WITH RESULT=AC1
51                 ;INC14:
52 03651 111405          INC 0,2,SNR         ;AC0=3777+1 AND BE NON ZERO
53 03652 063077          HALT                ;INC RESULT SHD=4000
54 03653 155000          MOV 2,3
55 03654 136000          ADC 1,3             ;ADC SUM OF 1+3 SHD=-1
56 03655 174004          COM 3,3,SZR         ;THEN 0
57 03656 063077          HALT
58 03657 101140          MOVOL 0,0           ;SET UP CONSTANTS NEXT TEST
59 03660 125120          MOVZL 1,1           ;SET UP RESULT NEXT TEST
60                       INCTS 15,4,3,7777,10000
```

```
0066 N2LOG
01                    ;AC0=7777 COMING INTO TEST,+1=AC1=10000
02                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
03                    ;BIT4 INTO BIT3 WITH RESULT=AC1
04                 ;INC15:
05 03661 111405          INC 0,2,SNR         ;AC0=7777+1 AND BE NON ZERO
06 03662 063077          HALT                ;INC RESULT SHD=10000
07 03663 155000          MOV 2,3
08 03664 136000          ADC 1,3             ;ADC SUM OF 1+3 SHD=-1
09 03665 174004          COM 3,3,SZR         ;THEN 0
10 03666 063077          HALT
11 03667 101140          MOVOL 0,0           ;SET UP CONSTANTS NEXT TEST
12 03670 125120          MOVZL 1,1           ;SET UP RESULT NEXT TEST
13                       INCTS 16,3,2,17777,20000
14                    ;AC0=17777 COMING INTO TEST,+1=AC1=20000
15                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
16                    ;BIT3 INTO BIT2 WITH RESULT=AC1
17                 ;INC16:
18 03671 111405          INC 0,2,SNR         ;AC0=17777+1 AND BE NON ZERO
19 03672 063077          HALT                ;INC RESULT SHD=20000
20 03673 155000          MOV 2,3
21 03674 136000          ADC 1,3             ;ADC SUM OF 1+3 SHD=-1
22 03675 174004          COM 3,3,SZR         ;THEN 0
23 03676 063077          HALT
24 03677 101140          MOVOL 0,0           ;SET UP CONSTANTS NEXT TEST
25 03700 125120          MOVZL 1,1           ;SET UP RESULT NEXT TEST
26                       INCTS 17,2,1,37777,40000
27                    ;AC0=37777 COMING INTO TEST,+1=AC1=40000
28                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
29                    ;BIT2 INTO BIT1 WITH RESULT=AC1
30                 ;INC17:
31 03701 111405          INC 0,2,SNR         ;AC0=37777+1 AND BE NON ZERO
32 03702 063077          HALT                ;INC RESULT SHD=40000
33 03703 155000          MOV 2,3
34 03704 136000          ADC 1,3             ;ADC SUM OF 1+3 SHD=-1
35 03705 174004          COM 3,3,SZR         ;THEN 0
36 03706 063077          HALT
37 03707 101140          MOVOL 0,0           ;SET UP CONSTANTS NEXT TEST
38 03710 125120          MOVZL 1,1           ;SET UP RESULT NEXT TEST
39                       INCTS 18,1,0,77777,100000
40                    ;AC0=77777 COMING INTO TEST,+1=AC1=100000
41                    ;INC INSTRUCTION SHOULD CAUSE CARRY THROUGH
42                    ;BIT1 INTO BIT0 WITH RESULT=AC1
43                 ;INC18:
44 03711 111405          INC 0,2,SNR         ;AC0=77777+1 AND BE NON ZERO
45 03712 063077          HALT                ;INC RESULT SHD=100000
46 03713 155000          MOV 2,3
47 03714 136000          ADC 1,3             ;ADC SUM OF 1+3 SHD=-1
48 03715 174004          COM 3,3,SZR         ;THEN 0
49 03716 063077          HALT
50 03717 101140          MOVOL 0,0           ;SET UP CONSTANTS NEXT TEST
51 03720 125120          MOVZL 1,1           ;SET UP RESULT NEXT TEST
```

```
10067 N2LOG
01
02                ;TEST INC OF -1 AC TO=0 WITH CRY COMP 0 TO 1
03 03721 102040 INC20:  ADCO 0,0
04 03722 101424         INCZ 0,0,SZR
05 03723 063077         HALT            ;INC-1 DID NOT=0
06 03724 101003         MOV 0,0,SNC
07 03725 063077         HALT            ;CRY OUT DID NOT COM 0 TO 1
08                ;EXAMINE AC0 FOR ALU FAILURE IF FIRST HALT
09                ;TEST INC OF-1 AC TO=0 AND CRY TO COMP 1 TO 0
10
11 03726 102020 INC21:  ADCZ 0,0
12 03727 101444         INCO 0,0,SZR
13 03730 063077         HALT            ;INC-1 DID NOT=0
14 03731 101002         MOV 0,0,SZC
15 03732 063077         HALT            ;CRY OUT DID NOT COM 1 TO 0
16                ;EXAMINE AC0 FOR ALU FAILURE IF FIRST HALT
```

```
10068 N2LOG
01
02                ;FIRST USE OF NEG INSTRUCTION
03                ;NEG-1 TO -1 TO VERIFY CORRECT INSTR REF
04
05 03733 102000 NEG00:  ADC 0,0
06 03734 100405         NEG 0,0,SNR
07 03735 063077         HALT            ;NEG MAY=COM+INC+SUB
08 03736 105224         MOVZR 0,1,SZR
09 03737 063077         HALT            ;NEG OF -1 SOMETHING OTHER THAN +1
10                ;EXAMINE AC0 FOR ALU ERROR
11
12                ;THE NEGATION OF +1 SHD=-1
13
14 03740 102000 NEG01:  ADC 0,0         ;SET=-1
15 03741 100140         COMOL 0,0       ;MAKES AC0=1
16 03742 100405         NEG 0,0,SNR     ;MAKES AC0=-1
17 03743 063077         HALT            ;(?)
18 03744 104004         COM 0,1,SZR     ;RESULT REALLY=-1
19 03745 063077         HALT            ;NEG OF +1 SOMETHING OTHER THAN -1
20                ;EXAMINE AC0 FOR ALU ERROR OR AC1 FOR COM
21
22                ;DEFINE MACRO FOR FURTHER TESTS OF NEG
23                      .MACRO NEGTS
24                ;AC0=^4 COMING INTO TEST IT SHD NEG TO=^5
25                ;NEG IS EQUIVALENT TO COM+INC
26                ;CARRY IS THROUGH BIT ^2 BUT SHOULD STORE AT BIT ^3
27                ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
28              ;NEG^1:
29                      NEG 0,2,SNR     ;^4+1 SHD=^5
30                      HALT            ;CARRY WENT THROUGH BIT ^3
31                      MOV 2,3
32                      ADC 1,3         ;AC1=COM OF ^5 AC3 SHD=-1
33                      COM 3,3,SZR     ;RESULT COM -1 SHD=0
34                      HALT            ;EXAM AC2 FOR ALU ERR SHD=^5
35                ;AC2=^5 IT SHOULD NEG AGAIN TO=AC0 OR ^4
36              ;NG^1A:
37                      NEG 2,3         ;AC2=^5 3 SHD=^4
38                      ADC 0,3         ;AC3 SHD NOW=-1
39                      COM# 3,3,SZR    ;AND ITS COM=0
40                      HALT            ;^5 DID NOT NEG TO ^4
41                ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF ^4
42                      MOVZL 0,0
43                      MOVZL 1,1       ;SET UP NEXT TEST
44              %
```

```
10069 N2LOG
01
02                      ;SET UP NEG TESTS
03                      ;START WITH AC0=1 AC1=0
04                      ;2ND TEST AC0=2 AC1=1
05
06 03746 120000                 ADC 1,1         ;SET UP AC1=-1
07 03747 120140                 COMOL 1,0       ;AC0=+1
08
09                              NEGTS 03,ALUCRY,15,1,177777
10                      ;AC0=1 COMING INTO TEST IT SHD NEG TO=177777
11                      ;NEG IS EQUIVALENT TO COM+INC
12                      ;CARRY IS THROUGH BIT ALUCRY BUT SHOULD STORE AT BIT 15
13                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
14                    ;NEG03:
15 03750 110405                 NEG 0,2,SNR     ;1+1 SHD=177777
16 03751 063077                 HALT            ;CARRY WENT THROUGH BIT 15
17 03752 155000                 MOV 2,3
18 03753 136000                 ADC 1,3         ;AC1=COM OF 177777 AC3 SHD=-1
19 03754 174004                 COM 3,3,SZR     ;RESULT COM -1 SHD=0
20 03755 063077                 HALT            ;EXAM AC2 FOR ALU ERR SHD=177777
21                      ;AC2=177777 IT SHOULD NEG AGAIN TO=AC0 OR 1
22                    ;NG03A:
23 03756 154400                 NEG 2,3         ;AC2=177777 3 SHD=1
24 03757 116000                 ADC 0,3         ;AC3 SHD NOW=-1
25 03760 174014                 COM# 3,3,SZR    ;AND ITS COM=0
26 03761 063077                 HALT            ;177777 DID NOT NEG TO 1
27                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 1
28 03762 101120                 MOVZL 0,0
29 03763 125120                 MOVZL 1,1       ;SET UP NEXT TEST
30                              NEGTS 04,15,14,2,177776
31                      ;AC0=2 COMING INTO TEST IT SHD NEG TO=177776
32                      ;NEG IS EQUIVALENT TO COM+INC
33                      ;CARRY IS THROUGH BIT 15 BUT SHOULD STORE AT BIT 14
34                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
35                    ;NEG04:
36 03764 110405                 NEG 0,2,SNR     ;2+1 SHD=177776
37 03765 063077                 HALT            ;CARRY WENT THROUGH BIT 14
38 03766 155000                 MOV 2,3
39 03767 136000                 ADC 1,3         ;AC1=COM OF 177776 AC3 SHD=-1
40 03770 174004                 COM 3,3,SZR     ;RESULT COM -1 SHD=0
41 03771 063077                 HALT            ;EXAM AC2 FOR ALU ERR SHD=177776
42                      ;AC2=177776 IT SHOULD NEG AGAIN TO=AC0 OR 2
43                    ;NG04A:
44 03772 154400                 NEG 2,3         ;AC2=177776 3 SHD=2
45 03773 116000                 ADC 0,3         ;AC3 SHD NOW=-1
46 03774 174014                 COM# 3,3,SZR    ;AND ITS COM=0
47 03775 063077                 HALT            ;177776 DID NOT NEG TO 2
48                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 2
49 03776 101120                 MOVZL 0,0
50 03777 125120                 MOVZL 1,1       ;SET UP NEXT TEST
51                              NEGTS 05,14,13,4,177774
52                      ;AC0=4 COMING INTO TEST IT SHD NEG TO=177774
53                      ;NEG IS EQUIVALENT TO COM+INC
54                      ;CARRY IS THROUGH BIT 14 BUT SHOULD STORE AT BIT 13
55                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
56                    ;NEG05:
57 04000 110405                 NEG 0,2,SNR     ;4+1 SHD=177774
58 04001 063077                 HALT            ;CARRY WENT THROUGH BIT 13
59 04002 155000                 MOV 2,3
60 04003 136000                 ADC 1,3         ;AC1=COM OF 177774 AC3 SHD=-1
```

```
0070 N2LOG
01 04004 174004                 COM 3,3,SZR     ;RESULT COM -1 SHD=0
02 04005 063077                 HALT            ;EXAM AC2 FOR ALU ERR SHD=177774
03                      ;AC2=177774 IT SHOULD NEG AGAIN TO=AC0 OR 4
04                    ;NG05A:
05 04006 154400                 NEG 2,3         ;AC2=177774 3 SHD=4
06 04007 116000                 ADC 0,3         ;AC3 SHD NOW=-1
07 04010 174014                 COM# 3,3,SZR    ;AND ITS COM=0
08 04011 063077                 HALT            ;177774 DID NOT NEG TO 4
09                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 4
10 04012 101120                 MOVZL 0,0
11 04013 125120                 MOVZL 1,1       ;SET UP NEXT TEST
12                              NEGTS 06,13,12,10,177770
13                      ;AC0=10 COMING INTO TEST IT SHD NEG TO=177770
14                      ;NEG IS EQUIVALENT TO COM+INC
15                      ;CARRY IS THROUGH BIT 13 BUT SHOULD STORE AT BIT 12
16                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
17                    ;NEG06:
18 04014 110405                 NEG 0,2,SNR     ;10+1 SHD=177770
19 04015 063077                 HALT            ;CARRY WENT THROUGH BIT 12
20 04016 155000                 MOV 2,3
21 04017 136000                 ADC 1,3         ;AC1=COM OF 177770 AC3 SHD=-1
22 04020 174004                 COM 3,3,SZR     ;RESULT COM -1 SHD=0
23 04021 063077                 HALT            ;EXAM AC2 FOR ALU ERR SHD=177770
24                      ;AC2=177770 IT SHOULD NEG AGAIN TO=AC0 OR 10
25                    ;NG06A:
26 04022 154400                 NEG 2,3         ;AC2=177770 3 SHD=10
27 04023 116000                 ADC 0,3         ;AC3 SHD NOW=-1
28 04024 174014                 COM# 3,3,SZR    ;AND ITS COM=0
29 04025 063077                 HALT            ;177770 DID NOT NEG TO 10
30                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 10
31 04026 101120                 MOVZL 0,0
32 04027 125120                 MOVZL 1,1       ;SET UP NEXT TEST
33                              NEGTS 07,12,11,20,177760
34                      ;AC0=20 COMING INTO TEST IT SHD NEG TO=177760
35                      ;NEG IS EQUIVALENT TO COM+INC
36                      ;CARRY IS THROUGH BIT 12 BUT SHOULD STORE AT BIT 11
37                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
38                    ;NEG07:
39 04030 110405                 NEG 0,2,SNR     ;20+1 SHD=177760
40 04031 063077                 HALT            ;CARRY WENT THROUGH BIT 11
41 04032 155000                 MOV 2,3
42 04033 136000                 ADC 1,3         ;AC1=COM OF 177760 AC3 SHD=-1
43 04034 174004                 COM 3,3,SZR     ;RESULT COM -1 SHD=0
44 04035 063077                 HALT            ;EXAM AC2 FOR ALU ERR SHD=177760
45                      ;AC2=177760 IT SHOULD NEG AGAIN TO=AC0 OR 20
46                    ;NG07A:
47 04036 154400                 NEG 2,3         ;AC2=177760 3 SHD=20
48 04037 116000                 ADC 0,3         ;AC3 SHD NOW=-1
49 04040 174014                 COM# 3,3,SZR    ;AND ITS COM=0
50 04041 063077                 HALT            ;177760 DID NOT NEG TO 20
51                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 20
52 04042 101120                 MOVZL 0,0
53 04043 125120                 MOVZL 1,1       ;SET UP NEXT TEST
54                              NEGTS 08,11,10,40,177740
55                      ;AC0=40 COMING INTO TEST IT SHD NEG TO=177740
56                      ;NEG IS EQUIVALENT TO COM+INC
57                      ;CARRY IS THROUGH BIT 11 BUT SHOULD STORE AT BIT 10
58                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
59                    ;NEG08:
60 04044 110405                 NEG 0,2,SNR     ;40+1 SHD=177740
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0071 N2LOG
04045 063077          HALT              ;CARRY WENT THROUGH BIT 10
04046 155000          MOV 2,3
04047 136000          ADC 1,3           ;AC1=COM OF 177740 AC3 SHD=-1
04050 174004          COM 3,3,SZR       ;RESULT COM -1 SHD=0
04051 063077          HALT              ;EXAM AC2 FOR ALU ERR SHD=177740
                    ;AC2=177740 IT SHOULD NEG AGAIN TO=AC0 OR 40
                   ;NG08A:
04052 154400          NEG 2,3           ;AC2=177740 3 SHD=40
04053 116000          ADC 0,3           ;AC3 SHD NOW=-1
04054 174014          COM# 3,3,SZR      ;AND ITS COM=0
04055 063077          HALT              ;177740 DID NOT NEG TO 40
                    ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 40
04056 101120          MOVZL 0,0
04057 125120          MOVZL 1,1         ;SET UP NEXT TEST
                      NEGTS 09,10,9,100,177700
                    ;AC0=100 COMING INTO TEST IT SHD NEG TO=177700
                    ;NEG IS EQUIVALENT TO COM+INC
                    ;CARRY IS THROUGH BIT 10 BUT SHOULD STORE AT BIT 9
                    ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
                   ;NEG09:
04060 110405          NEG 0,2,SNR       ;100+1 SHD=177700
04061 063077          HALT              ;CARRY WENT THROUGH BIT 9
04062 155000          MOV 2,3
04063 136000          ADC 1,3           ;AC1=COM OF 177700 AC3 SHD=-1
04064 174004          COM 3,3,SZR       ;RESULT COM -1 SHD=0
04065 063077          HALT              ;EXAM AC2 FOR ALU ERR SHD=177700
                    ;AC2=177700 IT SHOULD NEG AGAIN TO=AC0 OR 100
                   ;NG09A:
04066 154400          NEG 2,3           ;AC2=177700 3 SHD=100
04067 116000          ADC 0,3           ;AC3 SHD NOW=-1
04070 174014          COM# 3,3,SZR      ;AND ITS COM=0
04071 063077          HALT              ;177700 DID NOT NEG TO 100
                    ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 100
04072 101120          MOVZL 0,0
04073 125120          MOVZL 1,1         ;SET UP NEXT TEST
                      NEGTS 10,9,8,200,177600
                    ;AC0=200 COMING INTO TEST IT SHD NEG TO=177600
                    ;NEG IS EQUIVALENT TO COM+INC
                    ;CARRY IS THROUGH BIT 9 BUT SHOULD STORE AT BIT 8
                    ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
                   ;NEG10:
04074 110405          NEG 0,2,SNR       ;200+1 SHD=177600
04075 063077          HALT              ;CARRY WENT THROUGH BIT 8
04076 155000          MOV 2,3
04077 136000          ADC 1,3           ;AC1=COM OF 177600 AC3 SHD=-1
04100 174004          COM 3,3,SZR       ;RESULT COM -1 SHD=0
04101 063077          HALT              ;EXAM AC2 FOR ALU ERR SHD=177600
                    ;AC2=177600 IT SHOULD NEG AGAIN TO=AC0 OR 200
                   ;NG10A:
04102 154400          NEG 2,3           ;AC2=177600 3 SHD=200
04103 116000          ADC 0,3           ;AC3 SHD NOW=-1
04104 174014          COM# 3,3,SZR      ;AND ITS COM=0
04105 063077          HALT              ;177600 DID NOT NEG TO 200
                    ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 200
04106 101120          MOVZL 0,0
04107 125120          MOVZL 1,1         ;SET UP NEXT TEST
                      NEGTS 11,8,7,400,177400
                    ;AC0=400 COMING INTO TEST IT SHD NEG TO=177400
                    ;NEG IS EQUIVALENT TO COM+INC
                    ;CARRY IS THROUGH BIT 8 BUT SHOULD STORE AT BIT 7
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0072 N2LOG
                    ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
                   ;NEG11:
04110 110405          NEG 0,2,SNR       ;400+1 SHD=177400
04111 063077          HALT              ;CARRY WENT THROUGH BIT 7
04112 155000          MOV 2,3
04113 136000          ADC 1,3           ;AC1=COM OF 177400 AC3 SHD=-1
04114 174004          COM 3,3,SZR       ;RESULT COM -1 SHD=0
04115 063077          HALT              ;EXAM AC2 FOR ALU ERR SHD=177400
                    ;AC2=177400 IT SHOULD NEG AGAIN TO=AC0 OR 400
                   ;NG11A:
04116 154400          NEG 2,3           ;AC2=177400 3 SHD=400
04117 116000          ADC 0,3           ;AC3 SHD NOW=-1
04120 174014          COM# 3,3,SZR      ;AND ITS COM=0
04121 063077          HALT              ;177400 DID NOT NEG TO 400
                    ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 400
04122 101120          MOVZL 0,0
04123 125120          MOVZL 1,1         ;SET UP NEXT TEST
                      NEGTS 12,7,6,100,177000
                    ;AC0=100 COMING INTO TEST IT SHD NEG TO=177000
                    ;NEG IS EQUIVALENT TO COM+INC
                    ;CARRY IS THROUGH BIT 7 BUT SHOULD STORE AT BIT 6
                    ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
                   ;NEG12:
04124 110405          NEG 0,2,SNR       ;100+1 SHD=177000
04125 063077          HALT              ;CARRY WENT THROUGH BIT 6
04126 155000          MOV 2,3
04127 136000          ADC 1,3           ;AC1=COM OF 177000 AC3 SHD=-1
04130 174004          COM 3,3,SZR       ;RESULT COM -1 SHD=0
04131 063077          HALT              ;EXAM AC2 FOR ALU ERR SHD=177000
                    ;AC2=177000 IT SHOULD NEG AGAIN TO=AC0 OR 100
                   ;NG12A:
04132 154400          NEG 2,3           ;AC2=177000 3 SHD=100
04133 116000          ADC 0,3           ;AC3 SHD NOW=-1
04134 174014          COM# 3,3,SZR      ;AND ITS COM=0
04135 063077          HALT              ;177000 DID NOT NEG TO 100
                    ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 100
04136 101120          MOVZL 0,0
04137 125120          MOVZL 1,1         ;SET UP NEXT TEST
                      NEGTS 13,6,5,2000,176000
                    ;AC0=2000 COMING INTO TEST IT SHD NEG TO=176000
                    ;NEG IS EQUIVALENT TO COM+INC
                    ;CARRY IS THROUGH BIT 6 BUT SHOULD STORE AT BIT 5
                    ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
                   ;NEG13:
04140 110405          NEG 0,2,SNR       ;2000+1 SHD=176000
04141 063077          HALT              ;CARRY WENT THROUGH BIT 5
04142 155000          MOV 2,3
04143 136000          ADC 1,3           ;AC1=COM OF 176000 AC3 SHD=-1
04144 174004          COM 3,3,SZR       ;RESULT COM -1 SHD=0
04145 063077          HALT              ;EXAM AC2 FOR ALU ERR SHD=176000
                    ;AC2=176000 IT SHOULD NEG AGAIN TO=AC0 OR 2000
                   ;NG13A:
04146 154400          NEG 2,3           ;AC2=176000 3 SHD=2000
04147 116000          ADC 0,3           ;AC3 SHD NOW=-1
04150 174014          COM# 3,3,SZR      ;AND ITS COM=0
04151 063077          HALT              ;176000 DID NOT NEG TO 2000
                    ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 2000
04152 101120          MOVZL 0,0
04153 125120          MOVZL 1,1         ;SET UP NEXT TEST
                      NEGTS 14,5,4,4000,174000
```

```
0073 N2LOG
01                      ;AC0=4000 COMING INTO TEST IT SHD NEG TO=174000
02                      ;NEG IS EQUIVALENT TO COM+INC
03                      ;CARRY IS THROUGH BIT 5 BUT SHOULD STORE AT BIT 4
04                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
05                    ;NEG14:
06 04154 110405               NEG 0,2,SNR       ;4000+1 SHD=174000
07 04155 063077               HALT              ;CARRY WENT THROUGH BIT 4
08 04156 155000               MOV 2,3
09 04157 136000               ADC 1,3           ;AC1=COM OF 174000 AC3 SHD=-1
10 04160 174004               COM 3,3,SZR       ;RESULT COM -1 SHD=0
11 04161 063077               HALT              ;EXAM AC2 FOR ALU ERR SHD=174000
12                      ;AC2=174000 IT SHOULD NEG AGAIN TO=AC0 OR 4000
13                    ;NG14A:
14 04162 154400               NEG 2,3           ;AC2=174000 3 SHD=4000
15 04163 116000               ADC 0,3           ;AC3 SHD NOW=-1
16 04164 174014               COM# 3,3,SZR      ;AND ITS COM=0
17 04165 063077               HALT              ;174000 DID NOT NEG TO 4000
18                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 4000
19 04166 101120               MOVZL 0,0
20 04167 125120               MOVZL 1,1         ;SET UP NEXT TEST
21                            NEGTS 15,4,3,10000,170000
22                      ;AC0=10000 COMING INTO TEST IT SHD NEG TO=170000
23                      ;NEG IS EQUIVALENT TO COM+INC
24                      ;CARRY IS THROUGH BIT 4 BUT SHOULD STORE AT BIT 3
25                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
26                    ;NEG15:
27 04170 110405               NEG 0,2,SNR       ;10000+1 SHD=170000
28 04171 063077               HALT              ;CARRY WENT THROUGH BIT 3
29 04172 155000               MOV 2,3
30 04173 136000               ADC 1,3           ;AC1=COM OF 170000 AC3 SHD=-1
31 04174 174004               COM 3,3,SZR       ;RESULT COM -1 SHD=0
32 04175 063077               HALT              ;EXAM AC2 FOR ALU ERR SHD=170000
33                      ;AC2=170000 IT SHOULD NEG AGAIN TO=AC0 OR 10000
34                    ;NG15A:
35 04176 154400               NEG 2,3           ;AC2=170000 3 SHD=10000
36 04177 116000               ADC 0,3           ;AC3 SHD NOW=-1
37 04200 174014               COM# 3,3,SZR      ;AND ITS COM=0
38 04201 063077               HALT              ;170000 DID NOT NEG TO 10000
39                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 10000
40 04202 101120               MOVZL 0,0
41 04203 125120               MOVZL 1,1         ;SET UP NEXT TEST
42                            NEGTS 16,3,1,20000,160000
43                      ;AC0=20000 COMING INTO TEST IT SHD NEG TO=160000
44                      ;NEG IS EQUIVALENT TO COM+INC
45                      ;CARRY IS THROUGH BIT 3 BUT SHOULD STORE AT BIT 1
46                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
47                    ;NEG16:
48 04204 110405               NEG 0,2,SNR       ;20000+1 SHD=160000
49 04205 063077               HALT              ;CARRY WENT THROUGH BIT 1
50 04206 155000               MOV 2,3
51 04207 136000               ADC 1,3           ;AC1=COM OF 160000 AC3 SHD=-1
52 04210 174004               COM 3,3,SZR       ;RESULT COM -1 SHD=0
53 04211 063077               HALT              ;EXAM AC2 FOR ALU ERR SHD=160000
54                      ;AC2=160000 IT SHOULD NEG AGAIN TO=AC0 OR 20000
55                    ;NG16A:
56 04212 154400               NEG 2,3           ;AC2=160000 3 SHD=20000
57 04213 116000               ADC 0,3           ;AC3 SHD NOW=-1
58 04214 174014               COM# 3,3,SZR      ;AND ITS COM=0
59 04215 063077               HALT              ;160000 DID NOT NEG TO 20000
60                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 20000
```

```
0074 N2LOG
01 04216 101120               MOVZL 0,0
02 04217 125120               MOVZL 1,1         ;SET UP NEXT TEST
03                            NEGTS 17,2,1,40000,140000
04                      ;AC0=40000 COMING INTO TEST IT SHD NEG TO=140000
05                      ;NEG IS EQUIVALENT TO COM+INC
06                      ;CARRY IS THROUGH BIT 2 BUT SHOULD STORE AT BIT 1
07                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
08                    ;NEG17:
09 04220 110405               NEG 0,2,SNR       ;40000+1 SHD=140000
10 04221 063077               HALT              ;CARRY WENT THROUGH BIT 1
11 04222 155000               MOV 2,3
12 04223 136000               ADC 1,3           ;AC1=COM OF 140000 AC3 SHD=-1
13 04224 174004               COM 3,3,SZR       ;RESULT COM -1 SHD=0
14 04225 063077               HALT              ;EXAM AC2 FOR ALU ERR SHD=140000
15                      ;AC2=140000 IT SHOULD NEG AGAIN TO=AC0 OR 40000
16                    ;NG17A:
17 04226 154400               NEG 2,3           ;AC2=140000 3 SHD=40000
18 04227 116000               ADC 0,3           ;AC3 SHD NOW=-1
19 04230 174014               COM# 3,3,SZR      ;AND ITS COM=0
20 04231 063077               HALT              ;140000 DID NOT NEG TO 40000
21                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 40000
22 04232 101120               MOVZL 0,0
23 04233 125120               MOVZL 1,1         ;SET UP NEXT TEST
24                            NEGTS 18,1,0,100000,100000
25                      ;AC0=100000 COMING INTO TEST IT SHD NEG TO=100000
26                      ;NEG IS EQUIVALENT TO COM+INC
27                      ;CARRY IS THROUGH BIT 1 BUT SHOULD STORE AT BIT 0
28                      ;AND HIGHER ORDER BITS SHOULD REMAIN 1'S
29                    ;NEG18:
30 04234 110405               NEG 0,2,SNR       ;100000+1 SHD=100000
31 04235 063077               HALT              ;CARRY WENT THROUGH BIT 0
32 04236 155000               MOV 2,3
33 04237 136000               ADC 1,3           ;AC1=COM OF 100000 AC3 SHD=-1
34 04240 174004               COM 3,3,SZR       ;RESULT COM -1 SHD=0
35 04241 063077               HALT              ;EXAM AC2 FOR ALU ERR SHD=100000
36                      ;AC2=100000 IT SHOULD NEG AGAIN TO=AC0 OR 100000
37                    ;NG18A:
38 04242 154400               NEG 2,3           ;AC2=100000 3 SHD=100000
39 04243 116000               ADC 0,3           ;AC3 SHD NOW=-1
40 04244 174014               COM# 3,3,SZR      ;AND ITS COM=0
41 04245 063077               HALT              ;100000 DID NOT NEG TO 100000
42                      ;EXAMINE AC3 FOR ALU FAILURE SHD=-1 CREATED BY ADC OF 100000
43 04246 101120               MOVZL 0,0
44 04247 125120               MOVZL 1,1         ;SET UP NEXT TEST
```

```
                        ;0075 N2LOG
                        ;
                                        ;AC0=0 COMING INTO TEST IT SHD NEG TO =0
                        ;
                                        ;CARRY IS THROUGH BIT 0 AND SHOULD COM CRY
                        ;
000425 110404 NEG19:    NEG 0,2,SZR     ;-0+1=0
000426 063077           HALT            ;SEE AC2 NOT=0
000427 155000           MOV 2,3
000430 130000           ADC 1,3
000431 174004           COM 3,3,SZR     ;SKP AC2 REALLY=0
000432 063077           HALT            ;SEE AC2 SHD =0
                        ;
                                        ;AC2 =0 IT SHD NEGATE TO =0 IN AC3
                        ;
000433 154400 NG19A:    NEG 2,3
000434 116000           ADC 0,3
000435 174014           COM# 3,3,SZR
000436 063077           HALT            ;0 DID NOT NEG TO 0
                        ;EXAMINE AC3 FOR ALU FAILURE SHD =-1 CREATED BY ADC OF 0
                        ;
                        ;
                          ;NEGATING 0 SHOULD COMPLIMENT CRY 0 TO 1
                        ;
000437 102000 NEG20:    ADC 0,0
000440 100040           COMO 0,0
000441 100423           NEGZ 0,0,SNC
000442 063077           HALT            ;NEG 0 DID NOT SET CRY
                        ;
                          ;NEGATING 0 SHOULD COM CRY 1 TO 0
                        ;
000443 102000 NEG21:    ADC 0,0
000444 100020           COMZ 0,0
000445 100442           NEGO 0,0,SZC
000446 063077           HALT            ;NEG 0 DID NOT CLR CRY
```

```
                        ;0076 N2LOG
                        ;
                          ;TEST FOR EXISTANCE OF SUB INSTRUCTION
                          ;FIRST TIME FOR SUB
                        ;
000447 102000 SUB00:    ADC 0,0         ;AC0=-1
000450 102404           SUB 0,0,SZR     ;SUB -1 FROM -1
000451 063077           HALT            ;EXAMINE AC0 FOR ERR SHD=0
                        ;SUBTRACT +1 FROM +1 CHECK FOR 0 RESULT (2NO SUB)
000452 102000 SUB01:    ADC 0,0
000453 100405           NEG 0,0,SNR     ;SET AC0=+1
000454 063077           HALT            ;SET UP FAILED AC0 SHD=+1
000455 102404           SUB 0,0,SZR     ;+1-+1 SHD=0
000456 063077           HALT            ;SUB +1-+1 FAILED SEE AC0
                        ;
                          ;DEFINE SUBTRACT "SUB" TEST MACRO
                        ;
                          .MACRO SUBTS
                        ;AC0=A2 COMING INTO THIS TEST A2-A2 SHOULD=0 RESULT
                        ;0-A2 NEGATED-A2 SHD=0 INTO AC3
                        ;SUBA1:
                          MOVO 0,1
                          SUBZ 0,1,SZR
                          HALT            ;A2-A2 SEE AC1 SHD=0
                          MOV 0,0,SKN     ;0 CRY SHD =1 FROM CRYOUT
                          HALT    ;AC0=A2(?) CRY SHD=1
                          ADC 2,2
                          COM 2,2 ;MAKE AC2=0 FOR TEST
                        ;0-A2 SHOULD=-A2 NEGATED TO AC3
                          SUB 0,2         ;0-A2
                          NEGZ 2,3        ;NEGATED SHD=A2
                          SUBO 0,3,SZR    ;A2-A2 SHD=0 AGAIN
                          HALT
                          MOV 0,0,SZC     ;CRY SHD COMP 1 TO 0
                          HALT            ;CRY OUT FAILED
                          MOVZL 0,0       ;SET UP NEXT TEST
                        %
                        ;
                        ;SET UP SUBTRACT TESTS
000457 102000           ADC 0,0
000460 100140           COMOL 0,0
```

```
10077 N2LOG
01
02                      SUBTS 02,1
03                    ;AC0=1 COMING INTO THIS TEST 1-1 SHOULD=0 RESULT
04                    ;0-1 NEGATED-1 SHD=0 INTO AC3
05                  ;SUB02:
06 04304 105040         MOVO 0,1
07 04305 106424         SUBZ 0,1,SZR
08 04306 063077         HALT                ;1-1 SEE AC1 SHD=0
09 04307 101007         MOV 0,0,SBN         ;0 CRY SHD =1 FROM CRYOUT
10 04310 063077         HALT      ;AC0=1(?) CRY SHD=1
11 04311 152000         ADC 2,2
12 04312 150000         COM 2,2 ;MAKE AC2=0 FOR TEST
13                    ;0-1 SHOULD=-1 NEGATED TO AC3
14 04313 112400         SUB 0,2             ;0-1
15 04314 154420         NEGZ 2,3            ;NEGATED SHD=1
16 04315 116444         SUBO 0,3,SZR        ;1-1 SHD=0 AGAIN
17 04316 063077         HALT
18 04317 101002         MOV 0,0,SZC         ;CRY SHD COMP 1 TO 0
19 04320 063077         HALT                ;CRY OUT FAILED
20 04321 101120         MOVZL 0,0           ;SET UP NEXT TEST
21                      SUBTS 03,2
22                    ;AC0=2 COMING INTO THIS TEST 2-2 SHOULD=0 RESULT
23                    ;0-2 NEGATED-2 SHD=0 INTO AC3
24                  ;SUB03:
25 04322 105040         MOVO 0,1
26 04323 106424         SUBZ 0,1,SZR
27 04324 063077         HALT                ;2-2 SEE AC1 SHD=0
28 04325 101007         MOV 0,0,SBN         ;0 CRY SHD =1 FROM CRYOUT
29 04326 063077         HALT      ;AC0=2(?) CRY SHD=1
30 04327 152000         ADC 2,2
31 04330 150000         COM 2,2 ;MAKE AC2=0 FOR TEST
32                    ;0-2 SHOULD=-2 NEGATED TO AC3
33 04331 112400         SUB 0,2             ;0-2
34 04332 154420         NEGZ 2,3            ;NEGATED SHD=2
35 04333 116444         SUBO 0,3,SZR        ;2-2 SHD=0 AGAIN
36 04334 063077         HALT
37 04335 101002         MOV 0,0,SZC         ;CRY SHD COMP 1 TO 0
38 04336 063077         HALT                ;CRY OUT FAILED
39 04337 101120         MOVZL 0,0           ;SET UP NEXT TEST
40                      SUBTS 04,4
41                    ;AC0=4 COMING INTO THIS TEST 4-4 SHOULD=0 RESULT
42                    ;0-4 NEGATED-4 SHD=0 INTO AC3
43                  ;SUB04:
44 04340 105040         MOVO 0,1
45 04341 106424         SUBZ 0,1,SZR
46 04342 063077         HALT                ;4-4 SEE AC1 SHD=0
47 04343 101007         MOV 0,0,SBN         ;0 CRY SHD =1 FROM CRYOUT
48 04344 063077         HALT      ;AC0=4(?) CRY SHD=1
49 04345 152000         ADC 2,2
50 04346 150000         COM 2,2 ;MAKE AC2=0 FOR TEST
51                    ;0-4 SHOULD=-4 NEGATED TO AC3
52 04347 112400         SUB 0,2             ;0-4
53 04350 154420         NEGZ 2,3            ;NEGATED SHD=4
54 04351 116444         SUBO 0,3,SZR        ;4-4 SHD=0 AGAIN
55 04352 063077         HALT
56 04353 101002         MOV 0,0,SZC         ;CRY SHD COMP 1 TO 0
57 04354 063077         HALT                ;CRY OUT FAILED
58 04355 101120         MOVZL 0,0           ;SET UP NEXT TEST
59                      SUBTS 05,10
60                    ;AC0=10 COMING INTO THIS TEST 10-10 SHOULD=0 RESULT
```

```
 0078 N2LOG
01                    ;0-10 NEGATED-10 SHD=0 INTO AC3
02                  ;SUB05:
03 04356 105040         MOVO 0,1
04 04357 106424         SUBZ 0,1,SZR
05 04360 063077         HALT                ;10-10 SEE AC1 SHD=0
06 04361 101007         MOV 0,0,SBN         ;0 CRY SHD =1 FROM CRYOUT
07 04362 063077         HALT      ;AC0=10(?) CRY SHD=1
08 04363 152000         ADC 2,2
09 04364 150000         COM 2,2 ;MAKE AC2=0 FOR TEST
10                    ;0-10 SHOULD=-10 NEGATED TO AC3
11 04365 112400         SUB 0,2             ;0-10
12 04366 154420         NEGZ 2,3            ;NEGATED SHD=10
13 04367 116444         SUBO 0,3,SZR        ;10-10 SHD=0 AGAIN
14 04370 063077         HALT
15 04371 101002         MOV 0,0,SZC         ;CRY SHD COMP 1 TO 0
16 04372 063077         HALT                ;CRY OUT FAILED
17 04373 101120         MOVZL 0,0           ;SET UP NEXT TEST
18                      SUBTS 06,20
19                    ;AC0=20 COMING INTO THIS TEST 20-20 SHOULD=0 RESULT
20                    ;0-20 NEGATED-20 SHD=0 INTO AC3
21                  ;SUB06:
22 04374 105040         MOVO 0,1
23 04375 106424         SUBZ 0,1,SZR
24 04376 063077         HALT                ;20-20 SEE AC1 SHD=0
25 04377 101007         MOV 0,0,SBN         ;0 CRY SHD =1 FROM CRYOUT
26 04400 063077         HALT      ;AC0=20(?) CRY SHD=1
27 04401 152000         ADC 2,2
28 04402 150000         COM 2,2 ;MAKE AC2=0 FOR TEST
29                    ;0-20 SHOULD=-20 NEGATED TO AC3
30 04403 112400         SUB 0,2             ;0-20
31 04404 154420         NEGZ 2,3            ;NEGATED SHD=20
32 04405 116444         SUBO 0,3,SZR        ;20-20 SHD=0 AGAIN
33 04406 063077         HALT
34 04407 101002         MOV 0,0,SZC         ;CRY SHD COMP 1 TO 0
35 04410 063077         HALT                ;CRY OUT FAILED
36 04411 101120         MOVZL 0,0           ;SET UP NEXT TEST
37                      SUBTS 07,40
38                    ;AC0=40 COMING INTO THIS TEST 40-40 SHOULD=0 RESULT
39                    ;0-40 NEGATED-40 SHD=0 INTO AC3
40                  ;SUB07:
41 04412 105040         MOVO 0,1
42 04413 106424         SUBZ 0,1,SZR
43 04414 063077         HALT                ;40-40 SEE AC1 SHD=0
44 04415 101007         MOV 0,0,SBN         ;0 CRY SHD =1 FROM CRYOUT
45 04416 063077         HALT      ;AC0=40(?) CRY SHD=1
46 04417 152000         ADC 2,2
47 04420 150000         COM 2,2 ;MAKE AC2=0 FOR TEST
48                    ;0-40 SHOULD=-40 NEGATED TO AC3
49 04421 112400         SUB 0,2             ;0-40
50 04422 154420         NEGZ 2,3            ;NEGATED SHD=40
51 04423 116444         SUBO 0,3,SZR        ;40-40 SHD=0 AGAIN
52 04424 063077         HALT
53 04425 101002         MOV 0,0,SZC         ;CRY SHD COMP 1 TO 0
54 04426 063077         HALT                ;CRY OUT FAILED
55 04427 101120         MOVZL 0,0           ;SET UP NEXT TEST
56                      SUBTS 08,100
57                    ;AC0=100 COMING INTO THIS TEST 100-100 SHOULD=0 RESULT
58                    ;0-100 NEGATED-100 SHD=0 INTO AC3
59                  ;SUB08:
60 04430 105040         MOVO 0,1
```

```
0079 N2LOG
01 04431 106424          SUBZ 0,1,SZR
02 04432 063077          HALT              ;100-100 SEE AC1 SHD=0
03 04433 101007          MOV 0,0,SBN       ;0 CRY SHD =1 FROM CRYOUT
04 04434 063077          HALT     ;AC0=100(?) CRY SHD=1
05 04435 152000          ADC 2,2
06 04436 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
07                  ;0-100 SHOULD=-100 NEGATED TO AC3
08 04437 112400          SUB 0,2           ;0-100
09 04440 154420          NEGZ 2,3          ;NEGATED SHD=100
10 04441 116444          SUBO 0,3,SZR      ;100-100 SHD=0 AGAIN
11 04442 063077          HALT
12 04443 101002          MOV 0,0,SZC       ;CRY SHD COMP 1 TO 0
13 04444 063077          HALT              ;CRY OUT FAILED
14 04445 101120          MOVZL 0,0         ;SET UP NEXT TEST
15                       SUBTS 09,200
16                  ;AC0=200 COMING INTO THIS TEST 200-200 SHOULD=0 RESULT
17                  ;0-200 NEGATED-200 SHD=0 INTO AC3
18                 ;SUB09:
19 04446 105040          MOVO 0,1
20 04447 106424          SUBZ 0,1,SZR
21 04450 063077          HALT              ;200-200 SEE AC1 SHD=0
22 04451 101007          MOV 0,0,SBN       ;0 CRY SHD =1 FROM CRYOUT
23 04452 063077          HALT     ;AC0=200(?) CRY SHD=1
24 04453 152000          ADC 2,2
25 04454 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
26                  ;0-200 SHOULD=-200 NEGATED TO AC3
27 04455 112400          SUB 0,2           ;0-200
28 04456 154420          NEGZ 2,3          ;NEGATED SHD=200
29 04457 116444          SUBO 0,3,SZR      ;200-200 SHD=0 AGAIN
30 04460 063077          HALT
31 04461 101002          MOV 0,0,SZC       ;CRY SHD COMP 1 TO 0
32 04462 063077          HALT              ;CRY OUT FAILED
33 04463 101120          MOVZL 0,0         ;SET UP NEXT TEST
34                       SUBTS 10,400
35                  ;AC0=400 COMING INTO THIS TEST 400-400 SHOULD=0 RESULT
36                  ;0-400 NEGATED-400 SHD=0 INTO AC3
37                 ;SUB10:
38 04464 105040          MOVO 0,1
39 04465 106424          SUBZ 0,1,SZR
40 04466 063077          HALT              ;400-400 SEE AC1 SHD=0
41 04467 101007          MOV 0,0,SBN       ;0 CRY SHD =1 FROM CRYOUT
42 04470 063077          HALT     ;AC0=400(?) CRY SHD=1
43 04471 152000          ADC 2,2
44 04472 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
45                  ;0-400 SHOULD=-400 NEGATED TO AC3
46 04473 112400          SUB 0,2           ;0-400
47 04474 154420          NEGZ 2,3          ;NEGATED SHD=400
48 04475 116444          SUBO 0,3,SZR      ;400-400 SHD=0 AGAIN
49 04476 063077          HALT
50 04477 101002          MOV 0,0,SZC       ;CRY SHD COMP 1 TO 0
51 04500 063077          HALT              ;CRY OUT FAILED
52 04501 101120          MOVZL 0,0         ;SET UP NEXT TEST
53                       SUBTS 11,1000
54                  ;AC0=1000 COMING INTO THIS TEST 1000-1000 SHOULD=0 RESULT
55                  ;0-1000 NEGATED-1000 SHD=0 INTO AC3
56                 ;SUB11:
57 04502 105040          MOVO 0,1
58 04503 106424          SUBZ 0,1,SZR
59 04504 063077          HALT              ;1000-1000 SEE AC1 SHD=0
60 04505 101007          MOV 0,0,SBN       ;0 CRY SHD =1 FROM CRYOUT
```

```
0080 N2LOG
01 04506 063077          HALT     ;AC0=1000(?) CRY SHD=1
02 04507 152000          ADC 2,2
03 04510 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
04                  ;0-1000 SHOULD=-1000 NEGATED TO AC3
05 04511 112400          SUB 0,2           ;0-1000
06 04512 154420          NEGZ 2,3          ;NEGATED SHD=1000
07 04513 116444          SUBO 0,3,SZR      ;1000-1000 SHD=0 AGAIN
08 04514 063077          HALT
09 04515 101002          MOV 0,0,SZC       ;CRY SHD COMP 1 TO 0
10 04516 063077          HALT              ;CRY OUT FAILED
11 04517 101120          MOVZL 0,0         ;SET UP NEXT TEST
12                       SUBTS 12,2000
13                  ;AC0=2000 COMING INTO THIS TEST 2000-2000 SHOULD=0 RESULT
14                  ;0-2000 NEGATED-2000 SHD=0 INTO AC3
15                 ;SUB12:
16 04520 105040          MOVO 0,1
17 04521 106424          SUBZ 0,1,SZR
18 04522 063077          HALT              ;2000-2000 SEE AC1 SHD=0
19 04523 101007          MOV 0,0,SBN       ;0 CRY SHD =1 FROM CRYOUT
20 04524 063077          HALT     ;AC0=2000(?) CRY SHD=1
21 04525 152000          ADC 2,2
22 04526 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
23                  ;0-2000 SHOULD=-2000 NEGATED TO AC3
24 04527 112400          SUB 0,2           ;0-2000
25 04530 154420          NEGZ 2,3          ;NEGATED SHD=2000
26 04531 116444          SUBO 0,3,SZR      ;2000-2000 SHD=0 AGAIN
27 04532 063077          HALT
28 04533 101002          MOV 0,0,SZC       ;CRY SHD COMP 1 TO 0
29 04534 063077          HALT              ;CRY OUT FAILED
30 04535 101120          MOVZL 0,0         ;SET UP NEXT TEST
31                       SUBTS 13,4000
32                  ;AC0=4000 COMING INTO THIS TEST 4000-4000 SHOULD=0 RESULT
33                  ;0-4000 NEGATED-4000 SHD=0 INTO AC3
34                 ;SUB13:
35 04536 105040          MOVO 0,1
36 04537 106424          SUBZ 0,1,SZR
37 04540 063077          HALT              ;4000-4000 SEE AC1 SHD=0
38 04541 101007          MOV 0,0,SBN       ;0 CRY SHD =1 FROM CRYOUT
39 04542 063077          HALT     ;AC0=4000(?) CRY SHD=1
40 04543 152000          ADC 2,2
41 04544 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
42                  ;0-4000 SHOULD=-4000 NEGATED TO AC3
43 04545 112400          SUB 0,2           ;0-4000
44 04546 154420          NEGZ 2,3          ;NEGATED SHD=4000
45 04547 116444          SUBO 0,3,SZR      ;4000-4000 SHD=0 AGAIN
46 04550 063077          HALT
47 04551 101002          MOV 0,0,SZC       ;CRY SHD COMP 1 TO 0
48 04552 063077          HALT              ;CRY OUT FAILED
49 04553 101120          MOVZL 0,0         ;SET UP NEXT TEST
50                       SUBTS 14,10000
51                  ;AC0=10000 COMING INTO THIS TEST 10000-10000 SHOULD=0 RESULT
52                  ;0-10000 NEGATED-10000 SHD=0 INTO AC3
53                 ;SUB14:
54 04554 105040          MOVO 0,1
55 04555 106424          SUBZ 0,1,SZR
56 04556 063077          HALT              ;10000-10000 SEE AC1 SHD=0
57 04557 101007          MOV 0,0,SBN       ;0 CRY SHD =1 FROM CRYOUT
58 04560 063077          HALT     ;AC0=10000(?) CRY SHD=1
59 04561 152000          ADC 2,2
60 04562 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
```

```
0081 N2LOG
01
02 04563 112400          ;0-10000 SHOULD=-10000 NEGATED TO AC3
03 04564 154420          SUB 0,2          ;0-10000
04 04565 116444          NEGZ 2,3         ;NEGATED SHD=10000
05 04566 063077          SUBO 0,3,SZR     ;10000-10000 SHD=0 AGAIN
06 04567 101002          HALT
07 04570 063077          MOV 0,0,SZC      ;CRY SHD COMP 1 TO 0
08 04571 101120          HALT             ;CRY OUT FAILED
09                       MOVZL 0,0        ;SET UP NEXT TEST
10                       SUBTS 15,20000
11                    ;AC0=20000 COMING INTO THIS TEST 20000-20000 SHOULD=0 RESULT
12                    ;0-20000 NEGATED=20000 SHD=0 INTO AC3
13                 ;SUB15:
14 04572 105040          MOVO 0,1
15 04573 106424          SUBZ 0,1,SZR
16 04574 063077          HALT             ;20000-20000 SEE AC1 SHD=0
17 04575 101007          MOV 0,0,SBN      ;0 CRY SHD =1 FROM CRYOUT
18 04576 063077          HALT     ;AC0=20000(?) CRY SHD=1
19 04577 152000          ADC 2,2
20 04600 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
21                    ;0-20000 SHOULD=-20000 NEGATED TO AC3
22 04601 112400          SUB 0,2          ;0-20000
23 04602 154420          NEGZ 2,3         ;NEGATED SHD=20000
24 04603 116444          SUBO 0,3,SZR     ;20000-20000 SHD=0 AGAIN
25 04604 063077          HALT
26 04605 101002          MOV 0,0,SZC      ;CRY SHD COMP 1 TO 0
27 04606 063077          HALT             ;CRY OUT FAILED
28 04607 101120          MOVZL 0,0        ;SET UP NEXT TEST
29                       SUBTS 16,40000
30                    ;AC0=40000 COMING INTO THIS TEST 40000-40000 SHOULD=0 RESULT
31                    ;0-40000 NEGATED=40000 SHD=0 INTO AC3
32                 ;SUB16:
33 04610 105040          MOVO 0,1
34 04611 106424          SUBZ 0,1,SZR
35 04612 063077          HALT             ;40000-40000 SEE AC1 SHD=0
36 04613 101007          MOV 0,0,SBN      ;0 CRY SHD =1 FROM CRYOUT
37 04614 063077          HALT     ;AC0=40000(?) CRY SHD=1
38 04615 152000          ADC 2,2
39 04616 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
40                    ;0-40000 SHOULD=-40000 NEGATED TO AC3
41 04617 112400          SUB 0,2          ;0-40000
42 04620 154420          NEGZ 2,3         ;NEGATED SHD=40000
43 04621 116444          SUBO 0,3,SZR     ;40000-40000 SHD=0 AGAIN
44 04622 063077          HALT
45 04623 101002          MOV 0,0,SZC      ;CRY SHD COMP 1 TO 0
46 04624 063077          HALT             ;CRY OUT FAILED
47 04625 101120          MOVZL 0,0        ;SET UP NEXT TEST
48                       SUBTS 17,100000
49                    ;AC0=100000 COMING INTO THIS TEST 100000-100000 SHOULD=0 RESUL
50                    ;0-100000 NEGATED=100000 SHD=0 INTO AC3
51                 ;SUB17:
52 04626 105040          MOVO 0,1
53 04627 106424          SUBZ 0,1,SZR
54 04630 063077          HALT             ;100000-100000 SEE AC1 SHD=0
55 04631 101007          MOV 0,0,SBN      ;0 CRY SHD =1 FROM CRYOUT
56 04632 063077          HALT     ;AC0=100000(?) CRY SHD=1
57 04633 152000          ADC 2,2
58 04634 150000          COM 2,2 ;MAKE AC2=0 FOR TEST
59                    ;0-100000 SHOULD=-100000 NEGATED TO AC3
60 04635 112400          SUB 0,2          ;0-100000
61 04636 154420          NEGZ 2,3         ;NEGATED SHD=100000
```

```
0082 N2LOG
01 04637 116444          SUBO 0,3,SZR     ;100000-100000 SHD=0 AGAIN
02 04640 063077          HALT
03 04641 101002          MOV 0,0,SZC      ;CRY SHD COMP 1 TO 0
04 04642 063077          HALT             ;CRY OUT FAILED
05 04643 101120          MOVZL 0,0        ;SET UP NEXT TEST
06
07
```

```
10083 N2LOG
01                      ;LOAD ACCUMULATOR TESTS FIRST MRI FIRST LDA
02                      ;IF LDA HANGS TRY SETFETCH OR PTGHOLD MRI ROM 0
03 04644 102400 LDA00:  SUB 0,0
04 04645 105040         MOVO 0,1
05 04646 020054         LDA 0,K1        ;K1=1
06 04647 101005         MOV 0,0,SNR     ;AC IS AT LEAST NON ZERO
07 04650 063077         HALT            ;DID NOT LOAD AC0 WITH+1
08 04651 105234         MOVZR# 0,1,SZR  ;CHECK AC0 TO REALLY=+1
09 04652 063077         HALT            ;SEE AC0 NOT=+1
10                      ;FIRST USE OF MRI OR LDA INSTRUCTION
11                      ;INCORRECT RESULT IN AC0 COULD BE DUE TO ANY OF
12                      ;A VARIETY OF PROBLEMS INCLUDING EFA
13                      ;IF MRI DOES NOT SET ALC INSTRUCTION DECODES AS COMZ 1,0
14                      ;AC0 WILL=-1 AND CARRY WILL=0
15                      ;IF INSTRUCTION DECODES AS I/O IT'S NIO 40(AC0=0)
16                      ;IF DATA IN AC0 IS OTHER THAN 0 OR -1 EFA
17
18                      ;DEFINE MACRO TO VERIFY LDA DOES NOT DISTURB OTHER AC'S
19                      .MACRO LDAT1
20                  ;LDAA1:
21                      ADC 3,3         ;SET AC3=-1
22                      LDA 2,K1        ;LOAD +1 TO AC2
23                      COM 3,3,SZR     ;AC3 SHD STILL=-1
24                      HALT            ;LDA OF 2 DIST AC3
25                  %
26
27                      LDAT1 01,2,1
28                  ;LDA01:
29 04653 126000         ADC 1,1 ;SET AC1=-1
30 04654 020054         LDA 0,K1        ;LOAD +1 TO AC0
31 04655 124004         COM 1,1,SZR     ;AC1 SHD STILL=-1
32 04656 063077         HALT            ;LDA OF 0 DIST AC1
33                      LDAT1 02,0,2
34                  ;LDA02:
35 04657 152000         ADC 2,2 ;SET AC2=-1
36 04660 020054         LDA 0,K1        ;LOAD +1 TO AC0
37 04661 150004         COM 2,2,SZR     ;AC2 SHD STILL=-1
38 04662 063077         HALT            ;LDA OF 0 DIST AC2
39                      LDAT1 03,0,3
40                  ;LDA03:
41 04663 176000         ADC 3,3 ;SET AC3=-1
42 04664 020054         LDA 0,K1        ;LOAD +1 TO AC0
43 04665 174004         COM 3,3,SZR     ;AC3 SHD STILL=-1
44 04666 063077         HALT            ;LDA OF 0 DIST AC3
45                      LDAT1 04,1,0
46                  ;LDA04:
47 04667 102000         ADC 0,0 ;SET AC0=-1
48 04670 024054         LDA 1,K1        ;LOAD +1 TO AC1
49 04671 100004         COM 0,0,SZR     ;AC0 SHD STILL=-1
50 04672 063077         HALT            ;LDA OF 1 DIST AC0
51                      LDAT1 05,1,2
52                  ;LDA05:
53 04673 152000         ADC 2,2 ;SET AC2=-1
54 04674 024054         LDA 1,K1        ;LOAD +1 TO AC1
55 04675 150004         COM 2,2,SZR     ;AC2 SHD STILL=-1
56 04676 063077         HALT            ;LDA OF 1 DIST AC2
57                      LDAT1 06,1,3
58                  ;LDA06:
59 04677 176000         ADC 3,3 ;SET AC3=-1
60 04700 024054         LDA 1,K1        ;LOAD +1 TO AC1
```

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0084 N2LOG
01 04701 174004         COM 3,3,SZR     ;AC3 SHD STILL=-1
02 04702 063077         HALT            ;LDA OF 1 DIST AC3
03                      LDAT1 07,2,3
04                  ;LDA07:
05 04703 102000         ADC 0,0 ;SET AC0=-1
06 04704 034054         LDA 2,K1        ;LOAD +1 TO AC2
07 04705 100004         COM 0,0,SZR     ;AC0 SHD STILL=-1
08 04706 063077         HALT            ;LDA OF 2 DIST AC0
09                      LDAT1 08,2,1
10                  ;LDA08:
11 04707 126000         ADC 1,1 ;SET AC1=-1
12 04710 034054         LDA 2,K1        ;LOAD +1 TO AC2
13 04711 124004         COM 1,1,SZR     ;AC1 SHD STILL=-1
14 04712 063077         HALT            ;LDA OF 2 DIST AC1
15                      LDAT1 09,2,3
16                  ;LDA09:
17 04713 176000         ADC 3,3 ;SET AC3=-1
18 04714 034054         LDA 2,K1        ;LOAD +1 TO AC2
19 04715 174004         COM 3,3,SZR     ;AC3 SHD STILL=-1
20 04716 063077         HALT            ;LDA OF 2 DIST AC3
21                      LDAT1 10,3,0
22                  ;LDA10:
23 04717 102000         ADC 0,0 ;SET AC0=-1
24 04720 034054         LDA 3,K1        ;LOAD +1 TO AC3
25 04721 100004         COM 0,0,SZR     ;AC0 SHD STILL=-1
26 04722 063077         HALT            ;LDA OF 3 DIST AC0
27                      LDAT1 11,3,1
28                  ;LDA11:
29 04723 126000         ADC 1,1 ;SET AC1=-1
30 04724 034054         LDA 3,K1        ;LOAD +1 TO AC3
31 04725 124004         COM 1,1,SZR     ;AC1 SHD STILL=-1
32 04726 063077         HALT            ;LDA OF 3 DIST AC1
33                      LDAT1 12,3,2
34                  ;LDA12:
35 04727 152000         ADC 2,2 ;SET AC2=-1
36 04730 034054         LDA 3,K1        ;LOAD +1 TO AC3
37 04731 154004         COM 2,2,SZR     ;AC2 SHD STILL=-1
38 04732 063077         HALT            ;LDA OF 3 DIST AC2
```

```
10085 N2LOG
01
02
03                  ;DEFINE MACRO TO FURTHER TEST LDA INST
04
05                          .MACRO LDAT2
06                  ;LDAA1:
07                          LDA 1,A2        ;GET A3 TO AC1
08                          MOV 1,2
09                          SUB 0,2,SZR     ;AC0=A3 COMING INTO TEST
10                          HALT
11                          MOVZL 0,0       ;POSITION FOR NEXT TEST
12                  %
13
14 04733 102525             SUBZL 0,0,SNR   ;SET UP LDA TESTS
15 04734 063077             HALT            ;SET UP FAILED SEE AC0
16
17                          LDAT2 13,K1,1
18                  ;LDA13:
19 04735 024054             LDA 1,K1        ;GET 1 TO AC1
20 04736 131000             MOV 1,2
21 04737 112404             SUB 0,2,SZR     ;AC0=1 COMING INTO TEST
22 04740 063077             HALT
23 04741 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
24                          LDAT2 14,K2,2
25                  ;LDA14:
26 04742 024055             LDA 1,K2        ;GET 2 TO AC1
27 04743 131000             MOV 1,2
28 04744 112404             SUB 0,2,SZR     ;AC0=2 COMING INTO TEST
29 04745 063077             HALT
30 04746 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
31                          LDAT2 15,K4,4
32                  ;LDA15:
33 04747 024056             LDA 1,K4        ;GET 4 TO AC1
34 04750 131000             MOV 1,2
35 04751 112404             SUB 0,2,SZR     ;AC0=4 COMING INTO TEST
36 04752 063077             HALT
37 04753 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
38                          LDAT2 16,K10,10
39                  ;LDA16:
40 04754 024057             LDA 1,K10       ;GET 10 TO AC1
41 04755 131000             MOV 1,2
42 04756 112404             SUB 0,2,SZR     ;AC0=10 COMING INTO TEST
43 04757 063077             HALT
44 04760 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
45                          LDAT2 17,K20,20
46                  ;LDA17:
47 04761 024060             LDA 1,K20       ;GET 20 TO AC1
48 04762 131000             MOV 1,2
49 04763 112404             SUB 0,2,SZR     ;AC0=20 COMING INTO TEST
50 04764 063077             HALT
51 04765 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
52                          LDAT2 18,K40,40
53                  ;LDA18:
54 04766 024061             LDA 1,K40       ;GET 40 TO AC1
55 04767 131000             MOV 1,2
56 04770 112404             SUB 0,2,SZR     ;AC0=40 COMING INTO TEST
57 04771 063077             HALT
58 04772 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
59                          LDAT2 19,K100,100
60                  ;LDA19:
```

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20086 N2LOG
01 04773 024062             LDA 1,K100      ;GET 100 TO AC1
02 04774 131000             MOV 1,2
03 04775 112404             SUB 0,2,SZR     ;AC0=100 COMING INTO TEST
04 04776 063077             HALT
05 04777 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
06                          LDAT2 20,K200,200
07                  ;LDA20:
08 05000 024063             LDA 1,K200      ;GET 200 TO AC1
09 05001 131000             MOV 1,2
10 05002 112404             SUB 0,2,SZR     ;AC0=200 COMING INTO TEST
11 05003 063077             HALT
12 05004 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
13                          LDAT2 21,K400,400
14                  ;LDA21:
15 05005 024064             LDA 1,K400      ;GET 400 TO AC1
16 05006 131000             MOV 1,2
17 05007 112404             SUB 0,2,SZR     ;AC0=400 COMING INTO TEST
18 05010 063077             HALT
19 05011 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
20                          LDAT2 22,K1000,1000
21                  ;LDA22:
22 05012 024065             LDA 1,K1000     ;GET 1000 TO AC1
23 05013 131000             MOV 1,2
24 05014 112404             SUB 0,2,SZR     ;AC0=1000 COMING INTO TEST
25 05015 063077             HALT
26 05016 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
27                          LDAT2 23,K2000,2000
28                  ;LDA23:
29 05017 024066             LDA 1,K2000     ;GET 2000 TO AC1
30 05020 131000             MOV 1,2
31 05021 112404             SUB 0,2,SZR     ;AC0=2000 COMING INTO TEST
32 05022 063077             HALT
33 05023 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
34                          LDAT2 24,K4000,4000
35                  ;LDA24:
36 05024 024067             LDA 1,K4000     ;GET 4000 TO AC1
37 05025 131000             MOV 1,2
38 05026 112404             SUB 0,2,SZR     ;AC0=4000 COMING INTO TEST
39 05027 063077             HALT
40 05030 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
41                          LDAT2 25,K10K,10000
42                  ;LDA25:
43 05031 024070             LDA 1,K10K      ;GET 10000 TO AC1
44 05032 131000             MOV 1,2
45 05033 112404             SUB 0,2,SZR     ;AC0=10000 COMING INTO TEST
46 05034 063077             HALT
47 05035 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
48                          LDAT2 26,K20K,20000
49                  ;LDA26:
50 05036 024071             LDA 1,K20K      ;GET 20000 TO AC1
51 05037 131000             MOV 1,2
52 05040 112404             SUB 0,2,SZR     ;AC0=20000 COMING INTO TEST
53 05041 063077             HALT
54 05042 101120             MOVZL 0,0       ;POSITION FOR NEXT TEST
55                          LDAT2 27,K40K,40000
56                  ;LDA27:
57 05043 024072             LDA 1,K40K      ;GET 40000 TO AC1
58 05044 131000             MOV 1,2
59 05045 112404             SUB 0,2,SZR     ;AC0=40000 COMING INTO TEST
60 05046 063077             HALT
```

```
 0087 N2LOG
01 05047 101120         MOVZL 0,0       ;POSITION FOR NEXT TEST
02                      LOAT2 28,K100K,100000
03              ;LDA2A:
04 05050 024073         LDA 1,K100K     ;GET 100000 TO AC1
05 05051 131000         MOV 1,2
06 05052 112404         SUB 0,2,SZR     ;AC0=100000 COMING INTO TEST
07 05053 063077         HALT
08 05054 101120         MOVZL 0,0       ;POSITION FOR NEXT TEST
```

```
 0088 N2LOG
01
02
03                ;FIRST TEST OF BYTE SWAP "S"
04                ;CALC .IR8,IR9 INTO ALU SHIFTER
05
06 05055 102745 SWP00:  SUBOS 0,0,SNR
07 05056 101324         MOVZS 0,0,SZR   ;FIRST USE OF "S" AC0=0
08 05057 063077         HALT            ;EXAMINE AC0 FOR "SWAP" ERR
09 05060 102323 SWP01:  ADCZS 0,0,SNC   ;CRY SHD REMAIN=0
10 05061 101302         MOVS 0,0,SZC    ;SAME
11 05062 063077         HALT            ;SEE ZC SHIFTER
12 05063 102722 SWP02:  SUBZS 0,0,SZC   ;CRY SHD REMAIN=1
13 05064 101303         MOVS 0,0,SNC    ;SAME
14 05065 063077         HALT            ;SEE ZC SHIFTER
15 05066 102725 SWP03:  SUBZS 0,0,SNR   ;A 1 IN CRY SHD NOT AFFECT "S"
16 05067 101344         MOVOS 0,0,SZR   ;TRY SWAP 0'S WITH CRY=1
17 05070 063077         HALT            ;EXAMINE AC0 FOR CRY "S"
18                ;ERROR DEPENDS ON A 1 IN BIT 0 OR 15 SEE ALU SHIFTER
19
20                ;DEFINE SWAP TEST MACRO
21                      .MACRO SWPTS
22                ;TEST SWAP BIT A4 TO BIT A5
23                ;AC0=A6 AC1=A7 EXPECTED RESULT IN AC2 IS A7
24              ;SWPA1:
25                      LDA 0,A2        ;GET A6
26                      LDA 1,A3        ;A7 EXPECTED RESULT
27                      MOVZS 0,2,SZR   ;"S" BIT A4 TO BIT A5
28                      MOV 2,3,SNR
29                      HALT    ;POSS, "ZR" AND FAILURE "S"
30                      SUB 1,3,SZR
31                      HALT            ;"S" BIT A4 TO A5 FAILED EX AC2
32              ;SWA1A:
33                      COMOS 0,2       ;REPEAT TEST WITH A0
34                      COM 2,3         ;EXPECTED RESULT HERE IS A7
35                      SUB 1,3,SZR
36                      HALT            ;"S" A0 IN BIT A4 TO A5 SEE AC2
37                ;SWA1A TESTS SWAP OF COM A6
38              %
39
40
41
42                      SWPTS 04,K1,K400,15,7,1,400
43                ;TEST SWAP BIT 15 TO BIT 7
44                ;AC0=1 AC1=400 EXPECTED RESULT IN AC2 IS 400
45              ;SWP04:
46 05071 020054         LDA 0,K1        ;GET 1
47 05072 024064         LDA 1,K400      ;400 EXPECTED RESULT
48 05073 111324         MOVZS 0,2,SZR   ;"S" BIT 15 TO BIT 7
49 05074 155035         MOV 2,3,SNR
50 05075 063077         HALT    ;POSS, "ZR" AND FAILURE "S"
51 05076 136404         SUB 1,3,SZR
52 05077 063077         HALT            ;"S" BIT 15 TO 7 FAILED EX AC2
53              ;SA04A:
54 05100 110340         COMOS 0,2       ;REPEAT TEST WITH A0
55 05101 154000         COM 2,3         ;EXPECTED RESULT HERE IS 400
56 05102 136404         SUB 1,3,SZR
57 05103 063077         HALT            ;"S" A0 IN BIT 15 TO 7 SEE AC2
58                ;SW04A TESTS SWAP OF COM 1
59                      SWPTS 05,K2,K1000,14,6,2,1000
60                ;TEST SWAP BIT 14 TO BIT 6
```

```
0089 N2LOG
01                      ;AC0=2 AC1=1000 EXPECTED RESULT IN AC2 IS 1000
02                    ;SWP05:
03 05104 020055         LDA 0,K2        ;GET 2
04 05105 024065         LDA 1,K1000     ;1000 EXPECTED RESULT
05 05106 111324         MOVZS 0,2,SZR   ;"S" BIT 14 TO BIT 6
06 05107 155005         MOV 2,3,SNR
07 05110 063077         HALT    ;POSS. "ZR" AND FAILURE "S"
08 05111 136404         SUB 1,3,SZR
09 05112 063077         HALT            ;"S" BIT 14 TO 6 FAILED EX AC2
10                    ;SW05A:
11 05113 110340         COMOS 0,2       ;REPEAT TEST WITH A0
12 05114 154000         COM 2,3         ;EXPECTED RESULT HERE IS 1000
13 05115 136404         SUB 1,3,SZR
14 05116 063077         HALT            ;"S" A0 IN BIT 14 TO 6 SEE AC2
15                      ;SW05A TESTS SWAP OF COM 2
16                      SWPTS 06,K4,K2000,13,5,4,2000
17                      ;TEST SWAP BIT 13 TO BIT 5
18                      ;AC0=4 AC1=2000 EXPECTED RESULT IN AC2 IS 2000
19                    ;SWP06:
20 05117 020056         LDA 0,K4        ;GET 4
21 05120 024066         LDA 1,K2000     ;2000 EXPECTED RESULT
22 05121 111324         MOVZS 0,2,SZR   ;"S" BIT 13 TO BIT 5
23 05122 155005         MOV 2,3,SNR
24 05123 063077         HALT    ;POSS. "ZR" AND FAILURE "S"
25 05124 136404         SUB 1,3,SZR
26 05125 063077         HALT            ;"S" BIT 13 TO 5 FAILED EX AC2
27                    ;SW06A:
28 05126 110340         COMOS 0,2       ;REPEAT TEST WITH A0
29 05127 154000         COM 2,3         ;EXPECTED RESULT HERE IS 2000
30 05130 136404         SUB 1,3,SZR
31 05131 063077         HALT            ;"S" A0 IN BIT 13 TO 5 SEE AC2
32                      ;SW06A TESTS SWAP OF COM 4
33                      SWPTS 07,K10,K4000,12,4,10,4000
34                      ;TEST SWAP BIT 12 TO BIT 4
35                      ;AC0=10 AC1=4000 EXPECTED RESULT IN AC2 IS 4000
36                    ;SWP07:
37 05132 020057         LDA 0,K10       ;GET 10
38 05133 024067         LDA 1,K4000     ;4000 EXPECTED RESULT
39 05134 111324         MOVZS 0,2,SZR   ;"S" BIT 12 TO BIT 4
40 05135 155005         MOV 2,3,SNR
41 05136 063077         HALT    ;POSS. "ZR" AND FAILURE "S"
42 05137 136404         SUB 1,3,SZR
43 05140 063077         HALT            ;"S" BIT 12 TO 4 FAILED EX AC2
44                    ;SW07A:
45 05141 110340         COMOS 0,2       ;REPEAT TEST WITH A0
46 05142 154000         COM 2,3         ;EXPECTED RESULT HERE IS 4000
47 05143 136404         SUB 1,3,SZR
48 05144 063077         HALT            ;"S" A0 IN BIT 12 TO 4 SEE AC2
49                      ;SW07A TESTS SWAP OF COM 10
50                      SWPTS 08,K20,K10K,11,3,20,10000
51                      ;TEST SWAP BIT 11 TO BIT 3
52                      ;AC0=20 AC1=10000 EXPECTED RESULT IN AC2 IS 10000
53                    ;SWP08:
54 05145 020060         LDA 0,K20       ;GET 20
55 05146 024070         LDA 1,K10K      ;10000 EXPECTED RESULT
56 05147 111324         MOVZS 0,2,SZR   ;"S" BIT 11 TO BIT 3
57 05150 155005         MOV 2,3,SNR
58 05151 063077         HALT    ;POSS. "ZR" AND FAILURE "S"
59 05152 136404         SUB 1,3,SZR
60 05153 063077         HALT            ;"S" BIT 11 TO 3 FAILED EX AC2
```

```
0090 N2LOG
01                    ;SW08A:
02 05154 110340         COMOS 0,2       ;REPEAT TEST WITH A0
03 05155 154000         COM 2,3         ;EXPECTED RESULT HERE IS 10000
04 05156 136404         SUB 1,3,SZR
05 05157 063077         HALT            ;"S" A0 IN BIT 11 TO 3 SEE AC2
06                      ;SW08A TESTS SWAP OF COM 20
07                      SWPTS 09,K40,K20K,10,2,40,20000
08                      ;TEST SWAP BIT 10 TO BIT 2
09                      ;AC0=40 AC1=20000 EXPECTED RESULT IN AC2 IS 20000
10                    ;SWP09:
11 05160 020061         LDA 0,K40       ;GET 40
12 05161 024071         LDA 1,K20K      ;20000 EXPECTED RESULT
13 05162 111324         MOVZS 0,2,SZR   ;"S" BIT 10 TO BIT 2
14 05163 155005         MOV 2,3,SNR
15 05164 063077         HALT    ;POSS. "ZR" AND FAILURE "S"
16 05165 136404         SUB 1,3,SZR
17 05166 063077         HALT            ;"S" BIT 10 TO 2 FAILED EX AC2
18                    ;SW09A:
19 05167 110340         COMOS 0,2       ;REPEAT TEST WITH A0
20 05170 154000         COM 2,3         ;EXPECTED RESULT HERE IS 20000
21 05171 136404         SUB 1,3,SZR
22 05172 063077         HALT            ;"S" A0 IN BIT 10 TO 2 SEE AC2
23                      ;SW09A TESTS SWAP OF COM 40
24                      SWPTS 10,K100,K40K,9,1,100,40000
25                      ;TEST SWAP BIT 9 TO BIT 1
26                      ;AC0=100 AC1=40000 EXPECTED RESULT IN AC2 IS 40000
27                    ;SWP10:
28 05173 020062         LDA 0,K100      ;GET 100
29 05174 024072         LDA 1,K40K      ;40000 EXPECTED RESULT
30 05175 111324         MOVZS 0,2,SZR   ;"S" BIT 9 TO BIT 1
31 05176 155005         MOV 2,3,SNR
32 05177 063077         HALT    ;POSS. "ZR" AND FAILURE "S"
33 05200 136404         SUB 1,3,SZR
34 05201 063077         HALT            ;"S" BIT 9 TO 1 FAILED EX AC2
35                    ;SW10A:
36 05202 110340         COMOS 0,2       ;REPEAT TEST WITH A0
37 05203 154000         COM 2,3         ;EXPECTED RESULT HERE IS 40000
38 05204 136404         SUB 1,3,SZR
39 05205 063077         HALT            ;"S" A0 IN BIT 9 TO 1 SEE AC2
40                      ;SW 0A TESTS SWAP OF COM 100
41                      SWPTS 11,K200,K100K,8,0,200,100000
42                      ;TEST SWAP BIT 8 TO BIT 0
43                      ;AC0=200 AC1=100000 EXPECTED RESULT IN AC2 IS 100000
44                    ;SWP11:
45 05206 020063         LDA 0,K200      ;GET 200
46 05207 024073         LDA 1,K100K     ;100000 EXPECTED RESULT
47 05210 111324         MOVZS 0,2,SZR   ;"S" BIT 8 TO BIT 0
48 05211 155005         MOV 2,3,SNR
49 05212 063077         HALT    ;POSS. "ZR" AND FAILURE "S"
50 05213 136404         SUB 1,3,SZR
51 05214 063077         HALT            ;"S" BIT 8 TO 0 FAILED EX AC2
52                    ;SW11A:
53 05215 110340         COMOS 0,2       ;REPEAT TEST WITH A0
54 05216 154000         COM 2,3         ;EXPECTED RESULT HERE IS 100000
55 05217 136404         SUB 1,3,SZR
56 05220 063077         HALT            ;"S" A0 IN BIT 8 TO 0 SEE AC2
57                      ;SW11A TESTS SWAP OF COM 200
58                      SWPTS 12,K400,K1,7,15,400,1
59                      ;TEST SWAP BIT 7 TO BIT 15
60                      ;AC0=400 AC1=1 EXPECTED RESULT IN AC2 IS 1
```

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0091 N2LOG
01                      ;SWP12:
02 05221 020064                 LDA 0,K400      ;GET 400
03 05222 024054                 LDA 1,K1        ;1 EXPECTED RESULT
04 05223 111324                 MOVZS 0,2,SZR   ;"S" BIT 7 TO BIT 15
05 05224 155005                 MOV 2,3,SNR
06 05225 063077                 HALT    ;POSS. "ZR" AND FAILURE "S"
07 05226 136404                 SUB 1,3,SZR
08 05227 063077                 HALT            ;"S" BIT 7 TO 15 FAILED EX AC2
09                      ;SW12A:
10 05230 110340                 COMOS 0,2       ;REPEAT TEST WITH A0
11 05231 154000                 COM 2,3         ;EXPECTED RESULT HERE IS 1
12 05232 136404                 SUB 1,3,SZR
13 05233 063077                 HALT            ;"S" A0 IN BIT 7 TO 15 SEE AC2
14                        ;SW12A TESTS SWAP OF COM 400
15                              SWPTS 13,K1000,K2,6,14,1000,2
16                        ;TEST SWAP BIT 6 TO BIT 14
17                        ;AC0=1000 AC1=2 EXPECTED RESULT IN AC2 IS 2
18                      ;SWP13:
19 05234 020065                 LDA 0,K1000     ;GET 1000
20 05235 024055                 LDA 1,K2        ;2 EXPECTED RESULT
21 05236 111324                 MOVZS 0,2,SZR   ;"S" BIT 6 TO BIT 14
22 05237 155005                 MOV 2,3,SNR
23 05240 063077                 HALT    ;POSS. "ZR" AND FAILURE "S"
24 05241 136404                 SUB 1,3,SZR
25 05242 063077                 HALT            ;"S" BIT 6 TO 14 FAILED EX AC2
26                      ;SW13A:
27 05243 110340                 COMOS 0,2       ;REPEAT TEST WITH A0
28 05244 154000                 COM 2,3         ;EXPECTED RESULT HERE IS 2
29 05245 136404                 SUB 1,3,SZR
30 05246 063077                 HALT            ;"S" A0 IN BIT 6 TO 14 SEE AC2
31                        ;SW13A TESTS SWAP OF COM 1000
32                              SWPTS 14,K2000,K4,5,13,2000,4
33                        ;TEST SWAP BIT 5 TO BIT 13
34                        ;AC0=2000 AC1=4 EXPECTED RESULT IN AC2 IS 4
35                      ;SWP14:
36 05247 020066                 LDA 0,K2000     ;GET 2000
37 05250 024056                 LDA 1,K4        ;4 EXPECTED RESULT
38 05251 111324                 MOVZS 0,2,SZR   ;"S" BIT 5 TO BIT 13
39 05252 155005                 MOV 2,3,SNR
40 05253 063077                 HALT    ;POSS. "ZR" AND FAILURE "S"
41 05254 136404                 SUB 1,3,SZR
42 05255 063077                 HALT            ;"S" BIT 5 TO 13 FAILED EX AC2
43                      ;SW14A:
44 05256 110340                 COMOS 0,2       ;REPEAT TEST WITH A0
45 05257 154000                 COM 2,3         ;EXPECTED RESULT HERE IS 4
46 05260 136404                 SUB 1,3,SZR
47 05261 063077                 HALT            ;"S" A0 IN BIT 5 TO 13 SEE AC2
48                        ;SW14A TESTS SWAP OF COM 2000
49                              SWPTS 15,K4000,K10,4,12,4000,10
50                        ;TEST SWAP BIT 4 TO BIT 12
51                        ;AC0=4000 AC1=10 EXPECTED RESULT IN AC2 IS 10
52                      ;SWP15:
53 05262 020067                 LDA 0,K4000     ;GET 4000
54 05263 024057                 LDA 1,K10       ;10 EXPECTED RESULT
55 05264 111324                 MOVZS 0,2,SZR   ;"S" BIT 4 TO BIT 12
56 05265 155005                 MOV 2,3,SNR
57 05266 063077                 HALT    ;POSS. "ZR" AND FAILURE "S"
58 05267 136404                 SUB 1,3,SZR
59 05270 063077                 HALT            ;"S" BIT 4 TO 12 FAILED EX AC2
60                      ;SW15A:
```

```
0092 N2LOG
01 05271 110340                 COMOS 0,2       ;REPEAT TEST WITH A0
02 05272 154000                 COM 2,3         ;EXPECTED RESULT HERE IS 10
03 05273 136404                 SUB 1,3,SZR
04 05274 063077                 HALT            ;"S" A0 IN BIT 4 TO 12 SEE AC2
05                        ;SW15A TESTS SWAP OF COM 4000
06                              SWPTS 16,K10K,K20,3,11,10000,20
07                        ;TEST SWAP BIT 3 TO BIT 11
08                        ;AC0=10000 AC1=20 EXPECTED RESULT IN AC2 IS 20
09                      ;SWP16:
10 05275 020070                 LDA 0,K10K      ;GET 10000
11 05276 024060                 LDA 1,K20       ;20 EXPECTED RESULT
12 05277 111324                 MOVZS 0,2,SZR   ;"S" BIT 3 TO BIT 11
13 05300 155005                 MOV 2,3,SNR
14 05301 063077                 HALT    ;POSS. "ZR" AND FAILURE "S"
15 05302 136404                 SUB 1,3,SZR
16 05303 063077                 HALT            ;"S" BIT 3 TO 11 FAILED EX AC2
17                      ;SW16A:
18 05304 110340                 COMOS 0,2       ;REPEAT TEST WITH A0
19 05305 154000                 COM 2,3         ;EXPECTED RESULT HERE IS 20
20 05306 136404                 SUB 1,3,SZR
21 05307 063077                 HALT            ;"S" A0 IN BIT 3 TO 11 SEE AC2
22                        ;SW16A TESTS SWAP OF COM 10000
23                              SWPTS 17,K20K,K40,2,10,20000,40
24                        ;TEST SWAP BIT 2 TO BIT 10
25                        ;AC0=20000 AC1=40 EXPECTED RESULT IN AC2 IS 40
26                      ;SWP17:
27 05310 020071                 LDA 0,K20K      ;GET 20000
28 05311 024061                 LDA 1,K40       ;40 EXPECTED RESULT
29 05312 111324                 MOVZS 0,2,SZR   ;"S" BIT 2 TO BIT 10
30 05313 155005                 MOV 2,3,SNR
31 05314 063077                 HALT    ;POSS. "ZR" AND FAILURE "S"
32 05315 136404                 SUB 1,3,SZR
33 05316 063077                 HALT            ;"S" BIT 2 TO 10 FAILED EX AC2
34                      ;SW17A:
35 05317 110340                 COMOS 0,2       ;REPEAT TEST WITH A0
36 05320 154000                 COM 2,3         ;EXPECTED RESULT HERE IS 40
37 05321 136404                 SUB 1,3,SZR
38 05322 063077                 HALT            ;"S" A0 IN BIT 2 TO 10 SEE AC2
39                        ;SW17A TESTS SWAP OF COM 20000
40                              SWPTS 18,K40K,K100,1,9,40000,100
41                        ;TEST SWAP BIT 1 TO BIT 9
42                        ;AC0=40000 AC1=100 EXPECTED RESULT IN AC2 IS 100
43                      ;SWP18:
44 05323 020072                 LDA 0,K40K      ;GET 40000
45 05324 024062                 LDA 1,K100      ;100 EXPECTED RESULT
46 05325 111324                 MOVZS 0,2,SZR   ;"S" BIT 1 TO BIT 9
47 05326 155005                 MOV 2,3,SNR
48 05327 063077                 HALT    ;POSS. "ZR" AND FAILURE "S"
49 05330 136404                 SUB 1,3,SZR
50 05331 063077                 HALT            ;"S" BIT 1 TO 9 FAILED EX AC2
51                      ;SW18A:
52 05332 110340                 COMOS 0,2       ;REPEAT TEST WITH A0
53 05333 154000                 COM 2,3         ;EXPECTED RESULT HERE IS 100
54 05334 136404                 SUB 1,3,SZR
55 05335 063077                 HALT            ;"S" A0 IN BIT 1 TO 9 SEE AC2
56                        ;SW18A TESTS SWAP OF COM 40000
57                              SWPTS 19,K100K,K200,0,8,100000,200
58                        ;TEST SWAP BIT 0 TO BIT 8
59                        ;AC0=100000 AC1=200 EXPECTED RESULT IN AC2 IS 200
60                      ;SWP19:
```

```
 0093 N2LOG
01 05336 020073          LDA 0,K100K      ;GET 100000
02 05337 024063          LDA 1,K200       ;200 EXPECTED RESULT
03 05340 111324          MOVZS 0,2,SZR    ;"S" BIT 0 TO BIT 8
04 05341 155005          MOV 2,3,SNR
05 05342 063077          HALT     ;POSS. "ZR" AND FAILURE "S"
06 05343 136404          SUB 1,3,SZR
07 05344 063077          HALT             ;"S" BIT 0 TO 8 FAILED EX AC2
08                 ;SW19A:
09 05345 110340          COMOS 0,2        ;REPEAT TEST WITH A0
10 05346 154000          COM 2,3          ;EXPECTED RESULT HERE IS 200
11 05347 136404          SUB 1,3,SZR
12 05350 063077          HALT             ;"S" A0 IN BIT 0 TO 8 SEE AC2
13                ;SW19A TESTS SWAP OF COM 100000
```

```
 0094 N2LOG
01                ;DEFINE MACRO FOR NO LOAD TESTS (IR12=1)
02                .MACRO NOLOD
03                NLDA1:  ADC A2,A2        ;AC A2=-1
04                        COM# A2,A2,SNR   ;ATTEMPT TO MAKE ZEROS
05                        COM A2,A2,SZR    ;AC A2 SHD HAVE =-1
06                        HALT             ;AC A2 ALTERED IR12=1
07                        ADC# A2,A2,SZR ;NOLOAD 1'S
08                        MOV A2,A2,SZR    ;AC A2 SHD STILL=0'S
09                        HALT             ;IR12=1 DID NOT BLOCK 1'S
10                %
11                        NOLOD 1,0
12 05351 102000 NLD1:     ADC 0,0 ;AC0=-1
13 05352 100015           COM# 0,0,SNR     ;ATTEMPT TO MAKE ZEROS
14 05353 100004           COM 0,0,SZR      ;AC0 SHD HAVE =-1
15 05354 063077           HALT             ;AC0 ALTERED IR12=1
16 05355 102014           ADC# 0,0,SZR ;NOLOAD 1'S
17 05356 101004           MOV 0,0,SZR      ;AC0 SHD STILL=0'S
18 05357 063077           HALT             ;IR12=1 DID NOT BLOCK 1'S
19                        NOLOD 2,1
20 05360 126000 NLD2:     ADC 1,1 ;AC1=-1
21 05361 124015           COM# 1,1,SNR     ;ATTEMPT TO MAKE ZEROS
22 05362 124004           COM 1,1,SZR      ;AC1 SHD HAVE =-1
23 05363 063077           HALT             ;AC1 ALTERED IR12=1
24 05364 126014           ADC# 1,1,SZR ;NOLOAD 1'S
25 05365 125004           MOV 1,1,SZR      ;AC1 SHD STILL=0'S
26 05366 063077           HALT             ;IR12=1 DID NOT BLOCK 1'S
27                        NOLOD 3,2
28 05367 152000 NLD3:     ADC 2,2 ;AC2=-1
29 05370 150015           COM# 2,2,SNR     ;ATTEMPT TO MAKE ZEROS
30 05371 150004           COM 2,2,SZR      ;AC2 SHD HAVE =-1
31 05372 063077           HALT             ;AC2 ALTERED IR12=1
32 05373 152014           ADC# 2,2,SZR ;NOLOAD 1'S
33 05374 151004           MOV 2,2,SZR      ;AC2 SHD STILL=0'S
34 05375 063077           HALT             ;IR12=1 DID NOT BLOCK 1'S
35                        NOLOD 4,3
36 05376 176000 NLD4:     ADC 3,3 ;AC3=-1
37 05377 174015           COM# 3,3,SNR     ;ATTEMPT TO MAKE ZEROS
38 05400 174004           COM 3,3,SZR      ;AC3 SHD HAVE =-1
39 05401 063077           HALT             ;AC3 ALTERED IR12=1
40 05402 176014           ADC# 3,3,SZR ;NOLOAD 1'S
41 05403 175004           MOV 3,3,SZR      ;AC3 SHD STILL=0'S
42 05404 063077           HALT             ;IR12=1 DID NOT BLOCK 1'S
```

```
10095 N2LOG
01
02
03                ;FIRST USE OF STA INSTRUCTION
04                ;ALSO, FIRST LDA WITH 0 AS EFFECTIVE ADDRESS
05
06 05405 102000 STA00:  ADC 0,0
07 05406 040000         STA 0,0          ;FIRST USE OF STA
08 05407 024000         LDA 1,0          ;FIRST LDA OF LOC "0"
09 05410 130004         COM 1,2,SZR      ;SKIP IF LDA GOT -1 BACK
10 05411 063077         HALT             ;LDA FROM LOC "0" IS IN AC1
11                ;NOW STORE 0'S IN LOC 0 RETRY LDA 0
12 05412 102400 STA01:  SUB 0,0
13 05413 040000         STA 0,0          ;2ND STA IN LOC "0"
14 05414 024000         LDA 1,0          ;2ND LDA OF LOC "0"
15 05415 125004         MOV 1,1,SZR      ;SKP IS LDA GOT 0'S BACK
16 05416 063077         HALT
17                ;IF EITHER OF ABOVE HALTS EXAMINE LOC CONTAINING STA
18                ;IN CASE ADDRESSING MODE 1 ENABLED
19                ;IF STA00+1=-1 OR STA01+1=0 SEE IR7 ALU ROM
```

```
10096 N2LOG
01
02
03                ;CONTINUATION OF LDA TESTS
04                ;ADDRESSING MODE 01 (IR7=1 IR6=0)
05
06 05417 102000 LDA29:  ADC 0,0          ;SET AC0=-1
07 05420 020400         LDA 0,.          ;FIRST LDA WITH IR7=1
08 05421 024074         LDA 1,KLDA,      ;GET LDA 0,, FROM PAGE 0
09 05422 106404         SUB 0,1,SZR      ;RESULT LAST 2 LOADS SHD BE=
10 05423 063077         HALT             ;LDA 0 IR7=1 FAILED
11                ;EXPECTED RESULT IN AC0 PROBABLY LOADED LOC "0" INSTEAD
12                ;AT THIS POINT IN TEST "LOC 0"=0
13                ;NOW TEST FORWARD "LDA .+1" +1 OFFSET
14 05424 126000 LDA30:  ADC 1,1
15 05425 024401         LDA 1,.+1        ;GET NEXT MEM LOC
16 05426 020400         LDA 0,.+0        ;ALSO 0=LDA 0,.
17 05427 131000         MOV 1,2          ;SAVE LDA RESULTS
18 05430 112404         SUB 0,2,SZR      ;SKP BOTH LDA'S CORRECT
19 05431 063077         HALT             ;AC0 AND 1 SHD BOTH=LDA 0,.
20                ;USE NEGATIVE OFFEST FOR THE FIRST TIME
21                ;NOW TEST MODE 01 NEGATIVE OFFSET OF-1
22 05432 126000 LDA31:  ADC 1,1          ;SEE DISPXTND IF TEST FAILS
23 05433 020400         LDA 0,.          ;GET THIS INST TO AC0
24 05434 024777         LDA 1,.-1        ;FIRST USE - OFFSET TO AC1
25 05435 131000         MOV 1,2          ;SAVE LDA RESULTS
26 05436 112404         SUB 0,2,SZR      ;SKP BOTH LDA'S CORRECT
27 05437 063077         HALT             ;SEE DISP XTND +
28                ;LDA ALL AC'S WITH LDA 0,. USING FORWARD OFFSETS
29 05440 034403 LDA32:  LDA 3,.+3
30 05441 030402         LDA 2,.+2
31 05442 024401         LDA 1,.+1
32 05443 020400         LDA 0,.
33 05444 106414         SUB# 0,1,SZR
34 05445 063077         HALT             ;LDA 1,.+1 FAILED
35 05446 112414         SUB# 0,2,SZR
36 05447 063077         HALT             ;LDA 2,.+2 FAILED
37 05450 116414         SUB# 0,3,SZR
38 05451 063077         HALT             ;LDA 3,.+3 FAILED
39
40                ;TEST LDA SEQUENCE OF - OFFSETS
41 05452 020400 LDA33:  LDA 0,.
42 05453 024777         LDA 1,.-1
43 05454 030776         LDA 2,.-2
44 05455 034775         LDA 3,.-3
45 05456 106414         SUB# 0,1,SZR
46 05457 063077         HALT             ;LDA .-1 FAILED
47 05460 112414         SUB# 0,2,SZR
48 05461 063077         HALT             ;LDA .-2 FAILED
49 05462 116414         SUB# 0,3,SZR
50 05463 063077         HALT             ;LDA .-3 FAILED
51
52
```

```
10097 N2LOG
01                      ;TEST FOR EXISTENCE OF ISZ INSTR
02                      ;FIRST USE OF ISZ INSTRUCTION
03 05464 102400 ISZ00:  SUB 0,0
04 05465 040000         STA 0,0
05 05466 152000         ADC 2,2             ;SET AC2=-1 ISZ COULD=LDA OR STA
06 05467 010000         ISZ 0               ;+1 LOC 0 SHD NOW=+1
07 05470 105001         MOV 0,1,SKP         ;ALU CRY MIGHT NOT=1
08 05471 063077         HALT                ;ISZ (0+1) SKIPPED
09 05472 024000         LDA 1,0             ;SEE SETSKP AND ZR SKIP
10 05473 121225         MOVZR 1,0,SNR       ;MAKE SURE ISZ RESULT
11 05474 101003         MOV 0,0,SNC         ;IS=TO+1
12 05475 063077         HALT                ;0+1 DID NOT=+1
13 05476 154004         COM 2,3,SZR
14 05477 063077         HALT                ;ISZ CHANGED AC2
15
16                      ;TEST FOR EXISTENCE OF DSZ INSTRUCTION
17                      ;-1 TO 0 IN LOC 0 SHD=-1
18                      ;FIRST USE OF DSZ INST
19 05500 176400 DSZ00:  SUB 3,3
20 05501 040000         STA 0,0
21 05502 014000         DSZ 0               ;-1 TO 0 IN LOC 0
22 05503 105001         MOV 0,1,SKP
23 05504 063077         HALT                ;DSZ SKIPPED 0=1
24 05505 024000         LDA 1,0             ;GET DSZ RESULTS SHD=-1
25 05506 120004         COM 1,0,SZR
26 05507 063077         HALT                ;DSZ RESULT NOT=-1
27 05510 175004         MOV 3,3,SZR         ;AC3 SHD NOT BE DISTURBED
28 05511 063077         HALT                ;DSZ CHANGED AC3
29
30                      ;RETEST ISZ TO SKIP AND NOT CHNGE CRY
31                      ;+1 TO -1 IN LOC 0
32 05512 102000 ISZ01:  ADC 0,0
33 05513 040000         STA 0,0             ;(0)=-1
34 05514 111120         MOVZL 0,2           ;(AC2=-2) CRY=1
35 05515 010000         ISZ 0               ;+1-1=SETSKIP,ZR
36 05516 063077         HALT                ;ISZ-1 DID NOT SKIP
37 05517 101003         MOV 0,0,SNC         ;TEST CALC
38 05520 063077         HALT                ;CRY OUT CHANGED CRY
39 05521 020000         LDA 0,0
40 05522 101004         MOV 0,0,SZR
41 05523 063077         HALT                ;(LOC 0) DID NOT=0 AFTER ISZ
42 05524 140225         COMZR 2,0,SNR       ;MAKE SURE AC2 STILL=-2
43 05525 101003         MOV 0,0,SNC
44 05526 063077         HALT                ;ISZ CHANGED AC2
```

```
10098 N2LOG
01
02
03                      ;TEST DSZ SETSKP . ZR IN SKIP LOGIC
04 05527 102520 DSZ01:  SUBZL 0,0
05 05530 040000         STA 0,0             ;(LOC 0=+1)
06 05531 114000         COM 0,3             ;(AC3=-2)
07 05532 014000         DSZ 0               ;+1-1=SETSKP . ZR
08 05533 063077         HALT                ;DSZ DID NOT SKIP
09 05534 101002         MOV 0,0,SZC         ;TEST NOT CALC TO STOP CRYOUT
10 05535 063077         HALT                ;CRYOUT CHANGED CRY
11 05536 164225         COMZR 3,0,SNR
12 05537 101003         MOV 0,0,SNC         ;AC3 SHD STILL=-2
13 05540 063077         HALT                ;DSZ CHANGED AC3
14
15                      ;FIRST USE OF JMP INSTRUCTION JMP .+2
16                      ;ADDRS OF JMP TESTS ARE STORED IN LOC 0
17 05541 020002 JMP00:  LDA 0,.+2
18 05542 115001         MOV 0,3,SKP
19 05543 005541         JMP00
20 05544 040000         STA 0,0             ;ADDRS OF JMP TST TO LOC 0
21 05545 000402         JMP .+2
22 05546 063077         HALT                ;JMP DID NOT JMP
23 05547 116414         SUB# 0,3,SZR        ;AC0 AND AC3 SHD BE=
24 05550 063077         HALT                ;JMP CHANGED AC3 (JSR?)
25                      ;TEST JMP WITH A NEG OFFSET
26 05551 020002 JMP01:  LDA 0,.+2
27 05552 115001         MOV 0,3,SKP
28 05553 005551         JMP01
29 05554 040000         STA 0,0             ;LOC 0=ADDRS JMP TEST
30 05555 111001         MOV 0,2,SKP         ;GET TO JMP -
31 05556 000403         JMP .+3
32 05557 000777         JMP .-1
33 05560 063077         HALT
34 05561 116414         SUB# 0,3,SZR
35 05562 063077         HALT                ;JMP CHNGED AC0 OR AC3
```

```
!0099 N2LOG
01
02
03                  ;FIRST USE OF JSR INSTRUCTION
04
05 05563 020002 JSR00:  LDA 0,.+2
06 05564 115001         MOV 0,3,SKP
07 05565 005563         JSR00           ;ADRS THIS TEST
08 05566 040000         STA 0,0         ;TO LOC 0
09 05567 004002         JSR .+2         ;FIRST USE JSR
10 05570 063077         HALT            ;JSR DID NOT CHNG PC
11 05571 024075         LDA 1,K5
12 05572 123000         ADD 1,0         ;NOW AC0 AND AC3 SHD BE=
13 05573 116414         SUB# 0,3,SZR
14 05574 063077         HALT            ;JSR FAILED TO LOAD AC3
15                  ;TEST JSR WITH NEG OFFSET
16 05575 020002 JSR01:  LDA 0,.+2
17 05576 115001         MOV 0,3,SKP
18 05577 005575         JSR01           ;ADRS THIS TEST
19 05600 040000         STA 0,0         ;TO LOC 0
20 05601 111001         MOV 0,2,SKP
21 05602 000003         JMP .+3
22 05603 004777         JSR .-1         ;FIRST JSR - OFFSET
23 05604 063077         HALT            ;JSR DID NOT CHNG PC
24 05605 024076         LDA 1,K7
25 05606 123000         ADD 1,0
26 05607 116414         SUB# 0,3,SZR
27 05610 063077         HALT
28
29                  ;NOW TEST LDA USING INDEX MODE 2
30                   ;FIRST USE OF INDEXING OFFSET AND INDEX=0
31 05611 102000 LDA34:  ADC 0,0
32 05612 040000         STA 0,0         ;PREPARE AC'S
33 05613 110000         COM 0,2         ;0=-1  1 AND 2=0
34 05614 145000         MOV 2,1         ;AC3=+1
35 05615 050001         STA 2,1         ;(LOC 1)=0
36 05616 155400         INC 2,3
37 05617 025000         LDA 1,0,2
38 05620 167014         ADD# 3,1,SZR    ;AC3=+1 (AC1)=-1 IF LDA CORRECT
39 05621 063077         HALT            ;LDA 1,0,2 FAILED
40                  ;MAY HAVE USED AC3 AS INDEX (AC1) WILL=(LOC 1)
41
42                  ;TEST TO MAKE SURE EFA REALLY INDEXES MODE 2
43 05622 102000 LDA35:  ADC 0,0
44 05623 104000         COM 0,1
45 05624 131400         INC 1,2         ;AC2=1
46 05625 155400         INC 2,3         ;AC3=2
47 05626 044000         STA 1,0         ;LOC 0=0
48 05627 040001         STA 0,1         ;LOC 1=-1
49 05630 025000         LDA 1,0,2       ;GET (LOC 1) TO AC1
50 05631 106414         SUB# 0,1,SZR
51 05632 063077         HALT
```

```
!0100 N2LOG
01
02
03                  ;NOW USE STA MODE 2 INDEXED
04                  ;ALSO FIRST USE OF AN LDA PAGE 0 BIT 8=1
05
06 05633 030063 STA02:  LDA 2,K200      ;THIS LDA PREV TESTED
07 05634 051000         STA 2,0,2       ;STORE 200 IN LOC 200
08 05635 024200         LDA 1,200       ;DIRECT ACCESS 200
09 05636 132414         SUB# 1,2,SZR    ;NOT=LDA OR STA
10 05637 063077         HALT            ;COULD FAIL EFA DISPXTND
11                  ;IRH=1 SHD BE BLOCKED BY ALU ROM IR6,7=0 .EFA
12                  ;TRY STA AGAIN WITH + OFFSET
13                  ;CONTENTS OF LOC 200 STILL=200
14 05640 030063 STA03:  LDA 2,K200
15 05641 141400         INC 2,0
16 05642 041001         STA 0,1,2       ;201 TO LOC 201
17 05643 024201         LDA 1,201       ;GET 201 DIRECT
18 05644 122414         SUB# 1,0,SZR    ;
19 05645 063077         HALT            ;STA 0,1,2 FAILED
20
21                  ;TRY STA AGAIN WITH - OFFSET
22 05646 030063 STA04:  LDA 2,K200
23 05647 144000         COM 2,1
24 05650 045377         STA 1,-1,2      ;COM 200 TO LOC 177
25 05651 024177         LDA 0,177       ;GET IT BACK
26 05652 106414         SUB# 0,1,SZR    ;(LOC 177) SHD=COM 200
27 05653 063077         HALT            ;STA 1,-1,2 FAILED
28                  ;DISPXTND MAY HAVE FAILED EFA IR8=1 AND NOT INDEX 00
29                  ;ALU ROM IR6=1 AND EFA
30
31                  ;USE STA DIRECT TO 300
32                  ;AND LDA INDEXED MODE 3 TO RETRIEVE
33
34 05654 034063 STA05:  LDA 3,K200      ;PREP AC2 AND AC3 FOR
35 05655 030062         LDA 2,K100      ;TESTING INDEX 3 GETS AC3
36 05656 054300         STA 3,300       ;DOUBTFUL THAT DISPXTND FAILS
37 05657 160000         COM 3,0
38 05660 040200         STA 0,200       ;PREP LOC 200 IN CASE INDEXS AC2
39 05661 025500         LDA 1,100,3     ;FIRST USE OF INDEX 3
40 05662 136414         SUB# 1,3,SZR    ;AC1 AND AC3 SHD=200
41 05663 063077         HALT            ;LDA DIDN'T GET (LOC 300)
42                  ;IF (AC1)=COM OF 200 INDEX 2 WAS USED INSTEAD
43
44                  ;TEST LDA INDEXED AC3 WITH - OFFSET
45
46 05664 034077 STA06:  LDA 3,K300
47 05665 030063         LDA 2,K200
48 05666 160400         NEG 3,0
49 05667 040277         STA 0,277       ;-300 TO LOC 277
50 05670 025777         LDA 1,-1,3      ;LOC 277 TO AC1
51 05671 122414         SUB# 1,0,SZR    ;AC1 SHD=AC0
52 05672 063077         HALT            ;LDA 1,-1,3 FAILED
```

```
1@101 N2LOG
01
02
03                ;START TESTING AUTO INDEX AND INDIRECTS
04                ;USING MODE 2 SAFEST WAY TO LOAD LOC 20
05                ;AND AVOID "AUTO"
06
07 05673 030060 STA07:  LDA 2,K20
08 05674 020064         LDA 0,K400
09 05675 114400         NEG 0,3
10 05676 041000         STA 0,0,2       ;FIRST REF MEM LOC 20
11 05677 055001         STA 3,1,2
12 05700 024020         LDA 1,20        ;FIRST DIRECT REF LOC 20
13 05701 122414         SUB# 1,0,SZR    ;AC1 0 AND LOC 20 SHD=400
14 05702 063077         HALT            ;REFERENCE LOC 20 FAILED
15                ;AUTO ENABLED INTO SET AUTO COULD FAIL IR11=1
16                ;(20) AC1 AND AC0 SHOULD ALL=400
17
18                ;FIRST USE OF DEFER FOLLOWS
19                ;NOT AUTO INDEXED COULD HANG UP VIA NOT CP80
20 05703 024063 STA08:  LDA 1,K200      ;PREPARE REGISTERS
21 05704 044000         STA 1,0         ;FOR TEST
22 05705 130400         NEG 1,2
23 05706 050200         STA 2,200       ;200=-200
24 05707 044177         STA 1,177       ;177 AND 201
25 05710 044201         STA 1,201       ;=+200
26 05711 022000         LDA 0,@0        ;FIRST TIME IR5=1
27 05712 112414         SUB# 0,2,SZR    ;AC2 AND AC0 SHD=-200
28 05713 063077         HALT            ;FIRST DEFER FAILED
29 05714 020000         LDA 0,0
30 05715 106414         SUB# 0,1,SZR    ;LOC 0 SHD=200
31 05716 063077         HALT            ;AUTO INC OR DEC LOC 0
32                ;SEE NOT IR11 INTO SET AUTO
33                ;AC0=201 AUTO SET PREMATURELY
```

```
1@102 N2LOG
01
02
03                ;NOW TEST DEFER VIA AUTO LOC 20
04                ;FIRST TIME FOR AUTO
05                ;IF IT DOESN'T CLEAR GOOD LUCK +1 INST'S STARTS
06 05717 024077 STA09:  LDA 1,K300
07 05720 044020         STA 1,20        ;PREPARE REG'S
08 05721 120400         NEG 1,0         ;(20) 300 AND 277=320
09 05722 040301         STA 0,301       ;(301)=-300
10 05723 044300         STA 1,300
11 05724 044277         STA 1,277
12 05725 036020         LDA 3,@20       ;FIRST TIME AUTO
13 05726 116414         SUB# 0,3,SZR    ;(301) 0 AND AC3 SHD=-300
14 05727 063077         HALT            ;AUTO (@20) FAILED LDA
15 05730 030020         LDA 2,20
16 05731 125400         INC 1,1
17 05732 146414         SUB# 2,1,SZR    ;(20) SHD +1 TO=301
18 05733 063077         HALT            ;@20 DID NOT +1
19                ;AUTO DEC COULD HAVE SET SEE "NOT ALU12" AND SET AUTO
20                ;CONTENTS OF LOC 20 WILL=277
21                ;OR IF DEFER CLRS PREMATURE AC3 WILL=301
22                ;SEE "SET AUTO" INTO CLR DEFER TO BLOCK @ TO DEFER
23
24                ;NOW TEST AUTO DEC @30
25                ;FIRST TIME FOR AUTO DEC
26 05734 024063 STA10:  LDA 1,K200      ;NEXT STA COULD HURT IR12=1
27 05735 044030         STA 1,30        ;NO SET AUTO SO AUTO DEC SHD=@
28 05736 134400         NEG 1,3         ;ALU 12 HAS=1 PREVIOUSLY THOUGH
29 05737 054177         STA 3,177       ;177=-200
30 05740 044200         STA 1,200       ;200 201=+200
31 05741 044201         STA 1,201
32 05742 022030         LDA 0,@30       ;FIRST AUTO DEC
33 05743 116414         SUB# 0,3,SZR    ;AC0 AND 3 SHD=-200
34 05744 063077         HALT            ;FIRST AUTO DEC FAILED
35 05745 020030         LDA 0,30
36 05746 115400         INC 0,3
37 05747 136414         SUB# 1,3,SZR
38 05750 063077         HALT            ;(30) NOT=177 AUTO DEC
39                ;IF CONTENTS 30=201 SEE ALU12,SET AUTO INTO AUTO DEC
```

```
@103 N2LOG
01
02
03                      ;CASCADE DEFERS THROUGH 0 AND 1
04                      ;FIRST DEFER DEFERRED
05 05751 102620 STA11:  SUBZR 0,0
06 05752 101400         INC 0,0             ;CREATE #1
07 05753 040000         STA 0,0             ;(LOC 0)=#1
08 05754 024077         LDA 1,K300          ;(LOC 1)=300
09 05755 044001         STA 1,1
10 05756 134400         NEG 1,3
11 05757 054300         STA 3,300           ;(300)=-300
12 05760 044301         STA 1,301           ;(301)=300
13 05761 044277         STA 1,277           ;(277)=300
14 05762 032000         LDA 2,#0            ;SHD ALSO DEFER #1 TO LOC 300
15 05763 156414         SUB# 2,3,SZR        ;AC2,3 SHD BOTH=-300
16 05764 063077         HALT                ;DEFER DEFERRED FAILED
17                      ;IF AC2=300 SEE NOT CPB0 INTO CLEAR DEFER
18                      ;CPB0=1 SHD INHIBIT CLR DEFER
19
20                      ;CASCADE DEFERS THROUGH 20 TO 37
21                      ;20 TO 27 START=#17+1 TO #20  (20) EVENT=#37
22                      ;30 TO 36=#21-1 TO #20
23                      ;37=300-1 TO 277
24
25 05765 030060 STA12:  LDA 2,K20           ;SET UP
26 05766 020100         LDA 0,KD17          ;AUTO REGISTERS
27 05767 176400         SUB 3,3             ;20 TO 37
28 05770 024101         LDA 1,KM8
29 05771 041000         STA 0,0,2           ;FIRST 20 TO 27=#17
30 05772 151400         INC 2,2             ;THEN 30 TO 37=#21
31 05773 125404         INC 1,1,SZR
32 05774 000775         JMP STA12+4
33 05775 174005         COM 3,3,SNR
34 05776 000403         JMP .+3
35 05777 020102         LDA 0,KD21
36 06000 000770         JMP STA12+3
37 06001 020077         LDA 0,K300
38 06002 041377         STA 0,-1,2          ;(37)=300
39 06003 040300         STA 0,300
40 06004 040301         STA 0,301
41 06005 040017         STA 0,17
42 06006 114400         NEG 0,3
43 06007 054277         STA 3,277
44 06010 027360         LDA 1,0-20,2        ;EFA #20-#'S THROUGH 37 TO 300
45 06011 136414         SUB# 1,3,SZR        ;AC1 AND 3 SHD=-300
46 06012 063077         HALT                ;CASCADED DEFERS AUTO FAILED
47 06013 021360         LDA 0,-20,2         ;GET (20)AGAIN
48 06014 024103         LDA 1,KD37          ;GET #37
49 06015 106414         SUB# 0,1,SZR
50 06016 063077         HALT                ;AUTO LOC 20 INCORRECT
51
52
53
54
55                      ;TEST JMP "0" TO BLOCK SETFETCH AND 2WRADR1
56
57 06017 020002 JMP02:  LDA 0,.+2
58 06020 115001         MOV 0,3,SKP
59 06021 006017         JMP02
60 06022 040000         STA 0,0             ;ADRS OF JMPTST TO LOC 0
```

```
@104 N2LOG
01 06023 002403         JMP @JMP2L
02 06024 063077         HALT                ;JMP 0 FAILED TO
03 06025 063077         HALT                ;JMP AT ALL
04 06026 106031 JMP2L:  0,.+3
05 06027 063077         HALT                ;0 WAS IGNORED
06 06030 063077         HALT                ;0,.+3 MAY BE SKIP ALSO
07 06031 000032         .+1
08 06032 116414         SUB# 0,3,SZR        ;AC0 OR 3 CHANGED ON A JMP0
09 06033 063077         HALT
10
11                      ;JMP SHOULD NOT GENERATE SETSKIP "JMP 0"
12 06034 020413 JMP03:  LDA 0,JM3K          ;JMP #300
13 06035 040001         STA 0,1             ;TO LOC 1
14 06036 101400         INC 0,0
15 06037 040000         STA 0,0             ;JMP #301 TO 0
16 06040 024413         LDA 1,JM3R+1
17 06041 044300         STA 1,300           ;ERROR RETU TO LOC 1
18 06042 125400         INC 1,1
19 06043 044301         STA 1,301           ;OK RETU TO LOC 0
20 06044 002110         JMP @K0
21 06045 063077         HALT
22 06046 063077         HALT
23 06047 002300 JM3K:   JMP #300
24 06050 006051         .+1
25 06051 063077         HALT                ;JMP @K0 ZR,SETSKP
26
27                      ;LDA INDEXED WITH BIT 0=1
28                      ;SHOULD NOT DEFER
29
30 06052 030077 LDA36:  LDA 2,K300
31 06053 144400         NEG 2,1
32 06054 044301         STA 1,301
33 06055 044277         STA 1,277
34 06056 141400         INC 2,0
35 06057 040300         STA 0,300           ;0 WILL GET 301 IN ERROR
36 06060 153240         ADDOR 2,2           ;SET BIT 0=1
37 06061 035000         LDA 3,0,2           ;IR5=0 SHD NOT DEFER
38 06062 116414         SUB# 0,3,SZR
39 06063 063077         HALT                ;INDEX "CPB0" DEFERRED
```

```
1@105 N2LOG
01
02
03                      ;LDA AUTO REG 2@ SHOULD NOT DEFER
04                      ;WHEN IR5=0 AND (22) BIT 0=1
05
06 06064 030060 LDA37:  LDA 2,K2@
07 06065 034077         LDA 3,K3@@
08 06066 054300         STA 3,3@@
09 06067 054301         STA 3,3@1
10 06070 177240         ADDOR 3,3
11 06071 055000         STA 3,0,2
12 06072 153240         ADDOR 2,2
13 06073 021000         LDA 0,0,2
14
15                      ;JSR WITH BIT 0=1 IN INDEX REG
16                      ;SHOULD NOT DEFER AND SHD NOT
17                      ;ALLOW BIT 0 INTO AC3
18
19 06074 020402 JSR02:  LDA 0,.+2
20 06075 152621         SUBZR 2,2,SKP
21 06076 006112         JS02K
22 06077 151400         INC 2,2         ;COM 0,0,SKP
23 06100 050000         STA 2,0         ;TO LOC 0=#1
24 06101 024077         LDA 1,K3@@
25 06102 137240         ADDOR 1,3
26 06103 044001         STA 1,1         ;#3@@ (TO KEEP INVALID #)
27 06104 040300         STA 0,3@@       ;DEFER INCORRECT RETURN
28 06105 034107         LDA 3,KJRET     ;(JMP 0,3)
29 06106 054002         STA 3,2         ;TO GET US BACK
30 06107 100000         COM 0,0
31 06110 005377         JSR -1,2        ;(2) BIT 0=1 IR5=0 (JSR 0)
32                      ;ABOVE JSR SHD NOT DEFER JMP 0,3 IN LOC 2
33                      ;SHD BRING US BACK TO JSR +1
34 06111 175112         MOVL# 3,3,SZC   ;AC3 BIT 0 SHD=0
35 06112 063077 JS02K:  HALT            ;DEFERRED OR AC3 BIT 0=1
36 06113 126000         ADC 1,1
37 06114 107000         ADD 0,1         ;AC1=JS K-1
38 06115 136414         SUB# 1,3,SZR    ;AC3 SHD=JSR+1
39 06116 063077         HALT            ;WRONG ADDRS IN AC3
40
41                      ;TEST ISZ TO NOT ALTER AC'S
42                      ;TEMP @@
43 06117 102120 ISZ02:  ADCZL 0,0
44 06120 040000         STA 0,0         ;(0)=-1
45 06121 102400         SUB 0,0
46 06122 126400         SUB 1,1         ;AC'S ALL=0
47 06123 152400         SUB 2,2
48 06124 176400         SUB 3,3
49 06125 010000         ISZ 0
50 06126 101004         MOV 0,0,SZR
51 06127 063077         HALT            ;AC0 NOT=0 OR ISZ SKPD
52 06130 123000         ADD 1,0
53 06131 143000         ADD 2,0
54 06132 163014         ADD# 3,0,SZR
55 06133 063077         HALT            ;AC1-2-OR 3 ALTERED "ISZ"
56 06134 020000         LDA 0,0
57 06135 100004         COM 0,0,SZR     ;(0) SHD = -1 (SEE RMW)
58 06136 063077         HALT            ;ISZ 0 DID NOT CHNG (0)
```

```
1@106 N2LOG
01
02                      ;TEST AGAIN 0'S TO NOT ALTER ONES
03 06137 102400 ISZ03:  SUB 0,0
04 06140 040000         STA 0,0
05 06141 100000         COM 0,0
06 06142 125000         ADC 1,1
07 06143 152000         ADC 2,2
08 06144 176040         ADCO 3,3
09 06145 010000         ISZ 0
10 06146 175404         INC 3,3,SZR
11 06147 063077         HALT
12 06150 136000         ADC 1,3
13 06151 156003         ADC 2,3,SNC
14 06152 116014         ADC# 0,3,SZR
15 06153 063077         HALT                    ;AC1-2 OR 3
16
17                      ;TEST DSZ TO NOT ALTER AC'S
18                      ;TEMP REG IS USED IN DSZ
19 06154 122000 DSZ02:  ADC 0,0
20 06155 040000         STA 0,0
21 06156 100000         COM 0,0
22 06157 104400         NEG 0,1                 ;ALL AC'S=0
23 06160 130400         NEG 1,2
24 06161 154400         NEG 2,3
25 06162 010000         DSZ 0                   ;-1 TO -2
26 06163 150404         NEG 2,2,SZR
27 06164 063077         HALT                    ;DSZ CHANGED AC2
28 06165 132400         SUB 1,2
29 06166 112400         SUB 0,2
30 06167 172414         SUB# 3,2,SZR
31 06170 063077         HALT                    ;DSZ CHANGED AC0-1 OR 3
32
33                      ;AGAIN TEST DSZ TO NOT ALTER AC'S
34 06171 175520 DSZ03:  SUBZL 3,3               ;.+1
35 06172 050000         STA 3,0                 ;TO LOC 0
36 06173 154400         NEG 3,1
37 06174 174240         COMOR 3,2               ;AC'S=-1
38 06175 176000         ADC 3,3
39 06176 161240         MOVOR 3,0
40 06177 010000         DSZ 0
41 06200 063077         HALT                    ;DSZ DID NOT SKP
42 06201 160400         SUB 3,1
43 06202 140000         ADC 2,1
44 06203 100014         ADC# 0,1,SZR
45 06204 063077         HALT                    ;AC0 1 2 OR 3 ALTERED BY DSZ
46 06205 020000         LDA 0,0
47 06206 101004         MOV 0,0,SZR             ;(0) CHANGED TO = 0?
48 06207 063077         HALT                    ;DSZ DID NOT CHNG (0)
```

```
10107 N2LOG
01
02
03                      ;AUTO INCREMENT SHD NOT ALTER AC'S
04                      ;TEMP IS USED FOR AUTO INC
05 06210 152220 STA13:  ADCZR 2,2
06 06211 050023         STA 2,23
07 06212 126000         SUB 1,1
08 06213 044000         STA 1,0
09 06214 020104         LDA 0,KCBE      ;125252 (EVEN BITS)
10 06215 100000         COM 0,1
11 06216 111000         MOV 0,2
12 06217 154000         COM 2,3
13 06220 042023         STA 0,@23       ;125252 GOES TO LOC 0
14 06221 117000         ADD 0,3
15 06222 133000         ADD 1,2
16 06223 156414         SUB# 2,3,SZR
17 06224 063077         HALT            ;AUTO INC ALTERED AN AC
18
19                      ;AUTO DEC SHD NOT ALTER ANY AC
20 06225 176520 STA14:  SUBZL 3,3       ;.+1
21 06226 054037         STA 3,37        ;TO AN AUTO DEC
22 06227 020105         LDA 2,KCBO      ;052525
23 06230 140000         COM 2,0
24 06231 105000         MOV 0,1
25 06232 134000         COM 1,3
26 06233 052037         STA 2,@37       ;AUTO DEC TO LOC 0
27 06234 106414         SUB# 0,1,SZR
28 06235 063077         HALT            ;AC0 OR 1 ALTERED
29 06236 156414         SUB# 2,3,SZR
30 06237 063077         HALT            ;AC2 OR 3 ALTERED
31
32                      ;AN LDA WITH IR12=1 SHD NOT "NO LOAD"
33                      ;CALC=0
34
35 06240 102000 LDA3R:  ADC 0,0
36 06241 040030         STA 0,30
37 06242 100000         COM 0,0
38 06243 020030         LDA 0,30        ;IR R=1 SHD STILL LOAD
39 06244 100014         COM# 0,0,SZR
40 06245 063077         HALT            ;IR R=1 STOPPED 2WEN
```

```
10108 N2LOG
01
02
03                      ;TEST ISZ AND DSZ TO NOT SKIP
04                      ;DEFINE MACRO FOR TESTING
05                              .MACRO ISDST
06                      ;TEST OF ISZ DSZ TO  NOT SKIP AROUND A2
07                    ;IDSA1:
08                              LDA 0,KA2       ;GET A2
09                              STA 0,IDA1K
10                              ISZ IDA1K       ;+1
11                              DSZ IDA1K       ;-1
12                              DSZ IDA1K       ;-1
13                              ISZ IDA1K       ;+1
14                              LDA 1,IDA1K     ;SHD=A2 AGAIN
15                              SUB# 0,1,SZR
16                              HALT            ;IS DS SEQ FAILED A2
17                              MOV 0,0,SKP
18                    IDA1K:    0
19                    KA2:      %
20
21                              ISDST 00,2
22                      ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 2
23                    ;IDS00:
24 06246 020055                 LDA 0,K2        ;GET 2
25 06247 040411                 STA 0,ID00K
26 06250 014410                 ISZ ID00K       ;+1
27 06251 014407                 DSZ ID00K       ;-1
28 06252 014406                 DSZ ID00K       ;-1
29 06253 014405                 ISZ ID00K       ;+1
30 06254 024404                 LDA 1,ID00K     ;SHD=2 AGAIN
31 06255 106414                 SUB# 0,1,SZR
32 06256 063077                 HALT            ;IS DS SEQ FAILED 2
33 06257 101001                 MOV 0,0,SKP
34 06260 000000 ID00K:  0
35                              ISDST 01,4
36                      ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 4
37                    ;IDS01:
38 06261 020056                 LDA 0,K4        ;GET 4
39 06262 040411                 STA 0,ID01K
40 06263 014410                 ISZ ID01K       ;+1
41 06264 014407                 DSZ ID01K       ;-1
42 06265 014406                 DSZ ID01K       ;-1
43 06266 014405                 ISZ ID01K       ;+1
44 06267 024404                 LDA 1,ID01K     ;SHD=4 AGAIN
45 06270 106414                 SUB# 0,1,SZR
46 06271 063077                 HALT            ;IS DS SEQ FAILED 4
47 06272 101001                 MOV 0,0,SKP
48 06273 000000 ID01K:  0
49                              ISDST 02,10
50                      ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 10
51                    ;IDS02:
52 06274 020057                 LDA 0,K10       ;GET 10
53 06275 040411                 STA 0,ID02K
54 06276 014410                 ISZ ID02K       ;+1
55 06277 014407                 DSZ ID02K       ;-1
56 06300 014406                 DSZ ID02K       ;-1
57 06301 014405                 ISZ ID02K       ;+1
58 06302 024404                 LDA 1,ID02K     ;SHD=10 AGAIN
59 06303 106414                 SUB# 0,1,SZR
60 06304 063077                 HALT            ;IS DS SEQ FAILED 10
```

```
0109 N2LOG
01 06305 101001          MOV 0,0,SKP
02 06306 000000 ID02K:   0
03                       ISDST 03,20
04                  ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 20
05                 ;IDS03:
06 06307 020060          LDA 0,K20       ;GET 20
07 06310 040411          STA 0,ID03K
08 06311 010410          ISZ ID03K       ;+1
09 06312 014407          DSZ ID03K       ;-1
10 06313 014406          DSZ ID03K       ;-1
11 06314 010405          ISZ ID03K       ;+1
12 06315 024404          LDA 1,ID03K     ;SHD=20 AGAIN
13 06316 106414          SUB# 0,1,SZR
14 06317 063077          HALT            ;IS DS SEQ FAILED 20
15 06320 101001          MOV 0,0,SKP
16 06321 000000 ID03K:   0
17                       ISDST 04,40
18                  ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 40
19                 ;IDS04:
20 06322 020061          LDA 0,K40       ;GET 40
21 06323 040411          STA 0,ID04K
22 06324 010410          ISZ ID04K       ;+1
23 06325 014407          DSZ ID04K       ;-1
24 06326 014406          DSZ ID04K       ;-1
25 06327 010405          ISZ ID04K       ;+1
26 06330 024404          LDA 1,ID04K     ;SHD=40 AGAIN
27 06331 106414          SUB# 0,1,SZR
28 06332 063077          HALT            ;IS DS SEQ FAILED 40
29 06333 101001          MOV 0,0,SKP
30 06334 000000 ID04K:   0
31                       ISDST 05,100
32                  ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 100
33                 ;IDS05:
34 06335 020062          LDA 0,K100      ;GET 100
35 06336 040411          STA 0,ID05K
36 06337 010410          ISZ ID05K       ;+1
37 06340 014407          DSZ ID05K       ;-1
38 06341 014406          DSZ ID05K       ;-1
39 06342 010405          ISZ ID05K       ;+1
40 06343 024404          LDA 1,ID05K     ;SHD=100 AGAIN
41 06344 106414          SUB# 0,1,SZR
42 06345 063077          HALT            ;IS DS SEQ FAILED 100
43 06346 101001          MOV 0,0,SKP
44 06347 000000 ID05K:   0
45                       ISDST 06,200
46                  ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 200
47                 ;IDS06:
48 06350 020063          LDA 0,K200      ;GET 200
49 06351 040411          STA 0,ID06K
50 06352 010410          ISZ ID06K       ;+1
51 06353 014407          DSZ ID06K       ;-1
52 06354 014406          DSZ ID06K       ;-1
53 06355 010405          ISZ ID06K       ;+1
54 06356 024404          LDA 1,ID06K     ;SHD=200 AGAIN
55 06357 106414          SUB# 0,1,SZR
56 06360 063077          HALT            ;IS DS SEQ FAILED 200
57 06361 101001          MOV 0,0,SKP
58 06362 000000 ID06K:   0
59                       ISDST 07,400
60                  ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 400
```

```
0110 N2LOG
01                 ;IDS07:
02 06363 020064          LDA 0,K400      ;GET 400
03 06364 040411          STA 0,ID07K
04 06365 010410          ISZ ID07K       ;+1
05 06366 014407          DSZ ID07K       ;-1
06 06367 014406          DSZ ID07K       ;-1
07 06370 010405          ISZ ID07K       ;+1
08 06371 024404          LDA 1,ID07K     ;SHD=400 AGAIN
09 06372 106414          SUB# 0,1,SZR
10 06373 063077          HALT            ;IS DS SEQ FAILED 400
11 06374 101001          MOV 0,0,SKP
12 06375 000000 ID07K:   0
13                       ISDST 08,1000
14                  ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 1000
15                 ;IDS08:
16 06376 020065          LDA 0,K1000     ;GET 1000
17 06377 040411          STA 0,ID08K
18 06400 010410          ISZ ID08K       ;+1
19 06401 014407          DSZ ID08K       ;-1
20 06402 014406          DSZ ID08K       ;-1
21 06403 010405          ISZ ID08K       ;+1
22 06404 024404          LDA 1,ID08K     ;SHD=1000 AGAIN
23 06405 106414          SUB# 0,1,SZR
24 06406 063077          HALT            ;IS DS SEQ FAILED 1000
25 06407 101001          MOV 0,0,SKP
26 06410 000000 ID08K:   0
27                       ISDST 09,2000
28                  ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 2000
29                 ;IDS09:
30 06411 020066          LDA 0,K2000     ;GET 2000
31 06412 040411          STA 0,ID09K
32 06413 010410          ISZ ID09K       ;+1
33 06414 014407          DSZ ID09K       ;-1
34 06415 014406          DSZ ID09K       ;-1
35 06416 010405          ISZ ID09K       ;+1
36 06417 024404          LDA 1,ID09K     ;SHD=2000 AGAIN
37 06420 106414          SUB# 0,1,SZR
38 06421 063077          HALT            ;IS DS SEQ FAILED 2000
39 06422 101001          MOV 0,0,SKP
40 06423 000000 ID09K:   0
41                       ISDST 10,4000
42                  ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 4000
43                 ;IDS10:
44 06424 020067          LDA 0,K4000     ;GET 4000
45 06425 040411          STA 0,ID10K
46 06426 010410          ISZ ID10K       ;+1
47 06427 014407          DSZ ID10K       ;-1
48 06430 014406          DSZ ID10K       ;-1
49 06431 010405          ISZ ID10K       ;+1
50 06432 024404          LDA 1,ID10K     ;SHD=4000 AGAIN
51 06433 106414          SUB# 0,1,SZR
52 06434 063077          HALT            ;IS DS SEQ FAILED 4000
53 06435 101001          MOV 0,0,SKP
54 06436 000000 ID10K:   0
55                       ISDST 11,10K
56                  ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 10K
57                 ;IDS11:
58 06437 020070          LDA 0,K10K      ;GET 10K
59 06440 040411          STA 0,ID11K
60 06441 010410          ISZ ID11K       ;+1
```

```
@111 N2LOG
01 06442 014407          DSZ ID11K        ;-1
02 06443 014406          DSZ ID11K        ;-1
03 06444 010405          ISZ ID11K        ;+1
04 06445 024404          LDA 1,ID11K      ;SHD=10K AGAIN
05 06446 106414          SUB# 0,1,SZR
06 06447 063077          HALT             ;IS DS SEQ FAILED 10K
07 06450 101001          MOV 0,0,SKP
08 06451 000000 ID11K:   0
09                       ISDST 12,20K
10                 ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 20K
11                 ;IDS12:
12 06452 020071          LDA 0,K20K       ;GET 20K
13 06453 040411          STA 0,ID12K
14 06454 010410          ISZ ID12K        ;+1
15 06455 014407          DSZ ID12K        ;-1
16 06456 014406          DSZ ID12K        ;-1
17 06457 010405          ISZ ID12K        ;+1
18 06460 024404          LDA 1,ID12K      ;SHD=20K AGAIN
19 06461 106414          SUB# 0,1,SZR
20 06462 063077          HALT             ;IS DS SEQ FAILED 20K
21 06463 101001          MOV 0,0,SKP
22 06464 000000 ID12K:   0
23                       ISDST 13,40K
24                 ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 40K
25                 ;IDS13:
26 06465 020072          LDA 0,K40K       ;GET 40K
27 06466 040411          STA 0,ID13K
28 06467 010410          ISZ ID13K        ;+1
29 06470 014407          DSZ ID13K        ;-1
30 06471 014406          DSZ ID13K        ;-1
31 06472 010405          ISZ ID13K        ;+1
32 06473 024404          LDA 1,ID13K      ;SHD=40K AGAIN
33 06474 106414          SUB# 0,1,SZR
34 06475 063077          HALT             ;IS DS SEQ FAILED 40K
35 06476 101001          MOV 0,0,SKP
36 06477 000000 ID13K:   0
37                       ISDST 14,100K
38                 ;TEST OF ISZ DSZ TO  NOT SKIP AROUND 100K
39                 ;IDS14:
40 06500 020073          LDA 0,K100K      ;GET 100K
41 06501 040411          STA 0,ID14K
42 06502 010410          ISZ ID14K        ;+1
43 06503 014407          DSZ ID14K        ;-1
44 06504 014406          DSZ ID14K        ;-1
45 06505 010405          ISZ ID14K        ;+1
46 06506 024404          LDA 1,ID14K      ;SHD=100K AGAIN
47 06507 106414          SUB# 0,1,SZR
48 06510 063077          HALT             ;IS DS SEQ FAILED 100K
49 06511 101001          MOV 0,0,SKP
50 06512 000000 ID14K:   0
51
52                 ;TEST AEQB TO REALLY ASSERT FOR BIT 7
53                 ;CAN ONLY BE TESTED VIA # 420 "SUM 7" IS OTHER ZR AND
54 06513 030106 AEQB7:   LDA 2,K420       ;TO GET AT 420
55 06514 024077          LDA 1,K300       ;TEST CONSTANT
56 06515 045000          STA 1,0,2        ;(420)=300
57 06516 044277          STA 1,277        ;AUTO DEC SHOULDN'T
58 06517 120400          NEG 1,0
59 06520 040300          STA 0,300        ;(300)=-300
60 06521 044301          STA 1,301
```

```
@112 N2LOG
01 06522 037000          LDA 3,@0,2       ;
02 06523 162414          SUB# 3,0,SZR     ;420 SHD NOT BE AUTO REG
03 06524 063077          HALT             ;LDA @420 "AEQB" FAILED
04 06525 021000          LDA 0,0,2        ;GET (420) SHD STILL=300
05 06526 106414          SUB# 0,1,SZR
06 06527 063077          HALT             ;(420) WERE ALTERED
07
08
09
10                 ;PROCESSOR I/O INSTR TESTS
11
12 06530 102620          SUBZR 0,0
13 06531 040001          STA 0,1          ;INTA'S WILL @0
14                 ;ION SHD=0 NO SKIP ON BUSY NON ZERO
15 06532 063477 IO.00:   SKPBN CPU        ;ION=0 SHD NOT SKP
16 06533 101001          MOV 0,0,SKP
17 06534 063077          HALT             ;IR8 IR9=00 NO SKIP BN
18                 ;POWER LOW SHD=0 NO SKIP ON DONE NON ZERO
19 06535 063677 IO.01:   SKPDN CPU        ;SHD NOT SKP
20 06536 101001          MOV 0,0,SKP      ;DIDN'T IR8 IR9=10
21 06537 063077          HALT             ;SEE PWR LOW=1(SHDN'T)
22
23                 ;SKPBZ TO SKP ION=0 FIRST IO SKP TRUE
24 06540 063577 IO.02:   SKPBZ CPU        ;IR8 IR9=01
25 06541 063077          HALT             ;BUSY=0 DID NOT SKP
26                 ;TEST SKPDZ POWER LOW SHD=0
27 06542 063777 IO.03:   SKPDZ CPU        ;IR8 IR9=11
28 06543 063077          HALT             ;DONE=0 NO SKP(PWR LOW)
29                 ;NIO SHD NEITHER SKP NOR ALTER ANY AC'S
30 06544 122000 IO.04:   ADC 0,0
31 06545 125000          MOV 0,1          ;ALL AC'S=-1
32 06546 131000          MOV 1,2
33 06547 155000          MOV 2,3
34 06550 060077          NIO CPU          ;MAKE SURE IO SKP=0
35 06551 122001          ADC 1,0,SKP
36 06552 063077          HALT             ;NIO CPU SKIPPED
37 06553 156000          ADC 2,3
38 06554 162414          SUB# 3,0,SZR
39 06555 063077          HALT             ;NIO CHANGED AN AC
40
41                       .MACRO IOTS1
42                 ;DIA6 A2, CPU SHOULD ONLY ALTER AC=2
43                 ;IO.A1:
44                       ADC 0,0
45                       MOV 0,1          ;ALL AC'S=-1
46                       MOV 0,2
47                       MOV 0,3
48                       DIA6 A2,CPU      ;A7 A2
49                       ADC A3,A4,SKP    ;-1+0 SHD=-1
50                       HALT             ;DIA6 SKPD
51                       SUB# A5,A4,SZR
52                       HALT             ;AC=3,A4OR=5 ALTERED
53                       COM# A2,A2,SNR   ;DID AC=2 CHANGE?
54                       HALT             ;AC=2 NOT LOADED
55                 %
56
57                       IOTS1 B5,0,1,2,3,A,READS
58                 ;DIA 0, CPU SHOULD ONLY ALTER AC0
59                 ;IO.B5:
60 06556 122400          ADC 0,0
```

```
 0113 N2LOG
01 00557 105000          MOV 0,1          ;ALL AC'S=-1
02 00560 111000          MOV 0,2
03 00561 115000          MOV 0,3
04 00562 060477          DIA 0,CPU        ;READS 0
05 00563 132001          ADC 1,2,SKP      ;-1+0 SHD=-1
06 00564 063077          HALT             ;DIA SKPD
07 00565 172414          SUB# 3,2,SZR
08 00566 063077          HALT             ;AC1,2OR3 ALTERED
09 00567 100015          COM# 0,0,SNR     ;DID AC0 CHANGE?
10 00570 063077          HALT             ;AC0 NOT LOADED
11                       IOTS1 06,1,0,2,3,A,READS
12                  ;DIA 1, CPU SHOULD ONLY ALTER AC1
13                ;IO.06:
14 00571 102000          ADC 0,0
15 00572 105000          MOV 0,1          ;ALL AC'S=-1
16 00573 111000          MOV 0,2
17 00574 115000          MOV 0,3
18 00575 064477          DIA 1,CPU        ;READS 1
19 00576 112001          ADC 0,2,SKP      ;-1+0 SHD=-1
20 00577 063077          HALT             ;DIA SKPD
21 00600 172414          SUB# 3,2,SZR
22 00601 063077          HALT             ;AC0,2OR3 ALTERED
23 00602 124015          COM# 1,1,SNR     ;DID AC1 CHANGE?
24 00603 063077          HALT             ;AC1 NOT LOADED
25                       IOTS1 07,2,3,0,1,A,READS
26                  ;DIA 2, CPU SHOULD ONLY ALTER AC2
27                ;IO.07:
28 00604 102000          ADC 0,0
29 00605 105000          MOV 0,1          ;ALL AC'S=-1
30 00606 111000          MOV 0,2
31 00607 115000          MOV 0,3
32 00610 070477          DIA 2,CPU        ;READS 2
33 00611 162001          ADC 3,0,SKP      ;-1+0 SHD=-1
34 00612 063077          HALT             ;DIA SKPD
35 00613 122414          SUB# 1,0,SZR
36 00614 063077          HALT             ;AC3,0OR1 ALTERED
37 00615 150015          COM# 2,2,SNR     ;DID AC2 CHANGE?
38 00616 063077          HALT             ;AC2 NOT LOADED
39                       IOTS1 08,3,0,1,2,A,READS
40                  ;DIA 3, CPU SHOULD ONLY ALTER AC3
41                ;IO.08:
42 00617 102000          ADC 0,0
43 00620 105000          MOV 0,1          ;ALL AC'S=-1
44 00621 111000          MOV 0,2
45 00622 115000          MOV 0,3
46 00623 074477          DIA 3,CPU        ;READS 3
47 00624 106001          ADC 0,1,SKP      ;-1+0 SHD=-1
48 00625 063077          HALT             ;DIA SKPD
49 00626 146414          SUB# 2,1,SZR
50 00627 063077          HALT             ;AC0,1OR2 ALTERED
51 00630 174015          COM# 3,3,SNR     ;DID AC3 CHANGE?
52 00631 063077          HALT             ;AC3 NOT LOADED
53                       IOTS1 09,0,1,2,3,B,INTA
54                  ;DIB 0, CPU SHOULD ONLY ALTER AC0
55                ;IO.09:
56 00632 102000          ADC 0,0
57 00633 105000          MOV 0,1          ;ALL AC'S=-1
58 00634 111000          MOV 0,2
59 00635 115000          MOV 0,3
60 00636 061477          DIB 0,CPU        ;INTA 0
```

```
 0114 N2LOG
01 00637 132001          ADC 1,2,SKP      ;-1+0 SHD=-1
02 00640 063077          HALT             ;DIB SKPD
03 00641 172414          SUB# 3,2,SZR
04 00642 063077          HALT             ;AC1,2OR3 ALTERED
05 00643 100015          COM# 0,0,SNR     ;DID AC0 CHANGE?
06 00644 063077          HALT             ;AC0 NOT LOADED
07                       IOTS1 10,1,0,3,2,B,INTA
08                  ;DIB 1, CPU SHOULD ONLY ALTER AC1
09                ;IO.10:
10 00645 102000          ADC 0,0
11 00646 105000          MOV 0,1          ;ALL AC'S=-1
12 00647 111000          MOV 0,2
13 00650 115000          MOV 0,3
14 00651 065477          DIB 1,CPU        ;INTA 1
15 00652 112001          ADC 0,3,SKP      ;-1+0 SHD=-1
16 00653 063077          HALT             ;DIB SKPD
17 00654 156414          SUB# 2,3,SZR
18 00655 063077          HALT             ;AC0,3OR2 ALTERED
19 00656 124015          COM# 1,1,SNR     ;DID AC1 CHANGE?
20 00657 063077          HALT             ;AC1 NOT LOADED
21                       IOTS1 11,2,3,1,0,B,INTA
22                  ;DIB 2, CPU SHOULD ONLY ALTER AC2
23                ;IO.11:
24 00660 102000          ADC 0,0
25 00661 105000          MOV 0,1          ;ALL AC'S=-1
26 00662 111000          MOV 0,2
27 00663 115000          MOV 0,3
28 00664 071477          DIB 2,CPU        ;INTA 2
29 00665 166001          ADC 3,1,SKP      ;-1+0 SHD=-1
30 00666 063077          HALT             ;DIB SKPD
31 00667 106414          SUB# 0,1,SZR
32 00670 063077          HALT             ;AC3,1OR0 ALTERED
33 00671 150015          COM# 2,2,SNR     ;DID AC2 CHANGE?
34 00672 063077          HALT             ;AC2 NOT LOADED
35                       IOTS1 12,3,2,0,1,B,INTA
36                  ;DIB 3, CPU SHOULD ONLY ALTER AC3
37                ;IO.12:
38 00673 102000          ADC 0,0
39 00674 105000          MOV 0,1          ;ALL AC'S=-1
40 00675 111000          MOV 0,2
41 00676 115000          MOV 0,3
42 00677 075477          DIB 3,CPU        ;INTA 3
43 00700 142001          ADC 2,0,SKP      ;-1+0 SHD=-1
44 00701 063077          HALT             ;DIB SKPD
45 00702 122414          SUB# 1,0,SZR
46 00703 063077          HALT             ;AC2,0OR1 ALTERED
47 00704 174015          COM# 3,3,SNR     ;DID AC3 CHANGE?
48 00705 063077          HALT             ;AC3 NOT LOADED
49
```

```
;0115 N2LOG
01
02
03                      ;DOA 0, CPU SHOULD NOT HANG "OUT TIME"
04                      ;OUT GOES THROUGH T/S "TDO"
05                      ;FIRST TIME FOR ANY DOA -B OR C
06 06706 176000 IO.13:  ADC 3,3
07 06707 102000         ADC 0,0
08 06710 061077         DOA 0,CPU       ;SHD NOT SKP HALT OR ALTER AC'S
09 06711 100004         COM 0,0,SZR
10 06712 063077         HALT            ;DOA SKPD OR ALTERED AC0
11 06713 174004         COM 3,3,SZR
12 06714 063077         HALT            ;DOA ALTERED AC3
13
14                      ;DETERMINE WHICH PATH TO TAKE
15                      ;IN TESTING FROM THIS POINT ON
16                      ;TTO "DONE" IS USED FOR "TRUE" INTERRUPT TESTING
17                      ;TTO DONE=0 AND BUSY=0 "FALSE" INTERRUPT TESTS
18                      ;TTO DONE=0 AND BUSY=1 LOOP BACK TO A1A
19 06715 176000 IOX00:  ADC 3,3         ;SET PASS SWITCH
20 06716 063611         SKPDN TTO       ;DONE=?
21 06717 000414         JMP IOX01       ;=0
22 06720 063511         SKPBZ TTO       ;DONE=1  BUSY MUST=0
23 06721 063077         HALT            ;BUSY=0 OR DONE=1 FAILED
24 06722 063711         SKPDZ TTO       ;DONE=2 Z SHD NOT SKP
25 06723 101001         MOV 0,0,SKP
26 06724 063077         HALT            ;"DZ" ERR OR MAYBE "DN"
27 06725 063411         SKPBN TTO       ;DONE=1  BUSY CAN'T=1
28 06726 002403         JMP @IOX01-2    ;OK TO DO INTR TSTS
29 06727 063077         HALT            ;TTO IS BUSY NOT
30 06730 000765         JMP IOX00
31 06731 007143         INTDS
32 06732 000501         A1A             ;START OF LOGIC TEST
33 06733 063511 IOX01:  SKPBZ TTO       ;NO SKP IS WAITING
34 06734 002776         JMP .-2         ;DON'T WAIT FOR TTO DONE
35 06735 175404         INC 3,3,SZR
36 06736 063077         HALT            ;2ND TRY
37 06737 063711         SKPDZ TTO       ;FINITE TIME TWXT "DN" AND "BZ"
38 06740 000756         JMP IOX00+1     ;MAYBE DONE=1 (TIME LAPSE)
                        ;TTO DONE AND BUSY=0
                        ;PERFORM TESTS THAT REQUIRE  INTERRUPT TO BE FALSE
41
42 06741 102620 NIN00:  SUBZR 0,0
43 06742 040001         STA 0,1         ;1=00
44 06743 060177         NIOS CPU        ;1 TO ION "SHD NOT SKP"
45 06744 063477         SKPBN CPU       ;BUSY SHD=1 FOR CPU
46 06745 063077         HALT            ;ION DID NOT SET (NIOS SKPD)
47 06746 063477         SKPBN CPU       ;ION=0 HERE IS INTR
48 06747 063077         HALT            ;SEE PI AND NOT INTR
                        ;THERE SHD BE NO INTR REQUESTS PENDING
                        ;NIOC SHD CLR ION SKPBZ SHD NOT SKP
51 06750 060177 NIN01:  NIOS CPU        ;1 TO ION
52 06751 063577         SKPBZ CPU       ;BUSY=1
53 06752 063477         SKPBN CPU       ;SHD NOT CLR ION
54 06753 063077         HALT            ;BZ SKPD OR BN DIDN'T
55 06754 060277 NIN02:  NIOC CPU        ;SHD CLR ION
56 06755 063477         SKPBN CPU       ;BUSY=0
57 06756 063577         SKPBZ CPU
58 06757 063077         HALT            ;"C" DID NOT CLR ION
59
```

```
;0116 N2LOG
01
02                      ;IORST SHD CLR ION
03
04 06760 060177 NIN03:  NIOS CPU
05 06761 062677         IORST           ;DICC 0,CPU
06 06762 063577         SKPBZ CPU
07 06763 063077         HALT            ;IORST FAILED CLR ION
08
09                      ;DIC SHD ONLY CLR IO BUS NOT ION
10 06764 060177 NIN04:  NIOS CPU
11 06765 062477         DIC 0,CPU       ;NO "C" ION SHD STILL=1
12 06766 063477         SKPBN CPU       ;IR8,9=00 DID ION CLR
13 06767 063077         HALT            ;DIS CLRD ION IR8,9=00
14                      ;SAME TEST WITH "P" SHD NOT CLR ION IR8,9=11
15 06770 060177 NIN05:  NIOS CPU
16 06771 062777         DICP 0,CPU      ;IR8,9=11 "P" NOT "C"
17 06772 063477         SKPBN CPU
18 06773 063077         HALT            ;"P" CLRD ION
19                      ;"P" PULSE SHD NOT SET ION
20 06774 060277 NIN06:  NIOC CPU
21 06775 060377         NIOP CPU        ;IR8,9=11 "P" NOT "S"
22 06776 063577         SKPBZ CPU
23 06777 063077         HALT            ;"P" SET ION
24                      ;"S" WITH ION=1 SHD LEAVE IT=1
25 07000 060177 NIN07:  NIOS CPU        ;1 TO ION
26 07001 062577         DICS 0,CPU      ;AGAIN WITH IORST
27 07002 063477         SKPBN CPU
28 07003 063077         HALT            ;2ND "S" CLRD ION
29                      ;ION=1 AND SKPDN ON DEV 0 SHD NOT SKIP
30 07004 062677 NIN08:  IORST
31 07005 060177         NIOS CPU        ;SET ION
32 07006 063600         SKPDN 0         ;DEV #0 SHD NOT SKP
33 07007 101001         MOV 0,0,SKP     ;OK
34 07010 063077         HALT            ;CPUINST IN IO SKIP
35
36                      ;TEST "AND'S" DECODING CPU INST FOR "FALSE"
37                      .MACRO IOTS2
38                  ;NINA1:
39                      IORST
40                      NIOS CPU        ;SET ION FOR DEV^2
41                      SKPBN ^2        ;TEST NOT BIT ^3
42                      MOV 0,0,SKP
43                      HALT            ;ONLY DEV 77 SHD SKP
44                  ;IF ABOVE HALT SEE BIT^3 INTO "CPU INST" AND'S
45                  %
46                      IOTS2 09,76,15
47                  ;NIN09:
48 07011 062677         IORST
49 07012 060177         NIOS CPU        ;SET ION FOR DEV76
50 07013 063476         SKPBN 76        ;TEST NOT BIT 15
51 07014 101001         MOV 0,0,SKP
52 07015 063077         HALT            ;ONLY DEV 77 SHD SKP
53                  ;IF ABOVE HALT SEE BIT15 INTO "CPU INST" AND'S
54                      IOTS2 10,75,14
55                  ;NIN10:
56 07016 062677         IORST
57 07017 060177         NIOS CPU        ;SET ION FOR DEV75
58 07020 063475         SKPBN 75        ;TEST NOT BIT 14
59 07021 101001         MOV 0,0,SKP
60 07022 063077         HALT            ;ONLY DEV 77 SHD SKP
```

```
0117 N2LOG
01                      ;IF ABOVE HALT SEE BIT14 INTO "CPU INST" AND'S
02                          IOTS2 11,73,13
03                      ;NIN11:
04 07023 062677             IORST
05 07024 060177             NIOS CPU            ;SET ION FOR DEV73
06 07025 063473             SKPBN 73            ;TEST NOT BIT 13
07 07026 101001             MOV 0,0,SKP
08 07027 063077             HALT                ;ONLY DEV 77 SHD SKP
09                      ;IF ABOVE HALT SEE BIT13 INTO "CPU INST" AND'S
10                          IOTS2 12,67,12
11                      ;NIN12:
12 07030 062677             IORST
13 07031 060177             NIOS CPU            ;SET ION FOR DEV67
14 07032 063467             SKPBN 67            ;TEST NOT BIT 12
15 07033 101001             MOV 0,0,SKP
16 07034 063077             HALT                ;ONLY DEV 77 SHD SKP
17                      ;IF ABOVE HALT SEE BIT12 INTO "CPU INST" AND'S
18                          IOTS2 13,57,11
19                      ;NIN13:
20 07035 062677             IORST
21 07036 060177             NIOS CPU            ;SET ION FOR DEV57
22 07037 063457             SKPBN 57            ;TEST NOT BIT 11
23 07040 101001             MOV 0,0,SKP
24 07041 063077             HALT                ;ONLY DEV 77 SHD SKP
25                      ;IF ABOVE HALT SEE BIT11 INTO "CPU INST" AND'S
26                          IOTS2 14,37,10
27                      ;NIN14:
28 07042 062677             IORST
29 07043 060177             NIOS CPU            ;SET ION FOR DEV37
30 07044 063437             SKPBN 37            ;TEST NOT BIT 10
31 07045 101001             MOV 0,0,SKP
32 07046 063077             HALT                ;ONLY DEV 77 SHD SKP
33                      ;IF ABOVE HALT SEE BIT10 INTO "CPU INST" AND'S
34
```

```
0118 N2LOG
01
02                      ;AN "S" PULSE WITH DEV 0 (NOT CPU INST)
03                      ;SHD NOT SET ION
04 07047 062677 NIN15:  IORST
05 07050 060100             NIOS 0              ;"NOT" CPU BUT "S"
06 07051 063577             SKPBZ CPU           ;SEE 9301 GENERATING SETION
07 07052 063077             HALT                ;ION=1 ILLEGAL (CPU INST NOT)
08
09                      ;A "C" PULSE WITH DEV 0 (NOT CPU INST) SHD NOT CLR ION
10 07053 062677 NIN16:  IORST
11 07054 060177             NIOS CPU
12 07055 060200             NIOC 0              ;NOT CPU BUT "C"
13 07056 063477             SKPBN CPU           ;ION SHD STILL=1
14 07057 063077             HALT                ;"C" CLRD ION (NOT CPU-DEV 0)
15
16                      ;IO SKIPS SHD NOT GET TO  PTS1 "S" SHD NOT BE GEN
17 07060 062677 NIN17:  IORST
18 07061 063577             SKPBZ CPU           ;IR8,9=01 BUT IS NOT "S"
19 07062 063077             HALT
20 07063 063577             SKPBZ CPU           ;ION SHD STILL=0
21 07064 063077             HALT                ;FIRST BZ GEN'D "S"
22
23                      ;IO SKIP "DN" SHD NOT="C" NO PTS1
24 07065 060177 NIN18:  NIOS CPU
25 07066 063677             SKPDN CPU           ;IR8,9=10 BUT IS NOT "C"
26 07067 101001             MOV 0,0,SKP         ;POWER LOW=0 SHD NOT SKP
27 07070 063077             HALT                ;DN SKP'D WITH ION=1
28 07071 063477             SKPBN CPU           ;ABOVE HALT SEE NOT IR8
29 07072 063077             HALT                ;"DN" CLRD ION
30                      ;SET UP ALL CONDITIONS FOR IO SKP EXCEPT IN/OUT TIME
31 07073 062677 NIN19:  IORST
32 07074 102420             SUBZ 0,0
33 07075 103577             ANDCL# 0,0,SBN      ;EVERYTHING=0 NO SKP
34 07076 101001             MOV 0,0,SKP
35 07077 063077             HALT                ;AND=SKPBZ CPU
36                      ;SET UP ALL CONDITIONS FOR NIOS CPU EXCEPT PTS1
37 07100 062677 NIN20:  IORST
38 07101 102040             ADCO 0,0
39 07102 100177             COMCL# 0,0,SBN      ;ALL=0 NO SKP
40 07103 063577             SKPBZ CPU           ;ION SHD STILL=0
41 07104 063077             HALT                ;COMCL#=NIOS CPU
42
43                      ;SET UP ALL CONDITIONS FOR NIOS CPU
44                      ;EXCEPT IO ALCEN=0
45 07105 062677 NIN21:  IORST
46 07106 020177             LDA 0,177           ;NO IOALCEN
47 07107 063577             SKPBZ CPU           ;SEE IOALCEN (NOT),PTS1
48 07110 063077             HALT                ;LDA=NIOS CPU
49                      ;SET UP ALL CONDITIONS FOR IO SKPBZ CPU EX(IN/OUT)
50 07111 176000 NIN22:  SUB 3,3             ;USING AN LDA
51 07112 054177             STA 3,177           ;MAKE SURE SKP DOESN'T SET
52 07113 054[illegible]     STA 3,0
53 07114 023577             LDA 0,#177,3        ;ALMOST AN SKPBZ CPU
54 07115 101004             MOV 0,0,SZR
55 07116 063077             HALT                ;LDA=SKPBZ CPU
56 07117 014121             DSZ PKR00
57 07120 002404             JMP @.+4
58 07121 020122             LDA 0,PKR01
59 07122 040121             STA 0,PKR00
60 07123 101001             MOV 0,0,SKP
```

```
 0119 N2LOG
01 07124 000501          A1A
```

```
10120 N2LOG
01
02
03                ;START DFL CODE TO TTO
04                ;FOR INTERRUPT TESTING WHEN DONE=1
05
06 07125 102000 TTO00:  ADC 0,0           ;-1
07 07126 061111         DOAS 0,TTO        ;OUT TO TTO
08 07127 063411         SKPBN TTO         ;BUSY SHD=1
09 07130 063077         HALT              ;NO SKP TTO "BN"
10 07131 063511         SKPBZ TTO         ;
11 07132 100004         COM 0,0,SZR
12 07133 063077         HALT              ;TTO "BZ" ERR
13 07134 063711         SKPDZ TTO         ;DONE SHD=0 TTO
14 07135 063077         HALT              ;TTO "DZ" ERR
15 07136 063611         SKPDN TTO         ;TTO DONE SHD=0
16 07137 000402         JMP @.+2          ;OK LOOP THROUGH TEST
17 07140 063077         HALT              ;TTO DONE=1 IN ERR
18 07141 000501         A1A
19
20 07142 007357         PASSC
21                ;TTO DONE=1 USE TO TEST INTERRUPTS
22 07143 020416 INT00:  LDA 0,INT0K
23 07144 021200         LDA 1,JMP3K
24 07145 033055         LDA 2,K2          ;SET UP FOR
25 07146 050001         STA 2,1           ;TEST FIRST
26 07147 044002         STA 1,2           ;REAL INTERRUPT
27 07150 044300         STA 0,300
28 07151 175400         SUB 3,3
29 07152 075077         DOB 3,CPU         ;0 MSKO
30 07153 054000         STA 3,0           ;0 ADRS 0
31 07154 060177         NIOS CPU          ;ION
32 07155 000401         JMP .+1           ;WAIT
33 07156 063077         HALT              ;INTERRUPT DID NOT OCCUR
34 07157 063077         HALT
35 07160 007156         .=2
36 07161 007162 INT0K:  .+1
37 07162 034000         LDA 3,0
38 07163 020775         LDA 0,INT0K-1
39 07164 116414         SUB# 0,3,SZR
40 07165 063077         HALT              ;(0) NOT=NIOS+2
```

```
;0121 N2LOG
01
02                    ;TEST TO MAKE SURE #IN LOC 1 WILL DEFER
03 07166 020055 INT01:  LDA 0,K2          ;AND KEEP DEFERING
04 07167 103240         ADDOR 0,0
05 07170 040001         STA 0,1           ;#2 ALSO=COM 0,0,SZC
06 07171 024120         LDA 1,JMP3K       ;JMP #300
07 07172 044003         STA 1,3           ;WILL EXECUTE IN ERR
08 07173 030014         LDA 2,INT1K       ;IF FETCH IS DIRECTLY TO 1
09 07174 050300         STA 2,300         ;OR 2ND DEFER FAILS
10 07175 151400         INC 2,2           ;LEGAL RET
11 07176 050004         STA 2,4           ;WILL BE IN 4
12 07177 103000         ADD 0,0           ;#4=COM 0,0,SZR (WON'T SKIP)
13 07200 103240         ADDOR 0,0
14 07201 040002         STA 0,2           ;#4 TO LOC 2
15 07202 101320         MOVZ 0,0          ;0 CRY JMP #300 IN0
16 07203 060177         NIOS CPU
17 07204 000401         JMP .+1           ;FIRST INTR #0
18 07205 063077         HALT
19 07206 063077         HALT
20 07207 007210 INT1K:  .+1
21 07210 063077         HALT              ;LOC 1 OR 2 EXECUTED
22                    ;ABOVE HALT INTERRUPT IS NOT DOING #1
23                    ;OR DEFER BIT IN LOC 1 WAS NOT RECOGNIZED
24
25                    ;ION/IOF SHOULD NOT INTR
26 07211 102400 INT02:  SUB 0,0
27 07212 040000         STA 0,0
28 07213 101240         MOVOR 0,0
29 07214 040001         STA 0,1
30 07215 060177         NIOS CPU          ;ION
31 07216 060277         NIOC CPU          ;IOF
32 07217 000401         JMP .+1           ;STALL
33 07220 024000         LDA 1,0
34 07221 125004         MOV 1,1,SZR
35 07222 063077         HALT              ;INTR AFTER IOF
36
```

```
;0122 N2LOG
01
02                    ;MSK0=-1 SHD NOT ALLOW TTO INTR
03 07223 102000 INT03:  ADC 0,0
04 07224 062177         DOBS 0,CPU        ;MSK0=-1
05 07225 000401         JMP .+1           ;STALL
06 07226 024000         LDA 1,0           ;AWHILE
07 07227 063477         SKPBN CPU
08 07230 063077         HALT              ;MASK0=1 ALLOWED TTO INTR
09 07231 125004         MOV 1,1,SZR
10 07232 063077         HALT              ;LOC 0 ALTERED
11 07233 102400         SUB 0,0
12 07234 062077         DOR 0,CPU         ;0'S TO MASK 0
13 07235 000401         JMP .+1           ;STALL WAIT FOR INTR
14 07236 024000         LDA 1,0           ;INTR DID NOT OCCUR
15 07237 063577         SKPBZ CPU         ;IF BZ NO SKP
16 07240 063077         HALT
17 07241 125005         MOV 1,1,SNR       ;OR LOC0
18 07242 063077         HALT              ;WAS STILL=0
19                    ;INTERRUPT OVER A SKIP INSTRUCTION
20                    ;SHD STORE THE CORRECT ADDRESS IN LOC 0
21 07243 024007 INT04:  LDA 1,INT4K       ;RET ADRS
22 07244 044001         STA 1,1           ;TO LOC 1
23 07245 060177         NIOS CPU          ;ION
24 07246 125005         MOV 1,1,SNR       ;SET SKIP
25 07247 063077         HALT
26 07250 063077         HALT
27 07251 007250         .-1
28 07252 007253 INT4K:  .+1
29 07253 101001         MOV 0,0,SKP
30 07254 063077         HALT              ;INTR SKIPD
31 07255 020000         LDA 0,0
32 07256 030773         LDA 2,INT4K-1     ;ADRS (LOC 0) SHD=
33 07257 142414         SUB# 2,0,SZR
34 07260 063077         HALT              ;(LOC 0) INCOR
35                    ;INTERRUPT OVER SKIP INST FAILED
36                    ;INTERRUPT AFTER AN I/O SKIP
37                    ;SHD STORE CORRECT RESULT IN LOC 0
38 07261 024007 INT05:  LDA 1,INT5K
39 07262 044001         STA 1,1           ;RET ADRS
40 07263 060177         NIOS CPU          ;ION
41 07264 063477         SKPBN CPU         ;IO SKIP SET SKIP
42 07265 063077         HALT
43 07266 063077         HALT
44 07267 007266         .-1
45 07270 007271 INT5K:  .+1
46 07271 020000         LDA 0,0           ;INTR SKP WILL MISS THIS
47 07272 030775         LDA 2,INT5K-1     ;VALID INTR ADRS
48 07273 142414         SUB# 2,0,SZR
49 07274 063077         HALT              ;INC PC IN LOC 0
50
```

```
@123 N2LOG
@1
@2                  ;INTERRUPT AFTER A JSR SHD STORE
@3                  ;THE CORRECT ADDRESS IN LOC @
@4  07275 030410 INT06:  LDA 2,INT6K
@5  07276 050001         STA 2,1
@6  07277 153240         ADDOR 2,2          ;BIT @ OF AC2=1
@7  07300 060177         NIOS CPU           ;ION JSR GOES .+2
@8  07301 005375         JSR -3,2           ;JSR ADRS CALC BIT @=1
@9  07302 063077         HALT
1@  07303 063077         HALT               ;JSR/INT PREVENTS
11  07304 063077         HALT               ;EITHER HALT
12  07305 007306 INT6K:  .+1
13  07306 165401         INC 3,1,SKP        ;JSR+1 SHD=INTR ADRS
14  07307 063077         HALT
15  07310 020000         LDA @,@            ;GET (LOC @)
16  07311 101112         MOVL# @,@,SZC      ;BIT @ MUST=@
17  07312 063077         HALT               ;BIT @ LOC @=1
18  07313 106414         SUB# @,1,SZR       ;
19  07314 063077         HALT               ;LOC @ OR AC3 INCORRECT
2@                  ;LOC SHD=PC AFTER JSR  (JSR+2)
21                  ;AC3 SHD=PC BEFORE JSR  (JSR+1)
22                  ;NEITHER SHOULD HAVE BIT @=1 -SEE CPB@-
23                  ;NOT JSR OR NOT ZEROBIT FORCES NOT CPB@
24  07315 014121         DSZ PKR@@
25  07316 @@2@@4         JMP @,+4
26  07317 @2@122         LDA @,PKR@1
27  07320 @4@121         STA @,PKR@@
28  07321 101@@1         MOV @,@,SKP
29  07322 @@@5@1         A1A
3@  07323 014112         DSZ TESTK
31  07324 101@@1         MOV @,@,SKP
32  07325 @@@432         JMP PASSC
33
34                  ;FIRST LEVEL INTERRUPT TESTS COMPLETE
35                  ;CLR TTO DONE AND ION
36                  ;REDO NON INT TESTS
37  07326 102620 INT07:  SUBZR @,@
38  07327 @46@@1         STA @,1
39  07330 101120         MOVZL @,@
4@  07331 @4@@@@         STA @,@
41  07332 @6@177         NIOS CPU
42  07333 @62677         IORST
43  07334 @@@4@1         JMP .+1
44  07335 @24@@@         LDA 1,@
45  07336 101@@4         MOV @,@,SZR
46  07337 063077         HALT    ;IORST FAILED TO STOP INTERRUPT
47  07340 @63511         SKPBZ TTO
48  07341 063077         HALT    ;IORST DID NOT MAKE TTY BUSY=@
49  07342 063411         SKPBN TTO
5@  07343 101@@1         MOV @,@,SKP
51  07344 063077         HALT    ;TTO BUSY SHD =@
52  07345 063711         SKPDZ TTO
53  07346 063077         HALT    ;TTO DONE SHD =@ IORST
54  07347 063611         SKPDN TTO
55  07350 101@@1         MOV @,@,SKP
56  07351 063077         HALT
57  07352 063577         SKPBZ CPU
58  07353 063077         HALT
59  07354 @@24@1         JMP @,+1
6@  07355 @@6532         IO,@@
```

```
@124 N2LOG
@1  07356 @@7522         N2ARUN
@2
@3  07357 @24111 PASSC:  LDA 1,K5@
@4  07360 @44112         STA 1,TESTK
@5  07361 @24@65         LDA 1,K1@@@
@6  07362 @44122         STA 1,PKR@1
@7  07363 @44121         STA 1,PKR@@
@8  07364 @2@@46         LDA @,FGGS
@9  07365 101@@4         MOV @,@,SZR        ;AUTO RUN SYS?
1@  07366 @@2770         JMP @PASSC-1       ;YES RETURN
11                  ;6@ PASSES THROUGH INTERRUPT TESTS - PASS COMPLETE
12  07367 @2@113 PASST:  LDA @,K215         ;TRY VARIOUS WAIT LOOPS
13  07370 @61111         DOAS @,TTO         ;OUT CAR RET
14  07371 063411         SKPBN TTO          ;BUSY SHD=1
15  07372 063077         HALT
16  07373 063711         SKPDZ TTO          ;DONE SHD=@
17  07374 063077         HALT
18  07375 063511         SKPBZ TTO          ;WAIT LOOP
19  07376 @@@777         JMP .-1            ;FIRST TIME THIS WAY
2@  07377 063611         SKPDN TTO          ;DONE=1 IF REAL "BZ"
21  07400 063077         HALT
22                  ;NOW OUTPUT LINE FEED
23  07401 @24114         LDA 1,K212
24  07402 @65111         DOAS 1,TTO
25  07403 063711         SKPDZ TTO
26  07404 063077         HALT
27  07405 063411         SKPBN TTO
28  07406 063077         HALT
29  07407 063611         SKPDN TTO          ;FIRST SKPDN
3@  07410 @@@777         JMP .-1            ;WAIT LOOP
31  07411 063511         SKPBZ TTO          ;BUSY=@ IF REAL DONE
32  07412 063077         HALT
33  07413 126620         SUBZR 1,1
34  07414 @44@@1         STA 1,1
35                  ;TTO DONE=1 DO RESET WITHOUT "C" FOR CLR ION
36  07415 @6@177         NIOS CPU
37  07416 @62477         DIC @,CPU          ;IORST LESS "C" FOR ION
38  07417 @@@4@1         JMP .+1
39  07420 063477         SKPBN CPU          ;INTERRUPT?
4@  07421 063077         HALT               ;ION SHD STILL=1
41  07422 063711         SKPDZ TTO
42  07423 063077         HALT               ;TTO DONE SHD=@
43                  ;OUTPUT P
44  07424 @3@117         LDA 2,K32@
45  07425 @71111         DOAS 2,TTO
46  07426 063577         SKPBZ CPU          ;ION STILL=1
47  07427 @@@777         JMP .-1            ;WHEN IT=@ TTO DONE
48  07430 063611         SKPDN TTO          ;TTO DONE=@
49  07431 063077         HALT               ;BZ BEFORE INTR
5@  07432 @75477         INTA 3
51  07433 @24116         LDA 1,KTTO
52  07434 136414         SUB# 1,3,SZR       ;SKP DEV# OK
53  07435 063077         HALT               ;NOT "TTO" ON INTA
54
```

```
@125 N2LOG
01
02                      ;OUTPUT "A"
03 07436 034077         LDA 3,K300
04 07437 175400         INC 3,3
05 07440 060177         NIOS CPU
06 07441 075111         DOAS 3,TTO
07 07442 000401         JMP .+1
08 07443 063477         SKPBN CPU       ;ION SHD STILL=1
09 07444 063077         HALT
10 07445 020105 PASL1:  LDA 0,KCBO
11 07446 126000         ADC 1,1         ;DO XOR'S
12 07447 131000         MOV 1,2         ;WHILE WAITING
13 07450 113520         ANDZL 0,2       ;ODD BITS XOR'D TO
14 07451 107000         ADD 0,1         ;-1=EVEN BITS
15 07452 146400         SUB 2,1         ;XOR'D TO -1
16 07453 152000         ADC 2,2         ;AGAIN SHOULD=
17 07454 155000         MOV 2,3         ;THE ODD BITS
18 07455 113520         ANDZL 1,3
19 07456 133000         ADD 1,2
20 07457 172400         SUB 3,2
21 07460 142414         SUB# 2,0,SZR
22 07461 063077         HALT            ;PROCESSOR ARITH ERR
23 07462 063577         SKPHZ CPU       ;INTR OCCUR YET
24 07463 000762         JMP PASL1       ;NO
25 07464 063611         SKPDN TTO       ;TTO YES DONE=1
26 07465 063077         HALT            ;NO ERROR AT "BZ"
27                      ;INTERRUPT SHOULD OCCUR DURING A
28                      ;STRING OF IO INSTRUCTIONS OUTPUT FIRST S
29 07466 034115         LDA 2,K323
30 07467 102400         SUB 0,0
31 07470 040000         STA 0,0
32 07471 061000         DOA 0,0
33 07472 071111         DOAS 2,TTO      ;OUTPUT FIRST S
34 07473 060177 PASL2:  NIOS CPU
35 07474 060200         NIOC 0
36 07475 063577         SKPHZ CPU
37 07476 063477         SKPBN CPU
38 07477 060000         NIO 0
39 07500 065477         INTA 1
40 07501 060300         NIOP 0
41 07502 074477         DIA 3,CPU
42 07503 060400         DIA 0,0
43 07504 060100         NIOS 0
44 07505 061000         DOA 0,0
45 07506 060277         NIOC CPU
46 07507 034000         LDA 3,0
47 07510 175005         MOV 3,3,SNR
48 07511 000762         JMP PASL2
49 07512 034115         LDA 1,K323
50 07513 132414         SUB# 1,2,SZR
51 07514 063077         HALT
52 07515 101004         MOV 0,0,SZR
53 07516 063077         HALT
54 07517 071111         DOAS 2,TTO
55 07520 002401         JMP @.+1
56 07521 000501         A1A
57
```

```
@126 N2LOG
01 07522 014051 N2ARUN: DSZ EGGS+3
02 07523 002776         JMP @N2ARUN-1
03 07524 034052         LDA 3,EGGS+4
04 07525 020051         LDA 0,EGGS+3
05 07526 041776         STA 0,-2,3
06 07527 001400         JMP 0,3
07
```

```
12127 N2LOG
01
02
03 07530 047503          .TXT    /COPYRIGHT (C) DGC,1973,74,76
04       054520
05       044522
06       044107
07       020124
08       041450
09       020051
10       043504
11       020103
12       034461
13       031467
14       033454
15       026064
16       033067
17 07546 046101 ALL RIGHTS RESERVED/
18       020114
19       044522
20       044107
21       051524
22       051040
23       051505
24       051105
25       042526
26       000104
27
28 07560 131116 DIRT:   .TXTE   1N2LGCTST 31
29       043714
30       152303
31       152123
32       031640
33       000000
34 07566 000000          0
35 07567 000200          OTOSR
36 07570 157771          157771
37 07571 000000          0
38 07572 000000          0
39 07573 000000          0
40 07574 000000          0
41 07575 000000          0
42
43                       .END
```

```
0128 N2LOG

A1A   000501     4/02    5/25  115/32  119/01  120/18  123/29  125/56
A1P   000504     5/32
A1C   000507     5/38
A1D   000512     5/44
A1E   000515     5/50
A1F   000524     5/56
A1G   000523     6/02
A20   001025    14/06
A21   001027    14/12
A22   001032    14/18
A23   001035    14/27
A24   001044    14/33
A25   001043    14/40
A2A   000526     6/09
A2B   000531     6/15
A2C   000534     6/21
A2D   000537     6/27
A2E   000542     6/33
A2F   000545     6/39
A2G   000550     6/45
A3A   000553     6/52
A3B   000556     6/58
A3C   000561     7/04
A3D   000564     7/10
A3F   000567     7/16
A3F   000572     7/22
A3G   000575     7/28
A40   001222    19/17
A41   001226    19/24
A42   001232    20/04
A43   001236    20/09
A44   001241    20/17
A45   001245    20/27
A46   001247    20/31
A47   001252    20/36
A48   001256    21/04
A49   001262    21/11
A4A   000604     7/35
A4B   000603     7/41
A4C   000605     7/47
A4D   000611     7/53
A4F   000614     7/59
A4F   000617     8/05
A4G   000622     8/11
A50   001266    21/21
A51   001273    21/28
A5A   000625     8/18
A5B   000634     8/24
A5C   000633     8/30
A5D   000636     8/36
A5E   000641     8/42
A5F   000644     8/48
A5G   000647     8/54
A6A   000652     9/01
A6B   000655     9/07
A6C   000664     9/13
A6D   000663     9/19
A6E   000666     9/25
A6F   000671     9/31
```

A6G	000674		9/37						
A7A	000677		9/44						
A7B	000702		9/50						
A7C	000705		9/56						
A7D	000710		10/02						
A7E	000713		10/08						
A7F	000716		10/14						
A7G	000721		10/20						
A8A	000724		10/27						
A8B	000727		10/33						
A8C	000732		10/39						
A8D	000735		10/45						
A8E	000740		10/51						
A8F	000743		10/57						
A8G	000746		11/03						
A9A	000751		12/05						
A9B	000756		12/12						
A9C	000765		12/23						
A9D	000770		12/29						
A9E	000776		12/39						
A9F	001001		13/04						
A9G	001005		13/11						
A9H	001011		13/17						
A9I	001015		13/24						
A9J	001021		13/29						
AC15	003013		50/45						
ACIT2	000056	MC	17/06	17/13	17/19	17/25	17/31	17/37	17/43
			17/49	17/55	18/01	18/07	18/13	18/19	
ACITS	000035	MC	15/04	15/13	15/20	15/27	15/34	15/41	15/48
			15/55	16/02	16/09	16/16	16/23	16/30	
ADDT0	000327	MC	47/05	47/24	47/37	47/50	48/03	48/17	48/30
			48/43	48/56	49/10	49/23	49/36	49/49	50/03
			50/16	50/29					
ADDT1	000243	MC	37/05	38/02	38/17	38/32	38/47	39/02	39/17
			39/32	39/47	40/02	40/17	40/32	40/47	41/02
			41/17	41/32	41/47	42/08	42/23	42/38	42/53
			43/08	43/23	43/38	43/53	44/08	44/23	44/38
			44/53	45/08	45/23	45/38	45/53		
AEQB7	006513		111/54						
ANC00	002163		37/22						
AND00	003020		51/05						
AND01	003025		51/16						
AND02	003033		51/26						
AND03	003041		51/35						
AND20	003432		61/05						
AND21	003435		61/10						
AND22	003440		61/16						
AND23	003444		61/21						
AND24	003450		61/28						
AND25	003453		61/32						
AND26	003456		61/36						
AND27	003462		61/41						
ANDTS	000410	MC	52/03	53/02	53/29	53/56	54/23	54/50	55/17
			55/44	56/11	56/38	57/05	57/32	57/59	58/26
			58/53	59/20	59/47				
ASL15	001543		27/41						
ASL31	002156		36/33						
ASR15	001417		24/52						

ASR31	001752		32/33					
DIRT	007560		3/05	127/26				
DSZ00	005501		97/19					
DSZ01	005527		98/04					
DSZ02	006154		106/19					
DSZ03	006171		106/34					
DTOSH	000200		4/01	127/35				
EGGS	002040		3/08	3/09	124/08	126/01	126/03	126/04
ID00K	006260		108/25	108/26	108/27	108/28	108/29	108/30	108/34
ID01K	006273		108/39	108/40	108/41	108/42	108/43	108/44	108/48
ID02K	006306		108/53	108/54	108/55	108/56	108/57	108/58	109/02
ID03K	006321		109/07	109/08	109/09	109/10	109/11	109/12	109/16
ID04K	006334		109/21	109/22	109/23	109/24	109/25	109/26	109/30
ID05K	006347		109/35	109/36	109/37	109/38	109/39	109/40	109/44
ID06K	006362		109/49	109/50	109/51	109/52	109/53	109/54	109/58
ID07K	006375		110/03	110/04	110/05	110/06	110/07	110/08	110/12
ID08K	006414		110/17	110/18	110/19	110/20	110/21	110/22	110/26
ID09K	006423		110/31	110/32	110/33	110/34	110/35	110/36	110/40
ID10K	006436		110/45	110/46	110/47	110/48	110/49	110/50	110/54
ID11K	006451		110/59	110/60	111/01	111/02	111/03	111/04	111/08
ID12K	006464		111/13	111/14	111/15	111/16	111/17	111/18	111/22
ID13K	006477		111/27	111/28	111/29	111/30	111/31	111/32	111/36
ID14K	006512		111/41	111/42	111/43	111/44	111/45	111/46	111/50
INC00	003466		62/03						
INC01	003476		62/16						
INC02	003506		62/28						
INC20	003721		67/03						
INC21	003726		67/11						
INCTS	000534	MC	63/04	63/24	63/37	63/50	64/03	64/16	64/29
			64/42	64/55	65/08	65/21	65/34	65/47	65/60
			66/13	66/26	66/39				
INT00	007143		115/31	120/22					
INT01	007166		121/03						
INT03	007223		122/03						
INT04	007243		122/21						
INT05	007261		122/38						
INT06	007275		123/04						
INT07	007326		123/37						
INT0K	007161		120/22	120/36	120/38				
INT1K	007207		121/08	121/20					
INT4K	007252		122/21	122/28	122/32				
INT5K	007270		122/38	122/45	122/47				
INT6K	007305		123/04	123/12					
IOTS1	001220	MC	112/41	112/57	113/11	113/25	113/39	113/53	114/07
			114/21	114/35					
IOTS2	001257	MC	116/37	116/46	116/54	117/02	117/10	117/18	117/26
IOX00	006715		115/19	115/30	115/38				
IOX21	006733		115/21	115/28	115/33				
IO.00	006532		112/15	123/60					
IO.01	006535		112/19						
IO.02	006540		112/24						
IO.03	006542		112/27						
IO.04	006544		112/30						
IO.13	006706		115/06						
ISDST	001164	MC	108/05	108/21	108/35	108/49	109/03	109/17	109/31
			109/45	109/59	110/13	110/27	110/41	110/55	111/09
			111/23	111/37					
ISZ00	005464		97/03						

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ISZ01  000512      97/32
ISZ02  000117     105/43
ISZ03  000137     106/03
JM3K   000047     104/12   104/16   104/23
JMP00  000541      98/17    98/19
JMP01  000551      98/26    98/28
JMP02  000017     103/57   103/59
JMP03  000034     104/12
JMP2L  000026     104/01   104/04
JMP3K  000120       3/52   120/23   121/06
JS02K  000112     105/21   105/35
JSR00  000563      99/05    99/07
JSR01  000575      99/16    99/18
JSR02  000074     105/19
K0     000110       3/44   104/20
K1     000054       3/16    83/05    83/30    83/36    83/42    83/48    83/54
                   83/60    84/06    84/12    84/18    84/24    84/30    84/36
                   85/19    88/46    91/03
K10    000057       3/19    85/40    89/37    91/54   108/52
K100   000062       3/22    86/01    90/28    92/45   100/35   109/34
K1000  000065       3/25    86/22    89/04    91/19   110/16   124/05
K100K  000073       3/31    87/04    90/46    93/01   111/40
K10K   000070       3/28    86/43    89/55    92/10   110/58
K2     000055       3/17    85/26    89/03    91/20   108/24   120/24   121/03
K20    000060       3/20    85/47    89/54    92/11   101/07   103/25   105/06
                  109/06
K200   000063       3/23    86/08    90/45    93/02   100/06   100/14   100/22
                  100/34   100/47   101/20   102/26   109/48
K2000  000066       3/26    86/29    89/21    91/36   110/30
K20K   000071       3/29    86/50    90/12    92/27   111/12
K212   000114       3/48   124/23
K215   000113       3/47   124/12
K300   000077       3/35   100/46   102/06   103/08   103/37   104/30   105/07
                  105/24   111/55   125/03
K320   000117       3/51   124/44
K323   000115       3/49   125/29   125/49
K4     000056       3/18    85/33    89/20    91/37   108/38
K40    000061       3/21    85/54    90/11    92/28   109/20
K400   000064       3/24    86/15    88/47    91/02   101/08   110/02
K4000  000067       3/27    86/36    89/38    91/53   110/44
K40K   000072       3/30    86/57    90/29    92/44   111/26
K420   000106       3/42   111/54
K5     000075       3/33    99/11
K60    000111       3/45   124/03
K7     000076       3/34    99/24
KCBE   000104       3/40   107/09
KCRO   000105       3/41   107/22   125/10
KD17   000100       3/36   103/26
KD21   000102       3/38   103/35
KD37   000103       3/39   103/48
KJRET  000107       3/43   105/28
KLDA.  000074       3/32    96/08
KM8    000101       3/37   103/28
KTTO   000116       3/50   124/51
LDA00  004644      83/03
LDA29  005417      96/06
LDA30  005424      96/14
LDA31  005432      96/22
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LDA32  005447      96/29
LDA33  005452      96/41
LDA34  005611      99/31
LDA35  005622      99/43
LDA36  006052     104/30
LDA37  006064     105/06
LDA38  006244     107/35
LDAT1  001010  MC   83/19    83/27    83/33    83/39    83/45    83/51    83/57
                   84/03    84/09    84/15    84/21    84/27    84/33
LDAT2  001026  MC   85/05    85/17    85/24    85/31    85/38    85/45    85/52
                   85/59    86/06    86/13    86/20    86/27    86/34    86/41
                   86/48    86/55    87/02
N2ARU  007522     124/01   126/01   126/02
NEG00  003733      68/05
NEG01  003740      68/14
NEG19  004250      75/03
NEG20  004262      75/18
NEG21  004266      75/25
NEGTS  000006  MC   68/23    69/09    69/30    69/51    70/12    70/33    70/54
                   71/15    71/36    71/57    72/18    72/39    72/60    73/21
                   73/42    74/03    74/24
NG19A  004256      75/10
NIN00  006741     115/42
NIN01  006750     115/51
NIN02  006754     115/55
NIN03  006760     116/04
NIN04  006764     116/10
NIN05  006770     116/15
NIN06  006774     116/20
NIN07  007000     116/25
NIN08  007004     116/30
NIN15  007047     118/04
NIN16  007053     118/10
NIN17  007060     118/17
NIN18  007065     118/24
NIN19  007073     118/31
NIN20  007100     118/37
NIN21  007105     118/45
NIN22  007111     118/50
NLD1   005351      94/12
NLD2   005360      94/20
NLD3   005367      94/28
NLD4   005376      94/36
NOLOD  001131  MC   94/02    94/11    94/19    94/27    94/35
PASL1  007445     125/10   125/24
PASL2  007473     125/34   125/48
PASSC  007357     120/20   123/32   124/03   124/10
PASST  007367     124/12
PKR00  000121       3/53   118/56   118/59   123/24   123/27   124/07
PKR01  000122       3/54   118/58   123/26   124/06
SHIFT  000075  MC   22/04    22/21    22/31    22/41    22/51    23/01    23/11
                   23/21    23/31    23/41    23/51    24/01    24/11    24/21
                   24/31    24/41    25/10    25/20    25/30    25/40    25/50
                   25/60    26/10    26/20    26/30    26/40    26/50    26/60
                   27/10    27/20    27/30
SHIFZ  000150  MC   28/03    29/02    29/16    29/30    29/44    29/58    30/12
                   30/26    30/40    30/54    31/08    31/22    31/36    31/50
                   32/04    32/18    33/02    33/16    33/30    33/44    33/58
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0133 N2LOG

		34/12	34/26	34/40	34/54	35/08	35/22	35/36
		35/50	36/04	36/18				
STA00	005405	95/06						
STA01	005412	95/12						
STA02	005633	100/06						
STA03	005640	100/14						
STA04	005646	100/22						
STA05	005654	100/34						
STA06	005664	100/46						
STA07	005673	101/07						
STA08	005703	101/20						
STA09	005717	102/06						
STA10	005734	102/26						
STA11	005751	103/05						
STA12	005765	103/25	103/32	103/36				
STA13	006210	107/05						
STA14	006225	107/20						
STES1	000004	MC 5/06	5/24	5/30	5/36	5/42	5/48	5/54
		5/60	6/07	6/13	6/19	6/25	6/31	6/37
		6/43	6/50	6/56	7/02	7/08	7/14	7/20
		7/26	7/33	7/39	7/45	7/51	7/57	8/03
		8/09	8/16	8/22	8/28	8/34	8/40	8/46
		8/52	8/59	9/05	9/11	9/17	9/23	9/29
		9/35	9/42	9/48	9/54	9/60	10/06	10/12
		10/18	10/25	10/31	10/37	10/43	10/49	10/55
		11/01						
STES2	000021	MC 5/13	5/23	6/06	6/49	7/32	8/15	8/58
		9/41	10/24					
SUB00	004272	76/05						
SUB01	004275	76/09						
SUBTS	000721	MC 76/17	77/02	77/21	77/40	77/59	78/18	78/37
		78/56	79/15	79/34	79/53	80/12	80/31	80/50
		81/09	81/28	81/47				
SWP00	005055	88/06						
SWP01	005060	88/09						
SWP02	005063	88/12						
SWP03	005066	88/15						
SWPTS	001045	MC 88/21	88/42	88/59	89/16	89/33	89/50	90/07
		90/24	90/41	90/58	91/15	91/32	91/49	92/06
		92/23	92/40	92/57				
TESTK	000112	3/46	123/30	124/04				
TT000	007125	120/06						