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TYPE 5602X WRAIS

DIGITAL I/O SYSTEM

WIDE RANGE ANALOG INPUT SYSTEM

BASIC INTERFACE

PROPRIETARY INFORMATION

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I. INTRODUCTION

The 5602 WRAIS (Basic) Interface is designed to provide an interface capability with the Computer Products RTP 7480 series Wide Area Analog Input System (WRAIS) compatible with the 5602 Digital I/O System (DIOS). The 5602 WRAIS Interface provides a bus repeater for the I/O bus data and selective control lines for control of the WRAIS on a single 7"x9" PC card which occupies one slot in a standard DIOS chassis.

II. PROGRAMMING

Data and control transfer to the 5602 WRAIS Interface from the Nova CPU is via the standard procedure established for the DIOS (programmed I/O, program interrupt). There are two steps to programming the 5602 WRAIS interface. The first step consists of establishing the device sub-address (ASR=one of 256 DIOS addresses). The second step accomplishes the desired control/data transfer.

1. Device sub-address

The device sub-address is selected by issuing a DOA AC, DIOS instruction. The 8 lsbs of the data transfer specifies one of 256 possible sub-addresses (0 not used, 377_8 and 376_8 reserved). The WRAIS interface requires one of the 256 possible sub-addresses with the restriction that bits 10 to 13 of the DOA word must be zeroes.

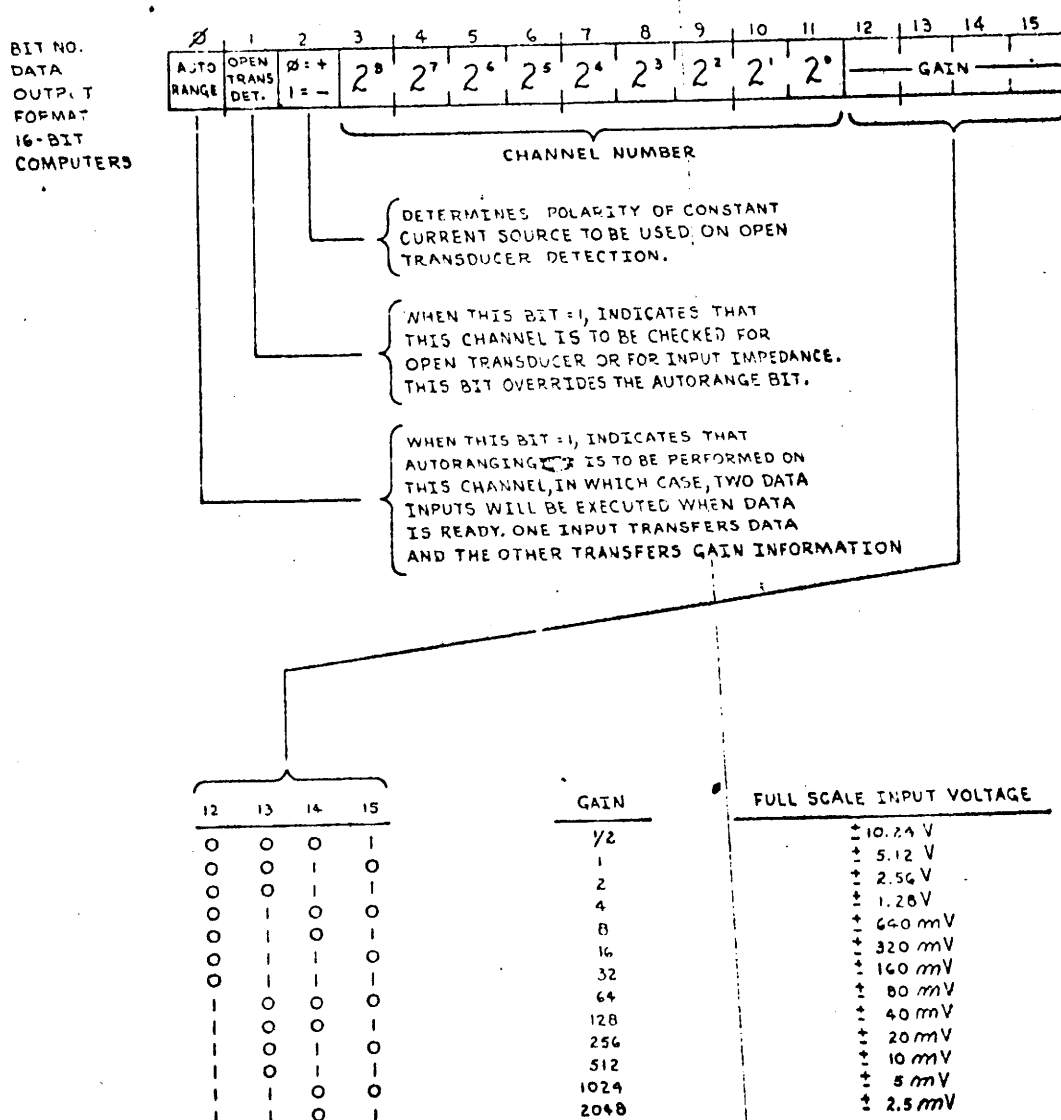
2. Busy/Done/Interrupt Testing

Testing of the Busy/Done/Interrupt logic allows the program to test when data is available on inputs. To test the Busy/Done status of the 5602 WRAIS interface it is first addressed with a DOA AC, DIOS. The status of the device may then be inputted with a DIA AC, DIOS instruction. Bit 0 corresponds to the device Busy Flag and Bit 1

corresponds to the device Done Flag. These bits can be tested to determine when to make a data transfer.

3. Initiating a Conversion in the WRAIS

Generation of a Data Output Word to the WRAIS is accomplished by issuing a DOB AC, DIOS (the device sub-address of the WRAIS interface being previously established via a DOA AC, DIOS). The format for the Data Output Word is as follows (ref. Computer Products PM070-027)



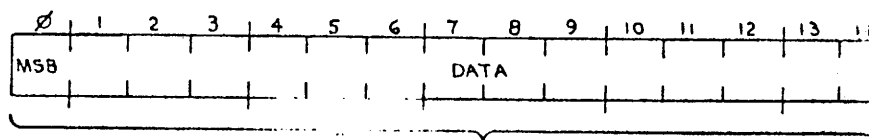
Data Output Format

The generation of the Data Output initiates a conversion of the selected channel input and gain setting of the WRAIS.

4. Initiating a Data Input from the WRAIS

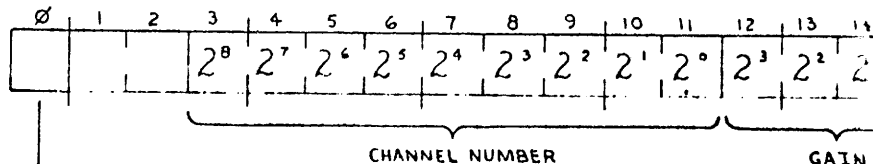
Once conversion is completed within the WRAIS, data is available for transfer to the Nova. The data available is contained in 16 bit words which may be inputted by issuing a DIB AC, DIOS (device sub-address being previously established). The format of the data words is as follows (ref. Computer Products PM070-027).

BIT NO.
FIRST
DATA
INPUT
WORD
FORMAT



DATA, TWO'S COMPLEMENT SIGN EXTENDED, RIGHT JUSTIFIED

BIT NO.
SECOND
DATA
INPUT
WORD
FORMAT



0 = AUTORANGE OFF
1 = AUTORANGE ON

NOTE: THE FIRST DATA INPUT EXECUTED AFTER THE EXECUTION OF A DATA OUTPUT TRANSFERS THE DIGITIZED DATA VALUE TO THE COMPUTER. IF A SECOND DATA INPUT IS EXECUTED PRIOR TO THE NEXT DATA OUTPUT, THE SECOND DATA INPUT TRANSFERS THE GAIN AND CHANNEL NUMBER INFORMATION TO THE COMPUTER. THE TWO WORD TRANSFERS ARE USED WHEN AUTORANGING, HOWEVER, THE SECOND WORD TRANSFER NEED NOT BE EXECUTED IF NOT DESIRED.

THE FORMAT FOR THE SECOND DATA INPUT WORD IS THE SAME AS FOR THE DATA OUTPUT WORD WHEN AUTORANGING; THEREFORE, THE GAIN NEED NOT BE MERGED WITH THE CHANNEL NUMBER AND STORED BACK IN MEMORY. INSTEAD, THE COMPLETE SECOND DATA INPUT WORD CAN SIMPLY BE STORED IN PLACE OF THE PREVIOUS CHANNEL NUMBER AND GAIN WITH NO MERGING REQUIRED.

Data Input Format

5. Initiating Conversion via Program Interrupt

An interrupt request from the 5602 WRAIS interface within the DIOS is similar to one from other standard Nova peripherals. Data 5 is connected as the mask bit for DIOS. Interrupts from the DIOS may be enabled or disabled via MSKO AC. If interrupts are to be used from the DIOS, its INTPIN and INTPOUT must be connected to the interrupt priority chain in the normal manner. The INTA instruction returns the DIOS address.

The interrupt service routine for the DIOS can further identify the interrupting sub-device by issuing DIC AC, DIOS which returns the address of the highest priority device requesting an interrupt. This instruction also loads this address into the address select register (ASR).

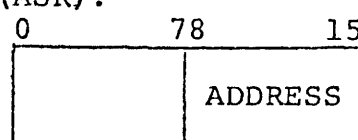
The device priority interrupt structure is also programmable within the DIOS. Device 377₈ and DOB AC, DIOS is analogous to MSKO in the implementation of sixteen levels of programmable priority interrupts among DIOS devices. The interrupt priority chain in the DIOS is analogous to the priority chain among CPU devices. Data 9 is fixed as the sub-mask bit for the WRAIS Interface.

Initiating an interrupt from the 5602 WRAIS interface, with BUSY/DONE/INTERRUPT logic may be done by issuing a start pulse to the sub-device via NIOS DIOS or DOBS AC, DIOS (the ASR being previously established for the WRAIS interface with a DOA AC, DIOS). The start pulse clears DONE/INTERRUPT and sets BUSY in the device. If an Output Data Word is issued to the WRAIS, initiating a conversion, the WRAIS will return a control line (TESTR) which indicates that the conversion is complete and data is available. If BUSY is set the TESTR control line will set DONE and reset BUSY (additional TESTR pulses

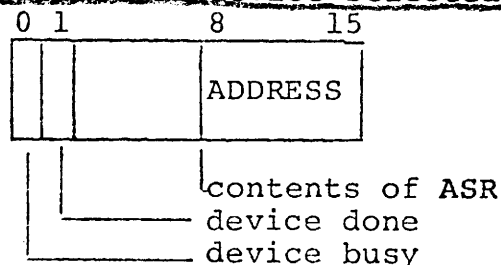
do not affect the status of BUSY/DONE). If the device interrupt disable is reset, the device interrupt flop is set at the end of the next instruction. The device interrupt flop generates an interrupt request to the DIOS CPU interface control card and, if the DIOS interrupt disable flag is reset, generates an interrupt request to the CPU.

6. Instruction Summary

DOA AC, DIOS: Load the contents of AC bits 8-15 into the address select register (ASR).



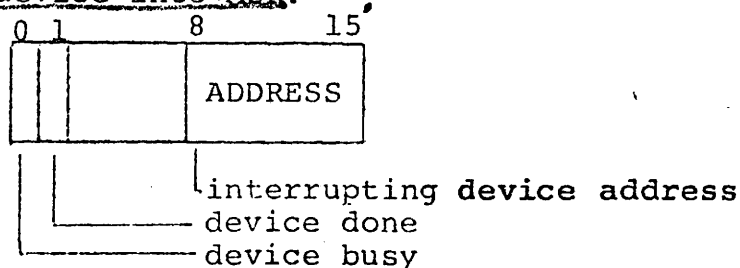
DIA AC, DIOS: Read Status of device selected by ASR



DIB AC, DIOS: Read Data Input from WRAIS (ref previous figure).

The first DIB AC, DIOS retrieves data while the second gets channel and gain setting.

DIC AC, DIOS: Read status of interrupting device; also load
address of interrupting device into ASR.



DOB AC, DIOS: Initiate conversion in WRAIS, transfer channel number and gain information in AC to WRAIS (ref. previous figure Data

Output format) (if dev=377₈ bits 0-15 is sixteen level priority interrupt mask).

START PULSE, DIOS: Sets BUSY/resets DONE/INTERRUPT in selected device.

CLEAR PULSE, DIOS: Clears BUSY/DONE/INTERRUPT in selected device.

Note that a general purpose interrupt routine may issue DIA AC, DIOS first to save ASR before issuing DIC AC, DIOS. It can be restored after servicing the interrupting device with the DOA AC, DIOS.

III. HARDWARE DESCRIPTION

The 5602 WRAIS Interface (basic) is contained on a single 7"x9" printed circuit card which plugs into a standard DIOS chassis. The 5602 WRAIS Interface has an etched PC connector on each end. One end connects to the DIOS Interface Bus on the backpanel. Connection from the WRAIS Interface to the WRAIS is made at the other end of the card (via cable which connects from P2 50 pin etched PC connector on the WRAIS Interface to slot 1 of the WRAIS).

The 5602 WRAIS Interface provides the capability of interfacing the WRAIS with the DIOS. The device selection of the WRAIS is set up for device 31₈ on the RTP interface card in the WRAIS (as selected by SW1 to SW6 of card in slot 4A).

Circuitry and logic provided on the card consists of

- (1) I/O Bus repeater for DATA₀ - DATA 15 (bidirectional)
- (2) Control lines (IORST, WAIS INPUT, WAIS OUTPUT) to WRAIS
- (3) Selection for WAIS device 31₈
- (4) Input circuitry to receive end of conversion (TESTR) from WRAIS
- (5) Standard BUSY/DONE/INTERRUPT logic
- (6) Card address selection logic (AS2 to AS5 must be 0's).

IV. 5602 WRAIS INSTALLATION WIRING INSTRUCTIONS

*DIOS interrupt priority chain with highest=closest to chassis control card

SIGNAL	CHASSIS BACKPLANE PIN
<u>ZINTPIN</u>	25
<u>ZINTPOUT</u>	26

*Sub-device address selection - allocation of 1 of 256 addresses is via GND connection to address jumper (GND corresponds to a bit=1 for this device)

SIGNAL	CHASSIS BACKPLANE PIN
AJ0	86
AJ1	85
AJ6	92
AJ7	91

(AJ2,AJ3,AJ4,AJ5 do not apply)

*Connect cable from WRAIS interface P2 (50 pin connector) to WRAIS slot 1.

5602 WRAIS Interface - P2 Pin Allocation

SIGNAL	PIN	(RTP I/O SLOT 1)
GROUND	A thru Y	101,128,201,228
TESTR	20	109
<u>WAIS DVS32</u>	23	110
<u>WAIS DVS16</u>	V	111
<u>WAIS DVS8</u>	W	112
<u>WAIS DVS4</u>	X	113
<u>WAIS DVS2</u>	Y	114
<u>WAIS DVS1</u>	A	115
<u>WAIS IORST</u>	19	116
<u>WAIS OUTPUT DATA</u>	24	117
<u>WAIS COM OUT</u>	22	118
<u>WAIS INPUT DATA</u>	18	119

<u>DA0</u>	2	207
<u>DA1</u>	3	208
<u>DA2</u>	4	209
<u>DA3</u>	5	210
<u>DA4</u>	6	211
<u>DA5</u>	7	212
<u>DA6</u>	8	213
<u>DA7</u>	9	214
<u>DA8</u>	10	215
<u>DA9</u>	11	216
<u>DA10</u>	12	217
<u>DA11</u>	13	218
<u>DA12</u>	14	219
<u>DA13</u>	15	220
<u>DA14</u>	16	221
<u>DA15</u>	17	222

Cable Length 5'

REFERENCES

Schematic: 001-000482 DIG I/O WRAIS Interface

Diagnostic: WRAIS Interface Test
095-000150 Binary Tape
096-000119 Program Listing

WRAIS System Test
095-000151 Binary Tape
096-000120 Program Listing