WANG

8101

PROFESSIONAL COMPUTER

Customer Engineering
Product Maintenance Manual

729-1190-B

PREFACE

This document is the Standard Maintenance (STD) Manual for the Professional Computer. It is organized in accordance with the approved STD outline established at the Field/Home Office Publications meetings conducted on September 14th and 15th, 1982. The scope of this manual reflects the type of maintenance philosophy selected for this product (swap unit, printed circuit assembly, chip level or any combination thereof).

The purpose of this manual is to provide the Wang-trained Customer Engineer (CE) with instructions to operate, troubleshoot and repair the Professional Computer. It will be updated on a regular schedule.

Second Edition (Sept 1983)

This edition of the Professional Computer STD manual obsoletes document(s) no. 729-1190-A and 729-1190-A1. The material in this document may only be used for the purpose stated in the Preface. Updates and/or changes to this document will be published as Product Service Notices (PSN's) or subsequent editions.

WARNING

****
*
* DO NOT OPEN THE SWITCHING POWER SUPPLY UNDER ANY
* CIRCUMSTANCE. EXTREMELY DANGEROUS VOLTAGE AND
* CURRENT LEVELS (IN EXCESS OF 300 VOLTS DC AND UN-
* LIMITED CURRENT) ARE PRESENT WITHIN THE POWER SUPPLY.
*
* DO NOT ATTEMPT TO REPAIR THE SWITCHING POWER
* SUPPLY; IT IS FIELD REPLACEABLE ONLY.
*
* AFTER POWERING THE UNIT DOWN AND DISCONNECTING THE AC
* POWER PLUG FROM THE WALL OUTLET, ALLOW ONE MINUTE
* BEFORE REMOVING THE POWER SUPPLY TO PROVIDE ADEQUATE
* TIME FOR ANY RESIDUAL VOLTAGE TO DRAIN THROUGH THE
* BLEEDER RESISTORS.
*
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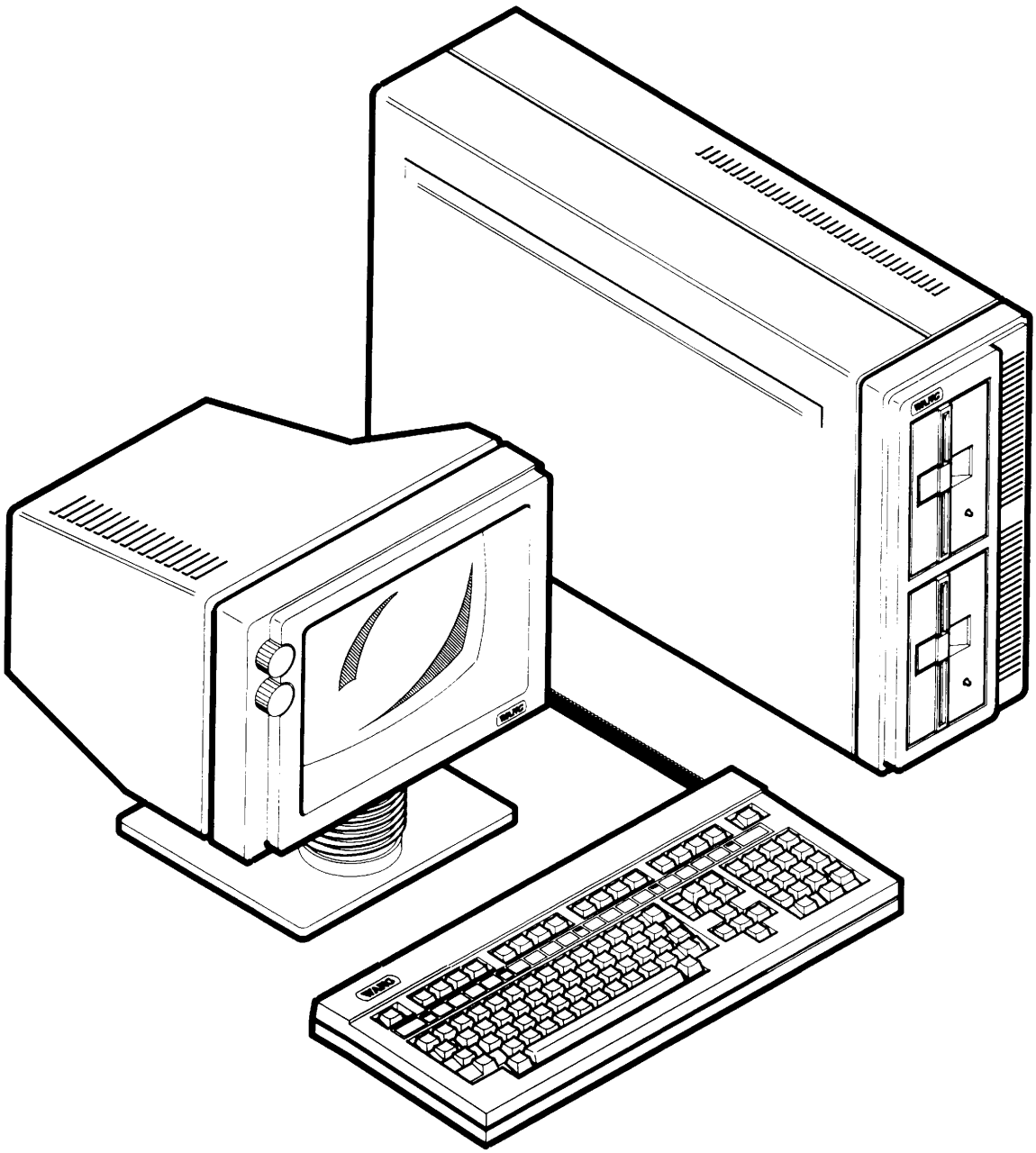


Wang Professional Computer

CHAPTER 1

INTRODUCTION

1.1 SCOPE

The Wang Professional Computer maintenance documentation is contained in a set of two (2) manuals; the PC Product Maintenance Manual (729-1190-B) and the PC Schematic Manual (729-1241).

The Product Maintenance Manual provides installation, theory of operation, installation and check-out procedures, corrective and preventive maintenance, removal and replacement procedures, and troubleshooting information for the Wang Professional Computer (PC) and its options. An IPB (illustrated parts breakdown) is provided to aid in locating and identifying all the PC's major components. An appendix is also included which contains a listing of cable assemblies, error messages, mnemonic codes, and System board Input/Output (I/O) address assignments.

The PC Schematic manual provides engineering schematics for the Professional Computer and its option boards.

The level of coverage in the Product Maintenance documentation is directed toward an Associate Field Engineering Technician (AFET) with a minimum of six months field experience who has received qualified PC training either directly from a Wang course instructor or indirectly via Wang video tape.

Included in this chapter are listings of applicable documentation (Software, User, and CE) related to the PC and its options. Also included is an overview of the standard PC equipment supplied and options available to further enhance and customize the PC to meet individual requirements.

A chart is included that contains five prepackaged configurations of the PC that can be ordered which include both standard and optional features.

A listing of the PC specifications is contained in paragraph 1.5. These specifications contain dimensions, net weight, power requirements, and environment conditions for the PC.

1.2 APPLICABLE DOCUMENTATION

Table 1-1, 1-2, and 1-3 lists software, user documentation, and CE product maintenance documentation available for the PC respectively. Software and documentation can be ordered by writing to the address directly following the table.

Table 1-1. PC Software

Model Number	CEI Number	Description
PC-SS001	195-2326-9	MS-DOS Operating System plus interpretive Basic
PC-SS010	195-2327-9	MS Basic Compiler
PC-SS011	195-2328-9	MS Pascal
PC-SS012	195-2329-9	MS FORTRAN
PC-SS013	195-2330-9	MS COBOL
PC-SS020	195-2331-9	Async Communications (includes 2236DW Emulation)
PC-SS021	195-2332-9	Remote Wangnet for VS (Leased line only)
PC-SS030	195-2333-9	Local Communications for VS (2246S only)
PC-SS031	195-2334-9	Local Communications for VS (2256C)
PC-SS032	195-2335-9	Local Communications for OIS (5536-4)
PC-SS033	195-2336-9	Local Communications/Alliance (5536-4)
PC-SS060	195-2337-9	2780/3780/WPS Support For PC
PC-SS063		3276 SNA/SDLC Software
PC-AS001	195-2338-9	PC Multiplan
PC-AS002	195-2339-9	PC Word Processing
PC-AS003		PC Business Graphics
PC-AS004		PC Data Base
PC-CS001		Software Productivity Package (Includes PC-AS001, PC-AS002, and PC-SS020)
	195-2459-9	PC Diagnostics

NOTE

ADDITIONAL SOFTWARE UPDATES WILL INCUR A NOMINAL CHARGE.

All software can be ordered by writing to the following address:

WANG LABORATORIES INC.
Software/Literature Control Centers
Building 4-1 M/S 2428
836 North Street
Tewksbury, MA 01876

Table 1-2. Wang User Documentation

Document Number	Title	Information Contained
700-7589	Documentation Guide	Directory of all user documentation.
700-7590	Introductory Guide	Basic introduction to the PC.
700-7592	BASIC Language Guide	BASIC programming for the PC.
700-7593	Program Development Guide	Programmer's guide to technical features of the PC.
700-7558	Communications Guide	A three part manual consisting of: How to use the teletypewriter emulation feature, operation of the Wang 2236DW Terminal emulation feature, and Programmer Support subroutines.
700-7588	Word Processing Manual Set of 2 books	A reference guide to specific Word Processing operations. A training manual designed for users not familiar with Wang Word Processing.
700-7600	PC Multiplan Manual Set of 2 books	A Multiplan Training Guide for user creation of a sample spreadsheet. A Multiplan Reference Guide that provides specific information on the command functions and procedures necessary to use Multiplan effectively.
700-7594	Compiled Basic Reference Guide	A reference guide for Compiled Basic Programming.
700-7595	FORTRAN Reference Guide	A reference guide for FORTRAN programming.
700-7596	PASCAL Reference Guide	A reference guide for PASCAL programming.
700-7597	COBOL Reference Guide	A reference guide for COBOL programming.
700-7598	Assembler Reference Guide	A reference guide for Assembler language programming.
700-8319	SNA 3276 Emulator Users Guide	A reference guide for Systems Network Architecture (SNA) communications.

Domestic and Canadian field personnel can order User documentation by submitting a withdrawal request to the following address:

WANG LABORATORIES INC.
General Services M/S 1183
51 Middlesex Street
No. Chelmsford, MA 01863

International field personnel can order User documentation by submitting a withdrawal request to the following address:

WANG LABORATORIES INC.
International Documentation Coordinator
M/S 1151
1 Industrial Avenue
Lowell, MA 01851

Table 1-3. Wang CE Maintenance Documentation

Document Number	Title	Information Contained
729-0000-B	Documentation Control and Processing Catalog	Contains listings of available CE documentation.
729-0976-A	CE Reprint For Epson MX80 Printer	A technical manual that contains the electrical and mechanical operations and repair of Epson MX80 Printer.
729-1241	PC Schematic Manual	Schematics pertaining to the PC.
729-1241-1	PC Schematic Update	Update to Schematic manual 729-1241.
729-1114	CE Reprint for Flexible Disk Drive 51/52	A technical manual that contains the electrical and mechanical operations of the 51/52 Disk Drive.
729-1167	CE Reprint For Tandon TM-100-1/2 Disk Drive	A technical manual that contains the electrical and mechanical operations and repair of Tandon 100-1/2 Drive.
729-1054	Daisy Printer DW20	A Wang PMM Manual on the repair and maintenance for DW20 Printer.

All CE Maintenance documentation can be ordered by writing to the following address:

WANG LABORATORIES INC.
c/o (Your Area Representative)
437 So. Union Street
Lawrence, MA 01843

1.3 SYSTEM DESCRIPTION

The low-cost Wang PC is a high performance, highly modular computer system which features both data and word processing capabilities. It can operate in a stand-alone mode, through coaxial cable to other Wang products, through telephone lines to Wang and non-Wang products, and through Wangnet.

The PC comes with many standard features and a host of optional features. This section describes each of these features and identifies the related product code (PC) for that feature.

1.3.1 Standard Equipment Supplied

The standard base unit PC (PC-001) is equipped with an Electronics unit, a Low-Profile Universal Keyboard, and a 5-1/4" Floppy Diskette Drive. See Figure 1-1.

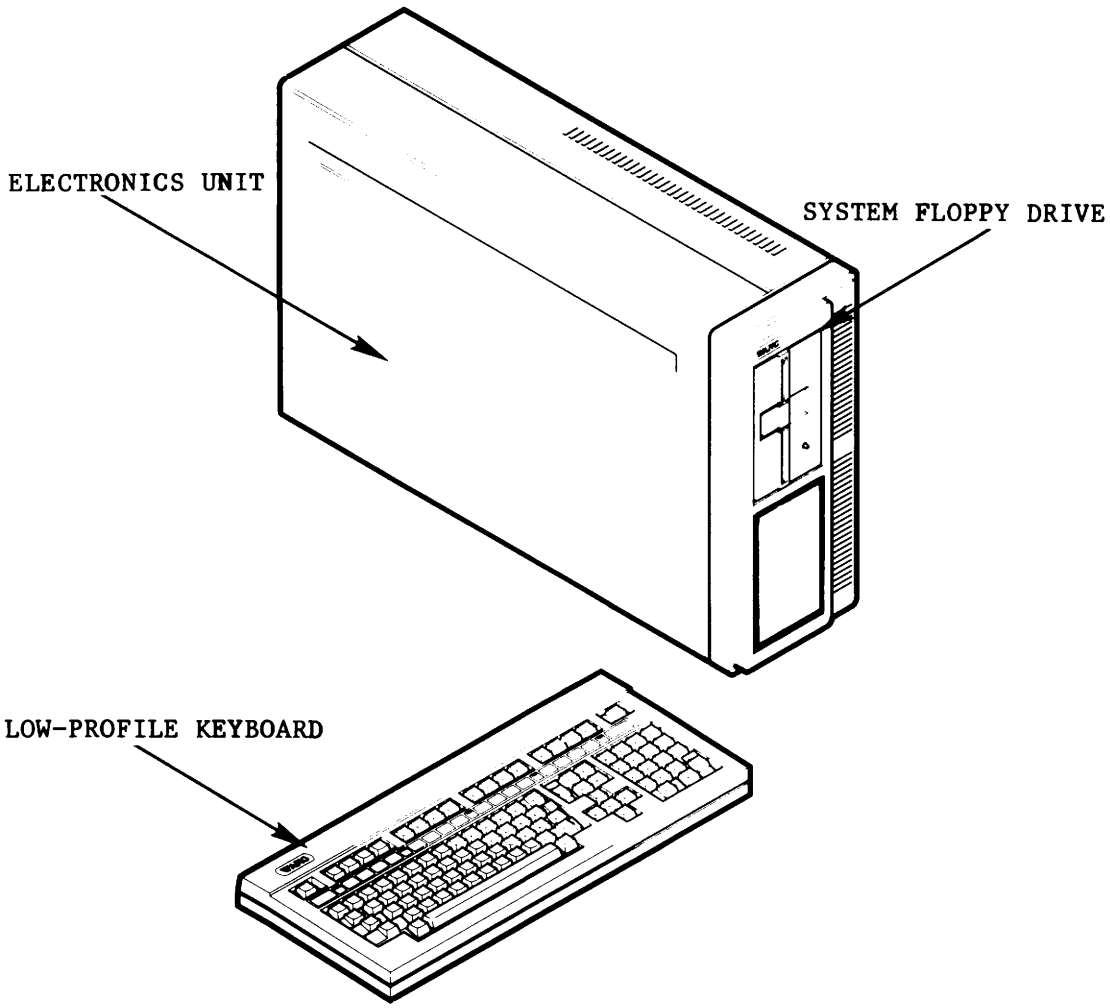


Figure 1-1. PC Standard Equipment (PC-001)

1.3.1.1 Electronics Enclosure (PC-001)

The Electronics Enclosure is compact, lightweight, and can control a variety of I/O devices. The Electronic Enclosure houses the 210-8221 CPU board, the 210-8237 Motherboard, the System Floppy Drive, an optional Floppy Drive or Winchester Disk Drive, the SPS-200 Switching Power supply, and up to five option boards. The Electronics Enclosure (PC-001) comes equipped with the following:

- o A standard 128KB of Parity-Checked memory for user programs.
- o Three channel direct memory access (DMA) capability.
- o A program-addressable internal clock.
- o An RS-232C asynchronous interface that supports serial devices and communications.
- o A Centronics-compatible parallel printer interface.
- o A standard 360KB Floppy Diskette Drive.
- o A keyboard interface.

1.3.1.2 Low-Profile Universal Keyboard (UNI/KBD-xx)

At present, five keyboard configurations are available for the PC. Refer to the following table:

Table 1-4. Keyboard Configurations

WLI No.	MODEL No.	DESCRIPTION
279-2042-US	UNI/KBD-US	KYBD UNIV KTC LOW PROF (UNITED STATES)
279-2042-UK	UNI/KBD-UK	KYBD UNIV KTC LOW PROF (UNITED KINGDOM)
279-2042-SL	UNI/KBD-SL	KYBD UNIV KTC LOW PROF (SPANISH-LATIN AMERICAN)
279-2042-AZ	UNI/KBD-AZ	KYBD UNIV KTC LOW PROF (AZERTY)
279-2044-GE	UNI/KBD-GE	KYBD UNIV EXP LOW PROF (GERMAN EXPANDED)

The Low-Profile Keyboard is a separate, detachable keyboard that contains 101 keys and a programmable speaker that can produce three simultaneous tones. The keyboard offers 16 programmable function keys, a HELP key, four cursor control keys (North Arrow, South Arrow, East Arrow, and West Arrow), as well as a calculator style key pad. Standard word processing Edit keys are also supported (eg. Insert, Delete, Move, Copy). A wide range of international character sets are supported and access to the complete 234 character set is provided.

1.3.1.3 Floppy Diskette Drive

One 5 1/4 inch Floppy Diskette Drive capable of 360K Bytes (the diskette controller is located on the CPU Board) is included with the base system. A second Floppy Diskette Drive (optional) can be installed in the base unit to provide an additional 360KB of storage. The optional Floppy Drive is controlled by the same diskette controller located on the CPU board.

1.3.2 OPTIONS

Many system options can be attached to further enhance the PC Base unit. Restrictions apply to some options. These restrictions will be discussed in respect to those particular options.

1.3.2.1 Monochrome Display (PC-PM004)

The Wang monochrome display is mounted on a pedestal base. This allows the user to rotate the device for ease in viewing. The display can be either placed on a flat surface (ie. desk top or on the top of the Electronics Enclosure when its position horizontally) or can be mounted on the optional pivot arm.

The pivot arm can be clamped to the side of a desk which allows the user to move it up to 14 inches off the desk at any angle or position.

The monitor's CRT is a 12 inch green-on-black diagonal screen that has a display area of 80 columns by 25 rows. The monitor must be used with either the Character Display Adapter (210-8243/8343) or the Character Display Adapter in conjunction with the Graphics Display Adapter (210-8233). Both adapters are further described below.

The monitor houses the CRT, the CRT monitor board, and a flyback transformer. The monitor's power is supplied through the monitor cable from the SPS-200 Power Supply.

1.3.2.2 Character Display Adapter (PC-PM001)

The Character Display Adapter is necessary to drive the Wang Monochrome display to generate the characters. The character resolution is 80 columns by 25 rows. This adapter is plugged into one of the five option slots within the Electronics Enclosure and is connected to the monitor via a dual cable. The monitor cable supplies the monitor with the operating voltages via one cable of the dual cable and the TTL Video via the other cable.

1.3.2.3 Graphics Display Adapter (PC-PM002)

The Graphics Display Adapter is necessary to drive the Wang Monochrome display to generate graphics. This adapter MUST be used in conjunction with the Character Display Adapter. When the Graphics Display Adapter is used with the Character Display Adapter, graphics with a resolution of 800 X 300 pixels as well as characters can be displayed. This adapter is plugged into one of the five option slots within the Electronics Enclosure and is cable-connected to the Character Display Adapter. Due to the cable length, the Graphics Resolution PCB must be installed adjacent to the Character Display PCB.

1.3.2.4 Color and Graphics Display Adapter (PC-PM003)

The Color and Graphics Display Adapter is necessary to control a Customer purchased output display device. The following four types of output devices can be driven by this adapter:

- o U.S. standard NTSC B&W Television with attached RF modulator.
- o U.S. standard NTSC Color Television with attached RF modulator.
- o B&W Video Monitor.
- o RGB Color Video Monitor.

Industry standard frequencies are supported. The display resolution, display area, and character size will vary depending on the attached output display device. This adapter is plugged into one of the five option slots within the Electronics Enclosure and is cable-connected to the output display device.

1.3.2.5 Memory Expansion Cards

The base system PC contains 128K of dynamic RAM memory within eighteen 64K RAM devices located on the 210-8221 PCB. To increase the program and data storage capabilities of the PC, a Memory Expansion card with additional dynamic RAM chips can be installed into one of the five option slots in the Electronics Enclosure unit. This option provides an additional 128K (PC-PM030), 256K (PC-PM031), or 512K (PC-PM032) of dynamic RAM to increase total memory capacity to either 256K, 384K, or 640K respectively.

1.3.2.6 Remote Communications (PC-PM040)

The Remote Communications option provides synchronous communications capabilities. This permits the PC to communicate through Wangnet to any Wangnet system or through a modem with auto-call feature to most any CPU system.

1.3.2.7 Local Communications (PC-PM041)

The Local Communications option provides 928-type workstation emulation for utilization by the PC. This option consist of two PCB boards interconnected through a ribbon cable. One board operates as a Datalink/Memory board operated directly from the PC's 8086 CPU, the other contains the circuitry necessary to allow operation of programs written for VS and OIS applications. These boards should occupy adjacent bus slots due to the interconnect cable length.

1.3.2.8 CP/M-80 Emulation Board (PC-PM050)

The CP/M-80 Emulation board allows the Wang PC to emulate the CP/M-80 operating system. This board can be installed into any of the five option slots in the Electronics Enclosure unit.

1.3.2.9 10MB Winchester Disk Drive and Adapter Board (PC-PM021)

A 5 1/4 inch Winchester Disk Drive can be installed in the base unit. The drive is housed in the same location in the base unit that is reserved for a second Floppy Drive. Either the second Floppy Drive or the Winchester can be installed, but not both. The Winchester Controller board must be installed in SLOT 5 ONLY (J9) of the Electronics Unit. This restriction is due to cabling required for the Winchester Drive. The Winchester Drive (when installed) is designated as Drive C.

1.3.2.10 20-CPS Daisy Printer (PC-PM011)

The DW20 Daisy printer is a bidirectional printer that operates at 20 cps (characters per second). This printer can print up to a 132 character line at 10 pitch and a 158 character line at 12 pitch.

The printer's character set contains 96 characters including uppercase and lowercase letters, numbers and special characters and symbols. The DW20 printer connects via a cable to the Base system's parallel port. Refer to the Daisy Printer DW20 manual (WLI P/N 729-1054) for printer specifications.

1.3.2.11 80-CPS Matrix Printer (PC-PM010)

The MX-80FT TYPE III Printer is a compact, bidirectional matrix printer that operates at 80 cps. The matrix printer is best suited for producing low volume draft quality output and graphics. Each pin on the printhead's font can be controlled as the print head moves across the paper. This enables the printer to print pictures, plot graphs, or create special character sets. The MX-80FT TYPE III printer connects via a cable to the Base System's parallel port. Refer to the CE Reprint For The Epson MX80 Printer (WLI P/N 729-0976) for printer specifications.

1.3.2.12 Monitor Clamp and Arm (PC-AC001)

This optional accessory is available to provide free movement and best placement for operator use of the Monitor. The arm can elevate the monitor 14 inches (35.56 cm) above the desk and pivot 25 to 30 degrees around its base. The clamp can be fastened to either side of a desk or table that has a 1 inch (minimum) to 2 inch (maximum) lip.

1.3.2.13 System Unit Clamp (PC-AC002)

This optional accessory is available to provide attachment of the Electronic Enclosure unit to a desk or a table. The clamp can be used for right or left side mounting on a desk or a table that has a 1 inch (minimum) to 2 inch (maximum) lip.

1.3.2.14 Additional Floppy Diskette Drive (PC-PM020)

A second Floppy Diskette Drive (optional) can be installed in the base unit to provide an additional 360KB of storage. This second Floppy Drive is controlled by the same diskette controller as fore mentioned in paragraph 1.3.1.3 Floppy Diskette Drive. This Drive is designated as Drive B.

1.4 SYSTEM CONFIGURATIONS

The PC is available in a number of configurations that can be tailored to meet specific customer requirements. At present, five prepackaged configurations made up of both standard and optional features can be ordered. These are delivered preassembled so that the customer does not have to install the adapter boards thereby minimizing the requirements of ordering, configuring, and setting up the delivered system. When ordering a particular PC configuration, the number of option slots must be considered since there are only five option slots available on the base unit. Customers may order more than five options, however; only five may be installed at any one time. Some option boards have particular restraints that will be discussed in detail in Chapter 2. Table 1-5 lists the five available PC configurations.

Table 1-5. PC System Configurations

	PC-				
HARDWARE/SOFTWARE	001	002	003B	004A	005A
Base System Unit with 128k Memory	X	X	X	X	X
360K Floppy Disk Drive	X	X	X	X	X
Low Profile Keyboard	X	X	X	X	X
MS/DOS Operating System (Plus Interpreter Basic)	X	X	X	X	X
MS/Compiled Basic	X	X	X	X	X
PC-PM001 Character Display Adapter		X	X	X	X
PC-PM004 Monochrome Display		X	X	X	X
PC-PM020 Second 360K Floppy Drive			X	X	
PC-PM002 Graphics Display Adapter				X	X
PC-PM030 Additional 128K RAM					X
PC-PM021 Winchester 10MB Disk Drive (with Adapter)					X

1.5 SYSTEM SPECIFICATIONS

Dimensions

Electronics Enclosure

Width	14.9 inches	(37.8 cm)
Length	23.1 inches	(58.7 cm)
Height	6.5 inches	(16.5 cm)

Monitor Assembly

Height	11.8 inches	(30.0 cm)
Width	13.0 inches	(33.0 cm)
Depth	10.8 inches	(27.4 cm)

Keyboard Assembly

Height	1.7 inches	(4.3 cm)
Width	18.3 inches	(46.5 cm)
Depth	7.8 inches	(19.8 cm)

Net-Weight

Electronics Enclosure	27.8 lb	(12.6 kg)
Monitor Assembly	14.0 lb	(6.4 kg)
Keyboard Assembly	4.5 lb	(2.0 kg)

Power Requirements

Minimum	Nominal	Maximum	Frequency
90v	115v	132v	47 - 63 Hz
180v	230v	264v	47 - 63 Hz

Wattage

330 watts at 115 volts
330 watts at 230 volts

Amperage

3.0 Amps at 115 volts
1.5 Amps at 230 volts

Operating Environment

Ambient Temperature
60 deg. F to 90 deg. F (16 deg. C to 32 deg. C)

Heat Dissipation

870 BTU per Hour

Non-operating Environment

Temperature
50 deg. F to 104 deg. F (10 deg. C to 40 deg. C)
Relative Humidity -- 20% to 80% (noncondensing)

Cabling

DW20 Printer Cable not to exceed 25 feet (7.6 meters)
MX80 Printer Cable not to exceed 25 feet (7.6 meters)

CHAPTER 2

THEORY

2.1 INTRODUCTION

This chapter contains the theory of operation of the PC system structure as well as individual PCBs operation and interface. The PCB theory consists of the PCBs required for PC configuration PC-002. Option PCBs theory is discussed in the latter part of this chapter.

The following discussion of the WANG Professional Computer is sectionalized into its main block functions. Block diagrams are used in conjunction with the text for references within the discussion. Reference will also be made to the schematics pertaining to the PCB being discussed. Mnemonic codes are defined during the discussion and an Alphanumeric listing of mnemonic codes is contained in Appendix C.

2.2 SYSTEM FUNCTIONAL DESCRIPTION

For the following discussion refer to the System Block Diagram, Figure 2-1. Each of the blocks will be discussed separately.

The System Unit consists of the following components:

- o CPU Board (210-8221)
- o SPS200 Power Supply
- o Motherboard (210-8237)
- o 360K Floppy Drive
- o Medium Resolution Character Generator (210-8243/8343)
- o Low-Profile Serial Keyboard
- o Wang Monitor
- o Option Boards
- o External Options

2.2.1 8221 CPU Board

The 8221 CPU board contains the logic devices required for PC operations as well as the handshaking capabilities between option devices that can be installed to enhance the PC operating ability. The CPU board is installed in busboard slot 0 (J4) and can only be installed in that slot. The CPU board interfaces directly to the Low-Profile keyboard via connector J3, an optional parallel printer via connector J2, and a RS232 connector via J4.

The 8221 CPU board contains the 16-bit master CPU device 8086 and an optional co-processor 8087 operating at 8 MHz. The 8086 CPU provides a 16-bit bidirectional data bus and a 20-bit address bus.

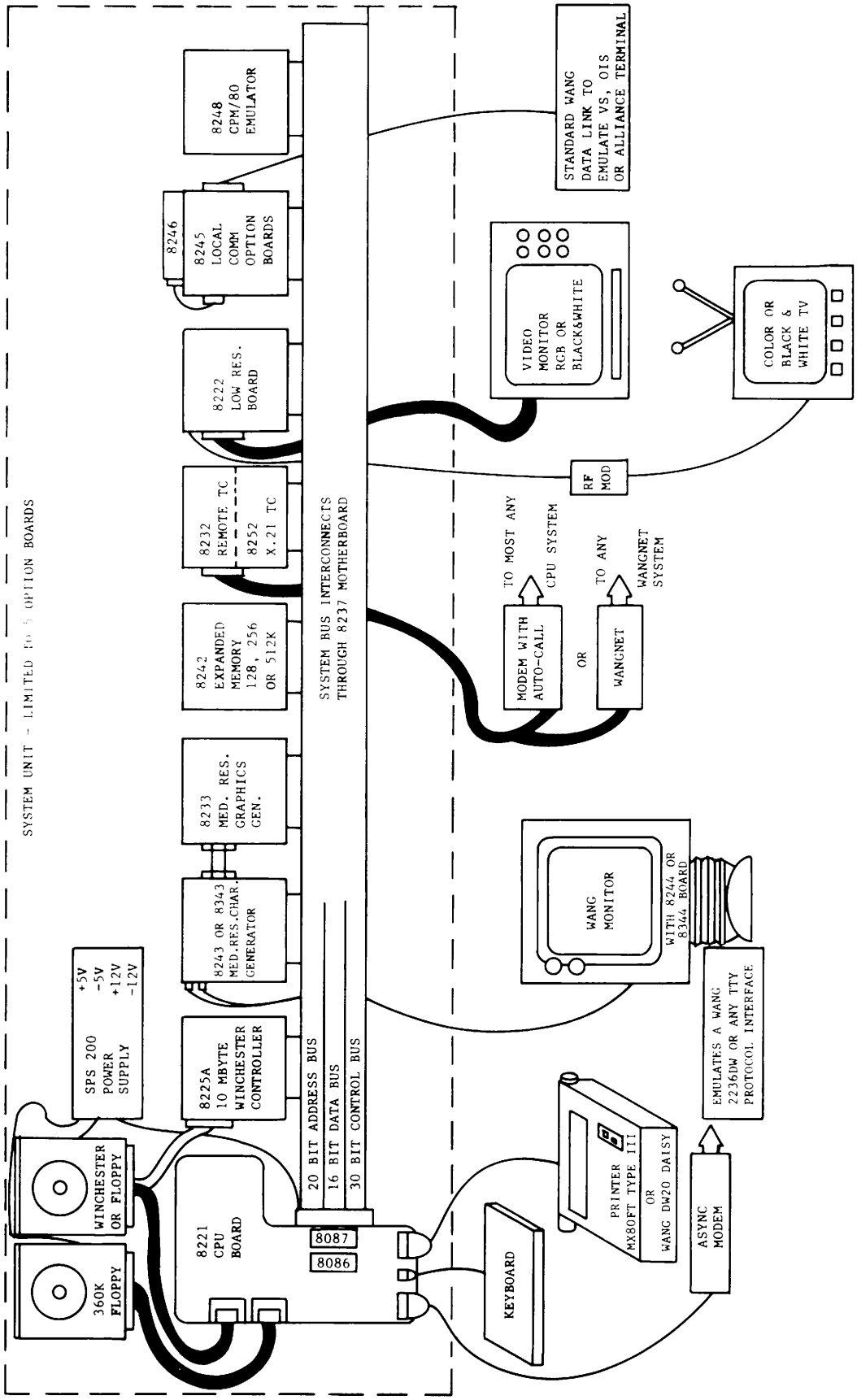


Figure 2-1. PC System Block Diagram

The 8086 CPU controls the bus except for the DMA transfers, which are controlled by the DMA logic (also located on the CPU board). The 8086 has direct addressing capability of one million bytes (1 Mbyte) of memory (location 0000H to FFFFH).

Also contained on the CPU board is 128K of parity-checked Dynamic Ram memory that can store system programs, application programs, or data. In addition to the dynamic RAM, two PROM devices contain the B.I.T. diagnostics and the bootstrap loader.

A 6402 UART is employed on the board to receive and transmit data to and from the keyboard. The CPU also contains the logic required to operate either one or two Floppy Disk drives.

The 8221 CPU board is discussed in detail in paragraph 2.3.

2.2.2 SPS200 Power Supply

The SPS200 Power Supply is a switching power supply that is switch selectable for either 115 vac or 230 vac input voltage. This power supply provides four regulated voltages (+5, -5, +12, -12) required by the PC operating system. These voltages are supplied through the common bus to all option boards as well as cable-connected to the floppy drives (Winchester). Power required by the Wang Monitor and the Low-profile Keyboard are also supplied by this source.

2.2.3 8237 Motherboard

The Motherboard provides a common bus that extends the 20-bit Address bus, the 16-bit Data bus, and the 30-bit Control bus to the other five option slots. These option slots are prioritized with Slot 5 having the Highest priorty and Slot 1 having the lowest priorty. Also common bussed are the voltage levels required by the system.

A feature unique to the PC is the slot decoding scheme which is hard-wired on the Motherboard's option slots and read by a software routine to determine whether an option board is installed in each slot and if installed what the option is. This scheme is discussed in detail later in this chapter.

2.2.4 360K Floppy Drive

The 360K Byte Floppy Drive presently used are Tandon and MPI drives operating MFM at 250 BPS (Bits per Second). The diskettes are 5 1/4 inch. Each diskette contains 40 tracks per side, double sided, with nine sectors per track. Each sector containing 512 bytes of data for a total of 368,640 bytes (360KB) of data per diskette.

The disk operating speed is 300 RPM $\pm$ 1.5% (300 RPM $\pm$ 45 RPM). The power requirements for the drive is +5 and $\pm$12 volts dc which is supplied by the PC's SPS-200 Switching Power Supply through the main harness assembly. See Figure 5-1 Power Distribution and Interconnection Diagram.

The system inputs and outputs data to the floppy drive. The floppy drive is a self-contained unit and is controlled by the CPU. Communications between the floppy drive and the CPU are via the Floppy Disk Controller chip which is located on the 8221 CPU board. Theory of operation of the floppy drive is not discussed in this manual. Refer to CE Reprint Manuals WLI No. 729-1167 for the Tandon Drive and WLI No. 729-1114 for the MPI Drive.

2.2.5 Medium Resolution Character Generator (210-8243/8343)

The medium resolution video controller produces TTL output to drive a Wang monochrome video monitor. Running at 18.824 KHz horizontally and 60 Hz vertically, the controller has 800 pixel by 300 pixel resolution when displaying either text characters or bit mapped dot graphics. The medium resolution video controller is under the control of the 8086 CPU device and is synchronized by the systems 8 MHz clock. An optional bit mapped graphics board, which must be paired with a character board via a ribbon cable, can be installed to produce bit mapped graphics. This board is discussed later in this chapter under Options (paragraph 2.2.8.2).

The 8243/8343 PCB is installed in any of the five busboard slots and is cable-connected to the Wang Video monitor via two cables. One cable (TTL Video) is an eight-pin barrel plug that provides the video signals to the Video Monitor. These signals include video, horizontal sync, vertical sync, and the intensity signals. The other cable (power) is a barrel plug that provides the power required by the Video monitor.

2.2.6 Low-Profile Serial Keyboard

The Low-profile Serial Keyboard connects directly to the 8221 CPU board via the four-wire keyboard cable connected at the CPU connector J3. The keyboard cable supplies the +5 volts and ground as well as being the median for the transferring of the serial transmit data and serial receive data.

The Low-Profile Keyboard contains an 8031 microprocessor and a 2758 1K Byte EPROM that contains the key decoding scheme. Included in the 8031 is an on-chip UART that provides the serial communication with the System Board's 6402 UART at 62.5 KBAUD rate. Two 8-position DIP switches are located on the keyboard PCB although these switches are not used. Six LEDs are located on the keyboard for diagnostic purposes and are turned on and off by the system software. When any key on the keyboard is depressed, its capacitive reactance will cause the 908 chip to output its specific bit configuration to the 8031 and raises an interrupt. The 8031 program will then convert the byte to serial data and transmit it to the 6402 UART located on the System board over the four-wire interface cable.

A speaker built into the keyboard enclosure is operated by a programmable tone oscillator chip, 76489. The volume level of the chip is under program control where as the system program can read the tone and volume setting at any time. Two tones can be programmed at once. If a character key is hit a BEEP will result and if a system function or command key is depressed a cheep will result. If these tones are not satisfactory, they can be changed to CLICK and CLACK sounds.

2.2.7 Wang Monochrome Monitor

The WANG Monochrome Display connects to the 8243/8343 Medium Resolution Character board via a dual cable that contains a cable for TTL video and a cable for the +12 volts and ground. The monitor's CRT is a 12 inch green-on-black diagonal screen that has a display area of 80 columns by 25 rows. If the graphics package is included, the screen is bit mapped 800 horizontal dots X 300 vertical dots and the graphics software package must be programmed to drive the display. The monitor is mounted on a "half-moon" swivel for operator convenience. The monitor must be used with either the Character Display Adapter (210-8243/8343) or the Character Display Adapter in conjunction with the Graphics Display Adapter (210-8233).

The monitor houses the CRT and the CRT monitor board. The monitor board contains a flyback transformer that provides the CRT gun and anode voltages. The Monitor board also contains the logic required to convert the video signals into an output display.

2.2.8 Option Boards

The Option Boards that can be installed in the PC are explained below. The option boards enhance the PC's capabilities and are not required for the basic operation of the system. Each board or board set is discussed individually including any restrictions that apply to that particular option.

2.2.8.1 10M Byte Winchester Controller (8225A) and Disk Drive

The 10M byte Winchester Controller PCB is an optional accessory required for the operation of a 10Mbyte Winchester Disk Drive. This option must be installed in busboard connector J9 (Slot 5) due to the cabling required. The 8225A PCB contains a Z80A microprocessor which is under the control of the 8086 CPU device.

The on-board Z80A CPU performs all disk surface operations to include the command phase, execution phase, and the result phase of the operations. The 8225A PCB is cable connected to the Winchester Drive via two ribbon cables. Refer to Chapter 4 Figure 4-39 for correct orientation of the cables.

The Winchester drive stores up to 10M bytes of formatted data using both sides of its dual platters. Under the direction of the WDC, its moveable read/write head assembly accesses 304 logical tracks on the recording media surfaces. There are sixteen 512-byte sectors per track on each surface, for a total 32 sectors per cylinder on a single-platter drive. Disk platters and recording heads are housed within a hermetically sealed enclosure with a filtered air recirculating system that protects both media and the heads from temperature variation and environmental contamination.

2.2.8.2 8233 Medium Resolution Graphics Generator

The 8233 Medium Resolution Graphics Board connects to the 8243/8343 board and cannot be used by itself, even though the 8243/8343 board can. The 8233 Graphics board uses the timing signals and the composite video from the 8243/8343 Board. The Graphics Board contains 32K bytes of dynamic RAM (sixteen 16K x 1 bit DRAMs) bit mapped memory that provides storage for the 800 x 300 (240,000) pixels required to map the CRT screen. Memory Refresh is performed on-board independently of the 8086 CPU. This PCB should occupy a bus slot adjacent to the 8243/8343 PCB due to the interconnect cable length.

2.2.8.3 8242 Expanded Memory Board

The 8242 extended memory board augments the 128k bytes of standard system memory with 128k, 256k, or 512k bytes of extended dynamic RAM with parity. Extended memory address space is organized into four 128K-byte banks.

2.2.8.4 8248 CP/M-80 Emulator

The 8248 CP/M-80 Emulator board contains a Z80A microprocessor chip operating at 4 MHz and 64K bytes of dynamic RAM. The Z80A operates independently from the 8086 CPU device with each CPU device having the ability to access the 64K of on-board memory. The Z80A CPU can be put into idle states by the 8086 therefore the 8086 can interrupt the Z80A. All memory timing is generated on-board independent of CPU control.

The CP/M-80 PCB allows the PC to read a disk formatted in 8-bits, store the data, and allow the data to be transferred in 16-bits to the PC main memory. Also, the CP/M-80 can transfer 16-bit data into the 8-bit format. This allows the PC the flexibility of running 8 bit programs.

2.2.8.5 8222 Low Resolution Board

The low resolution video controller option incorporates an MC6845-1 video timer and controller chip to drive a conventional monochrome broadcast television set, a color broadcast television set, a monochrome video monitor, monitor, or a red-green-blue (RGB) color monitor. All four low resolution display options use 15.70 KHz horizontal and 60 Hz vertical frequencies. All display 25 lines of text on the screen, but the number of characters in a line can be either 40 or 80, depending on whether a broadcast television set or a video monitor is used. Video monitors can display either 40 or 80 column text. A broadcast television set must use only the 40-column display format.

The customer has the responsibility of providing the broadcast television set or a video monitor. If the broadcast television set is selected, the customer must also provide a RF Modulator.

The low resolution video controller option can be installed in any of the Busboard's option slots. The controller board provides output connectors for both TV and Video Monitors.

2.2.8.6 Remote Telecommunication Controller (8232)

The 8232 Remote Telecommunication Controller contains a Z80A microprocessor, a multi-channel direct memory access controller, 4K bytes of EPROM for bootstrap loading and diagnostic programs and 60K bytes of RAM. The RTC board communications with the PC's CPU by DMA for data transfers and by interrupts for status information.

The RTC board supports both RS232-C and Automatic Calling Unit (ACU) interfaces. The RTC option is a single board that can be installed in any of the option slots available within the PC. Software is offered for the RTC to run 2780 or 3780 Batch Communications or to connect to Remote Wangnet.

2.2.8.7 Local Communications Option

The Local Communications Option consist of two boards; a CPU board and a Data Link board. The CPU board contains a Z80A microprocessor chip, 64K bytes of main memory and 16K bytes of CRT memory. The Data Link board contains all the logic necessary to emulate the standard Data Link interface portion of a Wang OIS or VS workstation. The Data Link board connects to a VS CPU, OIS Master Unit or a 928 Master Unit. This allows the PC to operate as an OIS, VS, or 928 Workstation.

The Local Communications dual board option must be installed in two adjacent option slots available within the PC.

2.2.9 EXTERNAL OPTIONS

A description of External Options available for the PC is explained in the following pages. Functional theory of these options are not discussed in this manual since these items are either Vendor supplied options or a technical manual is already available. Refer to Chapter 1 Table 1-3 for a reference of CE Reprint Manuals available.

2.2.9.1 Printers

Currently Wang offers two printers that can be used on the Professional Computer. These are; Epson MX80FT Type III and Wang Low-cost Daisy. Both printers connect to the CPU board's parallel port J2. The printers power is supplied via internal power supplies that require an ac input. No power is supplied by the PC for printer operations.

The Epson MX80FT Type III printer is a bidirectional dot matrix printer that operates at 80 cps. Each pin of the printheads font can be controlled individually as the printhead moves across the median. This allows greater flexibility when printouts of graphics and special characters are required. A Customer Engineering Reprint of the MX80 Printer Manual is available under part number 729-0976.

The Low-cost DW20 Daisy Printer is a bidirectional daisy printer that operates at 20 cps. This printer can print up to a 132 character line at 10 pitch or a 158 character line at 12 pitch. The printer outputs letter quality print. A Wang Product Maintenance Manual is available under part number 729-1054.

2.2.9.2 Wangnet (Modems)

Wangnet System or Modems with auto-call can be connected to the PC via the Remote Communications board 8232. This allows the PC to interface through most any CPU system or through the Wangnet System.

2.2.9.3 Video Monitors And Televisions

Video Monitors or televisions can be used to display the video output of the PC. If a Video Monitor is used (B/W or Color) the Low Resolution PCB must be installed. These Video Monitors are customer purchased items and are the responsibility of the customer for Preventive Maintenance and repairs. The Video monitor is cable-connected to the Low Resolution board. The monitor displays 80 characters per line X 25 lines.

If a television is used (B/W or Color) the Low Resolution PCB must be installed. The televisions are customer purchased items and also are the responsibility of the customer for Preventive Maintenance and repairs. The Television is also cable-connected to the Low Resolution board but a RF modulator must also be installed. The television displays 40 characters per line X 25 lines.

2.2.9.4 Async Modem

An Async Modem can be attached directly to the CPU board's RS232 connector J4. This allows the PC to serve as a workstation on the Wang 2200. As a workstation on the Wang 2200 system, the PC has access to the software, data, and resources of that system.

2.3 8221 CPU/SYSTEM BOARD THEORY OF OPERATION

The CPU/System board theory is divided into two sections; the CPU Processor theory and the System Board theory. Reference is made to block diagrams during the following discussion. The schematics pertaining to this board are WLI 210-8221 (6 sheets). No reference or callouts are made to the schematics as the theory of operation is only to the block diagram level.

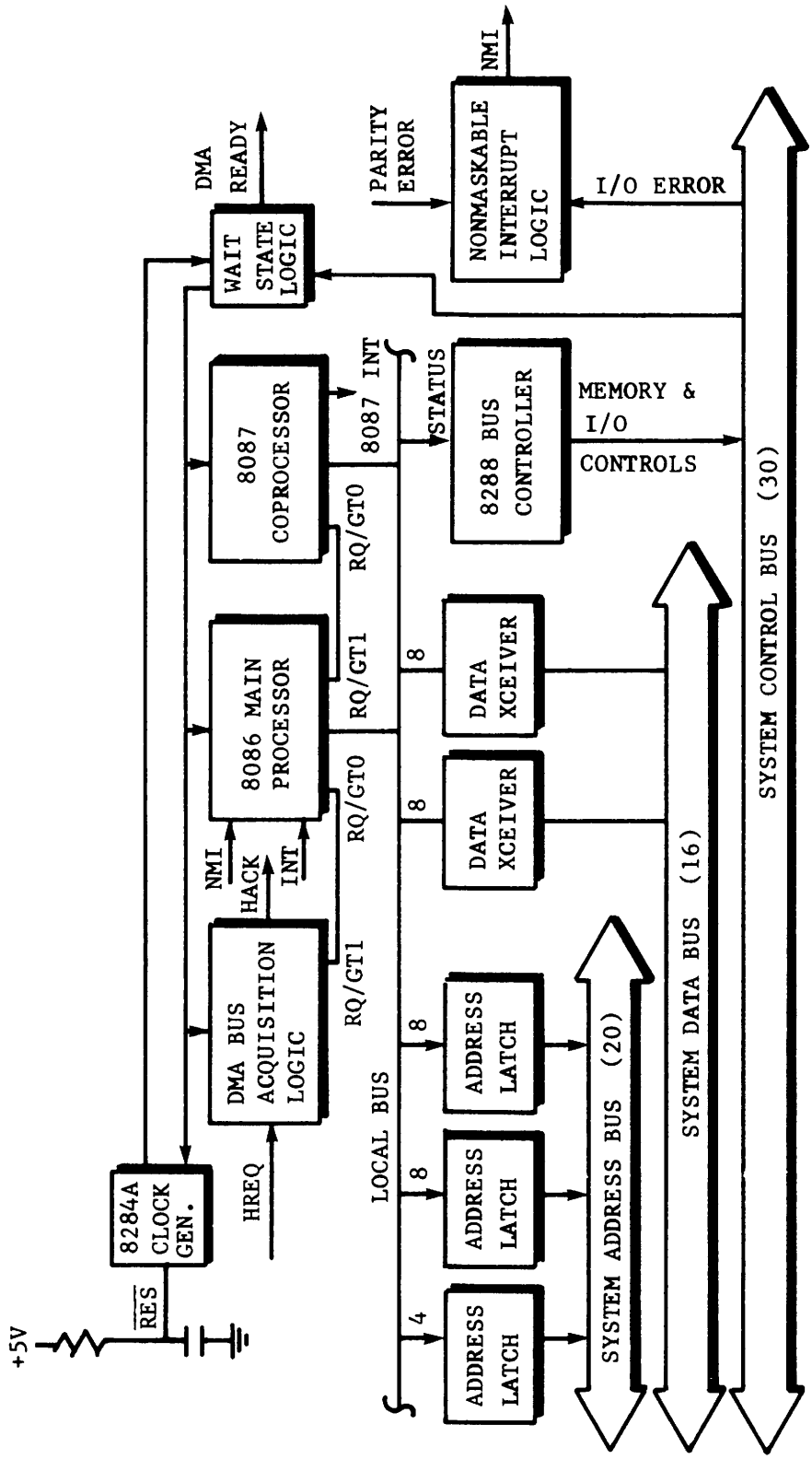


Figure 2-2. CPU Processor Block Diagram

2.3.1 CPU Processor Theory

For the following discussion refer to the CPU Block Diagram Figure 2-2.

2.3.1.1 8086/8087 Co-processors

The main processor is an 8086 running at up to 8 MHz; an optional 8-MHz 8087 coprocessor can be installed for high performance numeric data processing. The 8086 and its 8087 coprocessor communicate with one another across a local interprocessor bus. Both processors communicate with memory and I/O components across the system bus by means of address latches, data transceivers, and an 8288 Bus Controller chip.

8086 is the master and runs the main program. The 8086 is a 16-bit microprocessor with 20 address lines to access up to 1 Megabyte of memory. The 8086 also handles 2 levels of DMA requests. The higher level request (RQ/GT0) is connected to a 4 channel DMA controller chip through the DMA Bus Acquisition logic. The lower level request (RQ/GT1) is connected to the 8087 coprocessor.

The 8087 is a Numeric Data Processor (NDP) that operates as a coprocessor with the 8086 sharing the bus. The 8087 contains an extended 8086 instruction set that includes floating decimal point, trigonometry, exponents, and logarithmic functions plus high level math. The 8087 is not a stand-alone processor; it must be used in conjunction with an 8086 main processor. The 8086 fetches all instructions from memory and the 8087 monitors the op codes. When the op code is numeric, the 8087 executes it and the 8086 ignores it. For the 8087 instructions that require memory access, the 8087 requests a DMA cycle from the 8086 as it also shares memory with the 8086. Both chips are 40 pin and are installed in sockets.

The 8086 uses two types of addressing to access the 1M byte of memory the 8086 is capability of accessing. These are; memory reference instructions and input/output (I/O) instructions. Memory reference instructions generate memory mapped addresses. Input and output instructions generate I/O mapped addresses that identify I/O ports. When the system address bus contains an address on A1-19, other bus control lines determine whether the address identifies a register in a memory mapped device or an I/O port. Block diagram of Memory Mapped Addressing is shown in Figure 2-3 and a block diagram of I/O Mapped Addressing is shown in Figure 2-4.

Any addressable device can be designed to respond to a memory mapped address or an I/O port address. Addresses on I/O option boards are I/O mapped because I/O ports are identified in terms of the expansion slot in which a circuit board is installed. I/O option boards that contain memory mapped addresses, those addresses remain the same no matter where the circuit board is installed. They are reserved for their intended purpose, and special circuitry disables those addresses when they are not needed.

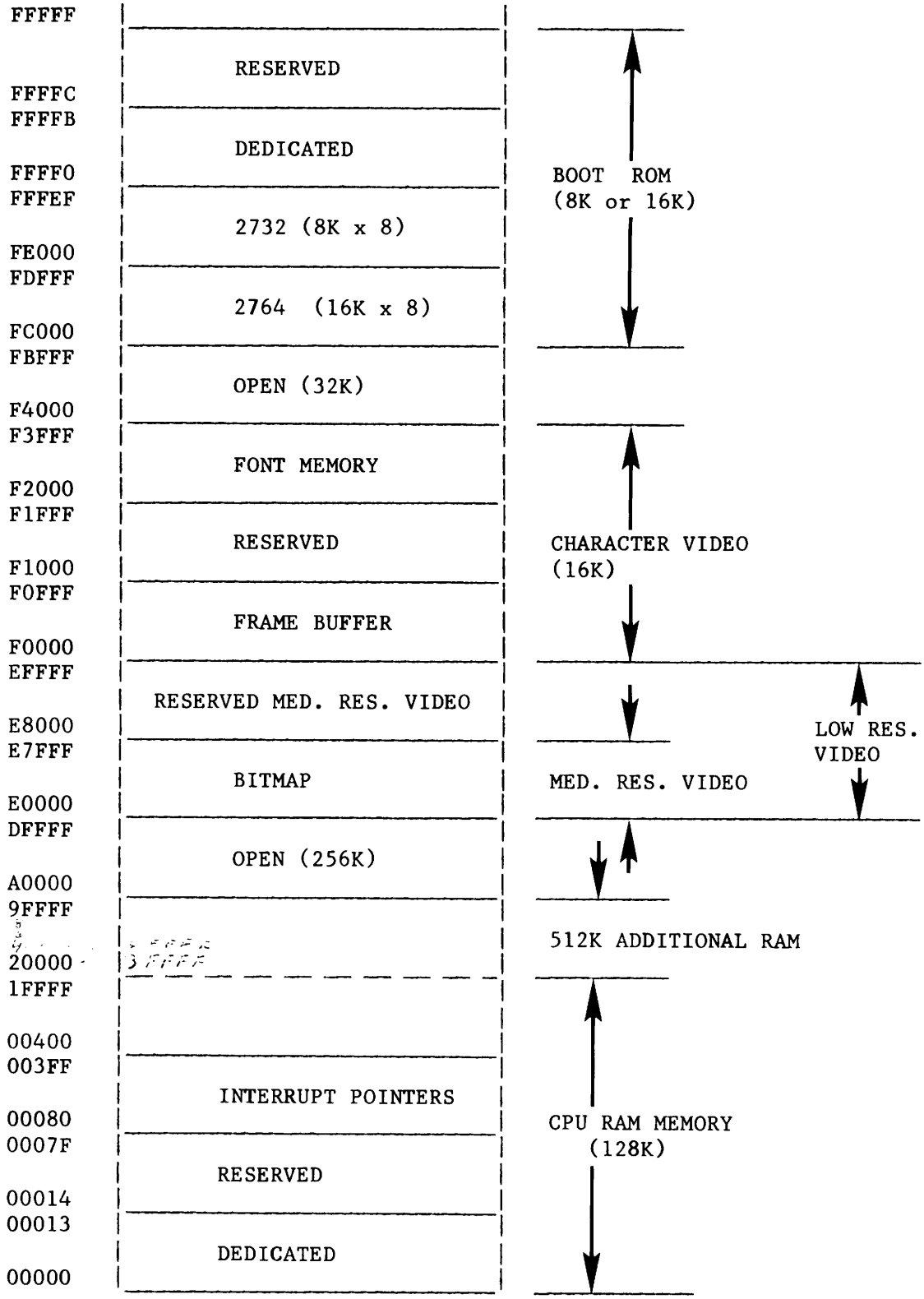


Figure 2-3. 8086 Memory Mapped Addressing

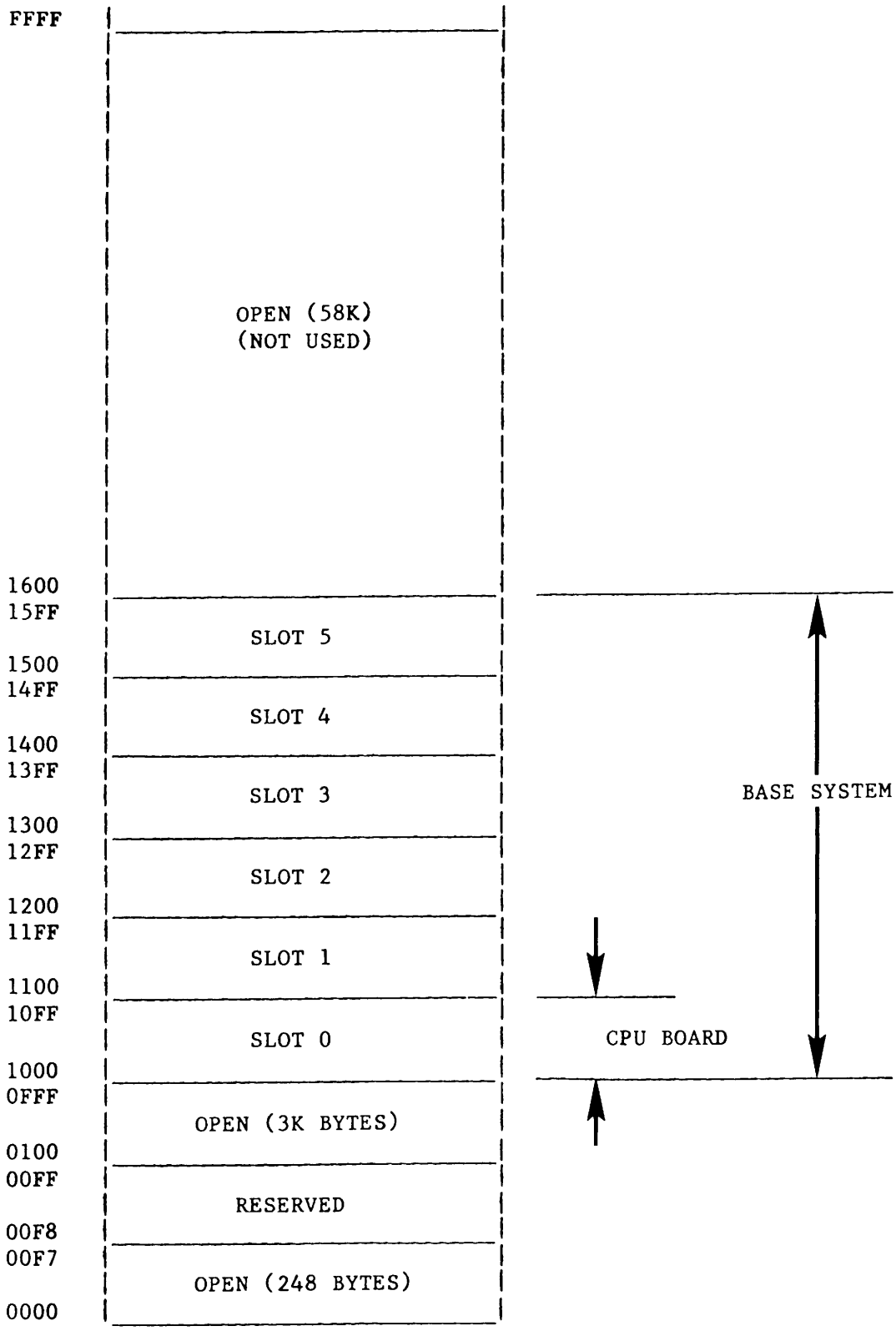


Figure 2-4. 8086 I/O Mapped Addressing

2.3.1.2 8284A Clock Generator and Wait State Logic

The 8284A Clock Generator generates an 8 MHz system clock from a 24 MHz crystal to drive the 8086/8087 and provides a general system clock that is also subdivided to drive slower devices such as the 4 MHz DMA chip, the 500 KHz floppy controller, and the CTC chips. The 8284A also provides the system reset signal for the system as well as the ready signal for the 8086/8087.

The Wait State Logic provides the 8284A with two ready signals, RDY1 and RDY2 (READY 1, READY 2). These two signals control the READY output to the 8086/8087 chips. When a PROM read or write or an I/O read or write is initiated, this logic toggles ready off for one T cycle. This results in the 8086/8087 inserting a one T-time wait state between T3 and T4 of the bus cycle. This is to allow for slower speed devices to respond to the I/O command. An 8086 T-time equals 125 nanoseconds and four T-times equal an 8086 bus cycle (500 nsecs). This is all the time required for main memory access during data-read and data-write operations.

2.3.1.3 DMA Bus Acquisition Logic

The DMA Bus Acquisition logic synchronizes the DMA requests with the CPU timing and controls the width of the REQUEST pulse. When the CPU completes its current bus cycle it will acknowledge the request by gating a 125 nsec pulse onto the RQ/GT0 line. This will cause the logic to gate acknowledge (HACK) back to the DMA controller. Once HACK is received by the DMA Controller, the controller executes the DMA transfer. The DMA Controller will then drop HREQ, and the bus acknowledge logic will gate the release pulse to the CPU on the RQ/GT0 line.

Once the DMA controller becomes the system bus master, it responds to the DMA request by asserting the corresponding DMA acknowledge (DACK1-3) line and placing an address on the system address bus. The device that initiated the DMA request is always an I/O mapped device and the address that the DMA controller places on address lines A0-19 in conjunction with BYTE HIGH ENABLE active low (-BHE) is always a memory mapped address. The I/O mapped device must recognize its DMA acknowledge signal and respond by reading (or writing to) the system data bus. The memory mapped device must recognize its address on the address bus and respond by writing (or reading) the system data bus. The DMA controller asserts one of two pairs of system bus signals to control the direction of the transfer.

2.3.1.4 DMA Controller Programming

Software in the 8086 writes to DMA registers to program each channel of the DMA controller. This establishes the direction of a DMA transfer, the first memory mapped address involved in the transfer, and the number of bytes to be transferred at successively higher or lower memory addresses. The 8086 also programs each I/O device option and assigns no more than one active device to each DMA channel.

By convention, the number of the DMA channel assigned to an I/O option board is always four less than its interrupt priority level. For example, all I/O option devices that operate at interrupt priority level 6 should use DMA channel 2, and only one such device should be active at a time.

A DMA operation that moves a block of data from an I/O device to a contiguous region of memory is called a DMA process. Once programmed, the DMA controller can complete a DMA process without software intervention. The controller executes a DMA process by performing one or more DMA transfers, each initiated by the I/O device. Although a DMA transfer can involve any number of bytes, single-byte transfers are generally used because they have the smallest impact on the dynamic memory refresh mechanism.

2.3.1.5 8288 Bus Controller and System Bus

The 8288 Bus Controller Chip decodes the S0-S2 (STATUS 0-2) lines from the CPU and generates the appropriate bus control signals as shown in Table 2-1. When a DMA cycle is in progress, the CPU gates the S lines high and the 8288 gates all its normal control lines OFF.

Table 2-1
Status Bit Decoding

STATUS INPUTS S2	S1	S0	CPU CYCLE	8288 COMMAND
0	0	0	INTERRUPT ACKNOWLEDGE	INTA
0	0	1	READ I/O PORT	IORC
0	1	0	WRITE I/O PORT	IOWC, AIOWC
0	1	1	HALT	NONE
1	0	0	INSTRUCTION FETCH	MRDC
1	0	1	READ MEMORY	MRDC
1	1	0	WRITE MEMORY	MWTC, AMWTC
1	1	1	PASSIVE	NONE

The System Bus is made up of 3 busses: the bidirectional system data bus, the 20 line system address bus, and the 30 line system control bus. During CPU operation, the addresses lines from the CPU are latched during T1 time of the bus cycle and for DMA cycles the latches are gated OFF by DMAAEN (DMA ACCESS ENABLE) active high.

The data transceivers are controlled by the Bus controller DEN (DATA ENABLE) and DT/R (DATA TRANSMIT/RECEIVE) signals. Memory cycles and I/O cycles both utilize the same control signals to the System Bus Transceivers. Included in the System Control Bus are the output lines from the 8288 Bus Controller, the DMA control lines, interrupt control lines, RDY lines, and the I/O & Memory Parity Error lines.

The Nonmaskable Interrupt Logic inputs are memory parity error (BADPARER) and I/O ERROR. These errors are considered fatal so they cannot be masked. Devices that can generate interrupts and the interrupt level for each device is listed below.

NONMASKABLE INTERRUPT	
SYSTEM BOARD RAM PARITY ERROR	The 8086 enables NMIs by writing to I/O port 1022H with D_0 set to one. The 8086 disables NMIs by writing to port 10E2H with D_0 cleared to zero.
OPTION BOARD I/O ERROR	Option boards assert the -I/O ERROR system bus line to request a NMI.

LEVEL 0 INTERRUPT FROM REALTIME CLOCK (Highest Priority)	
REALTIME CLOCK INTERRUPT	Set by channel 0 of the 8253-5 timer. Cleared by writing arbitrary data to port 10E0H.

LEVEL 1 INTERRUPT FROM 8235-5 TIMER	
SOFTWARE TIMER INTERRUPT	Set by terminal count signal from channel 2 of 8235-5 Timer. Cleared by reading port 10E2H.

LEVEL 1 INTERRUPTS FROM 2661 PROGRAMMABLE COMMUNICATIONS INTERFACE	
TRANSMITTER READY	Set when Transmit Data Holding Register is ready for 8086 to write new data into it. Cleared when 8086 writes to Transmit Data Holding Register or turns off transmitter.
RECEIVER READY	Set when Receive Data Holding Register contains data for the 8086 to read. Cleared when the 8086 reads Receive Data Holding Register or turns off receiver.
TRANSMITTER EMPTY OR DATA SET CHANGE	Set after transmitter serializes and sends last character loaded by the 8086 (Transmit Data Holding Register and Transmit Shift Register are both empty) or when either -DSR or -DCD changes state. Cleared when the 8086 reads EPCI Status Register.

LEVEL 1 INTERRUPT FROM PARALLEL I/O PORT	
DATA AVAILABLE	Set when Parallel I/O port has data for 8086 to read. Cleared when the 8086 reads a byte of parallel data from port 10EAH.
LATCHED ACKNOWLEDGE	Set by -ACKNLG signal from the parallel I/O interface. Cleared when the 8086 writes next byte to output port 10EAH or when the 8086 writes to output port 10ECH.
NOT BUSY	Set when the BUSY signal from the parallel printer goes inactive. Cleared when the 8086 reads input port 10ECH.

LEVEL 2 INTERRUPTS	
OPTION BOARD INTERRUPT	Set by a low level on -IRQ2 from the option board. Cleared by the 8086.
DMA TERMINAL COUNT (Channel 1, 2, or 3)	Set by the DMA Controller. Cleared by the 8086.
KEYBOARD TRANSMIT BUFFER REGISTER EMPTY	Set when the Keyboard Transmit Buffer Register is available to accept new data from the 8086. Cleared when the 8086 writes to Transmit Buffer Register or by the Clear Keyboard Transmit signal from the 8086.
KEYBOARD DATA RECEIVE	Set when the Keyboard has data ready for the 8086 to read. Cleared when the 8086 reads the Keyboard Receive Buffer Register.
FLOPPY DISK CONTROLLER CHIP INTERRUPT	Set when the NEC-765 device completes a floppy disk operation. Cleared by reading the first status byte in the result phase of the floppy disk operation.
FLOPPY DISK DRIVE 1 OR DRIVE 2 DOOR DISTURBED	Set by opening the door on Floppy Drive 1 or 2. (System Status Port 10E0H determines which door is open). Cleared by setting bit 2 (drive 1) or bit 3 (drive 2) of output port 1000H.
8087 INTERRUPT	Set by the 8087 to indicate that an unmasked exception occurred during a numeric instruction execution while the 8087 interrupts were enabled. Enabled, disabled, and cleared by 8086 instructions FNCLEX, FNSAVE, and FNINT.

2.3.2 SYSTEM BOARD THEORY

For the following discussion refer to the block diagram Figure 2-5.

2.3.2.1 System Bus Buffering

System Bus Double Buffering and Memory is the portion of the System Board that contains the Slot 0 I/O devices. All option boards have their own system bus buffers to protect the bus from failures on any option board and the same holds true for the I/O on the System Board.

On the System board, the address and data busses are double buffered although the System Control bus is not. This is because most of the system's control lines originate on the System Board .

2.3.2.2 RAM Control Logic And Address Mux

The RAM Control Logic and Address Mux interface the 128K bytes of DRAM arranged in 2 banks of nine 4864 chips each. These are dynamic RAMs requiring refresh and are organized 64K bits x 1 bit with eight bits of RAS/CAS addressing connected. Refer to Figure 2-3 for Memory Mapped Addressing. The COLEN signal controls the address Mux and is active when CAS is true to Mux the MSB eight address lines to the selected RAM bank. When RAS is active and CAS is inactive, the eight LSB address lines are muxed to the selected RAM bank as the ROW address. When both RAM banks are selected, a WORD transfer occurs. When the upper bank or lower bank is selected separately a byte transfer occurs. Address line A0 is not muxed to memory, but is used with BHE from the CPU to select WORD or upper or lower byte.

Address lines A17, A18, and A19 are not required for the lower 128K (basic) of RAM but are used on the Video Controller and Expanded Memory option PCBs.

The ninth memory bit is parity. The Parity Generator/Check logic generates this bit during a memory write bus cycle and checks it on a memory read bus cycle. When a parity error occurs, the BADPARER output signal is activated generating a NMI interrupt to be sent to the CPU.

2.3.2.3 I/O Chip Select Decode and 'SAD'

The 8086 uses both the System Address Bus and the Data Bus for I/O commands. When an I/O read or I/O write instruction is executed by the CPU, the 8288 Bus Controller will gate IOWC (AIOWC) or IORC active to disable memory and to enable an I/O command decoder on the System Board or on an option board. The LSB 16 address lines along with IORC or AIOWC are connected to these decoders so the bit configuration of the buffered address lines specifies the command. Address 1000-10FE are assigned to the System Board for a total of 128 commands as only word (even) addresses are used. Refer to Figure 2-4 for the I/O Mapped Addressing.

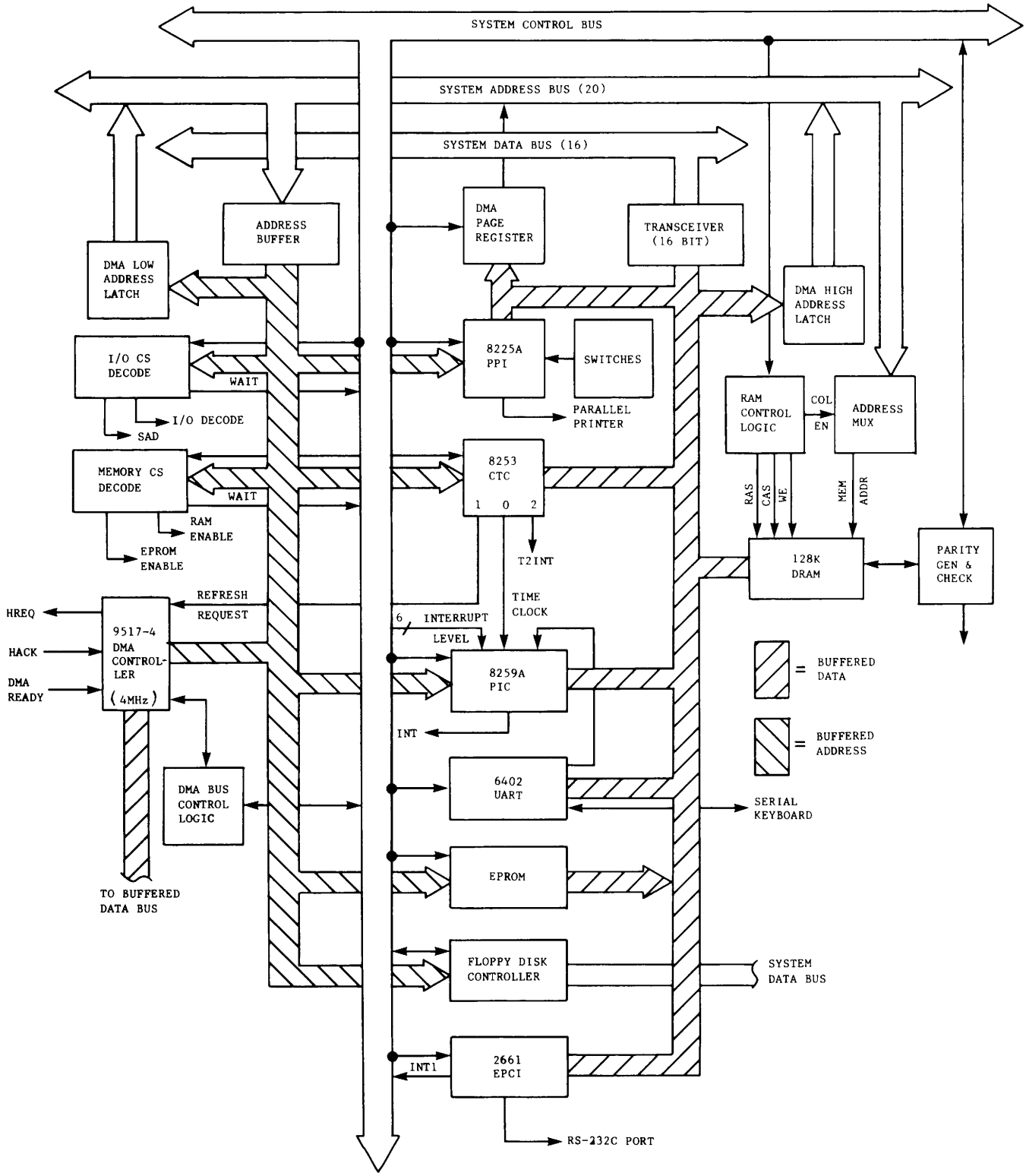
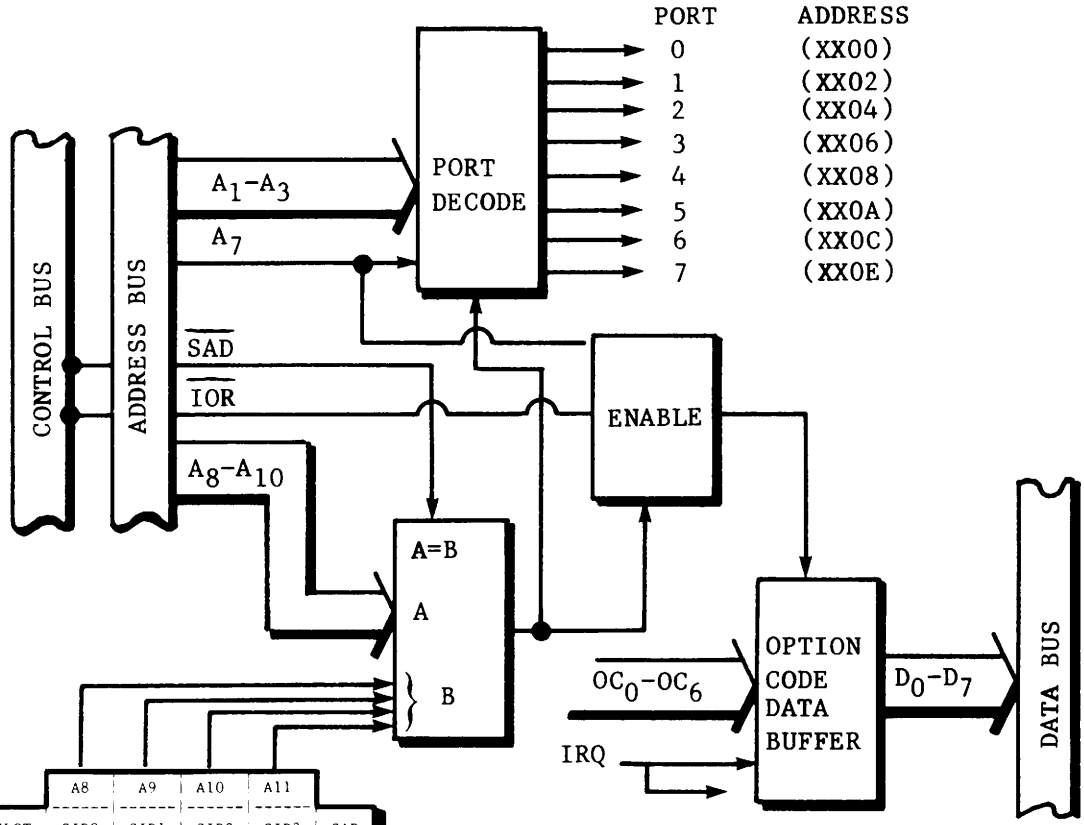


Figure 2-5. System Board Block Diagram

The System Data Bus will contain the data transferred to or from the selected I/O device (by the command decode). Not all commands such as 'CLR, RT, INT' require a data transfer.

A unique design has been built into this system to eliminate the need for switch selectable options. See Figure 2-5. The Motherboard connectors for each one of the five option slots are each wired for a different 4 bit slot address. This permits any option board to be placed in any one of the 5 slots. On system start-up, the CPU reads each slot with 10FE -15FE commands and the board inserted into the slot returns its specific hardwired ID on the data bus. If no board is installed in a slot, all ones are returned on the data bus to the CPU. The Slot Address Decode signal (SAD), is generated by a command decode on the System board and is routed to all the option slots.



I/D ADDR	I/O ADDR	SLOT	A8 SID0	A9 SID1	A10 SID2	A11 SID3	SAD
10FE	10XX	0	0	0	0	0	0
11FE	11XX	1	1	0	0	0	0
12FE	12XX	2	0	1	0	0	0
13FE	13XX	3	1	1	1	0	0
14FE	14XX	4	0	0	1	1	0
15FE	15XX	5	1	0	1	1	0
16FE	16XX	6	0	1	0	1	0
17FE	17XX	7	1	1	0	1	0
18FE	18XX	8	0	0	0	0	1
19FE	19XX	9	1	0	1	0	1
1AFE	1AXX	10	0	1	1	0	1
1BFE	1BXX	11	1	1	1	0	1
1CFE	1CXX	12	0	0	0	1	1
1DFE	1DXX	13	1	0	0	1	1
1EFE	1EXX	14	0	1	0	1	1
1FFE	1FXX	15	1	1	1	1	1

Figure 2-6. Slot Decode Block Diagram

Address lines A8 - A11 must equal the slot decode (0001-0101) and A4-A7 must be all ones. If an I/O write to 1x7E is executed, the options for the board will be loaded with the data bus bits configured for the option desired, such as TV mode or Video Monitor mode on the Low Resolution Controller Board. Table 2-2 identifies the I/O Option Codes.

Table 2-2. I/O Identification Codes

CIRCUIT BOARD	ID CODE
Empty Slot	FFH
CPU Board With Floppy Disk Controller	00H
Winchester Disk Controller	01H
Low Resolution Video Controller	10H
Medium Resolution Video Controller (Character Board Only)	11H
High Resolution Video Controller	13H
Medium Resolution Video Controller (Graphics Board)	14H
Medium Resolution Video Controller (Character Board with attached Graphics Board)	15H
RS-232/ACU Remote Telecommunication Controller	1CH
X.21 Remote Telecommunication Controller	1EH
Local Communications (928)	38H
Z80 CPU (CP/M-80)	39H
Extended Memory Board	3FH

2.3.2.4 9517A DMA Controller

The 9517A DMA Controller is a four channel programmable DMA controller with bus control outputs. Each channel has an internal 16 bit address register and a 16-bit byte count register. These registers are program loaded and commanded to increment or decrement as desired. An external 4-bit x 4 channel DMA page address register extends the DMA address capability to the full 20 bits. Any channel word register will generate a TC interrupt to the CPU when incremented to all ones or decremented through Zero to all ones. This allows a maximum of 64K Byte transfers per channel. At this time, the word register and address register for that channel will be automatically reinitialized to the original bit configuration if originally programmed to do so, or can be reloaded by the program as desired. The 4 channels are prioritized with channel 0 having the highest priority. Channel 4 (lowest priority) is used for RAM refresh.

2.3.2.5 8253-5 Programmable Interval Timer

The 8253-5 Programmable Interval Timer chip contains three identical and independent channels, each of which can operate as a realtime clock that generates a periodic interrupt request.

Each channel consists of a Control Register, a 16-bit down counter and two interface signals: a clock input, which decrements the counter, and an output for the channel to assert when its counter reaches zero. The clock input runs at 500 KHz for channels 0 and 2. Channel 1 clock input is a 2 MHz clock. Although the 8253-5 timer chip can operate in six different modes, only two are supported: mode 2, the "rate generator" mode, and mode 4, the "software triggered strobe" mode.

Timer channel 0 is used as a realtime clock and must be programmed to operate in mode 2. Writing to I/O port 1040H loads the channel 0 counter with an initial value that designates the number of clock pulses between output pulses. Channel 0 counts clock pulses, beginning with the next pulse immediately after the counter is loaded. It decrements its counter on the falling edge of each clock pulse. When the counter reaches zero, it generates a level 0 interrupt request, resets the counter, and immediately begins counting clock pulses for a new timing cycle. It is not necessary to reload the channel 0 counter between cycles. If a new value is loaded into the counter, it has no effect until after channel 0 generates its next interrupt request at the end of the current timing cycle. Since timer channel 0 is the only possible source of level 0 interrupt requests, it has no interrupt status flag. The 8086 clears a channel 0 timer interrupt by writing arbitrary data to I/O port 10E0H.

Timer channel 1 is reserved for timing the interval between dynamic memory refresh bursts. Like channel 0, timer channel 1 operates only in mode 2. Channel 1 generates DMA requests, not interrupt requests. Its counter must be loaded by writing a count of 60 (3CH) to I/O port 1042H.

Channel 2 is available for use as a general purpose timer that generates periodic level 2 interrupt requests. It operates in either mode 2 or mode 4. Mode 4 operation is nearly identical to mode 2 operation, but lacks the automatic reset offered in mode 2.

Only one interrupt request is generated in mode 4, and the counter must be reloaded to initiate a new channel 2 timing cycle. Channel 2 generates interrupt requests at priority level 2. Bit 0 of the Interrupt Status Port (I/O port 1022H) signals a timer channel 2 interrupt request. The 8086 loads or reads the channel 2 counter at I/O port 1044H. It clears an interrupt request from channel 2 of the timer by reading I/O port 10E2H.

To begin counting on any timer channel, a program first initializes the channel's Control Register by writing one byte to output port 1046H. A Control Register byte selects a channel (0-2), a mode of operation (2 or 4), a counter data format (binary or binary coded decimal), and the number of bytes required to specify an initial counter value (1 or 2). Software then loads the counter by writing one or two bytes to the 8-bit counter port dedicated to the channel that was selected: port 1040H for channel 0, port 1042H for channel 1, or port 1044H for channel 2.

The channel 1 output of the 8253 CTC chip initiates a Channel 0 DMA request every 120 usecs. When the request is granted by the CPU, 8 x 512 (4096) word locations in memory will be refreshed. This results in all of memory being refreshed in 1.92 ms, which is within the 2 ms specification.

The other 3 DMA channels are operated single byte instead of block mode due to the memory refresh requirement. Channel 0 only does 8 memory transfers at a time, which really is not a true block operation. Floppy disk transfers use DMA channel 2 and the other two channels (1 and 3) are available for the RTC, Winchester, or CP/M-80 option boards. The Low and Medium Resolution Controllers cannot utilize DMA as their memory is memory mapped as part of main memory and requires word access rather than byte access.

2.3.2.6 8259A Programmable Interrupt Controller

The 8259A PIC handles 8 levels of input interrupt requests and is programmable. Refer to Table 2-3. Level 0 has the highest priority and level 7 the lowest. Any or all levels can be masked or unmasked at any time by the program. The chip's input control words must be loaded at program start-up. The control words establish how the chip will operate, loads the 5 MSB bits of the 8-bit vector address, and initializes the chip. The 3 LSB bits of the vector address are automatically set to equal the level of the interrupt being serviced when an interrupt occurs.

Table 2-3. Interrupt Request Flag Addresses

INTERRUPT LEVEL AND TYPE		INTERRUPT REQUEST FLAG
NMI	System Board Parity Error	Port 10E0H bit 0 = 0
	Option Board I/O Error	Port 10E0H bit 1 = 0
Level 0	Realtime Clock (Timer Channel 0)	Only Possible Source
Level 1	Timer Channel 2	Port 1022H bit 0 = 0
	Serial Communications Interface	Port 1022H bit 1 = 0
	Parallel I/O Interface	Port 1022H bit 2 = 0
Level 2	DMA End of Process (Terminal Count)	Port 1022H bit 3 = 0
	Output to Keyboard	Port 1022H bit 4 = 1
	Input From Keyboard	Port 1022H bit 5 = 1
	Floppy Disk Operation Finished	Port 10E0H bit 3 = 1
	Floppy Disk Controller Error	Port 1022H bit 6 = 1
	Floppy Disk Door Status	Port 10E0H bits 4-7 = 1
	8087 Co-Processor	Port 1022H bit 7 = 1
	Option Board Interrupt	Slot Offset 10FEH bit 7 = 1
Level 3-6	Option Board Interrupt	Slot Offset 10FEH bit 7 = 1

2.3.2.7 6402 UART

The 6402 UART chip is the keyboard interface. The 6402 UART receives and transmits a serial 11-bit byte to and from the keyboard at 62.5 K baud. The 11 bits are made up of 1 start bit, an 8-bit data byte, and 2 stop bits.

When a keyboard key is depressed, the microprocessor on the keyboard converts the 8-bit keycode (identifying the key) from parallel to serial, adds the start bit and stop bits, and transmits it to the 6402 chip. The 6402 strips the start bit and stop bits, convert the serial data back to parallel data, and interrupts the 8086 CPU with a level 2 interrupt.

2.3.2.8 2661 Extended Programmable Communication Interface

The 2661 Extended Programmable Communication Interface (EPCI) is programmed by the 8086 to support RS-232C asynchronous serial data communication in full duplex or half duplex mode. The 2661 EPCI features 5-bit to 8-bit characters; 1, 1.5, or 2 stop bits; odd, even, or no parity; overrun, parity, and framing error detection; line break detection and generation; false start bit detection; automatic serial echo mode; and local or remote loopback operation for diagnostics. The EPCI contains an internal baud rate generator that can be programmed to produce internal transmit and receive clocks. It operates at 16 commonly used rates, ranging from 75 to 19,200 baud as shown in Table 2-4.

Table 2-4. 2661 EPCI Mode Register 2

BIT	VALUE	MEANING	VALUE	MEANING	VALUE	MEANING
3,2,1,0	0000	**	0101	300 Baud	1010	2400 Baud
	0001	75 Baud	0110	600 Baud	1011	3600 Baud
	0010	110 Baud	0111	1200 Baud	1100	4800 Baud
	0011	134.5 Baud	1000	1800 Baud	1101	7200 Baud
	0100	150 Baud	1001	2000 Baud	1110	9600 Baud
					1111	19200 Baud
4	Set to one denotes use internal receiver clock, set to zero denotes use external receiver clock.					
5	Set to one denotes use internal transmitter clock, set to zero denotes use external transmitter clock.					
7, 6	Unassigned.					

** Denotes loop on Power-Up diagnostics. Refer to paragraph 4.13.3.

The EPCI contains a transmitter and a receiver that operate independently. The transmitter accepts parallel data from the 8086, converts the data into a serial bit stream, inserts any additional bits required by the programmed communication technique, and generates a composite serial data stream on its output line. The receiver accepts serial data from the RS-232C interface, converts it to parallel format, strips off bits that implement the communication technique, and sends an assembled data character to the 8086.

The EPCI receiver performs the following operations. When the EPCI's Data Carrier Detect (-DCD, pin 8) input from the RS-232C interface is low and the Receive Enable bit of the Command Register (RxEN, bit 2) is high, the receiver begins accepting data by seeking the high to low transition of a start bit on its Receive Data (RxD) input line. After detecting a start bit transition, the receiver again samples the RxD line one-half bit time later. If RxD is now high, it continues seeking a start bit; otherwise, it has found the start bit and can now begin to sample the input line, one bit at a time, until it has assembled the proper number of data bits, a parity bit, and one or more stop bits. It then transfers the data to its Receive Data Holding Register, sets the Receive Ready bit (RxRDY) in the Status Register, and asserts its -RxRDY output line, causing a level 1 interrupt. The 8086 can now read the character at I/O port 1080H.

The receiver zeros unused high-order bits of the incoming character code and loads the Parity Error, Framing Error, and Overrun Error bits in the Status Register. When it detects that the line was low for the entire character (including stop bits), the receiver signals a line break by transferring one character with code 0 into the Receive Data Holding Register and setting the Framing Error bit in the Status Register. Following a line break, the RxD input line must return high before the receiver will begin searching for the next start bit.

The EPCI transmitter performs the following operations. When the EPCI's Clear to Send (-CTS, pin 5) input is low and the Transmit Enable flag (TxEN, bit 0) is set in the Command Register, the transmitter indicates to the 8086 that it can begin accepting data by setting the Transmit Ready bit (TxRDY, bit 0) in the Status Register and asserting its Transmit Ready output (-TxRDY), which causes a level 1 interrupt. Then, when the 8086 writes a character into its Transmit Data Holding Register via I/O port 1088H, the transmitter reverses both of these conditions, clearing -TxRDY. As soon as its Transmit Shift Register becomes free, the transmitter transfers the data character out of its Transmit Data Holding Register and again asserts -TxRDY thereby providing one full character of output buffering.

After automatically sending a start bit, the transmitter sends the proper number of data bits, beginning with the least significant bit, and appends an optional parity bit plus the proper number of stop bits. Then, if a new character is not yet available in the Transmit Data Holding Register, it keeps its TxD output line high, sets the TxEMT/DSCHG bit in its Status Register, and asserts its TxEMT/DSCHG output, generating a level 1 interrupt. Transmission resumes when the 8086 loads a new character into the Transmit Data Holding Register. Setting the Force Break flag (bit 3 of the Command Register) high forces a continuous low (ie, a line break) at the transmitter output.

Four 8-bit registers program the communication interface. Two Mode Registers establish the baud rate, parity, character format, and related parameters. A Command Register enables various communication options and a Status Register reports the detailed state of the communications channel.

An 8086 program writes data into the Mode Registers and Command Registers. The 8086 then transfers data to and from the 2661 EPCI while monitoring its status register. The I/O port assignments are addresses 1080-108E and are listed in Table 2-5.

Table 2-5. EPCI I/O PORT ASSIGNMENTS

Port	Address
Read Receive Holding Register	1080H
Read Status Register	1082H
Read Mode Registers 1 and 2	1084H
Read Command Register	1086H
Write Transmit Holding Register	1088H
Write SYN1, SYN2, and DLE registers (unused)	108AH
Write Mode Registers 1 and 2	108CH
Write Command Register	108EH

The RS-232C interface requires one 25-pin, "D" shell, male connector. The following table lists the RS-232C interface signals, their direction as seen by the EPCI, and their pin assignment on the interface cable. Note that the RS-232C connector pins 1, 9-19, and 21-25 are no connect.

Table 2-6. RS-232C Connector Pin Designation

Signal	I/O	Pin	Description
±0V		7	Signal ground and common return
TxD	O	2	Transmit Data
RxD	I	3	Receive Data
-RTS	O	4	Request to Send
-CTS	I	5	Clear to Send
-DSR	I	6	Data Set Ready
-DTR	O	20	Data Terminal Ready
-DCD	I	8	Data Carrier Detect
Pins 1, 9-19, and 21-25 are no connect.			

A dash (-) preceding the Mnemonic code denotes a low-active signal.

2.3.2.9 Floppy Disk Controller

The NEC 765 is an LSI Floppy Disk Controller (FDC) Chip, that operates one or two 5.25 inch, double-sided, double density, floppy disk drives at 360 KBytes of usable data per drive. Modified Frequency Modulation (MFM) or double density recording is used. Handshaking signals are provided in the 765 to make DMA operation possible with the aid of an DMA controller chip, the 9517A. Data transfers between the controller and main memory are facilitated by DMA requests from the disk controller. The 765 is capable of performing 15 different commands. These commands are listed in Table 2-7. Each command is initiated by a multi-byte transfer from the CPU and the result, (after execution of the command) may be a multi-byte transfer back to the CPU. Because of this multi-byte interchange, it is convenient to think of 765 operation as consisting of three phases.

Command Phase
Execution Phase
Result Phase

Software accesses three 8-bit registers in the FDC. Before a command is executed, the CPU writes a command byte sequence to the FDC Command Register at port 1016. This differs from 1-to-9 bytes depending on the command. After a command is completed or terminated abnormally, the CPU reads up to 7 bytes of Status from the FDC Operation Status Register also at port 1016H.

Table 2-7. Floppy Disk Controller Commands

Read Deleted Data	Read Data	Seek
Sense Drive Status	Specify	Read ID
Write Deleted Track	Write Data	Scan Equal
Sense Interrupt Status	Recalibrate	Scan High/Equal
Format a Track	Read A Track	Scan Low/Equal

The third register is the Controller Status Register. Unlike the OP Status Register which must be read after most disk operations, the Controller Status Register (also called Main Status Register) may be read at any time by reading port 1014H. The software must read this status byte before transfer of each byte during the command phase and during the result phase.

During the command phase and the result phase, the program must check the Main Status Register before transferring each byte of up to 9 bytes in either direction. During the execution phase of a surface operation, the FDC generates a channel 2 DMA request (DREQ2) whenever it needs a byte of data or has a data-byte available. The DMA Controller responds with a DMA Acknowledge (DACK) signal and a read or a write signal, depending on the direction. When the DMA Controller indicates terminal count (TC) (or the software does with a write to port 101C) the 765 will generate a level 2 interrupt to the CPU to inform the software that the command phase is complete and the result phase is starting. Reading the first byte of the result phase automatically resets the interrupt request.

Most FDC commands return seven bytes of data during the result phase. These seven bytes are:

3 bytes of auxiliary status information
4 bytes of disk address data.

The 15 FDC operations are made up of 3 command groups. Each group has a different number of bytes in the command and in the result sequence. Nine commands use a standard 9-byte command sequence and a 7-byte result sequence. The disk formatting operation uses a unique command sequence and the standard result format. The other 6 commands have unique command and result formats.

The first byte of the 9-byte sequence specifies the operation to be performed as well as the recording format. For some commands, this byte also specifies that the "skip option" is allowed and whether both tracks of the addressed cylinder (both sides) will be accessed. Byte 2 indicates which side is to be accessed and bytes 3, 4, and 5 supply the track side (which must agree with the 2nd byte) and sector number. Bytes 6-9 are used to select the number of sectors per track as well as the number of bytes per sector. The PC uses 512 byte sector selection which is 9 sectors per track with 512 bytes per sector.

2.3.2.10 8255-5 Parallel Peripheral Interface (PPI)

The 8255A Parallel Peripheral Interface (PPI) Chip is used for the printer interface. The 8255-5 contains three 8-bit ports. Two of the ports are used for the printer interface and one port is used to interface the cause of the level 1 and level 2 interrupts to the CPU with a read to port 1022H. Two of the ports, the interrupt port and the printer status port are read-only ports while the third port is a read and write port. In addition, a four-position BAUD Rate DIP switch (for Async communications) located on the CPU board, is hooked to this port and is read by the system software. These four switches are used as a baud rate default upon power-up. Any required changes of the baud rate after power-up may be selected via commands from the keyboard. The Baud Rate Switch Location and Baud rate select table is shown in Chapter 4 paragraph 4.7.1. The Parallel Port (J2) pin assignments are shown below.

Table 2-8. Parallel Port Pin Assignment

PIN #	SIGNAL	I/O	PIN #	SIGNAL	I/O
1	-DSTB IN	O	12	PE	I
2	DATA 1	I/O	13	SLCT	I
3	DATA 2	I/O	14	USR0/AUTO FEED XT	O
4	DATA 3	I/O	15	-POWER ON/OSCXT	I
5	DATA 4	I/O	18	-SMART/5 V	I
6	DATA 5	I/O	31	-RESET	O
7	DATA 6	I/O	32	-FAULT	I
8	DATA 7	I/O	34	-DSTB OUT	O
9	DATA 8	I/O	35	-DAV	I
10	-AKNLDG	I	36	USR1	O
11	BUSY	I			
Pins 16, 17, 19-30, 33 are tied to ground					

2.3.2.11 Power-Up EPROMS

Two EPROMs contain the Power-up Diagnostics and the Bootstrap instructions for the IPL. Every time the system is powered-up, the system will run the B.I.T diagnostics. Once the Diagnostics are completed, the 8086 CPU will issue the address for the IPL. The EPROM will issue the microcode when Chip Enable (CE) is active low and Output Enable (OE) is active low.

2.4 SPS200 SWITCHING POWER SUPPLY

The SPS200 Switching Power supply is capable of outputting four supply voltages +5, -5, +12, and -12 volts dc. The power supply input circuit converts the ac line voltage (115/230 vac) into rectified and filtered high voltage dc. The high voltage dc is chopped at a frequency of 25 KHz by a pulse width modulator presenting high voltage pulsating dc to a multiple output transformer. This transformer steps down the high voltage pulsating dc while isolating the ac supply line from the low voltage dc outputs.

One output voltage is feed back to the pulse width modulator to establish a feedback voltage used to regulate the ON/OFF relationship of the pulse width modulator with respect to the voltage level source. This feedback voltage becomes the regulating voltage with all other voltages remaining secondary.

The power supply ac input is applied to an EMI filter (ElectroMagnetic Interference) to reduce the EMI per rules set by the F.C.C. This ac source is then routed to the 115/230V select switch. The ac input (if 115V) is applied to the Fan and to the ac transformer. If the ac input is 230V, the ac is first input to a Full-wave bridge rectifier circuit then to the fan and the ac transformer. All output voltages are full-wave rectified through their associated diode rectifier circuit. The power-on signal (WOLFTRAP) is an output of a comparator circuit that forward-biases a NPN transistor once the output voltages are stabilized.

2.5 8237 MOTHERBOARD

The 8237 Motherboard is a compact board that fits vertically against the side of the SPS-200 power supply. Located at the top of the board are the power supply connectors (J1, J2, and J3), a noise filter, a despiking network for the Bus Control signals and the two system clocks. The system bus provides 16 bidirectional data lines, 20 address lines, and various control signal lines. Interrupt request lines implement six levels of priority interrupt and one nonmaskable "error" interrupt. The bus also contains the power lines providing the four voltage levels required by the option boards.

The Motherboard provides a common bus for all the fore mentioned signals plus provides a unique feature for slot decoding. Pins 81, 82, 83, and 84 of each of the five option board connectors are wired differently to provide the slot ID codes via the board that is plugged into the slot. The expansion slot decoding scheme was discussed in paragraph 2.3.2.3. The five option slots are prioritized with Slot 5 (J9) being the highest and Slot 1 (J5) being the Lowest. The Motherboard pin assignment for the option board expansion slots is shown in Table 2-9.

Table 2-9: SYSTEM BUS PIN ASSIGNMENTS (Expansion Slots Only)

Pin	Signal	Pin	Signal	Pin	Signal
1	GND	30	A13	59	D10
2	GND	31	A14	60	D11
3	CLK (8 MHz)	32	A15	61	D12
4	-RESET	33	A16	62	D13
5	-5 V	34	A17	63	D14
6	-IRQ2	35	A18	64	D15
7	-IRQ3	36	A19	65	WTR
8	-IRQ4	37	-BHE	66	HACK
9	-IRQ5	38	GND (monitor	67	-I/O ERROR
10	-IRQ6	39	GND power)	68	ADDSTB
11	-IRQ7	40	-DACK0	69	T/C
12	-AIOWC	41	-DACK1	70	RDY
13	-IORC	42	-DACK2	71	-SAD
14	-AMWC	43	-DACK3	72	MCE
15	-MRDC	44	-DREQ1	73	+12V (monitor
16	ALE	45	-DREQ2	74	+12V power)
17	A0	46	-DREQ3	75	-12 V
18	A1	47	DEN	76	+12V
19	A2	48	DT/R	77	4CLK
20	A3	49	D0	78	+5V
21	A4	50	D1	79	+5V
22	A5	51	D2	80	+5V
23	A6	52	D3	81	SID0
24	A7	53	D4	82	SID1
25	A8	54	D5	83	SID2
26	A9	55	D6	84	SID3
27	A10	56	D7	85	GND
28	A11	57	D8	86	GND
29	A12	58	D9		

NOTE: A dash (-) preceding the signal name denotes low-active signals.

2.6 360K BYTE FLOPPY DRIVE

The theory of operation for the Tandon and MPI Floppy Drives is not discussed in this manual. Information pertaining to the operation of these drive is contained in the CE Reprint version of the vendor technical manual. Refer to Chapter 1 Table 1-3 for available CE documentation.

2.7 MEDIUM RESOLUTION CHARACTER GENERATOR PCB (8243/8343)

For the following discussion, refer to the block diagram in Figure 2-7. The schematics pertaining to this board are WLI 210-8243/8343 (5 sheets). No callouts or references are made to the schematics as the theory of operation is only to the block diagram level.

2.7.1 Medium Resolution Board Overview

The medium resolution video controller produces TTL output to drive a Wang monochrome video monitor. Running at 18.824 KHz horizontally and 60 Hz vertically, the controller has 800 pixel by 300 pixel resolution when displaying either text characters or bitmapped dot graphics. (Bitmapped dot graphics is available when the Graphics Option board is paired with the Medium Resolution board.)

Partitioned into a standard matrix containing 25 rows of 80 columns each, the medium resolution display positions characters or arbitrary symbols, defined by software, within a 10 pixel by 12 pixel character cell. A cursor can be positioned over any character cell. Although cursor size and shape are programmable, the cursor normally occupies all 20 pixels in the lower two rows of a character cell. It can be programmed to blink at either of two repetition rates. Between blink cycles, during the cursor's off time, the overlaid portion of the character appears just as though no cursor were present. The cursor can occupy only one character cell at a time.

A programmable underscore occupies all 10 pixels in the bottom row of a character cell, when designated by software, and a programmable overscore fills all ten pixels in the top row. Software can assign underscore and overscore attributes to any combination of characters in a display. When adjacent characters are underscored, the underscore portions of their displays form a continuous horizontal line under all of the underscored characters. (This also occurs with adjacent overscored characters.)

Hardware subscript and superscript capabilities modify the normal appearance of a symbol or character. As with underscore and overscore, multiple characters can be subscripted or superscripted in any combination. Subscripting a character rolls the character one scan line downward within its character cell. Superscripting rolls the character cell display two scan lines upward. Wraparound does not occur.

Instead, if a character normally has pixels set in the bottom row of its cell, those pixels roll off the bottom of the cell and disappear when the character is subscripted; if a character has pixels defined in the top two rows of its display, those pixels disappear when the character is superscripted.

A font table associates every possible character code (byte) with the arbitrary character cell display pattern that is assigned to the character code. The 4k bit by 10 bit font table is downloaded from the 8086 to define up to 256 different characters or symbols. It establishes each of the 120 pixels in a 10- by 12-pixel character cell to support true lower case descenders, accent marks, foreign language fonts, and arbitrary graphic symbols. Like all other memory on the medium resolution video controller, font table locations must be word addressed at even memory locations.

The 8086 can update any part of the font table at any time, allowing flicker-free operation without constraints on font table access, and it can read the font table as well as write it. The font table is mapped to addresses F2000-4000H in the video memory address space. The font table is word addressed, and it contains 256 16-word entries. Its Nth entry defines the shape of the character with character code N. The word at the lowest address of a font table entry defines the top scan line in a subscripted character display. Successively higher addresses determine successively lower scan lines until the fifteenth word in an entry, which defines the bottom line in a superscripted character display. The sixteenth word at the highest font table entry address is not used.

Because subscripting shifts a character one scan line downward and superscripting shifts it two scan lines upward, a character actually consists of 15 pixel rows, only 12 of which are visible within its 12 pixel high character cell "window". For example, the character cell display for a subscripted character shows the top 12 rows of that character's complete font table definition. Canceling the subscript produces a normal character display; the character appears to roll upward by one scan line within its character cell window, raising the top row of pixels out of view and shifting in a thirteenth row at the bottom. Superscripting this same character shifts two more rows of pixels upward and out of the character cell window while shifting two new rows--the fourteenth and fifteenth--in from the bottom. At any time, only 12 of the 15 pixel rows in a font table entry are visible on the display. The middle nine rows are always visible, but subscripting and superscripting shifts them up and down between the top and the bottom of the character cell window.

Within its font table entry, a character is defined "upside down" and in its subscripted position. That is, the first (lowest) row of the 16-row font table entry defines the horizontal strip of pixels that will appear at the top of the character cell when the character is subscripted. The second row of the entry defines the row of pixels that will appear at the top when the character is displayed normally. The fourth row defines the row that will be on top of a superscripted display. The twelfth row will occupy the bottom of a subscripted display. Normal display rolls the thirteenth row of the font table entry up to the bottom of the character cell window, while superscripting shifts in the fourteenth and fifteenth rows. The sixteenth row of each font table entry is not used and cannot be displayed. Pixels defined by high order bits of each word in a font table entry are displayed to the left of pixels defined by low-order bits.

Up to 2000 characters of visible text reside in a 2k-word frame buffer formatted with character codes in the high-order bytes and character attribute bits in the low-order bytes. Frame buffer memory is mapped from F0000H (top left corner of display) to F0FFEH (bottom right corner of display) in the video memory address space. Since each word of the frame buffer corresponds to a particular 10- by 12-pixel character cell on the screen, the 8086 can change any display character simply by writing a new 16-bit code to the appropriate frame buffer address.

To create a character display, the video memory controller scans the first 2000 words in the frame buffer and uses each character code entered into the frame buffer as the address of a font table entry. The font table data determines the shape that will appear by defining the pattern of pixels assigned to the character code. For example, if the word at frame buffer address F0794H contains character code 0FH in its high-order byte, the controller paints the pixel pattern defined in the sixteenth font table entry into the tenth character cell on the thirteenth line of the display.

Frame buffer entries must be word addressed at even locations. Frame buffer memory access does not affect the CRT display, allowing flicker-free operation without constraints on frame buffer updating. The 8086 can read the frame buffer to determine what characters are present on the display screen. Characters of text can be interspersed with graphics information on the screen; however, text and graphics are ORed together before being displayed and, therefore, each pixel must be allocated to text or to graphics, but not both.

Eight character attributes can be selected individually or in combination to modify the normal appearance of a character. Attributes have no effect on graphics. They are selected on a per-character basis by setting specific bits in the low-order byte of the frame buffer entry. The following table lists the character attributes and their bit assignments. Combinations of attributes can be used to represent different character display modes, or fonts, on the screen.

Normal	Reverse
Bold	Reverse bold
Underscore	Reverse underscore
Bold underscore	Reverse bold underscore

Video controller hardware supports all of the 256 possible combinations of attributes; some combinations, however, lead to inconsistencies or conflicts that can detract from their use. If a character has the bold, reverse, and blink attributes, for example, the cursor will not be visible when it is positioned on that character. The cursor generally covers only background pixels in a character cell. In this instance, the cursor and the character's background both appear as high intensity, blinking dots, and one might be indistinguishable from the other.

The bold, blank, reverse, and blink attributes modify the way in which a character's font table entry (along with its underscore or overscore attributes) appears on the screen. In contrast, superscript and subscript attributes determine which portion of the font table entry appears. A pixel pattern displayed on the screen is jogged one scan line downward to create a subscripted character, or up two lines for a superscript.

The subscript attribute shifts a character one scan line downward within its character cell and the superscript attribute shifts the character two scan lines upward. If both the subscript attribute and the superscript attribute are selected, the character will be shifted one scan line upward. This combination of attributes generally is not used.

2.7.2 Functional Theory of Operation

For The Function Theory of Operation refer to Block Diagram Figure 2-7.

The 20 bit System Address bus is buffered on-board with 12 bits (BA1-BA12) being presented to the Address Mux circuitry for generation of the Attribute Memory addresses and Character Memory addresses. These same 12 address bits are presented to the Address Mux circuitry for generation of the Font memory addresses.

System Address bits 13-16 (BA13-BA16) are presented to a 3 to 8 decoder for the generation of control signals -FONT and -FRAME. Addresses 17-19 are used to denote Bitmapped memory as well as enabling the 3 to 8 decoder for -FONT and -FRAME signal generation.

The Data Transceiver logic controls the direction of the data bus as well as providing a Data Buffer for the 16 system data lines. Eight buffered data lines (Low-order bits BD0-BD7) are presented to the CRT Controller device.

The Motorola 6845 CRT Controller device (CRTC) performs the interface between 8086 CPU and the CRT display. The CRTC device generates the signals required to interface the digital system logic to a raster scan CRT display. The CRTC device provides the horizontal sync, vertical sync, and display enable signals. The timing required for the CRTC device is produced on-board via a 19.2 MHz crystal divided down to supply a 1 MHz clock rate.

The CRTC device provides the CRT refresh addresses to the frame (character) and attribute 2K Bytes of memory. The refresh address is muxed with the system address bus by a split cycle timing signal, CPU/CRT. The characters displayed on the CRT are loaded into the frame memory by the system software along with the attributes for each character location. That is, both the frame and attribute memories are word addressed together and the LSB byte is loaded into the attribute memory as the MSB byte is loaded into the frame memory.

During the CRT refresh half of the split cycle timing, the character to be displayed is read out of the frame memory and muxed, along with the character row count output of the 6845 Controller, to form a 12-bit address to the 4K x 10-bit Font Memory. At the same time, the attribute byte is read out of the attribute memory to the attribute logic. The attributes offered are Blink, Reverse Video, Blank, Bold, Underscore, Overscore, Superscript, and Subscript.

Since the attribute memory shadows frame memory, any one or combinations of these attributes are available to the programmer for every character location on the CRT. The 4K x 10-bit FONT memory contains the actual dots required to form the characters displayed on the screen. The FONT memory can be considered as a programmable character generator and must be loaded by the system software before anything can be displayed on the screen. This allows any language or character set to be displayed. The 10 bits read out of the FONT memory are loaded into a shift register by the SH/LD pulse going low, then they are shifted out serially, mixed with the attributes and cursor to form the video. All memory chips on this board are static memory devices so chip refresh is not required.

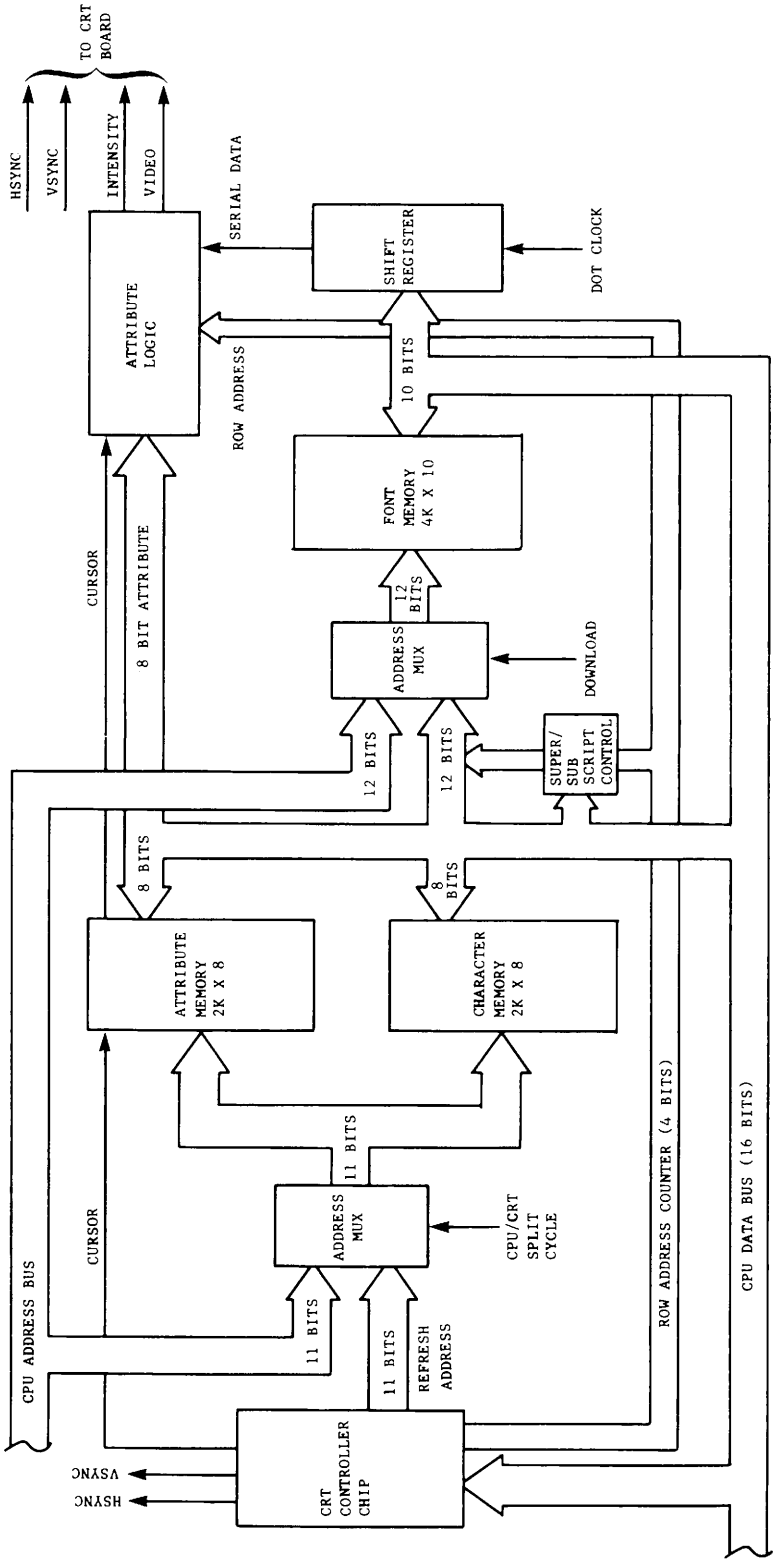


Figure 2-7. 8243/8343 Medium Resolution Video Controller Block Diagram

2.8 LOW-PROFILE SERIAL KEYBOARD

This section provides an overview of keyboard operations as well as a functional block-diagram level of theory discussion.

2.8.1 Keyboard Overview

The detached keyboard contains a dedicated microprocessor that accepts commands from the 8086 while sending both keyboard status data and keystroke data back to the 8086. The 8086 sends command data to the keyboard by writing a sequence of one or more command bytes to I/O port 10E8H. When the keyboard returns status data or keystroke data, the 8086 receives it by reading bytes from this port. Keyboard data can be sent and received simultaneously across the full-duplex keyboard interface.

After sending or receiving each byte of data, the keyboard interface generates a level 2 interrupt request. Software examines bits 4 and 5 of input port 1022H, the Interrupt Status Port, to identify the keyboard as the source of an interrupt request and determine which keyboard function generated the interrupt request. A transmit data interrupt sets bit 4 of the Interrupt Status Port when the keyboard is free to accept a byte from the 8086. A receive data interrupt sets bit 5 of this port when the 8086 must accept a byte of data from the keyboard. (Bits 0-3 and 6-7 of the Interrupt Status Port are used with other devices.) The keyboard buffers its output data so that it need not interrupt the 8086 more often than once every 10 ms.

Writing a byte of outbound data at I/O port address 10E8H automatically clears a keyboard transmit interrupt request. Alternately, if there is no more data to send, the interrupt request can be cleared by writing arbitrary data to output port 10E6H, the keyboard's Clear Transmit Interrupt Port. Reading a byte of inbound data at I/O port address 10E8H automatically clears a keyboard receive interrupt request.

Pressing a key causes the keyboard to send a 7-bit "keystroke code" to the 8086. Every key has its own unique keystroke code, which is arbitrary and bears no relationship to any of the various "character codes". In addition to the keystroke codes produced when they are pressed, the left and right "shift" keys also generate different codes, called release codes, when they are released.

The release code for any key is identical to its keystroke code, but with high-order bit 7 set (ie, keystroke code plus 80H). Special keyboard commands establish release codes for up to five other designated keys or, alternately, for all of the keys on the keyboard.

Any key on the keyboard is a potential "repeat" key. If the keyboard is programmed to generate a release code for a particular key, the CPU can assume that the key remains "down" (or pressed) between the time it receives the keystroke code and the time it receives the corresponding release code. Therefore, when a program that is monitoring the keyboard recognizes a pressed key in this way, it can decide whether the key will repeat, and at what rate.

Figures 2-8 and 2-9 show keystroke code assignments for the standard keyboard and the extended keyboard, respectively. There are some possible keystroke codes and their corresponding release codes that are not produced by any key. One of these, code 01, is used as a query response byte which is always followed by one or more status bytes. When the 8086 makes an inquiry by sending one of the query control byte sequences, it next continues accepting keyboard input until it receives the 01 query response byte and then accepts the appropriate number of status bytes before resuming normal keyboard input.

A 4-conductor cable fitted with a 4-pin DIN connector carries power and interface signals between the keyboard interface and the detached keyboard. The Keyboard connector and 4-pin DIN connector signals are shown below.

Table 2-10. Keyboard Connector Pin Assignment

Connector Pin No.	DIN Plug Pin No.	Signal
1	N/C	Negative lead to 8-ohm speaker.
2		Positive lead to 8-ohm speaker.
3	1	Ground.
4	3	Serial data output to keyboard.
5	4	5V power.
6	2	Serial data input from keyboard.

The keyboard interface is designed around a 6402 Universal Asynchronous Receiver Transmitter (UART) operating at 62.5K baud. On power-up or system reset, hardware initializes the UART to transmit and receive serial protocol that consists of one start bit (cleared to zero), an 8-bit data word (least significant bit first), and two stop bits (set to one), without parity.

The Lock and Shift keys have transmittable codes that allow maximum flexibility at the host system. The Lock key has a LED (BIT 0) for a visual indication that the key is engaged. The host system decodes the Lock key transmittal code and returns a code back to the keyboard through the 8031 to light the Key Lock LED.

The left and right shift keys have make and break codes in the keyboard default scheme. When either shift key is depressed, it will transmit its own x/y code (make code). When the shift key is released, a break code will be transmitted. The keyboard will only transmit the normal x/y codes. When a shift condition is sensed, the host system will append an 80 bit to all keys until it sees the break code for the shift key.

LED control commands are used to turn on individual LEDs as well as turn on and turn off all LEDs. The LED status command allows the host system to read the LED status at any time. The keyboard is initialized with all LEDs off.

N-key rollover exists between all encoded keys on the keyboard. Therefore; when a key is depressed while other keys are held down, the keyboard will be able to output the latest keycode.

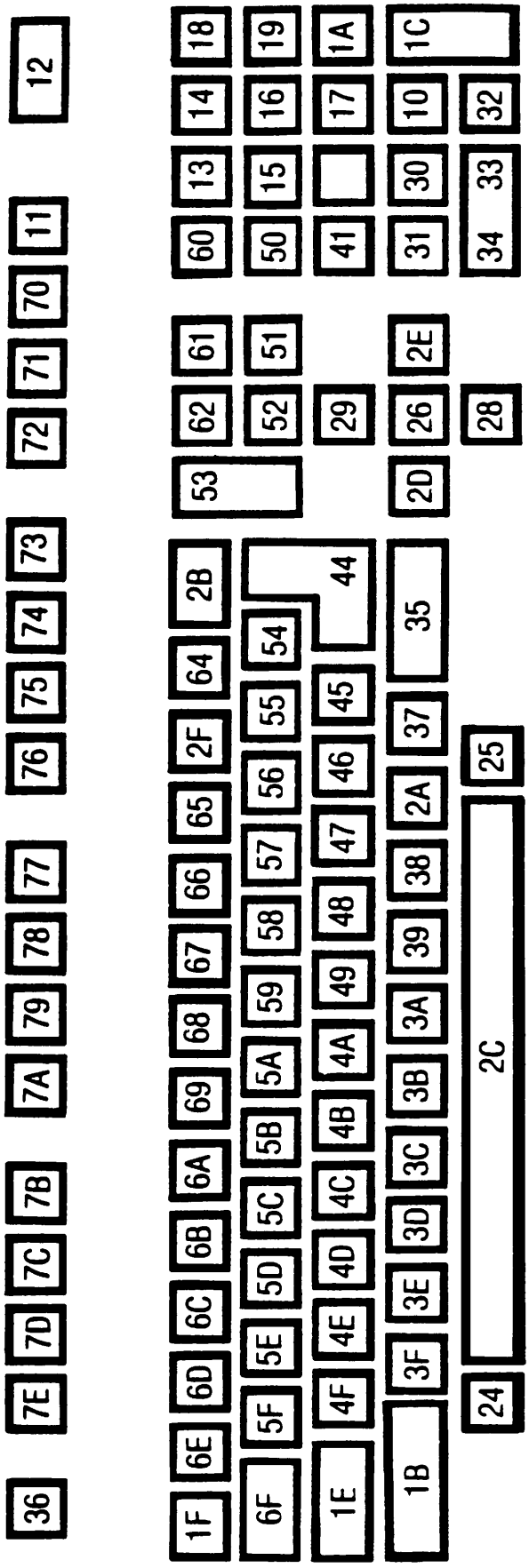


Figure 2-8. Standard Keyboard Mapping

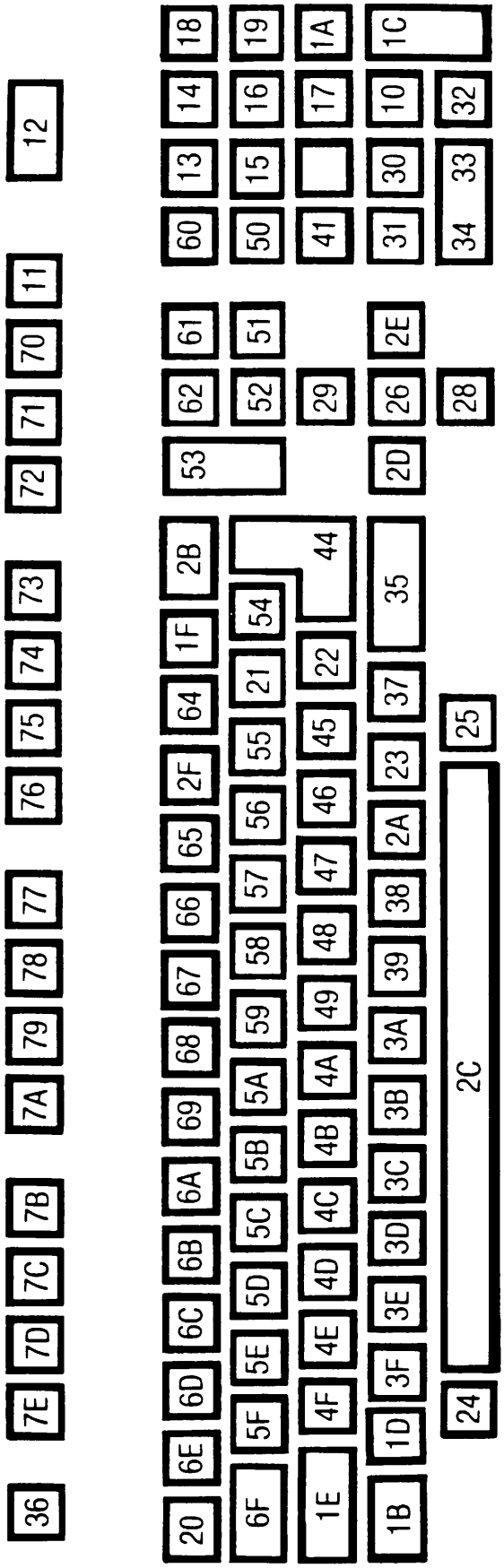


Figure 2-9. Expanded Keyboard Mapping

The CPU commands to light the six LEDs are important as these are used to indicate diagnostic errors. Two 8-bit switch banks on the keyboard are not used for PC applications but can be read by the CPU with a write 0E to 10E8H.

2.8.2 Keyboard Theory Of Operation

For the following discussion refer to the Keyboard Block Diagram Figure 2-10.

The 8031 device is a single-component 8-bit microprocessor that contains a 128 x 8-bit internal RAM memory, an internal oscillator and timing circuit for data synchronization, and a full duplex serial port UART. The 8031 device requires one supply voltage (+5v) for operation. Keyboard data can be sent and received simultaneously across the full-duplex keyboard interface.

Located on the PCB is a 4 MHz crystal generated clock used for the timing of the 8031 to the various other components located on the board. This clock is necessary since only power and data is transmitted from the 8086 CPU.

The keyboard keys are laid out in a 16 x 8 X/Y matrix for a total of 128 possible configurations. Not all possible configurations are used. The 8031 supplies three scan lines that are inputs to the 3 to 8 decoders. Each decoder provides a sequential strobe on each of its 8 X lines. These strobes are input to the two 8 switch banks (SW1 and SW2) to decipher the switch settings. These switches are not used on the PC and all should be open (OFF).

The Y lines are the return lines to the 908 device. When a key is depressed, the capacitive reactance is sensed by the 908 device and the 908 device will interrupt the 8031 device at port P3-3. When the interrupt is received, the 8031 performs a service routine to fetch the program contained in the EPROM. The capacitive reactance input to the 908 device changes an oscillator frequency within the device. The output of this oscillator is internally connected to an analog-to-digital convertor that provides the eight bit configuration code for that character. The 8031 adds one start bit and two stop bits to the eight bit character code and transfers the 11 bit data byte serially to the UART located on the CPU board.

The six LEDs located on the keyboard PCB are under the control of the 8086 CPU. The 8086 CPU sends a serial bit stream to the 8031 controller. The 8031 strips the start and stop bits and converts the serial data to parallel data. Then the 8031 executes the EPROM program and the data is presented to the LED tri-state latch. When enabled by the 8031, the latch data is output to the LEDs. Any low output will illuminate the appropriate LED.

The programmable sound generator circuitry incorporates a SN76489AN digital complex sound generator chip to provide 3 programmable tone generators and a noise generator, with programmable attenuation for volume control of all sounds and the ability to produce multiple sounds simultaneously. Tone generator channels 0, 1, and 2 each contain an independent tone generator and a dedicated attenuator. The noise generator on channel 3 consists of a noise source with a dedicated attenuator. Attenuators provide volume control by attenuating, or reducing, the loudness of the sound.

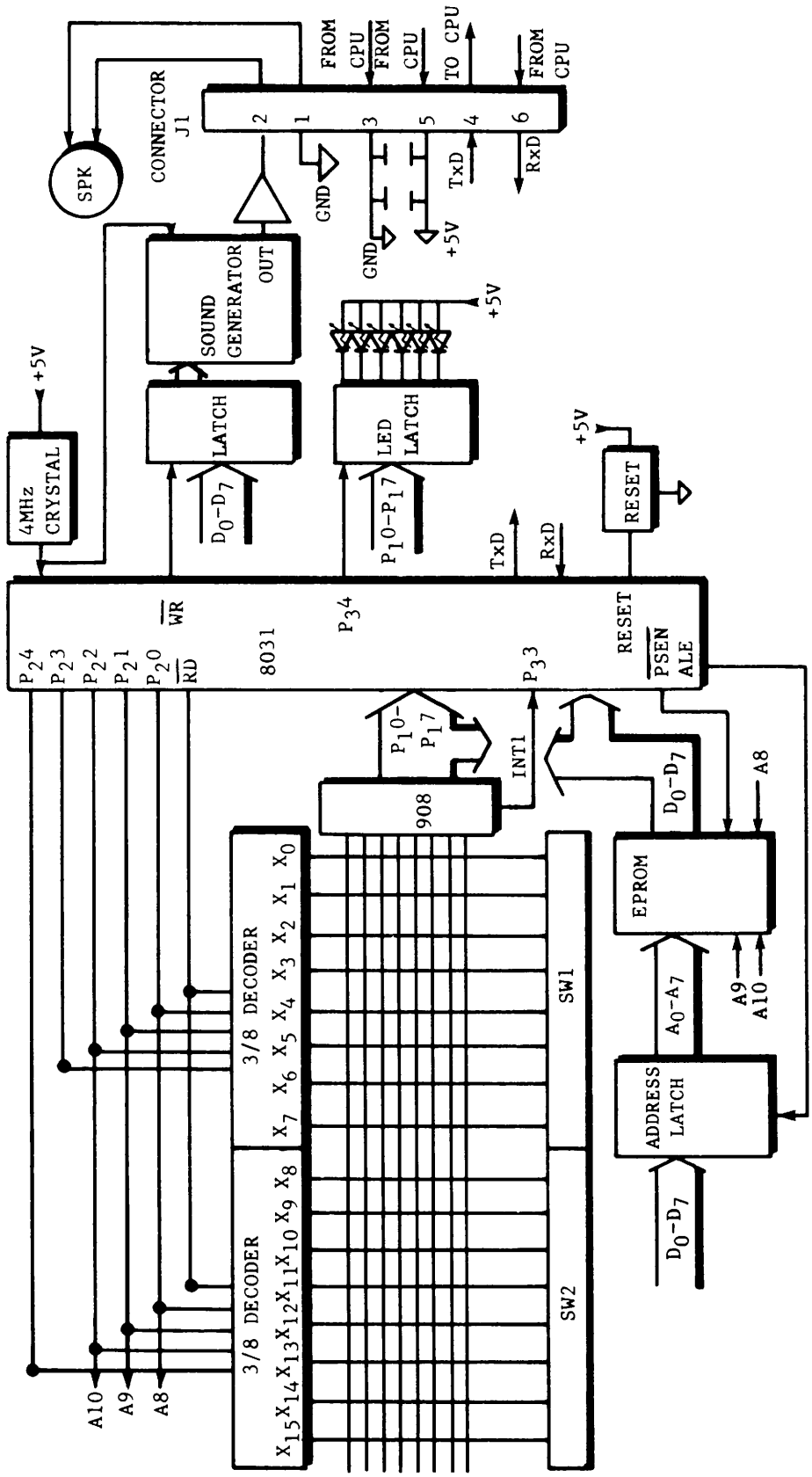


Figure 2-10. Low-Profile Keyboard Block Diagram

The 8086 programs any of the three tone generators on channels 0, 1, or 2 by loading the 10-bit Period Register for the channel, along with its 4-bit Attenuation Register. Each Period Register receives the value of the period for the output frequency produced on its channel, in units of 8 usec. This is equivalent to the value obtained by dividing the tone frequency by 125,000. Each Attenuation Register receives an attenuation factor between 0 and 30 db in units of 2 db. The maximum attenuation factor actually shuts off the channel so that no sound is produced.

To load a Period Register, the 8086 sends the keyboard a control byte sequence consisting of control code 32H followed by two Period Register control bytes. The first of these has bit 7 set to one, the tone generator channel number in bits 6 and 5, bit 4 cleared to zero, and the low-order four bits of the Period Register value in bits 3-0. The second Period Register Control byte has bits 7 and 6 cleared to zero and the high-order six bits of the Period Register value in bits 5-0.

To load an Attenuation Register, the 8086 sends a control byte sequence to the keyboard consisting of control code 31H followed by one Attenuation Register control byte. The Attenuation Register control byte has bit 0 set to one, the tone generator channel number in bits 6 and 5, bit 4 set to one, and the 4-bit attenuation factor in bits 3-0.

To load the noise generator's Control Register, the 8086 sends a 2-byte control sequence consisting of control code 31H followed by one noise control byte. The noise control byte has binary value "11100" in bits 7-3, with bit 2 either set to one for Gaussian white noise or cleared to zero for periodic noise. Bits 1 and 0 of the noise control byte designate the relative noise frequency as shown below:

0	0	High frequency noise.
0	1	Intermediate frequency.
1	0	Low frequency noise.
1	1	Channel 3 tone generator output determines noise frequency.

The procedure for loading the noise generator's Attenuation register is the same as the procedure for loading Attenuation Registers on the other three channels. The 8086 sends a 2-byte control sequence to the keyboard consisting of control code 31H followed by one Attenuation Register control byte. The Attenuation Register control byte has bit 0 set to one, the tone generator channel number (ie, 3 or binary "11") in bits 6 and 5, bit 4 set to one, and the 4-bit attenuation factor in bits 3-0. Attenuation factors are defined as for the three tone generator channels.

2.9 MONITOR THEORY OF OPERATION

For the following discussion refer to the block diagram Figure 2-11.

The Monitor unit contains a 12 inch CRT with a Monitor PCB for video input and scanning as well as controls to adjust the display. The CRT screen has a capacity of 25 lines with 80 characters per line for a total of 2000 characters displayed.

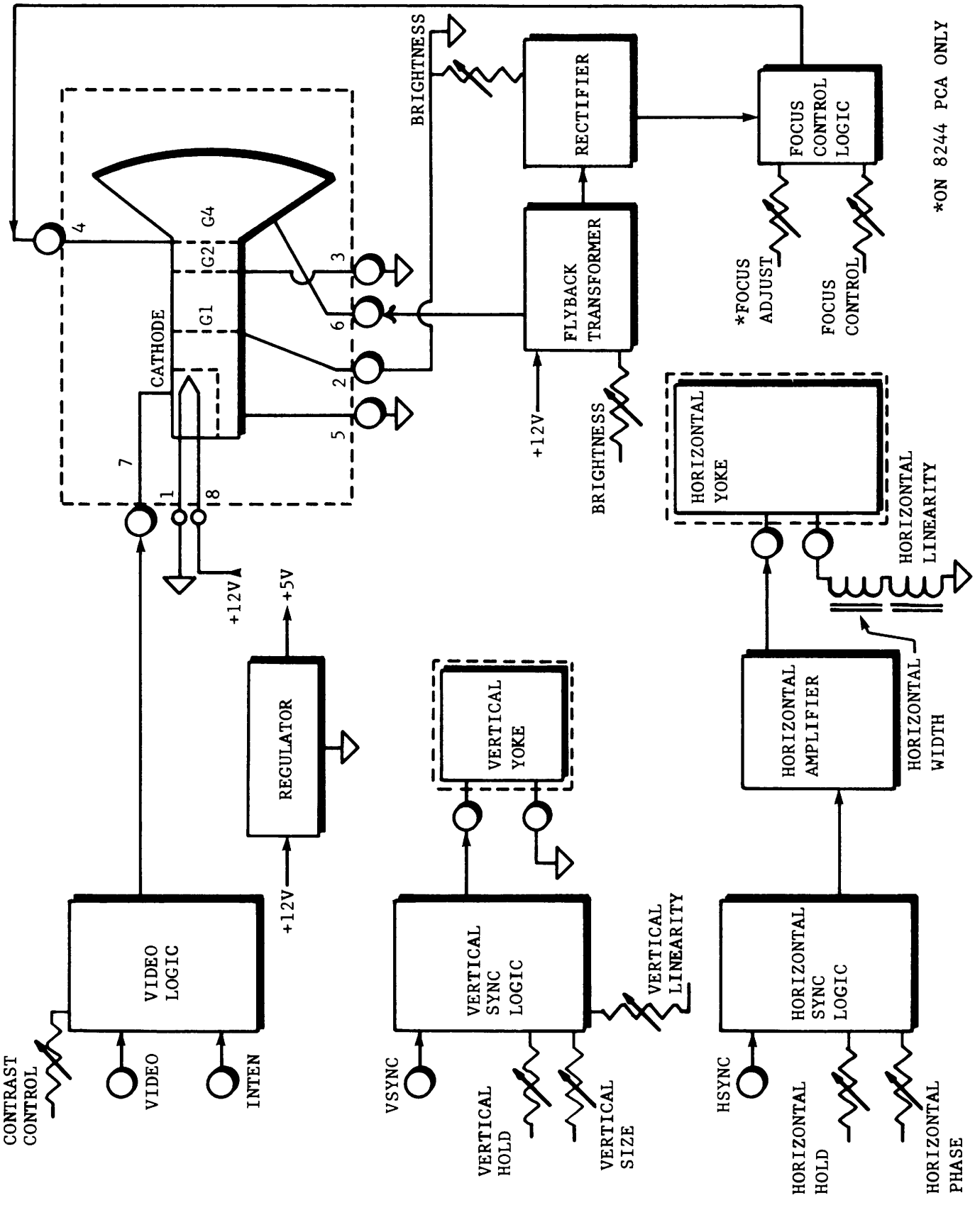


Figure 2-11. Monitor Board 8244/8344 Block Diagram

The Monitor board receives power (+12 volt) from the main power supply via one lead of the Monitor Cable assembly. This voltage is applied to a flyback transformer for the creation of the CRT voltage.

The Flyback transformer provides the gun and anode voltages required by the CRT. The front panel BRIGHTNESS control potentiometer is included in the flyback circuitry as is the focus control circuit consisting of two potentiometers, the focus adjustment and the focus control. The +12 volts is also regulated through a +5 volt regulator to supply the voltage required for the TTL components located on the board.

All the input signals (VIDEO, HSYNC, VSYNC, INTEN)) are generated on the Medium Resolution board (paragraph 2.7) and are presented to the Monitor board via the eight-pin monitor cable.

The Video input is presented to the circuitry made up of Q1 thru Q4 which separates and amplifies the video. The amplified video is then applied to the cathode of the 12 inch (diagonal) CRT. Included in this circuitry is the front panel contrast control.

The Horizontal Sync input is presented to the Horizontal Processor device. The horizontal phase adjustment and the horizontal hold adjustment are inputs to the horizontal processor device. The horizontal processor's output is applied to an amplifier circuit consisting of a transformer and a NPN transistor to drive the horizontal yoke. Adjustments for horizontal width and horizontal linearity make up the rest of the horizontal yoke output circuitry.

The Vertical Sync input is applied to Vertical Processor device. Vertical hold, vertical size, and vertical linearity adjustments are input to this device. The vertical processor contains its own internal amplifier. The vertical processor's output is applied to the vertical yoke.

2.10 OPTION BOARDS

The following Option boards theory of operation is discussed in the following pages. Each board discussed is to the functional block diagram level.

- o Winchester Controller Board 8225-A
- o Extended Memory Board 8242
- o Medium Resolution Graphics Option 8233
- o Low Resolution Controller Option 8222-A
- o Z80 Option Board 8248
- o Local Communications Option CPU Board 8246
- o Local Communications Option Datalink Board 8245
- o Remote Telecommunications Options 8232 and X.21 8252
- o Multiport Communications Controller 8251

2.10.1 Winchester Controller

The Winchester Disk Controller (WDC) is an intelligent, Z80A-based, I/O option board that operates one 5.25-in, Winchester technology, random access disk drive. The Winchester drive stores up to 10M bytes of formatted data using both sides of its two permanently mounted platters.

Under the direction of the WDC, its moveable read/write head assembly accesses 304 logical tracks on each of the recording media surfaces. There are sixteen 512-byte sectors per track on each surface, for a total of 64 sectors per cylinder on a dual-platter drive. Disk platters and recording heads are housed within a hermetically sealed enclosure with a filtered air recirculating system that protects both the media and the heads from temperature variation and environmental contamination.

WDC command execution is most conveniently viewed in four phases. An optional initialization phase begins the WDC command sequence. During initialization phase the 8086 accesses I/O ports to reset the WDC, abort any previous operation that might still be in progress, establish or change the WDC's interrupt priority level and DMA channel assignment, and perform other command set-up functions. Once the WDC has been initialized, a sequence of WDC commands can be executed without repeating the initialization procedure; however, a program has the option of reinitializing the WDC at any time.

During command phase, after any required initialization has been performed, the 8086 loads a sequence of eight command bytes into the WDC Command Register (output port 1x02H). The 8-byte command sequence supplies all information that the WDC needs to execute the command. It establishes the function code; a disk address consisting of the next sector, cylinder, and head to access (if any); and the number of sectors involved in the command (if applicable). Certain WDC commands accept other specialized types of information in their 8-byte command sequence. However, regardless of the function being performed, the 8086 always transfers exactly eight bytes into the WDC Command Register, even though some functions do not need all of the command phase information. These eight bytes designate the following:

1 Function code
2 Second byte always cleared to zero
3 Low-order byte of starting cylinder number
4 High-order byte of starting cylinder number
5 Starting surface (ie, read/write head) number (0-3)
6 Starting sector number (0-31)
7 Low-order byte of number of sectors to transfer
8 High-order byte of number of sectors to transfer

To read or write disk data, an 8086 program first initializes a DMA channel and then issues the appropriate WDC command. Execution phase begins when the 8086 writes the eight command bytes to the WDC Command Register. During execution phase, the WDC issues DMA requests and transfers single bytes of data across the DMA channel as needed. Internal WDC memory buffers up to 3 sectors (1536 bytes) of input or output data; therefore, the DMA data rate is not critical when reading or writing the Winchester disk. A WDC interrupt signals the end of execution phase and the beginning of result phase once the required number of sectors has been transferred.

During a read, write, or other sector-oriented operation, the current disk address automatically increments, increasing from sector 0 to sector 0FH, at the end of every 512-byte block. After sector 0FH on one surface has been accessed, the surface (or head) number automatically increases by one and sector 0 on the next surface is accessed next.

After the WDC accesses sector 0FH on the highest surface (either surface 1 on a single-platter drive or surface 3 on a dual-platter drive), the cylinder number automatically increases by one and sector 0 of surface 0 on the next cylinder is accessed next. Unlike sector and surface numbers, the cylinder address does not wrap around to zero after the highest numbered cylinder has been accessed. Therefore, a single WDC command can read or write any contiguous region of disk data, including the entire disk, but it cannot read or write beyond the highest numbered cylinder.

If the command is successful, a WDC interrupt request signals the end of execution phase and the beginning of result phase. The result phase makes eight bytes of status information and other housekeeping data available to the 8086 through the WDC Operation Status Register (input port 1x00H). In response to a WDC interrupt, the 8086 must either abort the command or else read all eight bytes of result phase data. The eight bytes of result phase data designate the following:

1 Function code for the command just performed
2 Operation Status Code
3 Low-order byte of next (or last) cylinder number
4 High order byte of next (or last) cylinder
5 Next (or last) surface (ie, head) number (0-4)
6 Next (or last) sector number (0-15)
7 Number of sectors transferred (low-order byte)
8 Number of sectors transferred (high-order byte)

The disk address contained in the next (or last) sector, surface, and cylinder fields is the address of the last sector transferred successfully (when an error occurs) or, in the absence of an error, the address of the sector following the last sector transferred. As mentioned earlier, sector, surface, and cylinder numbers automatically wrap around from sector 0FH to sector 0 of the next surface, from the highest numbered surface to surface 0 of the next cylinder, and from one cylinder to the next. However, after sector 0FH on the highest numbered surface of cylinder 96H--the last sector on the disk--has been transferred successfully, an illegal cylinder number will appear as the next cylinder number in the third status byte.

Reading I/O port 1x04H returns arbitrary data and automatically clears the 8086 interrupt request that signaled the beginning of result phase. The end of result phase (end of a WDC command) occurs when the 8086 reads the eighth and final byte of Operation Status Register information. As with the eight bytes of command phase input, result phase always returns exactly eight bytes of output even though most commands do not use all eight status bytes. Except for the EXECUTE DIAGNOSTIC (F0H) command, every WDC command returns eight bytes of result data, even though some commands do not use all eight of the status bytes.

The first status byte always contains the operation code for the command that was performed. The second status byte always contains 80H if the command was performed successfully. If an error prevented successful execution of a command, an error code will be contained in the second status byte.

2.10.2 Expanded Memory Board

The theory of operations for the expanded memory board is broken down into an Overview section (2.10.2.1) and a Theory section (2.10.2.2). The theory section is discussed to the block diagram level. Although three memory sizes are possible (128K, 256K, 512K) all data-write and data-read operations are functional performed the same. This section of the manual discusses the 512K memory board which incorporates the 128K and 256K version of expanded memory.

2.10.2.1 Expanded Memory Board Overview

An optional expanded memory board augments the 128k bytes of standard system memory with 128k, 256k, or 512k bytes of extended dynamic RAM with parity. The following are the WLI numbers of the expanded memory boards available:

WLI No. 210-8242	128K
WLI No. 210-8242-1	256K
WLI No. 210-8242-2	512K

The Professional Computer can accept up to 512K bytes of expanded memory, thus providing a total system capacity of 640K bytes of RAM. (128K resident on the System board and any combination of 128K bytes (128K, 256K, 512K) per expanded memory board with 1, 2, or 3 expanded memory boards installed.) The number of expanded memory boards should be kept to a minimum since only 5 option slots are available with the Electronics Unit.

Expanded memory address space is organized into four 128K byte banks. Each bank of extended memory must be initialized for access by means of the Memory Segment Boundary Register. This register assigns a base address to each of the four expanded memory banks. The following are the six usable base addresses allowed:

20000H	80000H
40000H	A0000H
60000H	C0000H

As with system board memory, parity is undefined before an extended memory location has been written with data, therefore; a parity error may occur if the program reads an extended memory location that was not first written with data. Extended memory parity errors generate an 8086 nonmaskable interrupt (NMI) request denoted I/O ERROR. The program can distinguish expanded memory parity errors from system memory parity errors by accessing an I/O port on the expanded memory board. The Expanded memory I/O ports are listed in Table 2-11.

The extended memory board utilizes circuitry to support only common memory cycles. These are: Read, Write, and RAS Only Refresh. Delayed write cycles and page mode operations are not possible. RAS Only Refresh is required to maintain data integrity. A refresh cycle time of 2 ms is required. In order to refresh the total memory, 128 refresh cycles must be performed within the 2 ms time frame with each cycle specifying a different row address. A refresh cycle will occur when RAS goes active.

Table 2-11. Expanded Memory Board I/O Ports

PORT	DESCRIPTION
1xC0H	Read or Write Extended Memory Segment Boundary Register. Four 4-bit fields determine the base address (3 bits) and on/off status (1 bit) of each 128k-byte bank of extended memory. Bit assignments are as follows:
	2, 1, 0 — High-order bits (A19, A18, A17) of base address for first 128k-byte bank of extended memory.
	3 — Set to one when first bank of extended memory is active. If cleared to zero, disables first bank.
	6, 5, 4 — High-order bits (A19, A18, A17) of base address for second 128k-byte bank of extended memory.
	7 — Set to one when second bank of extended memory is active. If cleared to zero, disables second bank.
	10, 9, 8 — High-order bits (A19, A18, A17) of base address for third 128k-byte bank of extended memory.
	11 — Set to one when third bank of extended memory is active. If cleared to zero, disables third bank.
	14,13,12 — High-order bits (A19, A18, A17) of base address for fourth 128k-byte bank of extended memory.
	15 — Set to one when fourth bank of extended memory is active. If cleared to zero, disables fourth bank.
1xCEH	Write arbitrary data to clear the parity error flag after a parity error.
1xFCH	Write arbitrary data to reset the extended memory board. Clears the Extended Memory Segment Boundary Register to zero, thereby disabling all extended memory. Also clears the parity error flipflop and establishes odd parity.
1xFEH	Read Option ID Code (D0-7 will be 3FH) and interrupt (parity) status. (D8 will be set to one if a parity error has occurred since the parity error flipflop was last cleared, otherwise cleared to zero).
	Read or write odd/even parity flag. Odd parity is established by setting D9 to one. This is the default option. Clearing D9 to zero selects even parity.

The memory array consists of either 18, 36, or 72 DRAM devices for storage capabilities or 128K, 256K, or 512K of parity-checked bytes respectively. Each configuration consists of a high-order and low-order RAM bank. Each bank (9 RAMs per bank) has its own parity RAM. The parity RAM is the ninth RAM (bit D8). Each RAM bank has a dedicated RAS/CAS drivers (upper and lower denoted RASLx and RASUx, CASLx and CASUx).

All write operations to memory are destructive as they change the data resident in that memory location. Read operations are non-destructive where a memory location can be read without the data integrity being altered. Parity is checked only after data has been written to a specific address location. Any data resident in memory before a write cycle is completed is not parity-checked.

Any parity error during a read operation generates a FATAL I/O ERROR (low-active). The Error signal is transferred via the Motherboard common bus to the CPU board's 8086 CPU device. Once the 8086 CPU receives this signal, it executes a special routine to determine where the I/O ERROR signal originated.

Upon power-up of the PC system, the PC system scans each option slot of the system to determine if any option boards are installed. When the Expanded Memory board is determined to be installed, a software routine is exercised to determine the actual memory size. This routine eliminates the need of having switch selectable or hardwired selectable memory codes to distinguish memory size.

Memory access can be either by 8086 CPU memory cycle or by a DMA transfer. Both memory accesses will be discussed in the section on theory of the Expanded Memory board.

2.10.2.2 Theory of Operation of Expanded Memory Board

The theory of operation section is discussed to the function block diagram level. Refer to the Expanded Memory Board block diagram in Figure 2-12.

The System Address bus (A1-A16) is buffered on-board with the buffered address being presented to the Address Mux. The Address Mux circuitry is necessary as the memory chips only require eight address lines to address any RAM location. In order to select the 16-bit address, the Address Mux is switched from the lower address lines (A1-A8) to the upper address lines (A9-A16). This switching of the address mux is accomplished by COLEN1 and COLEN2 (Column Enable) signal. The COLENx signals are generated by the STARTRAS (Start Row Address Strobe) signal delayed by 30 nseconds via a digital delay chip.

System Address Bus lines A17-A19 are used for the Address Comparator section of the memory board. The address comparator section consists of four 4-bit magnitude comparators. When address lines A17-A19 equal the bit configuration generated from the Memory Boundary Register, the corresponding magnitude comparator generates a High out on its A=B output. This HIGH enables the RAS (U and L) and the CAS (U and L) drivers for the selected RAM bank.

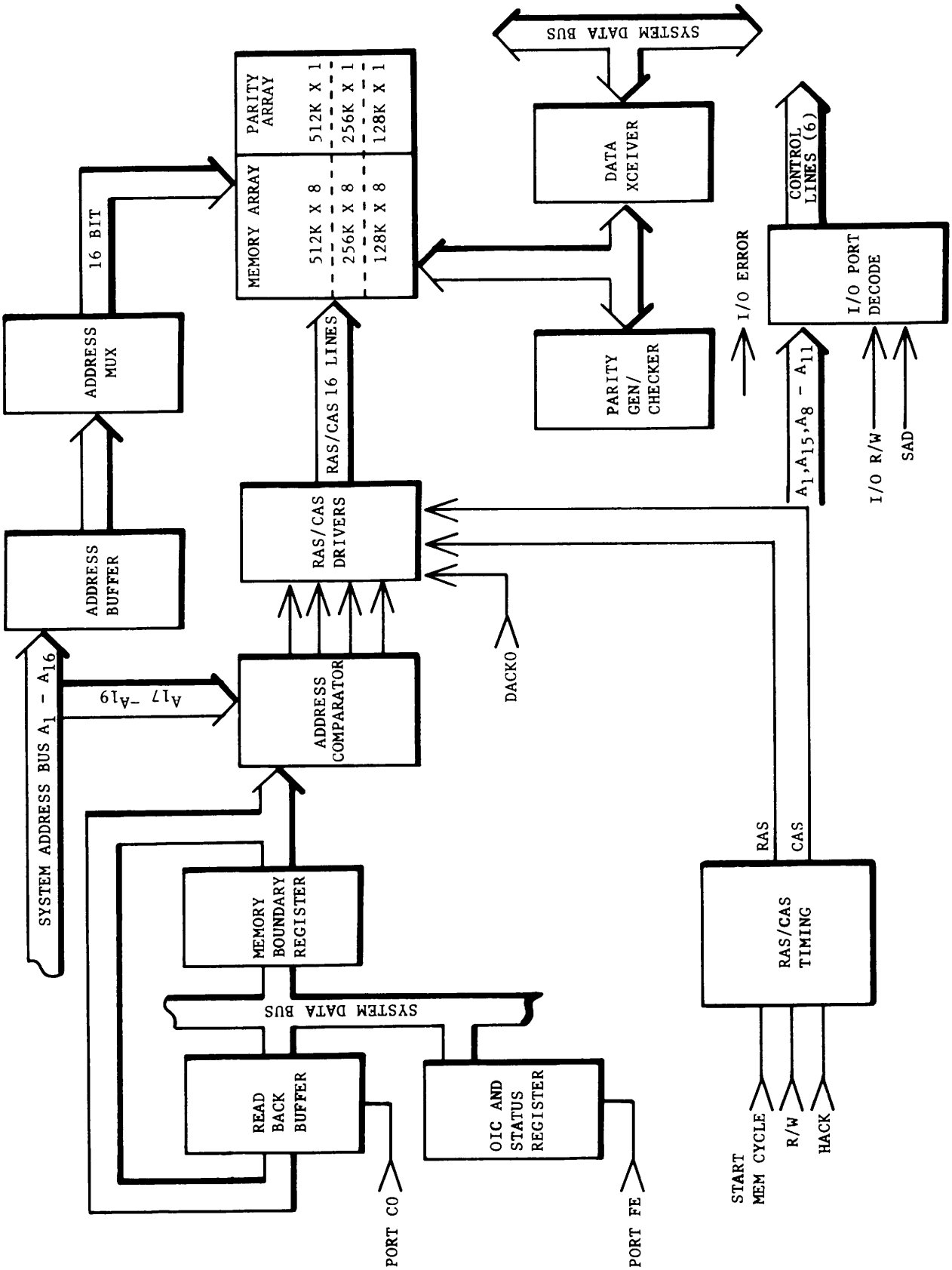
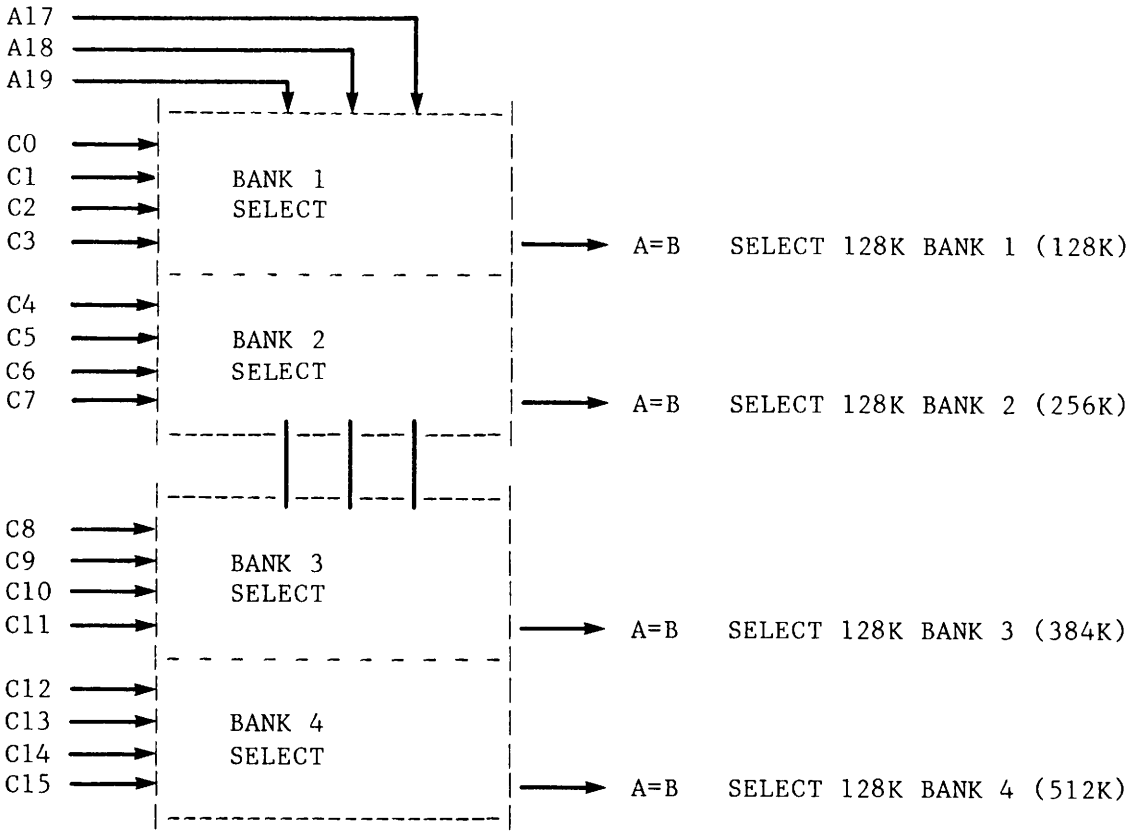


Figure 2-12. Extended Memory Board Block Diagram

The Memory Boundary Register receives the 16-bit data bus (16 bits for 512K version, 8 bits for 128K-256K version). The Boundary Register is broken down into four sections each having 4 bits. Three bits of each section are used by the comparator to compare the contents of the register with the bit configuration of address lines A17-A19. The fourth bit is used to enable or disable a particular RAM bank. The Boundary Register sections are shown below. The RAM banks for the following example are denoted BANK 1, 2, 3, and 4 which represent 128K, 256K, 384K, and 512K Bytes respectively.

It should be noted that memory boards that contain less than 512K bytes of memory do not require the upper 8 bits for RAM bank selection.



The Read Back Buffer consists of two 8-bit latch devices (one latch device for 128K-256K versions) used to latch the data presented on the data bus (16 bits for 512K version, 8 bits for 128K-256K versions). This allows the system to "Read Back" the data previously sent to the memory board.

The address comparator (as previously mentioned) selects one of the four RAM banks while disabling the others. These enable/disable signals are presented to RAS/CAS drivers. Each RAM bank has dedicated RAS/CAS drivers to prevent ringing and to offset the capacitance associated with each line. The enabled RAS/CAS driver presents the RAS/CAS signal to the selected RAM bank during the read-data and write-data operations. Refresh is not affected since refresh is accomplished by the DACK0 signal from the DMA controller located on the CPU/System board.

RAS/CAS timing block consists of the 8 MHz system clock, the 4 MHz clock from the CPU board, delay circuits and flip flops to create the RAS and CAS timing. The signal denoted START MEM CYCLE is not a signal denoted on the schematics rather it is a term used to encompass the number of signals required to activate the memory. Memory can be accessed by either a CPU Memory Cycle or a DMA transfer, each of which generate RAS/CAS timing differently. The RAS/CAS timing will be discussed in each section.

The RAS signal is always generated and is applied to the RAM bank during read operations, write operations, and during the RAS ONLY Refresh cycles. The CAS signal is also always generated but is gated OFF during RAS Refresh cycles and is gated ON during Read operations and Write operations only.

The CASL (lower) signal is gated to the CAS drivers when the CPU's A0 line is LOW denoting a lower 8-bit transfer. The CASU (upper) signal is gated to the CAS drivers when the BHE (Byte High Enable) signal from the CPU is LOW denoting an upper 8-bit transfer. When both A0 is LOW and BHE is LOW, this denotes a 16-bit transfer. The mode of transfer truth table is shown below.

Table 2-12. Data Mode of Transfer Truth Table

BHE	A0	MODE OF TRANSFER
0	0	16-BIT TRANSFER
0	1	UPPER 8-BIT TRANSFER
1	0	LOWER 8-BIT TRANSFER
1	1	NOT POSSIBLE

0 DENOTES LOGIC LOW
1 DENOTES LOGIC HIGH

The memory array consist of either 128K (16 64K X 1 bit RAMs plus 2 64K X 1 bit RAMs for parity), 256K (32 64K X 1 bit RAMs plus 4 64K X 1 bit RAMs for parity), or 512K (74 64K X 1 bit RAMs plus 8 64K X 1 bit RAMs for parity) of parity-checked memory. See Figure 2-12 for memory layout. Each byte of data retained in memory has an associated parity bit assigned.

The parity can be either even or odd. On power-up, the system reset signal selects odd parity. Odd parity can also be selected by writing to port 1xFC (refer to Table 2-11). Even parity can be selected by writing a "zero" to bit 9 of port 1xFC, therefore; odd parity can be selected by writing a "one" to bit 9 of port 1xFC. The parity (odd or even) is deciphered by the Parity Generator/Checker block. If an error is detected, the parity checker outputs the I/O ERROR signal to the NMI interrupt input of the 8086 CPU.

Note that the inclusion of the parity generator/checker circuit does improves the integrity of the data, however; if an even number of incorrect data bits are checked then no error will occur.

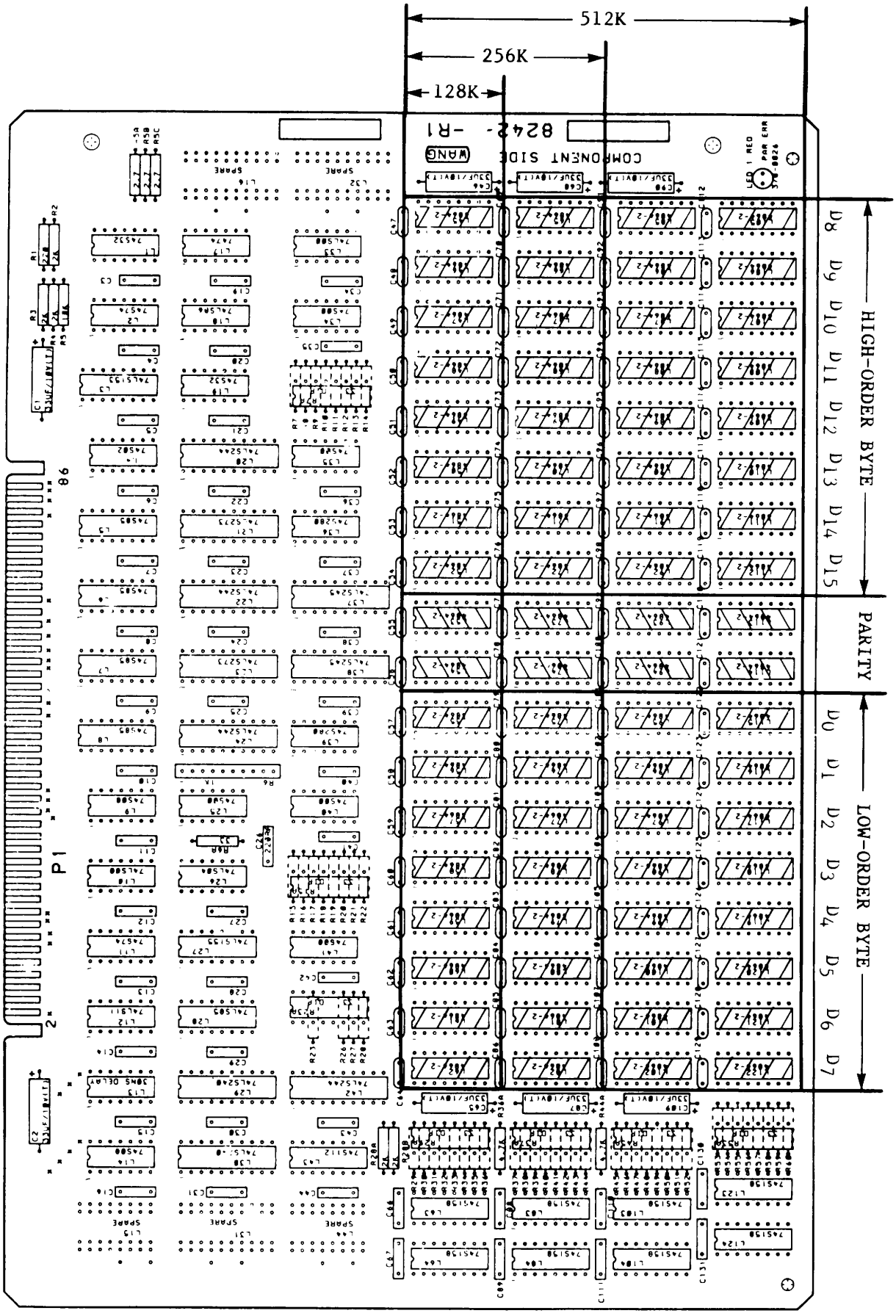


Figure 2-13. Expanded Memory Board RAM Layout

The Data Transceiver block consist of bidirectional buffers to buffer the system data bus to the memory data bus during write-data operations and buffers the memory data bus to the system data bus during read-data operations.

Memory access can be accomplished either by CPU access or by DMA Transfer. Each operation is discussed individually in the preceding paragraphs.

2.10.2.3 CPU MEMORY ACCESS

CPU memory access is accomplished by the 8086 CPU device sending the memory address location onto the System Address Bus. If the Memory Boundary Register matches the address bus (via the Address Comparator), this indicates that the expanded memory is to be accessed. If the Memory Boundary Register does not matches the address bus (via the Address Comparator), this indicates that the expanded memory was not being accessed. Under either condition the memory is always being refreshed.

When the Memory Boundary register matches the address bus, the memory address will be emitted from the Address Buffer to the input of the Address MUX. The Address Mux will switch the lower address lines first then the upper address lines. This is due to the fact that the RAMs have only eight address inputs. The lower address bits are strobe onto the lower RAM bank by the RAS signal. The COLEN (Column Enable) signal then switches the Address Mux causing the higher address bits to be presented to the upper RAM bank. The high order address bits are strobed onto the RAM bank by the CAS signal. Once the RAM address is established, the data to be input to the selected RAM bank is presented to the Data Transceivers. The Parity Generator Checker deciphers the data bit pattern and assigns a parity bit (even or odd depending on the data pattern) for each of the 8 bits of data being stored in memory. (Eight bits of the 16 bit data record is stored in the lower RAM bank and the other eight bits of the data record is stored in the upper RAM bank. Each RAM bank has a dedicated Parity RAM.)

The 8086 selects the mode of transfer (refer to Table 2-12) by outputting the appropriate signals on Address line A0 and on BHE. These signals are presented to a NOR gate circuit for the selection of either a 16-Bit Transfer, upper 8-bit transfer, or lower 8-bit transfer. This selects the appropriate CASU and/or CASL during read and write cycles. For our discussion the 16 bit transfer is used.

With the lower 8 bits of the data record along with the parity bit assigned available on the 8-bit memory data bus, the 8086 outputs a low on its AMWC line (Advanced Memory Write Command) which creates RAM WE (Write Enable) low. On the next negative transition of the CASL signal the data (9 bits) on the memory data bus will be strobed into the lower RAM bank. Now the upper 9 bits of data are presented to the memory address bus and on the negative transition of CASU this bits are strobed into the upper RAM bank.

A CPU read cycle is essentially the same with the exception that the AMWC signal is high. This generates a WE high being presented to the selected RAM bank.

The data is strobed out of memory on the negative transition of the appropriate CAS signal onto the memory data bus. This data is then presented to the Parity Checker with the data bit pattern being deciphered and checked against the parity bit assign to that 8 bits of data. If a parity error is discovered, the Parity Checker Generator outputs a low on the I/O ERROR line. This low is presented to the 8086 CPU. If no parity error occurs the data is pass through the data transceivers to the system data bus. It should be noted that the parity generator/checker may not discover multiple bit errors in the 8 bit data pattern. If the parity of the 8 bit data pattern written to memory is the same as the parity of the corrupted 8 bit data pattern read from memory, no I/O ERROR will occur.

2.10.2.4 DMA MEMORY ACCESS

DMA memory access is under the control of the 9517 DMA controller chip located on the CPU board. The timing required to generate RAS and CAS are synchronized by the 4 MHz clock from the DMA controller. The speed at which peripheral devices can transfer data is varied, therefore the DMA controller inserts delays or wait states. The wait states are accomplished by delaying the occurrence of CAS by 125 nsec intervals. As many delays can be inserted as deemed necessary by the DMA controller. RAS ONLY Refresh is accomplished by the DMA channel 0 DACK0 line (Data Acknowledge 0) which has no bearing on the rise of fall of CAS. Read data and Write data operations are performed the same as described in the CPU ACCESS paragraph.

DMA transfers can be one byte up to and including 64 byte transfers. Parity generation and checking is performed as previously described in the CPU ACCESS paragraph.

2.11 MEDIUM RESOLUTION GRAPHICS OPTION

The theory of operation section is discussed to the function block diagram level. Refer to the Medium Resolution Graphics block diagram in Figure 2-14.

The 8233 Medium Graphics Resolution board must be cable connected to the 8243/8343 Character Resolution board. The Graphics board receives the timing signals as well as the Vertical SYNC signal generated by the Character Resolution board to produce bit mapped graphics denoted as GHVIDEO. Located on the Graphics board are two banks of dynamic RAM memory chips for a total of 16K X 16 bits. All timing support, RAS, CAS, and the Chip enable circuitry required by the memory are resident on this board. The RAM memory provides storage for the 800 X 300 pixels (240,000 pixels) that are required to map the CRT screen. A graphics software program loads the memory with the graphics to be displayed. The data is read out of memory in 16 bits and converted to serial data through a shift register. The data is then shifted serial out (via the cable) to the Character generator board where it is logically OR'd with the Text Video output from the Character board. Once logically OR'd, this data (denoted VIDEO) is presented to the Monitor board located within the CRT unit.

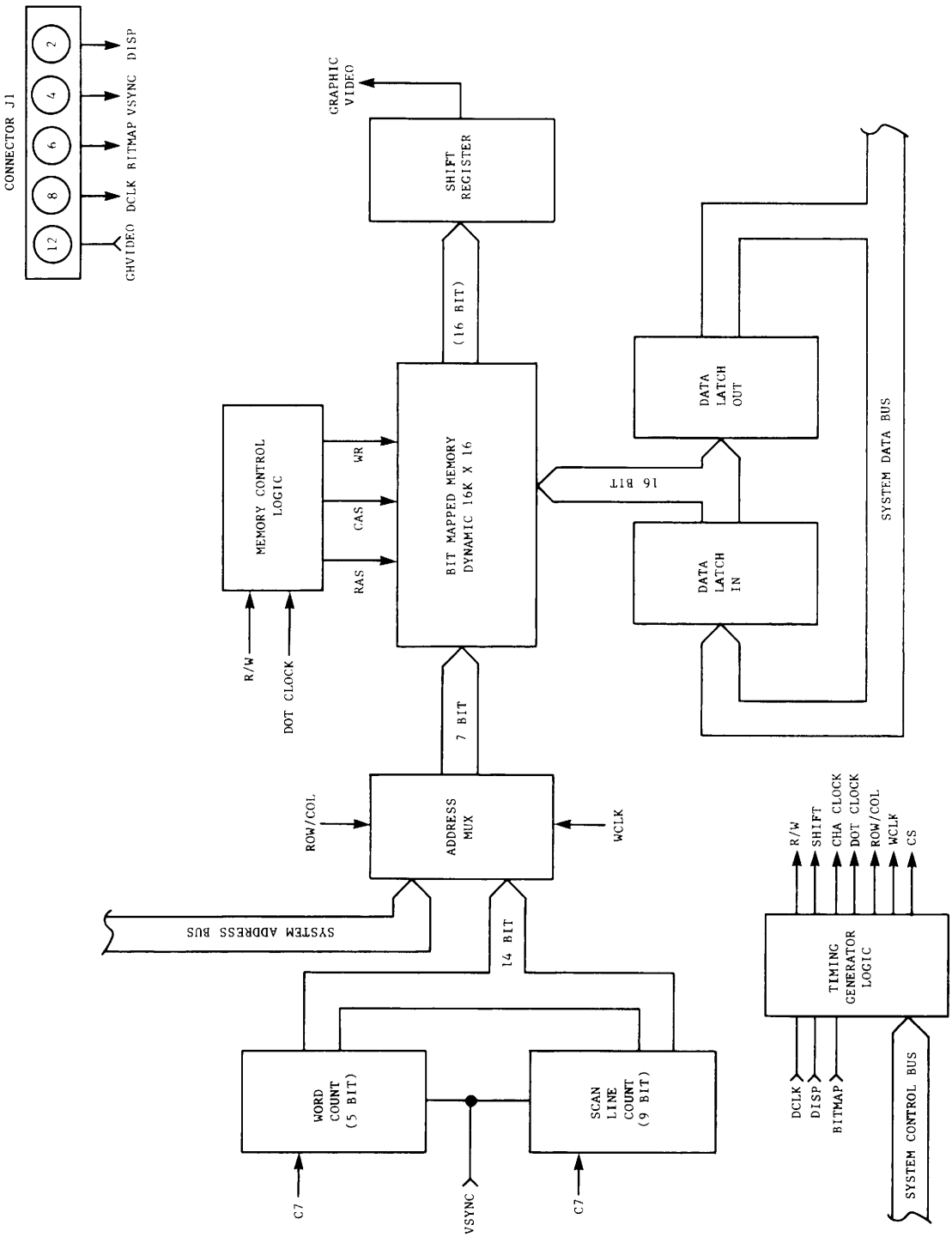


Figure 2-14. Graphics Resolution Board Block Diagram

The Medium Resolution Graphics Board receives the Video Sync (VSYNC) signal from the 8243/8343 PCB via connector J1 pin 4. The VSYNC signal is used to perform a clearing function for the Word Count and Scan Line Count registers. Timing for the registers is performed by the C7 clock derived from Display Clock (DCLK) signal which is also generated on the 8243/8343 PCB.

The DCLK signal, DISP, and BITMAP signals are generated on the 8243/8343 PCB and input to the Timing Generation Logic. The Timing logic generates the R/W, CPU/CRT, CPU/SCAN, DOT CLOCK, CHAR CLOCK, and the DOWNLOAD signals. All the timing required for the 8233 Graphics Resolution PCB is generated on board including RAS ONLY Refresh. Split cycle timing provides access to the memory for the system software for one half the cycle and CRT refresh from the 14 bit scan counter for the other half of the cycle.

The Address Mux supplies the Row address and the Column address for the 16K word memory array. Only even word locations are used. The DRAMS used are 16K X 1 Bit with each RAM retaining one data bit of the sixteen bit data record (D_0-D_{15}).

The Address Mux is switched by the ROW/COL signal. The ROW address is switch to the memory bank when ROW is active Low and the column address is muxed to the memory array when COL is high. When WCLK is low, the Word Count is Muxed to the memory array followed by the Scan Line Count.

The RAM devices use only seven address lines to select one of the 16K RAM addresses available within the RAM bank. The bit configuration is input to the Data Bus input latch and is presented to the memory chips data in (DIN) inputs when INB is inactive LOW. On the negative transition of CAS, (when WR is Low) the data bit presented to the input of the RAMs is strobe onto to RAM device.

In order to move the data from the RAM bank to the Video display, the address mux is selected and switched as previously mentioned above. The data is strobed out of memory when WR signal is High. On the following negative transition of CAS the data is strobed out of the memory location onto the internal data bus. This data is loaded into the shift register when SHIFT (SH) is inactive high. Once the data is loaded, SH will go to a low and the data will be clock out in serial one bit at a time on the next 16 positive transitions of the Dot Clock. The serial order is the highest bit (bit 15) out first to the lowest bit out last (bit 0).

This serial data out (denoted GHVIDEO) is presented to the 8243/8343 PCB via the interconnect cable and is OR'd with Text Video and presented to the Monitor Board located in the Monitor assembly. It should be noted that both Text and Graphics can be displayed on the screen at the same time but can not share a character cell.

2.12 LOW RESOLUTION CONTROLLER

The low resolution video controller option incorporates an MC6845-1 video timer and controller chip to drive a conventional monochrome broadcast television set, a color broadcast television set, a monochrome video monitor, or a red-green-blue (RGB) color monitor.

All four low resolution display options use 15.70-KHz horizontal and 60-Hz vertical frequencies. All display 25 lines of text on the screen, but the number of characters in a line can be either 40 or 80, depending on whether a broadcast television set or a video monitor is used, as shown in Table 2-13. Video monitors can display either 40- or 80-column text. A broadcast television set must use only the 40-column display format.

Table 2-13. Low Resolution Video Output Options

Output Device	Screen Size	Character Size
Broadcast television	320 x 200 pixels 40 x 25 characters	8 x 9 pixels (4 bits/pixel)
Video monitor	640 x 200 pixels 80 x 25 characters	8 x 9 pixels (2 bits/pixel)

Video display screens are divided into 40 or 80 columns. A column is a vertical strip, eight pixels wide, running from the top of the screen to the bottom. A character will generally fit entirely within one column (although this is not a requirement), and certain hardware capabilities, such as horizontal scrolling, operate on a per-column basis. A video monitor has 80 columns that are each eight pixels wide. A broadcast television has 40 columns, each with the same 8-pixel width. Thus, the columns on a broadcast television display are twice as wide as the columns on a video monitor of equal screen size. Broadcast television pixels are also twice as wide as their video monitor counterparts; however, pixels displayed on either device are equal in height.

The 32k-word low-resolution video memory space is divided into two planes of bitmap memory that drive an 80-column display, or four memory planes that produce half as many pixels to drive a 40-column display. Video memory must be word addressed; byte addresses cannot be used, and only even addresses are valid. Direct memory access, which handles only byte data, cannot be used to transfer information to or from video memory.

Eight consecutive pixels stored in one byte of video memory occupy the same character column and the same scan line on a display screen. In a sense, each video memory byte address is a set of character column by scan line coordinates. A word of video memory contains the eight pixels for one memory plane in its low-order byte and the eight pixels for another plane in its high-order byte. Both bytes of this word must be accessed together.

Video memory holds 128 columns, each 256 scan lines deep. Because there are only 200 scan lines down a display screen and at most 80 columns across it, only 16,000 words of video memory can be mapped to the screen at one time (in the case of an 80-column display). The remaining 16,768 words of the 32k-word video memory do not map to a visible location and are not displayed.

Software identifies the visible portion of video memory by loading the Scroll Register with the encoded column and scan line coordinates of the byte that is to be displayed in the upper left corner of the screen, the byte containing the eight pixels in memory plane 0 that are to be displayed at column 0 of scan line 0 on the screen. Named because changing its value "scrolls" the display window horizontally or vertically within video memory, the Scroll Register accepts only the six high-order bits of the 7-bit column number; therefore, the upper left corner of the display always corresponds to a video memory address that divides evenly by four. This means that even numbered columns in video memory must occupy even numbered columns on an 80-column display screen.

A Scroll Register value of EB00H positions the display "window" at the lowest video memory address. Incrementing the Scroll Register content by one scrolls the display window two character columns to the right (ie, the displayed text seems to shift two character columns to the left). After 24 such increments, on an 80-column display, the window has scrolled 48 columns to the right. Incrementing the scroll register beyond EB18H again shifts the display window two columns to the right, but now it wraps around in video memory so that the rightmost display column contains characters that were originally on the leftmost edge of the display.

If the Scroll Register is again initialized to EB00H, increasing the Scroll Register content by 100H now scrolls the display window one scan line downward (ie, the displayed text seems to shift one scan line upward). After 9 such increases, the Scroll Register contains F400H and window has scrolled downward across one row of characters. Video memory accommodates 256 scan lines, only 200 of which are displayed on the screen; therefore, after 100H has been added to the original Scroll Register content a total of 31 times, the Scroll Register contains 0A00H. Increasing the Scroll Register beyond 0A00H again shifts the display window downward, but now it wraps around in video memory so that the bottom scan line on the display contains pixels that were originally on the top edge of the display.

2.13 Z80 Option Board 8248

The Z80 Option board is used for applications where an eight-bit computer program is to be run on the 16-bit PC operating system. The Z80 Option contains a Z80A microprocessor chip operating at 4MHz, 64K bytes of parity-checked DRAM memory, discrete refresh circuitry for on-board memory, a Counter Timer Controller (CTC) device for interrupt priority, bus arbitration circuitry, and interface logic for the 8086 system bus. Each processor (on-board Z80A or 8086 CPU) can execute independently and share access to the on-board memory.

The Z80 Option board (CP/M-80) can be installed in any available option slot within the PC and does not require any external connections. NOTE: CP/M Emulation requires that the CP/M file to be executed resides on the same diskette as the emulation software.

The Z80 microprocessor CPU is the main processor for CP/M emulation. The Z80 CPU systems clock is the 4 MHz clock from the PC system bus denoted 4CLK. The Z80 operates independently of and can be disabled by the 8086 CPU device. The Z80 scheme is based on Bus Request/Bus Acknowledge cycle. That is when a Bus Request is generated by the 8086 (Bus Request is recognized at the end of the current machine cycle), the Z80 forces its address bus, data bus, and control signals to a high impedance state so the 8086 can control these lines. The Z80 will output an active low Bus Acknowledge signal indicating that the 8086 now has control over these lines.

The Z80 is initialized to a known state on power up by the low-active RESET signal. This signal causes the Z80 to execute NOP instructions allowing the 8086 CPU total access to the memory array. A software reset of the Z80 can be accomplished by writing to port 1xFCH. This pulse is extended to 2.5 msec and affects the circuitry the same as the power-on Reset. The 8086 CPU can also reset the Z80 so that it starts from address 0000H. The 8086 output (extended 2.5 msec) disables the NOP forcing logic allowing the Z80 to begin executing instructions.

The Z80 address lines (denoted ZADx) are input to the Refresh Address Mux and to the Address Mux. The Refresh address generator is used to generate the addresses during memory refresh. The Address mux selects either the Z80A memory address or the 8086 memory address depending on which processor presently has complete access of the memory.

The Z80A data bus (denoted ZDATx) is presented to the Data Mux and the Counter Timer Controller (CTC) device. The Data Mux selects the data from the 8086 data bus or the Z80 data bus depending on which bus is selected. In order for the Z80 data bus to be selected, the Z80 access line (denoted ZACC) must be active low.

The CTC device is used for interrupt priority. The CTC device interfaces directly with the Z80A CPU and some addressing logic. The CTC device is used in the counter mode with the counter set to one. It provides two possible interrupts that are already prioritized.

All interrupts to the Z80 from the 8086 are Mode 2 type. The Z80 NMI interrupt is not used. Once an interrupt is accepted, the Z80A generates a special M1 interrupt acknowledge cycle indicating that the interrupting device (CTC) can place an 8-bit vector onto the data bus. During this time the CPU automatically adds two Wait states to the cycle. The Z80A Input/Output (I/O) ports are shown in Table 2-14.

When the Z80 CPU has control of the memory, the Z80 provides the control signals required for refresh, read operations, write operations, and the request signals. These signals are buffered by circuitry on board.

The NOP circuitry is enabled in one of three ways; Parity Error Z80 (PARZ80), Parity Error 8086 (PAR86), and Reset. When enabled, the NOP circuitry forces NOP instructions onto the Z80 data bus ($ZDAT_{7-0} = 0$). The NOP is active for one instruction fetch cycle of the Z80 (four T states). The NOP Forcing logic is cleared by a CLRNOP signal generated by a retriggerable monostable multivibrator that is activated by an 8086 output instruction.

Table 2-14. Z80A I/O Ports

PORT	DESCRIPTION
0DH	Output. D7-D0 = 01H for compatibility with Local Comm. Option.
5C-5DH	Input. Read CTC Channels 1 and 2 Down Counters Contents.
5C-5DH	Output. CTC Channels 1 and 2 set. D7 - D0 equals Control, Time constant value and/or interrupt vector.
60-6FH	Output. Generates interrupt 1 to 8086 CPU. D7 - D0 don't care.
70-7FH	Output. Generates interrupt 1 to 8086 CPU. D7 - D0 don't care.

All interrupts to the 8086 CPU are latched and deciphered to determine the interrupt priority level (IRQx). Any one of six levels out of eight total are possible. Selecting IRQ0 and IRQ1 (the two interrupt levels not possible) disables interrupts from this board to the 8086. A Clear Interrupt port resets the latch after the interrupt is serviced.

It is possible that the Z80 would send two interrupts before the 8086 CPU processed one. Under this condition the second interrupt would be missed. To prevent this, the 8086 writes its status into memory during the interrupt service routines. The Z80 CPU reads the 8086 status before sending an interrupt to determine if the 8086 is available. If the 8086 is busy, the Z80 polls the 8086's status until the 8086 is not busy. Table 2-15 contains the 8086 Input/Output (I/O) ports.

The Data Mux selects either the data from the Z80 or the 8086 CPU. In order for the data from the Z80 to be selected, the signal ZACC must be active high. In order for data from the 8086 to be selected, the signal IACC must be active high. 8086 word access to memory is completed in two consecutive operations, each having eight bits of data. After a Power-On reset or a Soft Reset, the NOP forcing Logic is enabled forcing NOPs onto the Z80 data bus. The 8086 has complete control of memory and could load it with Z80 program code. Once the access is completed, the NOP Forcing logic is disabled and the Z80 is reset to address 0000H. Now the Z80 CPU starts executing the program from that address.

Each processor provides the control signals required for memory access. The memory is accessed on a first come first serve basis. If the 8086 has access of the memory, the Z80 is forced into Wait states. When the Z80 has access of the memory, the 8086 will wait for a maximum of seven additional Z80 T-states before it can access memory.

Table 2-15. 8086 I/O Ports LSB Only

PORT	DESCRIPTION
1x92H	An 8086 output that performs a multitude of functions. The bit assignments are as follows:
0	Don't Care
1	Set to one for compatibility with Local Comm. Option.
2	Z80 Bus Acknowledge Mode. When set to zero allows the Z80 to Execute instructions. When set to one stops Z80 by forcing Bus Request Low.
3	Force Parity Error. Set to one forces parity error on either access. Set to zero allows correct parity operation.
4	Parity Mask. Set to one denotes 8086 parity error does not affect Z80. Set to zero 8086 parity error forces NOPs to Z80.
7, 6, 5	8086 Interrupt Priority level select. D7 D6 D5 0 0 0 No interrupt to 8086 0 0 1 No interrupt to 8086 0 1 0 Select IRQ2 0 1 1 Select IRQ3 1 0 0 Select IRQ4 1 0 1 Select IRQ5 1 1 0 Select IRQ6 1 1 1 Select IRQ7
1x96H	Interrupts Z80 on CTC Channel 0 (Output).
1x98H	Interrupts Z80 on CTC Channel 1 (Output).
1xA8H	Bits D7-D0 set to equal 68H for compatibility with Local Comm. Option (Output).
1xAAH	Clears interrupts from Z80 (Output). Bit Assignment as follows: D7-D3 don't care. NOTE: This port is the same as Port 1xBxH. D2 D1 D0 0 1 1 Clear Z80 Parity Error Interrupt 1 0 1 Clear Interrupt 1 to 8086 1 1 0 Clear Interrupt 2 to 8086
1xB0H - 1xBFH	I/O Error Status Register (Input). Bit assignments are as follows: D7-D2, D0 don't care. NOTE: This port is the same as Port 1xECH. D1 set to one denotes 8086 parity error occurred. D1 set to zero denotes no 8086 parity error.

Table 2-15. 8086 I/O Ports LSB Only (Cont'd)

PORT	DESCRIPTION
1xC0H - 1xCFH	Option Board Memory Disable (Output). Bit assignments are as follows:
0	Set to one enables option memory onto 8086 bus. Set to zero disables option memory to 8086 bus.
3, 2, 1	Don't Care.
7, 6, 5, 4	Bits D7-D4 correspond to 8086 address bits A19-A16 respectively for memory mapping.
1xD0H - 1xDFH	Z80 Restart and disable the NOP forcing hardware (Output). Bits D7-D0 don't care.
1xECH	Interrupt Status Register (Input). Bit assignments as follows: NOTE: This port returns same data as 1xBxH.
2, 1, 0	Don't Care
3	Set to one denotes Z80 Parity error has occurred. Set to zero denotes no Z80 Parity error pending.
4	Don't Care.
5	Set to one denotes interrupt 1 from Z80. Set to zero denotes no interrupt 1 pending.
6	Set to one denotes interrupt 2 from Z80. Set to zero denotes no interrupt 2 pending.
7	Don't care.
1xFCH	Software reset (Output). D7-D0 don't care.
1xFEH	Option ID Number register (Input). Bit assignments as follows:
6-0 = 39H	Option ID Code.
7	Pending interrupt to 8086.

The memory array consists of nine 64k bit dynamic RAMs. Eight RAMs are use for data storage and the ninth RAM stores the parity bit. Parity is assigned during write to memory operations and checked during memory read operations. Therefore a write to memory must be performed before a memory read in order to initialize the parity data.

If a parity error occurs during an 8086 access, the parity error activates the low active I/O ERROR (8086 NMI Interrupt). This error shuts down the Z80 by forcing NOP instructions onto its data bus unless PMASK is active.

If a Z80 Parity Error occurs, the NOP Forcing hardware is activated relinquishing control of the memory to the 8086. An interrupt to the 8086 is generated and a bit in the Interrupt Status register is set indicating a Z80 parity error has occurred.

Note that the inclusion of the parity generator/checker circuit improves the integrity of the data, however; if an even number of incorrect data bits are checked then no error will occur.

Discrete refresh circuitry is used on-board since the Z80 can be held in the Bus Acknowledge state longer than the allowable refresh period. The 4MHz clock (4CLK) is divided down to generate an output every 8 microseconds. This 8 uS signal is used for refresh request and to increment the address counter so that 256 addresses will be generated in the refresh time frame.

One point to remember is that the 64K of memory located on the Z80 Option board can be accessed by the 8086 in its normal memory addressing mode. The 8086 CPU can turn off the Z80 CPU and the memory can be used as part of the systems expanded memory.

2.14 Local Communications Option

The Local Communications Option consist of a two board set; a DATALINK Board (WLI No. 210-8245) and a CPU Board (WLI No. 210-8246). These boards are interconnected via a ribbon cable, part number 220-3281. The Local Communications option can be installed in any two adjacent motherboard connectors. Included with this option is the software diskette which contains the software required for emulation of VS, OIS, and Alliance systems. The Local Communications option allows the PC to perform as a workstation on any of these systems. With this ability, the PC has access to the files, data, and programs available on the host system.

The Local Communications option is cable connected to the host system by a dual coaxial cable and terminated by a BNC and a TNC connector located on the Datalink board (8245).

The Datalink provides a means of local communication between the emulator board and an OIS/VS master. The link communicates though use of an 11 bit serial data stream used in an asynchronous fashion. This data stream consist of 1 start bit, 8 bits of data (MSB first), 1 parity bit (even), and one stop bit. The Local Comm. Option can perform 1 byte read, 1 byte write, 256 byte read, 256 byte write operations, slave restarts and status checks. Each of these functions will be further discussed later in the text.

The discussion of the Local Communications option will include the theory of operation of each of the the two boards and the interaction between this option and the PC system.

2.14.1 CPU Board 8246

The CPU board contains the following logic circuitry:

- o Z80A CPU with clock and interface circuitry
- o 8086 Bus Interface and I/O Control Circuitry
- o Interrupt Circuitry
- o Keyboard Simulation Logic

2.14.1.1 Z80A CPU, Clock and Interface Circuitry

The Z80 microprocessor CPU is the main data processor associated with the current workstation emulation. The Z80 CPU is able to communicate with the VS/OIS master via the use of a register in the Emulators Main memory. This register is frequently polled by the master via the datalink board. All processing is controlled by this Z80 with the exception of the handling of the keyboard and CRT display hardware which is controlled by the 8086.

The Z80 CPU systems clock is the 4 MHz clock from the PC system bus denoted 4CLK. All Z80 outputs are buffered and will impose only one TTL load upon the CPU.

The Z80 is initialized to a known state on power up by the low-active RESET signal. This signal causes the Z80 to execute NOP instructions allowing the 8086 CPU total access of the memory array. A software reset of the Z80 can be accomplished by writing to port 1x92H. This signal affects the circuitry the same as the power-on Reset. The 8086 CPU can also reset the Z80 so that it starts from address 0000H. The 8086 output (OUT 1xD0) disables the NOP forcing logic allowing the Z80 to begin executing instructions.

2.14.1.2 8086 Bus Interface and I/O Control Circuitry

The 8086 bus to Z80 bus interface circuitry is buffered on-board to impose only one TTL load on the 8086. An 8086 access to emulator memory can occur by either an odd byte, even byte, or word basis, where an I/O access must be by an even byte basis. (8086 data bits D0-D7 are only acknowledged).

The 8086 determines the I/O device type located on its bus by polling its I/O slots and reading the device code. The 8086 reads the ID Code through an "IN 1xFE". A 38H returned on data lines D6-D0 notifies the 8086 of the device type. In this instance a 38H denotes local communications (928).

The 8086 I/O control circuitry provides four unidirectional general purpose outputs to the Z80 from the 8086 and four general purpose inputs from the Z80 to the 8086. Each Output/Input is eight bits wide and has a one to one relationship between processor data bits on the data bus D0-D7.

The I/O ports corresponding to the Z80 and 8086 are shown below.

Z80 OUTPUT	8086 INPUT	8086 OUTPUT	Z80 INPUT
OUT 58	IN 1xE4	OUT 1xA0	IN 58
OUT 59	IN 1xE6	OUT 1xA2	IN 59
OUT 5A	IN 1xE8	OUT 1xA4	IN 5A
OUT 5B	IN 1xEA	OUT 1xA6	IN 5B

The following tables contain the Input/Output commands for the Z80 and the 8086 CPU device.

Table 2-16. Z80 Input Commands

PORT	DEVICE	FUNCTION
00	KEYBOARD	Read Keystroke Data. Bit D7=1 denotes Shift Key active. Bits D6-D0 denotes keyboard data (MSB-LSB).
06	KEYBOARD	Uppercase Only Sense Line. Uppercase never enabled. D0=0 always.
07	SLAVE TYPE REGISTER 1	Slave Type Setting for Z80.
08	SLAVE TYPE REGISTER 2	Slave Type Setting for Z80.
0F	ZEBUG	NOT USED. RESERVED FOR ZEBUG.
58	GEN. INPUT REGISTER 1	Input Register Set by 8086 and Read by Z80. Bits D7-D0 defined by application.
59	GEN. INPUT REGISTER 2	Input Register Set by 8086 and Read by Z80. Bits D7-D0 defined by application.
5A	GEN. INPUT REGISTER 3	Input Register Set by 8086 and Read by Z80. Bits D7-D0 defined by application.
5B	GEN. INPUT REGISTER 4	Input Register Set by 8086 and Read by Z80. Bits D7-D0 defined by application.
5C	CTC	Z80 CTC Channel 0 Down Count Value.
5D	CTC	Z80 CTC Channel 1 Down Count Value.
5E	CTC	Z80 CTC Channel 2 Down Count Value.
5F	CTC	Z80 CTC Channel 3 Down Count Value.

Table 2-17. Z80 Output Commands

PORT	DEVICE	FUNCTION
00	KEYBOARD	Sound Keyboard CLICK. Interrupt to 8086.
01	KEYBOARD	Sound Keyboard BEEP. Interrupt to 8086.
02	CRT	CRT Horizontal Scroll Start Location. Interrupt to 8086. Bits D7-D0 = Column Number.
05	CRT MAP IN	CRT Mapping Bit for Upper 16K of Z80 Memory. Bit D0=0 denotes top 16K is CRT Memory. Bit D0=1 denotes top 16K is Main Memory.
06	CRT SET	Select Primary CRT Character Set. Interrupt to 8086.
07	CRT SET	Select Secondary CRT Character Set. Interrupt to 8086.
0D	Z80 MODE INTERRUPT	Select Z80 Hardware Interrupt Mode. D0=0 denotes interrupt mode 0. D0=1 denotes interrupt mode 2.
0E	DIAGNOSTICS	Parity Generation and Checking Control. D0=0 denotes all memory writes will generate correct parity. D0=1 denotes all memory writes will generate bad parity. D1=0 denotes Z80 will continue code execution on any detected parity error. D1=1 denotes Z80 will stop current code execution on detected parity error.
0F	ZEBUG	NOT TO BE USED.
58	GEN. OUTPUT REGISTER 1	Output Register Set by Z80 and Read by 8086. D7-D0 defined by application.
59	GEN. OUTPUT REGISTER 2	Output Register Set by Z80 and Read by 8086. D7-D0 defined by application.
5A	GEN. OUTPUT REGISTER 3	Output Register Set by Z80 and Read by 8086. D7-D0 defined by application.
5B	GEN. OUTPUT REGISTER 4	Output Register Set by Z80 and Read by 8086. D7-D0 defined by application.
5C	Z80 CTC	Z80 CTC Command/Data for Channel 0. D7-D0 contains command information, count data, or interrupt vector.
5D	Z80 CTC	Z80 CTC Command/Data for Channel 1. D7-D0 contains command information, count data, or interrupt vector.

Table 2-17. Z80 Output Commands (Cont'd)

PORT	DEVICE	FUNCTION
5E	Z80 CTC	Z80 CTC Command/Data for Channel 2. D7-D0 contains command information, count data, or interrupt vector.
5F	Z80 CTC	Z80 CTC Command/Data for Channel 3. D7-D0 contains command information, count data, or interrupt vector.
60-6F	GEN. PUR. INTERRUPT 1	General Purpose Interrupt to 8086.
70-7F	GEN. PUR. INTERRUPT 2	General Purpose Interrupt to 8086.

Table 2-18. 8086 Input Commands

PORT	DEVICE	FUNCTION
1x80 - 1x8F	DIAGNOSTICS	Selected Status Register for 2001 Datalink. Register — Function 0 — UART Data Buffer Data 1 — Turn Around Time 1 2 — No Data Timeout Counter 4 — Datalink Instruction 5 — Turn Around Time 2 6 — Address Low Count 7 — Internal Status Byte Data
1xB0 - 1xBF	MISC. INPUTS	Local/Remote Switch. D0=0 denotes Local Mode Selected D0=1 denotes Remote Mode Selected 8086 Parity Status. D1=1 denotes 8086 parity error has occurred Z80 Board Status. D7=0 denotes Z80 board is present D7=1 denotes Datalink board operation
1xE0	MISC. STATUS REG.	Primary Vs. Secondary CRT Character Set. D0=0 denotes Primary Set selected D0=1 denotes Secondary Set selected Z80 CRT Memory Write Status. D1=0 denotes CRT memory has been written D1=1 denotes no CRT memory write occurred Z80 Parity Error Status D4=0 denotes Z80 parity error occurred D4=1 no Z80 parity error occurred

Table 2-18. 8086 Input Commands (Cont'd)

PORT	DEVICE	FUNCTION
1xE2	CRT SCROLL LOCATION	CRT Horizontal Scroll Start Location. D7-D0 holds display column start location
1xE4	GEN. INPUT REGISTER 1	Input Register Set by Z80 and Read by 8086. D7-D0 defined by application.
1xE6	GEN. INPUT REGISTER 2	Input Register Set by Z80 and Read by 8086. D7-D0 defined by application.
1xE8	GEN. INPUT REGISTER 3	Input Register Set by Z80 and Read by 8086. D7-D0 defined by application.
1xEA	GEN. INPUT REGISTER 4	Input Register Set by Z80 and Read by 8086. D7-D0 defined by application.
1xEC	8086 INT. STATUS REG.	Interrupt Status Register. Interrupt caused by any of the following: D0=1 Keyboard Click D1=1 Keyboard Beep D2=1 Z80 CRT Memory Write D3=1 Z80 Parity Error Detected D4=1 Horizontal Scroll Change D5=1 General Interrupt 1 from Z80 D6=1 General Interrupt 2 from Z80 D7=1 Primary Vs. Secondary CRT Set change
1xEE	CRT SCREEN SEC.WRITTEN	Data Bits=1 depict which four row section of the CRT screen was written into by the Z80. D0=1 Rows 0-3 D1=1 Rows 4-7 D2=1 Rows 8-11 D3=1 Rows 12-15 D4=1 Rows 16-19 D5=1 Rows 20-23 D6=1 Rows 24-27 D7=0 Always
1xF0 - 1xFF	BOARD ID INTERRUPT STATUS	Board ID Code and Interrupt Status Bit. D7=1 denotes interrupt from this board D6-D0=38 denotes board ID code

Table 2-19. 8086 Output Commands

PORT	DEVICE	FUNCTION
1x80 - 1x8F	DATALINK STATUS CONT. AND BIT SEL.	Datalink Control Bit. D0=0 denotes force Not Ready on 2001 chip D0=1 denotes remove Not Ready from 2001 chip Datalink Register Select D3 D2 D1 0 0 0 UART Data Buffer 0 0 1 Turn Around Time 1 0 1 0 Timeout Counter 0 1 1 Undefined 1 0 0 Instruction Register 1 0 1 Turn Around Time 2 1 1 0 Address Low Counter 1 1 1 Internal Link Status Byte Datalink Definition Bits. D7-D4 Correspond to settings for Datalink Switch
1x92	Z80/PARITY CONTROL	Z80 Processor and Parity Control. D0 Not Used D1=0 denotes force Z80 into Reset condition D2=1 denotes force Z80 into DMA condition D3=0 Allow all writes to emulator memory to have correct memory D3=1 Force all writes to emulator memory to have incorrect parity D4=0 Allow Z80 code execution to be stopped by Z80 upon detection of emulator parity error D4=1 Override Z80 Stop on Parity Error selection
	INTERRUPT LEVEL SEL.	8086 Interrupt Level Select Bits. D7 D6 D5 0 0 0 No Interrupt issued to 8086 0 0 1 No Interrupt issued to 8086 0 1 0 Allow IRQ2 Interrupt 0 1 1 Allow IRQ3 Interrupt 1 0 0 Allow IRQ4 Interrupt 1 0 1 Allow IRQ5 Interrupt 1 1 0 Allow IRQ6 Interrupt 1 1 1 Allow IRQ7 Interrupt
1x94	KEYBOARD DATA	Keyboard Data to Z80. D7=1 denotes Shift Key active. D6-D0 denotes Key Data (MSB to LSB)
1x96	Z80 INTERRUPT	Initiate Mode 2 Interrupt to Z80. Activate highest priority Mode 2. Interrupt to Z80 through CTC Channel 0

Table 2-19. 8086 Output Commands (Cont'd)

PORT	DEVICE	FUNCTION
1x98	Z80 INTERRUPT	Initiate Mode 2 Interrupt to Z80. Activate second highest priority Mode 2. Interrupt to Z80 through CTC Channel 1
1x9A	Z80 INTERRUPT	Initiate Mode 2 Interrupt to Z80. Activate second lowest priority Mode 2. Interrupt to Z80 through CTC Channel 2
1x9C	Z80 INTERRUPT	Initiate Mode 2 Interrupt to Z80. Activate lowest priority Mode 2. Interrupt to Z80 through CTC Channel 3
1x9E	CLEAR CRT SEC. WRITE	Setting data bits D2-D0 to a specific code will clear the associated CRT section. D2 D1 D0 — Clear Status on Rows 0 0 0 — 0-3 0 0 1 — 4-7 0 1 0 — 8-11 0 1 1 — 12-15 1 0 0 — 16-19 1 0 1 — 20-23 1 1 0 — 24-27
1xA0	GEN. OUTPUT REGISTER 1	Output Register Set by 8086 and Read by Z80. D7-D0 defined by application.
1xA2	GEN. OUTPUT REGISTER 2	Output Register Set by 8086 and Read by Z80. D7-D0 defined by application.
1xA4	GEN. OUTPUT REGISTER 3	Output Register Set by 8086 and Read by Z80. D7-D0 defined by application.
1xA6	GEN. OUTPUT REGISTER 4	Output Register Set by 8086 and Read by Z80. D7-D0 defined by application.
1xA8	8086 INT. MASK REG.	Interrupt Mask Register. Setting the associated bit will cause the following interrupt to be enabled. D0 = Keyboard Click D1 = Keyboard Beep D2 = CRT Write D3 = Parity Error D4 = Horizontal Scroll Location D5 = General Interrupt 1 D6 = General Interrupt 2 D7 = Primary Vs. Secondary CRT Set

Table 2-19. 8086 Output Commands (Cont'd)

PORT	DEVICE	FUNCTION
1xAA	8086 INTERRUPT CLEAR CONTROL	Remove Device Interrupt Request. Issuing this OUT with associated data bits set will cause the associated interrupt condition to be reset. D2 D1 D0 0 0 0 Keyboard CLICK 0 0 1 Keyboard BEEP 0 1 0 CRT Write 0 1 1 Parity Error 1 0 0 Horizontal Scroll Location 1 0 1 General Interrupt 1 1 1 0 General Interrupt 2 1 1 1 Primary Vs Secondary CRT Set
1xAC	WORKSTATION SLAVE TYPE REGISTER 1	Workstation Device Type Control Bits. Read by Z80 through an IN 07. D7-D0 correspond to PC system configuration.
1xAE	WORKSTATION SLAVE TYPE REGISTER 2	Workstation Device Type Control Bits. Read by Z80 through an IN 08. D7-D0 correspond to PC system configuration.
1xB0 - 1xBF	8086 PARITY CLEAR AND CRT MAP IN	D0=1 denotes Clear I/O ERROR condition D1=0 denotes Map In upper 16K as Emulator CRT memory D1=1 denotes Map In upper 16K as Emulator Main memory D2-D7 not used
1xC0 - 1xCF	OPTION BD. MEMORY ENABLING AND 8086 MEMORY MAP IN	Option Board Memory Enable. D0=0 denotes disable memory from 8086 bus D0=1 denotes enable memory from 8086 bus Mapping Bits for 8086 Memory Location D7-D4 corresponds to 8086 addresses A19-A16 respectively.
1xD0 - 1xDF	Z80 RESTART COMMAND	This output with any data pattern will cause the Z80 to receive a reset pulse that will clear the NOP generator and force the Z80 to begin executing its code at location 0000H.
1xF0 - 1xFF	OPTION BD. SOFTWARE RESET	This output with any data pattern will cause all circuitry on this board set to be conditioned as if a System Power On Reset had occurred.

2.14.1.3 Interrupt Circuitry

The 8086 CPU can interrupt the Z80 and the Z80 can interrupt the 8086. The Z80 handles interrupts in mode 0 or mode 2 depending on which interrupt is selected. The Z80 notifies the external hardware of the interrupt selected. This is accomplished by issuing an OUT 0D with D0 set to 0 for mode 0 or D0 set to 1 for mode 2.

The Z80A CTC device is used for interrupt priorities. The CTC device interfaces directly with the Z80A CPU with no other logic being necessary. The CTC device provides four possible interrupts (0-3) that are already prioritized (interrupt 0 highest, interrupt 3 lowest). The CTC device can be read at anytime by the Z80A CPU to determine if an interrupt is pending and the type of interrupt. Four independent channels are available to the 8086 to interrupt the Z80. These channels will only be active when Mode 2 type interrupt operations are selected. Each of these channels are presented to the CTC device which is programmed for down counting with each register preset to 1.

When the 8086 issues an interrupt to one of these registers, a Z80 interrupt will be generated. The Z80 responds by issuing an interrupt acknowledge and accepts and executes the interrupt routine. The correspondence between the 8086 outputs and the CTC channel interrupts are as follows:

8086 OUTPUT	CTC CHANNEL INTERRUPT INVOKED
1x96	0
1x98	1
1x9A	2
1x9C	3

Only one mode 0 interrupt is allowed from the 8086 to the Z80. This interrupt is associated with the keyboard and is explained in paragraph 2.14.1.4 Keyboard Simulation Logic.

Z80 interrupts to the 8086 can occur from any of eight possible means. Two interrupts are general purpose interrupts and the other six interrupts are Keyboard Click, Keyboard Beep, CRT Memory Write, CRT Horizontal Scroll Location Change, Emulator Memory Parity Error, and Primary/Secondary CRT Character Set Selection. See appropriate table for definitions.

The 8086 handles interrupts from the Z80 in the following manner. Interrupts occurring from the emulator board will activate a preprogrammed interrupt request line of the 8086. When the 8086 acknowledges the interrupt request, the 8086 will perform an interrupt handling routine to decipher the interrupting device. This is performed by the 8086 polling ID Code registers and reading bit D7. If bit D7 is set to one, than that device is requesting the interrupt service.

The 8086 interrogates the emulator board ID code through an IN 1xF0. Upon recognizing the emulator board interrupt request, the 8086 will read the interrupt device register with an IN 1xEC and determine by the bits set to which emulator device generated the request. The 8086 will then issue an OUT 1xAA along with a data command to the interrupting device, clearing the interrupt request. Now the 8086 will service the interrupt.

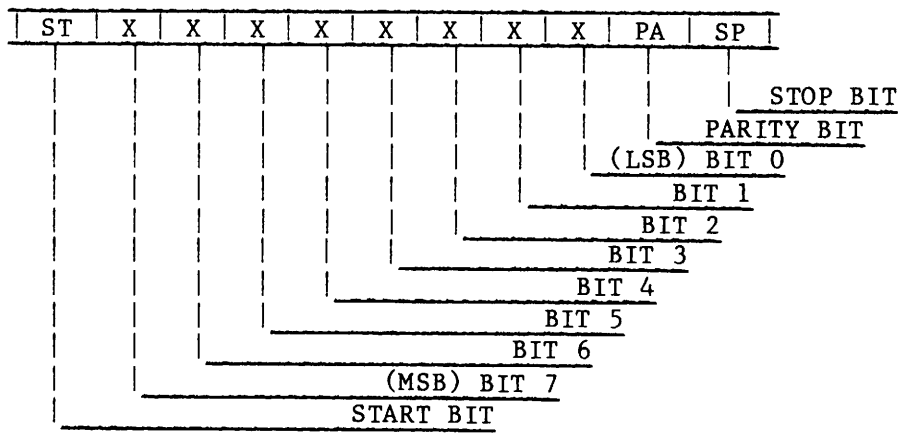
2.14.1.4 KEYBOARD SIMULATION LOGIC

The emulation of the workstation keyboard occurs as follows. When a key is depressed on the keyboard, the data will be read and translated into the appropriate code by the 8086. The Z80 is then interrupted by an OUT 1x94 with this data. This will cause a mode 0 interrupt to the Z80. The Z80 (if not busy) will acknowledge the interrupt and a C7 will be forced onto the data bus for the next Z80 instruction. This instruction generates a restart of the Z80 at the keyboard buffer handler entry point. This process is repeated for each keyboard key depressed.

The Z80 controls the Key Clicks and Beeps. A Click is generated by the Z80 issuing an OUT 00. A Beep is generated by the Z80 issuing an OUT 01. Both of these conditions will interrupt the 8086.

2.14.2 DATALINK 8245

The Datalink board 8245 is the second board of the two board option. The Datalink circuitry provides the means of local communication between the emulator board and an OIS or VS master. The link communicates through the use of an 11 bit serial data stream (asynchronous). The data stream consists of the following:



The Datalink can perform six functions, these are:

STATUS READ — The Status Read is a method the master uses to interrogate a slave. Eight bits of information are transmitted from the slave starting with the least significant bit first. The scheme is as follows

- D0 IPL STATUS, a high indicates that the slave is just powered on.
- D1 LINE ERROR, a high indicates to the master that the slave has detected a parity error during a transmission from the master to the slave.
- D2 MAIN PARITY ERROR, a high indicates to the master that the main emulator memory has detected a parity error.
- D3 SYSTEM POWER ON, always a high, it indicates to the master that the slave has power applied to it.
- D4-7 HARDWARE DEVICE TYPE, define the type of slave device which is connected to the datalink.

1 BYTE READ — The master has the ability to read any location in main memory. The master supplies the address of the location and it is read via DMA paths.

1 BYTE WRITE — The master has the ability to write any location in main memory. The master supplies the address of the location and it is written via DMA paths.

256 BYTE READ — The master has the ability to read a page of main memory. It supplies the starting address location and the Datalink circuitry automatically increments until a page of memory has been read using the DMA path. During this DMA transfer, the CPU is locked out.

256 BYTE WRITE — The master has the ability to write a page of main memory. It supplies the starting and the Data. The address is automatically incremented. During this DMA transfer, the CPU is locked out.

RESTART — The Datalink has the capability of restarting the slave. The restart resets the Z80 and removes the NOP bus condition if it exists.

The following logic is located on the Datalink PCA. Each is discussed individually is the preceding text.

- o 64K Triple Ported Main Memory
- o 16K CRT Memory
- o Memory Arbitration and Refresh logic
- o 928 Datalink Interface

2.14.2.1 64K TRIPLE-PORTED MAIN MEMORY

The Main Memory consists of nine 64K x 1 bit dynamic RAMS that are shared between the Z80 CPU, 8086 CPU, and the Datalink. Eight bits of the memory are used for program/data storage with the ninth bit used for parity storage. The memory is tripled ported where two ports co-exist between the Z80 CPU and the Datalink and one port (the third port) is for the 8086/refresh circuitry.

Memory access occurs when either an 8086 memory request or a Z80/Data Link memory request is received by the memory controller. The memory controller grants memory access allowing memory read or memory write operations.

Parity is checked on the Main Memory any time during a data read operation occurs from the Z80, 8086 , or Datalink. During normal operations, correct parity is written on all memory writes from these devices. The Z80 has the ability to select Stop On Parity in the event of a parity error. Circuitry on-board will then force NOPs onto the Z80 data bus. The master will also be notified of the parity error condition via an input to the Datalink status register. The 8086 is also notified of this condition.

During 8086 memory access, if a parity error is detected the I/O ERROR flag will be activated generating a NMI interrupt. THe 8086 can determine if the I/O ERROR was generated by this option by performing an IN 1xB0 and interrogating bit D1. If D1=1, the I/O ERROR was generated from this board. The error condition is cleared by issuing an OUT 1xB0 with data bit D0=1.

During Z80 memory access, if a parity error is detected an interrupt is generated to the 8086. The Z80 will be forced into executing NOP instructions until a restart is issued from either the 8086 or the Datalink.

Circuitry on-board allows 16 bit data read/write operations from the 8086. Note that the Z80 and Datalink are only 8 bit operations. The lower 8 bits of the data record are written/read first followed by the upper 8 bits.

2.14.2.2 CRT MEMORY

The CRT memory consists of nine 16K x 1 Bit dynamic RAMS. The CRT memory is dual ported and shared between the Z80 CPU and the 8086. Eight bits of this memory are used for CRT character storage or attribute storage with the ninth bit used for parity storage/checking. The Datalink does not have access to this memory.

Data access to this memory when an 8086 or a Z80 memory request is received by the memory controller. The memory controller grants access to the requesting device and allows memory read or write operations to be performed.

The Z80 addresses the CRT memory for read or write operations on a 24 row by 160 column basis using the high order byte then the low order byte. The addressing scheme is shown on the preceding page.

High Order Z80 Address (ROW)

A15	A14	A13	A12	A11	A10	A9	A8
1	1	Z	X	X	X	X	X

Z=0 Denotes Attribute Memory Selected
Z=1 Denotes Character Memory Selected
XXXXX = Binary Row Address (0 to 23)

Low Order Z80 Address (COLUMN)

A7	A6	A5	A4	A3	A2	A1	A0
Y	Y	Y	Y	Y	Y	Y	Y

YYYYYYYY = Binary Column Address (0 to 159)

When a 8086 performs a read or write to the CRT memory, the lower 16 bits (A15-A0) correspond to the ROW/COLUMN definition as describe for the Z80. 8086 addresses are always by EVEN word access. As with the Z80 address, the attribute memory select and character memory select differ soley by the "Z" bit. The Z80 must change the location on each memory write. However, 8086 memory writes allow both character and attribute to be read through one access.

The attribute data as defined for the Z80 is in the following format:

D7=0 denotes Low Intensity
D7=1 denotes High Intensity

D6=0 denotes Blink Off
D6=1 denotes Blink On

D5=0 denotes Cursor Off
D5=1 denotes Cursor ON

D4=0 denotes No Underline
D4=1 denotes Underline

D3, D2, D1, and D0 are not defined and can be any value.

The 8086 displays information by the following means: The 8086 is notified that a display update is required by receiving an interrupt. This interrupt could be generated in one of two ways. Either a CTC time-out based on a length of time or through notification of a CRT memory write by the emulator hardware. Once the interrupt is received, the software has two options. One is to read the entire displayable character area a word at a time. It would then write to the medium resolution board the new character/attribute word to be displayed on the CRT screen. The other option is to read a hardware port which indicates the four row section of the visible screen that was changed by the Z80. This is performed by a read IN 1xEE. The software then has to update the rows indicated by the hardware port by performing the character/attribute write to the medium resolution board as previously stated earlier.

2.14.2.3 MEMORY ARBITRATION AND REFRESH

The memory circuitry is independent of any the systems that can access it. The memory arbitration and refresh logic performs the following functions:

1) It monitors memory requests from the Datalink, Z80, and 8086/Refresh.

2) It arbitrates between requesting devices and grants access to the first requesting device.

3) It generates wait conditions to other devices that raise a memory request but were not granted immediate access.

4) The circuitry maps the appropriate address, data, and control signals onto its bus as well as generates its own memory sequence signals to properly read and write the data from and to memory.

5) Upon completion of a memory access, the next device requesting the bus is granted access. The previous device is locked out until other requesting devices have completed their access.

All memory refresh is done by discrete circuitry that creates a Refresh request every 8-10 microseconds. The refresh addresses are created by this circuitry.

2.14.2.4 928 DATALINK INTERFACE

The Datalink circuitry is designed around the 2001 datalink chip. The datalink is normally in the receive mode and will enter the transmit mode only on instruction from the master. The link communicates through the use of an 11 bit serial data stream (as previously discussed) at a bit rate of 4.275 MHz, resulting in a total time for each bit transferred of 2.57 microsecond. In order to provide this bit rate, a clock circuitry on-board consisting of a 17.1 MHz crystal is included. This clock is also divided down and used for the memory arbitration and sequence logic.

Located on the back panel of the Datalink board is a BNC and a TNC connector. These connectors interface the Local Comm. option to the host system. The BNC and TNC lines are phase shifted 180 degrees with an amplitude difference of .5 volts. This affords the host and Datalink to distinguish the data from transients on the line. The BNC/TNC connectors are driven by a dual differential line driver for transmitting the data stream. A dual differential receiver is used on the receive end to complete the link.

2.15 REMOTE TELECOMMUNICATIONS OPTION

The Professional Computer Remote Telecommunications option (RTC) provides the physical link interface for local data communications. Two controller boards form the basis of this family. One option board, 8232, provides a RS232-C interface (Domestic). The other option board, 8252, provides X.21 interface to a circuit switched, synchronous data network or a packet switched network.

The RTC option board can be installed in any option slot located within the PC. It may be cable-connected to a telephone network via a synchronous modem with auto-call, or through Wangnet Fixed Frequency Modem (FFM) to any Wangnet system. Both RTC options offer high-speed synchronous data communications plus all the functionality needed by the higher level network protocols. Included with the option board is the VS Remote Wangnet software.

The RTC PCA has an 8 position DIP switch denoted SW1 (refer to Figure 2-15 for switch location) that is set depending on the mode of operation used. The switch settings are discussed below.

		OFF (Zero)	ON (One)
[1]	Bit D0	Synchronous operation (LSB)	Asynchronous operation
[2]	Bit D1	Send serial data in NRZ mode	Select NRZI mode
[3]	Bit D2	Not Assigned	Select loop-on Power on
[4]	Bit D3	Not Assigned	Not Assigned
[5]	Bit D4	Set STRS to Mark	Set STRS to Space
[6]	Bit D5	Not Assigned	Not Assigned
[7]	Bit D6	Not Assigned	Not Assigned
[8]	Bit D7	Not Assigned (MSB)	Generates an 8086 interrupt request

These Switches are read by the Z80A CPU (located on board) by issuing an IN40. The Z80 Input/Output commands are further explained in this section. The default setting for all switches is zero.

Located on the RTC board is a RS232-C connector J5 and an Auto-Call connector J1. Figure 2-15 shows the connector locations and pin configurations. These connectors are defined as follows. The signals enclosed in brackets [ ] are EIA Mnemonic codes.

Table 2-20. RS232-C Connector (J5) Pin Assignments

Signal	I/O	Pin	Description
GND [AA]		1	Chassis Ground
TxD [BA]	O	2	Transmit Data
RxD [BB]	I	3	Receive Data
RTS [CA]	O	4	Request to Send
CTS [CB]	I	5	Clear to Send
DCB [CC]	I	6	Data Set Ready
+0V		7	Signal ground and common return
$\overline{\text{D}}$CA [CF]	I	8	Data Carrier Detect
INTBCLK	O	11	Interrupt B Clock
TXC [DB]	I	15	Transmit Clock
RXC [DD]	I	17	Receive Clock
[SCA]	O	19	Secondary Request to Send
DTR [CD]	O	20	Data Terminal Ready
RI [CE]	I	22	Ring Indicator
Pins 9, 10, 12-14, 16, 18, 21, 23-25 are unassigned.			

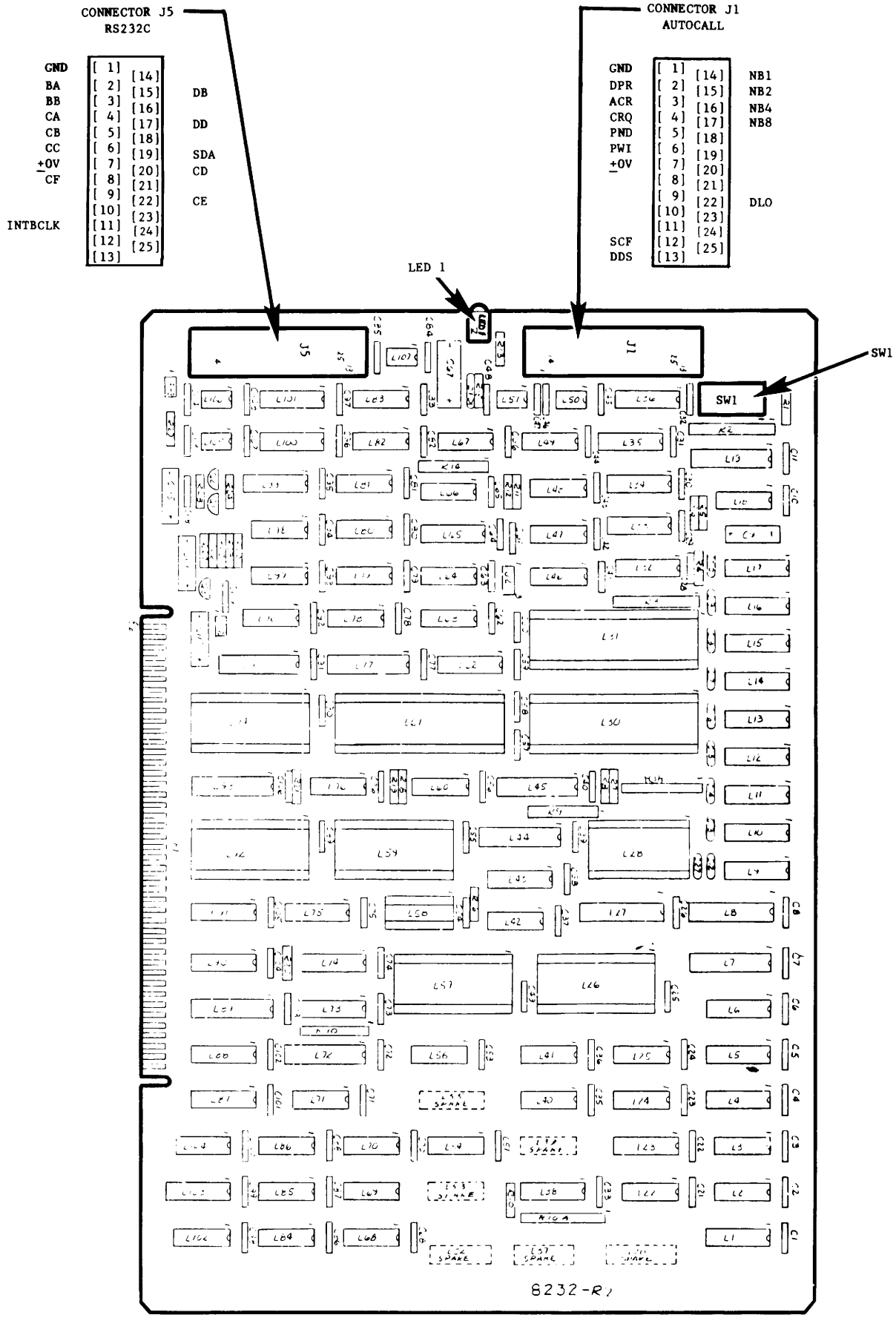


Figure 2-15. RTC PCA 8232 Connector Locations

Table 2-21. AutoCall Connector (J1) Pin Assignments

Signal	I/O	Pin	Description
GND		1	Chassis Ground
DPR	O	2	Digit Present
ACR	I	3	Abandon Call and Retry
CRQ	O	4	Call Request
PND	I	5	Present Next Digit
PWI	I	6	Power Indication
$\pm$OV		7	Signal Ground
$\overline{\text{COS}}$	I	13	Call Origination Status
NB1	O	14	Digit Bit 0
NB2	O	15	Digit Bit 1
NB4	O	16	Digit Bit 2
NB8	O	17	Digit Bit 3
DLO	I	22	Data Line Occupied

2.15.1 RTC Board Theory of Operation

Refer to the RTC Block diagram Figure 2-16 for the following discussion.

The RTC interface contains a Z80A CPU, a Serial data communications controller (SIO/2), a parallel bidirectional data port for communications and handshaking between the RTC and the 8086 CPU, 4K of Bootstrap PROM, 60K of Dynamic RAM for data storage and memory control signals. Each block is discussed separately.

The Z80A microprocessor is the main processor for remote telecommunications. The Z80 CPU system's clock is the 4 MHz clock from the PC system bus denoted 4CLK. The Z80 address bus (denoted ZADx) are presented to the Address Mux and the Z80 I/O Port Controller. The DMA Controller also generates memory addresses during DMA transfers.

A 256 by 1 bit static RAM contains a lookup table that determines whether any character received by SIO channel A is one of the special characters that can cause an interrupt request. The lookup table RAM receives its address from the 8-bit data bus and its data from the low-order Z80 address line (ZA0). When initializing the character recognition table, accumulator data identifies the lookup table entry while the Z80A executes either an OUT 30 to clear the entry addressed by the accumulator contents (and thereby request an interrupt whenever the corresponding character is recognized), or an OUT 31 to set that lookup table entry (and suppress interrupt requests when the corresponding character is recognized).

Two CTC devices are located on the RTC board, a primary CTC and a secondary CTC. The primary CTC device is used to generate Z80A interrupt requests when any of the four DMA channels completes a DMA transfer operation or when the character recognition logic encounters a special character. It also provides a programmable baud rate clock and performs general purpose counting or timing functions.

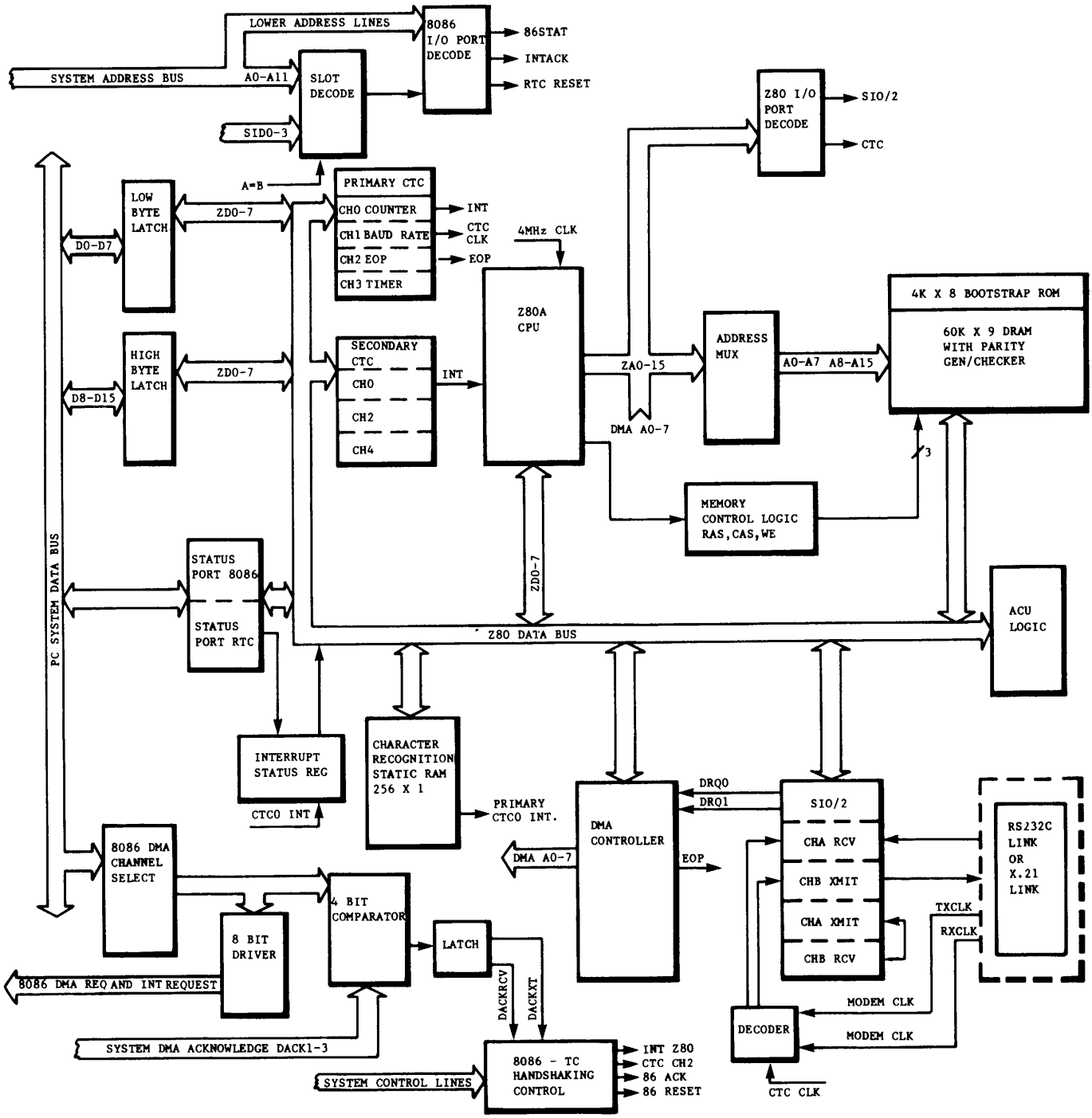


Figure 2-16. RTC Functional Block Diagram

The secondary CTC generates Z80A interrupt requests for the Inbound and Outbound Data Registers and the programmed interrupt request port. Thus, primary CTC events originate on the RTC board and secondary CTC events originate in the 8086.

Primary CTC channel 0 is programmed to operate in counter mode with an initial value of 1; it is used only to generate character recognition interrupt requests. Output from the character recognition lookup table is gated by DMA control logic and applied to the counter input of CTC channel 0 during DMA write cycles. An active input indicates that the last character received on SIO channel A was recognized as a special character. This decrements the channel 0 count to zero and triggers the character recognition interrupt request.

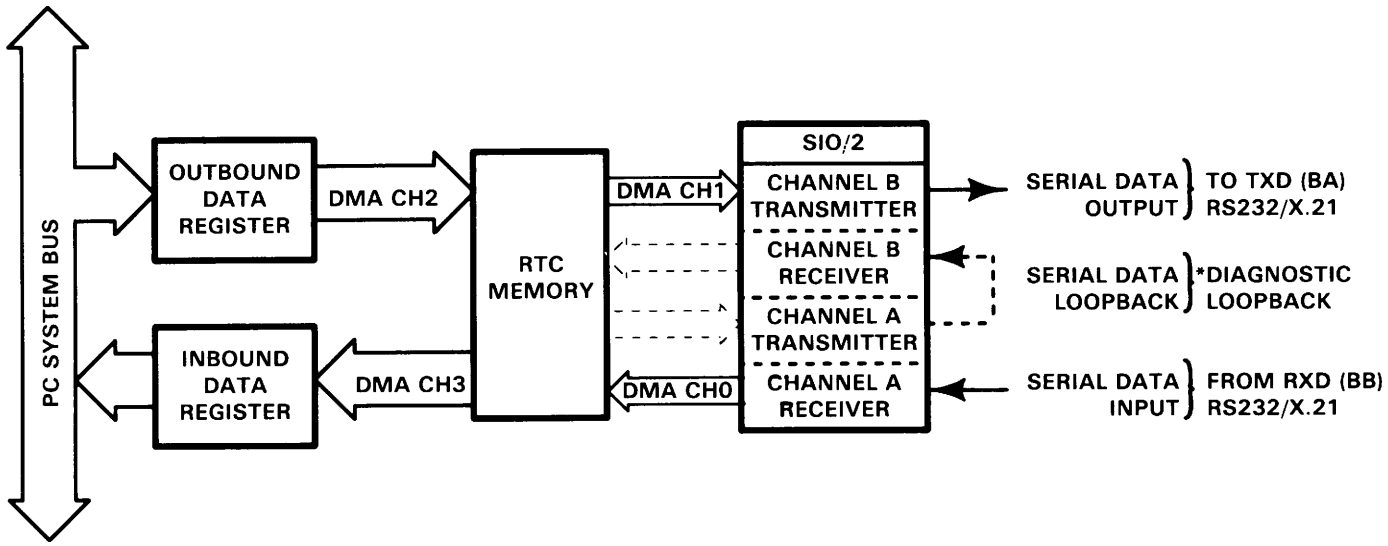
CTC channel 1 is the programmable baud rate generator. Operating as a timer, it produces the SIO channel A receiver clock and the SIO channel B transmitter clock, but only when the clock mode flipflop is cleared to select internal clock operation with an asynchronous modem. Optionally, CTC channel 1 can also generate an internal baud rate clock for loopback operation, an internal clock for CRC character generation, or a baud rate clock for synchronous or asynchronous null modem applications. When operating as a counter, CTC channel 1 tallies RS-232C transmitter clock pulses and generates a clock for checking flag characters under the SDLC or HDLC protocols.

CTC channel 2 receives End Of Process (EOP, low-active) signals from the DMA controller and generates DMA EOP interrupt requests. Like CTC channel 0, CTC channel 2 operates in counter mode with an initial count value of 1.

CTC channel 3 is available for use as a general purpose timer. In addition, channels 2 and 3 are connected in series to implement an extended timer with channel 3 as the high-order stage. The extended timer can be used for relatively lengthy timeouts or other special functions when DMA transfers are not required.

RTC memory consists of 4k bytes of EPROM for bootstrap loading and diagnostic programs, and 60k bytes of RAM. The EPROM occupies the lowest 4K bytes of address space. The RAM memory is organized as 9-bit memory with eight data bits and a parity bit. The RAM parity errors trigger a Z80A nonmaskable interrupt. The EPROM and the memory array uses I/O mapped port addressing.

The Serial Input/Output (SIO/2) device contains two independent full-duplex channels. Channel A receives input from the RS-232C or X.21 communication interface and transmits loopback output to SIO channel B. Channel B, in turn, transmits output to the appropriate communication interface and receives loopback input from channel A. The SIO/2 device converts outbound data from parallel to serial and sends it to the RS232C or X.21 interface connector. With inbound data, the SIO/2 converts the serial data from the communications interface to a parallel format and sends it to the RTC memory. The block diagram shown in Figure 2-17 demonstrates the inbound data path and the outbound data interface to the system bus.



*DIAGNOSTIC LOOPBACK REQUIRES LOOPBACK CONNECTOR
WLI 420-1040 RTC
WLI 421-0010 X.21

Figure 2-17. RTC Outbound/Inbound Data Path

The DMA controller performs fast, bidirectional, 1-byte data transfers between the Inbound and Outbound Data Registers, RTC memory, and the SIO chip. When receiving data, a DMA write cycle carries inbound data from SIO receiver channel A to RTC memory across DMA channel 0. When transmitting, SIO transmit channel B obtains outbound data from RTC memory by means of a DMA read cycle on DMA channel 1. Simultaneous transfers in both directions support full-duplex communication. During loopback operation, DMA channel 1 carries data to SIO channel A instead of channel B, and DMA channel 0 returns data from channel B instead of channel A.

The 8086 initializes an RTC by executing an OUT instruction that causes an RTC software reset. Then, during subsequent operations, the 8086 and the Z80A microprocessor in the RTC can communicate in three ways: by exchanging status information, interrupt requests, or data. The 8086 can read a 16-bit register containing RTC status flags; the RTC, in turn, can read 8086 status from an 8-bit status register. Similarly, the 8086 can access an output port that causes a Z80A interrupt request on the RTC board, and the RTC board's Z80A can interrupt the 8086.

Data transfers are the most common means of communication between the 8086 and the RTC. Two registers (called the Inbound and Outbound Data Registers) form a bidirectional data path for either programmed data transfers or DMA transfers. The 8086 has one DMA channel available to receive data from or transmit data to the RTC. In contrast, the RTC has two DMA channels, one for receiving data from the 8086 and one for sending data to the 8086. I/O ports allow the 8086 and the Z80A to execute programmed data transfers along the same data paths used by the DMA interface.

To send outbound data, the 8086 writes the Outbound Data Register, which the Z80A reads to receive inbound data, the 8086 reads the Inbound Data Register which the Z80A can write. The Inbound and Outbound Data Registers are named from a system viewpoint. Inbound data includes data that comes in from the communication link and moves inward through the RTC toward the main system memory. The RTC's Z80A looks back towards the 8086 interface and reads the Outbound Data register and writes the Inbound Data Register.

Both the Inbound Data Register and the Outbound Data Register are 16-bit registers that accept and receive only 8-bit data. For programmed data transfers, these registers are treated exactly as though they were 8-bit I/O ports. When the 8086 writes either byte of the Outbound Data Register, what ever byte it writes is the next byte made available for the Z80A to read. When the Z80A writes a byte to the Inbound Data Register, the byte it writes is replicated in the other byte, and the 8086 can read either one. DMA transfers capitalize on this design to multiplex high-order bytes and low-order bytes from D0-15 onto the 8-bit RTC board.

In response to a read at offset 10FEH (highest I/O port address), the 8232 board returns its option ID code of 1CH on D0-6 and the 8252 board returns its option ID code of 1E. The option ID code returned on D0-6 from port offset 10FEH is the only difference between these two RTC option boards that is enforced by hardware. When gating their 7-bit option ID codes onto D0-6, both boards drive D7 high only if they have a pending 8086 interrupt request. The RTC decodes only the low-order four bits of an I/O port address offset. Table 2-22 lists all RTC I/O ports that the 8086 can access.

Table 2-22. RTC 8086 I/O PORTS

Port	Description
1xF0H	Read RTC Status Register. The 8086 can read either the low or the high order byte of this 16-bit port, or it can read the entire 16 bits of status. Only bits 10 and 11 of the RTC Status Register are set by hardware. Bit assignments are as follows: D4-7 Set when Z80A software running on the RTC board executes an OUT 52. D10 Outbound Data Register empty. Set when Z80A (or DMA) reads either byte of the Outbound Data Register, port 1xF8H. Remaining byte may or may not contain data. Cleared when 8086 (or DMA) writes either byte of Outbound Data Register. Generates a DMA request when D2 at output port offset F2H is set. D11 Inbound Data Register full. Set indicates that the Inbound Data Register, port 1xF4H, contains a single byte of data. Cleared when the 8086 (or DMA) reads the Inbound Data Register. Generates a DMA request when D3 at output port offset F2H is set. D0-3 Unassigned. D8, D9 and D12-15 are not used. Write 8086 Status Register. Loads D0-7 into the 8086 Status Register on the RTC.

Table 2-22. RTC 8086 I/O PORTS (Cont'd)

Port	Description
1xF2H	Write to enable Outbound Data register and DMA channels. Bits D0 and D1 are both set during RTC operation. When cleared, they disable the programmed output (OUT 1xF8H instruction) data path hardware for diagnostics with no effect on DMA transfers. Only one of bits D2 and D3 is normally set at a time. Clearing both D2 and D3 disables DMA transfers between the RTC and system memory. The default after a reset is D0-3 cleared. Bit assignments are: D0 Set to initialize low-order byte of Outbound Data Register. Cleared to disable low-order byte of Outbound Data Register. When cleared, output port offset F8H is disabled. Does not affect DMA. D1 Set to initialize high-order byte of Outbound Data Register. Cleared to disable high-order byte of Outbound Data Register. When cleared, output port offset F8H is disabled. Has no effect on DMA. D2 Outbound DMA enable. When set, the RTC automatically generates a DMA request each time D10 of the RTC Status Register is set, indicating that either half of the Outbound Data Register is empty and able to accept a byte of data. Software sets this bit when the system DMA controller is programmed to make outbound data transfers (DMA read cycle). D3 Inbound DMA enable. When set, the RTC automatically generates a DMA request each time D11 of the RTC Status Register is set, indicating that the Inbound Data Register contains a byte of data. Software sets this bit when the system DMA controller is programmed to make inbound data transfers (DMA write cycle). D4-7 Unassigned.
1xF4H	Read Inbound Data Register and clear bit 11 of RTC Status Register (port 1xF0H). The 16-bit Inbound Data Register holds only one byte of data, with bits 0-7 always equal to bits 8-15. When the Z80A writes either byte of the Inbound Data Register, that byte is automatically copied into the other byte. This allows the 8086 to obtain both high and low-order bytes by reading the appropriate portion of the register. Write interrupt priority level and DMA channel assignment. This information must be provided before 8086 interrupts are enabled. Only one of bits D1, D2, and D3 is normally set at a time. Bit assignments are as follows: D1 Assigns DMA channel 1 and interrupt level 5 if set. (D2 and D3 should be cleared.) D2 Assigns DMA channel 2 and interrupt level 6 if set. (D1 and D3 should be cleared.) D3 Assigns DMA channel 3 and interrupt level 7 if set. (D1 and D2 should be cleared.) D0, D4-7 are unassigned.

Table 2-22. RTC 8086 I/O PORTS (Cont'd)

Port	Description
1xF6H	Write arbitrary data to generate a Z80A interrupt request via channel 0 of the secondary CTC.
1xF8H	Write Outbound Data Register. Like the Inbound Data Register, the 16-bit Outbound Data Register holds only one byte of data at a time. The 8086 writes either the high-order byte or the low-order byte of this register, but not both, depending upon whether the outgoing data originated in a high or low-order byte of memory. Data normally alternates between high and low-order bytes.
1xFAH	Write arbitrary data to acknowledge 8086 interrupt request from RTC. Causes RTC to remove its interrupt request.
1xFCH	Write arbitrary data to reset the RTC.
1xFEH	Read Option ID Code (D0-6 will be 1CH for the 8252 board or 1EH for the 8232 board) and interrupt status (D7 set if the RTC has a pending 8086 interrupt request). On the 8252 (X.21) Option only, write with: D4 Set to one to generate level 2 interrupts. D5 Set to one to generate level 3 interrupts. D6 Set to one to generate level 4 interrupts. Only one of bits 4-6 is normally set at a time, and bits 1-3 of port 1xF4H are normally all cleared to zero when any of these bits is set. (If one of bits 1-3 in port 1xF4H is set to one, the DMA channel determines the interrupt priority level).

Outbound parallel data flows from the system bus through the Outbound Data Register to RTC memory, and from there to the Serial Input/Output (SIO) chip, which converts the outbound data to serial format and sends it to the RS232C or X.21 interface connector. On the inbound data path, serial data from the communication interface travels first to the SIO chip, which converts it to parallel format, and then through RTC memory on its path to the Inbound Data Register.

The SIO chip contains two independent full-duplex channels. Channel A receives input from the RS-232C or X.21 communication interface and transmits loopback output to SIO channel B. Channel B, in turn, transmits output to the appropriate communication interface and receives loopback input from channel A.

Table 2-23. RTC Z80A I/O PORT ADDRESSES

PORT	DESCRIPTION
00-03H	SIO chip registers.
10-1FH	DMA controller chip registers.
20-23H	Primary CTC registers.
30H	Write a data character to clear that character's recognition table entry and enable its character recognition interrupt.
31H	Write a data character to set that character's recognition table entry disabling its character recognition interrupt.
40H	Read Option Switches. Loads configuration option switch settings into the accumulator with switch 1 LSB and switch 8 MSB. D0 0 to select external clock (synchronous operation) 1 for internal clock (asynchronous operation). D1 0 to send serial data in NRZ mode. 1 to select NRZI mode. D4 0 to set /SRTS to mark. 1 to set /SRTS to space. D7 Set to generate an 8086 interrupt request. The default is zero in every case.
44H	Read 8086 Status Register. Write arbitrary data to reset RTC.
48H	Write arbitrary data to signal "DTE Ready" (C=OFF and T=0) on the 8252 (X.21) option board only. The power-up default condition is "DTE Uncontrolled Not Ready" (C=OFF and T=1).
4CH	Read ACU Status Register on 8232 (RS-232C) option only. Bit assignments are as follows: D0 Abandon Call and Retry. D1 Present Next Digit. D2 Power Indicator. Power on when set. D3 Call Origination Status. D4 Data Line Occupied. D5-7 Not assigned. Write ACU Command Register on 8232 (RS-323C) option only. Bit assignments are as follows: D0-3 Digit bits 0-3. D4 Digit Present. D5 Digit Request Flag. D6-7 Not assigned. Write with Bit 7 set to one to enable break detection on the 8252 (X.21) board only. When break detection is enabled, circuitry on the 8252 board gates the received data and clock to the SIO channel B receiver. SIO channel B then detects the continuous low condition lasting at least 16 bit times, that signals a break.

Table 2-23. RTC Z80A I/O PORT ADDRESSES (Cont'd)

PORT	DESCRIPTION
50H	Read Outbound Data Register.
51H	Write low-order byte of RTC Status Register. Assigned bits in the high-order byte are set by hardware.
52H	Write D4-7 into bits 12-15 of the RTC Status Register.
54H	Enable Inbound Data Register. Bits D4 and D5 normally are both set during RTC operation. When cleared, they disable the programmed output (OUT 56H instruction) data path hardware for diagnostics, but they have no effect on DMA transfers. Bit assignments are as follows: D4 Set to initialize low-order byte of Inbound Data register. Cleared to disable low-order byte of Inbound Data Register. When cleared, output port 56H is disabled for low-order byte output. Has no effect on DMA. D5 Set to initialize high-order byte of Inbound Data Reg. Cleared to disable high-order byte of Inbound Data Reg. When cleared, output port 56H is disabled for high-order byte output. Has no effect on DMA. D0-3 and D6-7 are not assigned.
56H	Write Inbound Data Register. OUT 54H with D4 and D5 set should precede first OUT 56H.
60-63H	Secondary CTC Registers
70H	Read to toggle LED indicator. Read returns byte of 0 and turns LED on (if it is off) or off (if it is on). Initial setting is on. Write arbitrary data to enable bad (ie, odd) parity generation.
71H	Write arbitrary data to enable good (ie, even) parity generation. In the absence of a write to port offset 70H, good parity is the default setting.

The Z80A interrupts and interrupt priority are as follows: Nonmaskable interrupts (NMI) denote parity errors. Parity errors have the highest priority except for the bus request (BUSRQ) signal from the DMA Controller. Following NMI's in order of priority are maskable interrupt mode 2 and vectored interrupts. The SIO chip and the CTC are the only sources of vectored interrupt requests. Connected in a daisy chain, they provide an interrupt nesting mechanism that automatically selects the highest priority device when both request service simultaneously. An RETI instruction ends an interrupt service routine by reinitializing the daisy chain for proper handling of nested priority interrupts. Table 2-24 lists all possible vectored interrupts by priority.

Table 2-24: RTC VECTORED Z80A INTERRUPTS IN ORDER BY PRIORITY

Interrupt	Function
SIO Channel A Receiver	highest priority
SIO Channel A Transmitter	used only for loopback operation
SIO Channel A Status	not used under BISYNC, Ring Indicator signal provides external/status signal
SIO Channel B Receiver	used only for loopback operation
SIO Channel B Transmitter	
SIO Channel B Status	not used under BISYNC
Primary CTC Channel 0	character recognition interrupt or general purpose timer
Primary CTC Channel 1	SIO receiver and transmitter clocks or counter for checking SDLC and HDLC flag characters
Primary CTC Channel 2	end of process for all four DMA channels
Primary CTC Channel 3	software timer
Secondary CTC Channel 0	Z80A interrupt request from 8086
Secondary CTC Channel 1	Z80A interrupt when 8086 writes Outbound Data Register.
Secondary CTC Channel 2	Z80A interrupt when 8086 reads Inbound Data Register
Secondary CTC Channel 3	Unassigned, lowest priority

On the 8232 (RS-232C) option board, an automatic calling unit (ACU) completely automates data transmission via the telephone network. Four binary signal lines (DO-3 or NB1, 2, 4, and 8) to the ACU carry a defined character set of 16 codes. Codes 0 through 9 correspond to the digits zero through nine. Codes 10 through 13 correspond to asterisk (*), pound sign (#), End of Number (EON), and the separation control character (SEP), respectively. Codes 14 and 15 are not defined. The RTC sends EON after sending the last digit of the number it is dialing. In response to EON, the ACU immediately transfers the communication channel to the data set without waiting for an answer signal from the called data set. SEP signals a pause between successive digits. For example, in response to SEP, the ACU may again wait for a dial tone before turning ON circuit PND. Table 2-25 contains definitions of the ACU interface signals.

Table 2-25. AUTOMATIC CALLING UNIT INTERFACE

Name	Pin	I/O	Description
NB1	14	O	Digit bit 0
NB2	15	O	Digit bit 1
NB4	16	I	Digit bit 2
NB8	17	O	Digit bit 3
DPR	2	O	Digit Present. Indicates to the ACU that it can read the 4-bit code on NB1, 2, 4, and 8, which must not change state while DPR is active.
CRQ	4	O	Call Request. Asks the ACU to place a call. Must remain active in order to hold the line open (ie, remain off-hook). ACU aborts the call if CRQ goes inactive before COS or DSC goes active.
ACR	3	I	Abandon Call and Retry. When active, determines that a prescribed time has elapsed between successive events in the calling procedure and thereby indicates to the RTC when the call should be abandoned. Action is required by the RTC to abandon the call.
PND	5	I	Present Next Digit. When active, indicates that the ACU is ready to accept the next 4-bit digit from the RTC. Otherwise, when inactive, tells the 8086 to disable DPR and set the NB1, 2, 4, and 8 for the next digit.
PWI	6	I	Power Indication. Active to indicate that the ACU is powered on.
COS	13	I	Call Origination Status. Designated as "DSS" in an earlier RS-366 specification, indicates whether connection to a slave has been established. It can also indicate the status of the automatic call origination procedures. COS does not, however, indicate the operational status or preparedness of the associated data set.
DLO	22	I	Data Line Occupied. When active, indicates that the communication channel is in use (controlled by equipment other than the ACU originating the call). Falling edge does not occur until all interchange circuits return to their idle condition.

Located on the RTC PCB is a LED (denoted LED 1, see Figure 2-15 for location) that is used during the diagnostics routine to denote a Pass/Fail condition of the RTC diagnostics. This LED can be seen by viewing the rear panel of the RTC board.

When the power-on diagnostics are run, either on power up or loop continuously (if Switch Bank 3 of SW1 is set), the LED will illuminate during the diagnostic tests and will be turned off upon successful completion.

The 4K X 8 bit ROM contains a program that provides a Built-In-Test (B.I.T) for the RTC Option. The B.I.T contains a Power-On Self Test, a RTC/PC Interface Test, and a PC Interprocessor Control Operating System Layer (PCIPC) test.

The Power-On Self Test checks the integrity of most of the LSI chips and all of the RAM devices when power is applied to the PC. This test can be set to continuously loop if Switch Bank 3 (Bit 2) of SW1 is set to the ON position as previously discussed.

The Interface Test is invoked by the On-Line Diagnostic Monitor. It tests the interface chips (High Byte Latch and Low Byte Latch) and their associated circuitry.

The PCIPC Test provides a communication path for the operating system software between the PC and the RTC.

Refer to the diagnostic documentation included with the diskette for test operation and definition of errors and error codes.

2.16 MULTIPORT COMMUNICATION CONTROLLER (PC-PM042)

The Multiport Communication Controller (MCC, PCA 8251) is a single board option that, when installed, allows the Wang PC to communicate with an IBM host in the System Network Architecture (SNA) using Synchronous Data Link Control (SDLC) protocol. The Software Package PC-SS063 3276 SNA/SDLC Emulation must be loaded into the PC in order to run the PC SNA Emulation. Refer to Appendix D SNA EMULATION in this manual for operating instructions and screen loads. The Wang Professional Computer Communications Guide WLI 700-7558 contains detailed operating instructions.

The MCC option (PCB 8251) can be installed in any of the option slots within the PC system. Refer to paragraph 4.9.1 for option board installation. The minimum PC configuration for this option consists of a PC-001, a Medium Resolution Character Generator, a MCC card, a keyboard, a printer (optional), a monitor, a modem and RS232-C cables. The modem must be RS-232-C/V.24 compatible. This could be either a Null modem for cable communications, or a synchronous/asynchronous modem for voice grade phone line communications.

The MCC option has three (3) RS232 ports located on the rear panel. See Figure 2-18 for locations. Two of the ports (J1 and J2) are BISYNC and all three ports are ASYNC. For synchronous emulation either Port 1 or Port 2 can be used. For asynchronous emulation either Port 1, 2, or 3 can be used.

To connect the Wang PC to the modem, simply attach a RS-232-C/V.24 cable to the appropriate port of the MCC card. Attach the other end of the cable to the Null Modem or the synchronous modem depending on the communication link. Be sure the cable connector's mounting screws are tightened to ensure proper mating connection. Three RS232 cables are available; these are:

220-0332	12 foot length
220-0333	25 foot length
220-0334	50 foot length

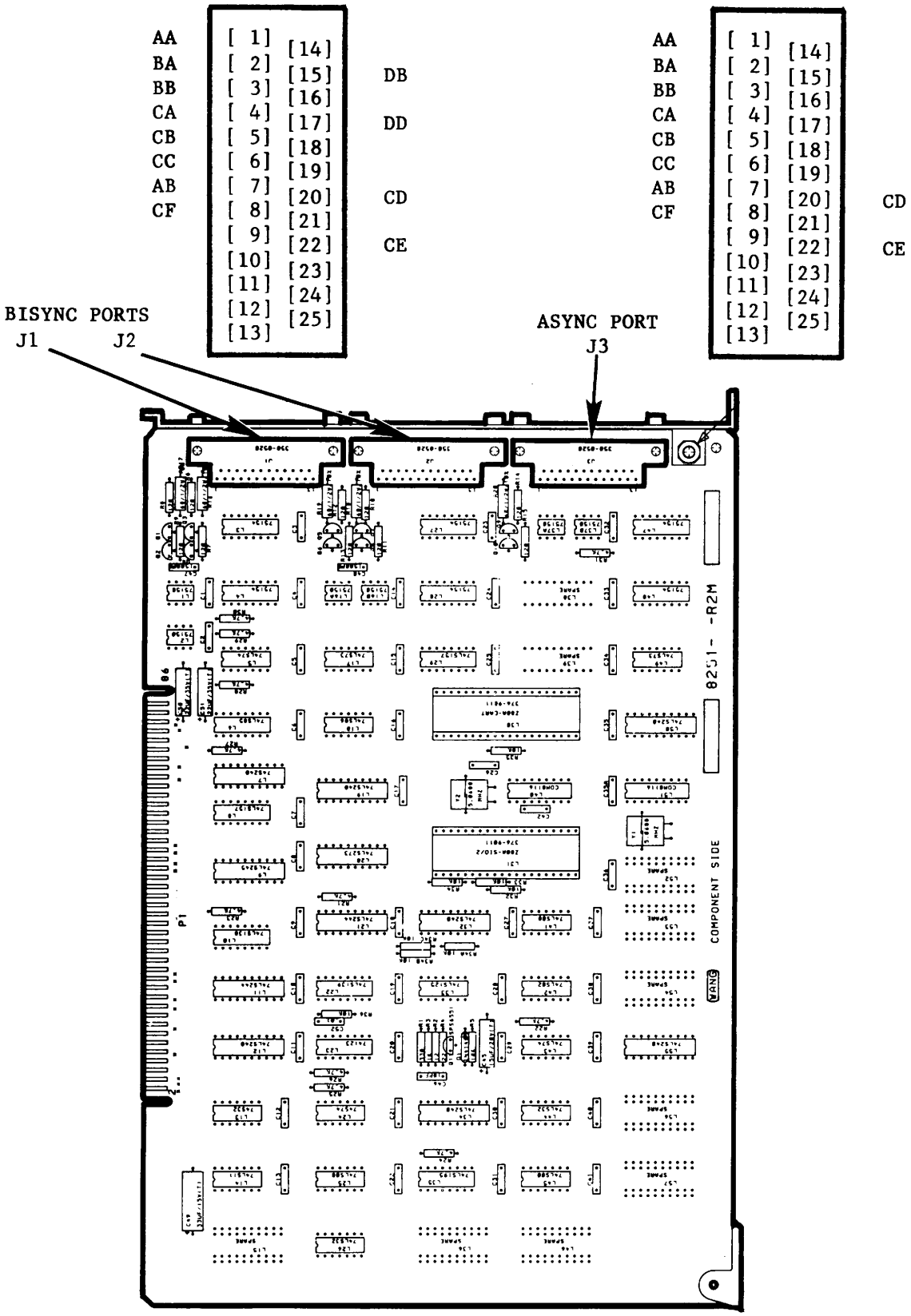


Figure 2-18. MCC Board 8251 Port Locations

2.16.1 MCC Option Theory of Operation

For the following discussion refer to the MCC 8251 Controller Block Diagram in Figure 2-19.

The 8251 Controller is I/O mapped and does not support Direct Memory Access (DMA). The controller is interrupt driven and only uses the lower data byte of the PC data bus (bits D0-D7). The controller is addressed by I/O byte instructions (A1-4, A8-11). These instructions are decoded on board and are explained later in the text.

The 8251 Controller is interrupt selectable by the PC Software interrupts 2, 3, and 4 with interrupt 2 being the default level on power up or after a board reset.

The three ports (numbered Port 1, 2, and 3) are standard 25 position "D" connectors. Ports 1 and 2 communication functions are handled by the Z80A-SIO/2 device. This device supports async, bisync, SDLC/HDLC, and modems (async and bisync). Port 3 functions are handled by the DART device which operates asynchronously only.

Located on the 8251 PCA is the Slot Decode logic. This logic is used to compare the board ID number (1F) and Slot number (xx) for the PC CPU to determine the slot location of the board and the type of board installed in that location. On system power up the CPU reads each slot (refer to paragraph 2.3.2.3). When the slot the MCC card is installed in is read, the bit pattern (Slot ID) is returned on the data bus to the CPU.

The MCC card uses only 8 address lines from the 8086 CPU (A1-4, A8-11). Addresses A8-11 are used for the slot decode and addresses A1-4 are used for I/O port decoded. Addresses A1 and A2 are also used to enable the SIO/2 and the DART device.

The I/O Port Decode decodes the addresses on the A1-A4 address bus and latches the enabled port low. The ports, their respective address bit pattern, and port function are shown below. All these ports are decoded from the System Address Bus and are exclusive to the MCC board.

BIT PATTERN				PORT	PORT FUNCTION
A4	A3	A2	A1	SELECT	
1	0	0	0	8	Read Status Buffer
1	0	0	1	9	Write Port 1 Baud Rate Register
1	0	1	0	A	Write Port 2 Baud Rate Register
1	0	1	1	B	Write Ports 1 and 2 Function Register
1	1	0	0	C	Write Port 3 Baud Rate Register
1	1	0	1	D	Not Used
1	1	1	0	E	Write Soft Reset for board
1	1	1	1	F	Read Slot Identifier Port

Each port listed above are further defined in the following text.

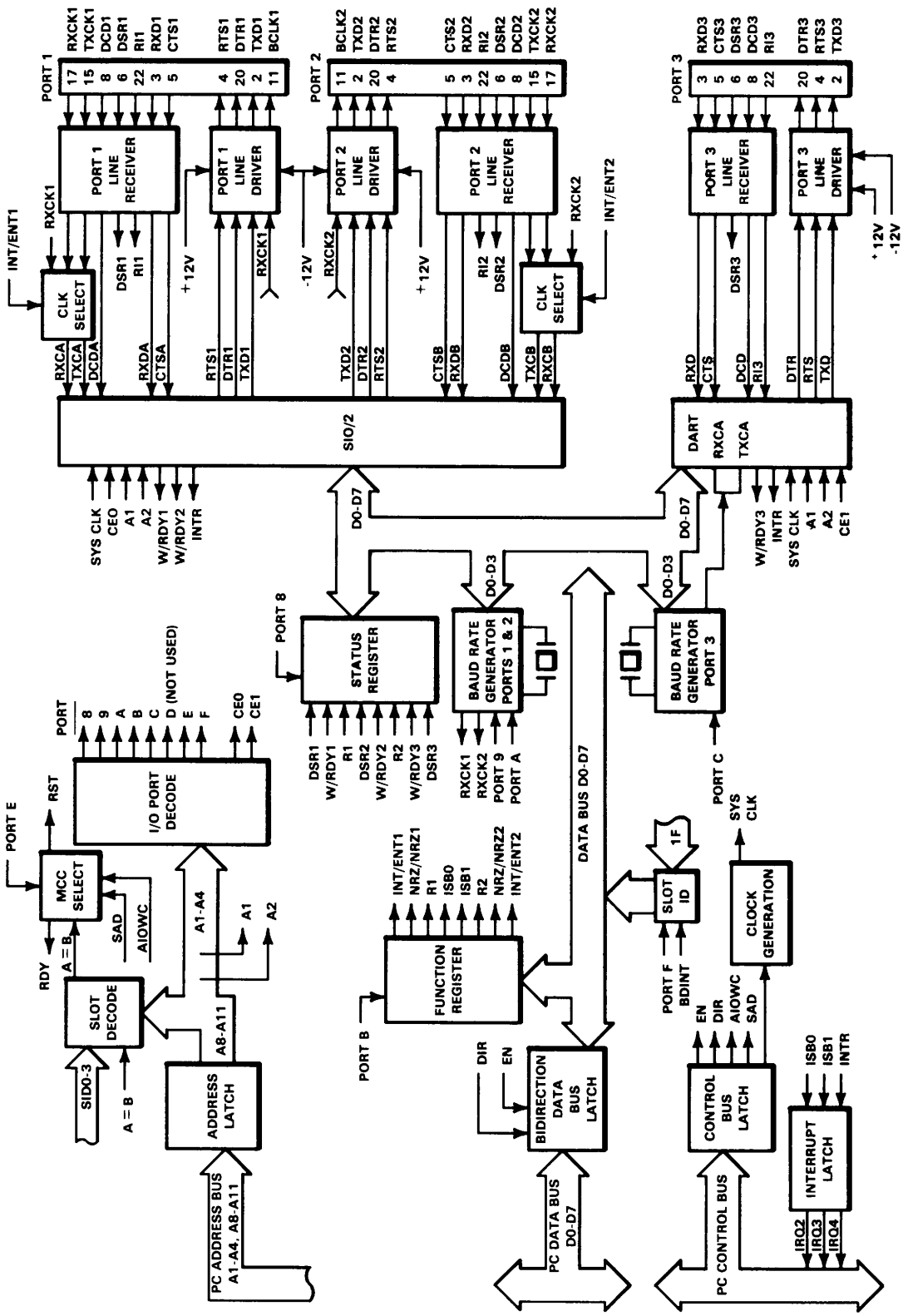


Figure 2-19. MCC 8251 Controller Block Diagram

Only the lower byte of the PC Data Bus (data bits D0-D7) is used on the MCC Card. This data byte is presented to the MCC board's data bus via a Data Bus Driver/Receiver chip. Two control signals (DIR and EN) are required in order for data to be transmitted between the PC Data Bus and the MCC Card data bus. The Data Bus Driver/Receiver is enabled (EN) when the slot decode (A=B) is selected by the PC CPU. The direction of the data bus is dependant on the Direction control signal (DIR). When DIR is Low, data transmission from the MCC card data bus is presented to the PC Data Bus. When DIR is High, data transmission from the PC Data Bus is presented to the MCC card data bus.

The Slot ID is the hardwired board identification code. This port is read by an IN to Port F. An IN to Port F gates the hardwired ID code onto the boards data bus (data bits D6-D0). Bit 7 will be active if the MCC card has a pending interrupt request. This interrupt request can either be generated by the SIO/2 or the DART device.

The Clock generation circuitry generates the MCC cards system clock (SYSCLK) used by the SIO/2 and the DART. This clock signal is derived from the PC systems 4CLK signal which synchronizes the MCC card with the PC system.

The Function Register decodes the bit pattern on the data bus (D7-D0) when enabled by an OUT to Port B. The Software written to the Function Register determines by Port (either Port 1 or Port 2) whether the on-board Baud Rate generator or the modem clock is used for data transmission, whether the data transmission uses the Non Return to Zero (NRZ) or Non Return to Zero Inverted (NRZI) encoding technique, and enables either Ring Indicator Port 1 or Port 2. Two bits (D7 and D6) are used for interrupt priority level. The bit pattern and the associated RS-232-C Port is as follows: An IN to Port B is an invalid instruction.

BIT	RS-232-C PORT	FUNCTION
0	1	When set denotes external clock selected (modem) When low denotes internal baud rate clock selected
1	1	When set denotes NRZI selected When low denotes NRZ selected
2	1	When set denotes Ring Indicator (RI) enabled When low denotes RI disabled
3	2	When set denotes external clock selected (modem) When low denotes internal baud rate clock selected
4	2	When set denotes NRZI selected When low denotes NRZ selected
5	2	When set denotes Ring Indicator (RI) enabled When low denotes RI disabled
6 and 7		Interrupt Request level select bits as follows:

BIT 6	BIT 7	Interrupt Request Level
0	0	2
1	0	3
0	1	4
1	1	Invalid

Two Baud Rate generators located on board produce clocks (when enabled) whose frequencies are 16 times the actual baud rate of the SIO/2 and the DART. SIO/2 ports A and B utilizes one of the Baud Rate generators and the DART utilizes the other one. The Baud Rate generators are programmed by the bit pattern on the data bus bits D3-D0. This bit pattern is read by an OUT to Port 9 for SIO/2 Channel A, an OUT to Port A for SIO/2 Channel B, and an OUT to Port C for the DART. An IN to Ports 9, A, and C are invalid. The bit pattern for Baud Rate Selection is shown in Table 2-26.

Table 2-26. Baud Rate Select Bit Pattern

D3	D2	D1	D0	HEX	Baud Rate
0	0	0	0	0	50.00
0	0	0	1	1	75.00
0	0	1	0	2	110.00
0	0	1	1	3	134.50
0	1	0	0	4	150.00
0	1	0	1	5	300.00
0	1	1	0	6	600.00
0	1	1	1	7	1,200.00
1	0	0	0	8	1,800.00
1	0	0	1	9	2,000.00
1	0	1	0	A	2,400.00
1	0	1	1	B	3,600.00
1	1	0	0	C	4,800.00
1	1	0	1	D	7,200.00
1	1	1	0	E	9,600.00
1	1	1	1	F	19,200.00

The above Baud Rate selection is used in Asynchronous mode of operation by the DART and the SIO/2 (if the SIO/2 is being run in Async mode). In synchronous mode, the SIO/2 requires a xl clock which means that the baud rate selected by the Baud Rate generator must be different from the desired rate of the SIO/2. The selected baud rate must be 1/16th the rate desired. Table 2-27 shows the Baud Rate selection required by the SIO/2 for the synchronous mode of operation.

Table 2-27. SIO/2 Synchronous Baud Rate Selection

SIO/2 Baud Rate	Generator Baud Rate
1,200	75 (min)
2,400	150
4,800	300
9,600	600
19,200	1200
38,400	2400
76,800	4800

The Status Register contains the status of the three RS-232-C ports as well as the status of the SIO/2 and the DART device. The CPU reads the Status Register by sending an IN to Port 8. An IN to Port 8 reads the status and transmits it to the CPU via the data bus bits D0-D7. An OUT to Port 8 is an invalid instruction. The data bit assignments are as follows:

Bit 0 SIO/2 Channel A W/RDY1 (WAIT/READY 1) (LSB)
Bit 1 SIO/2 Channel B W/RDY2 (WAIT/READY 2)
Bit 2 RS-232-C Port 1 DSR1 (Data Set Ready 1)
Bit 3 RS-232-C Port 2 DSR2 (Data Set Ready 2)
Bit 4 RS-232-C Port 1 RI (Ring Indicator)
Bit 5 RS-232-C Port 2 RI (Ring Indicator)
Bit 6 DART Channel A W/RDY3 (WAIT/READY 3)
Bit 7 RS-232-C Port 3 DSR3 (Data Set Ready 3) (MSB)

The SIO/2 device is a two channel Synchronous Input/Output device used to interface the Modem/Host to the PC system. Both channels of the SIO/2 are full duplex each having separate control and status lines. The SIO/2 functions as a Serial-to-Parallel convertor and a Parallel-to-Serial converter in a two channel full duplex mode. The SIO/2 is CPU selectable (Address lines A1 and A2) and can decipher CPU commands by reading the data bus when enabled by the CPU.

Command mode is enable when address bit A2 is high. A CPU write to the SIO/2 causes the information on the data bus to be interpreted as a command for the channel selected by address bit A1. When A1 is high channel B is selected and when A1 is low channel A is selected. The SIO/2 decodes four ports which are defined below.

Port 0 An IN to Port 0 generates a data transfer from the SIO Channel A Receive Data register to the CPU on the data bus bits D0-D7. An OUT to Port 0 generates a data transfer to the SIO Channel A Transmit Data Register from the CPU on the data bus bits D0-D7.

Port 1 An IN to Port 1 generates a data transfer from the SIO Channel B Receive Data register to the CPU on the data bus bits D0-D7. An OUT to Port 1 generates a data transfer to the SIO Channel B Transmit Data Register from the CPU on the data bus bits D0-D7.

Port 2 An OUT to Port 2 generates a control byte write from bus data bits D0-D7 to the SIO Channel A register. An IN to Port 2 is invalid.

Port 3 An OUT to Port 3 generates a control byte write from bus data bits D0-D7 to the SIO Channel B register. An IN to Port 3 is invalid.

When address A2 is low, the information on the data bus is data. The SIO/2 data bus transfers both data and commands between the CPU and the SIO. Data bit 0 is the least significant bit and data bit 7 the highest.

All signals from the modem link (RS-232-C/V.24) to the SIO/2 are via Line Receiver chips. The SIO/2 outputs to the modem link are through Line Drivers that modulate the signals to +12 volts for a logic High and -12 volts for a logic low.

All outputs from the modem link are through 68 ohm resistors for cable to Modem link impedance match. The RS-232-C/V.24 connectors are standard 25 pin "D" connectors. The pin assignments for Port 1 and Port 2 (Bisync) are shown below.

Table 2-28. MCC Card Port 1 and Port 2 Pin Assignments

Signal [EIA]	I/O	Pin	Description
GND [AA]		1	Chassis Ground
TXD [BA]	O	2	Transmit Data
RXD [BB]	I	3	Receive Data
RTS [CA]	O	4	Request to Send
CTS [CB]	I	5	Clear to Send
DSR [CC]	I	6	Data Set Ready
±0V		7	Signal ground and common return
$\overline{\text{DCD}}$ [CF]	I	8	Data Carrier Detect
INTBCLK	O	11	Interrupt B Clock
TXC [DB]	I	15	Transmit Clock
RXC [DD]	I	17	Receive Clock
DTR [CD]	O	20	Data Terminal Ready
RI [CE]	I	22	Ring Indicator
Pins 9, 10, 12-14, 16, 18, 19, 21, 23-25 are unassigned.			

The Dual Channel Asynchronous Receiver/Transmitter DART device is used as a Serial-to-Parallel data converter and a Parallel-to-Serial data convertor. The DART interfaces the modem/host to the PC system in async applications. As the SIO/2, the DART can decipher commands from the PC CPU. The DART is CPU selectable (Address lines A1 and A2) and reads CPU commands by reading the data bus when properly enabled. Command mode is enabled when address bit A2 is high. A CPU write to the DART causes the information on the data bus to be interpreted as a command for the channel selected by address bit A1. Only channel A of the DART is used by the MCC card. The DART decodes four ports which are defined below.

Port 4 — An IN or OUT instruction to Port 4 generates a data transfer to or from the DART Channel A Data register for TC port 3. Data bus bits D7-D0 are either written to or read from the DART.

Port 5 — An IN or OUT instruction to Port 5 generates a data transfer to or from the DART Channel B Data register for TC port 3. Data bus bits D7-D0 are either written to or read from the DART. NOTE that DART Channel two function is not used.

Port 6 — An OUT to Port 6 generates a control byte write from bus data bits D0-D7 to the DART Channel A register. An IN to Port 2 is invalid.

Port 7 — An OUT to Port 7 generates a control byte write from bus data bits D0-D7 to the DART Channel B register. An IN to Port 3 is invalid.

When address A2 is low, the information on the data bus is data. The DART's data bus transfers both data and commands between the CPU and the DART. Data bit 0 is the least significant bit. All signals from the modem link (Port 3) to the DART are via Line Receiver chips. The DART outputs to the modem link are through Line Drivers that modulate the signals to +12 volts for a logic High and -12 volts for a logic low. The Transmit Data (TXD) output from the modem link is via a 68 ohm resistor for cable to Modem link impedance match. The RS-232-C/V.24 connector is a standard 25 pin "D" connectors. Port 3 pin assignments are shown below.

Table 2-29. MCC Card Port 3 Pin Assignments

Signal [EIA]	I/O	Pin	Description
GND [AA]		1	Chassis Ground
TXD [BA]	O	2	Transmit Data
RXD [BB]	I	3	Receive Data
RTS [CA]	O	4	Request to Send
CTS [CB]	I	5	Clear to Send
DSR [CC]	I	6	Data Set Ready
±0V		7	Signal ground and common return
DCD [CF]	I	8	Data Carrier Detect
DTR [CD]	O	20	Data Terminal Ready
RI [CE]	I	22	Ring Indicator
Pins 9 thru 19, 21, 23, 24 and 25 are unassigned.			

It should be noted that the MCC card does not contain any memory devices, therefore all data received and transmitted is directly written to and received from main memory.

The Inbound Data Path and the Outbound Data Path is shown in Figure 2-20. The Outbound data is transferred by the PC system bus (lower 8 bits) from main memory to the MCC card. This data is presented to either the SIO/2 device for synchronous communications or the DART device for asynchronous communications.

For synchronous communication transmission, the SIO/2 deciphers CPU command codes and selects the channel requested for data communications. The command code is software controlled generated from operator entered parameters. These parameters are discussed in Appendix D. The parallel data bit pattern is converted to serial within the SIO/2 device. The SIO/2 formats the serial data with the required Sync characters and generates the Cyclic Redundancy Check (CRC) characters providing the appropriate protocol. This protocol is then transferred serially through the modem link to the host system.

In the Receive Mode, the SIO/2 receives the formatted protocol from the Host system and checks the CRC bit(s). If a CRC error is detected, the SIO/2 will abort the current message and request a re-call of the message from the host. If the CRC data is correct, the SIO/2 strips the Sync characters and the CRC characters and converts the serial bit stream into parallel. The SIO/2 transmits the parallel bit pattern to the CPU system memory via the data bus.

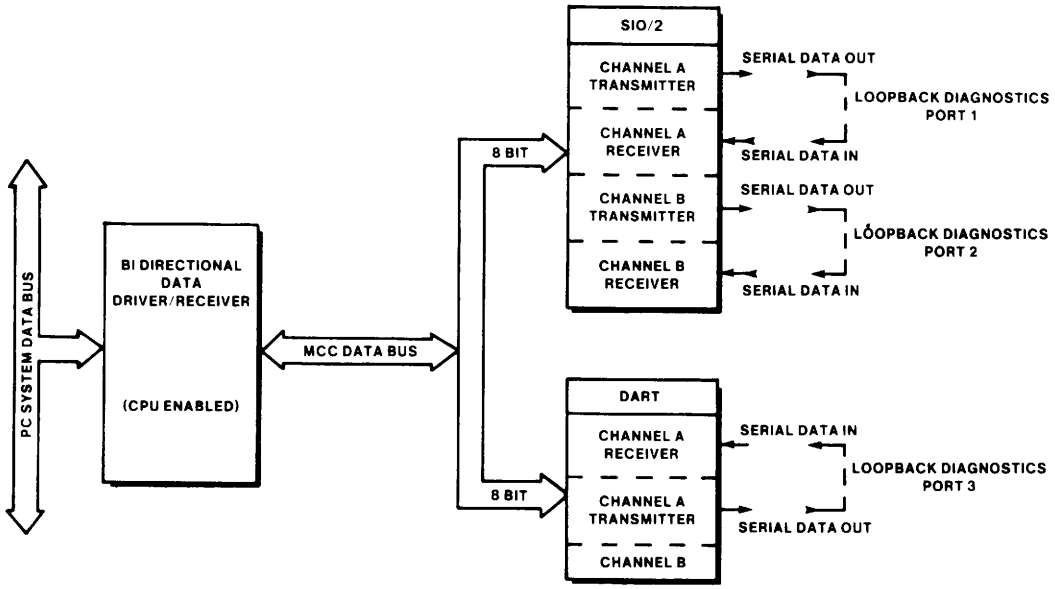


Figure 2-20. MCC Card Inbound/Outbound Data Paths

The DART device functions much the same as the SIO/2 device. Only channel A of the DART is used for data transmission, channel B is not used. The DART, being Asynchronous communications, uses Start, Stop, and Parity bits in the serial data protocol. The DART deciphers the command code on the data bus when address line A2 is high. The command code enables the DART to format the serial protocol using either 1, 1 1/2 or 2 Stop bits, even, odd or no parity, and selects the clock mode. When the DART receives data from the Host, the DART checks parity, strips the start and stop bits and converts the serial data to parallel. If a parity error occurs, the DART buffers the data bit received and initiates a Host recall.

The PC Floppy Diagnostic Package (Part Number 195-2459-9) contains diagnostic tests for the MCC card. These test are accessible through the CE operating mode and the Customer operating mode. The tests are explained in the diagnostic documentation include with the diskette. The Dash lines in Figure 2-20 show the Inbound/Outbound data path during diagnostic testing. This test requires a loopback connector (Wang Part Number 420-1040) to be installed on the Port being tested.

CHAPTER 3

OPERATION

3.1 INTRODUCTION

This chapter provides information pertaining to the operator controls and indicators, the PC initial control settings, initial turn-on procedures, and normal and emergency shut-down procedures.

3.2 CONTROLS AND INDICATORS

The Controls and Indicators of the Professional Computer are discussed in respect to the system component they are located on.

3.2.1 Electronics Unit Indicators

Located on the front of the System Floppy Drive (Drive A) is a LED. This LED will illuminate when the diskette loaded in the drive is being accessed by the system. This LED will toggle on and off while the information contained on the disk is either being read or the data read is being verified.

Located on the rear of the CPU board is a LED designated LED 1. See Figure 4-14. This LED will toggle on and off while the diagnostic test is being run. This LED is visible by viewing between the printer connector J2 and the keyboard connector J3. See Figure 4-12.

3.2.2 TTL Monitor Controls And Indicators

The TTL Monitor has two controls located on the upper front left-hand corner of the unit. See Figure 4-24. These controls are Monitor Brightness (top) and Monitor Contrast (bottom). These controls allow the operator to select the desired Contrast and Brightness while viewing the Monitor's display.

Prompts or messages will appear on the Monitor's display notifying the operator of an error condition. A listing of the IPL/Diagnostic Error messages are contained in Appendix B. Also included in Appendix B is a listing of messages that may be displayed by the operating system.

3.2.3 Keyboard Indicators

Located on the Keyboard are six LEDs (see Figure 4-23 for LED locations). These LEDs are software programmable and are used to denote diagnostic error codes during System Power-On.

3.2.3 Keyboard Indicators (Cont'd)

When Power is first applied, all the LEDs will illuminate for an instant. Then they will alternately illuminate on-then-off as the different diagnostic tests are being performed. Upon the successful completion of the Diagnostic Tests, all the LEDs will be turned OFF. If one or more LEDs remains lit, then a diagnostic error has been detected. Refer to Chapter 4 paragraph 4.13 Power-Up Diagnostic.

The Caps Lock Key (LED 0) allows letters to be capitalized while the numeric and symbolic characters remain unshifted. When the Caps Lock is depressed, the LED is illuminated. Depressing the Caps Lock a second time extinguishes the LED.

3.2.3.1 Important Keyboard Keys

A complete description of the keyboard keys is included in the PC Introductory Guide (WLI P/N 700-7590). The following discussion of the Important Keyboard Keys contains a general description of the special function the keys perform. Refer to the appropriate reference manual for definitions of the keys in regard to the software application being used.

HELP — Depressing the "HELP" key prompts the system to display the HELP Screen. This screen displays descriptions of the menu selections or the functions and commands available within a particular software application. The level of HELP information is directly related to the software being run.

CANCEL — Depressing the "CANCEL" key while using the system menus notifies the system to ignore the work done in the present operation or selection.

2ND — Depressing and holding down the "2ND" key while depressing a specified 2ND code keys perform special functions. One special function is Restart (Warm Start). Refer to chapter 4 paragraph 4.11 for description.

EXECUTE — Depressing the "EXECUTE" key notifies the computer to accept a display and to begin to carry out the function selected.

3.3 INITIAL CONTROL SETTINGS

The initial control setting for the PC are discussed in Chapter 4 paragraph 4.7. Depending on the options attached to your system (if any), ensure that each has the proper switch setting.

3.4 INITIAL TURN-ON PROCEDURES

Prior to powering-on the PC, ensure that all packing materials (tape, plastic wrap, etc.) is removed from the unit. Be sure that the Floppy Disk Drive (s) cardboard protector has been removed. Inspect the System to ensure that all cables are properly attached as described in Chapter 4.8 (PC Installation). Be sure to verify the proper voltage switch setting as described in Chapter 4 paragraph 4.7.2.

3.4.1 System Initialization

Be sure that the ac Power Switch (labeled I/O) located on the rear of the Electronics Unit is in the OFF (O) position. Insert the MS-DOS diskette into Floppy Drive A and latch the door closed. Power-Up the System Unit.

When power is first applied the System Units fan starts, a short beep will sound, the Boot PROM diagnostics will run, the Keyboard LEDs will flash on, and after a short time the Floppy's LED will illuminate. Now the System will execute the IPL (Initial Program Load). After the IPL is completed, the Floppy LED will go out and the Monitor will display the MS-DOS program title and request that the Time and Date be entered. Refer to Chapter 4 paragraph 4.10 (Powering-On the System) for a complete power-up sequence of events.

3.5 NORMAL SHUT-DOWN PROCEDURE

Before you Power-Down the Professional Computer return to the Main System Menu. Remove the floppy diskette (s), then Power-Down the system by turning the ac Power ON/OFF (I/O) switch to the OFF (O) position. When the system is powered down, ensure that the Floppy Drive Doors are closed. This will protect the Drive heads from dust and foreign materials.

3.6 EMERGENCY SHUT-DOWN PROCEDURE

In case of an Emergency situation when the normal Shut-Down procedure can not be used, perform the following:

Turn the ON/OFF (I/O) switch to the OFF (O) position.
Remove the ac power cord from the wall outlet.

3.7 OPERATOR PREVENTIVE MAINTENANCE

Operator Preventive maintenance consists of general cleaning of the unit. To clean the unit, use a slightly damp lint-free cloth to wipe down the outside case of the monitor, electronics unit, and keyboard. DO NOT USE CHEMICAL OR ABRASIVE CLEANERS. To clean the monitor screen, use a good quality glass cleaner and a soft lint-free cloth. Dust between the keyboard keys with a soft-bristled brush.

Operators are responsible for printer preventive maintenance. This includes general cleaning, removal of paper dust, and ribbon replacement.

CHAPTER 4

INSTALLATION AND CHECKOUT

4.1 SCOPE

This section provides information for unpacking, inspecting, installing, and verifying correct operation of the PC and its options. The PC is designed to be set up and installed by the customer. System modularity permits customers to upgrade to more powerful configurations without purchasing another system or replacing the base unit to support additional peripherals.

4.2 PRE-INSTALLATION SITE CHECK

No special pre-site planning is required for installation of the PC other than the recommended operating environment and procedural safeguards called out in the Customer Site Planning Guide (document No. 700-5978). The customer has the responsibility of ensuring that the PC installation site conforms to requirements given in the guide.

4.3 SPECIAL TOOLS AND TEST EQUIPMENT

The standard items provided in the WANG CE Tool Kit will suffice for the installation of the Wang Professional Computer. No special tools other than a cardboard-cutting knife and a screwdriver are necessary for unpacking the PC and its peripheral components. An oscilloscope will be required for performing adjustments on the Floppy Drives as described in Chapter 5.

4.4 UNPACKING

The Wang PC is designed for customer installation. Detailed step-by-step unpacking and installation instructions are provided as a separate document (Wang PC Introductory Guide 700-7590). The customer is responsible for unpacking the components, attaching them correctly, and running the diagnostic program to verify correct PC system operation.

NOTE

Perform a careful visual inspection of each shipping container for any indication of possible shipping damage (crushed edges, corners, puncture holes, tears, etc.). If any shipping damage is noted, now or during subsequent opening of any package, file an appropriate claim promptly with the carrier involved and notify the WLI Distribution Center Dept #90, Quality Assurance Department, Tewksbury, Mass. 01876, of the nature and extent of the damage while making arrangements for equipment replacement.

4.4 UNPACKING (Cont'd)

The Wang Professional Computer (PC-002) is shipped in four (4) individual boxes. Each of the boxes is labeled with a graphic representation of the component contained in the box. Figure 4-1 shows the PC fully packaged.

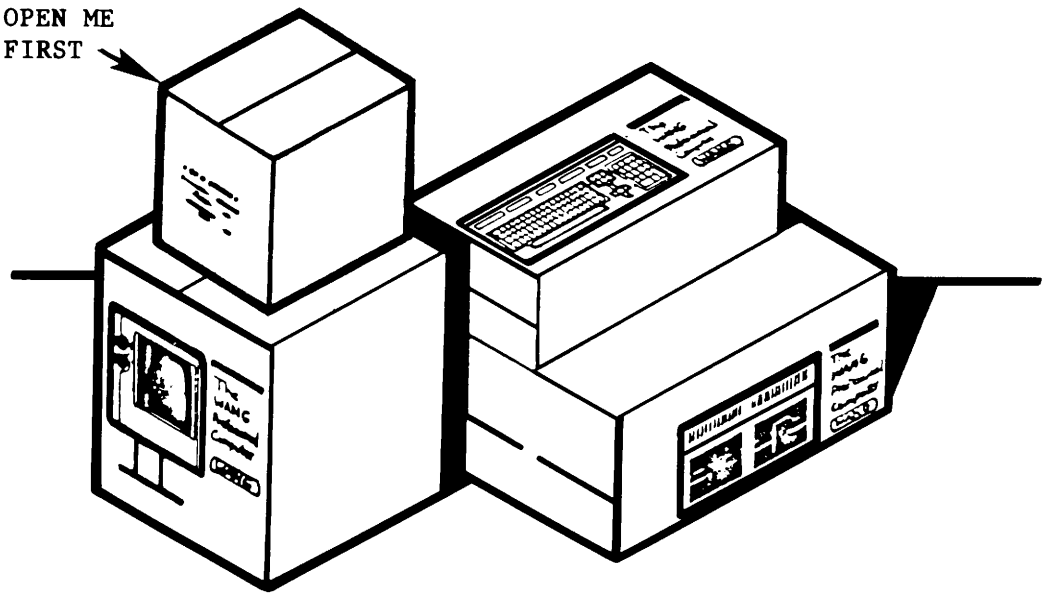


Figure 4-1. The Wang Professional Computer Fully Packaged

The unpacking procedures discussed in this section correspond to the order the boxes should be unpacked. After you finish upacking a box, save all of the packing material that came with your system. For the purpose of safety, you should reuse this material whenever you store or transport your system.

4.4.1 UNPACKING THE AUTO-ENCLOSED MATERIALS BOX

Open the Auto-Enclosed material box labeled (OPEN ME FIRST) and remove the contents. Refer to Figure 4-2. Enclosed in the box should be the following items: Note that the items listed below are furnished for PC-001.

- o MS/DOS Operating System (Plus Interpreter Basic) Diskette (s)
- o MS/Compiled Basic Diskette
- o PC Diagnostic Diskette
- o Wang PC Introductory Guide
- o Wang PC Documentation Guide
- o Wang PC BASIC Language Guide
- o Four protective rubber feet for the Electronics Unit

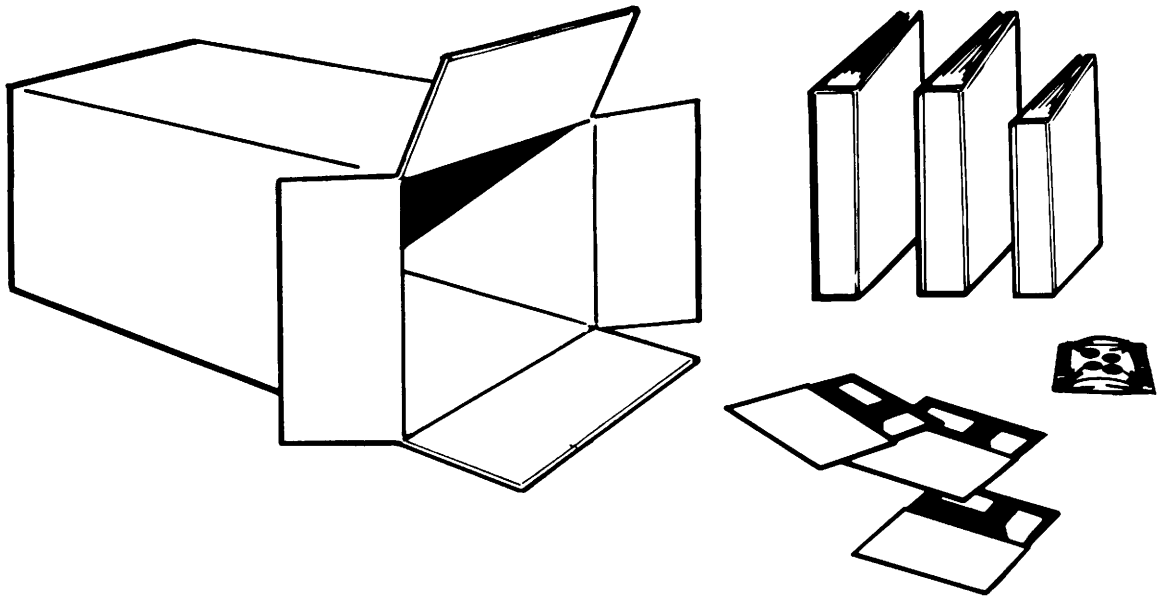


Figure 4-2. Opening The Auto-Enclosed Materials Box

4.4.2 UNPACKING THE KEYBOARD

Open the keyboard box as shown and remove the keyboard. (See Figure 4-3.) Place the keyboard on your desk or work surface as shown in Figure 4-3. Figure 4-3 shows all the items contained in the keyboard box. Make sure you unpack all the parts shown.

NOTE

FOR THE FIRST 2000 UNITS SHIPPED THE AUTO-ENCLOSURE MATERIAL WAS CONTAINED IN THE KEYBOARD BOX. AFTER THE INITIAL 2000, THE AUTO-ENCLOSURE MATERIAL IS SHIPPED IN ITS OWN BOX.

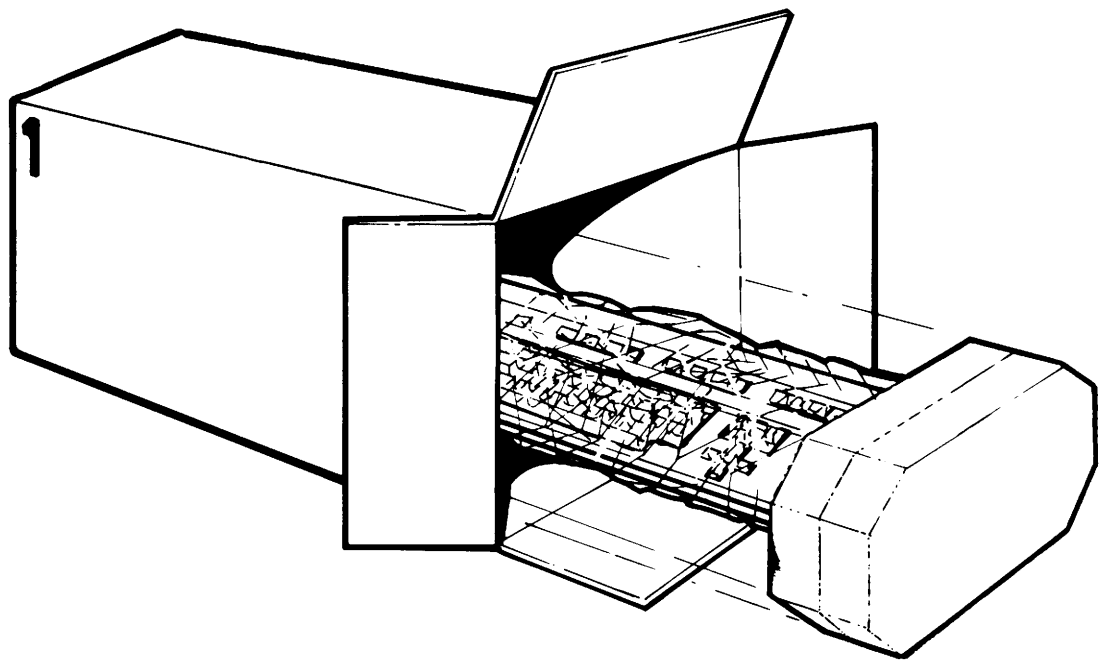


Figure 4-3. Unpacking The Keyboard

4.4.3 UNPACKING THE ELECTRONICS UNIT

Open the Electronics unit box and position it as shown in Figure 4-4. Grasp the handholds on the outside of the foam cushions and remove the foam from the box. Now lift the Electronics Unit out of the box. Place the unit on your desk so that the back panel with the red power switch is facing you. Figure 4-5 shows all the items contained in the electronics unit box. Make sure that you unpack all the parts shown.

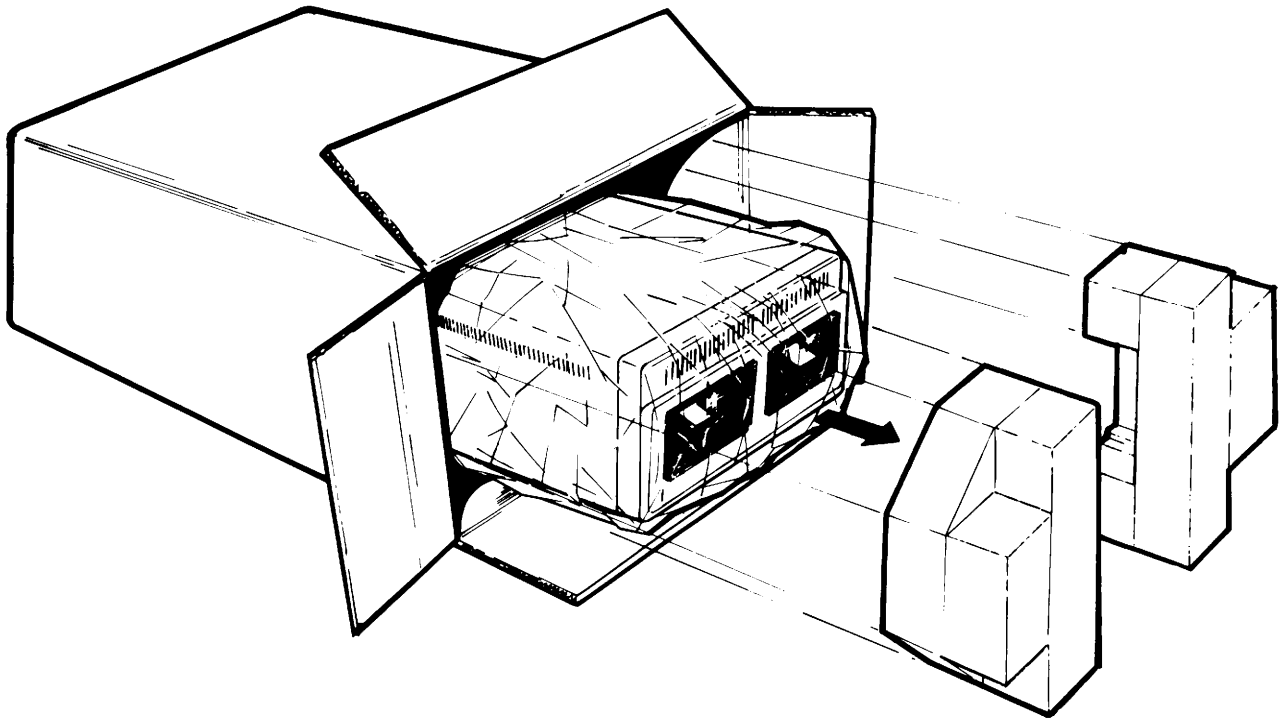


Figure 4-4. Unpacking the Electronics Unit

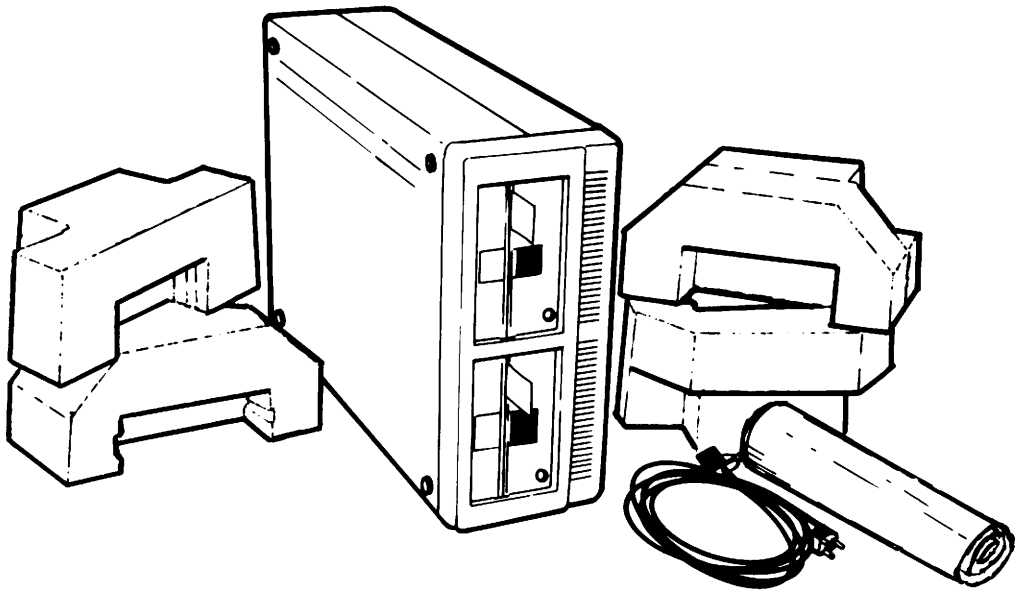


Figure 4-5. Electronics Unit Components

4.4.4 UNPACKING THE MONITOR

Position the Monitor box as shown in Figure 4-6. Open the monitor box top, remove the shipping foam and lift the monitor out of the box. Note that the Monitor Cable is included with the Medium Resolution Character Board option and is not enclosed with the monitor. Figure 4-7 shows the monitor unpacked.

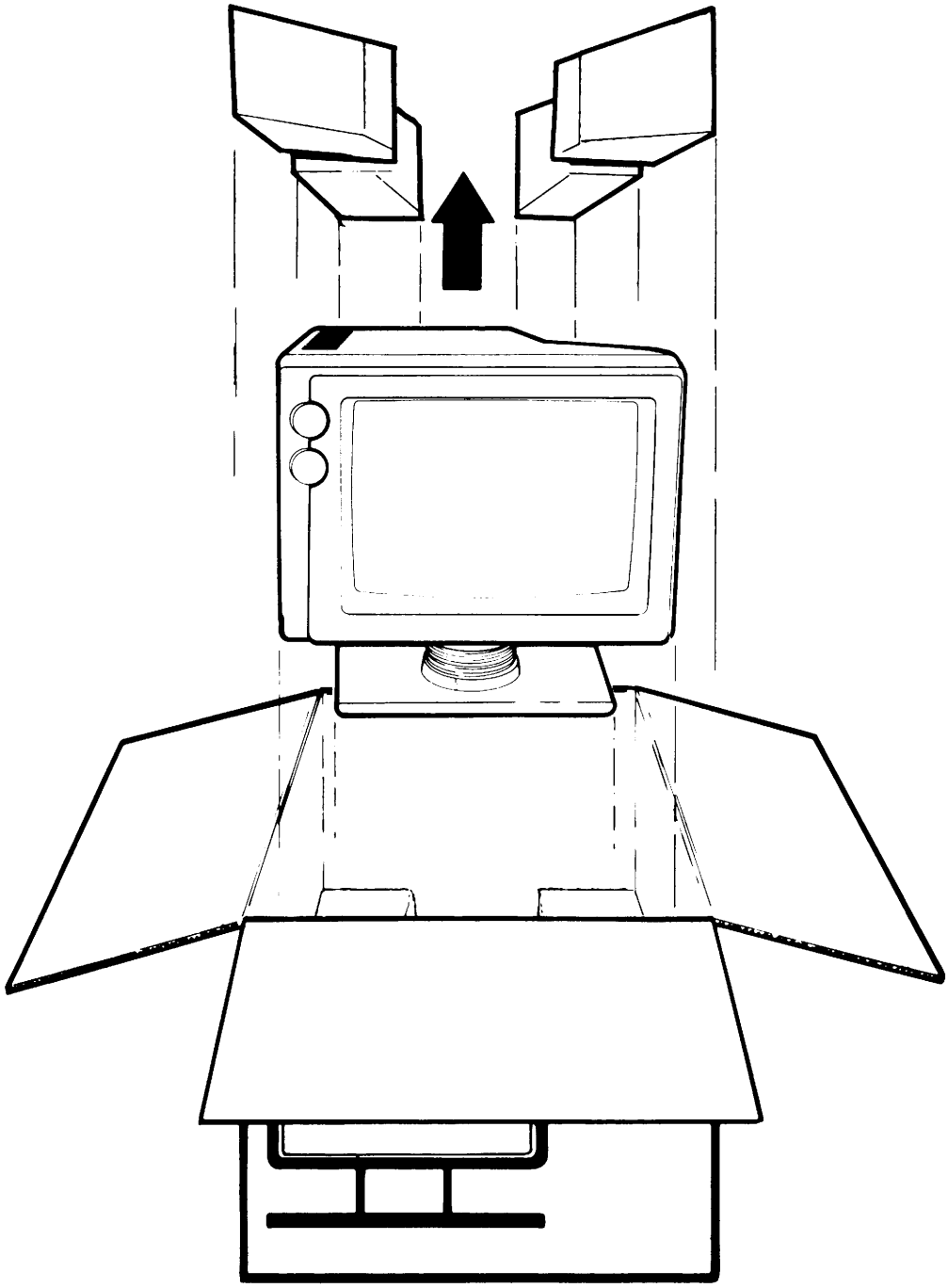


Figure 4-6. Unpacking the Monitor

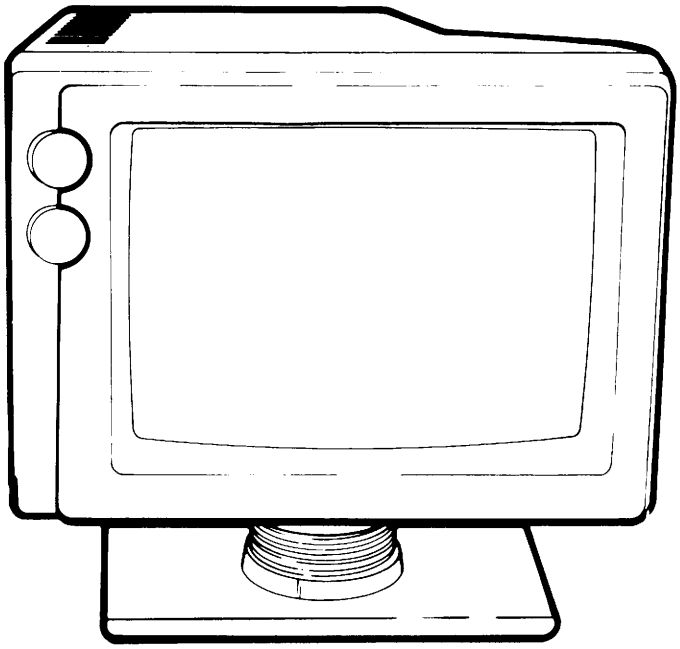


Figure 4-7. Wang PC Monitor

4.4.5 UNPACKING SYSTEM ATTACHMENTS

The Wang Professional Computer monitor must be mounted on either the monitor arm or the monitor base. The electronics unit can lie flat or be mounted on the side of a desk using the desk clamp attachment.

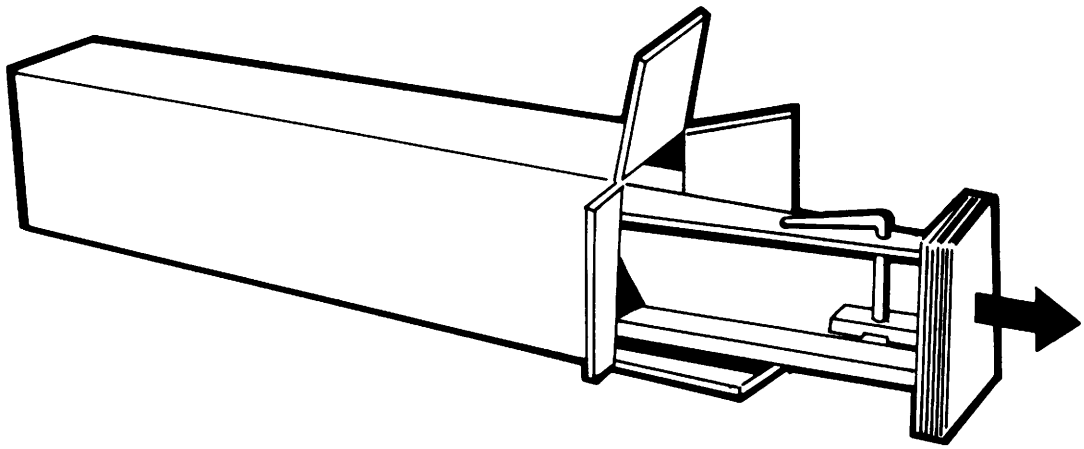


Figure 4-8. Unpacking the Desk Clamp

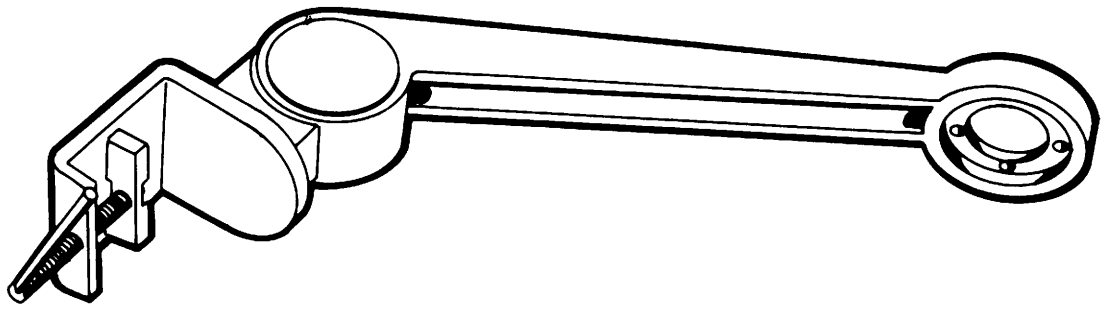


Figure 4-9. Wang PC Monitor Arm

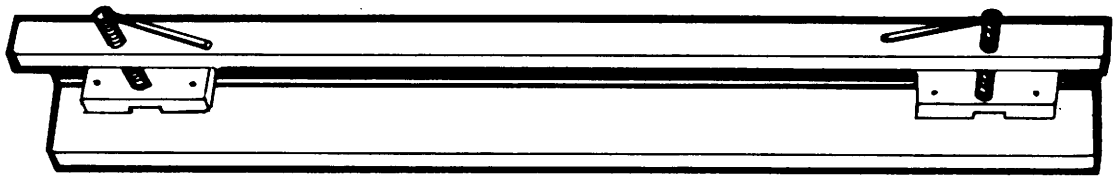


Figure 4-10. Wang PC Electronics Unit Desk Clamp

4.4.6 FINAL UNPACKING SEQUENCE

Perform the following steps to finish unpacking the PC. Proceed to inspect externally and internally for any shipping damage prior installation.

Step 1 Remove the diskette drive shipping protector.

( ) A thin piece of cardboard has been inserted in each disk drive during manufacturing to protect the drive from damage during shipping. These shipping protectors must be removed before connecting the system. To properly remove the shipping protectors from the diskette drives of your electronics unit, do the following:

Located in the diskette drive you will find a piece of cardboard. This is the shipping protector. See Figure 4-11. Remove the shipping protector by grasping the tab and pulling it out. Store the shipping protector with the other packing materials in the Electronics Unit box.

NOTE
IF YOUR ELECTRONICS UNIT HAS A SECOND DISKETTE DRIVE REPEAT THIS PROCEDURE FOR THAT DRIVE.

Step 2 Remove the voltage setting label.

( ) Remove the voltage setting label from the power switch located on the rear of the electronics unit. Your PC has been preset at the factory for operation at 115 VAC. Operating the PC outside the continental United States, the line voltage MUST be set to 230 VAC. Refer to paragraph 4.7.2 for 115V/230V Switch setting.

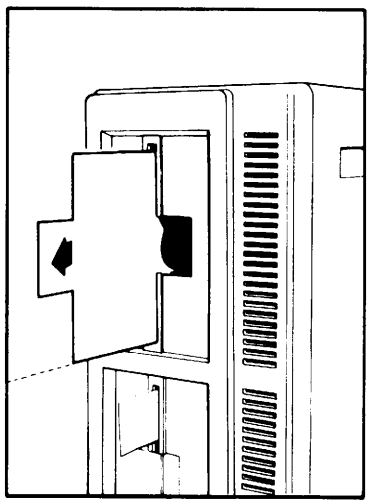


Figure 4-11. Removing the Shipping Protector From the Diskette Drive

Step 3 Unpack the remaining boxes.

( ) The equipment you have already unpacked (the electronics unit, keyboard, and monitor) forms the base system of your Wang PC. The unopened boxes (if any) contain equipment you can add to your computer to enhance its capabilities. Refer to the paragraph 4.8 for installation of these system options or peripherals.

Step 4 Save all of the packing material

( ) Save all of the packing material that came with your system. For the purpose of safety, you should reuse this material whenever you transport your system.

4.5 INSPECTION

After unpacking the PC, the CE should inspect all equipment, cables, and components for possible damage. Any damage should be reported as previously discussed in paragraph 4.4.

4.6 INTERCONNECTION OF EQUIPMENT

This section identifies all connectors, power cables, signal cables, switches, printed circuit boards, jumpers, etc, as necessary to interconnect the PC and its various peripherals. Both standard and optional equipment supplied as part of the PC is covered.

4.6.1 CONNECTOR IDENTIFICATION

The overall PC design concept is such that no two cable connectors are of the same physical type; therefore, it is impossible to interconnect the equipment in a wrong manner. The following illustrations show the different types of connectors the CE will encounter when installing the PC.

4.6.2 BASE UNIT

Figure 4-12 shows the location of and defines the function of all base unit connectors, PCB's, switches, cables, and indicators used to interconnect the base unit to the remaining peripheral components of the PC.

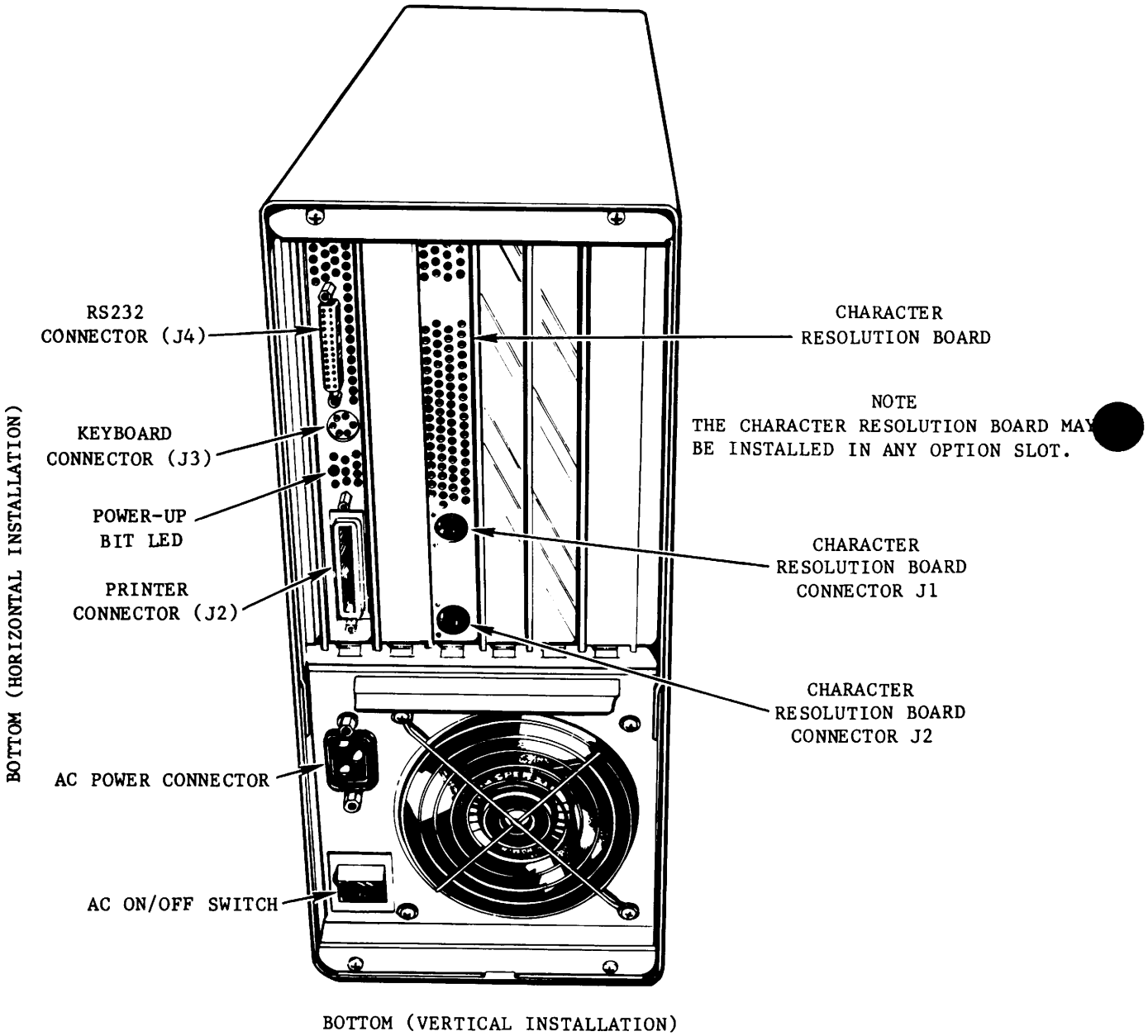


Figure 4-12. Electronics Base Unit

4.6.2.1 Base Unit PCB's

The location of the PCB's installed in the base unit is shown in Figure 4-13. Access to the internal chassis of the base unit is accomplished by first laying the base unit on its side with the air vents pointing downward, removing the four screws from the rear cover, then sliding the chassis out of the cover assembly.

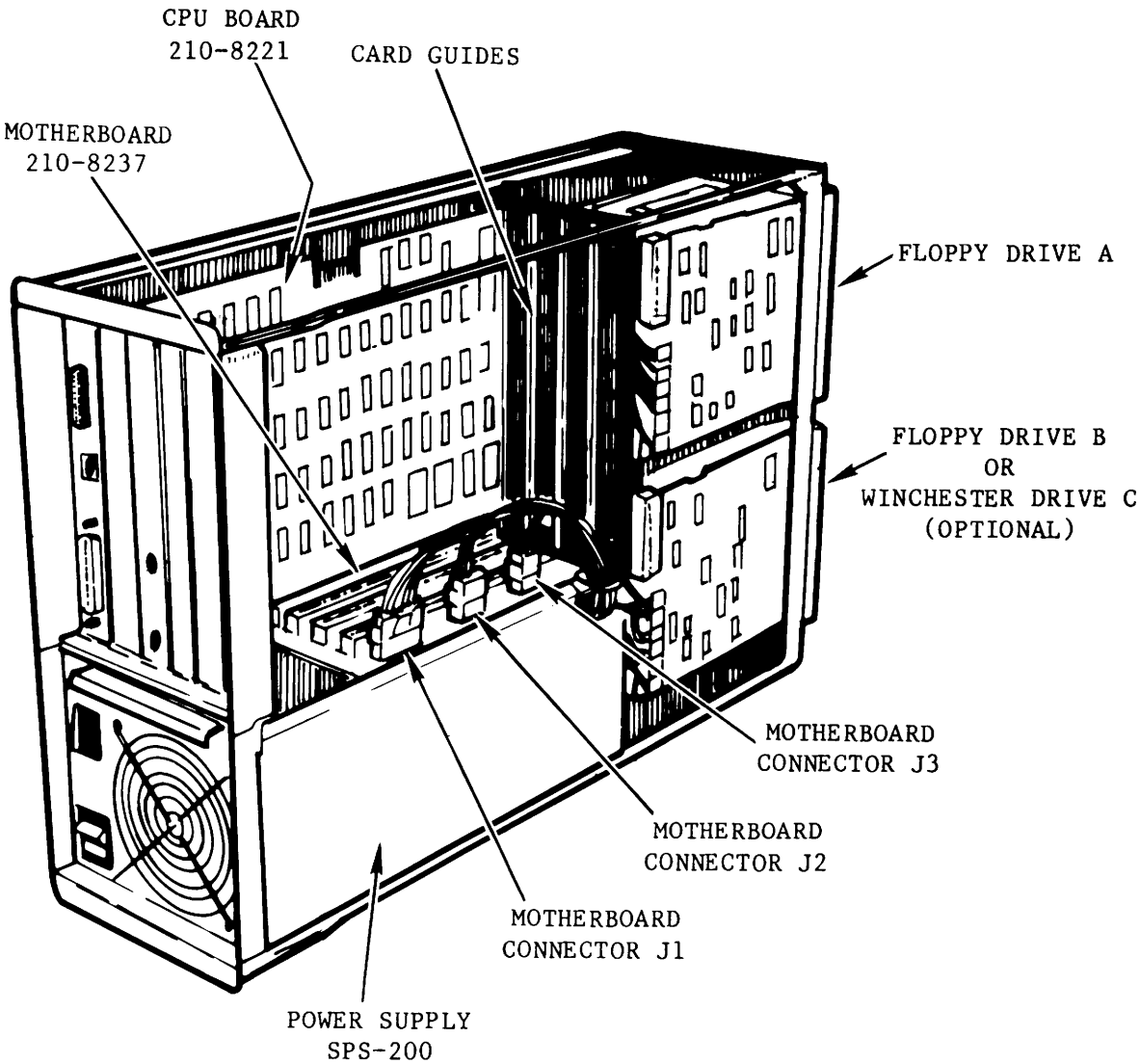


Figure 4-13. Base Unit Cover Removed and PCB Locations

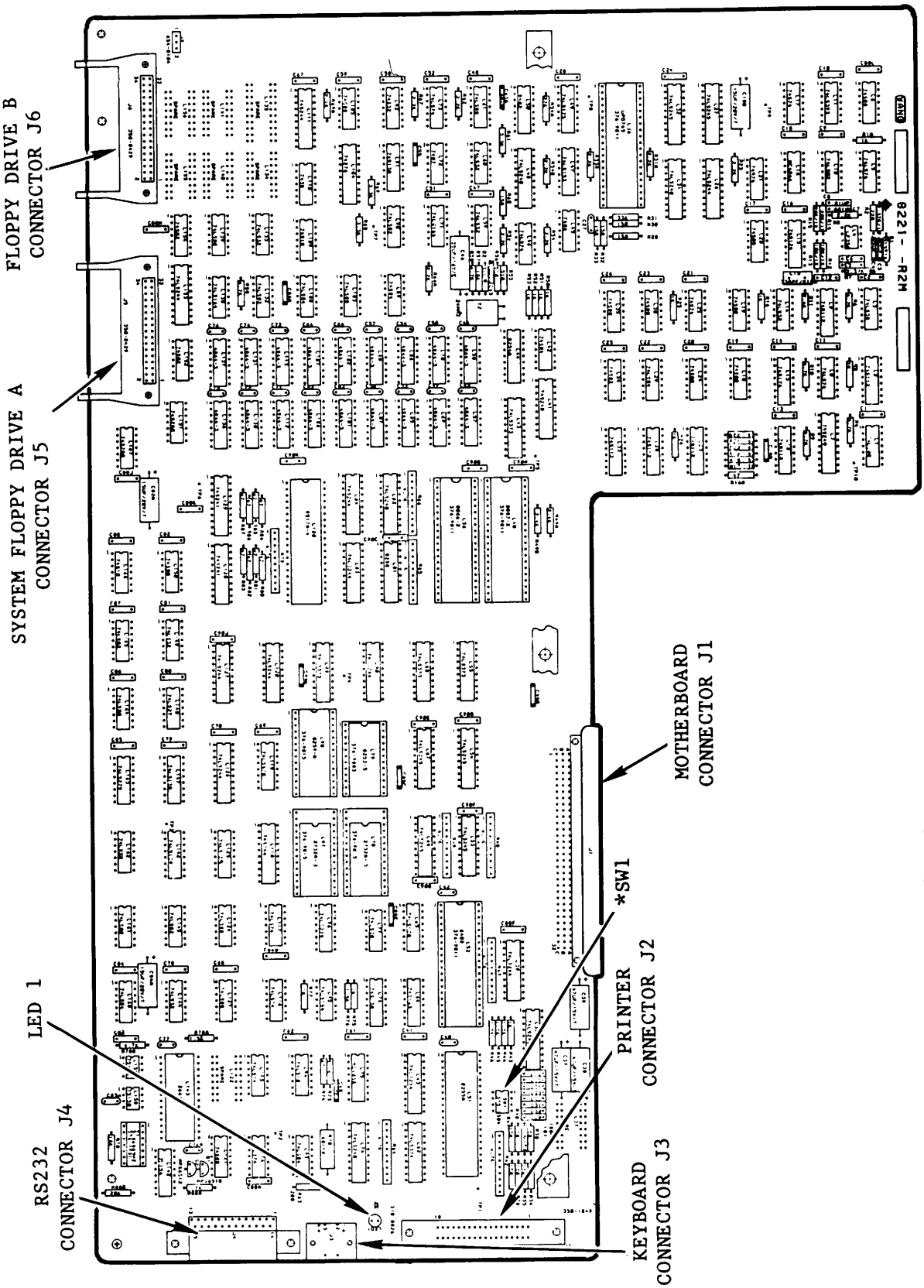


Figure 4-14. CPU System Board (210-8221)

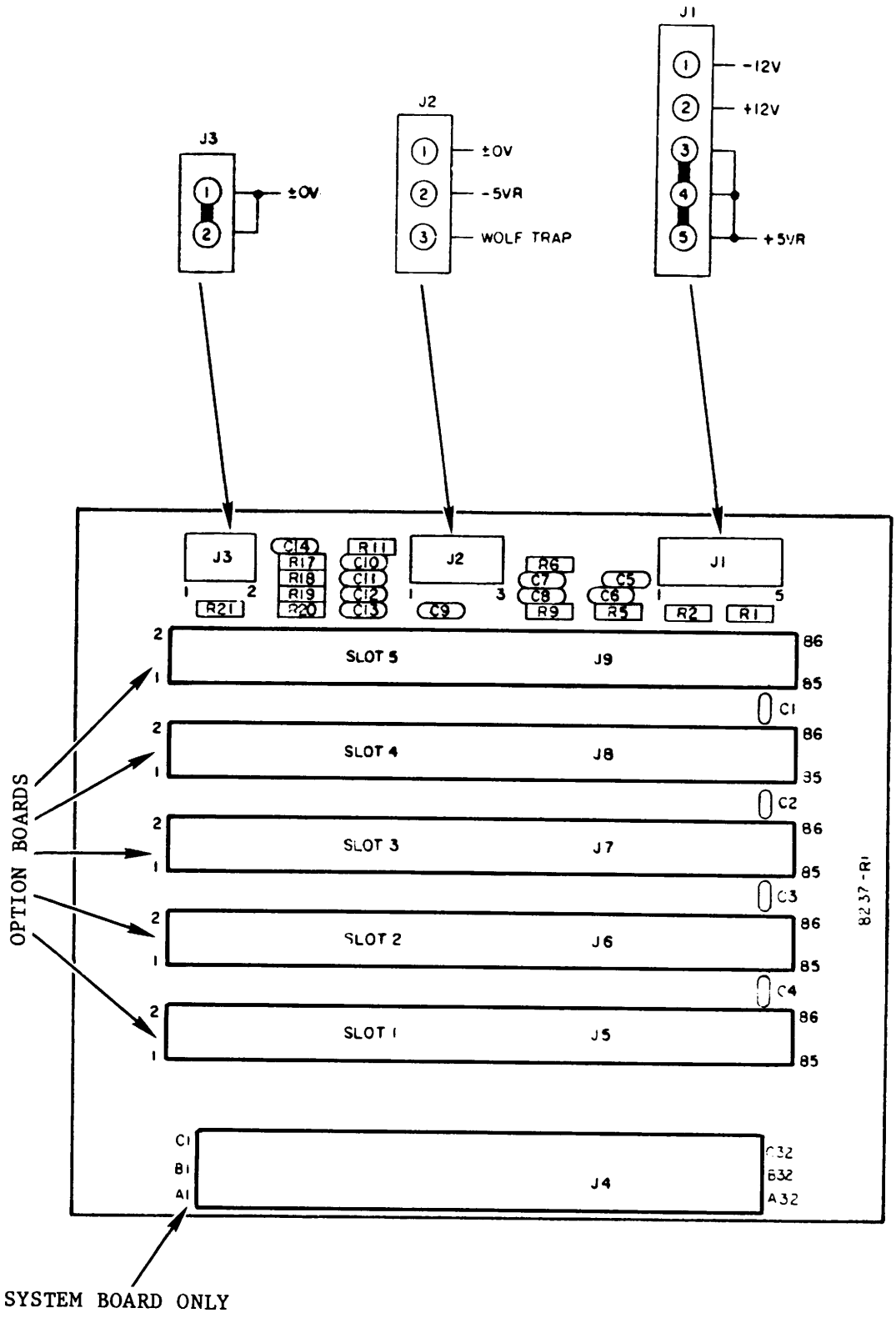


Figure 4-15. Motherboard (210-8237)

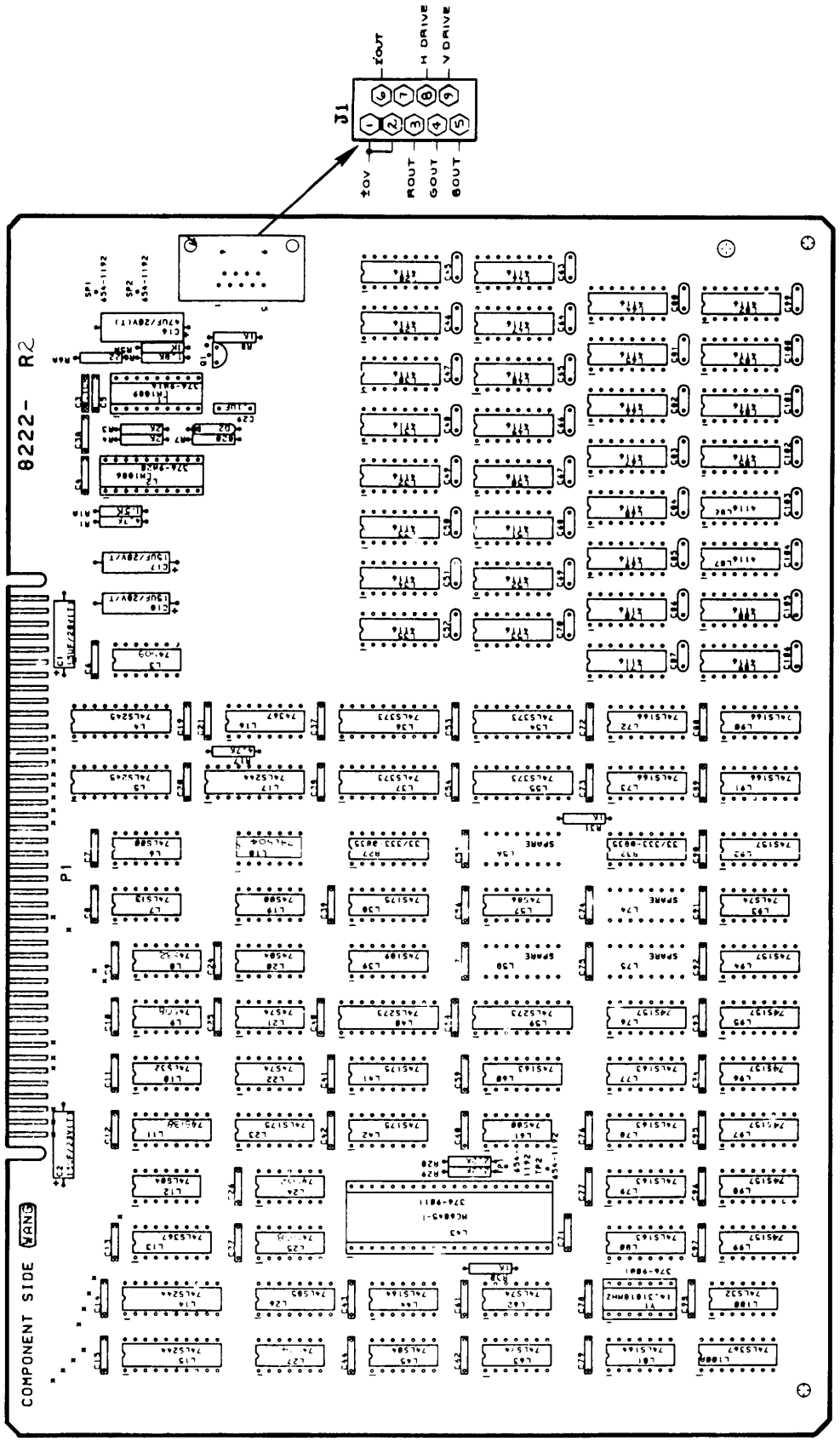


Figure 4-16. Low Resolution Board (210-8222)

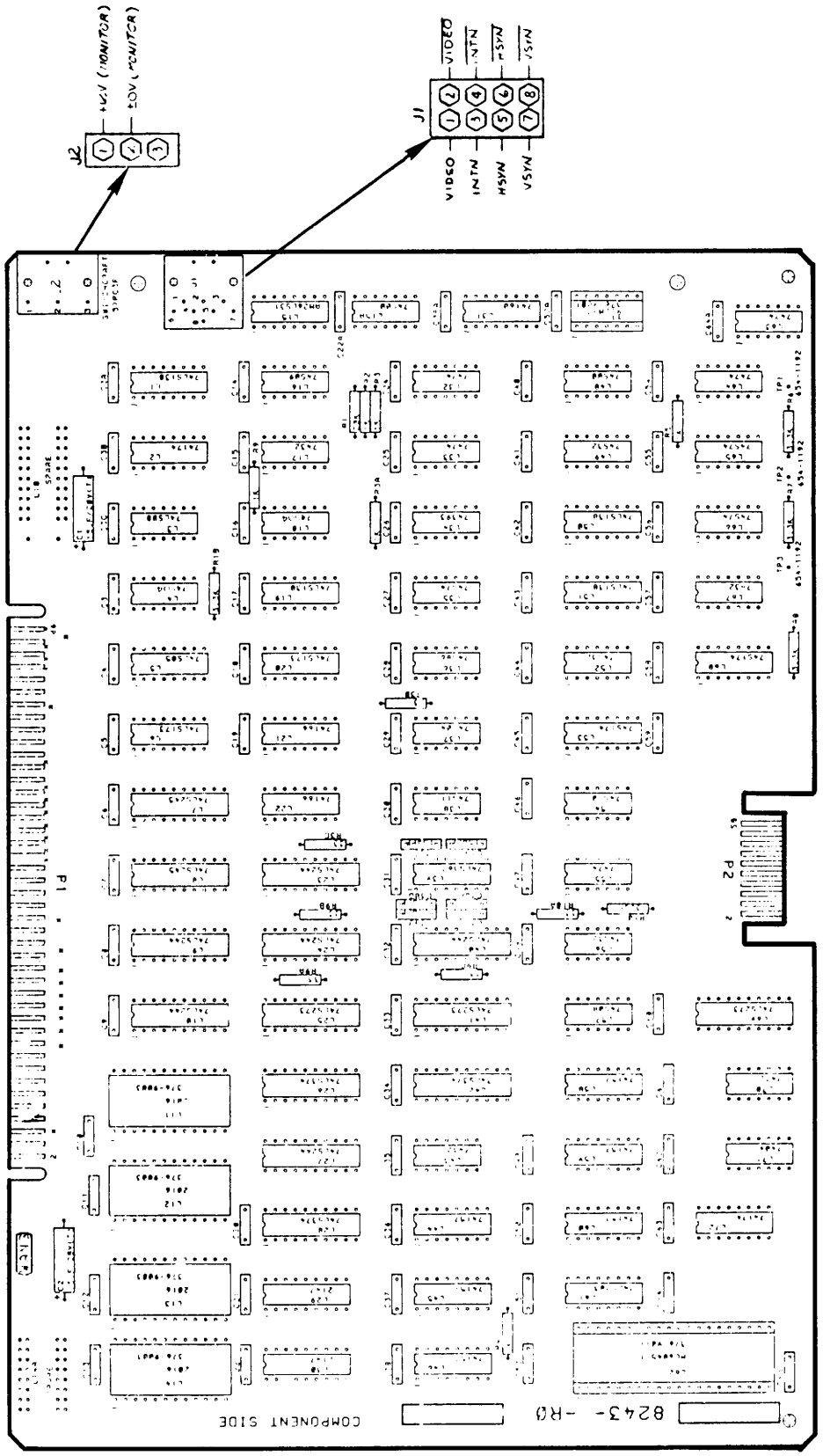


Figure 4-17. Character Resolution Board (210-8243)

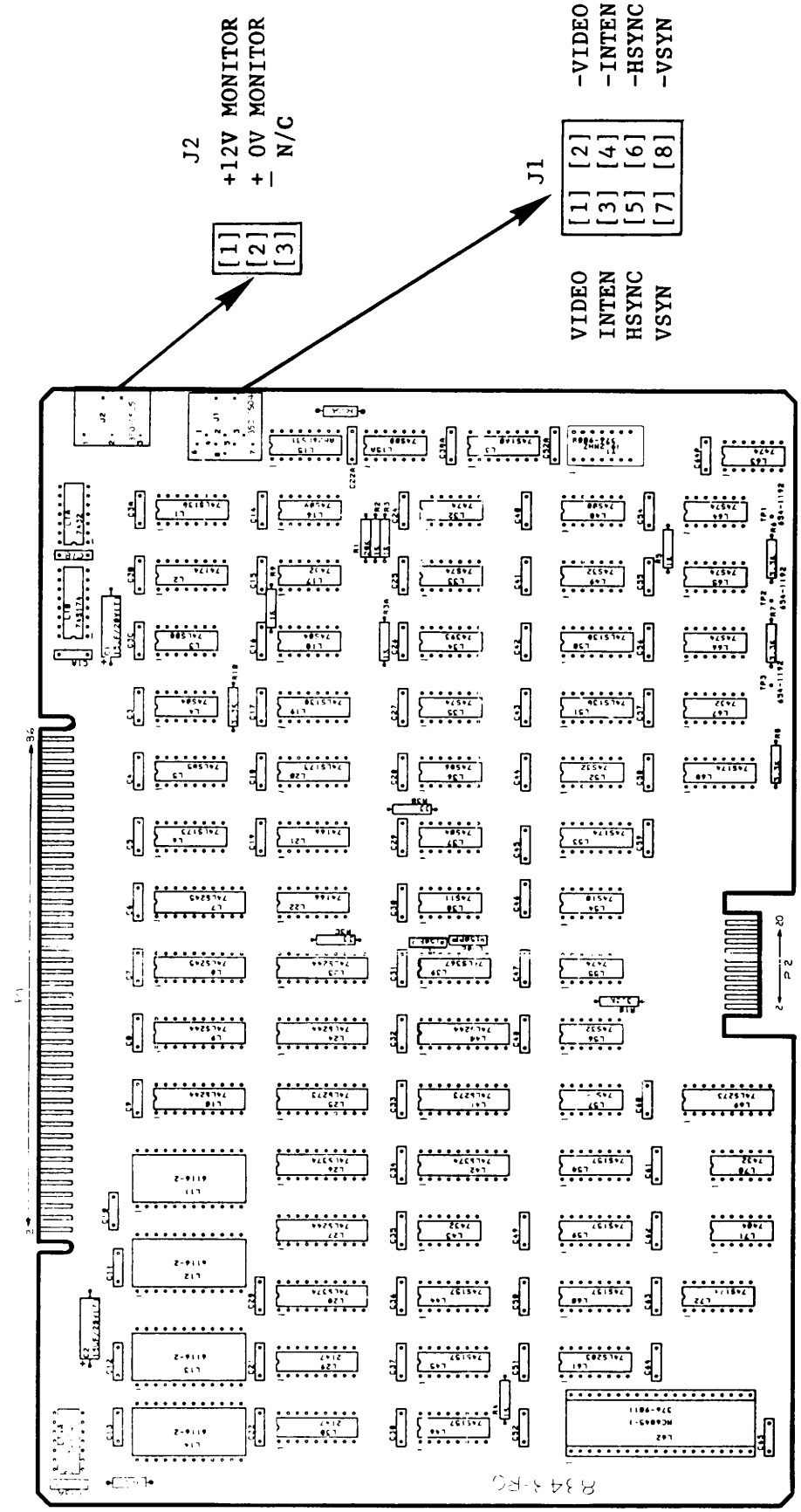


Figure 4-18. Character Resolution Board (210-8343)

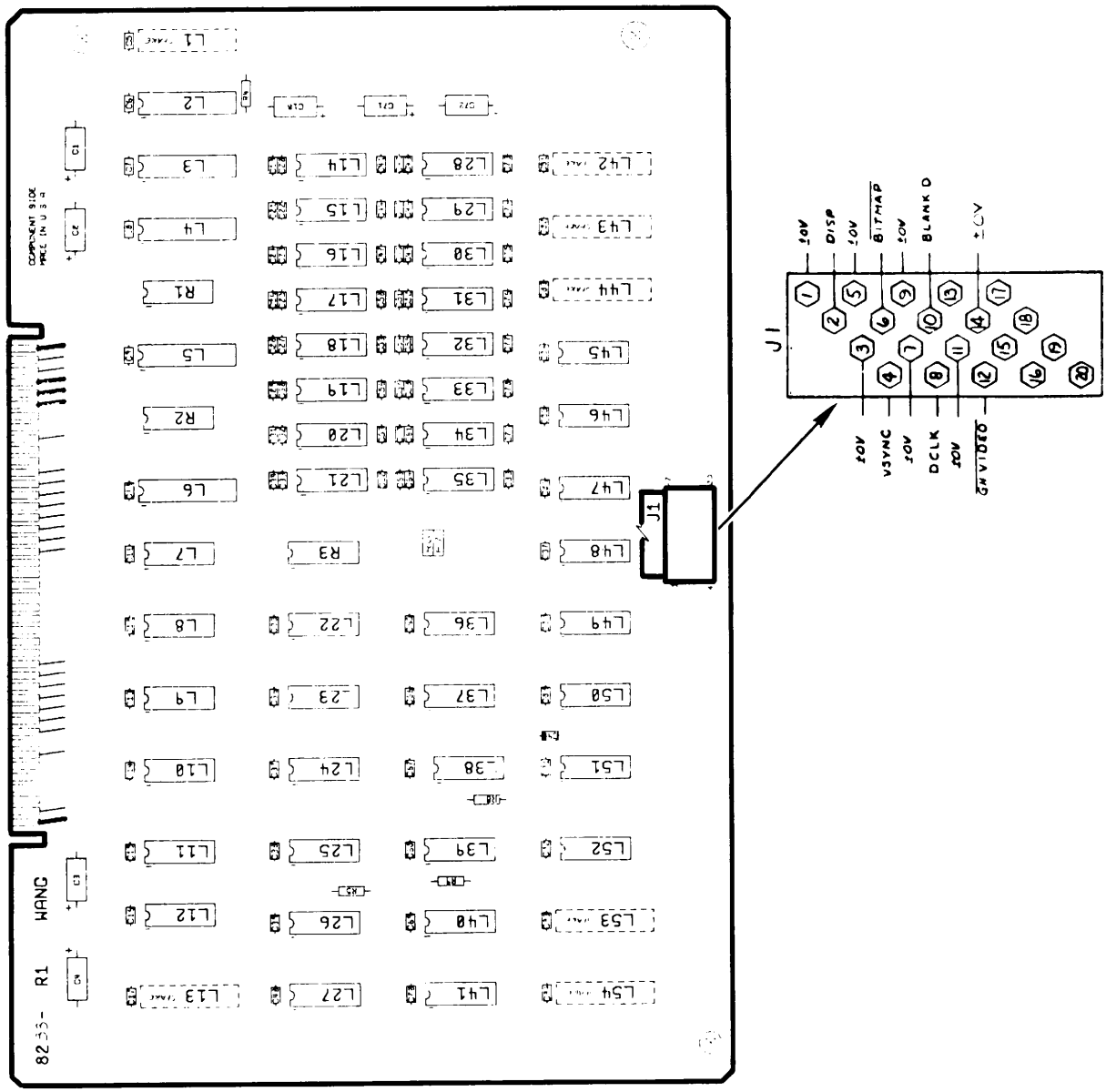


Figure 4-19. Graphics Resolution Board (210-8233)

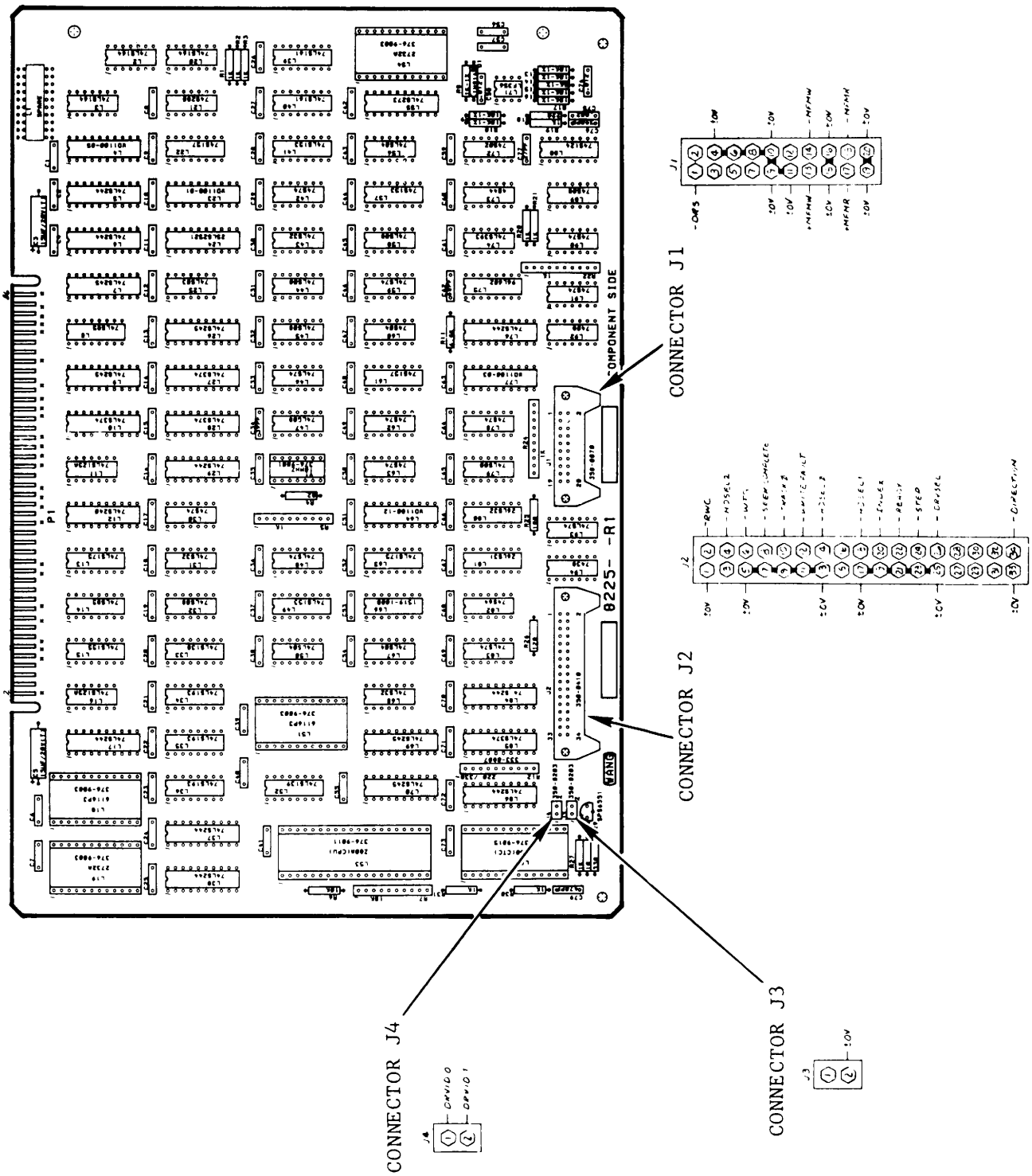
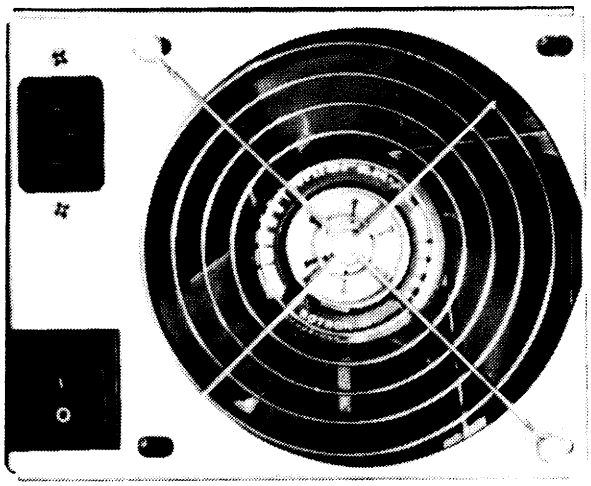
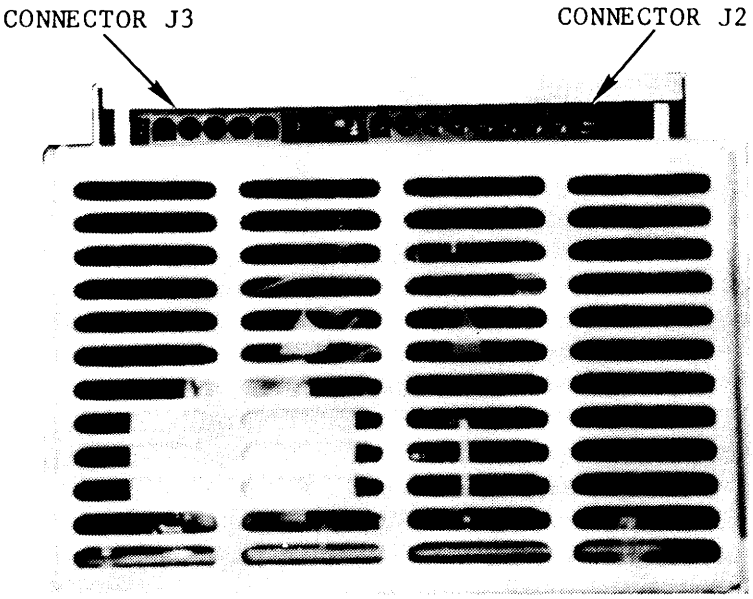


Figure 4-20. Winchester Controller Board (210-8225A)



REAR VIEW



FRONT VIEW

Figure 4-21. Wang Switching Power Supply (270-0792)

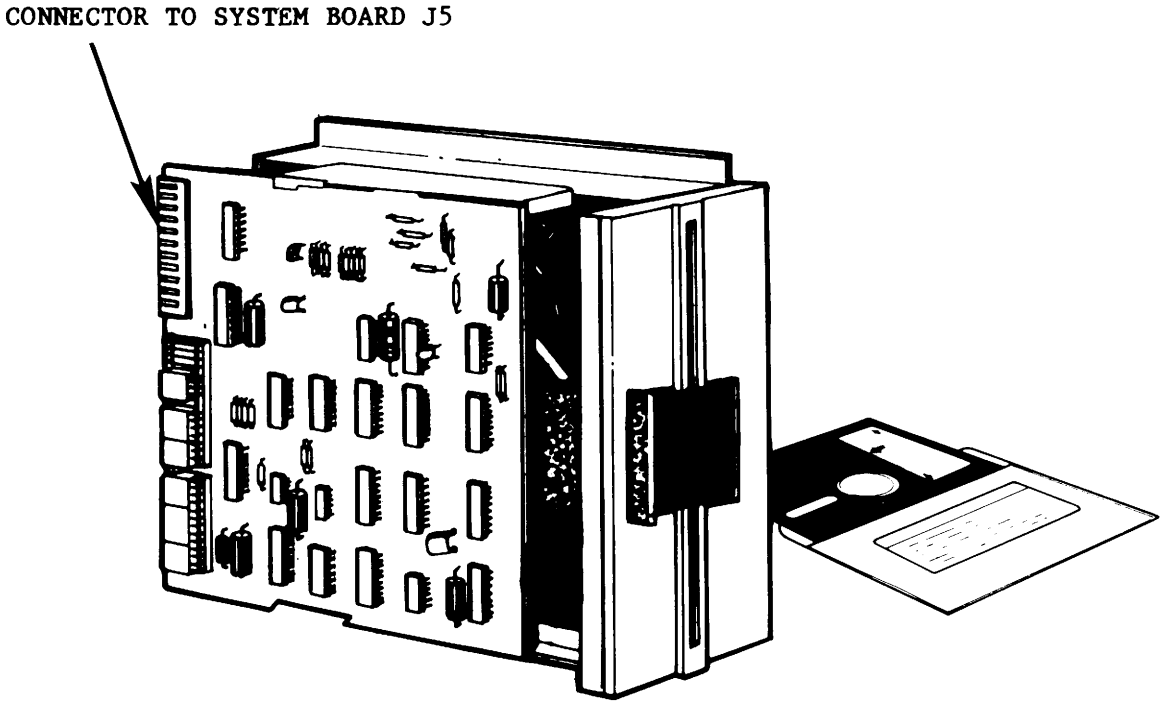


Figure 4-22. Floppy Disk Drive A (Drive B Optional)(278-4026))

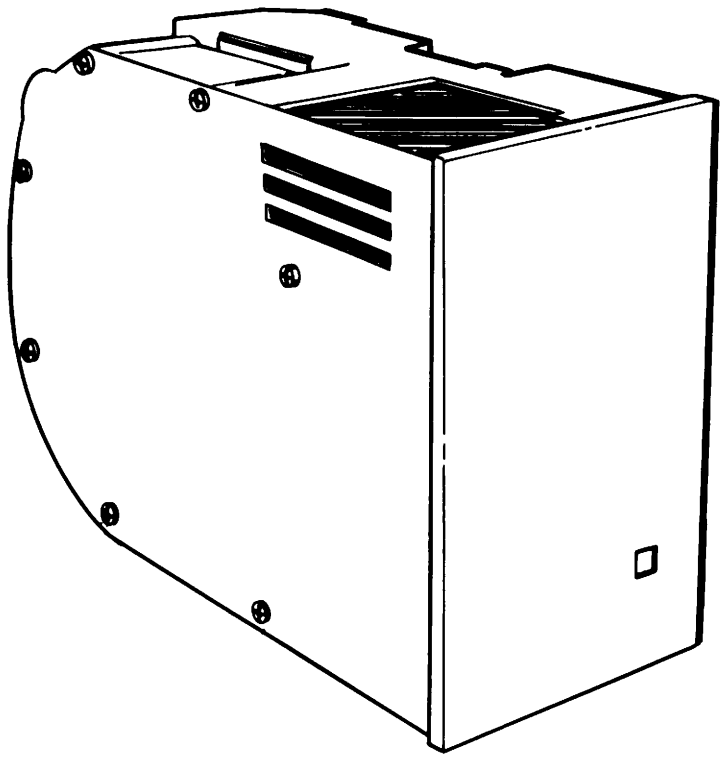


Figure 4-23. Winchester Drive (Drive C Optional) (278-4030)

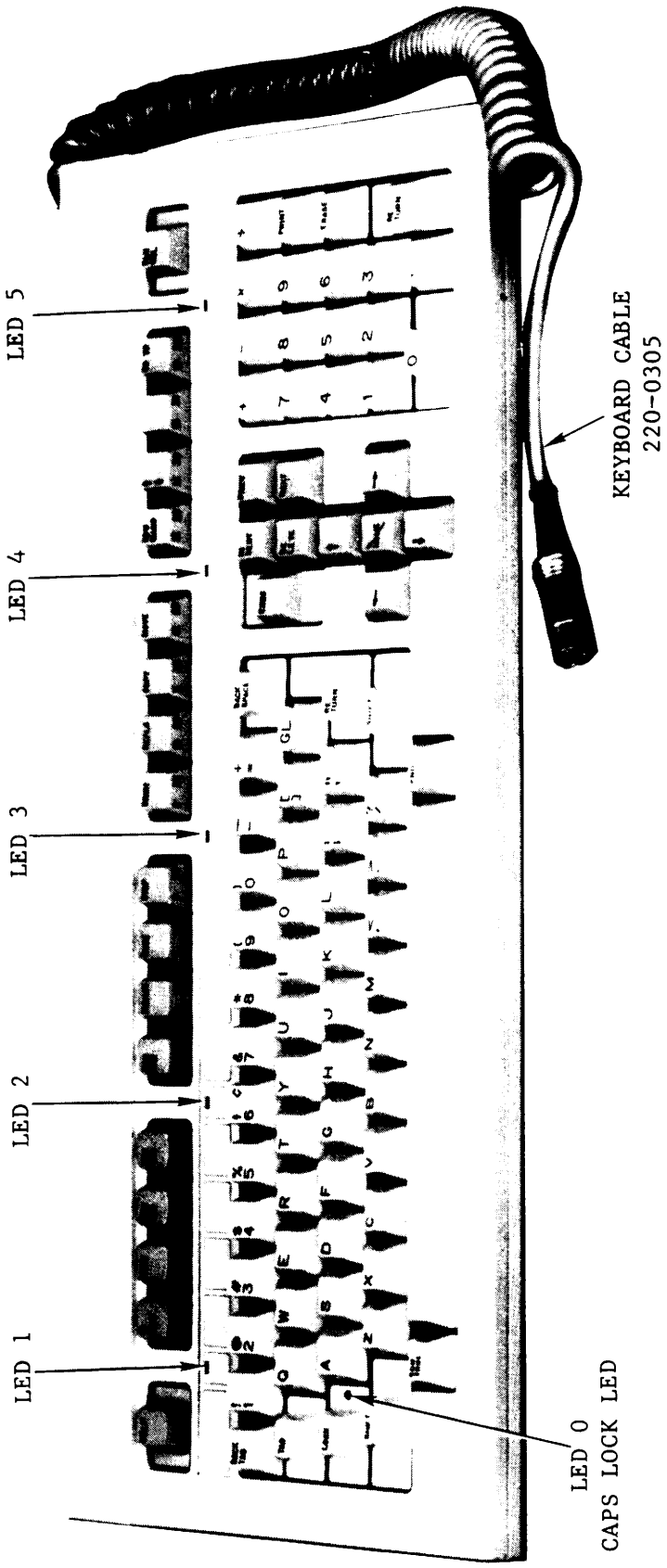


Figure 4-24. Low-Profile Serial Keyboard (279-2042)

4.6.2.3 VIDEO MONITOR

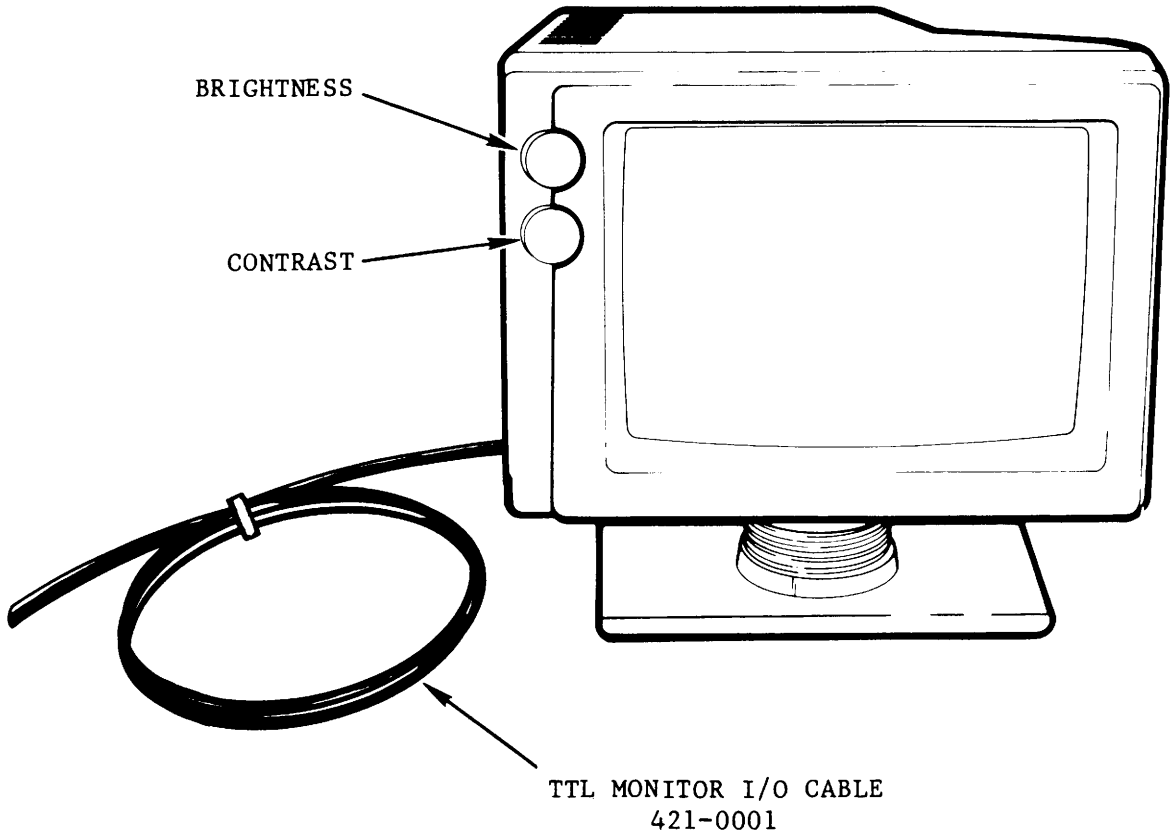


Figure 4-25. TTL Monitor Assembly (279-0541)

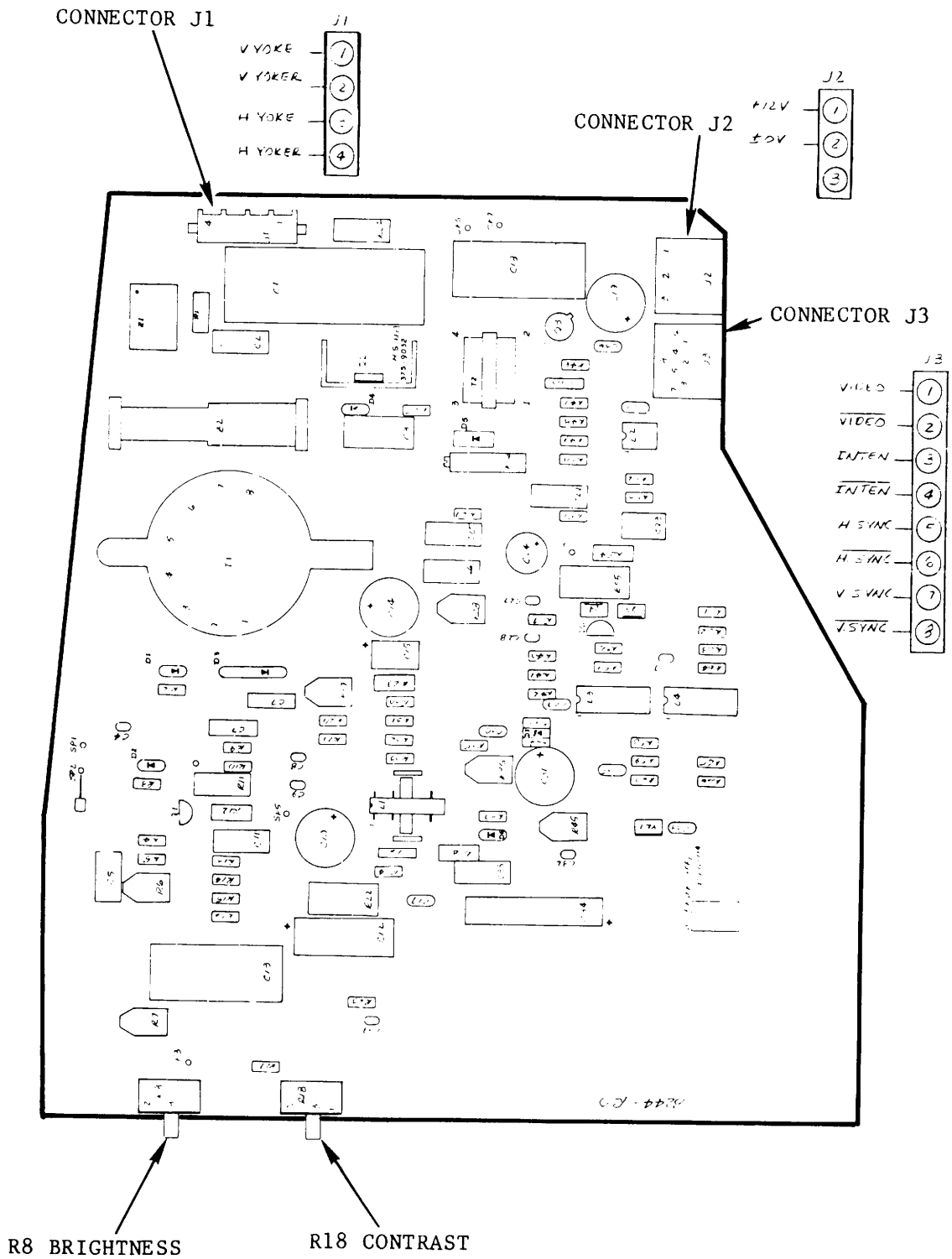


Figure 4-26. Monitor Electronics Board (210-8244)

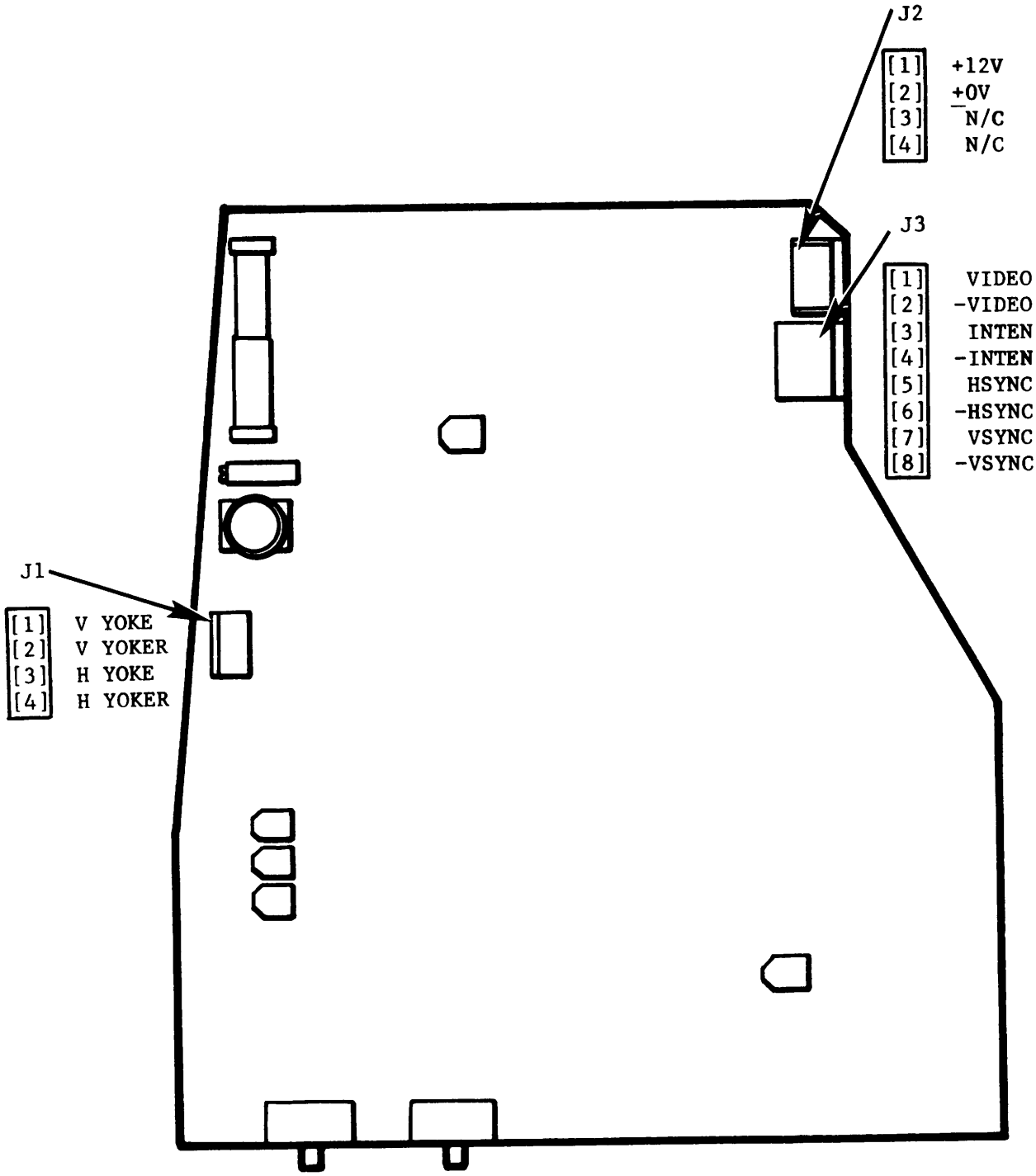


Figure 4-27. Monitor Electronics Board (210-8344)

4.6.2.4 PRINTERS (OPTIONAL)

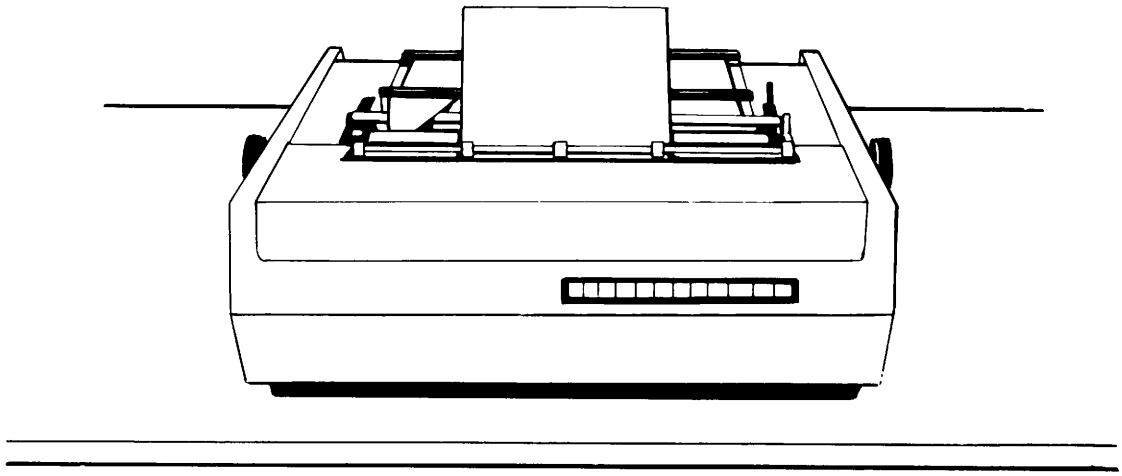


Figure 4-28. Wang Daisy DW20

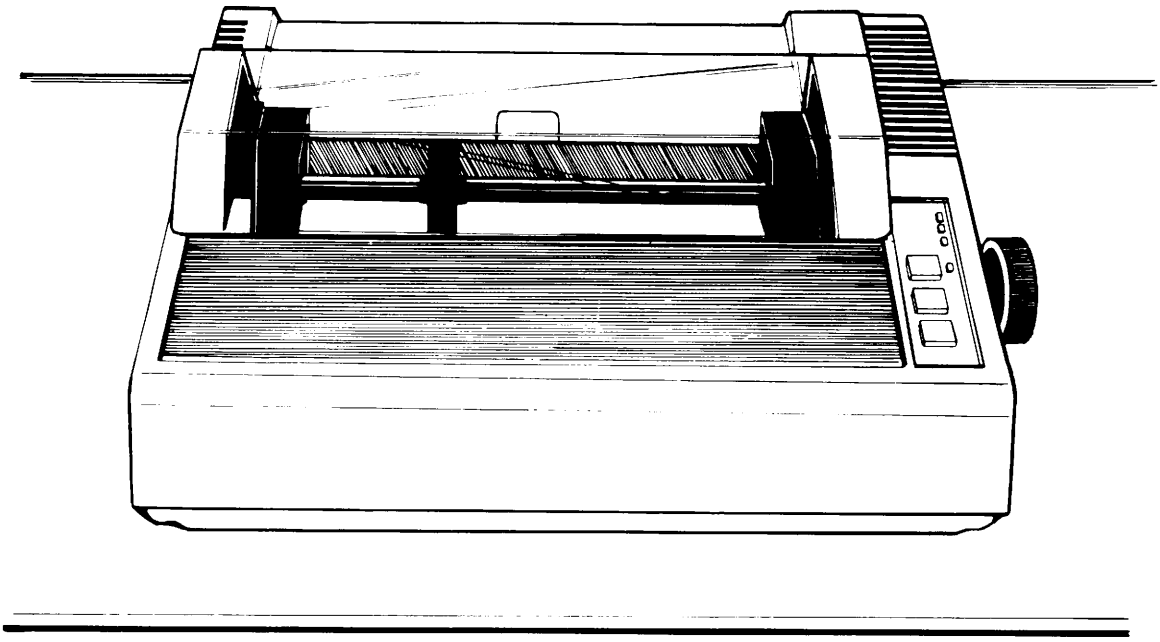


Figure 4-29. MX-80FT TYPE III Printer (725-0129)

4.7 SWITCH SETTINGS

Before powering-up the System, ensure that the switch settings are set as described below. There are six Switch settings which should be checked. These are:

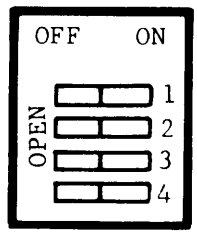
SW1 Located on the System Board PCB.
115V/230V Switch located on the Switching Power Supply.
SW1 and SW2 Located on the Keyboard PCB.
SW1 and SW2 located on the MX-80FT TYPE III Printer (if used).

4.7.1 System Board Switch Setting

The System Board 4-Position DIP Switch SW1 (see Figure 4-14 for location) is the Baud Rate Default Select for RS232 Asynchronous communications. The Baud Rate is software selectable and can override the Default Switch setting. This switch should be set according to the Baud transmit rate as determined by the protocol used. The Baud Rate switch setting is shown in Table 4-1.

Table 4-1. Baud Rate Selection Table

SWITCH SETTING 1 2 3 4	BAUD RATE
0 0 0 0	**
0 0 0 1	75
0 0 1 0	110
0 0 1 1	134.5
0 1 0 0	150
0 1 0 1	300
0 1 1 0	600
0 1 1 1	1200
1 0 0 0	1800
1 0 0 1	2000
1 0 1 0	2400
1 0 1 1	3600
1 1 0 0	4800
1 1 0 1	7200
1 1 1 0	9600
1 1 1 1	19200



SW1

** Denotes loop on power-up diagnostics. Refer to paragraph 4.13.

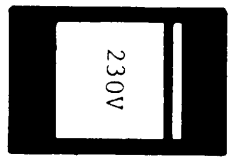
0 Denotes ON (CLOSED)
1 Denotes OFF (OPEN)

4.7.2 115/230V Switch Setting

Located on the Power Supply (accessible from the outside of the Power Supply assembly see Figure 4-30) is the 115V/230V Voltage Select Switch SW1. This Switch should be checked for the proper setting dependent upon the input voltage level. This switch has two setting, these are:

115V showing denotes 115V ac power source input.
230V showing denotes 230V ac power source input.

115V Source



230V Source

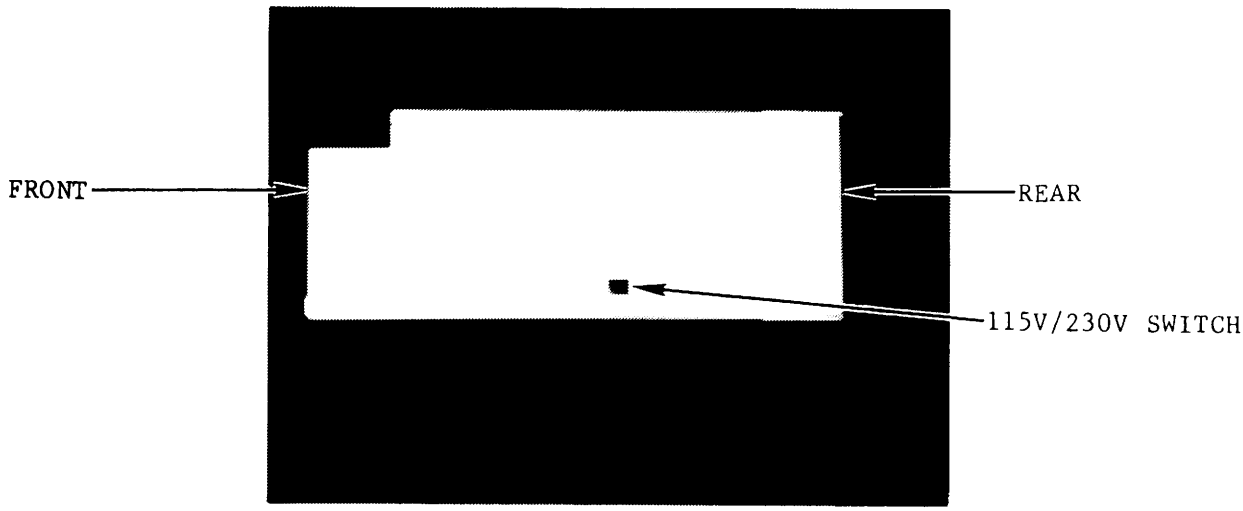


Figure 4-30. 115V/230V Switch Location

4.7.3 Keyboard Switch Setting

The Universal Low Profile Keyboard PCB contains two 8-position DIP Switches SW1 and SW2. These switches are not used for PC applications. Both DIP Switches should be set to the OFF position. See Figure 4-31 for switch locations. Refer to Chapter 5 paragraph 5.5.3 Keyboard Disassembly for access to the Keyboard PCB.

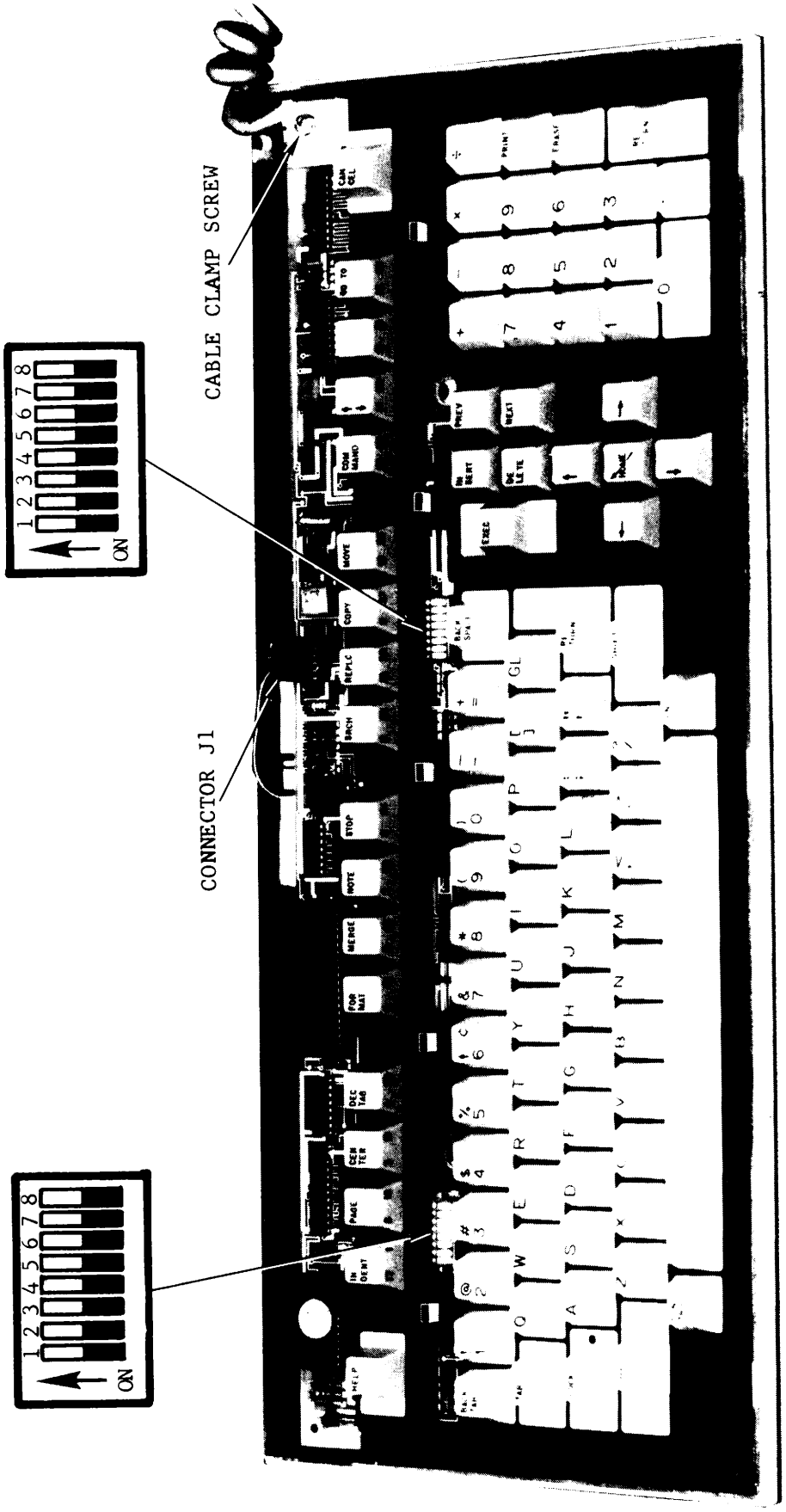


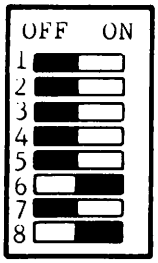
Figure 4-31. Low-Profile Keyboard DIP Switch Locations

4.7.4 MX-80FT TYPE III Printer Switch Setting

The MX-80FT TYPE III Printer (optional) has two DIP Switches, an 8-position DIP Switch SW1 and a 4-position DIP Switch SW2. These DIP switches are located on the Printer's HMPT BOARD as shown in Figure 4-32. (Refer to CUSTOMER ENGINEERING REPRINT FOR EPSON MX-80 PRINTER MANUAL 729-0976.) The default switch setting for the MX80FT Printer is defined in Table 4-2.

Table 4-2. MX80FT TYPE III Switch Setting

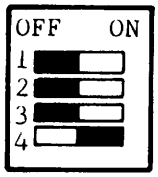
SWITCH 1



SW1

SWITCH SETTING	DEFAULT SETTING
1-1	OFF
1-2	OFF
1-3	OFF
1-4	OFF
1-5	OFF
1-6	ON
1-7	OFF
1-8	ON

SWITCH 2



SW2

SWITCH SETTING	DEFAULT SETTING
2-1	OFF
2-2	OFF
2-3	OFF
2-4	ON

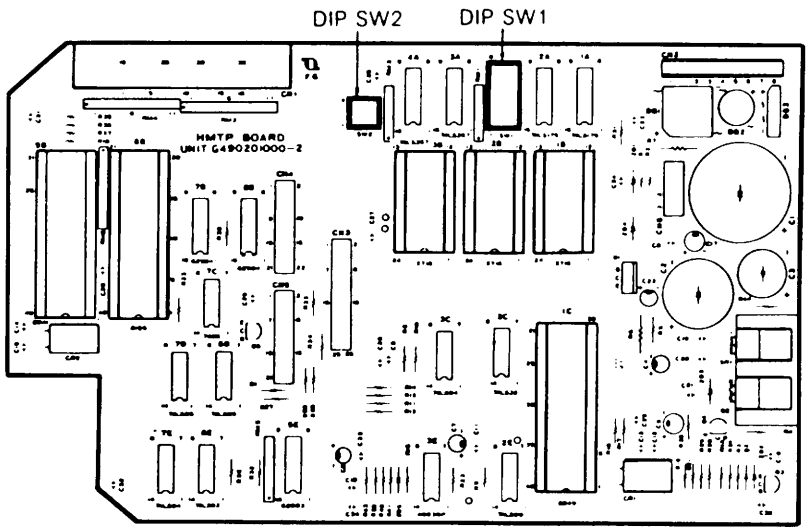


Figure 4-32. MX-80FT TYPE III Printer Switch Locations

4.7.5 DW-20 Printer

No switch settings are required for the DW 20 Printer.

4.7.6 System Floppy Drive

One of two floppy drives can be used, Tandon or MPI. Only the System Floppy Drive A has the terminator chip installed (see Figure 4-33 for location). Check the System Drive A and the optional Floppy Drive B (if any) for correct configurations. If a Floppy diskette and a Winchester drive are used, both must have the terminator chip installed.

TANDON DISK DRIVE

Both the System Floppy Drive A and the Optional Floppy Drive B (if used) must have the 14-pin Programmable Shunt jumper pins 2 to 13 (DS1) installed. All remaining jumpers are removed. The Floppy's Programmable Shunt is installed in a 16-pin I.C. socket. ENSURE THAT THE SHUNT'S PIN 1 IS INSTALLED IN PIN 1 OF THE SOCKET. See Figure 4-34 for Floppy Shunt Jumper Identification and Figure 4-33 for the Programmable Shunt Socket location.

MPI DISK DRIVE

Both the System Floppy Drive A and the Optional Floppy Drive B (if used) must have the 12-pin Programmable Shunt jumper pins 1 to 12 (DS0) and 6 to 7 (HM) installed. All remaining jumpers are removed. The Floppy's Programmable Shunt is installed in a 14-pin I.C. socket. ENSURE THAT THE SHUNT'S PIN 1 IS INSTALLED IN PIN 2 OF THE SOCKET. See Figure 4-34 for Floppy Shunt Jumper Identification and Figure 4-33 for the Programmable Shunt Socket location.

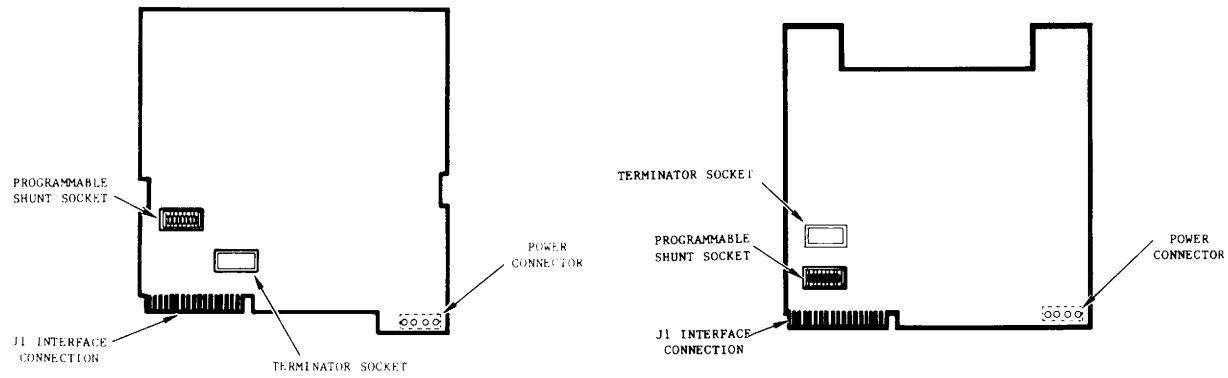
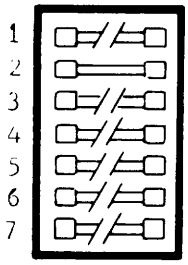


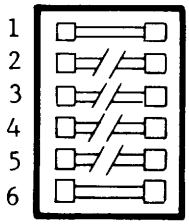
Figure 4-33. Floppy Drive Programmable Shunt Location

TANDON SHUNT



HS = HEAD SELECT
DS1 = DRIVE SELECT 1
DS2 = DRIVE SELECT 2
DS3 = DRIVE SELECT 3
MUX = MULTIPLEX
DS4 = DRIVE SELECT 4
HM = HEAD MOTOR

MPI SHUNT



DS0 = DRIVE SELECT 0
DS1 = DRIVE SELECT 1
DS2 = DRIVE SELECT 2
MUX = MULTIPLEX
DS3 = DRIVE SELECT 3
HM = HEAD MOTOR

Figure 4-34. Floppy Drive Shunt Identification

4.8 INSTALLATION

The installation of the PC consists of only four connections that have to be made. These are:

- Connecting the Keyboard
- Connecting the Monitor
- Connecting the ac Power Cord
- Connecting the Printer (Optional)

The first 200 Professional Computers systems were manufactured with Composite Video Character Display boards (210-8223) and Monitor boards (210-8227). The Monitor I/O cable was permanently attached to the Monitor Assembly. Composite Video systems are obsolete and should never be sold to the customer.

From unit 200 and above, PC systems were manufactured with TTL Character Display boards (210-8243) and Monitor boards (210-8244). The Monitor cable (421-0001) is now detachable and has DIN type connectors. In addition, the TTL Monitor plastic covers are made different and are not compatable with the Composite Video Monitor.

The Composite Video type boards, cables, and Monitor are NOT interchangeable with the TTL Video type.

4.8.1 System Unit Installation

Ensure that the Electronics unit contains all the PCB's that are required for operation of your system configuration. If you are using the Wang Monochrome Monitor, then the Medium Resolution Character Generator board 210-8243/8343 must be installed. If you are using a RGB or B/W Video monitor or a Television, then the Low Resolution board 210-8222 must be installed.

If there are five black panels covering the expansion slots, then you have a Base Unit. If this is the case, you must install a video card in the Electronics Unit before you can connect your system. Refer to Chapter 5 paragraph 5.5 System Disassembly for the procedures to disassemble the Electronics Unit and to install an option board.

4.8.2 Connecting The Keyboard

Locate the keyboard connector on the back panel of the Electronics Unit labeled J3. See Figure 4-12. Connect the plug on the end of the keyboard cable to the keyboard connector located on the back panel. The Keyboard connector and the Keyboard cable plug are keyed allowing the plug to be installed in only one way. Be sure to align the pins in the plug to the connector to prevent damaging either of the two.

4.8.3 Connecting The Monitor

The Wang Character Resolution board 210-8243/8343 has two connectors on it as shown in Figure 4-17 (8243) or 4-18 (8343). The card can be installed in any one of the five slots within the electronics unit and not necessarily were shown in Figure 4-12. Locate the two connectors at the end of the monitor's cable. Connect the eight pin plug (Video) into the connector labeled J1 located on the Character Resolution board. Connect the other plug (Voltage) into the bottom connector labeled J2 on the Character Resolution board.

4.8.4 Connecting The AC Power Cord

****
* CAUTION *
*
* BEFORE CONNECTING THE AC POWER CORD, BE SURE THE *
* POWER SUPPLY ASSEMBLY IS SET FOR THE APPROPRIATE *
* VOLTAGE RATING AS DESCRIBED IN PARAGRAPH 4.7.2. *
*
****

Connect the ac power cable to the three prong ac power connector located on the rear of the Electronics Unit. See Figure 4-12. Secure the power cord to the back panel by screwing the two flathead screws to the posts on each side of the power cord connector. BE SURE THAT THE ON/OFF SWITCH LOCATED NEXT TO THE AC POWER CONNECTOR IS IN THE OFF (O) POSITION. Connect the three prong ac plug into an ac wall socket to complete the installation.

The monitor and keyboard are now connected to the electronics unit. The power switch (RED) located on the electronics unit controls the power sent to all three components. As a result, whenever you Power-On the Electronics Unit both the Monitor and the Keyboard are also powered-on.

4.8.5 Connecting The Printer (Optional)

NOTE

WHEN USING THE EPSON MX-80FT TYPE III PRINTER, ENSURE THE PRINTER SWITCH SETTING ARE CORRECT. SEE PARAGRAPH 4.7.4.

The DW20 and the MX80FT Type III printer connects to the Electronics unit parallel port J2. To connect the printer, simply insert the printer cable into the appropriate connector on the back panel of the Electronics Unit. Then tighten the two screws on either side of the cable connector to fasten the cables in place. See Figure 4-35 for Printer connections. Plug the printers ac power cord into an ac wallout to complete the installation.

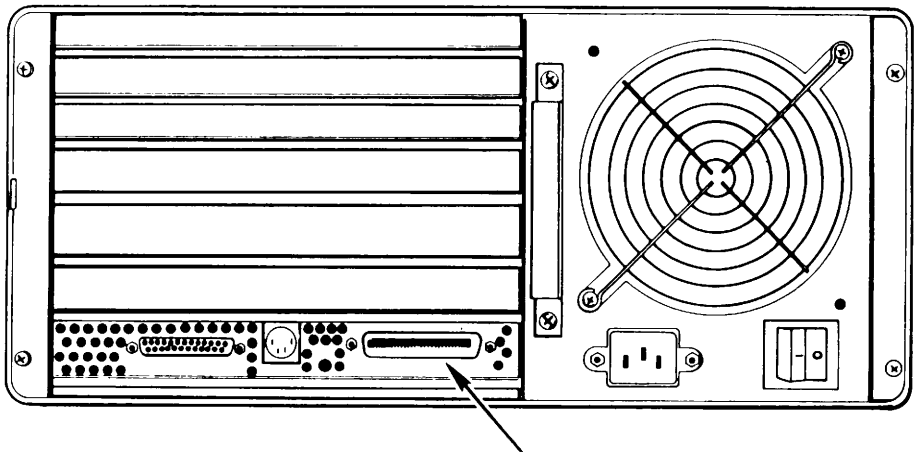


Figure 4-35. Printer Cable Connector

4.9 SYSTEM EXPANSION

The procedures required to expand the Wang Professional Computer are described in this section. There are two types of system expansion; one is the addition of a Option PCB, the other is the addition of a second diskette drive (Drive B) or a Winchester drive (Drive C).

NOTE

THE WINCHESTER CONTROLLER BOARD (210-8225A) MUST BE INSTALLED IN OPTION SLOT 5 DUE TO CABLE RESTRICTIONS.

4.9.1 Installing An Option PCB

To install an option PCB, perform the following:

1) With the System Unit Powered-down, the ac Power ON/OFF Switch OFF (O) disconnect all cables (ie. monitor cable, keyboard cable, ac power cord, etc.) from the rear of the Electronics Unit. The Electronics Unit should be free of any external cables before you proceed.

4.9.1 Installing An Option PCB (Cont'd)

2) Position the Electronics Unit as shown in Figure 4-36. Unscrew the four Phillips head screws located in the corners of the back panel. Put one hand on the handle on the back panel and place your other hand firmly on top of the electronics unit and pull the electronics unit's chassis out of its cover. Hold the cover in place with one hand while pulling on the handle with your other hand.

3) Move the cover off to one side of your work area and position the Electronics Unit into the vertical position as shown in Figure 4-37.

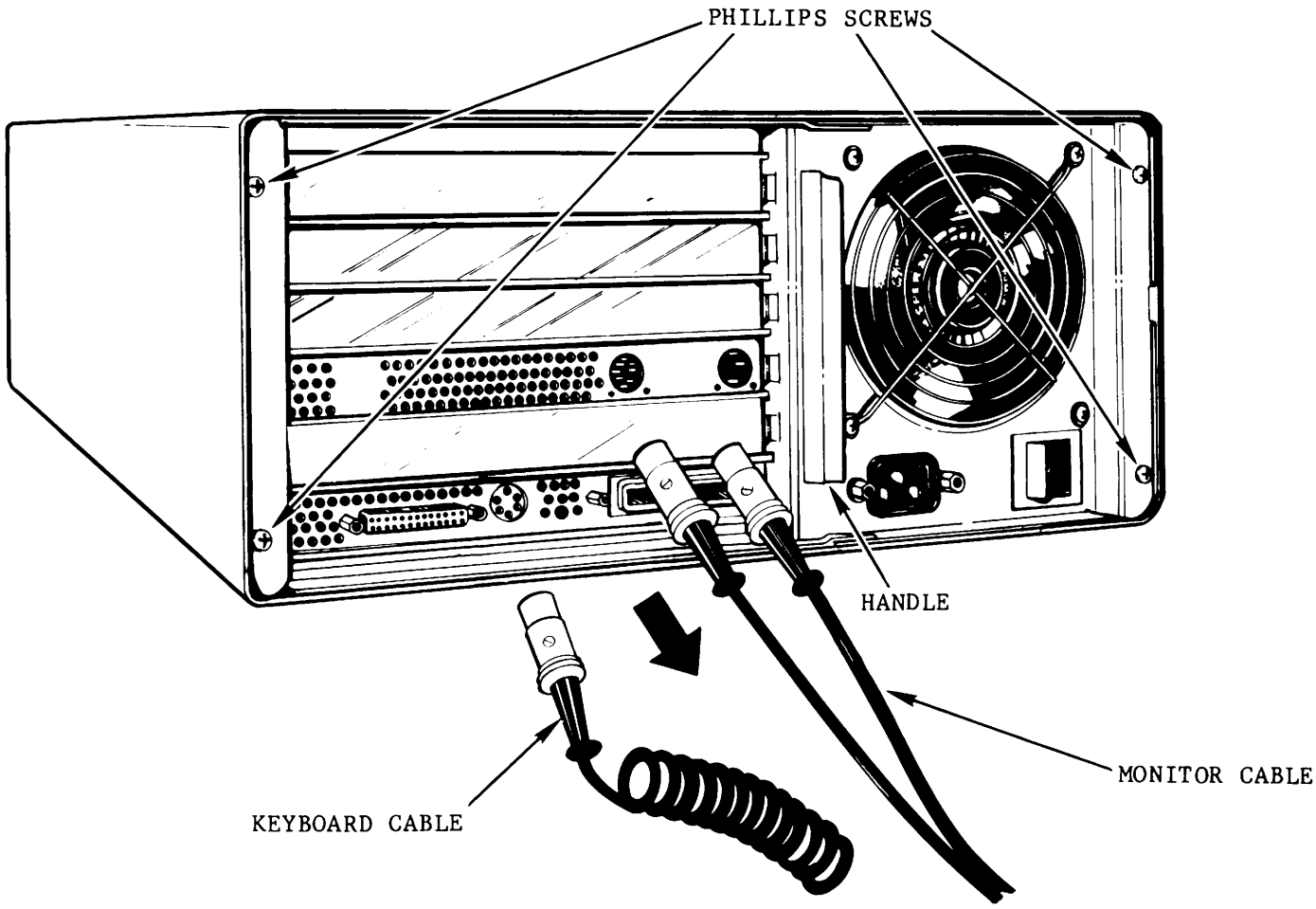


Figure 4-36. Electronic Unit Rear View

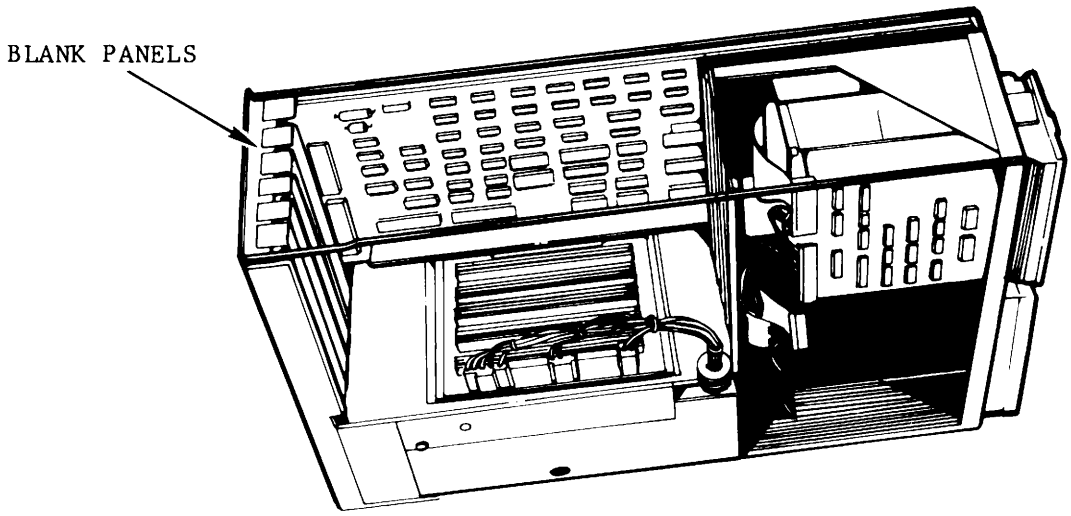


Figure 4-37. Electronics Unit Vertical Position

4) Unscrew the screw on the top of the panel that's occupying the space where the PCB is to be inserted. To remove the panel, push up on the panel from underneath, then slide the panel up and out of the back panel.

5) Align the PCB to be installed (edge connector downward) above the Electronics Unit so that the component side of the PCB is facing away from the CPU System Board.

6) Slide the PCB into the card guides while ensuring the PCB aligns with the interlocking guides on both sides.

7) Firmly press the PCB's edge connector into the Motherboard's option slot. The lip on top of the PCB should fit flush to the top of the ledge on the chassis. The hole in the PCB's panel should line up with the hole in the chassis. Now, screw the PCB into place with the screw that was unscrewed from the blank panel in step 4.

8) This completes the option PCB installation. Repeat the procedures listed above for all other option PCB's to be installed.

4.9.2 Installing a 2nd Diskette Drive (Drive B)

To install a second Floppy Diskette Drive perform the following:

1) Remove the Electronic Units cover as explained in paragraph 4.9.1 steps 1 thru 3.

2) Remove the Blank Drive Panel from the chassis by removing the screw located directly under the blank panel. This screw will be used later to secure the drive in place. Now pull the blank panel directly out of the chassis. Note that the drive's metal mounting plate is attached. Remove the two screws that attach the blank panel to the drive mounting plate. This plate and the two screws will be attached to the drive to be installed. Store the blank panel with your other Wang PC packing materials.

3) Drive A has to be removed so that Drive B's cables can be threaded under Drive A. To remove Drive A, first unclip the ribbon cable from the back of Drive A's controller board. Rock the connector plug from one side to the other while pulling it off the connector. Let the cable hang free after you disconnect it.

4) Disconnect the power cable from the back of Drive A's controller board. Gently rock the connector and pull outward. Also Let the power cable hang free after you disconnect it.

5) Unscrew the screw (located on the Drives front panel) holding the drive to the chassis. Now grasp the drive and pull it completely out of the unit.

```
**********************************************************
*                        CAUTION                         *
*                                                        *
*  DO NOT LAY THE DRIVE DOWN ON ITS CONTROLLER CARD      *
*  AS THIS COULD CAUSE DAMAGE THE COMPONENTS.            *
*                                                        *
**********************************************************
```

6) Now install Drive B cable by taking the end of the ribbon cable with the thinner connector and thread it through the hole shown in Figure 4-38. When correctly threaded, the holes on the connector should face away from you.

7) Open the jaws of connector J6 located on the system board. Each side snaps open. Insert the connector on the ribbon cable into the connector on the system card. Check that the connector is correctly seated and snap the jaws closed.

8) Now take the other end of the ribbon cable and drop it through the hole in the chassis between the two drives. See Figure 4-38.

9) Use the cable clip shown in Figure 4-38 to turn the cable in the proper direction for its connection to Drive B. Follow the sequence of steps shown in Figure 4-38 to fold the cable correctly. When correctly folded, slide the cable into the cable clip.

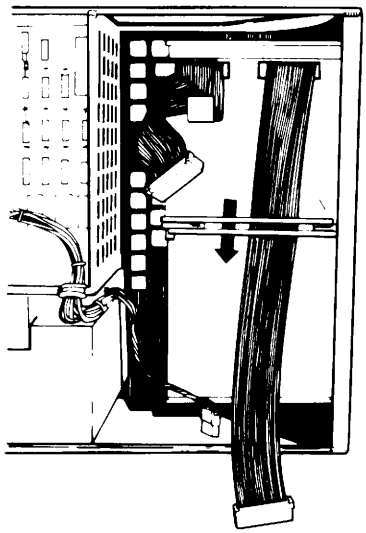
10) Install the drive metal plate removed in step 2 to Drive B. Ensure that Drive B is configured properly (refer to paragraph 4.7.6) and position Drive B with the component PCB facing to the left. Slide the drive about halfway into the chassis. Be sure that the drive's metal plate is sliding in the guides provided.

11) Connect the power cable (4 pin Plug) onto the power connector located on the diskette drive's controller card. See Figure 4-38.

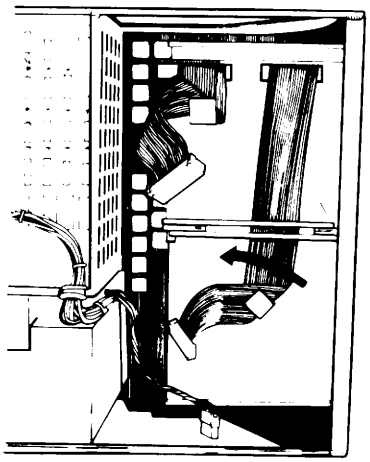
12) Now press the ribbon cable connector onto the controller card's connector, the cable should slide on easily.

13) Slide the drive the rest of the way into the chassis being careful not to crimp or damage the cables. Secure the drive in place with the screw removed in step 2.

14) Now reinstall Drive A. To install Drive A, reverse the procedures in steps 3, 4, and 5.



THREADING THE CABLE



FOLDING THE CABLE

CONNECTING THE POWER CONNECTOR

Figure 4-38 Floppy Drive Cabling

4.9.3 Installing a Winchester Disk Drive (Drive C)

To install a Winchester Disk Drive perform the following:

1) Perform the steps outlined in paragraph 4.9.1 (Installing an Option PCB) to install the Winchester Controller Board. Be sure to install this PCB in Motherboard slot 5 (J9).

2) Perform the steps 1 and 2 in paragraph 4.9.2 (Installing a 2nd Diskette Drive) to install the Winchester Drive.

3) If Floppy Drive B has to be removed prior to installing the Winchester Drive (Drive C), reverse the procedures listed in paragraph 4.9.2 (Installing 2nd Diskette Drive) steps 6 through 13.

4) The Winchester Drive cables are attached to the Winchester Controller PCB connectors J1 and J2. Connector J1 is the smaller of the two connectors. See Figure 4-39 for Winchester Drive cabling.

5) Now replace the Electronic Unit cover as described in paragraph 4.9.4.

6) Check the drive for proper operation by running the power-up diagnostics. Ensure the Winchester drive is formatted, this is accomplished by selecting the FORMAT A DISK utility on the SYSTEM UTILITIES MENU.

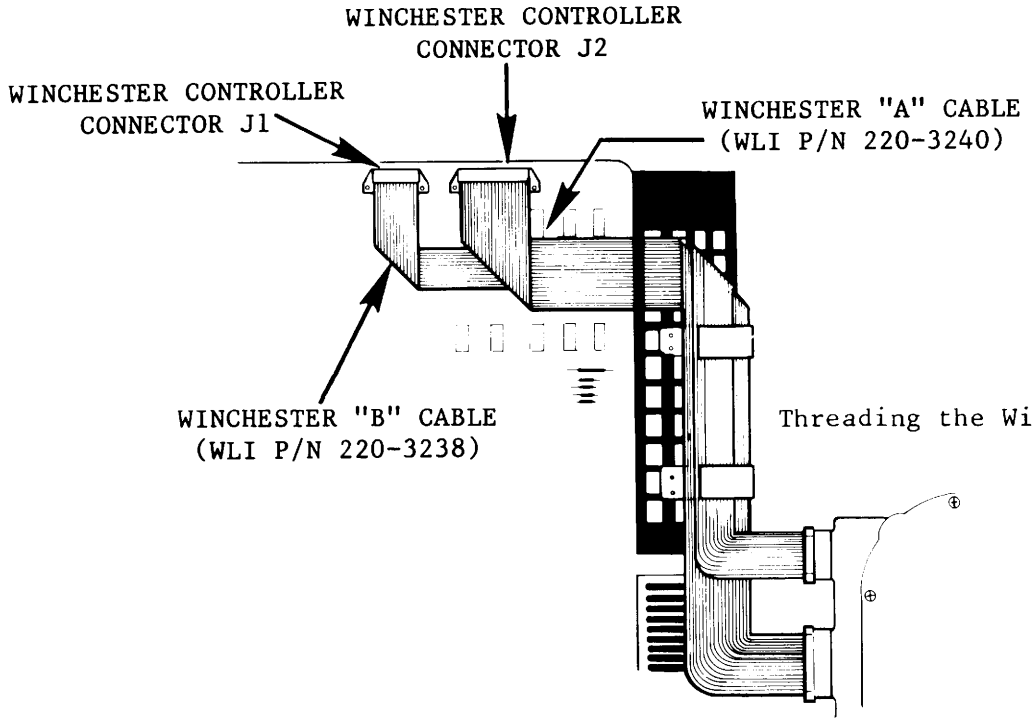
4.9.4 Replacing the Electronics Unit Cover

Before replacing the Electronics Unit cover, ensure the air vents located on the cover are pointing downward. To replace the cover, grasp each side of the chassis. Lift the chassis over the bottom edge of the cover and slowly slide the electronics unit into the cover. Place one hand on the cover while using the other hand to push on the handle on the back panel of the electronics unit. Install the four screws in the rear panel to secure the cover to the chassis. Now refer to paragraph 4.10 Powering-On The System.

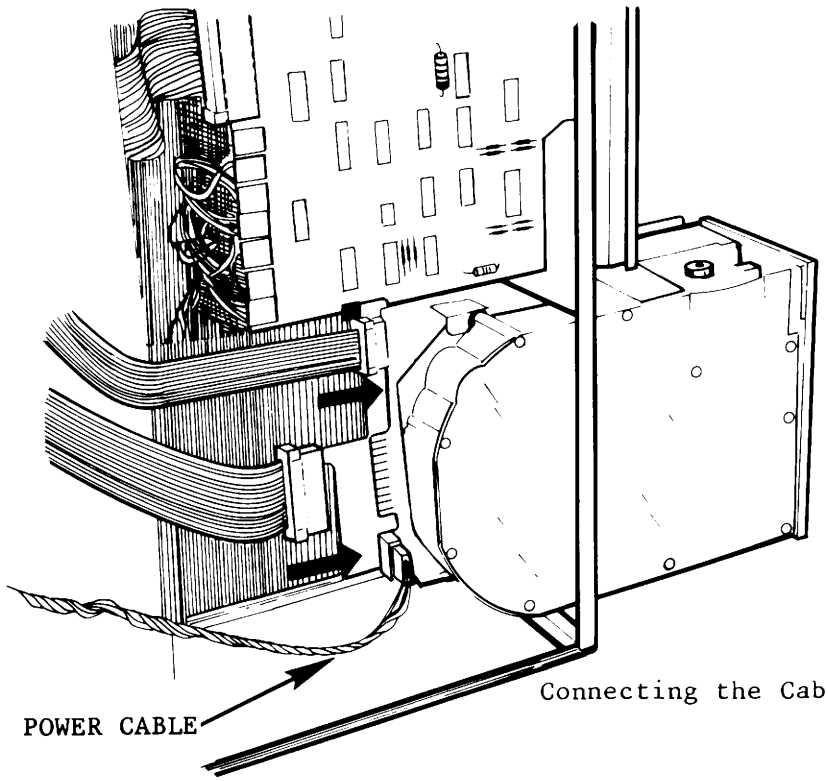
4.10 POWERING-ON THE SYSTEM

```
**************************************************************************
*                                CAUTION                                 *
*                                                                        *
*  BEFORE LOADING THE SYSTEM DISK, BE SURE THE SYSTEM IS POWERED OFF     *
*  AND THE SHIPPING PROTECTOR (S) ARE REMOVED FROM THE FLOPPY DRIVE.     *
*                                                                        *
**************************************************************************
```

Load the System diskette into Drive A. To load the diskette, open Drive A's door by pulling outward. Slide the System diskette into Floppy Drive A. Be sure the recording slot of the diskette goes into the drive first. Use the Insert and Up arrows on the orientation label to confirm that the position of the diskette is correct as you insert it in the drive. Slide the diskette completely into the drive and close the drive's door.



Threading the Winchester Cables



Connecting the Cables to the Drive

Figure 4-39. Winchester Drive Cabling

NOTE

FOR THE PURPOSE AND CLARITY OF THIS MANUAL, REVISION LEVELS (REV) ARE DENOTED x.xx. THE ACTUAL REVISION LEVEL DISPLAYED DENOTES THE LEVEL OF SOFTWARE BEING RUN.

Power-On the System by moving the power switch to the ON (I) position. During initial Power-On, the system will run a series of Power-On diagnostic tests. These tests will run every time the system is powered-on. While the tests are running, you'll notice that the six red indicator lights on the keyboard light up. If your system is operating correctly, the indicator lights will all go off after ten seconds to a maximum of 30 seconds and the start-up display message will appear on the screen as shown.

```
WANG PROFESSIONAL COMPUTER REV x.xx

01 WILL START FROM DRIVE A
```

When this is displayed, a BEEP will be emitted from the keyboard. This beep informs the operator that operator intervention is now possible. If there is no operator intervention, then after a five (5) second delay the following will be displayed and the system will now attempt to load from drive A.

```
WANG PROFESSIONAL COMPUTER REV x.xx

01 WILL START FROM DRIVE A

02 STARTING FROM DRIVE A
```

During the 5 second delay (after the beep is heard), the operator can perform one of five operator options. These are:

- Depress the "P" key
- Depress the "G" key
- Depress the "D" key
- Depress the "Q" key
- Depress the "M" key

Depressing the "P" key prompts the system to Re-IPL. If this key is depressed, the system will again run the power-up diagnostics and the start-up message will be displayed.

Depressing the "G" key prompts the system to proceed to load the software without waiting for the delay.

Depressing the "D" key prompts the system to re-direct the start to a different drive device. When this key is depressed the following is displayed:

```
:D
03 RE-DIRECT START
:_
```

Enter the new drive device nomenclature (B or W if previously started from Drive A).

To re-direct to Drive B, type in "B" and depress the "RETURN" key. The system will now attempt to load the system software from Drive B.

To re-direct to the Winchester, type in "W" and the decimal slot identification (ID) number the Winchester Controller board is located in (01-15), then depress the "RETURN" key (see example). The system will now attempt to load the system software from the Winchester.

Example: If the Winchester Controller PCB is located in slot 5, then enter:

W05 "RETURN"

Depressing the "Q" key executes a warm start. A warm start is the system Re-IPL without running power-up diagnostic. The warm start is futher discussed in paragraph 4.11.

Depressing the "M" key displays the following Diagnostic Menu:

1 - RECAL
2 - CYL 1
3 - CYL 16
4 - CYL 40
5 - RS232 LOOP
6 - RE-RUN BIT

The above menu is discussed in paragraph 4.13.3. To return to the start-up menu depress the number "6" key to rerun the power-up diagnostic.

If the message in Figure 4-40 is displayed, this means that the computer can not do anything until the System Software is loaded. Ensure the System Diskette is installed in Drive A. Then depress the "R" key. The system will now attempt a Re-try (Re-IPL).

```
WANG PROFESSIONAL COMPUTER REV x.xx

*** 40 NO AUTO-START DEVICE
:_
```

Figure 4-40. The Non-Start Display

The System Software diskette contains all of the files that are necessary to start the system including the operating system and System Menu programs. In order to start the system you must use the System Software diskette or a diskette that has the system files on it. If another diskette is used the system will display the following message on the Monitor:

```
WANG PROFESSIONAL COMPUTER REV x.xx

01 WILL START FROM DRIVE A

02 STARTING FROM DRIVE A

***41 START FAILED
   71 DRIVE A NO WANG START TRACK
   :_
```

If this situation occurs, remove the disk in Drive A (or the selected default drive) and insert the system diskette. Depress the letter "R" key to re-IPL the system.

NOTE

DRIVE A IS THE START-UP DEFAULT DRIVE. THE SYSTEM ASSUMES DRIVE A TO BE THE DEFAULT DRIVE UNLESS THE INSTRUCTIONS FOR THE DEFAULT DRIVE ARE ALTERED THROUGH THE SYSTEM UTILITIES MENU -- SET DEFAULT DRIVE.

The Time and Date screen below will appear automatically every time you start your system with the System Software diskette. If you want to set the date and time simply fill in the information, the correct format is automatically provided. Once the time and date is set, an organizational and historical record of the files on that particular diskette is recorded. Depressing the "HELP" key will give an explanation of how to set the time and date.

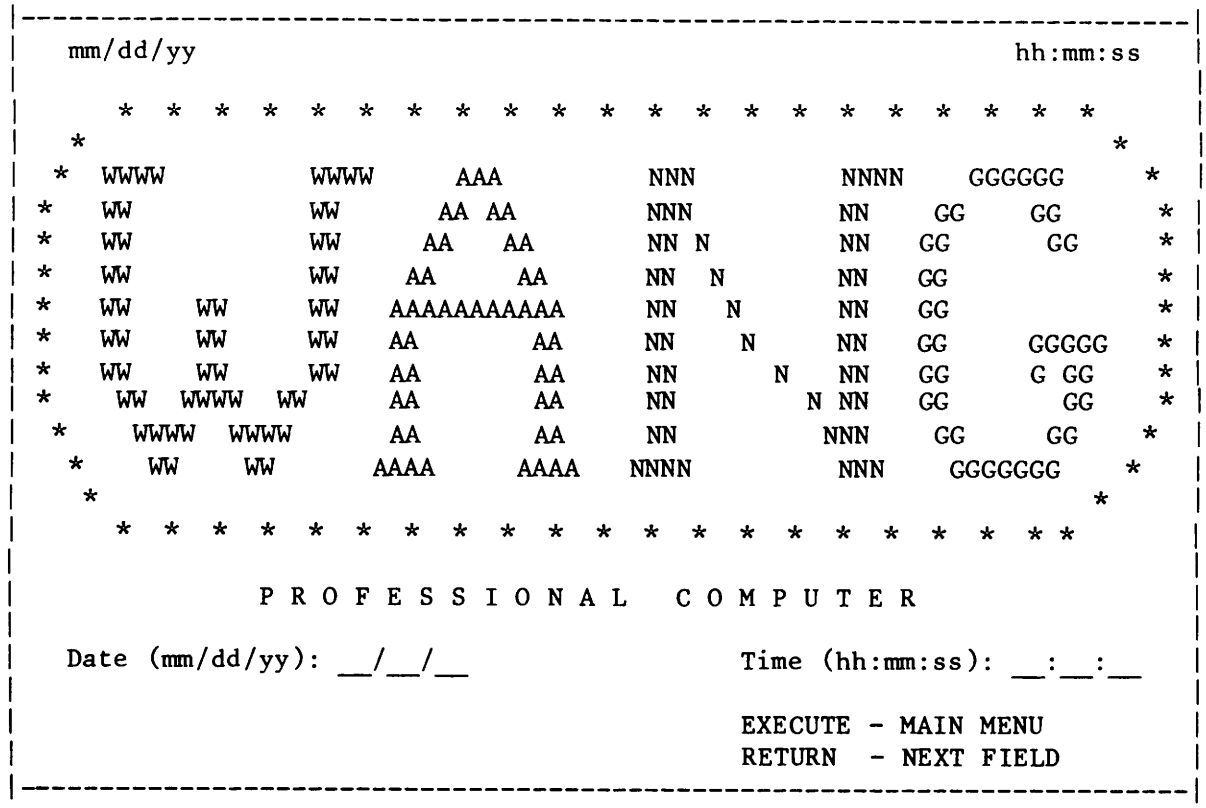


Figure 4-41. The Date and Time Screer

However, the time and date does not have to be set each time you start the system. If the time and date are not to be set, depress the "EXECUTE" key to proceed to the Main System Menu. This Menu is shown in Figure 4-42.

NOTE

FOR THE PURPOSE AND CLARITY OF THIS MANUAL, SOFTWARE RELEASE LEVELS ARE DENOTED x.x. THE ACTUAL RELEASE LEVEL DISPLAYED DENOTES THE LEVEL OF SOFTWARE BEING RUN. THE SYSTEM SCREEN LOADS DISPLAYED ARE SYSTEM SCREENS AS OF THIS WRITING, ACTUAL SCREEN LOADS MAY VARY PER CUSTOMER.

```
mm/dd/yy          Wang Professional Computer          hh:mm:ss
              M A I N   S Y S T E M   M E N U
                        Release x.x

Select an Item and Proceed

                  _ Applications
                  _ Conversion Aids
                  _ System Utilities
                  _ Program Development
                  _ Communications
                  _ DOS Command Processor
                  _ Other

                                SPACE BAR - Item Select
                                EXECUTE   - Proceed
```

Figure 4-42. The Main System Menu Display

By positioning the acceptance block to the option you want and depressing the "HELP" key, that menu will be described on the HELP screen. The various menus and screen loads are discussed in paragraph 4.12 Main Menu Options.

If you now remove the System Software diskette from Drive A you will notice that the Main System Menu remains on the screen. That happens because when the system started the menu program and others, was loaded from the diskette into memory. These programs will remain in the Systems memory until they are either deleted, the system is powered down, or the system is restarted.

4.11 SYSTEM RESTART (Warm Start)

The System can be restarted (Warm Started) by reinserting the System Software diskette in Drive A (if removed) and depressing the following keys:

Hold down the "2ND" key and depress the "COMMAND" key.
Release both keys, then depress the "CANCEL" key.

This results in the system running the IPL sequence without running the power-up diagnostics.

4.12 MAIN SYSTEM MENU OPTIONS

The following are the various menus that will be displayed when properly selected from the Main System Menu as shown in Figure 4-42. By positioning the acceptance block to the option you want and depressing the "EXECUTE" key, that menu will be appear on the screen.

4.12.1 Applications

Applications are programs used to achieve a specific practical objective. For example, the Multiplan program helps you answer specific business and financial questions, and the Wang PC Word Processing facilitates the writing, editing, and printing of text.

Selecting the Applications option on the Main System Menu, the following appears on the screen.

```
|-------------------------------------------------------------------|
|                                                                   |
|  mm/dd/yy          Wang Professional Computer          hh:mm:ss   |
|                A P P L I C A T I O N S  M E N U                   |
|                           Release x.x                             |
|                                                                   |
|  Select an Item and Proceed                                       |
|                                                                   |
|                             _ Multipan                            |
|                             _ Word Processing                     |
|                             _ Other                               |
|                                                                   |
|                                                                   |
|                                                                   |
|                                    SPACE BAR - Item Select        |
|                                    EXECUTE   - Proceed            |
|                                    CANCEL    - Previous Menu      |
|                                                                   |
|-------------------------------------------------------------------|
```

Figure 4-43. The Applications Menu

By positioning the acceptance block to the option you want (using the SPACE BAR) and depressing the "HELP" key, that option will be described on the HELP screen. To return to the previous menu depress the "CANCEL" key. For application of the various menu options refer to the Wang PC Introductory Guide 700-7590.

4.12.2 System Utilities

System Utilities are general-purpose programs that support other functions of the computer. As soon as you select the System Utilities option, the System Utilities menu appears on the screen.

```
|-----------------------------------------------------------------|
|                                                                 |
|  mm/dd/yy          Wang Professional Computer          hh:mm:ss |
|           S Y S T E M   U T I L I T I E S   M E N U             |
|                        Release x.x                              |
|                                                                 |
|  Select an Item and Proceed                                     |
|                                                                 |
|      _ Check Disk                  _ Path - Change Directory    |
|      _ Directory Display           _ Path - Make Directory      |
|      _ Disk Copy                   _ Path - Remove Directory    |
|      _ Disk Format                 _ Path - Select Alternates   |
|      _ File Compare                _ Set Date                   |
|      _ File Copy                   _ Set Default Drive          |
|      _ File Copy With Append       _ Set National Defaults      |
|      _ File Delete                 _ Set Time                   |
|      _ File Rename                 _ Write Verify               |
|      _ Modify System Menus         _ Other                      |
|                                                                 |
|                                    SPACE BAR - Item Select      |
|                                    EXECUTE   - Proceed          |
|                                    CANCEL    - Previous Menu    |
|                                                                 |
|-----------------------------------------------------------------|
```

Figure 4-44. System Utilities Menu

By positioning the acceptance block to the option you want (using the SPACE BAR) and depressing the "HELP" key, that option will be described on the HELP screen. To return to the previous menu depress the "CANCEL" key. For application of the various menu options refer to the Wang PC Introductory Guide 700-7590.

4.12.3 Program Development

The Program Development Menu contains programs that are useful for writing, correcting, modifying, and running programs. For example, the Program Development Menu contains an option named Basic. Selecting this option allows you to use the programming language known as interpretive BASIC.

Selecting the Program Development option on the Main System Menu, the following appears on the screen.

```
|-------------------------------------------------------------------|
|                                                                   |
|  mm/dd/yy          Wang Professional Computer          hh:mm:ss   |
|        P R O G R A M   D E V E L O P M E N T   M E N U            |
|                        Release x.x                                |
|                                                                   |
|  Select an Item and Proceed                                       |
|                                                                   |
|                          _ Basic                                  |
|                          _ Debugger                               |
|                          _ Editor                                 |
|                          _ Linker                                 |
|                          _ Library Manager                        |
|                          _ Other                                  |
|                                                                   |
|                                                                   |
|                                  SPACE BAR - Item Select          |
|                                  EXECUTE   - Proceed              |
|                                  CANCEL    - Previous Menu        |
|-------------------------------------------------------------------|
```

Figure 4-45. Program Development Menu

By positioning the acceptance block to the option you want (using the SPACE BAR) and depressing the "HELP" key, that option will be described on the HELP screen. To return to the previous menu depress the "CANCEL" key. For application of the various menu options refer to the Wang PC Introductory Guide 700-7590.

4.12.4 Communications

The options on the Communications Menu allow the Wang PC to serve as a workstation on the Wang 2200, VS, OIS, or Alliance systems or to communicate with a host computer. As a workstation on any of the multi-user Wang systems the PC has access to the software, data, and resources of that system.

Communicating with host computers allow access to timesharing systems to speedily collect, transfer, and analyze data. When the Communications option is selected from the Main System Menu, the Communications Menu appears on the screen as shown in Figure 4-46.

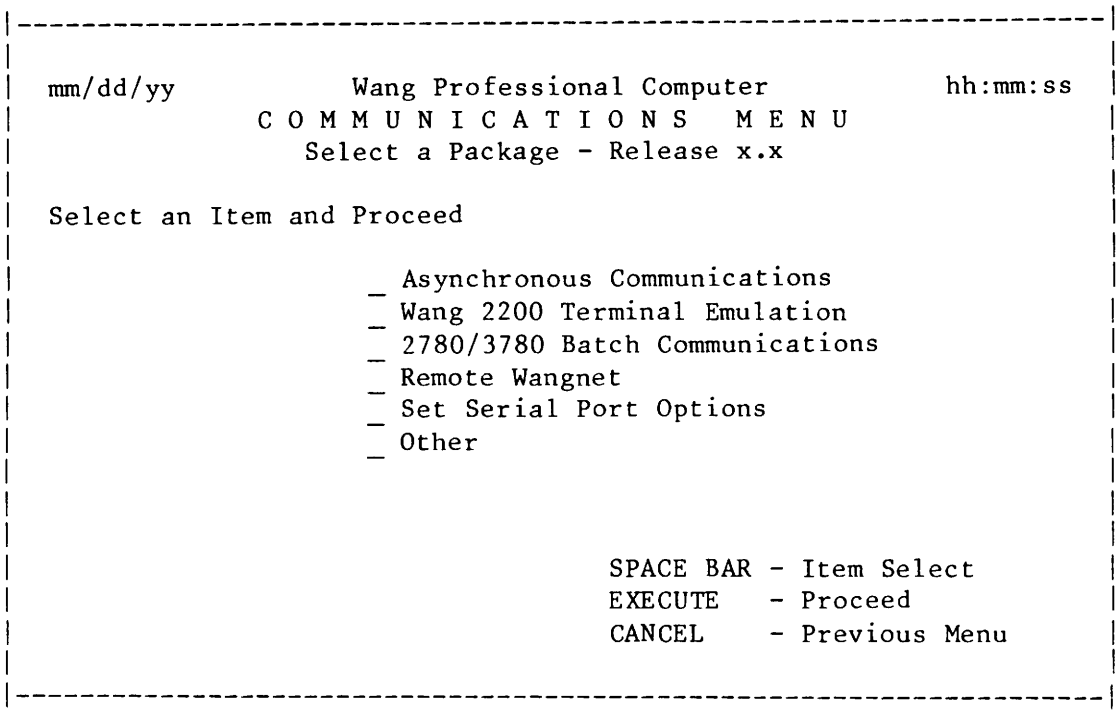


Figure 4-46. Communications Menu

By positioning the acceptance block to the option you want (using the SPACE BAR) and depressing the "HELP" key, that option will be described on the HELP screen. To return to the previous menu depress the "CANCEL" key. For application of the various menu options refer to the Wang PC Introductory Guide 700-7590.

4.12.5 DOS Command Processor

The DOS Command Processor option offers a way to give instructions to the PC without using menus. By depressing the "HELP" key, the HELP screen will be displayed giving a description of the DOS Command Processor. When this option is selected from the Main System Menu, the following prompt (DOS prompt) appears on the screen:

```
A:_
```

The response to this prompt is by typing in a file specification beginning at the cursor position. The letter A denotes the default drive. If the default drive has been changed from Drive A, that drive designation (letter B or C) will appear. Refer to the Wang PC Introductory Guide 700-7590 for a detailed description of the DOS Command Processor.

4.12.6 Other

The option designated "Other" allows the user to execute programs without using menus. When "Other" is selected from the Main System Menu the following is displayed:

File Spec: _____

Depressing the HELP key, this option will be described on the HELP screen. Refer to the Wang PC Introductory Guide 700-7590 for a detailed description of this menu option.

4.12.7 Conversion Aids

Conversion aids are programs used to convert Wang Word Processing documents to files that can be used by other programs and to convert files used by other programs to Wang Word Processing documents. Figure 4-47 shows the Conversion Aids Menu. This menu is used with Wang Word Processing, if word processing is not on the system this menu should not be used.

```
|-------------------------------------------------------------------|
|                                                                   |
|  mm/dd/yy          Wang Professional Computer          hh:mm:ss   |
|            C O N V E R S I O N   A I D S   M E N U                |
|                        Release x.x                                |
|                                                                   |
|  Select an Item and Proceed                                       |
|                                                                   |
|                            _ Convert Document to Text             |
|                            _ Convert Text to Document             |
|                            _ Other                                |
|                                                                   |
|                                                                   |
|                                                                   |
|                                  SPACE BAR - Item Select          |
|                                  EXECUTE   - Proceed              |
|                                  CANCEL    - Previous Menu        |
|                                                                   |
|-------------------------------------------------------------------|
```

Figure 4-47. Conversion Aids Menu

4.13 POWER-UP DIAGNOSTIC

The Built-in-Test (B.I.T.) EPROMS located at L78 and L97 on the 8221 CPU/System board are used to verify system integrity on Power-Up. Also resident in the EPROM is the Initial Program Load (IPL) code for Bootstrap of the operating system.

The main purpose of the B.I.T. diagnostics is to verify that enough circuitry is functional to attempt the successful loading of the system software. Upon completion of the diagnostics, control is turned over to the IPL code to automatically begin loading of the system software.

It must be noted that the B.I.T. diagnostics DO NOT test the disk drives for write or read operations. The IPL portion of the EPROM assumes the disk drives work correctly. If there is a disk problem at this time, the Bootstrap will report any errors via the output console device.

Also contained in the B.I.T. diagnostics are routines for Floppy Disk Alignment, RS232 Loopback tests, and provisions for keyboard loopback testing and the re-execution of the diagnostics.

4.13.1 Operation

The B.I.T. diagnostics automatically begin to operate upon Power-On of the CPU. As soon as power is applied, the LED located on the rear of the CPU board (shown in Figure 4-12) illuminates and then extinguishes within three (3) seconds. If this fails to occur, suspect the Power Supply or the CPU board to be defective.

Approximately 1/2 second after the CPU LED is turned off, all serial Keyboard LEDs are turned on. If they fail to illuminate, suspect the CPU board or the Keyboard to be defective.

These LEDs will extinguish one-by-one as the diagnostic tests are being run. All LEDs will extinguish within a maximum 30 seconds (dependant upon the number of options installed) after power is applied.

When all LEDs have extinguished, the diagnostics have completed and control is turned over to the Bootstrap to begin the IPL sequence.

If any of the Keyboard LEDs or the CPU LED remain illuminated after 30 seconds or so, then a FATAL ERROR has occurred. Execution will cease (hang) and the system will not IPL. **NOTE: FATAL ERROR LEDS PATTERNS ARE PRESENTLY NOT DEFINED.**

4.13.2 Error Reporting

Errors are reported in two forms; FATAL and NON-FATAL. FATAL errors are reported via the Keyboard and CPU board LEDs. NON-FATAL errors are reported via the output console device (s) if detected, or the RS232 port device or the Parallel port device.

4.13.2.1 FATAL ERRORS

Errors which will inhibit the PC from loading the operating system are considered to be FATAL. FATAL errors are displayed via the six LEDs located on the Low Profile Keyboard (see Figure 4-24 for LED locations) and the LED located on the rear of the 8221 CPU board.

FATAL errors cause the B.I.T. diagnostics to suspend operation (hang) and report to the Keyboard/CPU LEDs. Control never gets passed to the Bootstrap; therefore, the Floppy Based Diagnostics (or any disk) can not be run.

Most FATAL errors are caused by a defective CPU board or Power Supply. However, its possible that a defective option board could affect the System Bus causing a FATAL error to occur.

When a FATAL error does occur, all voltages should be checked first. Remove all option boards and re-run the power-on diagnostics. (Refer to Chapter 5 paragraph 5.5 for Removal and Replacement procedures.) If the diagnostics now pass, install the option boards one at a time until the failure re-occurs. The last card installed is probably the defective one.

If a FATAL error still occurs after all option boards have been removed, then the CPU board is probably defective. This assumes all Power Supply voltages are correct. The Motherboard could also be at fault.

4.13.2.2 NON-FATAL ERRORS

Errors which will not inhibit the PC from loading the operating system are considered to be NON-FATAL. In the event of a NON-FATAL error, the Bootstrap portion of the EPROM will be responsible for displaying messages to the user via the current output console device (s). This will be accomplished after the Built-In-Tests have completed and before the Bootstrap is attempted. NON-FATAL error messages are listed in Appendix B of this manual.

In the event of a NON-FATAL error, the Floppy Based Diagnostic should be run to further diagnose the problem.

4.13.3 B.I.T. Options

Two options are available during the B.I.T. operation. The first option allows the user to access the Diagnostic Menu via a keystroke entry. (Refer to paragraph 4.10.) The second option is loop on B.I.T., available via the Baud Rate Switch located on the 8221 CPU board. (Refer to paragraph 4.7.1 for switch setting.)

1. The Diagnostic Menu will appear as follows:

```
1 - RECAL
2 - CYL 1
3 - CYL 16
4 - CYL 40
5 - RS232 LOOP
6 - RE-RUN BIT
```

Simply type in the number to select the desired function.

Selections 1 through 4 are routines for alignment of Floppy Disk Drive A. To align Drive B, swap the floppy drive cables.

Selection 5 requires an external loopback connector (WLI P/N 420-1040) to be installed on the RS232 port located on the rear of the 8221 CPU board. See Figure 4-12 for RS232 port location. The Baud rate for the test is taken from the SW1 switch setting located on the 8221 CPU board. See Figure 4-14 for SW1 location.

Selection 6 will re-execute the entire B.I.T power-up sequence.

2. Loop on B.I.T.

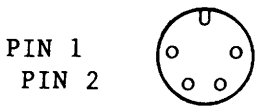
This option allows the user to loop on the power-up diagnostic. The option is selected by setting SW1 located on the 8221 CPU board to the all ON (O or CLOSED) state. No loop count will be kept and control will be passed to the IPL code only to display any NON-FATAL errors found. Control is then returned to the beginning of the B.I.T. This loop will continue until SW1 switch setting is changed.

4.13.4 Keyboard Loopback

If the NON-FATAL keyboard error message "MISSING OR DEFECTIVE" appears on the screen during the B.I.T. sequence, then perform the following procedure to determine the failing unit.

1) Power down the system and remove the keyboard cable from the CPU connector J3.

2) Jumper pins 2 and 3 of connector J3 together. Simply use a piece of wire or a paper clip. See connector J3 detailed view.



Pin 1 = ± 0v (Logic Ground)
Pin 2 = Serial Data into Keyboard
Pin 3 = Serial Data out from Keyboard
Pin 4 = Regulated +5v

3) Power-Up the system to re-run the B.I.T..

4) If the B.I.T. passes without error, the Keyboard is probably defective. If the B.I.T. still fails, the CPU board is probably defective.

4.13.5 Floppy-Based Diagnostic

NOTE

THE FLOPPY-BASED DIAGNOSTIC WILL NOT RUN IF IT IS WRITE-PROTECTED. ENSURE THE WRITE TAB IS REMOVED (OFF).

The CE Floppy-Based Diagnostic software package (P/N 195-2459-9) contains the diagnostic diskette (WLI P/N 732-0022) and documentation to be used by Customer Engineering and Manufacturing.

The diagnostic software incorporates multiple levels of diagnostic capability and error reporting depending on the user. It also assumes that a portion of the system already functions correctly due to the fact the system did not report a FATAL error condition from the B.I.T.

The initial release of the diagnostic diskette uses the MS DOS Operating System to load the diagnostics. Once loaded, the system will request the date and time to be entered. After accepting the date and time, the system will then display the DOS Command Processor prompt:

A:_

When this appears, type in the program name "DIAGNOSE" followed by depressing the "RETURN" key. The system will now load the diagnostic programs. Once loaded, the system will display the Diagnostic Disclaimer screen. Depending on what is typed at this time, the user will either access the Customer level or the CE/Manufacturing level of operation.

Typing in YES will allow the user to enter the Customer level.
Holding down the "2ND" key while typing in "D" and then "M" will allow the user to enter the CE/Manufacturing level of operation.

Refer to the diagnostic documentation included with the diskette for further operating instructions and diagnostic interpretations.

The second and future releases of the diagnostics will be standalone versions and will not include the MS DOS operating system. Once loaded, the first screen displayed will be the disclosure screen. Operating from this point will be the same as discussed above.

CHAPTER 5
PREVENTIVE AND CORRECTIVE MAINTENANCE

5.0 PREVENTIVE MAINTENANCE

No scheduled preventive maintenance is required for the Professional Computer.

5.1 CORRECTIVE MAINTENANCE

The Corrective Maintenance section provides information pertaining to the electrical and mechanical adjustments of the PC.

5.1.1 Special Tools

No special tools are required to perform corrective maintenance on the Wang Professional Computer. All maintenance performed can be accomplished with the Wang Standard Tool Kit WLI P/N 726-9401. Special tools that are listed in paragraph 5.3.2 are recommended though not required.

5.2 ELECTRICAL ADJUSTMENTS

The SPS-200 Power Supply is a switching power supply which is a completely enclosed unit. No field adjustments will be made on the power supply assembly, it is FIELD REPLACEABLE ONLY. CAUTION should be taken because the Power Supply Unit contains EXTREMELY DANGEROUS VOLTAGE AND CURRENT LEVELS.

5.2.1 Electrical Measurements and Checks

There are four voltage levels that can be checked. These are:

+5 Vdc $\pm$ 5%
-5 Vdc $\pm$ 0.2 volts
+12 Vdc $\pm$ 5%
-12 Vdc $\pm$ 0.4 volts

These voltages must be checked from inside the System Unit. With the Electronic Unit in the horizontal position with the air vents pointing down, remove the four Phillips-Head screws located on the four corners of the unit's rear panel. Grasp the vertical angle bracket located on the rear of the unit with one hand and hold the cover with the other hand and carefully pull the unit straight out of the cover. Set the cover to one side.

Locate the motherboard located near the Switching Power supply. Using a digital voltmeter measure the following voltages. See Figure 5-1 for power distribution and connector locations.

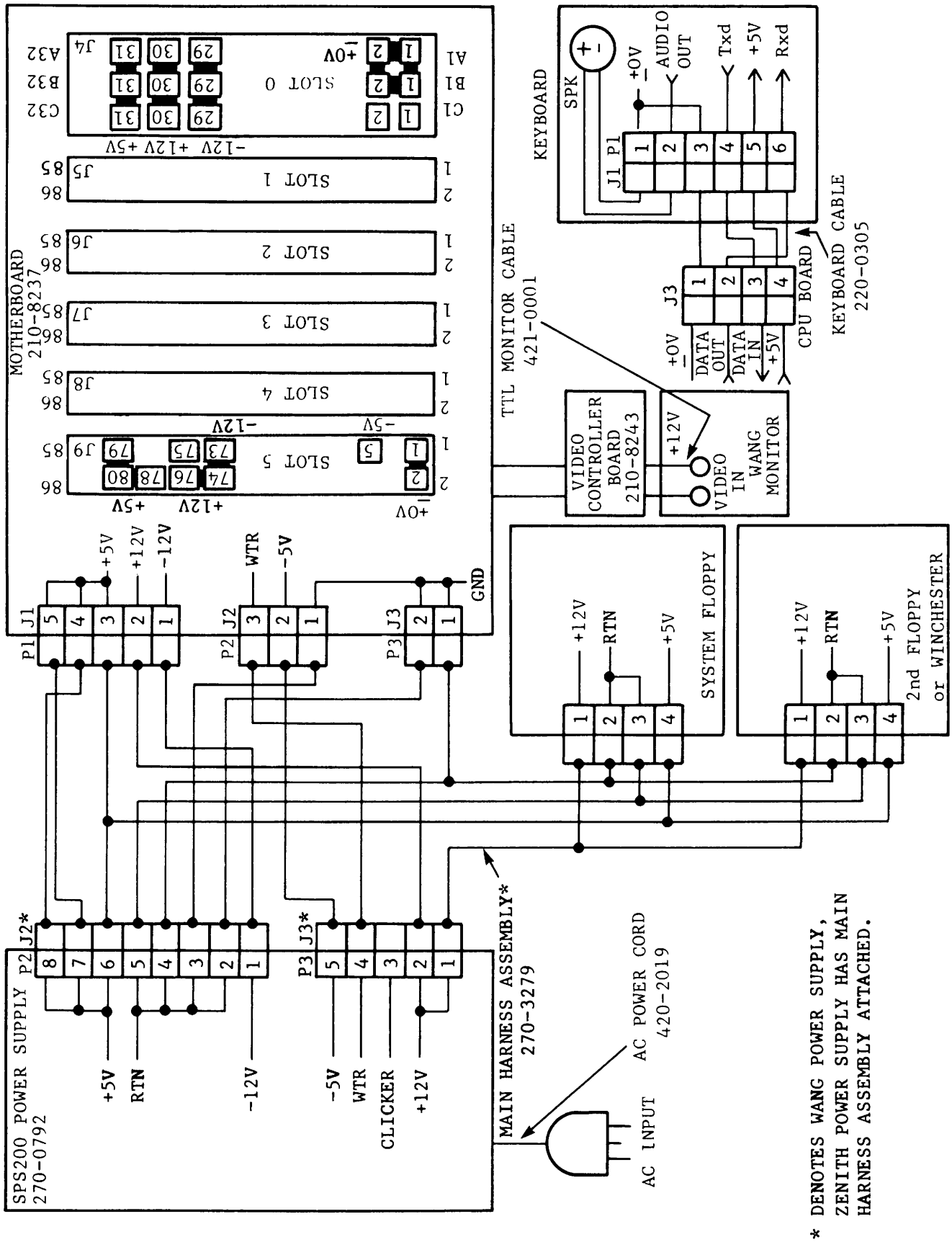


Figure 5-1. Power Distribution and Interconnection Diagram

Voltmeter setting:

20 Volt Scale dc

a. +12 Volt

( ) Place the Red lead (positive) on the Motherboard connector P1 pin 2. Place the black lead (negative) on the Motherboard connector P3 pin 1. Read the voltage level displayed, it should be +12 Volts ± .6V.

b. +5 Volt

( ) Place the red lead (positive) on the Motherboard connector P1 pin 3. Place the black lead (negative) on the Motherboard connector P3 pin 1. Read the voltage level displayed, it should be +5 volts ± .25.

c. -12 Volt

( ) Place the Red lead (positive) on the Motherboard Connector P1 pin 1. Place the black lead (negative) on the Motherboard connector P3 pin 1. Read the voltage level displayed, it should be -12 Volts ± .4V.

d. -5 Volt

( ) Place the Red lead (positive) on the Motherboard Connector P2 pin 2. Place the black lead (negative) on the Motherboard connector P3 pin 1. Read the voltage level displayed, it should be -5 Volts ± .25V.

If any voltage is incorrect or missing, replacement of the Switching Power Supply is required. Refer to the Removal and Replacement procedure as described in paragraph 5.5.1.1.

If all voltages levels are correct, then reassemble the unit. Before reassembly, ensure the electronics unit cover is positioned with the air vents pointing downward. Now, slide the unit into the cover being careful not to pinch any cable assemblies. Install the four Phillips-Head screws removed from the four corners of the unit's rear panel. Check all cables attached (the ac power cable, the keyboard cable, the monitor cable etc.) to the unit's rear panel for proper connections.

5.3 MECHANICAL ADJUSTMENTS

The Mechanical Adjustment procedures discussed below will enable the AFET to properly align the PC Floppy Disk Drive (s) and to verify that the Floppy drive is operating properly. The following outlined adjustment procedures are for adjusting drive A, to adjust drive B reverse the floppy drive cables at the System board connectors J5 and J6. The floppy disk drive (s) in the system may be either Tandon TM-100 or MPI Model 52. Tandon disk drive adjustments are contained in section 5.3.1 and MPI disk drive adjustments are contained in section 5.3.2.

5.3.1 TANDON FLOPPY DISK DRIVE ADJUSTMENTS

Equipment Required:

Wang Standard Tool Kit WLI P/N 726-9401
Digital Multimeter
Dual Channel Oscilloscope (Tektronix Model 465 or equivalent)
Wang Alignment Diskette WLI P/N 726-8068

5.3.1.1 FLOPPY DISK VOLTAGE CHECK

( ) Remove the System Unit cover as described in paragraph 5.5.1 steps 1-3 and place the System Unit in the vertical position (power supply down).

( ) Reconnect the ac power cord, the keyboard cable, and the monitor cable to the system unit and Power-On the unit. Using the multimeter, measure the Floppy Drive voltage levels at the Motherboard connector P1 as follows: See Figure 5-1 for P1 location.

P1 Pin 2 +12 Volts ± 5% (11.4 Vdc to 12.6 Vdc)
P1 Pin 3 +5 Volts ± 5% (4.74 Vdc to 5.25 Vdc)

5.3.1.2 TANDON DRIVE MOTOR SPEED ADJUSTMENT

1) Power-Off the System Unit. Remove the front plate screw holding the System floppy drive in place and slide the drive straight out as far as its cables will allow, being careful not to apply excessive tension to the cables.

2) Insert the Special Alignment Diskette (P/N 726-8068) into Drive A.

3) With the System Unit in the vertical position (power supply down) and the drive slide out, Power-On the unit and wait for the B.I.T. to be completed. When completed, the following will be displayed on the Monitor screen:

WANG PROFESSIONAL COMPUTER REV x.xx

01 STARTING FROM DRIVE A

4) Now within five (5) seconds depress the "M" key. The following menu will be displayed on the screen.

1 RECAL
2 CYL 1
3 CYL 16
4 CYL 40
5 RS232 LOOP
6 RE-RUN BIT

5) With this menu displayed, the floppy motor spins continuously thereby allowing for easier motor speed check and adjustment. This menu will also be used for the Radial-Track alignment, End-Stop adjustment, and the Index-To-Data alignment.

6) View the spindle pulley through the slot in the bottom cover plate. With flourescent light shining through the slot, observe the strobe effect of the timing marks on the spindle pulley. If operating from 60 Hz power observe the outer trace, if operating from 50 Hz power observe the inner trace (see Figure 5-2). Note that Figure 5-2 is the bottom view of the TM-100 Drive with the bottom plate removed.

7) The timing marks should appear stationary when the drive motor is running at the correct speed. If the Floppy Drive motor speed is out of adjustment perform the following:

8) Using an insulated screwdriver, slowly turn R4 (located on the servo board at the rear of the floppy, see Figure 5-2) while viewing the timing marks. The timing marks will turn as you turn R4. Adjust R4 till the timing marks appear to be stationary.

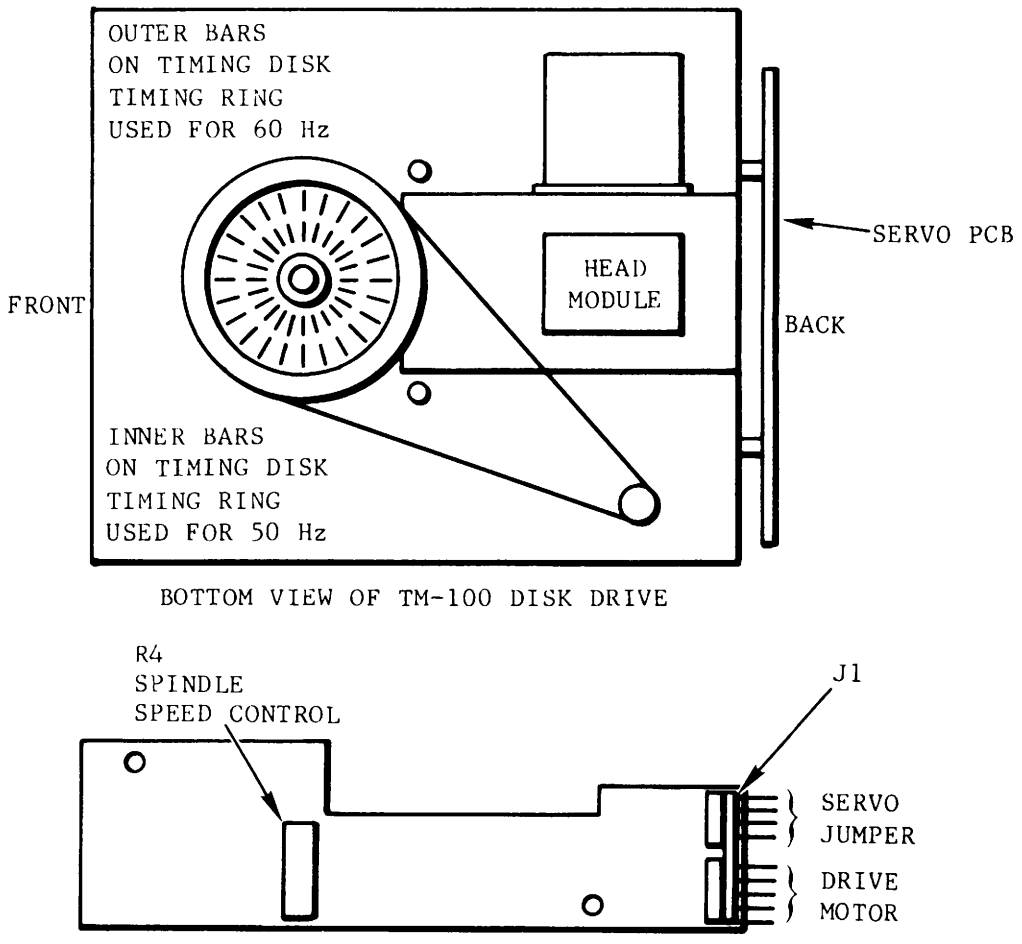


Figure 5-2. Location of R4 Speed Control Pot

5.3.1.3 TANDON DRIVE RADIAL-TRACK ALIGNMENT

The radial track alignment procedure aligns head positioning. The alignment check/adjustment ensures that track 16 position calculated by the head positioning logic coincides with track 16 position on the alignment diskette.

1) Set up the Oscilloscope as follows:

Scope channel A: TP1 on drive PCB
Scope channel B: TP2 on drive PCB
Ground scope probes to TP10 on drive PCB
Time Base: 20 Milliseconds per division
Amplitude: 50 Millivolt per division
Coupling: ac
External Trigger: TP7 with probe ground to TP6
Read Differentially: A plus B, B inverted

See Figure 5-3 for Test Point (TP) locations.

****
* CAUTION *
*
* CAUTION SHOULD BE TAKEN WHEN CONNECTING THE SCOPE *
* PROBES NOT TO SHORT OUT CONNECTOR P7. *
*
****

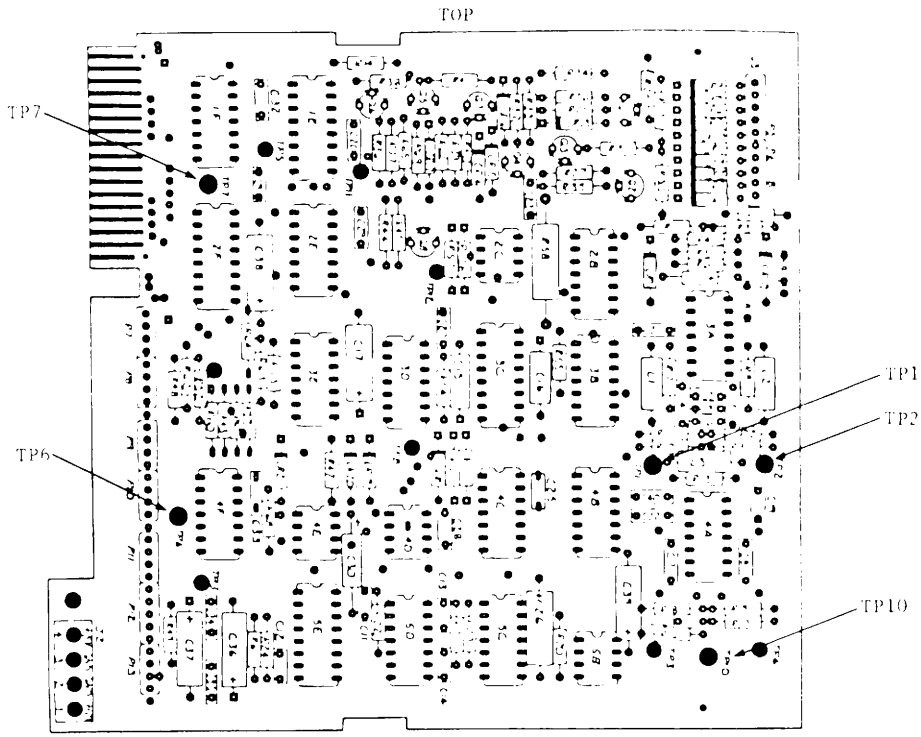


Figure 5-3. Tandon Floppy Drive PCB Test Point Locations

2) With the Diagnostic menu displayed as discussed in paragraph 5.3.2.2 steps 3 and 4, complete the following.

3) With the System Unit in the vertical position (power supply down) and the drive slide out as far as its cables will allow, loosen the two module retaining screws (See Figure 5-4) accessible through the two holes in the Drives bottom plate 1/2 turn counterclockwise.

4) Loosen the top module retaining screw (See Figure 5-4) one-half (1/2) turn counter-clockwise.

5) Depress the number "1" key on the keyboard to step the head to track 0.

7) Depress the number "3" key to drive the head to track 16 and adjust the Scope to display the "CAT EYE" pattern (Figure 5-5).

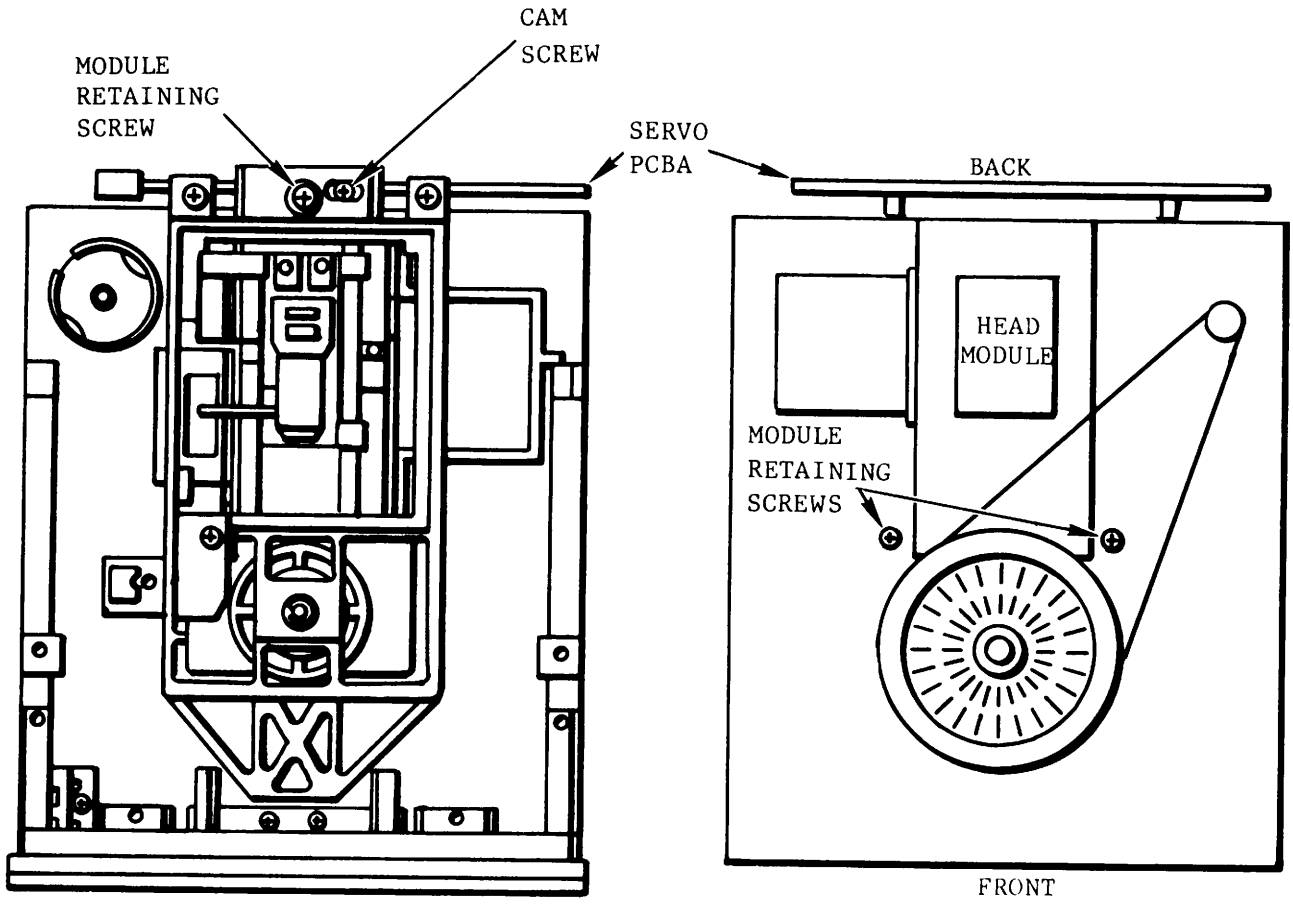
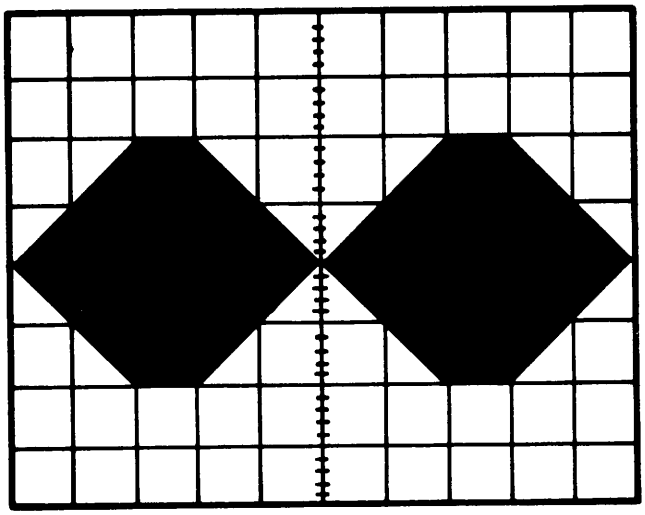


Figure 5-4. Head Module Retaining Screw Locations



EQUAL AMPLITUDE
(ON TRACK 16)

TIME SCALE = 20 ms/Div

Figure 5-5. Cats Eye Pattern

8) Verify that both CAT EYES are within 80% amplitude of each other and record the exact amplitude of each EYE.

9) Now drive the heads to track 0 by depressing the number "1" key, then drive the heads back to track 16 by depressing the number "3" key and repeat step 8.

10) Drive the heads to track 40 by depressing the number "4" key, then back to track 16 by depressing the number "3" key and repeat step 8.

11) With the heads at track 16, turn the adjusting cam screw clockwise with a flat blade screwdriver while watching the CATS EYE pattern on the oscilloscope. If you mis-adjust the radial-track alignment, one of the CATS EYES will decrease in amplitude while the other increases in amplitude.

12) Adjust the cam screw until the CATS EYE are equal in amplitude. Then readjust slightly so the eyes are equal in amplitude to the recorded values for track 16 for both heads.

13) Tighten the three module retaining screws and repeat the radial-track alignment steps 8 through 10 as described above. If any of the tracks/heads do not agree with the original readings, readjustment of the cam is required.

14) If you are unable to meet the tolerance called out in step 8, the Tandon Floppy Drive must be replaced. Refer to paragraph 5.5.1.2.

5.3.1.4 TANDON TRACK 00 END-STOP ADJUSTMENT

NOTE

THIS ADJUSTMENT MUST BE CHECKED FOLLOWING A RADIAL-TRACK ALIGNMENT.

Set up the Oscilloscope as follows:

Scope channel A: TP1
Scope channel B: TP2
Ground scope probes to TP10
Time Base: 20 Millisecond per division
Amplitude: 50 Millivolt per division
Coupling: ac
External Trigger: TP7 with probe ground to TP6
Read Differentially: A plus B, B inverted

1) Select track 00 by depressing the number "1" key on the keyboard.

2) Turn the track 00 stop screw (Figure 5-6) two turns counterclockwise using an .050" Allen wrench.

3) Now turn the stop screw clockwise until the scope signal starts to decease in amplitude.

4) Now turn the stop screw counterclockwise until the amplitude stops increasing, then continue an additional 1/8 turn counterclockwise.

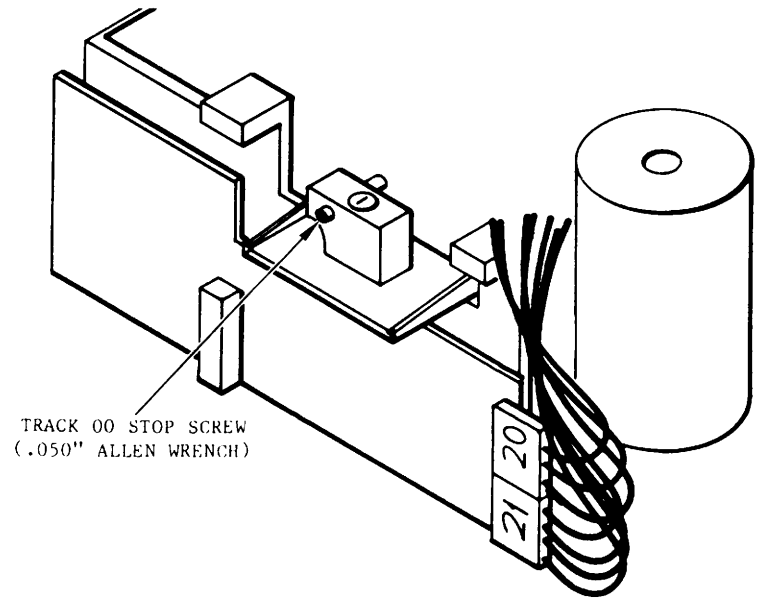


Figure 5-6. Track 00 End-Stop Screw Location

5.3.1.5 TANDON INDEX-TO-DATA ALIGNMENT

The Index-To-Data alignment pertains to an interval between the sensing of the Track-Index and the actual transmission of data. A standardized Index-To-Data interval is required to allow the interchangeability of diskettes.

Set up the Oscilloscope as follows:

Scope channel A: TP1
Scope channel B: TP2
Ground scope probes to TP10
Time Base: 50 Mircosecond per division
Amplitude: 50 Millivolt per division
Coupling: ac
External Trigger: TP7 with probe ground to TP6
Trigger: Positive Slope
Read Differentially: A plus B, B inverted

1) With the system Power-On and the alignment diskette inserted in the drive, select track 1 by depressing the "2" key. The data pattern on the oscilloscope should start 200 ±100 microseconds from the start of the sweep.

2) Loosen the Index-To-Data sensor retaining screw (See Figure 5-7) through the slot in the bottom cover 1/4 turn counterclockwise using a Phillps screwdriver.

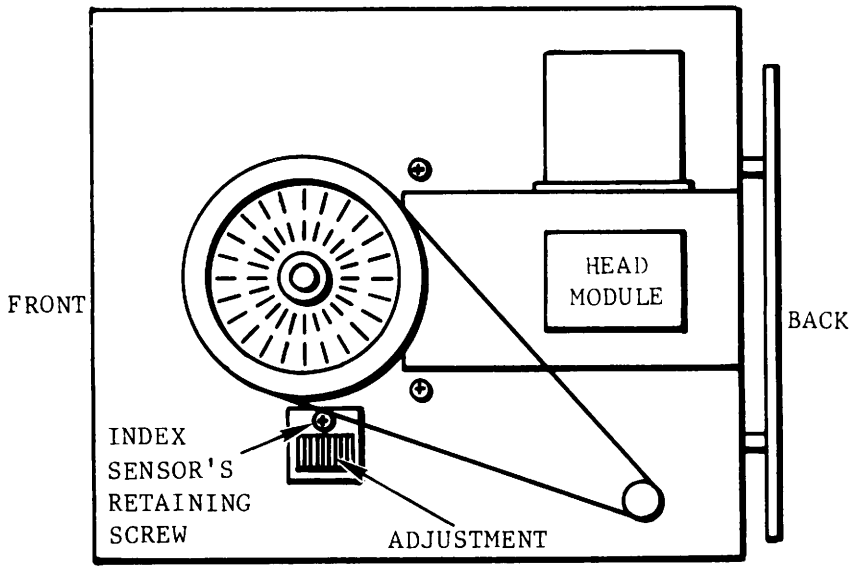


Figure 5-7. Index Sensor Retaining Screw and Adjustment

3) Slide the sensor back and forth while watching the oscilloscope pattern. The Start-of-Trace-to-data gap should increase as the sensor is moved in one direction, and decrease as the sensor is moved in the opposite direction.

4) Adjust the senor for a Start-of-Trace-to-Data gap of 200 microseconds ±100 microseconds. See Figure 5-8. Tighten the sensor retaining screw and recheck the data pattern for proper tolerance.

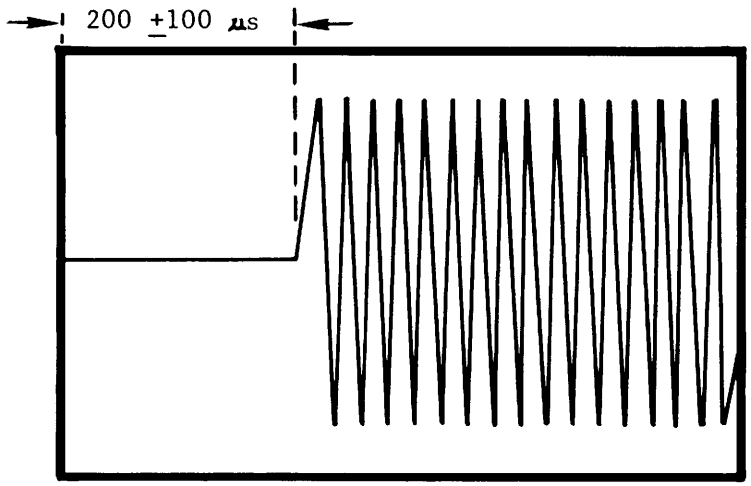


Figure 5-8. Index-To-Data Alignment Pattern

5.3.1.6 TANDON NEOPRENE DRIVE BELT

The neoprene drive belt tension is not critical and does not need to be adjusted.

5.3.1.7 TANDON WRITE-PROTECT SWITCH

Set up the Oscilloscope as follows:

Scope channel A: TP9
Ground scope probe to TP6
Time Base: 50 Millisecond per division
Amplitude: 2 Volts per division
Trigger: Internal, automatic

1) Insert a non-write protected diskette (tab removed) halfway into the drive.

2) Ensure that the switch is actuated. TP9 should be at logic 1 (+5V).

3) Insert minidiskette fully against the diskette back stop and close front latch. Ensure that switch is deactivated. TP9 should go to logic 0 (0V).

4) To adjust the switch loosen the retaining screw, and remove the switch assembly. Set the switch either higher or lower as required.

5.3.2 MPI DISK DRIVE ADJUSTMENTS AND MEASUREMENTS

Equipment Required:

Wang Standard Tool Kit WLI P/N 726-9401
Dual Channel Oscilloscope (Tektronix Model 465 or equivalent)
Digital Multimeter
CE alignment diskette (P/N 726-8068)
0.050 hex torque screwdriver set to 32 inch-ounces
#0, #1 Phillips head screwdrivers
#0 Phillips head torque screwdriver set to 20 inch-ounces

5.3.2.1 MPI DISK DRIVE VOLTAGE CHECK

1) Remove the System Unit cover as described in paragraph 5.5.1 and place the System Unit in the vertical position (power supply down).

2) Reconnect the ac power cord, the keyboard cable, and the monitor cable to the system unit and Power-On the unit. Using the multimeter, measure the Floppy Drive voltage levels at the Motherboard connector P1 as follows: See Figure 5-1 for P1 location.

P1 Pin 2 +12 Volts $\pm$ 5% (11.4 Vdc to 12.6 Vdc)
P1 Pin 3 +5 Volts $\pm$ 5% (4.74 Vdc to 5.25 Vdc)

5.3.2.2 MPI DRIVE MOTOR SPEED ADJUSTMENT

1) Power-Off the System Unit. Remove the front plate screw holding the right-hand floppy drive in place and slide the drive straight out as far as its cables will allow, being careful not to apply excessive tension to the cables.

2) Insert the Special Alignment Diskette (P/N 726-8068) into Drive A.

3) With the System Unit in the vertical position (power supply down) and the drive slid out, Power On the unit and wait for the B.I.T. to be completed. When completed, the following will be displayed on the Monitor screen:

WANG PROFESSIONAL COMPUTER REV x.xx

01 STARTING FROM DRIVE A

4) Now within five (5) seconds depress the "M" key. The following menu will be displayed on the screen. With this menu displayed, the floppy drive motor spins continuously thereby allowing for easier motor speed check and adjustment. This menu will also be used for the Radial-Track alignment, End-Stop adjustment, and the Index-To-Data alignment.

1 RECAL
2 CYL 1
3 CYL 16
4 CYL 40
5 RS232 LOOP
6 RE-RUN BIT

5) View the spindle pulley through the slot in the bottom cover plate. With flourescent light shining through the slot, observe the strobe effect of the timing marks on the spindle pulley. If operating from 60 Hz power observe the outer trace, if operating from 50 Hz power observe the inner trace (see Figure 5-10).

6) The timing marks should appear stationary when the drive motor is running at the correct speed. If the Floppy Drive motor speed is out of adjustment perform the following:

7) Using a straight slotted screwdriver, slowly turn R38 (see Figure 5-9 for location) while viewing the timing marks. The timing marks will turn as you turn R38. Adjust R38 until the timing marks appear to be stationary.

5.3.2.3 MPI RADIAL-TRACK ALIGNMENT

The radial track alignment procedure aligns head positioning. The alignment check/adjustment ensures that track 16 position calculated by the head positioning logic coincides with track 16 position on the alignment diskette.

1) Set up the Oscilloscope as follows:

Scope channel A: TP1 on drive PCB
Scope channel B: TP2 on drive PCB
Ground scope probes to ground leads of capacitors C30/C31
Time Base: 20 Millisecond per division
Amplitude: 50 Millivolt per division
Coupling: ac
External Trigger: TP6 with probe ground to C30/C31
Trigger Mode: Normal
Read Differentially: A plus B, B inverted

See Figure 5-9 for Test Point (TP) locations.

2) With the Diagnostic menu displayed as discussed in paragraph 5.3.2.2 steps 3 and 4, complete the following.

3) Depress the number "1" key on the keyboard to step the head to track 0.

4) Depress the number "3" key to drive the head to track 16 and adjust the Scope to display the "CAT EYE" pattern (Figure 5-5).

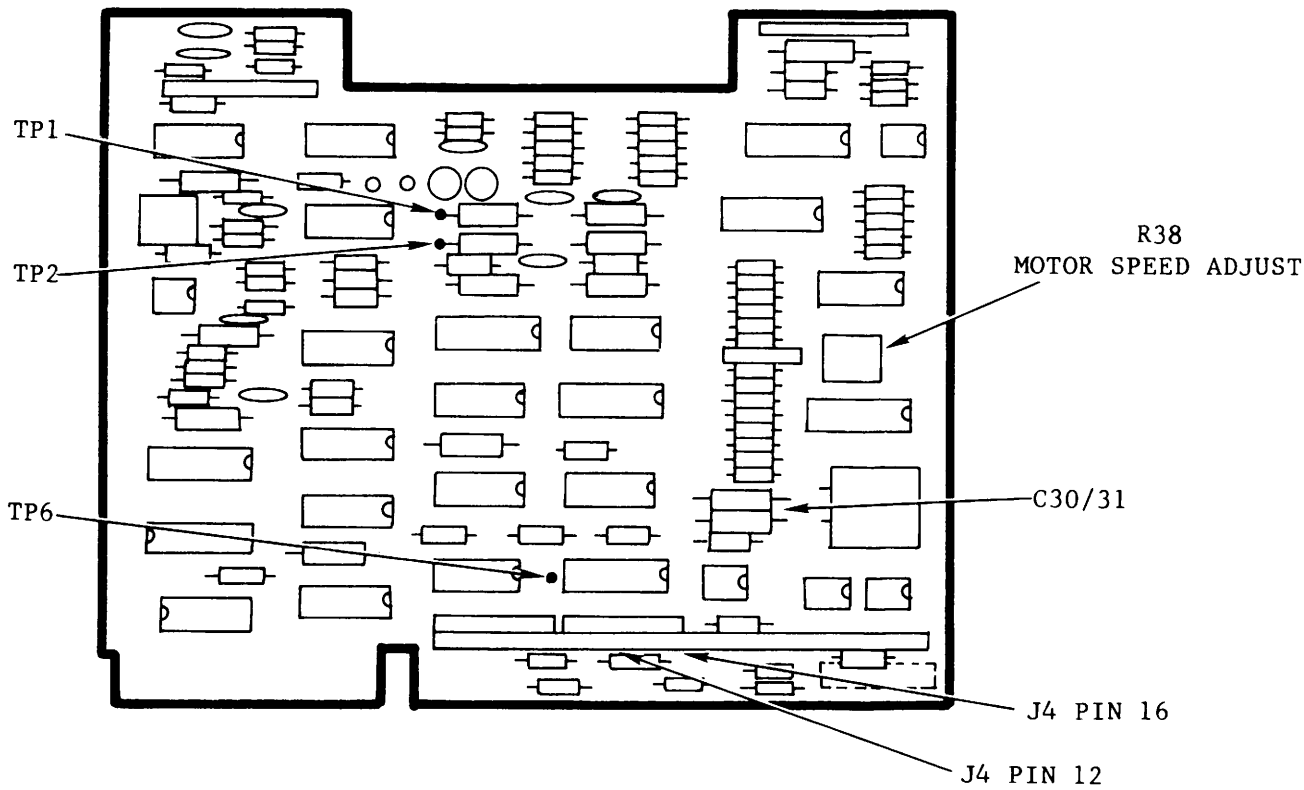


Figure 5-9. MPI PCB Test Point Locations

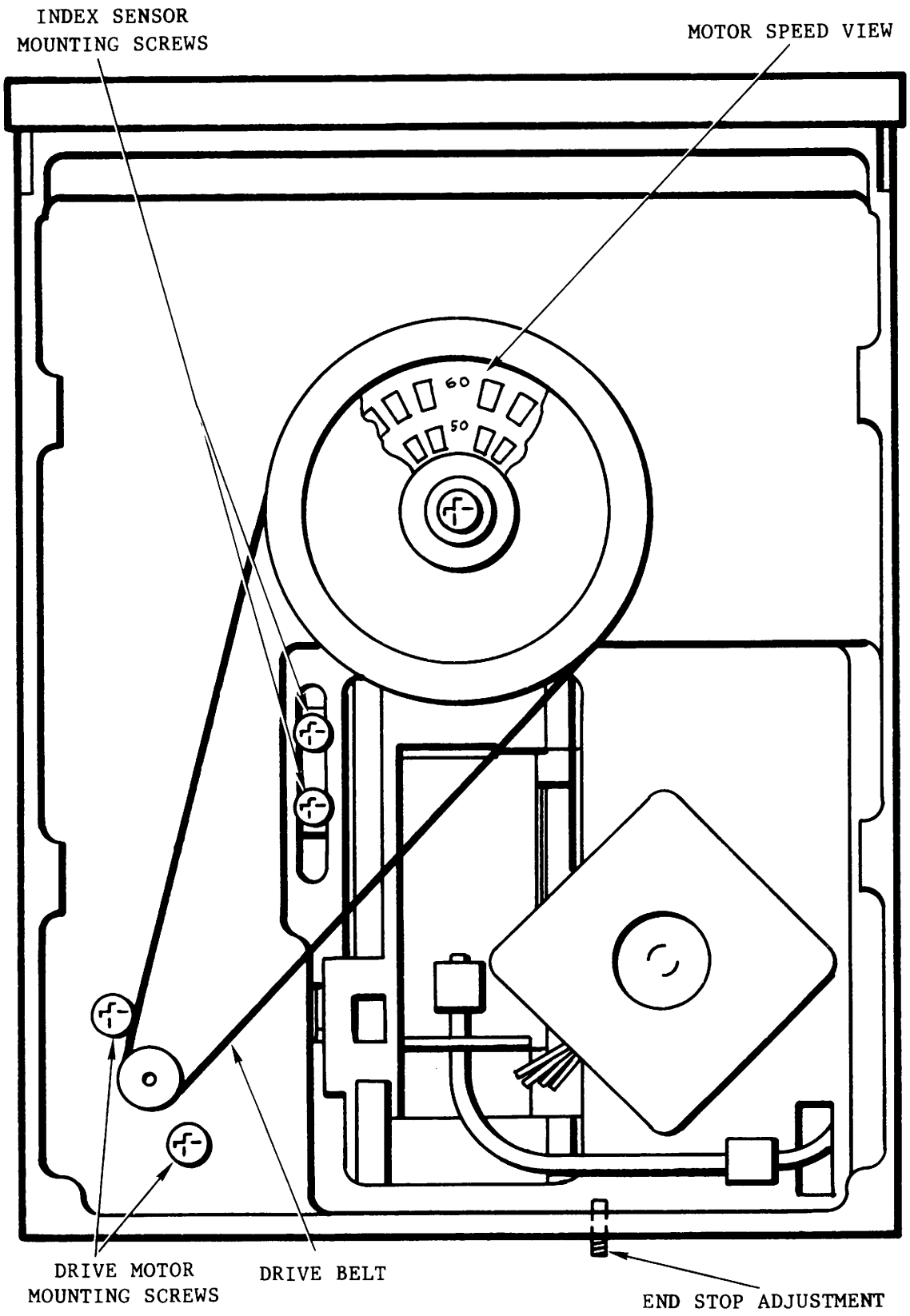


Figure 5-10. MPI 52 Disk Drive Bottom View

5) Verify that both CAT EYES are within 80% amplitude of each other and record the exact amplitude of each EYE. Peaks of unequal amplitude indicate that the head is not centered over track sixteen. The difference in the height of the two peaks is relative to the distance the head is displaced from the center of the track. If the peaks are not within 80% of each other, the physical position of the heads require adjustment.

6) Now drive the heads to track 0 by depressing the number "1" key, then drive the heads back to track 16 by depressing the number "3" key and repeat step 5.

7) Drive the heads to track 40 by depressing the number "4" key, then back to track 16 by depressing the number "3" key and repeat step 5.

8) With the heads at track 16, loosen the set screw in the stepper pulley (see Figure 5-11) using the 0.050 hex screwdriver and CAREFULLY position the pulley until the scope pattern appears with peaks of equal amplitude. *If you mis-adjust the radial-track alignment, one of the EYES will decrease in amplitude while the other increases in amplitude.

```
**********************************************************
*                        CAUTION                         *
*                                                        *
*  BE GENTLE:  A VERY SMALL ADJUSTMENT TO THE STEPPER    *
*  PULLEY INCREASES THE HEAD POSITION SIGNIFICANTLY.     *
*                                                        *
**********************************************************
```

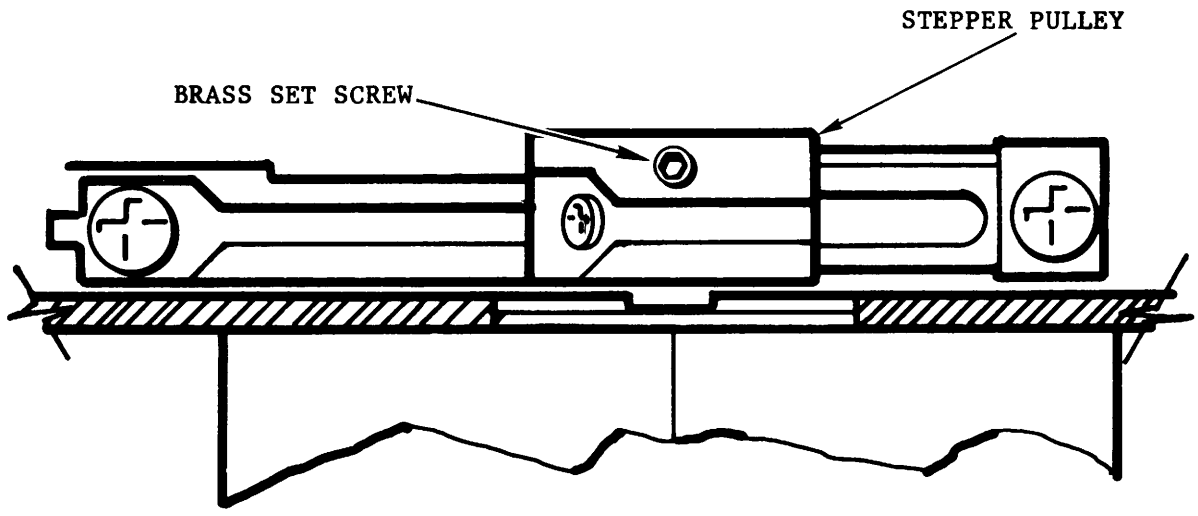


Figure 5-11. Stepper Pulley/Band Assembly

9) When the pattern is correct, tighten the set screw with "2 inch-pounds" of torque, which if you don't have a torque screwdriver is a fairly gentle twist. If the screw is made excessively tight, it will damage the motor shaft and make future adjustment extremely difficult if not impossible.

TO VERIFY ALIGNMENT:

10) Command a return to track 0 by depressing the number "1" key and then step forward to track 16 by depressing the number "3" key. Now step the heads to track 40 by depressing the number "4" key and then return to track 16 by depressing the number "3" key. If the pattern shifts, repeat the adjustment procedures and verify again.

11) If you are unable to meet the tolerance called out in step 5, the Drive must be replaced. Refer to paragraph 5.5.1.

5.3.2.4 MPI INDEX-TO-DATA ALIGNMENT

The Index-To-Data alignment pertains to an interval between the sensing of the Track-Index and the actual transmission of data. A standardized Index-to-Data interval is required to allow the interchangeability of diskettes.

1) Set up the Oscilloscope as follows:

Scope channel A: TP1 on drive PCB
Scope channel B: TP2 on drive PCB
Ground scope probes to ground leads of capacitors C30/C31
Time Base: 50 Mircosecond per division
Amplitude: .1 volt per division
Coupling: dc
External Trigger: TP6 with probe ground to C30/C31
Trigger Mode: Positive
Read Differentially: A plus B, B inverted

2) Verify the radial-track alignment (paragraph 5.3.2.3).

3) Step the head to Track 1 by depressing the number "2" key. The Data Pattern on the oscilloscope should start 200 ±100 microseconds from the start of the trace (Figure 5-8). If this condition is not met, perform the following adjustment:

4) Loosen the 2 Phillips head INDEX SENSOR Mounting screws located at the bottom of the drive in the recessed area. See Figure 5-10. (Note the mounting holes are slotted.)

5) Carefully slide the Sensor back and forth until the oscilloscope shows a data pattern starting 200 ±100 microseconds from the start of the trace.

```
**************************************************
*                    CAUTION                     *
*                                                *
*  DO NOT OVERTIGHTEN THESE SCREWS OR YOU MAY    *
*  BREAK THE PLASTIC SENSOR MOUNTING BLOCK.      *
*                                                *
**************************************************
```

6) Use a 20 inch-ounce torque screwdriver to tighten the sensor mounting screws, and recheck the data pattern for proper tolerance.

5.3.2.5 MPI TRACK 00 END STOP

1) Verify the radial-track alignment (paragraph 5.3.2.3).

2) Check that a maximum track seek (Key 4) and a return to Track 00 (Key 1) will cause the carriage to be within "ten thousandths" (.010) of an inch from the end stop. The end stop is a black setscrew in the frame which can be seen by looking straight down at the rear of the drive (see Figure 5-10).

3) If this specification is not met, perform the following:

   Adjust the set screw in or out until the carriage comes to rest approximately ten-thousandths (.010) of an inch away from it (.010 of an inch is equal to a half a turn of the set screw).

   Verify the adjustment by Commanding a maximum track seek (Key 4) and a return to Track 00 (Key 1). Be sure that the carriage does not hit the end stop.

5.3.2.6 MPI DRIVE BELT ADJUSTMENT

The new model drives all have neoprene (black) drive belts. Older Model drives have mylar (yellow) belts. They are adjusted differently as follows:

1) Mylar (Yellow) Drive Belt Adjustment

   Loosen the drive motor mounting screws (bottom of chassis). Adjust the drive motor so that the tension on one leg of the drive belt is 17 $\pm$ 1 grams. A tensionmeter may be used to make this measurement. Tighten the drive motor mounting screws after adjusting the belt.

2) Neoprene (Black) Drive Belt Adjustment

   Loosen the drive motor mounting screws (bottom of chassis). Position the drive motor as close to the spindle assembly as possible. Tighten the drive motor mounting screws. No belt tension measurement is necessary.

5.3.2.7 MPI WRITE-PROTECT CHECK

The MPI drive write-protect consist of a LED and a phototransistor. When a write-protected diskette (tab ON) is inserted, the light from the LED is blocked reverse-biasing the phototransistor presenting a high to J4 pin 16. When a non-write protected diskette (tab OFF) is inserted, the light from the LED forward-biases the phototransistor presenting a low at J4 pin 16. For the following test point locations refer to Figure 5-9.

Scope Setting:

Scope channel A: J4 Pin 16
Ground scope probe to C30/31
Time Base: 50 Millisecond per division
Amplitude: 2 Volts per division
Trigger: Internal, auto
Coupling: dc

1) Insert a non-write protected diskette (tab OFF) into the drive and close the door. J4 pin 16 should be at logic 0 (Ground).

2) Insert a write protected diskette (tab ON) into the drive and close the door. J4 pin 16 should be at logic 1 (+5V).

3) If either reading is incorrect, replacement of the drive is required. Refer to paragraph 5.5.1 System Unit Disassembly.

5.3.3 WINCHESTER DRIVE ADJUSTMENTS

The Winchester Drive is a Field Replaceable Unit Only. No corrective maintenance is performed on this unit.

5.4 VIDEO MONITOR ADJUSTMENTS

Two monitor alignments are discussed, the first is for systems using only a Character display, the second is for systems using both a Character and Graphics display. Monitor alignment is required every time the Monitor board is replaced and when drifting of the display occurs due to aging.

The Video Monitor adjustments entail the adjustments for vertical linearity, vertical size, vertical hold, focus, width, and horizontal hold. Refer to the Monitor Board component layout in Figure 5-12 for the 8244 PCB or Figure 5-13 for the 8344 PCB adjustment locations.

Equipment Required:

Wang Standard Tool Kit	WLI P/N 726-9401
Wang Diagnostic Diskette	WLI P/N 732-0022
Six Inch Ruler	
Eight Inch Ruler	

5.4.1 VIDEO MONITOR ADJUSTMENTS FOR CHARACTER DISPLAY ONLY

Two Video Monitor adjustments for Character Display are discussed. The first is the Video Monitor adjustments using the Floppy-Based Diagnostics. The second is the Video Monitor adjustments when the Floppy-Based Diagnostics are not available. This is accomplished by writing a short BASIC program.

NOTE

COMPONENT LOCATIONS FOR THE 8244 PCB ARE ENCLOSED IN PARENTHESIS ( ), AND COMPONENT LOCATIONS FOR THE 8344 PCB ARE ENCLOSED IN BRACKETS [ ].

5.4.1.1 VIDEO MONITOR ADJUSTMENTS USING FLOPPY-BASED DIAGNOSTIC

1) Power-Off the System and remove the Monitor Cables and the Monitor cover as described in the Removal and Replacement procedures Section 5.5.2. DO NOT remove the Monitor's Contrast or Brightness knobs.

```
**********************************************************************
*                              CAUTION                               *
*                                                                    *
*  HIGH VOLTAGE IS PRESENT ON THE COMPONENT SIDE OF THE MONITOR      *
*  BOARD.  ALL ADJUSTMENTS (EXCEPT THE HORIZONTAL HOLD) WILL BE      *
*  MADE FROM THE NON-COMPONENT SIDE OF THE BOARD THROUGH ACCESS      *
*  HOLES LABELED DENOTING THE ADJUSTMENT POTENTIOMETERS.             *
*                                                                    *
**********************************************************************
```

2) Reconnect the Monitor Cables.

3) Insert the Diagnostic diskette (WLI P/N 732-0022) into Floppy Drive A and Power-On the System. The Diagnostic Disclaimer screen will appear on the screen. Hold down the "2nd" key and depress the letters "d" then "m" to display the CE Menu.

4) Depress the "RETURN" key, then the "SPACE BAR" to locate the select block next to "Select by Manual Entry" then depress the "EXECUTE" key to display the list Diagnostic tests. Step the cursor down to Wang Monitor attributes Test and select it by depressing the "INSERT" key. Depress the "EXECUTE" key to run the test. When the attributes come up on the screen, depress the "MOVE" key and the screen will fill with "HO" characters. This display will be used for the following monitor adjustments.

5) Adjust the Vertical Hold (R45) [R6] to the center of its stable range.

6) Adjust the Vertical Size (R36) [R7] for a vertical display height of 6 $\pm$ 1/8 inches (15.2 cm $\pm$ 3 mm). This measurement is the character display height, NOT the height of the raster.

7) Adjust the Vertical Linearity Control (R19) [R5] for character rows of equal height. Repeat steps 6 and 7 as required to achieve proper results.

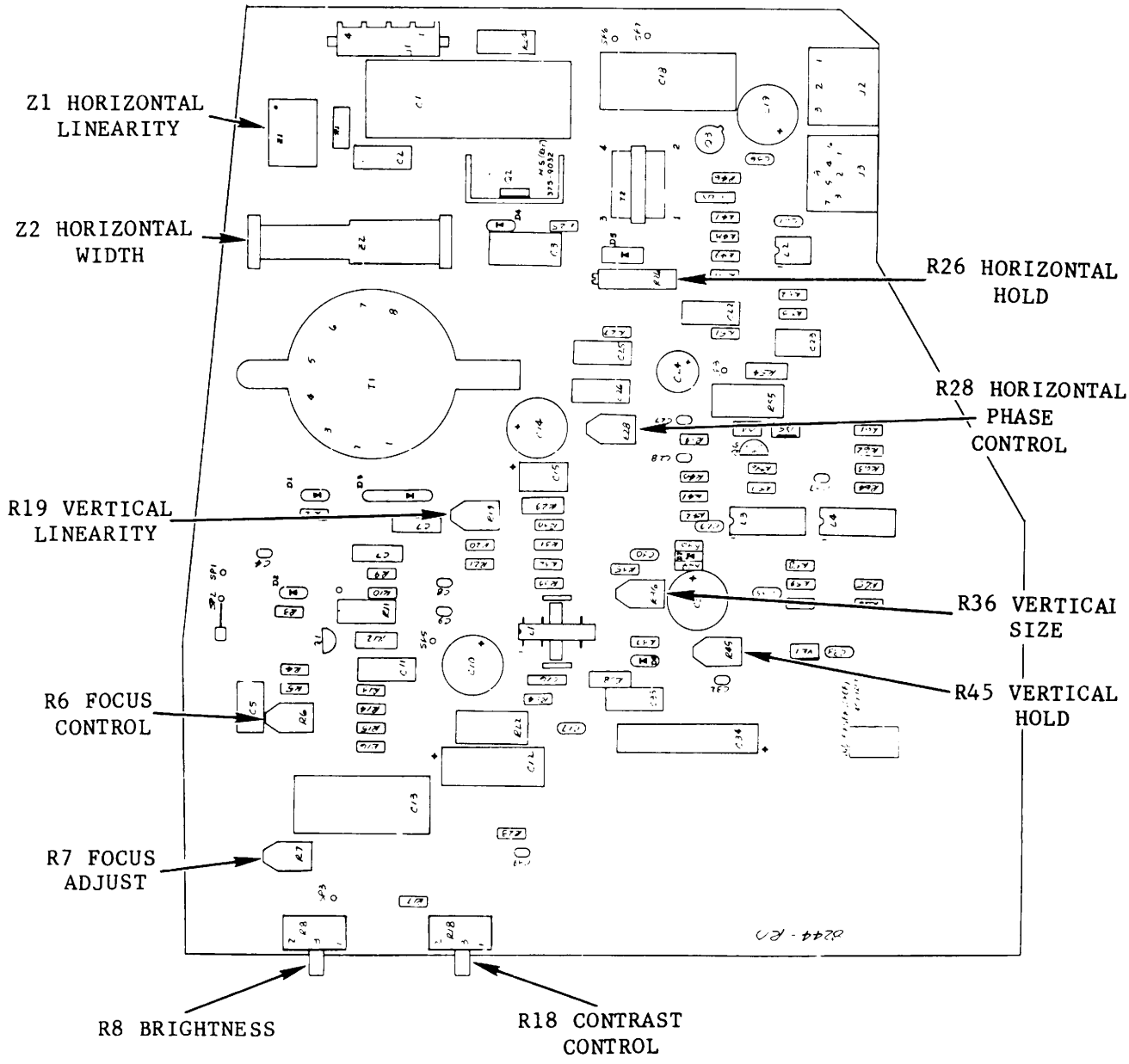


Figure 5-12. Monitor Board 8244 Test Point Locations

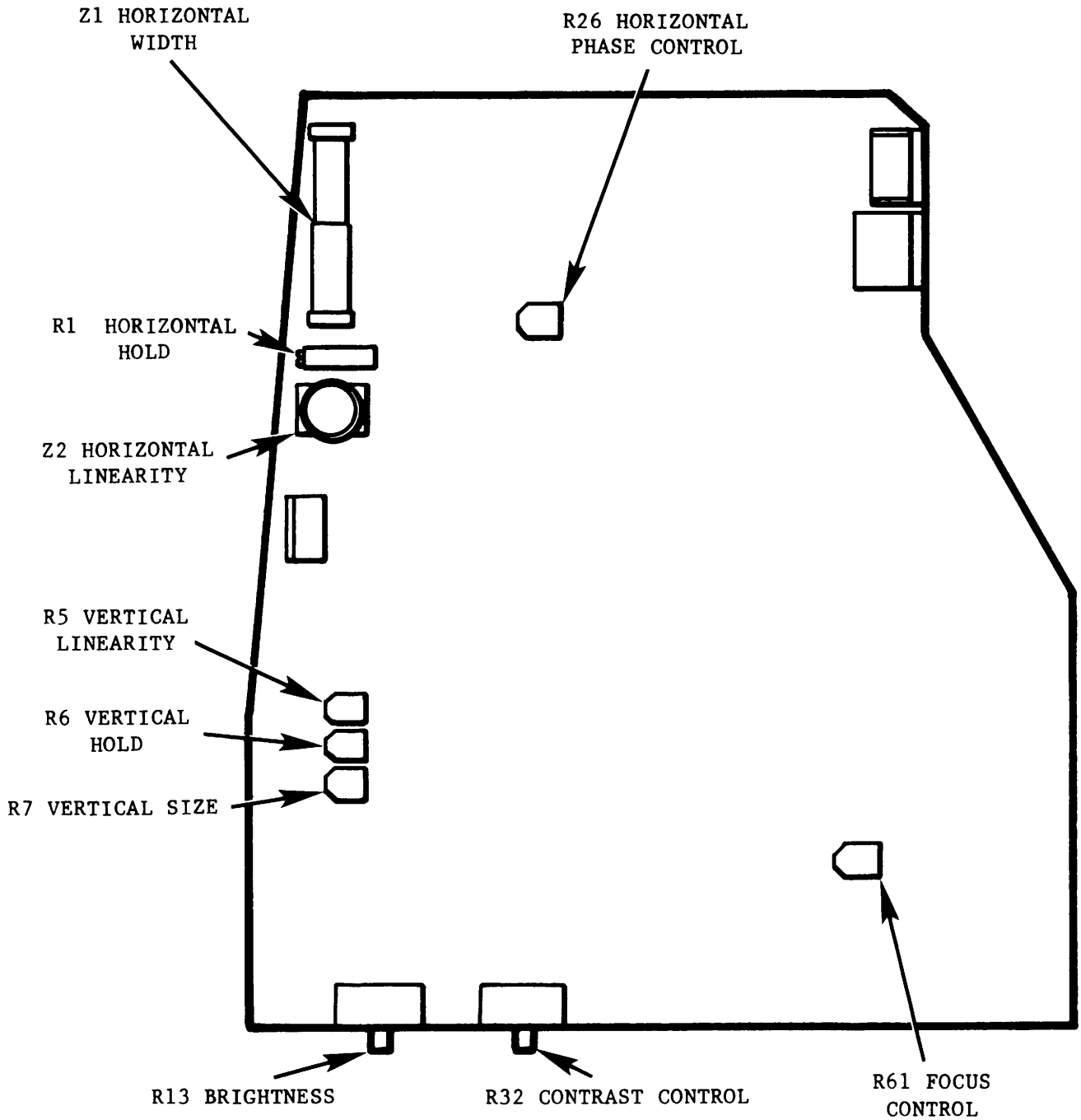


Figure 5-13. Monitor Board 8344 Test Point Locations

8) Check the display width to be within 19.7 to 21 cm (7 3/4 to 8 1/4"). This measurement is the character display width, NOT the width of the raster. This is a factory adjustment and should not have to be made in the field. If this adjustment is needed, adjust the Horizontal Width Coil (Z2) [Z1].

9) Adjust the Horizontal Phase Control (R28)[R26] completely counterclockwise.

10) Adjust the Horizontal Hold pot (R26) [R1] clockwise so that the video pattern overlaps at the left most edge and touches the left edge of the HO pattern.

11) Adjust the Horizontal Phase Control (R28) [R26] to center the characters horizontally on the raster. Turn up the Brightness Control (R8) [R13] located on the front panel so the raster can be observed. Adjust the Focus Control (R6) [R61] for the best overall screen display.

12) Power OFF and reassemble the Monitor unit. Run the diagnostics to check out the system.

5.4.1.2 VIDEO MONITOR ADJUSTMENTS (Diagnostic Unavailable)

If the Floppy Diagnostic Diskette is not available, perform the following to display the "HO" pattern.

1) Perform steps 1 and 2 of Paragraph 5.4.1.1 Video Monitor Adjustments Using Floppy-Based Diagnostic.

2) Insert the System Diskette (with BASIC programming) into Floppy Drive A and power-on the system. Enter the current date and time to access the Main System Menu.

3) Select the Dos Command Processor and depress the "EXECUTE" key. The following will be displayed:

A:_ (Denotes Drive A)

4) Type in "BASIC" (to select the BASIC program) and depress the "RETURN" key. Now enter the following basic program:

```
10 CLS  [CR]                 (CLS denotes Clear Load Screen)
20 FOR A = 1 TO 960  [CR]    (Total Characters on Screen to be displayed)
30 PRINT "HO";  [CR]         (Characters to be printed on the screen)
40 NEXT A  [CR]              (Loop command to Load screen from 1 to 960)

                             NOTE:  [CR] DENOTES "RETURN" KEY
```

5) Now type in "RUN" followed by depressing the "RETURN" key. The Monitor will display 23 lines of "HO" characters (a full screen minus the two bottom lines). This display will be used for the following Monitor adjustments.

6) Now perform steps 5 through 11 as described in paragraph 5.4.

7) When all adjustments are made, exit from the program by entering:

"SYSTEM" [CR]

This will return you to the Dos Command Processor and an A:_ will be displayed. Now type in:

EXIT [CR]

This command will return the system to the Main Menu.

8) Power-Off the system unit and reassemble the Monitor unit. Run the diagnostics to check out the system.

5.4.2 VIDEO MONITOR ADJUSTMENTS FOR CHARACTER AND GRAPHICS DISPLAY

The following Monitor adjustments are required when a Graphics board and Character board are used to drive the Video Monitor.

1) Power-Off the System and remove the Monitor Cables and the Monitor cover as described in the Removal and Replacement procedures paragraph 5.5.2. DO NOT remove the Monitor's Contrast or Brightness knobs.

```
**********************************************************************
*                              CAUTION                               *
*                                                                    *
*  HIGH VOLTAGE IS PRESENT ON THE COMPONENT SIDE OF THE MONITOR      *
*  BOARD.  ALL ADJUSTMENTS (EXCEPT THE HORIZONTAL HOLD) WILL BE      *
*  MADE FROM THE NON-COMPONENT SIDE OF THE BOARD THROUGH ACCESS      *
*  HOLES LABELED DENOTING THE ADJUSTMENT POTENTIOMETERS.             *
*                                                                    *
**********************************************************************
```

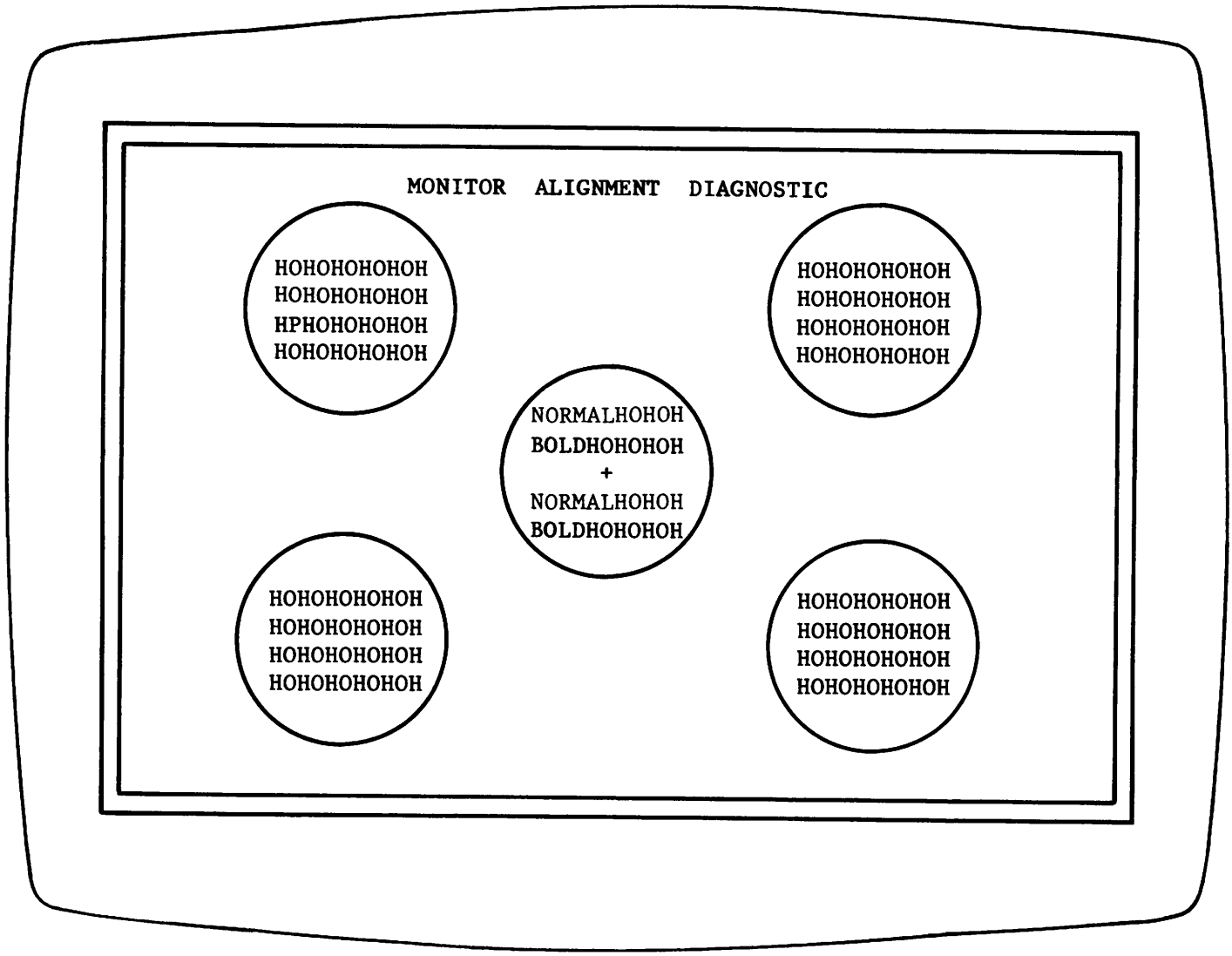
2) Reconnect the Monitor Cables.

3) Insert the Diagnostic diskette (WLI P/N 732-0022) into Floppy Drive A and Power-On the System. The Diagnostic Disclaimer screen will appear on the screen. Hold down the "2nd" key and depress the letters "d" then "m" to display the CE Menu.

4) Depress the "RETURN" key, then the "SPACE BAR" to locate the selection block next to "Select by Manual Entry" then depress the "EXECUTE" key to display the list of Diagnostic tests. Step the cursor down to "Wang Monitor Alignment" and select it by depressing the "INSERT" key. Depress the "EXECUTE" key to load the alignment into the system. The following alignment tests will be used for monitor adjustments.

6) Three different tests can be displayed on the monitor screen. These are: INVERSE VIDEO SCREEN, MONITOR ALIGNMENT SCREEN, and the GRID PATTERN SCREEN. Depress the space bar once to display the INVERSE VIDEO SCREEN. This screen load is referenced later in step 25.

7) Now depress the SPACE BAR to display the MONITOR ALIGNMENT TEST. The display shown in Figure 5-14 will be displayed. Note that the screen in the text is a representation of the actual screen being displayed and is not drawn to scale.



NOTE: NOT TO SCALE
CIRCLES ARE 2 INCHES IN DIAMETER

Figure 5-14. Monitor Alignment Screen

8) Depress the SPACE BAR once more to display the GRID PATTERN as shown in Figure 5-15.

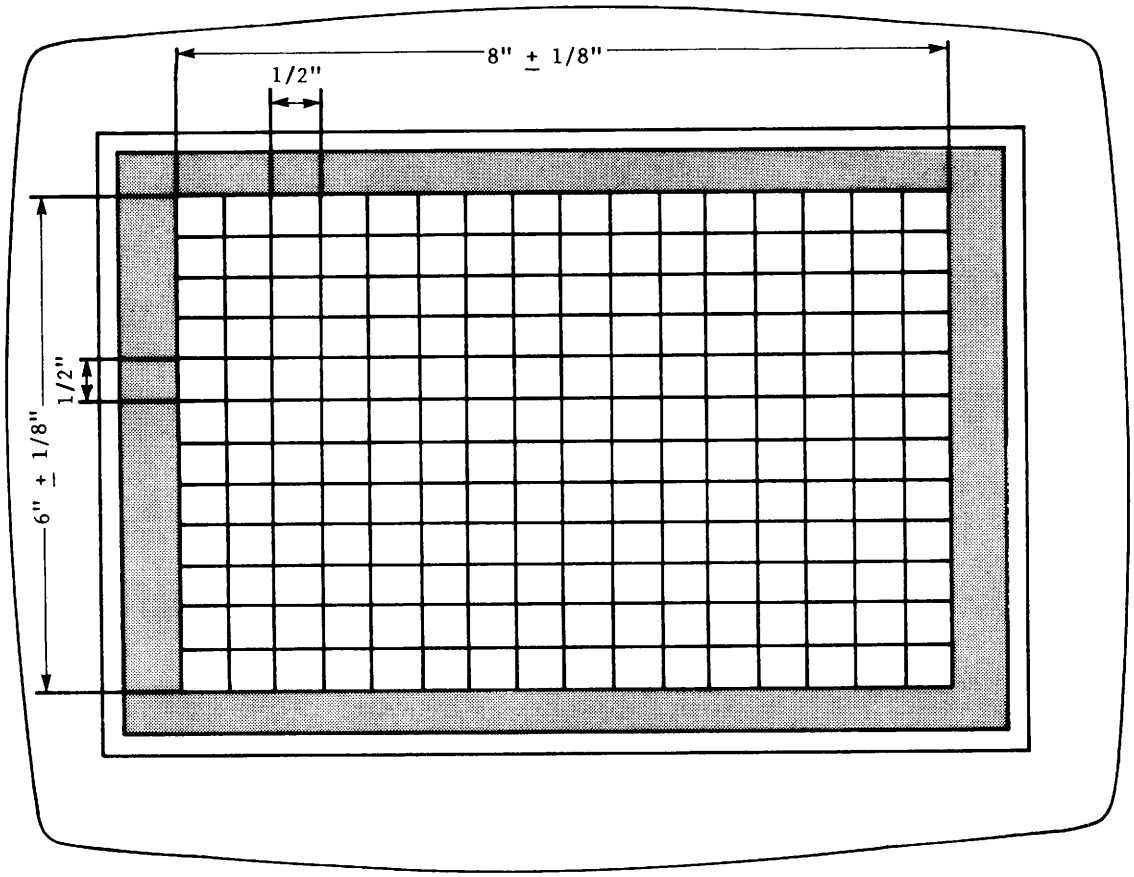


Figure 5-15. Monitor Alignment Grid Pattern

Alignment Procedures

9) Depress the SPACE BAR twice to display the Monitor Alignment Screen.

10) Adjust the Horizontal Phase pot (R28)[R26] completely counterclockwise.

11) Adjust the Horizontal Hold (R26) [R1] so that the video pattern overlaps at the left most edge and touches the left edge of the two left most circles. Refer to Figure 5-16.

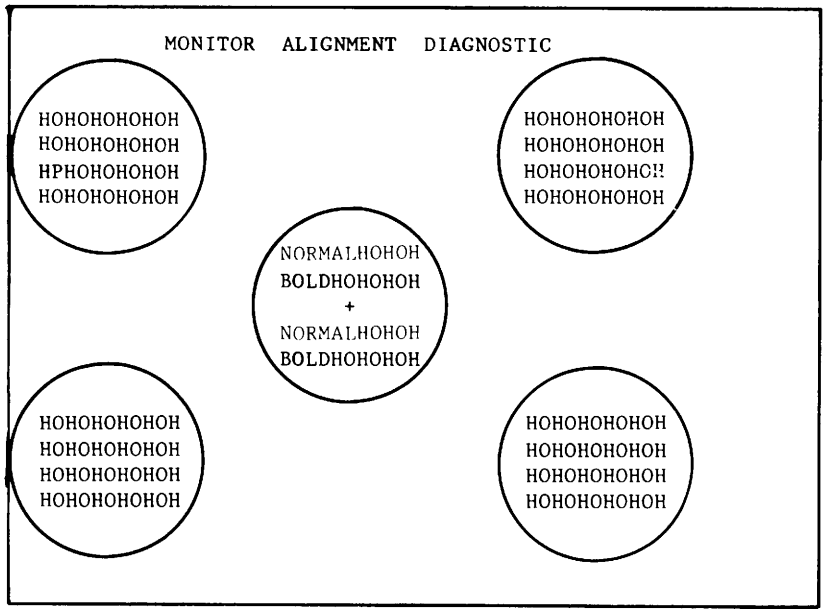


Figure 5-16. Monitor Alignment Screen Horizontal Hold Adjustment

12) Adjust the Horizontal Phase Control pot (R28) [R26] to center the display within the raster.

13) Now, depress the SPACE BAR once to display the Monitor Alignment Grid Pattern. Refer to Figure 5-15.

14) Adjust the Vertical Hold (R45) [R6] to the center of its stable range.

15) Now adjust the Vertical size (R36) [R7] for a display height of 6 inches $\pm$ 1/8 inch (15.2 cm $\pm$ 3 mm). See Figure 5-15.

16) Adjust the Horizontal Width coil (Z2) [Z1] for a display width of 8 inches $\pm$ 1/8 inch (20.3 cm $\pm$ 3 mm). See Figure 5-15.

17) Adjust the Vertical Linearity (R19) [R5] so the squares at the top of the display are the same vertical size as the squares at the bottom of the display. This adjustment may affect the Vertical height, repeat step 13 if required.

18) Adjust the Horizontal Linearity coil (Z1) [Z2] so the width of the squares along the left-hand margin are the same width as the squares along the right-hand margin. Now recheck the display width (step 14) and readjust if required.

19) Adjust the two tabs around the CRT neck one at a time to center the display and to eliminate any barreling, pincushioning, or distortion. Refer to Figure 5-17 for example of Barreling and Pincushioning.

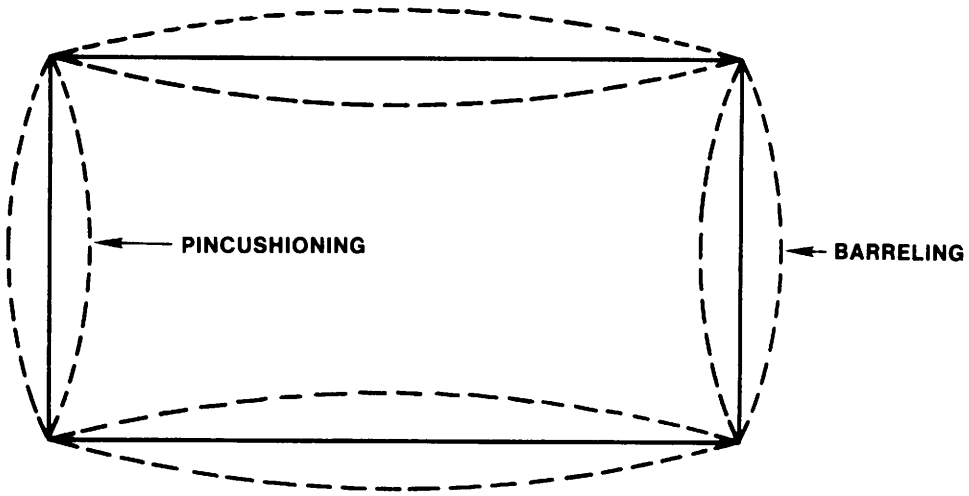


Figure 5-17. Pincushioning and Barreling of CRT

20) Place the 8 inch scale parallel to the top matrix line on the display. It should be straight to within ± 1/16 of an inch (1.5 mm).

21) Now check the right and left margins with the scale. Both margins should be straight to within ± 1/16 of an inch (1.5 mm).

22) If the display can not be brought into tolerance with the centering tabs, adjustment of the pincushion magnets is required. Adjust the pincushion magnets one at a time to remove pincushioning or barreling. Now measure each square for 1/2 inch ± 1/16 inch sides (13 mm ± 1.5 mm). If the vertical sides become out of tolerance, readjust the Vertical size and linearity. If the Horizontal sides of the squares become out of tolerance, readjust the Horizontal width and linearity. Measure the display height and width for proper tolerance.

23) Depress the SPACE BAR twice to display the MONITOR ALIGNMENT SCREEN as shown in Figure 5-14. The five circles should appear perfectly round. The circles measure 2 inches in diameter. If the circles are distorted, recheck the adjustments in steps 9-19.

24) Now adjust the Focus Control (R6) [R61] for the best overall display pattern.

25) To adjust Brightness and Contrast, depress the SPACE BAR to display the INVERSE VIDEO SCREEN. Adjust the Brightness control for normal viewing. Then adjust the Contrast control for the best overall viewing level between the normal display level and the reverse video level. To check adjustments depress the SPACE BAR to display the MONITOR ALIGNMENT SCREEN.

26) If all the forementioned adjustments does not bring the display into tolerance, replacement of the monitor is recommended. If the monitor adjustments are within tolerance, Power-Off the system unit and reassemble the Monitor.

5.5 REMOVAL AND REPLACEMENT

The Removal and Replacement procedures will enable the AFET to remove and replace defective units to the Field Repair level. Options to be installed are discussed in Chapter 4.9.1 System Expansion.

5.5.1 System Unit Disassembly

1) Turn the Power Switch (labeled I/O) to the OFF Position. Disconnect all the cables (ie. the ac power cable, the keyboard cable, the monitor cable) from the rear of the System Unit.

2) Position the System Unit horizontally (air vents pointing down) and remove the four Phillips-head screws from the rear corners of the unit (see Figure 5-18).

3) Grasp the vertical angle bracket located on the rear of the unit with one hand and hold the cover with the other hand and carefully pull the unit straight out of the cover. Set the cover to the side.

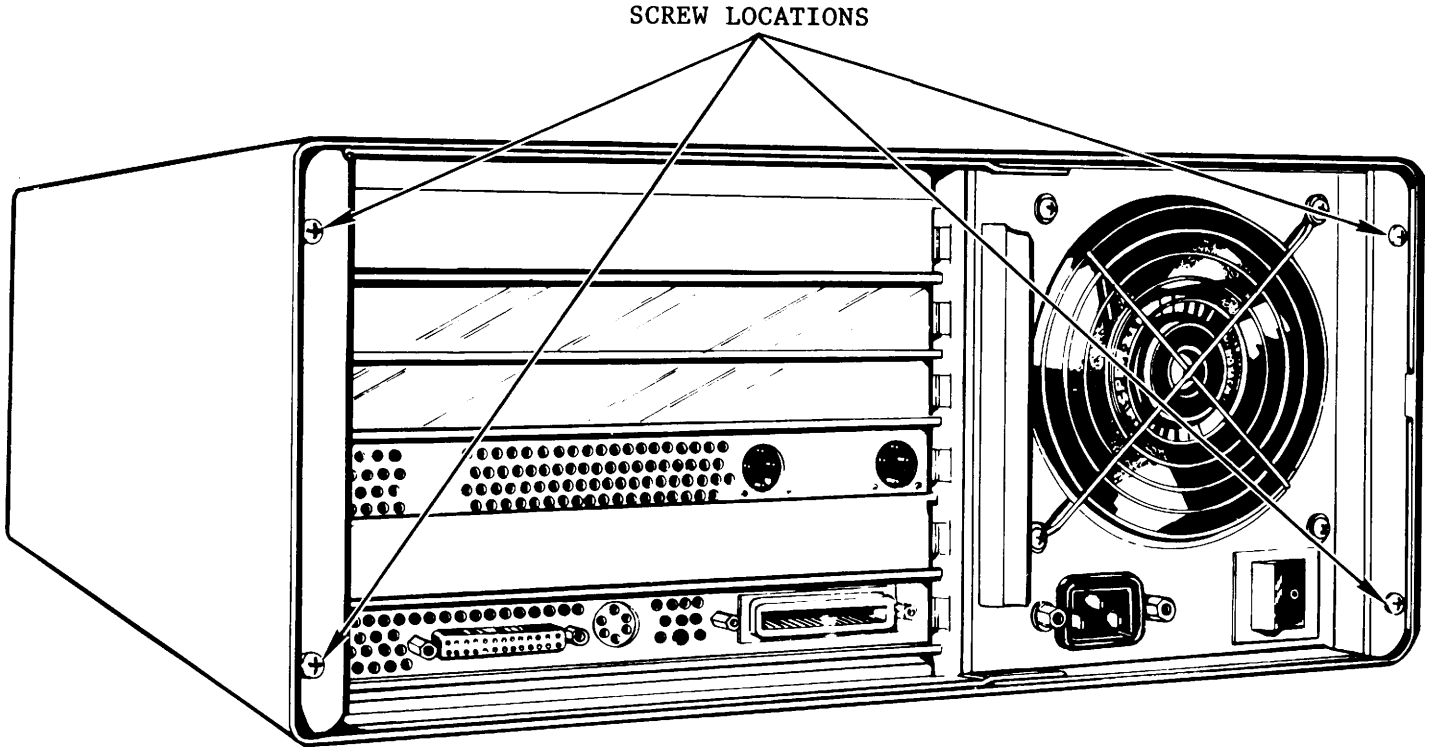


Figure 5-18. System Unit Cover Removal

System Board Removal and Replacement

4) Now set the System Unit in the Vertical position (see Figure 5-19) with the power supply down and carefully remove the System Floppy Drive ribbon cable from the top left connector J5 and remove Floppy Drive B ribbon cable (if any) from connector J6 located on the 210-8221 System board. Pull enough ribbon cable slack to move the connectors out of the way (over the side of the floppy drive).

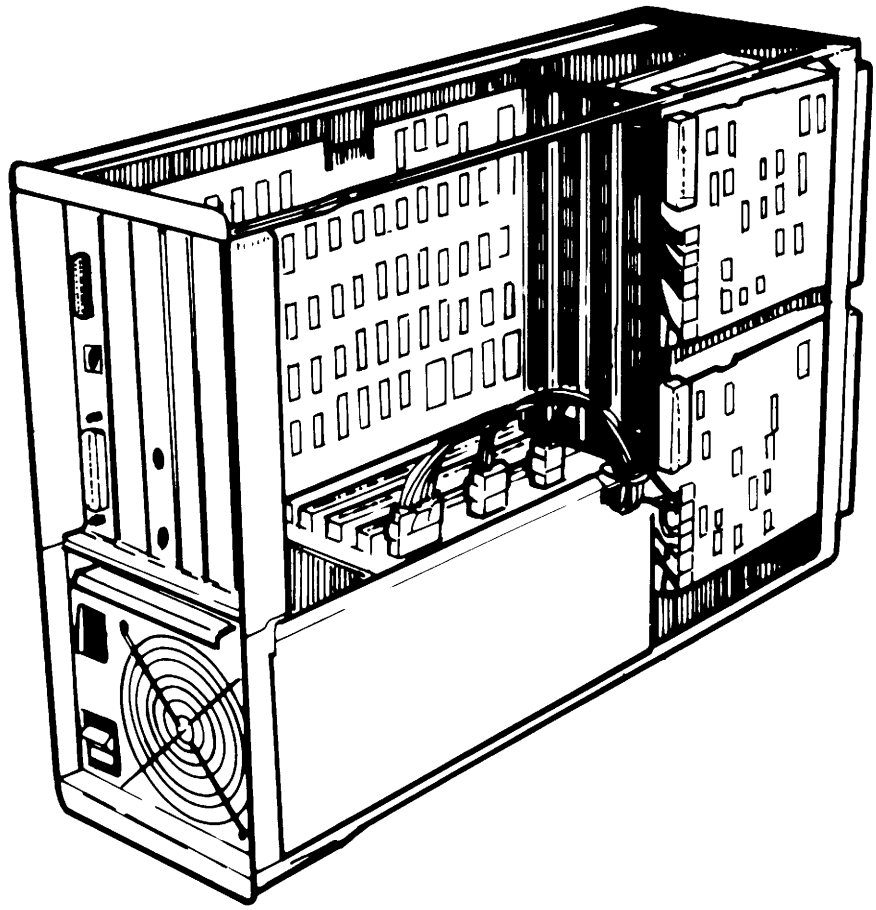


Figure 5-19. Electronic Unit in Vertical Position

5) At the top left (rear of unit) of the System board, remove the Phillip head screw from the RF shield tab (attached to the System board). This screw holds the System board in place. Remove the System board by placing your fingers between the system board and the top of the power supply. Push up on the system board in order to free it from the motherboard connector. Carefully pull the System board up until it clears the card guides. Be sure the floppy drive ribbon cables are out of the way to prevent the cables from being damaged.

6) To install a System Board, reverse the procedures in steps 4 and 5.

Option Board Removal and Replacement

7) At the top left (rear of the unit) of the option board, remove the Phillips-head screw from the RF shield tab attached to the board. This screw holds the option board in place. Remove the option board by pulling up on one side then the other in order to free it from the motherboard connector. Then slide the option board out of the card guides. Repeat this procedure for other option boards that are to be removed.

8) To install an option board, reverse the procedure in step 7.

5.5.1.1 POWER SUPPLY REMOVAL

One of two power supplies are used in the PC; a Wang power supply or a Zenith power supply. The only difference is the main harness assembly. The Wang power supply uses a plugable wiring harness whereas the Zenith power harness is built into the supply. The Wang power supply replacements are shipped with the harness assembly.

```
**********************************************************************
*                              CAUTION                               *
*                                                                    *
*  AFTER POWERING DOWN THE UNIT AND DISCONNECTING THE AC POWER       *
*  PLUG FROM THE AC POWER RECEPTACLE,  ALLOW ONE MINUTE BEFORE       *
*  REMOVING THE POWER SUPPLY TO PROVIDE  ADEQUATE TIME FOR ANY       *
*  RESIDUAL VOLTAGE TO DRAIN THROUGH THE BLEEDER RESISTORS.          *
*                                                                    *
**********************************************************************
```

1) Remove the ac cable from the power supply (if not previously removed). With the System unit in the vertical position (power supply down) and the Electronic Unit cover removed, remove the two screws at the rear of the unit that secure the power supply to the system rear panel. Be sure not to remove the two screws that mount the fan guard to the power supply. Then remove the one screw located on the side of the power supply directly below the non-component side of the system board.

2) Remove the main harness assembly connectors from the Motherboard connectors J1, J2, and J3. Remove the main harness connector (power) from the System Floppy Drive. Remove the Main Harness connector (power) from the optional Floppy Drive or Winchester Drive if installed.

3) Facing the rear of the unit, slide the power supply and harness assembly to the right and out of the unit. Note that the harness assembly is removed with the power supply.

4) Before replacing the power supply, check for the proper voltage setting as discussed in Chapter 4 paragraph 4.7.2. To replace the Power Supply, reverse the procedure as describe above.

5.5.1.2 Floppy Drive Removal and Replacement

1) Remove the Electronics Unit cover as discussed in paragraph 5.5.1 steps 1 thru 3.

2) With the Electronics Unit in the vertical position (power supply down) remove the screw holding the floppy drive in place.

3) Slide the drive out far enough to enable the removal of the power cable and the ribbon cable. Once removed slide the drive out of the unit.

4) When replacing the drive, ensure the drive's metal plate is attached. If not, remove the metal plate from the previously removed drive and attach it to the drive to be installed.

5) Ensure the drive's PCB is configured properly, refer to paragraph 4.7.6 for the correct configuration in regard to vendor and whether the drive is to be installed in Drive A or Drive B.

6) Slide the drive partially into the System Unit being sure the drives metal plate is sliding in the nylon guide provided. Now reconnect the two cables removed in step 3.

7) Slide the drive the rest of the way into the System Unit being careful not to crimp either of the two cables. Secure the drive in place with the screw removed in step 2.

5.5.1.3 Winchester Drive Removal and Replacement

1) Remove the Electronics Unit cover as discussed in paragraph 5.5.1 steps 1 thru 3.

2) With the Electronics Unit in the vertical position (power supply down) remove the screw holding the Winchester drive in place.

3) Slide the drive out far enough to enable the removal of the power cable and the two ribbon cables. Once removed, slide the drive out of the unit.

4) When replacing the drive, ensure the drive's metal plate is attached. If not, remove the metal plate from the previously removed drive and attach it to the drive to be installed.

5) Slide the drive partially into the System Unit being sure the drives metal plate is sliding in the nylon guide provided. Now reconnect the two cables removed in step 3.

6) Slide the drive the rest of the way into the System Unit being careful not to crimp either of the two cables. Secure the drive in place with the screw removed in step 2.

5.5.2 Wang Monitor Disassembly

1) Remove the Monitor cables attached to the rear of the Wang monitor. Remove the two thumb screw wheel knobs located on the front upper left of the monitor. These are removed by pulling them straight out.

2) Turn the monitor upside down, setting it on its top cover. Remove the two screws that hold the cover to the face plate. Turn the monitor right side up and set it back on its pedestal.

****
* WARNING *
*
* DO NOT TWIST THE SCREWDRIVER WHILE PERFORMING THE MONITOR *
* COVER REMOVAL. THIS WILL RESULT IN DAMAGING THE COVER. *
*
****

3) Using a small flat-blade screwdriver, push the right rear retaining spring tab holding the cover to the face plate down through its slot to free the cover on the right side. Holding the right side cover free, push the left rear retaining spring tab down through its slot to free the cover on the left side. Now remove the cover by pulling it straight back to clear the neck of the CRT.

WARNING

CRT DISCHARGE PROCEDURE

Before performing any other removal/replacement procedures, discharge the CRT anode according to the following procedures.

Even with power removed, the Cathode Ray Tube can hold a charge of several thousand volts. To eliminate the risk of accidental CRT discharge, discharge the CRT anode as follows:

4) Attach one end of a length of insulated wire to the metal shaft of a plastic-handled, heavy-duty screwdriver.

5) Attach the other end of the wire to chassis ground.

6) Using a non-conductive tool such as a plastic alignment tool, carefully raise the edge of the rubber anode cap enough to insert the screwdriver.

7) Taking care not to touch the metal shaft of the screwdriver or any metal part of the Monitor, discharge the CRT anode by touching the anode clip with the grounded screwdriver.

8) After discharging the CRT, remove the grounding wire and reseat the rubber anode cap.

9) Unplug the CRT cable connector from J1 located at the rear of the monitor board and disconnect the "FASTON" clip from the retaining screw ground lug located at the top left side near the monitor's Brightness and Contrast potentiometers. Now disconnect the CRT neck socket connector.

10) Disconnect the High-Voltage connector from the CRT and unscrew the monitor board holding screw that holds the monitor board to the faceplate. Removal of this screw requires a long-shafted flat blade screw driver.

11) To reassembly the monitor, reverse the previously discussed procedures. NOTE: It is easier to install the Monitor Board retaining screw with the Monitor setting on its face plate.

5.5.3 KEYBOARD DISASSEMBLY AND REASSEMBLY

```
**********************************************************************
*                              CAUTION                               *
*                                                                    *
*  CAUTION SHOULD BE TAKEN WHILE TURNING THE KEYBOARD OVER.  THE     *
*  THREE PARTS COULD SEPARATE BREAKING EITHER OF THE TWO SPEAKER     *
*  WIRES, EITHER AT THE SPEAKER OR AT THE SPEAKER CONNECTOR  J1.     *
*                                                                    *
**********************************************************************
```

1) Disconnect the keyboard cable from the system unit.

2) Turn the Keyboard over (setting it on a flat surface) and remove the two screws from the bottom of the unit that hold the assembly together. After removing the screws, carefully turn the keyboard back over and set it in its normal position.

3) Remove the Keyboards top cover and disconnect the cable at connector J1 (located on the top center of the PC board) being careful not to damage the two speaker wires.

4) Remove the Cable Clamp Screw located on the top right corner of the Keyboard PCB.

5) Remove the PC board/Keyboard assembly from the bottom cover. Be sure to leave the J1 plug and cable assembly in the bottom cover.

5.5.3.1 Keyboard Reassembly

6) Reinstall the Cable Clamp Screw to hold the Keyboard cable in place on the replacement keyboard.

7) Install the new PC board/Keyboard into the bottom cover. Reinstall the J1 plug into the J1 connector assembly. Ensure that the static abatement strap is making contact with the bottom housing.

Replace the top cover and check that the keyboard cable is properly positioned in the slot provided and that the two speaker wires are not pinched. Carefully turn the keyboard over and reinstall the two screws that were removed in step 2. Return the keyboard to its normal position and reconnect the keyboard cable to the system unit.

5.6 REASSEMBLY CHECKOUT PROCEDURE

( ) Connect the monitor cable and the keyboard cable to the system unit. Connect the ac power cord to the system unit. Ensure the power switch (I/O) is OFF, plug the ac power cord into the wall outlet.

( ) Insert the MS-DOS System Program Diskette into Drive A and latch the drive door closed. Now Power-On the system unit.

( ) When power is first applied the System Units fan starts, a short beep will sound, the Boot PROM diagnostics will run, the Keyboard LEDs will flash on, and after a short time the Floppy's LED will illuminate. Now the System will execute the IPL (Initial Program Load). After the IPL is completed, the Floppy LED will go out and the Monitor will display the MS-DOS program title and request that the Time and Date be entered.

( ) Enter the current date and time through the keyboard. After these are entered, the MAIN MENU will be displayed confirming the system is operating properly.

CHAPTER 6

SCHEMATICS

Chapter 6 Schematics is not provided in this manual. This information is contained in the Professional Computer Schematics Manual WLI Number 729-1241.

CHAPTER 7

ILLUSTRATED PARTS BREAKDOWN

7.1 SCOPE

The following Illustrated Parts Breakdowns (IPB) provide reference to assemblies that are identified for maintenance procedures. IPB's included in this manual are:

- o Figure 7-1. Low Profile Keyboard
- o Figure 7-2. TTL Monitor Assembly
- o Figure 7-3. CPU Electronics Enclosure

The Part Numbers followed by double asterisk (**) are RSL Items.

LOW PROFILE KEYBOARD ASSEMBLY

ITEM No.	PART No.	DESCRIPTION
	279-2042-US**	UNI/KBD-US (UNITED STATES)
	279-2042-UK**	UNI/KBD-UK (UNITED KINGDOM)
	279-2042-SL**	UNI/KBD-SL (SPANISH-LATIN AMERICAN)
	279-2042-AZ**	UNI/KBD-AZ (AZERTY)
	279-2044-GE**	UNI/KBD-GE (GERMAN EXPANDED)
1	615-2059	STRIP, FUNCTION
2	449-0608	COVER, TOP (NON-EXPANDED)
	449-0611	COVER, TOP (EXPANDED)
3	650-4120	SCREW, 8-32 X 3/8 PAN HD PHIL
	652-0029	LOCKNUT (USE WITH ITEM 3)
4	725-2738-US	KEYBOARD, UNIVERSAL KTC LOW PROFILE (US)
	725-2738-UK	KEYBOARD, UNIVERSAL KTC LOW PROFILE (UK)
	725-2738-SL	KEYBOARD, UNIVERSAL KTC LOW PROFILE (SL)
	725-2738-AZ	KEYBOARD, UNIVERSAL KTC LOW PROFILE (AZ)
	725-2739-GE	KEYBOARD, UNIVERSAL EXP. KTC LOW PROFILE (GE)
5	220-0305	CABLE ASSEMBLY
6	449-0607	BASE, KEYBOARD
7	655-0286	FOOT, 5/8 DIA X 1/8 THICK SELF ADHESIVE
	655-0291	FOOT, 5/8 DIA X 1/16 THICK SELF ADHESIVE
8	650-4160	SCREW, 8-32 X 1/2 PAN HD PHIL
9	320-0306	SPEAKER, ROUND 2 IN. 8 OHM LOW PROFILE

** DENOTES RSL ITEM

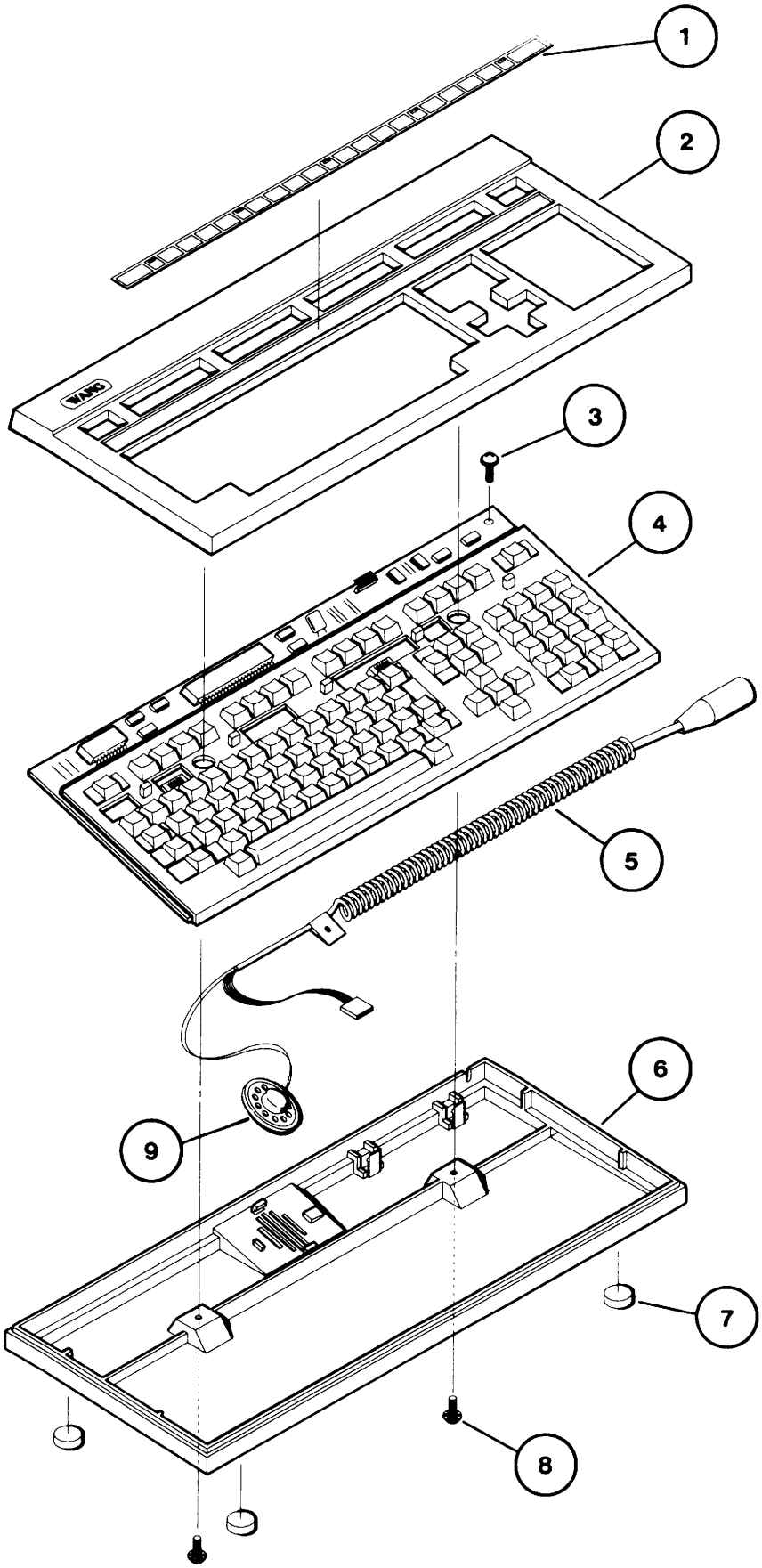


FIGURE 7-1 Low Profile Keyboard

TTL MONITOR ASSEMBLY
279-0541**

ITEM No.	PART No.	DESCRIPTION
1	449-0630	COVER, MONITOR
2	651-0268	FASTENER, #8-32 U-TYPE
3	650-6160	SCREW, 10-32 X 1/2 TRUSS HD PHIL
4	654-0125	TERMINAL LUG, 0.200 HOLE X 1/4 IN. SPADE
5	220-1964	GROUNDING CABLE ASSEMBLY (REQUIRES ITEM 30 FOR INSTALLATION)
6	270-3289	YOKE ASSY (LESS MAGNETS)
	320-0126	MAGNET, 11 GAUSS
	320-0127	MAGNET, 20 GAUSS
	320-0128	MAGNET, 15 GAUSS
7	340-0111	TUBE, C/R 12 IN. (LESS YOKE ASSY)
8	462-0610	STANDOFF, 3/8 HEX X 1-5/8 IN. LONG
9	653-6000	WASHER
10	449-0631	BEZEL, MONITOR
11	650-4121	SCREW, 8-32 X 3/8 PHIL HD FLT (WHITE)
12	650-9077	SCREW, 1/4 - 28 X 1-3/4 HEX
13	449-0635	BELLOW, SLEEVE
14	449-0626	COLLAR, BALL JOINT
15	478-0805	BALL JOINT
16	449-0627	BASE, MONITOR
17	449-0625	CAP SPRING
18	652-0064	STOP NUT, 1/4 - 28
19	650-3160	SCREW, 6-32 X 1/2 PAN HD PHIL
20	655-0286	FOOT, 5/8 X 1/8 SELF-ADHESIVE
21	449-0596	KNOB
22	449-0629	HOLDER, PCB UPPER
23	449-0628	HOLDER, PCB LOWER
24	653-4001	WASHER
25	651-0052	SCREW, 8 X 1/2 SELF TAP PAN HD PHIL
26	451-4985	BRACKET (INCLUDED WITH ITEM 29)
27	220-1263	WIRE AND LUG ASSY (INCLUDED WITH ITEM 29)
28	421-0001**	CABLE ASSY, I/O
29	210-8244**	PCA, MONITOR
	210-8344**	PCA, MONITOR
30	452-2737	CLIP, SPRING
31	653-6006	WASHER
32	465-1637	SPRING (INCLUDED WITH ITEM 5)

** DENOTES RSL ITEM

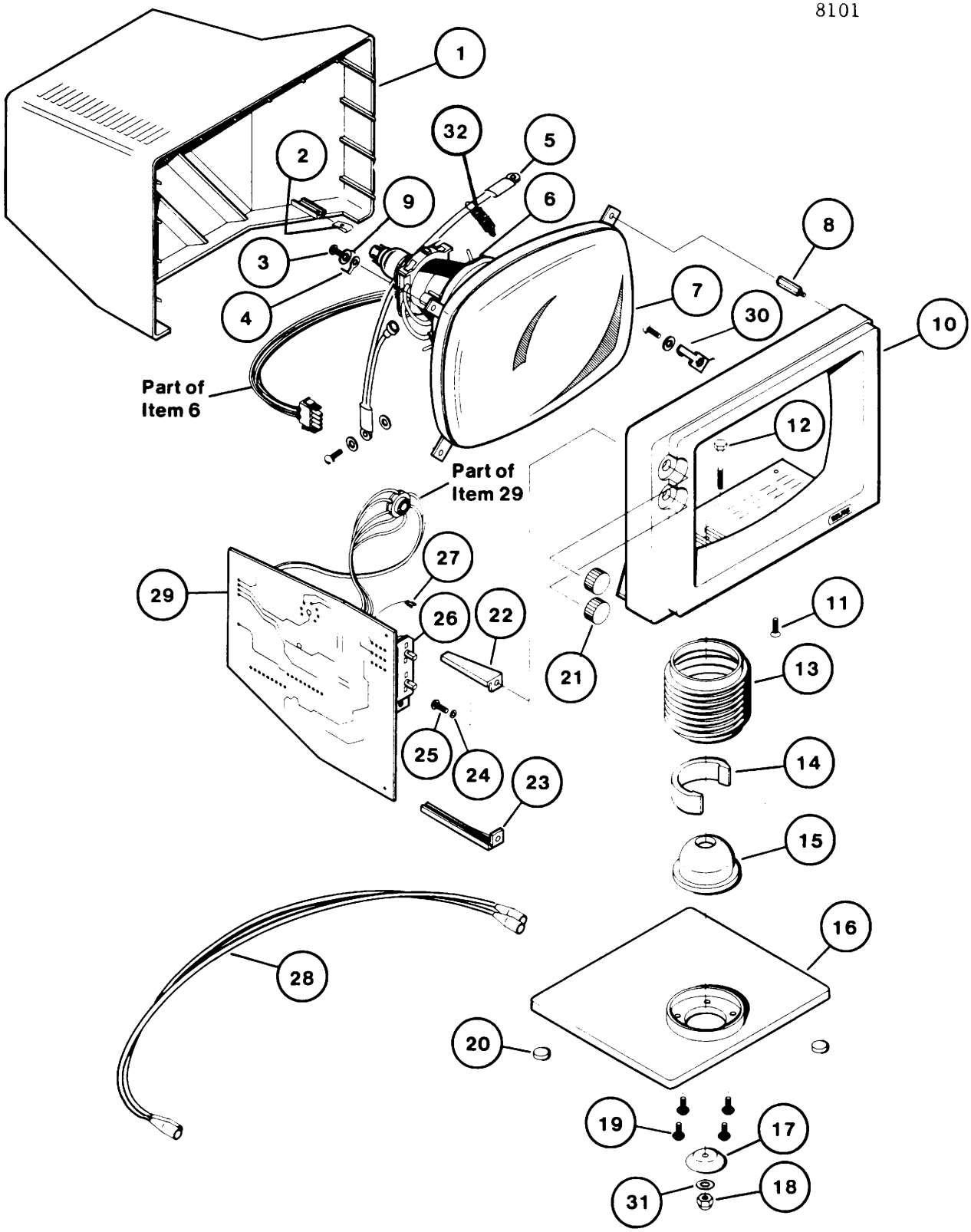


FIGURE 7-2 TTL Monitor Assembly 279-0541

CPU ELECTRONICS ENCLOSURE

ITEM	PART NO.	DESCRIPTION
1	210-8221-A**	PCA, CPU/MEMORY BOARD
2	465-1243	CARD GUIDE, NYLON WHITE 8 IN.
3	452-4042	CARD GUIDE, NYLON WHITE 4 IN.
4	278-4026**	DISKETTE DRIVE, DSDD 48TPI
5	220-3239**	CABLE, SYSTEM DRIVE (USE WITH ITEM 4)
6	465-1242	CARD GUIDE, NYLON WHITE 6 IN.
7	650-3080	SCREW, 6-32 x 1/4 PAN HD. PHIL.
8	450-0153	BEZEL, BLANK OR
	278-4026**	DISKETTE DRIVE DSDD 48TPI (USE CABLE 220-3240**) OR
	278-4030**	WINCHESTER DRIVE 10MB (USE "A" CABLE 220-3240**)(USE "B" CABLE 220-3238**)
9	458-3026	ENCLOSURE, CPU
10	478-0822	PIN GUIDE
11	651-0006	SCREW, #6 SELF TAP 1/2 IN. LONG
12	449-0622	BEZEL, CPU
13	458-3200	CHASSIS, CPU
14	654-1205	GROMMET
15	270-3279**	HARNESS ASSY. (INCLUDES ITEM 14)
16	449-0671	CABLE CLAMP
17	210-8237**	PCA, MOTHERBOARD
18	270-0792**	POWER SUPPLY, SWITCHING SPS 200
19	420-2019	POWER CORD
20	651-0070	SCREW, #8 SELF TAP x 5/8 IN.
	653-4000	#8 FLAT WASHER
21	650-2120	SCREW, 4-40 x 3/8 IN.(1200 UNITS
	652-0032	#6 LOCKNUT AND BELOW)
	650-3132	SCREW, 6-32 x 3/8 IN.(1200 UNITS
	653-3000	FLAT WASHER AND ABOVE)
	653-3001	LOCK WASHER
22	445-9106	HANDLE, CHASSIS PULL
23	452-3009	RF SHIELD, BLANK
25	452-0284	PLATE, MOUNTING
26	650-3120	SCREW, 6-32 X 3/8
	653-3000	#6 FLAT WASHER
27	650-3120	SCREW, 6-32 X 3/8 (300 UNITS
	653-3000	#6 FLAT WASHER AND BELOW)
	653-3007	#6 NYLON WASHER
	650-3080	SCREW 6-32 X 1/4 PAN HD.(300 UNITS
	653-3000	#6 FLAT WASHER AND ABOVE)

24* LISTED BELOW ARE OPTION BOARDS

210-8222-A**	COLOR AND GRAPHICS BOARD
210-8225-A**	WINCHESTER CONTROLLER BOARD
210-8233**	GRAPHICS DISPLAY ADAPTER
210-8243/8343-A**	CHARACTER DISPLAY ADAPTER
210-8245-A**	LOCAL COMMUNICATIONS BOARD (DATA LINK)
210-8246-A**	LOCAL COMMUNICATIONS BOARD (CPU)
220-3281**	CABLE ASSY FOR LOCAL COMM. BOARDS
210-8248-A**	CP/M-80 EMULATOR BOARD
210-8242**	EXPANDED MEMORY BOARD 128K
210-8242-1**	EXPANDED MEMORY BOARD 256K
210-8242-2**	EXPANDED MEMORY BOARD 512K
210-8232-A**	REMOTE COMMUNICATIONS BOARD
210-8252-A**	X.21 REMOTE COMMUNICATION BOARD
210-8251**	MULTIPORT COMMUNICATIONS CONTROLLER

** DENOTES RSL ITEMS

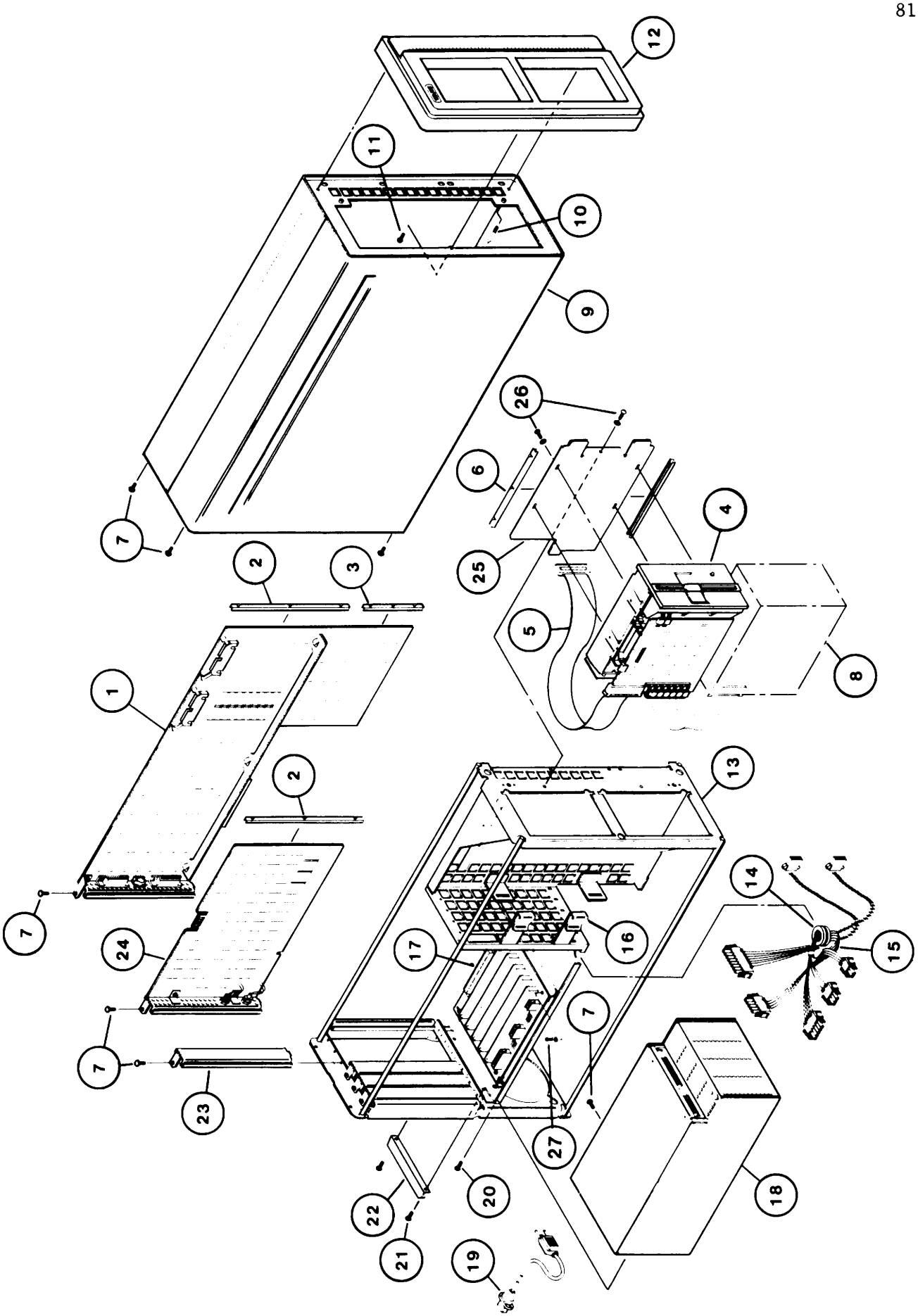


Figure 7-3 CPU Electronics Enclosure

CHAPTER 8

TROUBLESHOOTING

8.1 SCOPE

Effective troubleshooting is carried out from a system viewpoint. No procedure can list every potential problem or combination of problems for even a very simple device. Use the troubleshooting charts in this section as an aid in the systematic investigation, diagnosis, and repair of failures common to the Wang Professional Computer system.

The troubleshooting flowcharts on the following pages provide reference to common failures and solutions of error conditions common to the PC. Two troubleshooting flow charts are included in this chapter. These are:

- Low Profile Keyboard Troubleshooting Flowchart
- Electronic Unit/Monitor Troubleshooting Flowchart

LOW PROFILE KEYBOARD FAILURE

If the following Power-Up diagnostic message appears, use the flowchart below to determine the cause of the keyboard failure.

Power-Up Diagnostic Message:

*22 KEYBOARD DEFECTIVE
50 OR MISSING

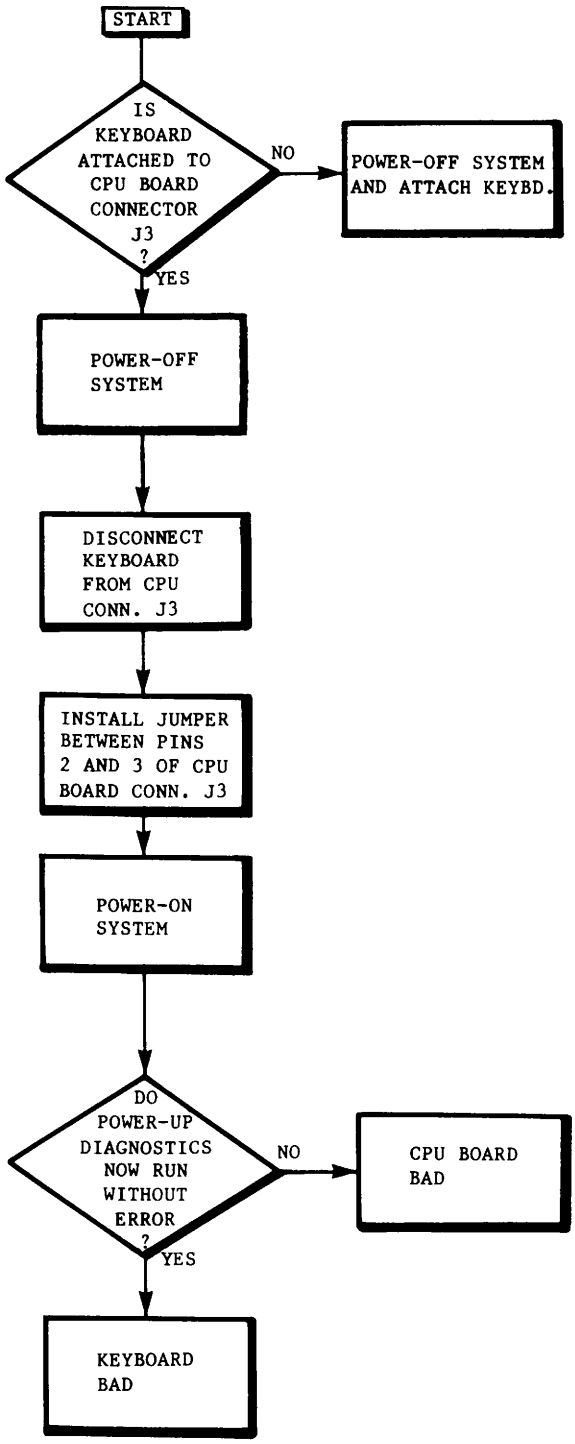


Figure 8-1. Low Profile Keyboard Troubleshooting Flowchart

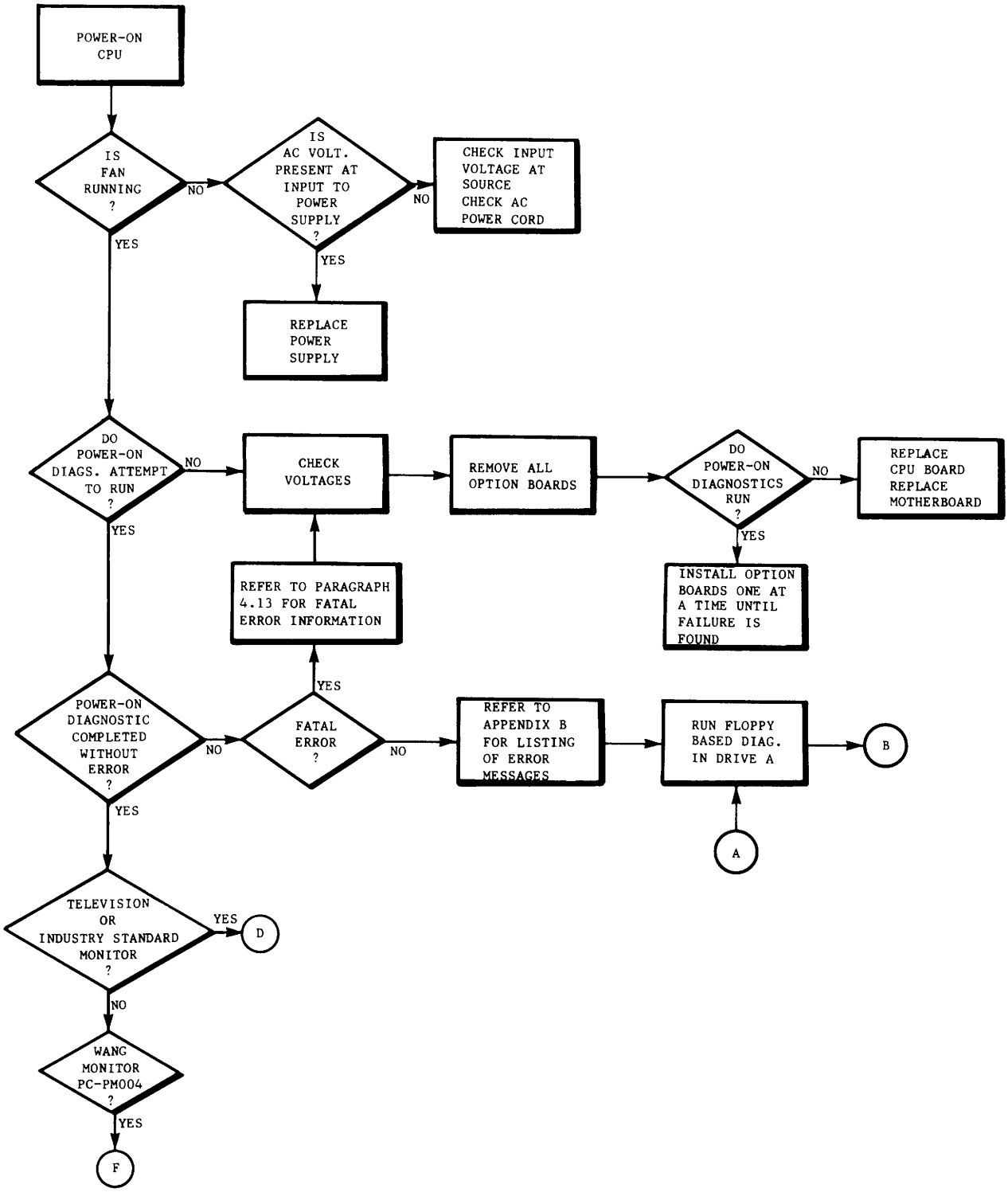


Figure 8-2. PC Troubleshooting Flow Chart (Sheet 1 of 5)

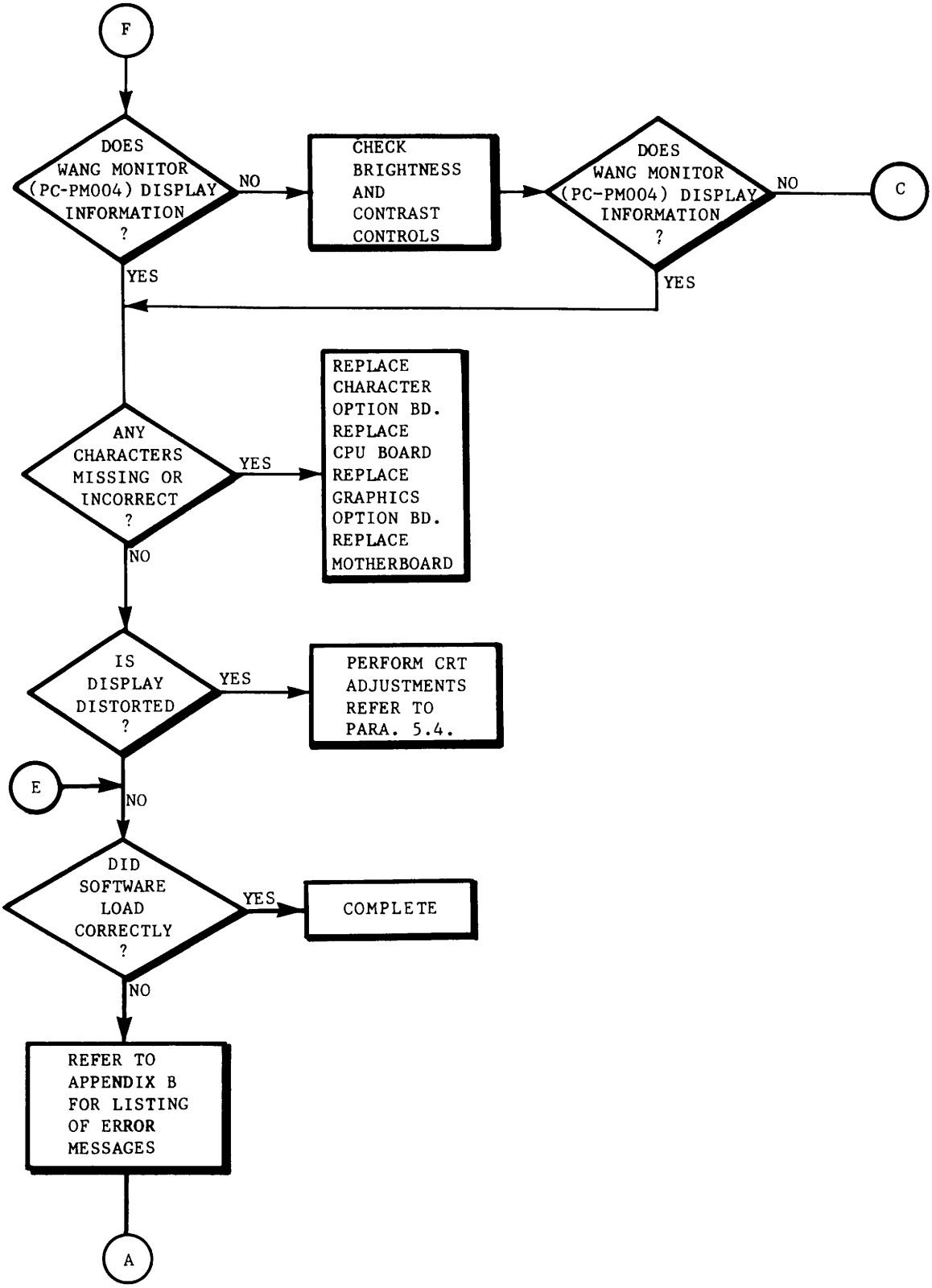


Figure 8-2. PC Troubleshooting Flow Chart (Sheet 2 of 5)

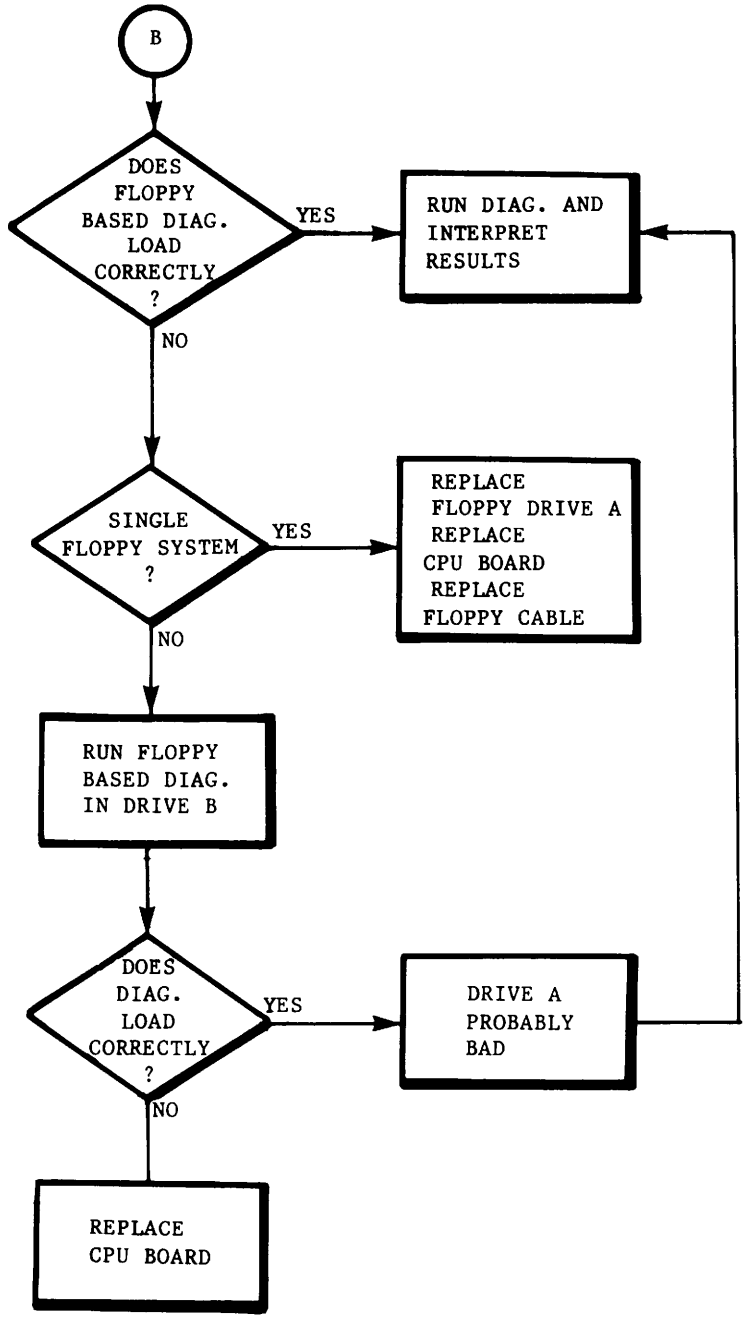


Figure 8-2. PC Troubleshooting Flow Chart (Sheet 3 of 5)

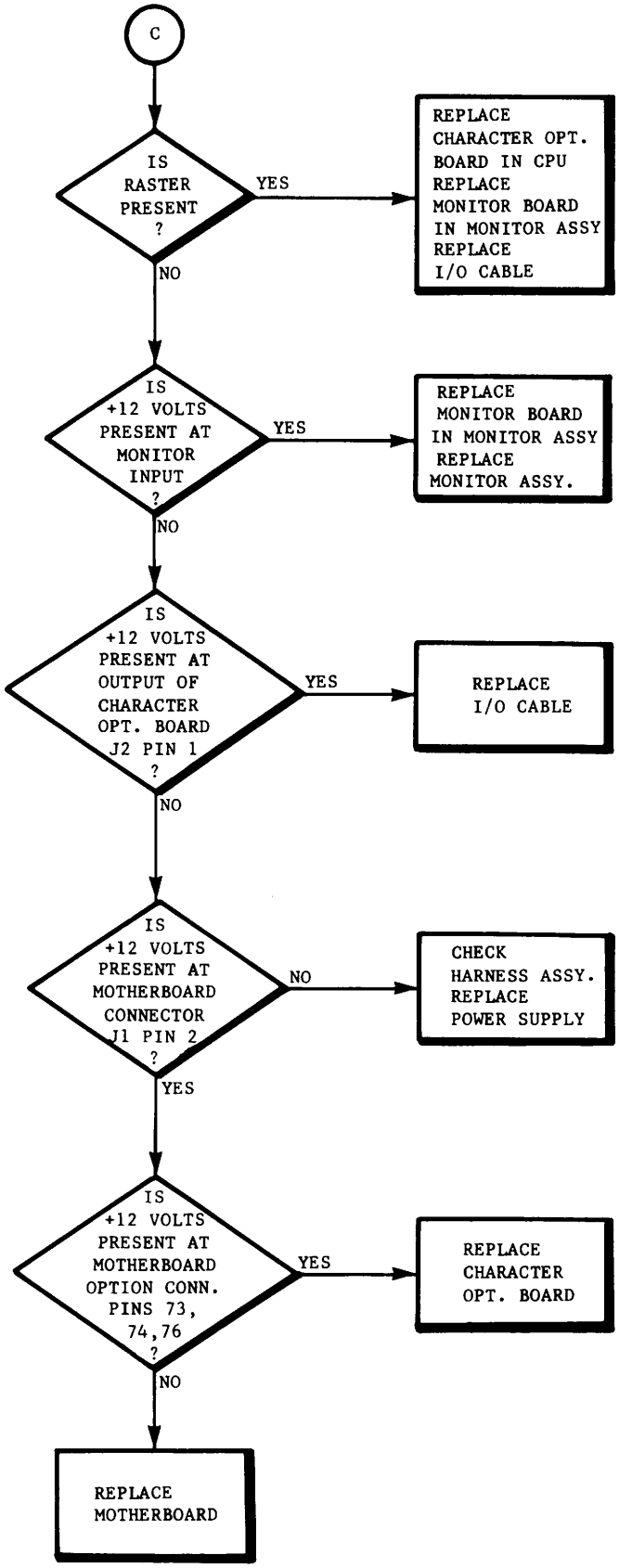


Figure 8-2. PC Troubleshooting Flow Chart (Sheet 4 of 5)

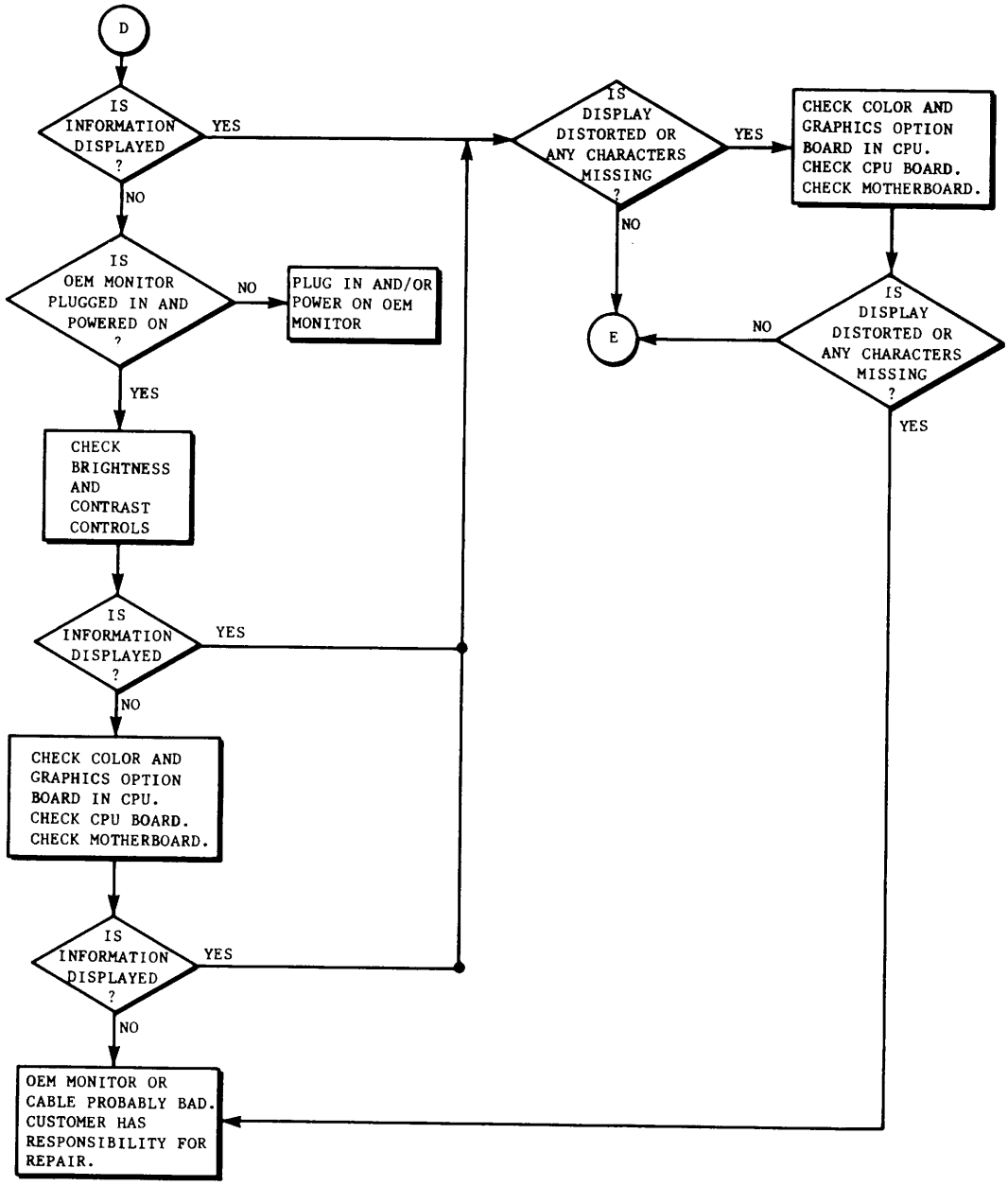


Figure 8-2 PC Troubleshooting Flow Chart (Sheet 5 of 5)

8101

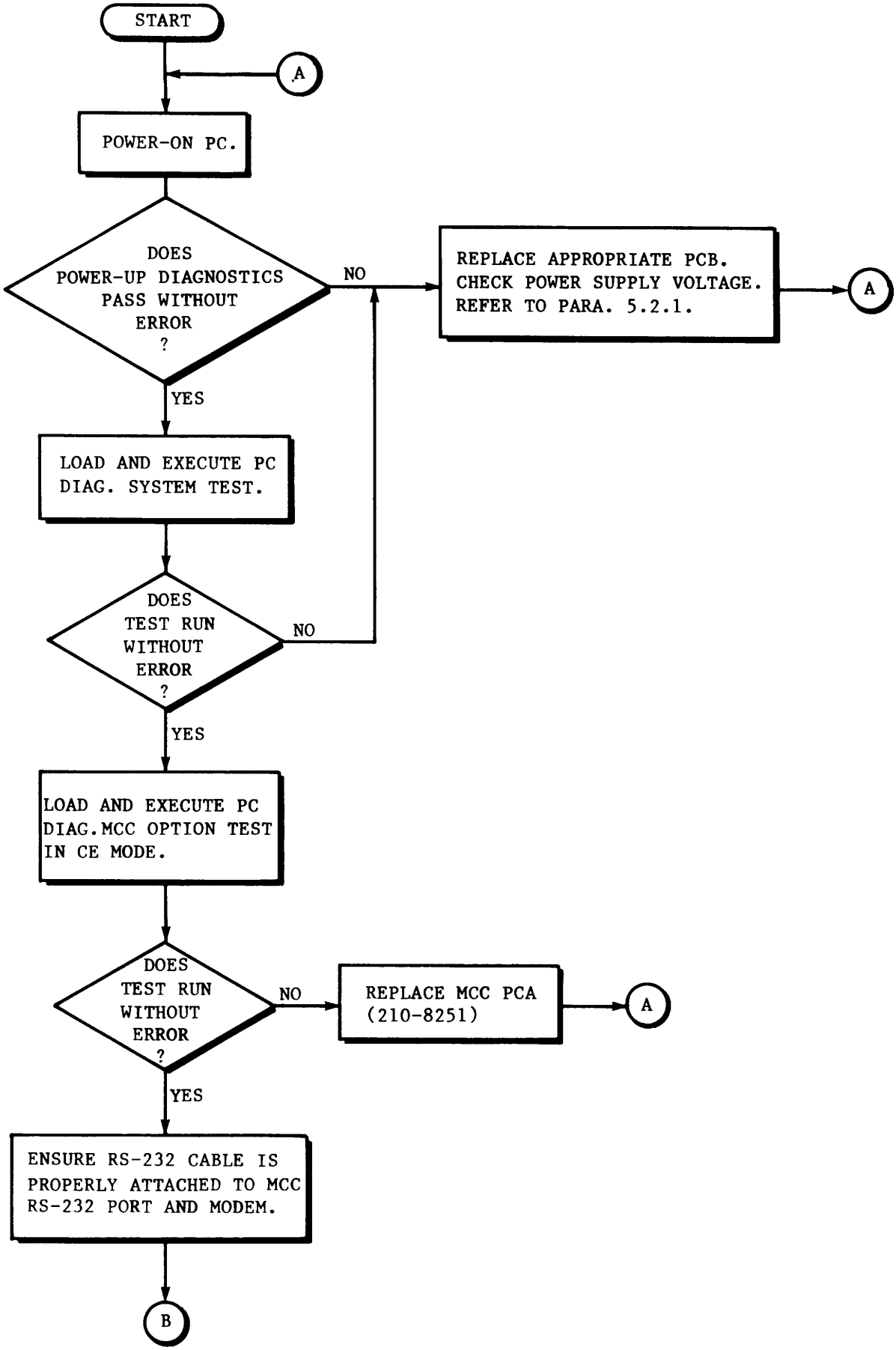


Figure 8-3. MCC Option Troubleshooting Flowchart (Sheet 1 of 2)

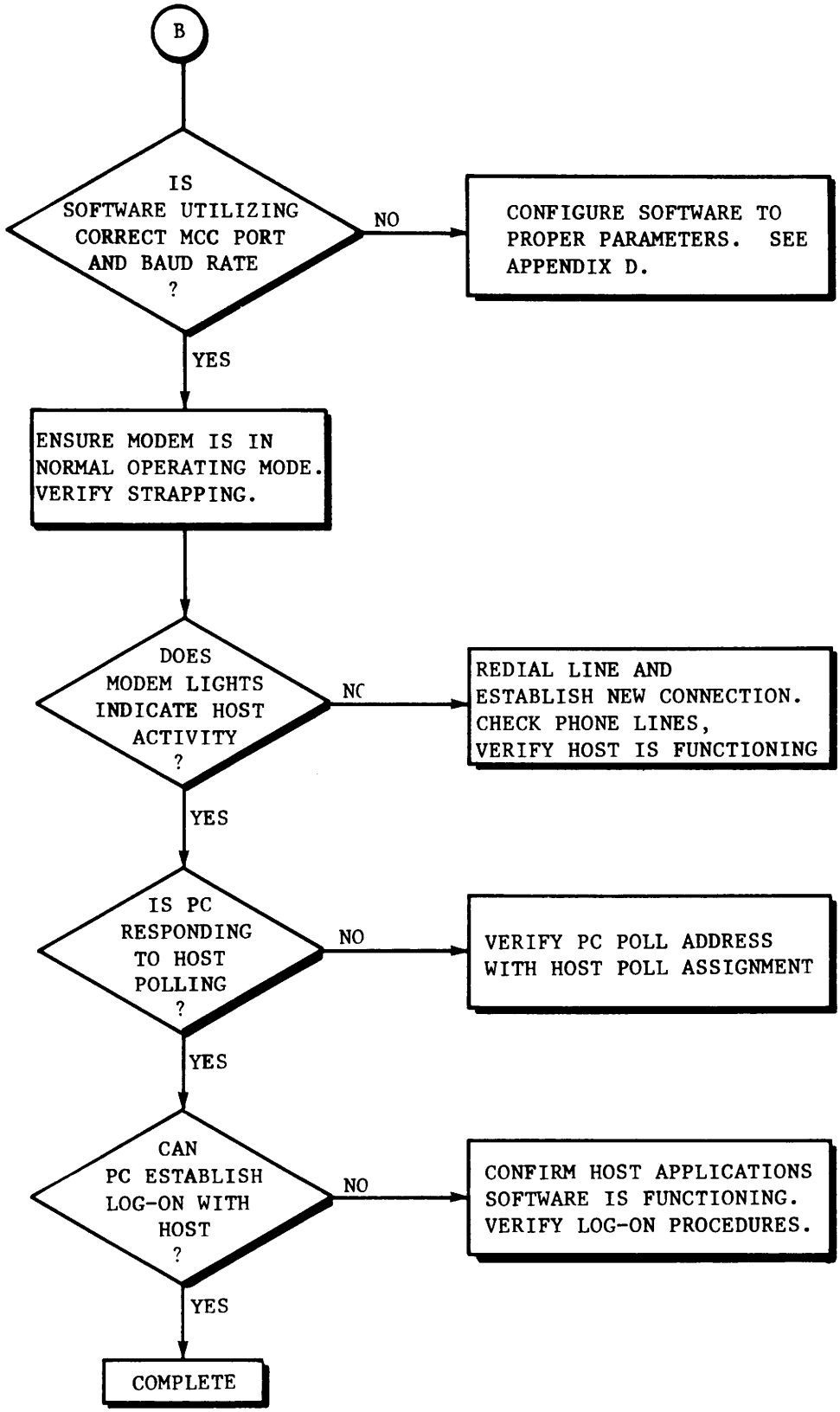


Figure 8-3. MCC Option Troubleshooting Flowchart (Sheet 2 of 2)

APPENDIX A

CABLE ASSEMBLIES

PART No.	DESCRIPTION
220-0105-4	Epson (PC-PM010) and DW-20 (PC-PM011) Printer I/O Cable
220-0305	Keyboard Cable Assembly
220-3238	Winchester "B" Cable
220-3239	System Floppy Cable (Drive A)
220-3240	2nd Optional Floppy Cable (Drive B)
220-3240	Winchester "A" Cable (Same as 2nd Floppy Cable)
220-3281	Cable Assembly Used With Local Communication Boards (Connects the two board system together)
220-0332	RS-232 Cable (12 foot length) between MCC Option and Modem.
220-0332	RS-232 Cable (25 foot length) between MCC Option and Modem.
220-0332	RS-232 Cable (50 foot length) between MCC Option and Modem.
220-0315	Pigtail Cable Only For 2200 Emulation (Connects between the CPU RS232 Async Port and the RS232 Cable)
270-3279	Main Harness Assembly Cable (Connects between Power Supply and Motherboard)
420-2019	AC Power Cord
421-0001	TTL Monitor I/O Cable

APPENDIX B

ERROR MESSAGES

The following error messages are start-up messages. The 2 digit number preceding each start-up message is an international translation code which domestic PC users can disregard. The start-up messages are listed in numerical order. An explanation follows each message.

WANG PROFESSIONAL COMPUTER REV 1.00

This is an informational message that indicates the system is performing the power-on diagnostics and that the system is preparing to start. The revision number (REV) displayed is the version of the System's EPROM.

01 WILL START FROM device

This is an informational message that indicates which start-up device the system intends to start from. The system runs a prioritized list of start-up devices until it finds the first operational start-up device from which it attempts to start. The prioritized list of devices are as follows:

- Drive A
- Drive B
- Winchester (Drive C)

When this message appears on the screen, the power-up diagnostics have successfully completed their tests.

02 STARTING FROM device

This is an informational message that is displayed when the system is ready to begin the final start-up sequence. There is a short pause before this message is displayed, then the system begins the final start-up sequence.

03 RE-DIRECT START

A prompt if re-direct is specified. This message appears after the operator enters the new device nomenclature during the Re-direct sequence.

04 RE-DIRECT CO

A prompt if re-direct is specified.

05 RE-DIRECT CI

A prompt if re-direct is specified.

*21 device IN SLOT ## DEFECTIVE
reason

This type of warning is displayed for each start-up device that the power-up diagnostic determines is defective. The defective device reasons are listed as messages 50-57 in this appendix.

*22 device DEFECTIVE
reason

This type of warning is displayed for each System Card device (eg. Drive B) that the power-on diagnostic determines is defective. The defective device reasons are listed as messages 50-57 in this appendix.

*23 ILLEGAL RE-DIRECT

Error if illegal specification. This message is displayed if the operator attempts to re-direct the boot to an invalid, non-installed, or defective device. Depressing the "RETURN" key will cause the system to re-check all boot devices for a functional device.

***40 NO AUTO-START DEVICE

This message indicates that a serious error was encountered during the start-up sequence. The error must be corrected before the system can proceed. Auto-start devices only include Drive A, Drive B, and the Winchester. This message occurs if all of the auto-start devices are defective or nonexistent. This message can be created if the system does not include a Winchester drive and/or all diskette drive doors are left open while the system attempts to start.

***41 START FAILED
device - reason

This message indicates that a serious error was encountered during the start-up sequence. The error must be corrected before the system can start. The reasons that appear in this type of message are listed as messages 70-73 in this appendix.

***42 INVALID INTERRUPT

This message indicates that a serious error was encountered during the start-up sequence. The condition must be corrected before the system can start.

***43 PARITY ERROR

This message indicates that a memory parity error was encountered during the power-up sequence. The condition must be corrected before the system can start.

***44 SYSTEM FILES MISSING

This operating system message indicates that the system can not proceed until you load a diskette that contains the system files in the current drive and restart the system.

***45 DISK READ ERROR

This operating system message is displayed if the system can not read the disk in the current drive.

***46 DEFECTIVE START DISK

This operating system message indicates that incorrect information is on the start-up disk. This condition can be created by using a formatted diskette that does not include a copy of the system files on it when the system start was attempted.

50 OR MISSING

A defective device reason which indicates that in certain cases a diskette drive or the Wang Keyboard may present the same symptoms as it would if the device was not included on the system.

51 MEMORY ERROR

A defective device reason that indicates the devices has a problem with its memory.

52 READ ERROR

A defective device reason that indicates a problem has occurred in transferring data between the device and the system.

53 WRITE ERROR

A defective device reason that indicates a problem has occurred in transferring data between the system and the device.

54 DMA ERROR

A defective device reason that indicates the system has a problem with the Direct Memory Access chip transferring data correctly.

55 STATUS ERROR

A defective device reason that indicates the system has a problem with some device or LSI chip that returned an incorrect or bad status.

56 LOOP BACK

A defective device reason that indicates there is a loopback connector attached.

57 SYSTEM CARD FAILURE

A defective device reason that indicates some device-related electronics on the system card has failed.

70 READ ERROR

A start failure reason that indicates a read failed on the particular device. This reason can occur if the disk is not formatted correctly or if there is defective data on the disk.

71 NO WANG START TRACK

A start failure reason that indicates the disk in the start-up drive does not have a valid Wang start-up track.

72 NOT READY

A start failure reason that indicates the start-up device was not ready to start. You can cause this message to appear if you forget to insert a diskette in Drive A or Drive B and have the door closed when you start the system or if the diskette is install incorrectly in the drive.

73 FAILURE

A start failure reason. This message is a catch-all phrase if no other code applies or the failure is strange.

91 LOOPING ON POWER-ON

An informational message that indicates the status of the power-on diagnostics. This message is displayed when SW1 (located on the 8221 CPU board) has been set to an all ON condition. The power-up diagnostic will run continuously until SW1 is switched to a different configuration.

The following error messages are listed alphabetically, each followed by an explanation. The explanation begins with the name of the program that displays the message. If the program is a system utility, the name is given first as it appears on the System Utilities menu, then as it is invoked from the DOS Command Processor.

Allocation Error for file [filename]

CHECK DISK (CHKDSK). The named file had an allocation unit allotted to it that did not exist (a unit number larger than the largest possible allocation number). CHECK DISK truncates the file at the last valid sector.

Attempted Write-Protect Violation

FORMAT. The diskette is write protected therefore, cannot be written to. To restart formatting, insert a new diskette and depress any key.

Bad Command or File Name

COMMAND.COM. The preceding command is not valid, internal DOS command, and the computer could not find a file called [Command-Name]. COM or [Command-Name]. EXE on the disk in the specified or default drive.

Can not load MSDOS.SYS, Please re-IPL

BIOS.SYS. The computer attempted a system start-up but could not load the operating system program MSDOS.SYS from the System disk. Make sure the disk is the default drive contains MSDOS.SYS. "Re-IPL" means to restart the system.

Data error reading drive (x) Abort, Retry, Ignore?

MSDOS.SYS. The computer has detected a data transmission error. The computer is waiting for you to make one of the following responses:

A (Abort). The computer terminates the program that requested the I/O operation.

R (Retry). The computer attempts the operation again.

I (Ignore). The computer attempts to continue the program as if the error has never occurred.

Usually, the logical order for these responses is Retry (R), I (Ignore), and A (Abort).

Directory error-file: (Filename)

CHECK DISK (CHKDSK). The file has no valid sectors allotted to it. Therefore, CHECK DISK deleted the file.

Disk error reading drive (x)
Abort, Retry, Ignore?_

MSDOS.SYS. A disk read error occurred. The computer retried the operation four (4) times. Refer to the "Data error reading drive (x)" message.

If disk read error occurs while the Debugger program is executing, only the first line of message appears.

Disk error writing drive (x)
Abort, Retry, Ignore?_

MSDOS.SYS. A disk write error occurred. The computer retried the operation four times. Refer to the "Data error reading drive (x)" message.

If disk write errors occur while the Debugger program (refer to the Wang PC Program Development Guide) is executing, only the first line of the message appears.

Disk unsuitable for system disk

FORMAT. FORMAT detected a defective track at a place where a system file was to be written. If you use the diskette at all, use it only for files other than the system files.

Diskette not initialized

CHECK DISK (CHKDSK). CHECK DISK could not find the root director or File Allocation Table on the disk. Format the disk again before using it. To save the data on the disk, you may be able to first copy the contents of a disk to an already-formatted disk.

Divide overflow

MSDOS.SYS. A program tried to divide by zero, or an error in the program's logic caused the computer to suspend execution of the program.

Duplicate file name or File not found

RENAME. You attempted to give a file a name already in the directory, or the file being renamed was not on the disk.

Error in EXE file

COMMAND.COM. The relocation data supplied by the Linker program (refer to the Wang PC Program Development Guide) contains an error.

Error while reading COMMAND. COM, please re-IPL

BIOS.SYS. The computer attempted a system startup but could not read the operating system program COMMAND.COM from disk into memory. If retrying with the same disk does not succeed, use another disk containing COMMAND.COM. "Re-IPL" means to restart the system.

File allocation table bad, drive (x)
Abort, Retry, Ignore?_

MSDOS.SYS. Refer to the "Data error reading drive (x)" message. If retrying does not succeed, you must format the disk again.

File cannot be copied onto itself

COMMAND.COM. The COPY utility cannot create an output file with the same name and on the same disk as the input file. Either give the output file a new name or put it on another disk.

File COMMAND.COM not found, please re-IPL

BIOS.SYS. The computer attempted a system startup but could not find the operating system file COMMAND.COM on the disk. Make sure the disk in the default drive contains COMMAND.COM. "Re-IPL" means to restart the system.

File creation error

COMMAND.COM. An attempt to add a file name to a directory failed. Use CHECK DISK to determine what condition caused the failure, e.g., the root directory being full.

File not found

COMMAND.COM. A file specified in a command was not found on the disk.

File size error for file (filename)

CHECK DISK (CHKDSK). The size allocated for the file differs from the size listed in its directory. The directory size has been adjusted to the actual size. (The amount of useful data may be less than the size shown because the last data block may not be used fully.)

Files cross-linked: (filename) and (filename)

Check Disk (CHKDSK). Two files share the same allocation unit. To correct the problem, you can edit, make copies of, or delete either or both files.

Format failure

FORMAT.FORMAT found a disk error. The diskette cannot be used, perhaps because it is not the proper type for the Wang PC.

Incompatible system size

SYSTEM TRANSFER (SYS). The transfer did not take place because the destination disk has a copy of the system files smaller than the one being copied. Use another disk or reformat this disk.

Insert disk with batch file and strike any key when ready

COMMAND.COM. The diskette with the batch file that was executing was removed. To resume execution, insert a diskette with the batch file in the correct drive and press any key.

Insert DOS disk in default drives and strike any key when ready

MSDOS.SYS and FORMAT. The default drive does not contain a disk with the system files. Therefore, DOS cannot reload the command processor and FORMAT cannot load the system files.

Insufficient disk space

COMMAND.COM. The disk does not have sufficient available space for the file being written. Use CHECK DISK to find the amount of available space.

Invalid COMMAND.COM. Insert DOS disk in default drive and strike any key when ready

MSDOS.SYS. The command processor cannot be reloaded because the copy of COMMAND.COM on the diskette is incorrect. Insert a correct system diskette and press any key.

Invalid date
Enter new date:_

DATE. You entered an invalid date or separator. The legal separators in a date are hyphens (-) and slashes (/).

Invalid drive specification

COMMAND.COM You entered an invalid drive designation in a command or in a parameter supplied with a command.

Invalid parameter

CHECK DISK (CHKDSK), FORMAT, and SYSTEM TRANSFER (SYS). You did not enter a valid drive designator followed by a colon.

Invalid time
Enter new time:_

TIME. You entered an invalid time or separator. The legal separator is the colon (:).

Missing file name

RENAME. You did not supply the second file name

No room for system on destination disk

SYSTEM TRANSFER (SYS). The system cannot be transferred because the reserved space needed for the system files does not exist on the disk. Reformat the disk or use another disk.

Not ready error reading drive (x)
Abort, Retry, Ignore?

MSDOS.SYS. Put a diskette in the drive.

Program too big to fit in memory

COMMAND.COM. The program cannot be loaded because there is not enough space available in memory.

Sector not found error reading drive (x)
Abort, Retry, Ignore?_

MSDOS.SYS. Refer to the "Data error reading drive (x)" message.

Sector not found error writing drive (x)
Abort, Retry, Ignore?_

MSDOS.SYS. Refer to the "Data error reading drive (x)" message.

Seek not found error reading drive (x)
Abort, Retry, Ignore?_

MSDOS.SYS. Refer to the "Data error reading drive (x)" message.

Seek not found error writing drive (x)
Abort, Retry, Ignore?_

MSDOS.SYS. Refer to the "Data error reading drive (x)" message.

System Error: Parity

BIOS.SYS. A hardware malfunction has occurred in memory.

Terminate batch job (Y/N)?

MSDOS.SYS. This message is displayed if you press CANCEL during the execution of a batch file. Press Y to terminate the execution of the batch file. Pressing N only terminates the command executing when you pressed CANCEL. Execution of the batch file then continues with the next command.

Track 0 bad-disk unusable

FORMAT. The startup record, File Allocation Table, and root directory must be written to Track 0.

Write error

FORMAT. An error occurred while FORMAT was writing the startup record or the system files.

Write fault error writing drive (x)
Abort, Retry, Ignore?_

MSDOS.SYS. Refer to the "Data error reading drive (x)" message.

Write protect error writing drive (x)
Abort, Retry, Ignore?_

MSDOS.SYS. Refer to the "Data error reading drive (x)" message.

NNNNNNNNNNN bytes of disk space freed

CHECK DISK (CHKDSK). Disk space shown as allocated was not actually allocated and has been freed.

APPENDIX C

MNEMONIC CODES AND DEFINITIONS

The Mnemonic code listing contains the Input/Output (I/O) signals. The mnemonic codes are listed in numerical order followed alphabetically, each followed by a definition. The definition contains the mnemonic description and the functions that are performed or controlled. A dash (-) proceding the mnemonic code denotes a low-active signal.

SIGNAL	DESCRIPTION
4CLK	A 4 MHz clock with a 250-ns period and a 50% duty cycle that is available for use by I/O devices including auxiliary processors.
A0	Low-Order Address Line. A0 is active to access the low-order byte (D0-7) of the 16-bit word addressed by A1-19. In order to access only the high-order byte, A0 is high and -BHE is active. Both A0 and -BHE are active during full word access.
A1-19	System Address Bus. Generated by a processor or the DMA controller, A1-19 identify words of memory, memory mapped device registers, or I/O ports. A1-19 implement a 512K-word address space. A1 is the low-order bit.
AIOWC-	Advanced I/O Write Command. The processor or DMA controller asserts -AIOWC to write data from the system data bus (D0-15) to an I/O mapped device.
ALE	Address Latch Enable. Asserted by the 8288 Bus Controller chip. ALE provides a falling edge that can be used to latch an address from the system address bus during processor-generated bus cycles.
AMWC-	Advanced Memory Write Command. The processor or DMA controller issues -AMWC to write data from the system data bus to memory (or a memory mapped register).
BHE-	Byte High Enable. -BHE is active to access the high-order byte (D8-15) of the 16-bit word addressed by A1-19. To instead access only the low-order byte, -BHE is high and A0 is active. Both A0 and -BHE are active during full word access.
CLK	System Clock. Derived from the 8284A Clock Generator chip, the CLK line runs at 8 MHz with a 125-ns period and approximately a 33% duty cycle.
CTS-	Clear to Send. Must be low in order for transmitter to operate.

APPENDIX C (Cont'd)

SIGNAL	DESCRIPTION
D0-15	Data Bus. D0 is the low-order bit. D0-7 comprise the low-order byte, which always occupies an even memory address.
DACK0-3-	DMA Acknowledge lines. -DACKn is the acknowledge for DMA request signal DREQn (n = 1, 2, or 3). DACK0 indicates that the current bus cycle is a dynamic RAM refresh cycle.
DCD-	Data Carrier Detect. Must be low for receiver to operate. DCD changing state causes an interrupt. Its complement is Status Register bit 6.
DEN	Data Enable. Asserted by the 8288 Bus Controller chip, DEN provides a pulse that can be used to enable system data bus transceivers during processor-generated bus cycles.
DREQ1-3-	DMA Request Lines. Held low by I/O device options to request DMA service. -DREQn requests service on DMA channel n (n = 1, 2, or 3). It can be released when the corresponding -DACKn is asserted.
DSR-	Data Set Ready. General purpose input. Its complement is Status Register bit 7.
DT/R	Data Transmit/Receive. Asserted by the 8288 Bus Controller chip to indicate the direction of data flow during a processor generated bus cycle. DT/R stays high during memory write or I/O write cycles and goes low during part of memory read or I/O read cycles.
DTR-	Data Terminal Ready. General purpose output is the complement of Command Register bit 1.
GND	Ground Lines.
HACK	DMA Hold Acknowledge. Indicates that a DMA cycle is in progress and the DMA controller is the system bus master.
I/O ERROR-	I/O Device Error. Asserted by parity (or other error) checking circuits to indicate an error and generate a nonmaskable interrupt (NMI).
IORC-	I/O Read Command. Processor or DMA controller issues -IORC to read data from an I/O device via the data bus.

APPENDIX C (Cont'd)

SIGNAL	DESCRIPTION
IRQ2-7-	Interrupt Request Lines. Used to request prioritized interrupts at levels 2-7 by asserting one of -IRQ2-7 respectively, and holding it low until the 8086 acknowledges the request. -IRQ2 has highest priority when fixed priority is used.
MRDC-	Memory Read Command. Processor or DMA Controller chip asserts -MRDC to read data from system memory or a memory mapped I/O device register via the system data bus.
RDY	I/O Device Ready. Asserted by memory or I/O option devices to add wait states that extend the current bus cycle by one or more CLK (or 4CLK) cycles.
RESET-	System Reset. Synchronized with the falling edge of CLK, -RESET is used to initialize system logic during the power-on sequence or after a power outage.
RTS-	Request to Send. General purpose output is the complement of Command Register bit 5.
RxD	Receive Data. Serial data input to receiver. "Mark" is high and "space" is low.
SAD-	Slot Address Decode. When active, indicates that system address bus lines A13-15 are cleared to zero while A12 is set to one. This provides I/O option boards with partial I/O port decoding. Since -SAD will be active even when a memory address in the format "x1xx" is on the bus, it must be further qualified by -IORC or -AIOWC to read or write an I/O port.
SID0-3	Slot Identification Pins. Hardwired to 5v pull-up or ground, SID lines present a 4-bit code that uniquely identifies each expansion slot to the circuit board installed in that slot.
T/C	Terminal Count. Asserted by DMA Controller chip to indicate that it has exhausted its word count for DMA channel use.
TxD	Transmit Data. Serial data output line from transmitter. Value of one or "mark" is high and value of zero or "space" is low. Held in mark condition when transmitter is disabled.
WTR	Wolftrap. From the power supply, when active indicates that dc power is applied.

APPENDIX D

PC SNA 3276 EMULATION

D.1 SCOPE

Appendix D contains information, screen loads, keyboard layout, and operator information required for the use of the Multiport Communications Option card (PC-PM042). The intent of this Appendix is to familiarize the CE with SNA 3276 Emulation using the Wang Professional Computer. This Appendix should be used as a reference to the SNA 3276 Emulator User Guide number 700-8319.

D.2 Loading SNA 3276 Software

In order to run 3276 Emulation, the Wang software diskette (PC-SS063) must be loaded into the PC system. Perform the following:

1. Power-on the PC using the System Diskette.

2. When the system comes up, proceed to the Main System Menu and select the Communications Menu. See Figure D-1 Communications Menu.

3. Insert the SNA 3276 Emulation Diskette into the disk drive. Once the diskette is inserted, select SNA 3270 Terminal Emulation from the menu. The program will then be loaded into the PC's memory. If the SNA 3270 Terminal Emulation selection is not present the Communications Menu must be modified to include this selection. Refer to the Wang Professional Computer SNA 3276 Emulator User Guide.

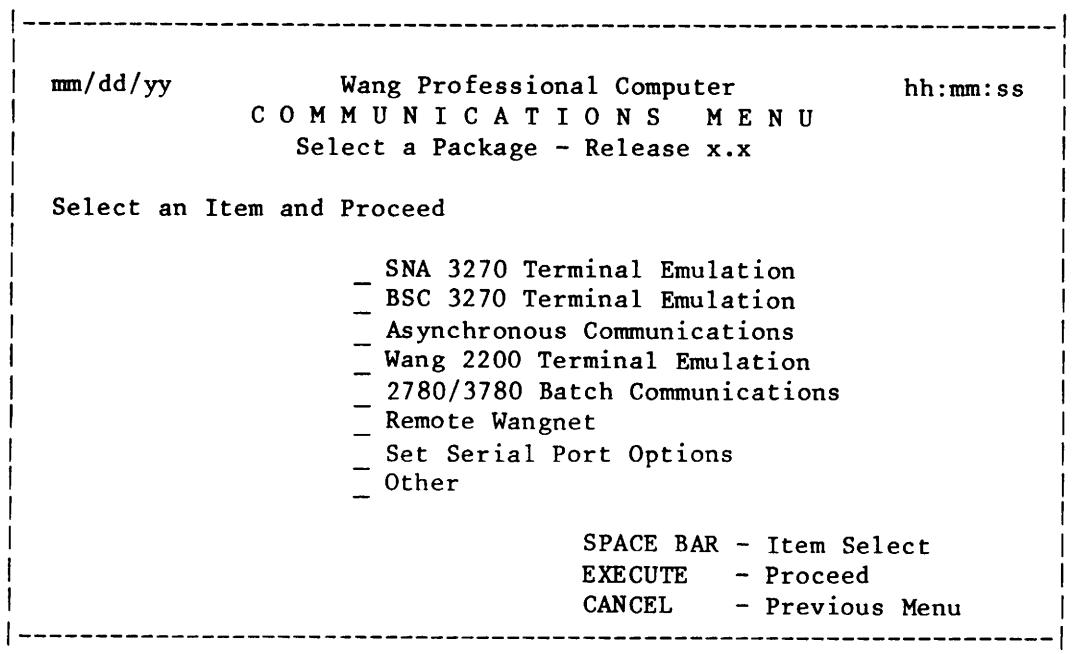


Figure D-1. Communications Menu

4. Position the acceptance block next to the this selection and depress "EXECUTE". The message "Loading Configuration Program: Please Wait" will be displayed in the center of the screen. After this message appears, the Select a Configuration Menu will be displayed. A sample of this menu is shown in Figure D-2.

```
Wang Professional Computer
3270 Terminal Emulation (version x.x)
Select a Configuration


Make a Selection and Press EXECUTE

__ Create a New Configuration

__ DEFAULTS

                          EXECUTE - Proceed
                          CANCEL  - Previous Menu
```

Figure D-2. The Select a Configuration Menu

This menu allows you to either select a configuration already created or to create a new configuration. Configurations previously created will be shown on the menu. To create a new configuration perform the following:

Select Create a New Configuration by positioning the acceptance block next to the entry and depress EXECUTE. The Create a New Configuration Menu will be displayed as shown in Figure D-3.

```
Wang Professional Computer
3270 Terminal Emulation (version x.x)
SNA 3270 Configuration

Configuration Name:_____________________________

Synchronous Communications Port  1  in Slot  0
SDLC Station Address  C1
Switched Line (Yes/No):
Duplex:      * Half   Full
NRZI   (Yes/No):  N
RTS Delay      * OFF     ON

DSC Printer       * Off      On       LU Number
SCS Printer       * Off      On       LU Number

                          EXECUTE - Proceed
                          CANCEL  - Previous Menu
```

Figure D-3. The SNA 3270 Configuration Menu

The SNA 3270 Configuration Menu data fields are defined as follows:

Configuration Name - The Configuration name is a text string that identifies the host connection to the user. This name maps to a file that contains the configuration parameters.

Synchronous Communications Port/Slot - The port number is the designation of the connector that connects the communications controller (MCC PCA Port) to the communications link. The slot number is the actual slot number the MCC board is installed in. The default values are Port 1 Slot 0.

SDLC Station Address - The SDLC station address is the address that identifies the PC to the host. The default address is C1. This is a host specified parameter. If the default address is not used, the station address must be obtained from the host system administrator.

Switched Line - This parameter is for a dial-up (Switched) line. When a null modem or lease line is used the parameter must be a N (No). When Switched line is Y (Yes) a field is displayed to the right on the same line for XID entry. The XID entry is an eight character hexadecimal number that identifies the dial-up line to the host.

Duplex - The Duplex parameter is a host specified transmission line characteristic. This must be compatible with the host system and is obtained from the host system administrator.

NRZI - NRZI (Non Return to Zero Inverted) is an encoding technique where a binary one (1) is represented by a no transition and a binary zero (0) is represented by a transition. This field is host specified and is obtained from the host system administrator.

RTS DELAY - This parameter set the Request to Send bit (bit 4) of the communications options field to 0 for OFF or to 1 for ON. This field is host specified and is obtained from the host system administrator.

LU/DSC Printer - When the DSC (Data Stream Compatibility) printer is ON, the LU number must be specified. This field is host specified and is obtained from the host system administrator.

LU/SCS Printer - When the SCS (SNA Character String) printer is ON, the LU number must be specified. This field is host specified and is obtained from the host system administrator.

Ensure that all the fields are properly defined. Consult the host system administrator for all fields that are Host specified to ensure compatibility for SNA communications.

Once all the fields are defined depress EXECUTE to display the Run, Modify or Delete menu. This menu is shown in Figure D-4. This menu allows you to Run the SNA emulation, modify the configurations or delete a configuration.

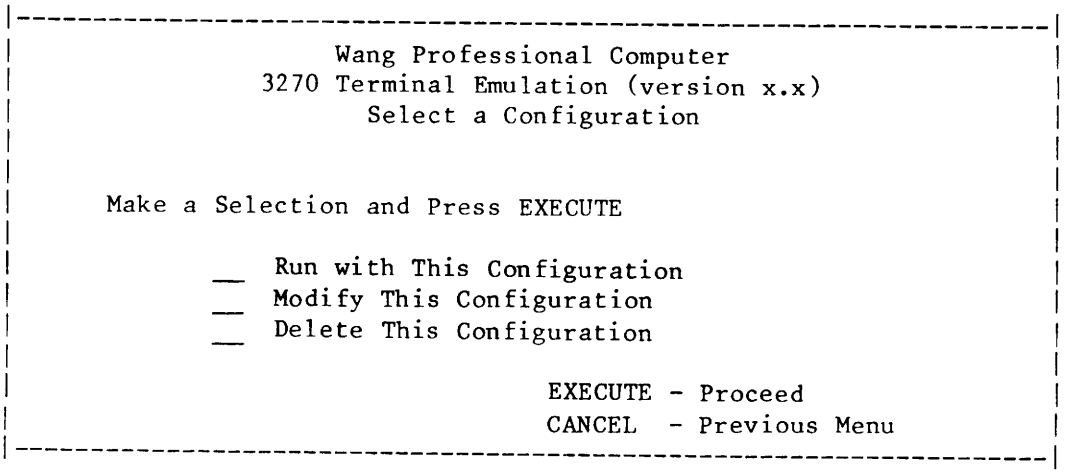


Figure D-4. The Run, Modify or Delete Menu

When the Run with This Configuration is selected, the screen is cleared and the message "Loading 3270 Emulator with '_____' Configuration" appears in the center of the screen. The configuration name selected appears in the blank space. After this message disappears from the screen, a 3270 Display System Emulator Title screen appears momentarily with the following message displayed on the OIA Status line. (The OIA Status Line is explained in paragraph D.4.)

READY INACTIVE COMM __ (22 or 33)

At this point, the Wang PC keyboard appears as a 3276 Display station to an IBM host. The PC is inhibited from normal operations/applications. The 3276 keyboard emulation is provided in paragraph D.3.

D.3 KEYBOARD 3276 EMULATION

The Wang PC keyboard supports 3276 Emulation keys by using either one or two keystrokes. The following table cross-references the PC keyboard key(s) to the 3276 Emulation Keyboard key. The SHIFT/xxxx notation denotes the SHIFT key must be depressed with the assigned key.

3276 Emulation Key	PC Keyboard Key(s)
ATTN (Attention)	GL (Glossary)
ALT CURSOR (Alternate Cursor)	PREV
CLEAR	SHIFT/COMMAND
CURSOR SEL (Cursor Select)	NEXT
DEV CNCL (Device Cancel	SHIFT/UP-DOWN ARROW
DUP (Duplicate)	SHIFT/GO TO
ERASE END OF FIELD	ERASE
ERASE INPUT	SHIFT/ERASE
FIELD MARK	SHIFT/PF31
INDENT	SHIFT/PRINT

3276 Emulation Key	PC Keyboard Key(s)
PA1	SHIFT/SRCH
PA2	SHIFT/REPLC
PF1	INDENT
PF2	PAGE
PF3	CENTER
PF4	DEC TAB
PF5	FORMAT
PF6	MERGE
PF7	NOTE
PF8	STOP
PF9	SRCH
PF10	REPLC
PF11	COPY
PF12	MOVE
PF13	COMMAND
PF14	UP/DOWN ARROW
PF15	BLANK
PF16	GO TO PAGE
PF17	SHIFT/INDENT
PF18	SHIFT/PAGE
PF19	SHIFT/CENTER
PF20	SHIFT/DEC TAB
PF21	SHIFT/FORMAT
PF22	SHIFT/MERGE
PF23	SHIFT/NOTE
PF24	SHIFT/STOP
PRINT	PRINT
RESET	CANCEL
NEW LINE	RETURN
BACK TAB	BACK TAB
TAB	TAB
LOCK	LOCK
SHIFT	SHIFT
BACK SPACE	BACK SPACE
TEST	SHIFT/GL
DEV CNCL	PF30
ENTER	EXEC
INSERT	INSERT
DELETE	DELETE
CUR BLINK	SHIFT/PREV
CLICK	SHIFT/NEXT
NORTH	UP ARROW
SOUTH	DOWN ARROW
WEST	LEFT ARROW
EAST	RIGHT ARROW
HOME	HOME
DOUBLE LEFT	SHIFT/LEFT ARROW
DOUBLE RIGHT	SHIFT/RIGHT ARROW

A complete description of the Key Functions is contained in the SNA 3276 Emulator User Guide.

D.3.1 Help Key

The HELP Key on the Low-Profile Keyboard can be used whenever an operator error or problem occurs. To use the Help Key, position the acceptance block (by depressing the Space Bar) next to option to be selected. Depress the Help key to display the Help Screen. This screen contains information pertainent to the option selected. To exit from the Help Screen depress CANCEL and the system will return to the previous sceen.

D.4 OPERATOR INFORMATION AREA

The Operator Information Area (OIA) displays 3276 session status information. The OIA occupies the bottom line (line 25) on the display screen. This display is always present during emulation and can not be turned off. The OIA contains six parts which are:

- o Connection Status (Columns 1-5, 11-16)
- o Session Ownership (Columns 21-28)
- o Input Inhibited Conditions (Columns 62-74)
- o Implementation-Specific Area (Columns 40-60)
- o Session Status (Columns 30-40)
- o User Aids (Columns 7, 15-20)

Each area of the OIA line is explained in the preceding text.

CONNECTION STATUS

Columns 1-5	READY	This indicator indicates that the emulator is ready.
Columns 11-16	ONLINE	This Indicator is displayed along with the READY denoting the terminal is on-line.

SESSION OWERSHIP

Columns 21-28	UNOWNED	This indicates that the session is unowned. The operator must depress the System Request Key (for lease line) or dial the host number to Log-On.
	LOGON	This prompt indicates that the session owner is the system operator. A Log-on is expected.
	(appl name)	This indicates that the session owner is the operator's application program. The first eight characters of the application name are displayed.
	TEST	This indicates the display station is in test mode.

INPUT INHIBIT CONDITIONS

Columns 62-74	PLEASE WAIT	This indicates that time is required to complete a function.
	LOCKED	This indicates that the host application has disabled the keyboard. Press RESET to restore keyboard operation.
	BUSY	This indicates that the host is BUSY and did not accept the request. Press RESET and retry.
	WHAT ?	This indicates an unavailable function has been requested. Press RESET and retry.

IMPLEMENTATION-SPECIFIC AREA

Columns 40-60		This area can be used for any display or query operation needed during 3276 Emulation.

SESSION STATUS

Columns 30-40	INACTIVE	This Indicates the LU is not activated.
	ACTIVE	This indicates that the LU has been activated successfully.
	IN SESSION	This indicates the session has been established.
	DATA FLOW	This indicates that the session data flow is enabled.

USER AIDS

Column 7	H	This indicates that the SNA Emulation is operating in the HELP file.
Columns 15-20	_(Up Arrow)	This indicates that the SNA Emulation is in the Insert Mode.

APPENDIX E

3278 EMULATION

E.1 INTRODUCTION

The Wang 3278 Emulation board PC-PM048 allows the Wang PC to emulate as an IBM 3278 Display station attached to an existing IBM Network Host. The 3278 Emulation board is a single board option that is installed in the PC and is intended for use in a single-user, single-task environment. The 3278 Emulation terminal may be attached to one of the following control units:

- o IBM 3274 Control Unit
- o IBM 3276 Display Station/Control Unit

The 3274 Control Unit connects devices like the 3278 Display Station to an IBM host or a Telecommunications Unit (TCU) such as the 3705. The Emulator connection may be remote, using leased or dial-up lines, or direct via a local channel.

The 3276 Display Station/Control Unit connects terminals and printers to an IBM host via a TCU. This connection is remote using leased or dial-up lines.

E.1.1 APPLICABLE DOCUMENTATION

The documentation listed below is 3278 Emulation Board user documentation. This document can be ordered by writing to the following address.

700-8618 Wang 3278 Terminal Emulation User Manual

Domestic and Canadian field personnel can order user documentation by submitting a withdrawal request to the following address:

WANG LABORATORIES INC.
Information Resources Management M/S 5526
51 Middlesex Street
No. Chelmsford, MA 01863

International field personnel can order user documentation by submitting a withdrawal request to the following address:

WANG LABORATORIES INC.
International Documentation Coordinator
M/S 1151
1 Industrial Avenue
Lowell, MA 01851

E.1.2 Software Requirements

The software required to operate the 3278 Emulation board is:

- Version 1.1 or higher of Wang PC Operating System
- 3278 Interface Software package (PC-SS065)

E.1.3 System Description

The 3278 Emulation system hardware required to operate the Wang PC as an emulated 3278 terminal is listed below.

- Wang PC (5-slot or Expanded Chassis)
- 128K Memory (Located on CPU/System Board)
- One Diskette Drive
- 3278 Interface Card (PC-PM048)
- Character Display Adapter Board (PC-PM001)
- RG62A Coaxial Cable With BNC Connetors at Each End (5000 feet maximum length)
- A 3274 or 3276 with Integral Category A Interface (User Supplied)

When the Professional Computer is attached to a control unit via the 3278 Emulator board, the emulator board provides protocol compatibility with 3278 Model 2, 3, or 4 terminals. This option enhances the Professional Computer allowing it to access host applications and host subsystems such as the IBM Information Management System (IMS), the Customer Information Control System (CICS), and the Time Sharing Option (TSO).

An independent processor on-board the 3278 Emulator Board handles coax protocol requirements. In addition, the emulator board contains a memory buffer that can maintain a display screen image at all times whether a 3278 emulation task or a PC function is being performed.

E.1.4 System Configurations

The 3278 Emulation Board is a single-board option that can be used with the Professional Computer (PC) and the Wang PIC image processing system (PIC). The PC/PIC with the 3278 Emulator board installed is dependant to 3278 emulation ONLY when the 3278 Emulation software is running. When the 3278 Emulation software is not running, any PC option/configuration may be used.

One of two configurations can be used; Remote or Local. Local configuration consist of the PC with the 3278 Emulation PCB installed attached to an 3274 Control Unit. See figure E-1 for local configuration.

Remote configuration consists of the PC with the 3278 Emulation PCB installed attached to an 3274 Control Unit or an 3276 Display Station/Control Unit. The 3274 or 3276 is connected to the host via modems and either lease lines or voice-grade lines. Refer to figure E-2 for Remote Configuration.

E.1.5 System Specifications

Single Board Option

Cable Length	Up to 5000 feet (1524 meters)

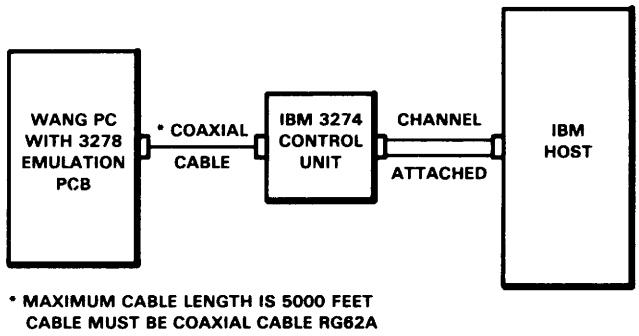


Figure E-1. 3278 Local Configuration

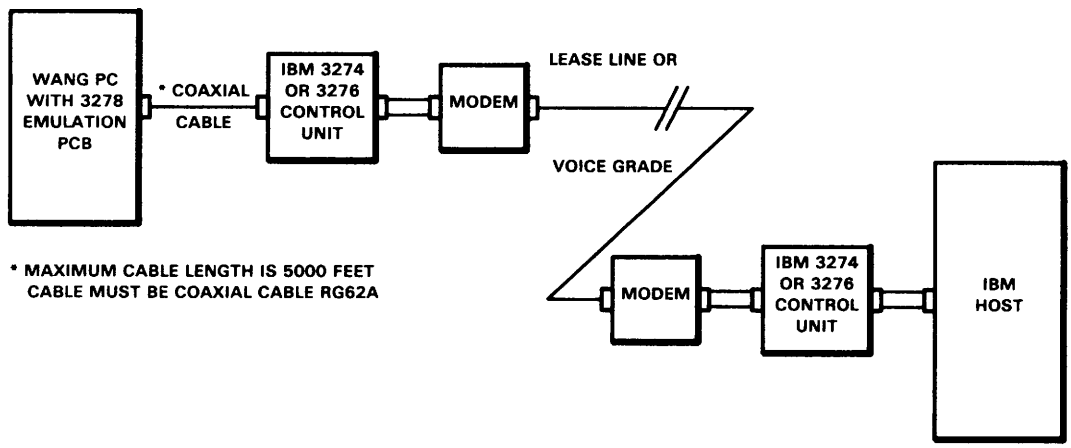


Figure E-2. 3278 Remote Configuration

E.2 3278 EMULATION INDICATORS and CONTROLS

The PC 3278 Emulation supports the standard 3278 terminal function on the Wang PC Keyboard. Some PC Keyboard keys and combinations of PC keyboard keys perform certain 3278 Emulation functions. These functions are discussed in paragraph E.2.1.

The 3278 Emulation also provides the Operator Information Area Status line (OIA) which occupies the last line of the monitor screen. Two status line modes are provided; Text Mode and Symbol Mode. The OIA Status line is discussed in paragraph E.2.2.

E.2.1 3278 Keyboard Emulation

Once the 3278 Emulation software is loaded into the PC system and 3278 Emulation is selected, the Wang PC keyboard supports 3278 Emulation keys by using either one or two keystrokes. The following table cross-references the PC keyboard keys to the 3278 Emulation Keyboard keys. The SHIFT/xxxx notation denotes the SHIFT key must be pressed with the assigned key. A Function strip is supplied with the software diskette that identifies the PF Key functions.

Table E-1. 3278 Emulation Keyboard Keys

3278 Emulation Key	Wang PC Keyboard Key(s)	Action
ALT CURSOR (Alternate Cursor)	PREV	Changes cursor display from rectangular to underlined and vice-versa
ATTN (Attention)	GL (Glossary)	Request Communication with the host operating system
BACK SPACE	BACK SPACE	Moves cursor to a previous input field or the beginning of the current input field
BACK TAB	BACK TAB	Moves cursor to the first position of a current or previous field, or to the top of the screen
CLEAR	SHIFT/COMMAND	Clears display screen, initializes all input fields

Table E-1. 3278 Emulation Keyboard Keys (Cont'd)

3278 Emulation Key	Wang PC Keyboard Key(s)	Action
CLICK	SHIFT/NEXT	Enables/disables keyboard clicking
CURSR BLINK	SHIFT/PREV	Enables/disables cursor blinking
CURSR SEL (Cursor Select)	NEXT	Perform selector-light-pen detection function on selected fields
DELETE	DELETE	Deletes character indicated by the cursor in an input field
DEV CNCL (device cancel)	SHIFT/UP-DOWN ARROW	Cancels local printing operation in progress
DOUBLE LEFT	SHIFT/LEFT ARROW	Moves cursor two spaces left
DOUBLE RIGHT	SHIFT/RIGHT ARROW	Moves cursor two spaces right
DUP (Duplicate)	SHIFT/GO TO	Fills input field with asterisk (*) characters
EAST	RIGHT ARROW	Moves cursor one position right
ENTER	EXEC	Transfers screen data to host for processing
ERASE TO END OF FIELD	ERASE	Erases all characters from the cursor to the end of the input field in which the cursor rests
ERASE INPUT	SHIFT/ERASE	Erases all characters in all input fields
FIELD MARK	SHIFT/PF31	Inserts a semi-colon in an input field as an end-of-field identifier
HOME	HOME	Moves cursor to the first position of the first input field at top left of the screen
INDENT	SHIFT/PRINT	Causes entry into Print ID Mode, assigns a printer for local copy purposes
INSERT	INSERT	Enables character insertion mode
LOCK	LOCK	Allows only uppercase character entry

Table E-1. 3278 Emulation Keyboard Keys (Cont'd)

3278 Emulation Key	Wang PC Keyboard Key(s)	Action
NEW LINE	RETURN	Moves cursor to first position of first field in the next line
NORTH	UP ARROW	Moves cursor up one line
PA1	SHIFT/SRCH	Request access to application programs
PA2	SHIFT/REPLC	Request access to application programs
PA3	SHIFT/COPY	Request access to application programs
PF1-PF16	ALL FUNCTION KEYS UNSHIFTED	Request host application processing
PF17-PF24	SHIFT/INDENT, PAGE, CENTER, DEC TAB, FORMAT, MERGE, NOTE, STOP	Request host application processing
PRINT	PRINT	Sends screen data to local printer
RESET	CANCEL	Clears screen, restores keyboard for data entry, after input inhibit condition occurs
SHIFT	SHIFT	Enter uppercase characters into input field
SOUTH	DOWN ARROW	Moves cursor down one position
SYS REQ	SHIFT/MOVE	Initiates or terminates session with host
TAB	TAB	Moves cursor to first character location of next input field, or extreme top left
TEST	SHIFT/GL	Display test in status line, no test performed
WEST	LEFT ARROW	Moves cursor one space left

E.2.2 OIA STATUS LINE

The OIA Status Line occupies the last line (eg. line 25 for 3278 Model 2) of the display screen. The Operator Information Area (OIA) displays 3278 session status information. This information is displayed in inverse video.

Two status line modes are available, Text mode and Symbol mode. In Symbol mode, the Status Line contains symbols that resemble standard IBM 3278 Status line symbols. In Text mode, the status line contains the english-language replacements for the standard 3278 symbols.

Three columns on the Status Line provide information about the 3278 Emulation session. These status indicators are summarized in Table E-2. Information pertaining to other columns of the Status Line is explained in Appendix D of the Professional Computer Manual.

Table E-2. 3278 Status Line

Column	Indicator	Meaning
75	R	The emulator is running in Resident Mode. If this column is blank, the emulator is running in normal mode.
77	xx (two digits)	This number indicates the data area row currently displayed at the top of the screen.
80	x (one digit)	Indicates the model number of the 3278 terminal being emulated.

E.2.3 EXTENDED FUNCTIONS

The 3278 Emulation Board supports a number of functions not available on the standard 3278 terminal. These functions are briefly discussed in this section. Refer to the 3278 Emulation manual for detailed description.

Six extended functions are supported. These functions are:

- Screen Capture
- Screen Append
- Local Print
- Resident Emulator Mode
- Test
- Exit

To access an extended function, perform the following:

1) Press the Shift and Help keys at the same time. The following information appears on the Status Line:

A)PPEND C)APTURE E)XIT P)RINT R)ESIDENT T)EST

2) Press Shift and Help again at the same time then press the first letter of Extended Function requested. See example.

ex. SHIFT/HELP P (selects local Print function)

3) To exit from the Extended Function press SHIFT/HELP or SHIFT/HELP E.

Table E-3 summarizes the Extended Functions.

Table E-3. 3278 Extended Functions

FUNCTION	COMMAND	RESULTING ACTION
Screen Capture	SHIFT/HELP C	Saves a screen of data in a user-specified local disk file; overwrites a DOS file with the same name if one exists.
Screen Append	SHIFT/HELP A	Adds a screen of data to a user-specified local disk file.
Local Print	SHIFT/HELP P	Sends one screen of data to the PC configured printer.
Resident Emulator Mode	SHIFT/HELP R	Eliminates the need to re-load the emulator software for each use.
Test	SHIFT/HELP T	Resets the system and displays the main system menu.

E.3 3278 PCB INSTALLATION

This section provides information for unpacking, inspecting, installing, and verifying correct operation of the 3278 Emulation Board.

E.3.1 SPECIAL TOOLS AND TEST EQUIPMENT

The standard items provided in the WANG CE Tool Kit will suffice for the installation of the Wang Professional Computer. No special tools other than a cardboard-cutting knife and a screwdriver are necessary for unpacking and installing the 3278 Emulation PCB.

E.3.2 UNPACKING

NOTE

Perform a careful visual inspection of each shipping container for any indication of possible shipping damage (crushed edges, corners, puncture holes, tears, etc.). If any shipping damage is noted, now or during subsequent opening of any package, file an appropriate claim promptly with the carrier involved and notify the WLI Distribution Center Dept #90, Quality Assurance Department, Tewksbury, Mass. 01876, of the nature and extent of the damage while making arrangements for equipment replacement.

Unpack the 3278 Emulation board as shown in figure E-3.

Save all of the packing material that came with the 3278 Emulation PCB. For the purpose of safety, you should reuse the packing materials whenever the PCB is transported.

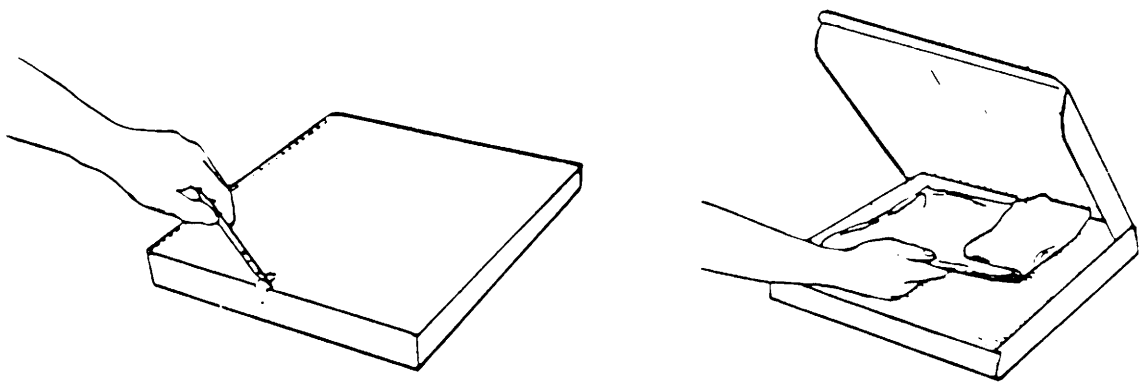


Figure E-3. Unpacking the 3278 Emulation Board

E.3.3 INSPECTION

After unpacking the Option board(s), the CE should inspect all components for possible damage. Any damage should be reported as previously discussed in paragraph E.3.2.

E.3.4 EQUIPMENT IDENTIFICATION

This section identifies the components of the 3278 Emulator Board prior to installation. Refer to Figure E-4. Note: The 2K/8K Jumpers (shown in callout) must either be in the 2K position or removed from the board. The 4K/16K Jumper must be in the 4K position or removed.

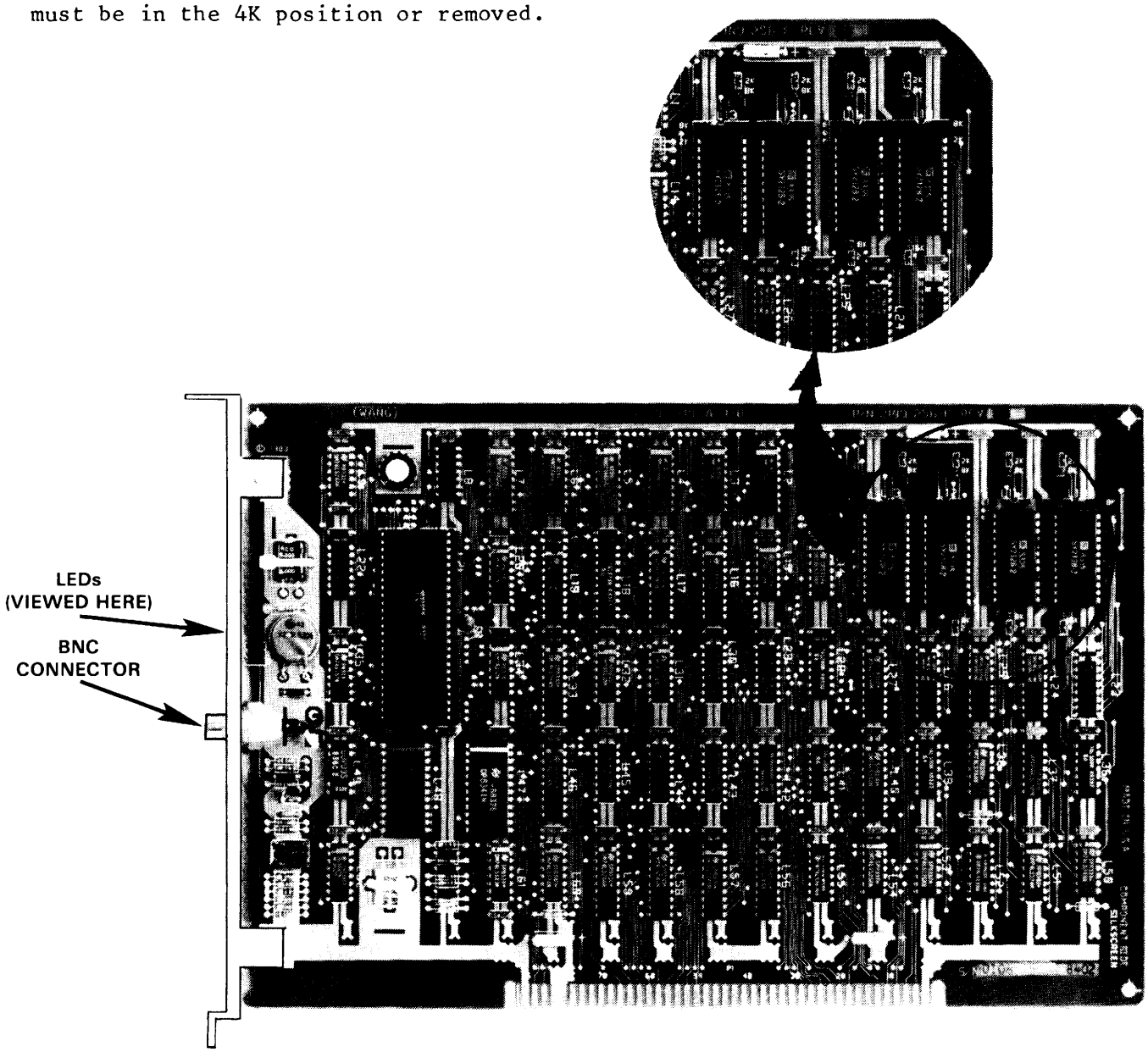


Figure E-4. 3278 Emulation Board Identification

E.3.5 INSTALLATION

This section contains installation information for proper installation of the 3278 Emulator PCB. This section consists of installing the 3278 Emulator PCB into the PC and connecting the coaxial cable. Note: This option is customer installable, the information presented below is for CE reference.

E.3.5.1 Installing the 3278 Emulator Board

The 3278 Emulator Board can be used in either the 5-slot PC or the Expanded Chassis PC. This option board may be installed in any available option slot. To install the PCB perform refer to paragraph 4.9.1 Installing an Option PCB.

E.3.5.2 Installing the Coaxial Cable

The coaxial cable connects the Wang PC (5-slot or Expanded Chassis) to the 3274 or 3276 Control Unit. Any combination of cable lengths can be used up to but not exceeding 5000 feet (1524 meters). It is the customers responsibility to run the coaxial cable from the controller to the terminal's location.

BNC Splicing Adapters (350-2077) must be used to connect different cable lengths together. To connect the coaxial cable to the 3278 Emulator interface perform the following:

1) Check with the system administrator at the host site to verify that the emulated terminal model (eg. 3278-2) is properly configured.

2) Ensure the proper coaxial cable (RG62A) and cable length is being used. Nine lengths of "Ready-Made" cables are available from Wang; these are:

READY-MADE COAXIAL CABLES

Part Number	Length
120-2321-001	10 feet
120-2321-002	25 feet
120-2321-003	50 feet
120-2321-004	100 feet
120-2321-005	250 feet
120-2321-006	500 feet
120-2321-007	750 feet
120-2321-008	1000 feet
120-2321-009	2000 feet

Raw cable can be ordered and cut to the desired length. BNC connectors must be installed on both ends of the cable. The parts required to make custom length cables and the BNC Splicing Adapter (Bullets) are as follows:

Nomenclature	Part Number
Raw Coaxial Cable (2000 feet)	420-0164
BNC Connector (two required per cable)	350-2114
BNC Splicing Adapter (one per two cables)	350-2077

3) Connect one of the Coaxial Cable BNC Connectors to the 3278 Emulator Board installed in the PC. Connect the other BNC connector to the interface unit (either a 3274 or 3276 Control unit).

E.3.6 SYSTEM POWER-ON

The start-up procedures refer to a dual drive start-up procedure with drive A being the default drive. If a winchester is used and has the system files loaded, start-up will be from the winchester.

Power on the Electronics Unit. Once power is applied, load the system diskette into floppy drive A. When the Time and Date Screen is displayed enter the current time and date and press EXECUTE to display the Main System Menu as shown in figure E-5.

NOTE

FOR THE PURPOSE AND CLARITY OF THIS MANUAL, SOFTWARE RELEASE LEVELS ARE DENOTED x.x. THE ACTUAL RELEASE LEVEL DISPLAYED DENOTES THE LEVEL OF SOFTWARE BEING RUN. THE SYSTEM SCREEN LOADS DISPLAYED ARE SYSTEM SCREENS AS OF THIS WRITING, ACTUAL SCREEN LOADS MAY VARY PER CUSTOMER.

```
mm/dd/yy          Wang Professional Computer          hh:mm:ss
              M A I N   S Y S T E M   M E N U
                        Release x.x

  Select an Item and Proceed

                    _ Applications
                    _ Conversion Aids
                    _ System Utilities
                    _ Program Development
                    _ Communications
                    _ DOS Command Processor
                    _ Other

                                  SPACE BAR - Item Select
                                  EXECUTE   - Proceed
```

Figure E-5. The Main System Menu Display

With the Main System Menu displayed, select System Utilities and press EXECUTE. The System Utilities menu will be displayed on the screen.

```
mm/dd/yy          Wang Professional Computer          hh:mm:ss
          S Y S T E M   U T I L I T I E S   M E N U
                        Release x.x

Select an Item and Proceed

     _ Check Disk                    _ Path - Change Directory
     _ Directory Display             _ Path - Make Directory
     _ Disk Copy                     _ Path - Remove Directory
     _ Disk Format                   _ Path - Select Alternates
     _ File Compare                  _ Set Date
     _ File Copy                     _ Set Default Drive
     _ File Copy With Append         _ Set National Defaults
     _ File Delete                   _ Set Time
     _ File Rename                   _ Write Verify
     _ Modify System Menus           _ Other

                                   SPACE BAR - Item Select
                                   EXECUTE   - Proceed
                                   CANCEL    - Previous Menu
```

Figure E-6. System Utilities Menu

Select the Modify System Menus option from the System Utilities Menu and press EXECUTE. The Interactive Menu Design Utility as shown in figure E-7 will be displayed.

```
mm/dd/yy          Wang Professional Computer          hh:mm:ss
                Interactive Menu Design Utility
                        Release x.x

Select desired option

                    __ Create new menu
                    __ Edit existing menu

       Menu file ID: ________________________________________

           On Drive: ___

                                   SPACE BAR - Item Select
                                   EXECUTE   - Proceed
                                   CANCEL    - Previous Menu
```

Figure E-7. Interactive Menu Design Utility Screen

Select "Edit existing menu" option and press RETURN. The cursor will move to the "Menu File ID:" area. Now enter;

TCMENU.DAT

Leave the On Drive area blank to specify that TCMENU.DAT is on the default drive. Press EXECUTE to accept the currently displayed values and proceed to the next menu. When the next menu is displayed, press EXECUTE to proceed the menu shown in figure E-8.

```
|-----------------------------------------------------------------|
|                    Wang Professional Computer                   |
|              C O M M U N I C A T I O N S   M E N U               |
|                          Release x.x                            |
|                                                                 |
|                 __ Asynchronous Communications                  |
|                 __ Wang 2200 Terminal Emulation                 |
|                 __ 2780/3780 Batch Communications               |
|                 __ Remote WangNet                               |
|                 __ Other                                        |
|                                                                 |
|                                                                 |
| * Add new Entry    _ Delete          EXECUTE - Select Operation |
| _ Edit             _ Edit Header     CANCEL  - End/Update Menu  |
| _ Reorder          _ Edit Help Screen                           |
|-----------------------------------------------------------------|
```

Figure E-8. Selecting an Entry Screen

Move the acceptance block to the space where the 3278 Emulation Option is to be displayed on the menu and press RETURN. Select "Add New Entry" and press EXECUTE. Once selected, the following menu appears as shown in figure E-9.

```
|-----------------------------------------------------------------|
|                    Wang Professional Computer                   |
|              C O M M U N I C A T I O N S   M E N U               |
|                          Release x.x                            |
|                                                                 |
|                 __ Asynchronous Communications                  |
|                 __ *                                            |
|                 __ Wang 2200 Terminal Emulation                 |
|                 __ 2780/3780 Batch Communications               |
|                 __ Remote WangNet                               |
|                 __ Other                                        |
|                                                                 |
| File Name:**          File Extension:***    On Drive:__         |
| In Directory:                                                   |
| Module Type: _ Menu   @ Program         EXECUTE - Accept Screen |
|_ Other _ System Functions  _ Command    CANCEL - Cancel Operation |
|                                                                 |
|-----------------------------------------------------------------|
```

Figure E-9. Adding New Menu Entry Screen

Note the cursor is positioned in the Menu Option description field denoted by the asterisk (*). Enter:

3278 Terminal Emulation (or other desired name)

Now press the RETURN key to move the cursor to the "File Name" field denoted by two asterisks (**). Enter:

wpc3278

Now press the RETURN key to move the cursor to the "File Extension" field denoted by three asterisks (***). Enter:

exe

Leave "On drive" field blank to specify that wpc3278.exe is located on the default drive. Press RETURN to move to the Module Type field. Select the option "Program" (denoted by the @ sign) to indicate that wpc3278.exe is a program file. Press EXECUTE to accept the additions made. Now press CANCEL to "Update" the menu.

Now the prompt "Press EXECUTE to update menu definition or Press CANCEL to return to menu without updating file" occurs. Press EXECUTE to store the information input into the previously described menus. Once the PC has finished writing the information into the TCMENU.DAT file press the CANCEL key until the Main System Menu is displayed.

E.4 RUNNING The 3278 EMULATION SOFTWARE

To run the 3278 software perform the following:

1) Power-on the system with a diskette that has the system files on it. Now, load the 3278 Emulation diskette into the default drive.

2) Access the Communications menu from the Main System Menu and select the 3278 Emulation Option.

3) One screen of information about the 3278 Emulator and the copyright appear on the screen, this information then disappears and the OIA status line appears.

4) At this point, follow the conventions and commands provided by the IBM host's system administrator to access the application programs.

E.5 POWER-ON DIAGNOSTICS

Located on the 3278 Emulation PCB (visible through a slot in the rear RF shield) are three LEDs colored Green, Red, and Yellow. During System power-on, the 3278 Emulator runs a series of Power-up test whose results are displayed on these LEDs. These test in order of occurrence are;

- o Board Locate Test
- o Down Load RAM Test
- o Read/Write Register Test
- o Display RAM Parity Test
- o Coax Loopback/Relay Test
- o Controller Detect Test

The Board locate test is performed by the 8086 CPU to determine if a 3278 Emulator board is present. If the 3278 Emulator is not detected by the CPU then a error has occur and no other diagnostics will be run. The LEDs will not be illuminated.

The Down Load RAM test performs a test on the program RAM located on the 3278 Emulator board. This test checks all program RAM bits as well as checks parity. If this test fails no other diagnostics will be run. The LEDs will not be illuminated.

The Read/Write Register test allows the 8086 CPU to write to and read the read/write registers located on the 3278 Emulation board. The 3278 emulator's on-board microprocessor also reads and writes these registers during this test. If this test fails no other diagnostics will be run. The LEDs will not be illuminated.

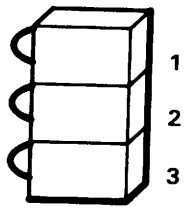
The Display RAM/Parity test allows the 3278 on-board microprocessor to write to and read from the display RAM circuitry. This test checks memory locations and error detection circuits. Like the previous test, if an error occurs no other diagnostics will run and no LEDs will be illuminated.

The Coax Loopback/Relay test checks the data path out to the transceiver circuitry back through the receiver circuitry. If the loop is successful, the Coax link relay (a relay in line with the BNC connector which provides a terminator when the 3278 Emulator is not running and provides the pathway only when the 3278 Emulator board is operational) is energized providing the data path. Once this test is completed and the relay is closed the Yellow LED is illuminated.

The Controller Detect test checks if a controller is located on the other end of the Coax cable. If no controller is available or the cable is not connected, an error occurs. The LED pattern is Yellow On, Red and Green Off. The problem maybe that the controller's port is undefined or the coax cable is unattached or defective. Attach the coax cable to another controller port that is defined for 3278 Emulator use.

If all the tests pass and the 3278 Emulator can communicate with the controller, all LEDs will be On. LED yellow will be on constant and LEDs Red and Green may be blinking.

The LEDs definition are defined as follows;



RED Coax Receive

GREEN Coax Transmit

YELLOW Relay Closed

The LED Truth Table is as follows:

Table E-4. LED Truth Table

RED	GREEN	YELLOW	CONDITION
X	X	X	Board Operational
*	*	0	Board Defective
0	0	X	Coax Defective or Controller Problem

X denotes ON
0 denotes OFF
* denotes Don't Care

If a Coax Error or Controller problem is reported, remove the coax from the controller port and reconnect to a different controller port which is defined for 3278 emulation of the same model type. Retest the 3278 Emulation Power-Up diagnostics. If the same error condition is reported, contact the system administrator to ensure proper system configuration.

Note: Connections to a port of different model configuration may cause only partial operation or undefined errors. ENSURE CORRECT MODEL TYPE PORT IS USED WITH THE MODEL TYPE PROGRAM.

E.6 PCDS Diagnostics

PC Diagnostics diskette contains the Diagnostics Program "FORTE". This diagnostic program can be run in either the Customer mode or the CE Mode. Refer to the documentation supplied with the diskette for operating procedures.

E.7 CONFIGURATION UTILITY

The PC 3278 Emulator diskette contains a Configuration Utility program (3278CNF) that allows the user to make certain changes, Such as:

- o Change the IBM Model Configuration
- o Change the Status Line Configuration
- o Change the Keyboard Configuration

The Configuration Utiltiy is stored on the 3278 Software Diskette. To access this file perform the following:

1) With the Main System Menu displayed on the screen and the 3278 Emulator software diskette loaded into Drive A, select Option "Other" and press EXECUTE. Now Enter:

   3278CNF

   The Configuration Utility screen will be displayed. See figure E-10.

```
|-------------------------------------------------------------------|
|                    Wang Professional Computer                     |
|              3278 Terminal Emulation (version x.x)                |
|                         Release x.x                               |
|                                                                   |
|  Select an Item and Press Enter:                                  |
|                                                                   |
|             __ Model Configuration                                |
|             __ Status Line Configuration                          |
|             __ Keyboard Configuration                             |
|                                                                   |
|                                     EXECUTE  - Proceed            |
|                                     CANCEL   - Previous Menu      |
|-------------------------------------------------------------------|
```

Figure E-10. Configuration Utility Screen

Position the acceptance block to the configuration to be change and press EXECUTE, that selection will be displayed on the screen. The three options available thru this program are discussed in the preceding text.

E.7.1 Model Configuration Utility

The Model Configuration Utility allows the user to change the configured IBM Model Number (eg. Model 2 to Model 3, Model 2 to Model 4 etc). To use this utility, perform the following:

With the Configuration Utility Screen displayed as in figure E-10, position the acceptance block next to "Model Configuration" and press EXECUTE. The Model Configuration Screen will be displayed as shown in figure E-11.

```
|-------------------------------------------------------------------|
|                    Wang Professional Computer                     |
|               3278 Terminal Emulation (version x.x)               |
|                        Model Configuration                        |
|                                                                   |
|  Select a Terminal Model:                                         |
|                                                                   |
|              __ IBM 3278 Model 2                                  |
|              __ IBM 3278 Model 3                                  |
|              __ IBM 3278 Model 4                                  |
|                                                                   |
|                                      EXECUTE  - Proceed           |
|                                      CANCEL   - Previous Menu     |
|-------------------------------------------------------------------|
```

Figure E-11. Model Configuration Screen

Move the acceptance block to the model to be emulated and press EXECUTE. If CANCEL is pressed, the system returns to the Configuration Menu and the model number is not changed.

E.7.2 Status Line Configuration

With the Configuration Utility Screen displayed as in figure E-10, position the acceptance block next to "Status Line Configuration" and press EXECUTE. The Status Line Configuration Screen will be displayed as shown in figure E-12.

```
|-------------------------------------------------------------------|
|                    Wang Professional Computer                     |
|               3278 Terminal Emulation (version x.x)               |
|                                                                   |
|  Select a Status Line Mode:                                       |
|                                                                   |
|              __ Text Mode                                         |
|              __ Symbol Mode                                       |
|                                                                   |
|                                      EXECUTE  - Proceed           |
|                                      CANCEL   - Previous Menu     |
|-------------------------------------------------------------------|
```

Figure E-12. Status Line Configuration Screen

If the Text mode is selected, the status line (bottom line of the display) contains English language replacements for the standard 3278 status line symbols. In Symbol mode, the status line contains standard 3278 Emulation symbols. These Symbols are shown in figure E-13.

Select the desired mode and press EXECUTE. If CANCEL is pressed, the system returns to the Configuration Menu and the Status Line Mode will remain the same.

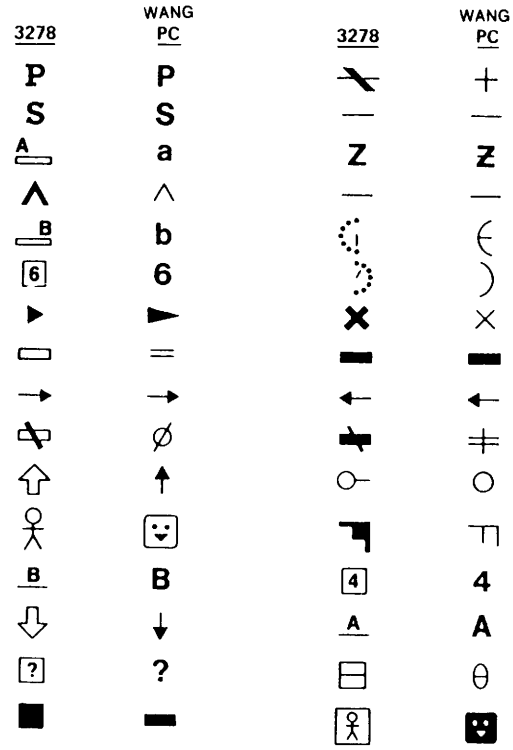


Figure E-13. Wang PC 3278-2/3/4 and 3278 Special Symbols

E.7.3 Keyboard Configuration

The Keyboard Configuration Option allows the end user to change the non-alphanumeric special keys (PF1-PF24, Prev, Next etc) from the 3278 keys or key combinations to any key or key combination more suited to the end user's need. This option contains two screens, each screen is shown in the preceding text.

With the Configuration Utility Screen displayed as in figure E-10, position the acceptance block next to "Keyboard Configuration" and press EXECUTE. The first Keyboard Configuration Screen will be displayed on the screen as shown in figure E-14.

```
Wang Professional Computer
3278 Terminal Emulation (version x.x)
Keyboard Configuration

PF1:  PF1          PF13:  PF13
PF2:  PF2          PF14:  PF14
PF3:  PF3          PF15:  PF15
PF4:  PF4          PF16:  PF16
PF5:  PF5          PF17:  PF17
PF6:  PF6          PF18:  PF18
PF7:  PF7          PF19:  PF19
PF8:  PF8          PF20:  PF20
PF9:  PF9          PF21:  PF21
PF10: PF10         PF22:  PF22
PF11: PF11         PF23:  PF23
PF12: PF12         PF24:  PF24

                   EXECUTE  - Proceed
                   CANCEL   - Previous Menu
```

Figure E-14. Keyboard Configuration Menu Screen 1

Any field can be changed by typing over the value of the underlined portion. Press Cancel to return to the previous menu with no changes being accepted. To advance to the second screen press EXECUTE. This screen is shown in figure E-15.

```
Wang Professional Computer
3278 Terminal Emulation (version x.x)
Keyboard Configuration

Alt. Cursor:   PREV          Field Mark:    PF31
ATTEN:         GL            Home:          HOME
CLEAR:         PF29          INDENT:        Shift PRINT
CLICK:         Shift NEXT    Insert:        INSERT
Cursor Blnk:   Shift PREV    Print:         PRINT
Cursor Sel:    NEXT          Reset:         CANCEL
Delete:        DELETE        Newline:       RETURN
Device Cncl:   PF30          SYS REQ:       PF28
Dup:           PF32          TEST:          Shift GL
Enter:         EXEC          Double Left:   Shift Left
Erase EOF:     ERASE         Double Right:  Shift Right
Erase Inp:     Shift ERASE

                   EXECUTE  - Proceed
                   CANCEL   - Previous Menu
```

Figure E-15. Keyboard Configuration Menu Screen 2

Change key entries on this menu by typing over the value on the underlined portion of the screen. Press CANCEL to return to Keyboard Configuration Menu Screen 1. Press EXECUTE to exit the menu. Note to exit the menu and to save all entries made, the exit must be from the second screen. When the Configuration Menu is exited, the software checks for duplicate or illegal entries. If an illegal entry or a duplicate entry is found, one of the following error messages will be displayed:

XXX: Duplicate Entry, try again

XXX: Keyboard Code not allowed

XXX denotes the keycode that is duplicated or illegal. Move the cursor to the indicated keycode and insert the correct code. Exit the Menu as previously discussed.

WANG PROFESSIONAL COMPUTER

EXPANDED CHASSIS ADDENDUM

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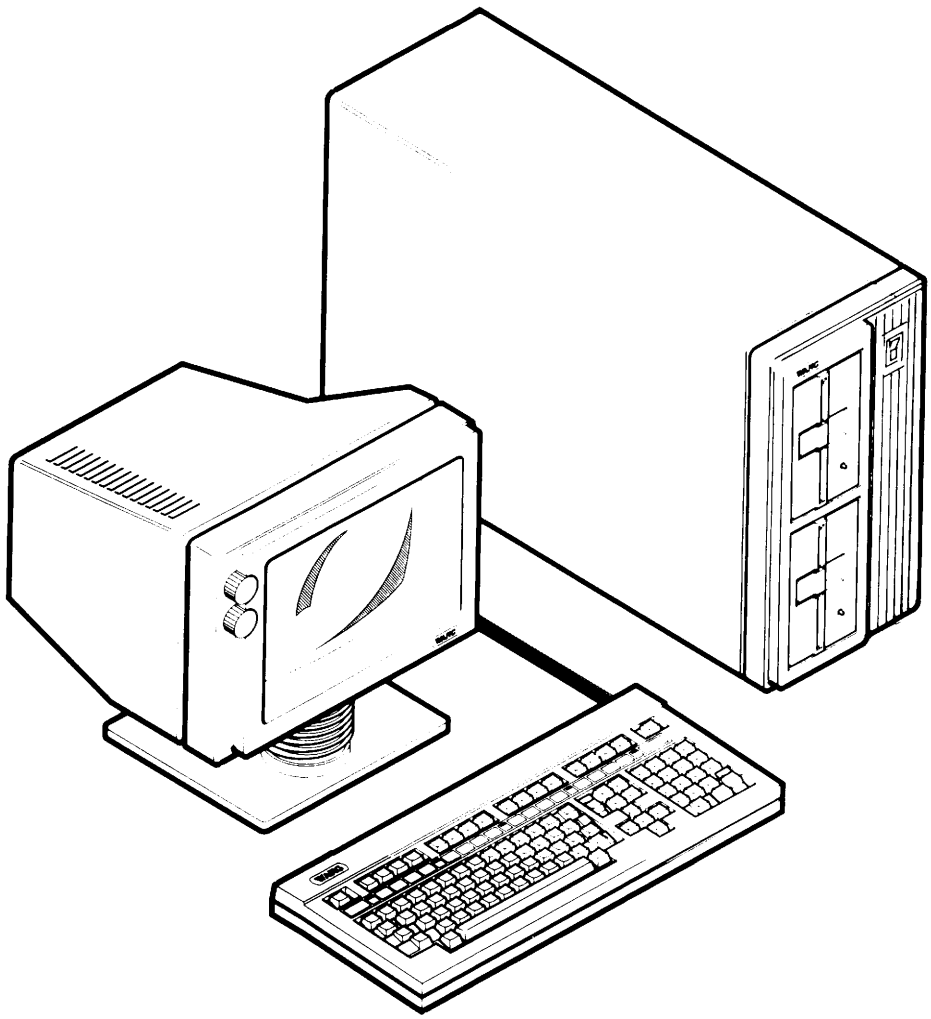
LIST OF TABLES



Expanded Chassis Professional Computer

CHAPTER 1

INTRODUCTION

1.1 SCOPE

The Wang Expanded Chassis PC maintenance documentation for Wang PC trained CE's is contained in this PC addendum. This addendum is designed to be used in conjunction with the PROFESSIONAL COMPUTER MANUAL part number 729-1190.

This addendum provides installation, controls and indicators, corrective and preventive maintenance, and removal and replacement procedures, for the Expanded Chassis PC. An IPB (illustrated parts breakdown) is provided to aid in locating and identifying all the major components.

PC option board schematics are provided in the PC Schematics manual part number 729-1241.

The level of coverage in this addendum is directed toward an Associate Field Engineering Technician (AFET) with a minimum of six months field experience who has received qualified commercial PC training either directly from a Wang course instructor or indirectly via Wang video tape.

A chart is included that contains prepackaged configurations of the Expanded Chassis PC that can be ordered which include both standard and optional features.

A listing of the Expanded Chassis specifications is contained in paragraph 1.5. These specifications contain dimensions, net weight, power requirements, and environment conditions for the PC.

1.2 APPLICABLE DOCUMENTATION

Applicable documentation (software, user documentation, and CE product maintenance documentation) is listed in the Professional Computer manual.

1.3 SYSTEM DESCRIPTION

The basic Wang Expanded Chassis PC is a high performance, highly modular computer system which features data processing, word processing, and image processing capabilities. It can operate in a stand-alone mode, through coaxial cable to other Wang products and through telephone lines to Wang and non-Wang products.

The Expanded Chassis PC comes with many standard features and a host of optional features. These features (standard and optional) are identified in the Professional Computer manual.

The Expanded Chassis enclosure is compact, lightweight, and can control a variety of I/O devices. The Electronic Enclosure houses the 210-8644 CPU board, the 210-9641 Motherboard, the System Floppy Drive, an optional Floppy Drive or 10MB Winchester Drive, an SPS-255 Switching Power supply, and up to eight option boards. The CPU/System board is equipped with the following:

- o A standard 128KB of Parity-Checked memory for user programs.
- o Three channel direct memory access (DMA) capability.
- o A program-addressable internal clock.
- o An RS-232C asynchronous interface that supports serial devices and communications. (Does not require option board)
- o A Centronics-compatible parallel printer interface.
- o A Floppy Diskette Drive Interface capable of controlling two 360K disk drives.
- o A keyboard interface.

The option boards, keyboard, and monitor are the same as for the 5-slot Professional Computer.

1.4 SYSTEM CONFIGURATIONS

The Expanded Chassis PC is available in a number of configurations that can be tailored to meet specific customer requirements. Presently, four configurations made up of both standard and optional features can be ordered. These are delivered pre-assembled so that the customer does not have to install the option boards thereby minimizing the requirements of ordering, configuring, and setting up the delivered system. Table 1-1 lists the available Expanded Chassis (XC) configurations.

Table 1-1. Expanded Chassis System Configurations

	PC-				
HARDWARE/SOFTWARE	XC	XC1	XC2	XC3	XC4
Base System Unit with 128k Memory	X	X	X	X	X
360K Floppy Disk Drive	X	X	X	X	X
Low Profile Keyboard	X	X	X	X	X
MS/DOS Operating System (Plus Interpreter Basic)	X	X	X	X	X
MS/Compiled Basic	X	X	X	X	X
PC-PM001 Character Display Adapter		X	X	X	X
PC-PM004 Monochrome Display		X	X	X	X
PC-PM020 Second 360K Floppy Drive			X	X	
PC-PM002 Graphics Display Adapter				X	X
PC-PM030 Additional 128K RAM					X
PC-PM021 Winchester 10MB Disk Drive (with Adapter)					X

1.5 SYSTEM SPECIFICATIONS

Dimensions

Electronics Enclosure

Width	9.50 inches	(24.13 cm)
Length	23.25 inches	(59.06 cm)
Height	14.75 inches	(37.47 cm)
Depth	7.80 inches	(19.81 cm)

Net-Weight

Electronics Enclosure 52.00 lb (23.59 kg)

Power Requirements

Minimum	Nominal	Maximum	Frequency	Wattage
103v	115v	127v	47 - 63 Hz	400
206v	230v	254v	47 - 63 Hz	400

Amperage

3.0 Amps at 115 volts
1.5 Amps at 230 volts

Operating Environment

Ambient Temperature
45 deg. F to 100 deg. F (7 deg. C to 38 deg. C)

Altitude - 500 feet below sea level
- 10,000 feet above sea level
Heat Dissipation - 1440 BTUs per Hour

Non-operating Environment

Temperature
50 deg. F to 104 deg. F (10 deg. C to 40 deg. C)
Relative Humidity - 5% to 85% (non-condensing)
Maximum Wet Bulb Temperature 75 deg. F (24 deg. C)
Maximum Temperature Rate of Change 12 deg. F/Hour (6.7 deg. C/Hour)

Cabling

Electronics Unit to Monitor	12 feet	(3.66 meters)
Electronics Unit to Keyboard	6 feet	(1.83 meters)
Power Cord	12 feet	(3.66 meters)

CHAPTER 2

THEORY

2.1 SCOPE

The theory section for the Expanded Chassis Professional Computer consists of the theory for the Motherboard and the SPS255 Switching Power Supply. These two components are the only hardware differences (other than the weldment and enclosure cover) between the 5-slot PC and the Expanded Chassis PC. Option board theory of operation is contained in the Professional Computer manual.

2.2 Motherboard (210-9257) Theory of Operation

The Motherboard (9257) provides a common bus that extends the 20-bit Address bus, the 16-bit Data bus, and the 30-bit Control bus to the other eight option slots. These option slots are prioritized with Slot 8 (J12) having the Highest priority and Slot 1 (J5) having the lowest priority. Also common bussed are the voltage levels required by the system.

The 9257 Motherboard is a compact board that fits vertically against the side of the SPS-255 power supply. Located at the top of the board are the power supply connectors (J1, J2, and J3), a noise filter, a despiking network for the bus control signals and the two system clocks. The system bus provides 16 bidirectional data lines, 20 address lines, and various control signal lines. Interrupt request lines implement six levels of priority interrupt and one nonmaskable "error" interrupt. The bus also contains the power lines providing the four voltage levels required by the option boards.

Pins 81, 82, 83, and 84 of each of the eight option board connectors are wired differently to provide the slot ID codes via the board that is plugged into the slot. The eight option slots are prioritized with Slot 8 being the highest and Slot 1 being the Lowest. Motherboard pin assignment for the option board expansion slots is shown in Table 2-1.

Table 2-1: Motherboard Pin Assignments (Expansion Slots (J5-12) Only)

Pin	Signal	Pin	Signal	Pin	Signal
1	GND	30	A13	59	D10
2	GND	31	A14	60	D11
3	CLK (8 MHz)	32	A15	61	D12
4	-RESET	33	A16	62	D13
5	-5 V	34	A17	63	D14
6	-IRQ2	35	A18	64	D15
7	-IRQ3	36	A19	65	WTR
8	-IRQ4	37	-BHE	66	HACK
9	-IRQ5	38	GND (monitor	67	-I/O ERROR
10	-IRQ6	39	GND power)	68	ADDSTB
11	-IRQ7	40	-DACK0	69	T/C
12	-AIOWC	41	-DACK1	70	RDY
13	-IORC	42	-DACK2	71	-SAD
14	-AMWC	43	-DACK3	72	MCE
15	-MRDC	44	-DREQ1	73	+12V (monitor
16	ALE	45	-DREQ2	74	+12V power)
17	A0	46	-DREQ3	75	-12 V
18	A1	47	DEN	76	+12V
19	A2	48	DT/R	77	4CLK
20	A3	49	D0	78	+5V
21	A4	50	D1	79	+5V
22	A5	51	D2	80	+5V
23	A6	52	D3	81	SID0
24	A7	53	D4	82	SID1
25	A8	54	D5	83	SID2
26	A9	55	D6	84	SID3
27	A10	56	D7	85	GND
28	A11	57	D8	86	GND
29	A12	58	D9		

NOTE: A dash (-) preceding the signal name denotes low-active signals.

2.3 SPS255 Switching Power Supply

The SPS255 Switching Power Supply is capable of outputting four supply voltages +5, -5, +12, and -12 volts dc. The power supply input circuit converts the ac line voltage (115/230 vac) into rectified and filtered high voltage dc. The high voltage dc is chopped at a frequency of 25 KHz by a pulse width modulator presenting high voltage pulsating dc to a multiple output transformer. This transformer steps down the high voltage pulsating dc.

The +5 output voltage is fed back to the pulse width modulator to establish a feedback voltage used to regulate the ON/OFF relationship of the pulse width modulator with respect to the voltage level source. This feedback voltage becomes the regulating voltage with all other voltages remaining secondary.

The power supply ac input is applied to an EMI filter (ElectroMagnetic Interference) to reduce EMI. This ac source is then routed to the 115/230V select switch.

All output voltages are full-wave rectified through their associated diode rectifier circuit. The power-on signal (WOLFTRAP) is an output of a comparator circuit that forward-biases a NPN transistor once the output voltages are stabilized.

Two voltages are adjustable; +5 and +12 volts. These voltages are adjustable from the outside of the power supply enclosure. The +5 volts must be adjusted first (the +5 volts output is used for the voltage regulator feedback voltage as discussed above), then adjust the +12 volts. Refer to Chapter 5 for adjustment procedures and power supply measurements locations.

2.4 Option PCB Theory

Option PCB theory is contained in the Professional Computer manual.

CHAPTER 3

OPERATION

3.1 INTRODUCTION

This chapter provides information pertaining to the operator controls and indicators, the Expanded Chassis initial control settings, initial turn-on procedures, and normal and emergency shut-down procedures.

3.2 CONTROLS AND INDICATORS

The Controls and Indicators for the Expanded Chassis PC are discussed in the following pages. Only the Expanded Chassis is discussed. The various peripheral devices (keyboard, Monitor, etc) are discussed in the Professional Computer manual.

3.2.1 Expanded Chassis Electronics Unit Indicators

Located on the front of the System Floppy Drive (Drive A) and the optional floppy drive (Drive B) is a LED. This LED will illuminate when the diskette loaded in the drive is being accessed by the system. This LED will toggle on and off while the information contained on the disk is either being read or the data read is being verified. When a winchester is installed, drive A LED will blink once as the system checks to see if a floppy is installed and determines whether to continue winchester boot or floppy boot. If the boot is from the winchester, the winchester's LED will illuminate. See figure 3-1.

Also located on the front panel is the On/Off (1/0) switch.

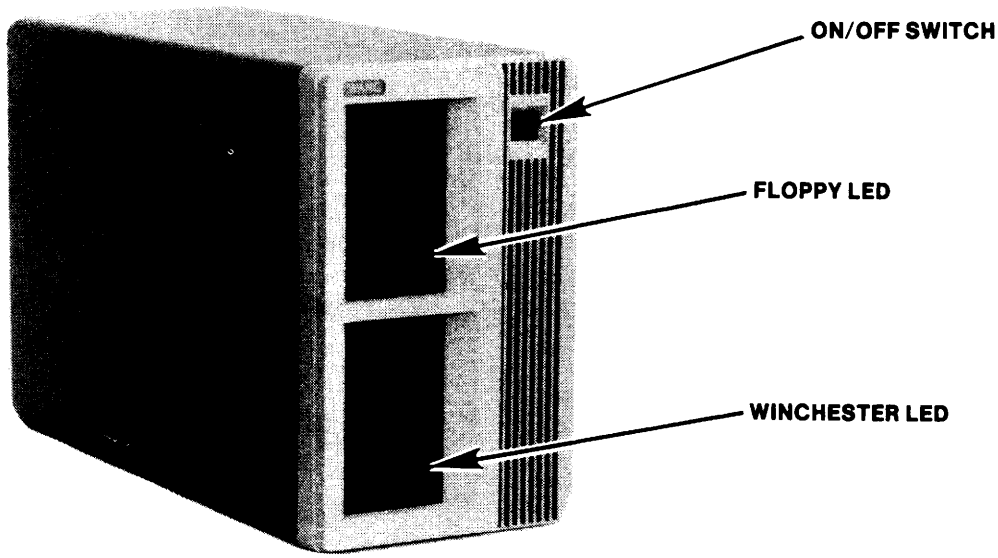


Figure 3-1. Electronics Unit Front Panel Controls/Indicators

Located on the rear of the CPU/System board is a parity LED. This LED is designated LED 1. The parity LED is visible by viewing through the grill work on the rear of the unit. See Figure 3-2 for viewing area. This LED will toggle on and off while the diagnostic test is being run or in the event of a parity error during operation.

Other option boards that have parity LEDS (ie, RTC board, Expanded Memory board) located on-board are viewed in the manner as described above. The illustration below shows the Diagnostic LED location for the RTC PCA.

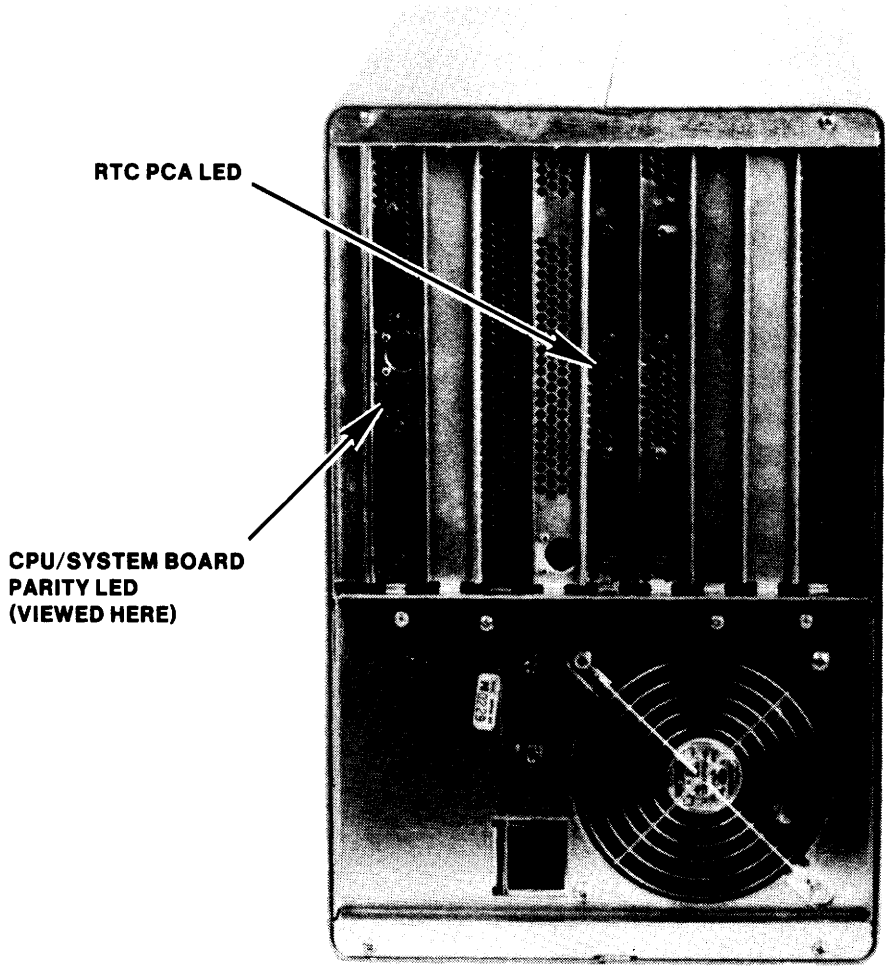


Figure 3-2. Electronics Unit Rear Panel Controls/Indicators

3.3 INITIAL CONTROL SETTINGS

The initial control setting for the PC are discussed in Chapter 4 paragraph 4.7. Depending on the options attached to your system (if any), ensure that each has the proper switch setting.

3.4 INITIAL TURN-ON PROCEDURES

Prior to powering-on the PC, ensure that all packing materials (plastic wrap, tape, etc.) are removed from the unit. Be sure the floppy disk drive(s) cardboard protector has been removed. Inspect the system to ensure all cables are properly attached as described in Chapter 4.8 Installation. Verify the proper voltage switch setting as described in Chapter 4 paragraph 4.7.2.

3.4.1 System Initialization

When power is first applied, the System Unit's fan starts, a short beep will sound, the Boot PROM diagnostics will run, and the Keyboard LEDs will flash on. Now insert the MS-DOS diskette into Floppy Drive A and latch the door closed. After a short time the Floppy's LED will illuminate and the system will execute the IPL (Initial Program Load). After the IPL is completed, the Floppy LED will go out and the Monitor will display the MS-DOS program title and request that the Time and Date be entered. After entering the time and date, the Main Menu will be displayed on the monitor. This denotes a successful power-up. Refer to Chapter 4 paragraph 4.11 (Powering-On the System) for a complete power-up sequence of events.

3.5 NORMAL SHUT-DOWN PROCEDURE

Before you Power-Down the Professional Computer return to the Main System Menu. Remove the floppy diskette (s), then Power-Down the system by turning the ac power ON/OFF (I/O) switch to the OFF (O) position. When the system is powered down, insert the card drive protector into drive(s) and close the Drive's doors. This will protect the drive heads from dust and foreign materials.

3.6 EMERGENCY SHUT-DOWN PROCEDURE

In case of an Emergency situation when the normal Shut-Down procedure can not be used, perform the following:

Turn the ON/OFF (I/O) switch to the OFF (O) position.
Remove the ac power cord from the wall outlet.

3.7 OPERATOR PREVENTIVE MAINTENANCE

Operator Preventive maintenance consists of general cleaning of the unit. To clean the unit, use a slightly damp lint-free cloth to wipe down the outside case of the electronics unit. DO NOT USE CHEMICAL OR ABRASIVE CLEANERS.

CHAPTER 4

INSTALLATION AND CHECKOUT

4.1 SCOPE

This section provides information for unpacking, inspecting, installing, and verifying correct operation of the Expanded Chassis PC. The Expanded Chassis PC is designed to be set up and installed by the customer. System modularity permits customers to upgrade to more powerful configurations without purchasing another system or replacing the base unit to support additional peripherals.

4.2 PRE-INSTALLATION SITE CHECK

No special pre-site planning is required for installation of the Expanded Chassis PC other than the recommended operating environment and procedural safeguards called out in the Customer Site Planning Guide (document No. 700-5978). The customer has the responsibility of ensuring that the Expanded Chassis PC installation site conforms to requirements given in the guide.

4.3 SPECIAL TOOLS AND TEST EQUIPMENT

The standard items provided in the WANG CE Tool Kit will suffice for the installation of the Wang Professional Computer. No special tools other than a cardboard-cutting knife and a screwdriver are necessary for unpacking the PC and its peripheral components.

4.4 UNPACKING

The Wang PC is designed for customer installation. The customer is responsible for unpacking the Expanded Chassis PC components, attaching them correctly, and running the diagnostic program to verify correct PC system operation.

NOTE

Perform a careful visual inspection of each shipping container for any indication of possible shipping damage (crushed edges, corners, puncture holes, tears, etc.). If any shipping damage is noted, now or during subsequent opening of any package, file an appropriate claim promptly with the carrier involved and notify the WLI Distribution Center Dept #90, Quality Assurance Department, Tewksbury, Mass. 01876, of the nature and extent of the damage while making arrangements for equipment replacement.

4.4.1 UNPACKING THE EXPANDED CHASSIS ELECTRONICS UNIT

Open the Electronics unit box by carefully cutting the tape along the box top. Open the top flaps and remove the top foam panel from the box. Now lift the Electronics Unit out of the box. Place the unit on your desk so that the front panel with the red power switch is facing you. The ac power cable is included in the Expanded Chassis box. See Figure 4-1.

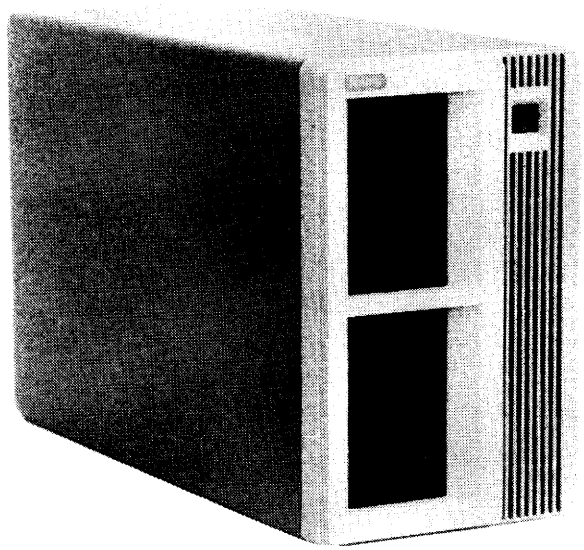


Figure 4-1. The Expanded Chassis Electronics Unit Unpacked

4.4.2 UNPACKING OPTION PCBS

Unpack all PCB card boxes that came with the equipment. These cards have to be installed in the Expanded Chassis PC prior to system installation.

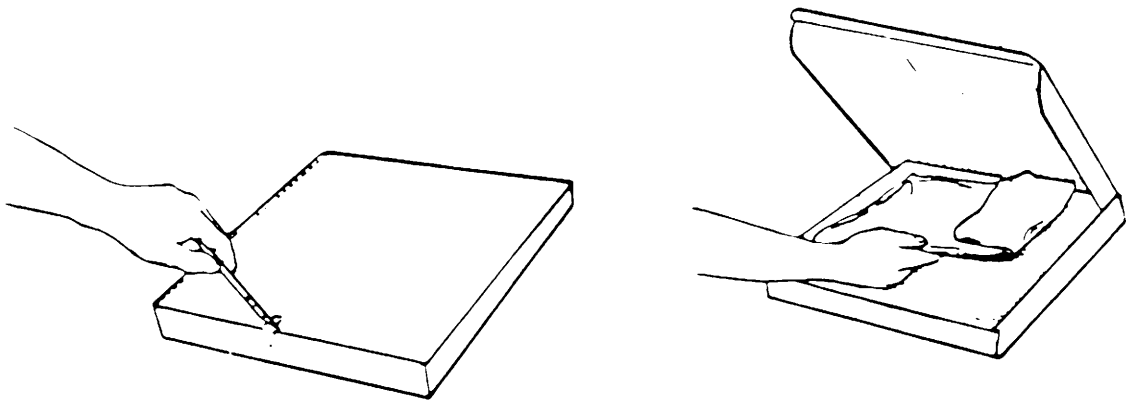


Figure 4-2. Unpacking PCB Cards

4.4.3 FINAL UNPACKING SEQUENCE

Perform the following steps to finish unpacking the Expanded Chassis PC. Inspect externally and internally for any shipping damage prior installation.

Step 1 Remove the diskette drive shipping protector.

( ) A thin piece of cardboard has been inserted in each disk drive during manufacturing to protect the drive from damage during shipping. These shipping protectors must be removed before connecting the system. To properly remove the shipping protectors from the diskette drives of your electronics unit, do the following:

Remove the cardboard shipping protector located in the drive by pulling it straight out. See Figure 4-3. The cardboard shipping protector(s) should be replace whenever the system is powered down.

NOTE
IF YOUR ELECTRONICS UNIT HAS A SECOND DISKETTE DRIVE REPEAT THIS PROCEDURE FOR THAT DRIVE.

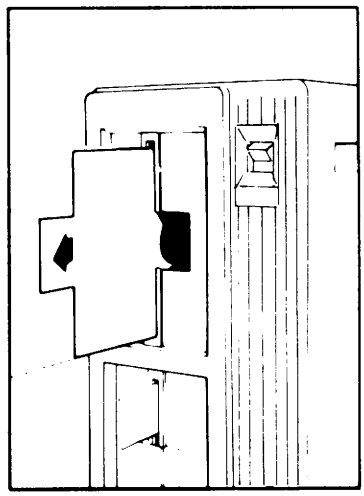


Figure 4-3. Removing the Shipping Protector From the Diskette Drive

Step 2 Remove the voltage setting label.

( ) Remove the voltage setting label from the power switch located on the front of the electronics unit. The Expanded Chassis PC has been preset at the factory for operation at 115 VAC. Operating the PC outside the continental United States, the line voltage MUST be set to 230 VAC. Refer to paragraph 4.7.2 for 115V/230V Switch setting.

Step 3 Save all of the packing material

( ) Save all of the packing material that came with your system. For safety purposes, reuse this material whenever your system is transported.

4.5 INSPECTION

After unpacking the Expanded Chassis, the CE should inspect all equipment, cables, and components for possible damage. Any damage should be reported as previously discussed in paragraph 4.4. If permanent damage to components is evident, do not continue the installation.

4.6 EXPANDED CHASSIS COMPONENT and CONNECTOR IDENTIFICATION

This section identifies the components that differ from the 5-slot PC as well as identifies all connectors, power cables, signal cables, switches, printed circuit boards, jumpers, etc, as necessary to connect the Expanded Chassis PC and its various peripheral items.

4.6.1 Expanded Chassis Base Unit (Rear View)

Figure 4-4 shows the location of all base unit connectors and indicators used to interconnect the base unit to the PC peripheral components. The illustration shown below is a representation of the Expanded Chassis PC Electronics Unit. The location of the option boards and the option boards installed may vary between units.

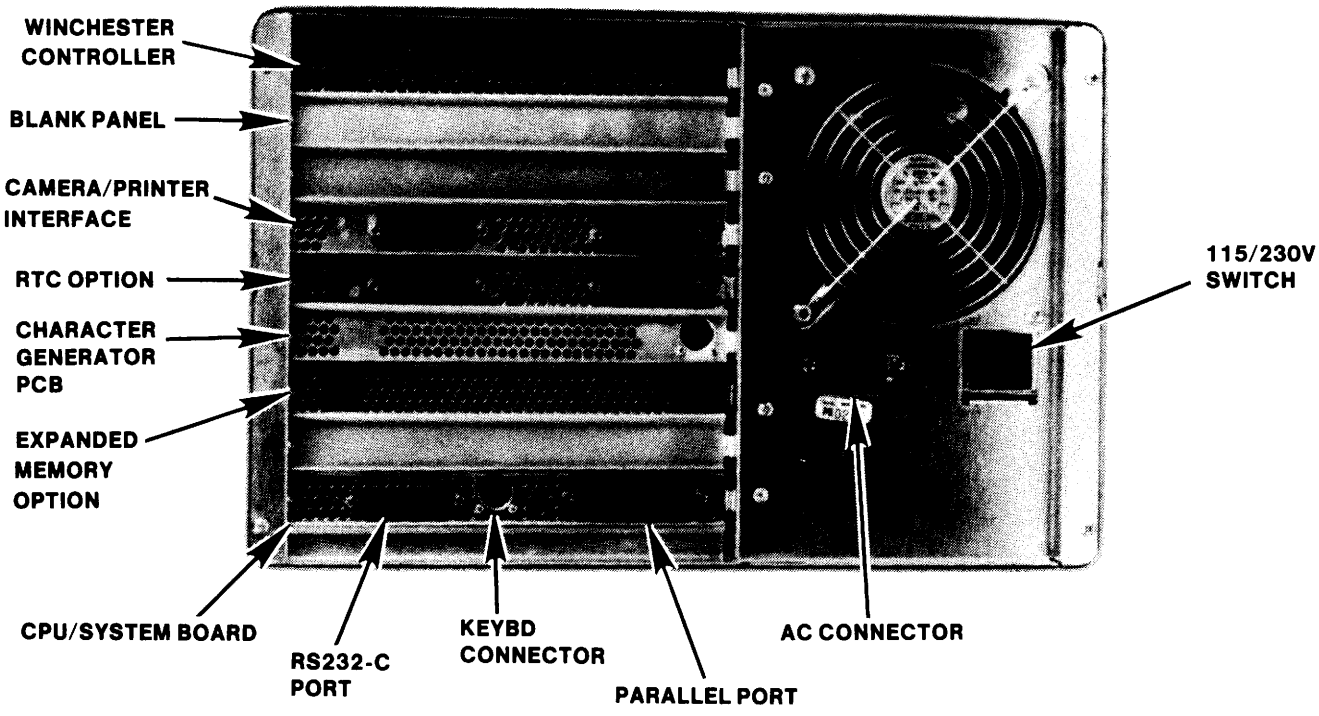


Figure 4-4. Expanded Chassis Electronics Base Unit

4.6.2 Expanded Chassis Base Unit (Internal view)

The Electronics Unit with the cover removed is shown in Figure 4-5. This illustration shows the Expanded Chassis PC in the vertical position.

Access to the internal chassis of the base unit is accomplished by laying the base unit on its side with the air vents pointing downward and removing the four screws from the rear panel (2 screws on each side). Carefully stand the Electronics Unit on its rear panel and lift the enclosure cover up and off of the unit. Set the cover to the side and place the Electronics Unit in the Vertical position with the power supply down.

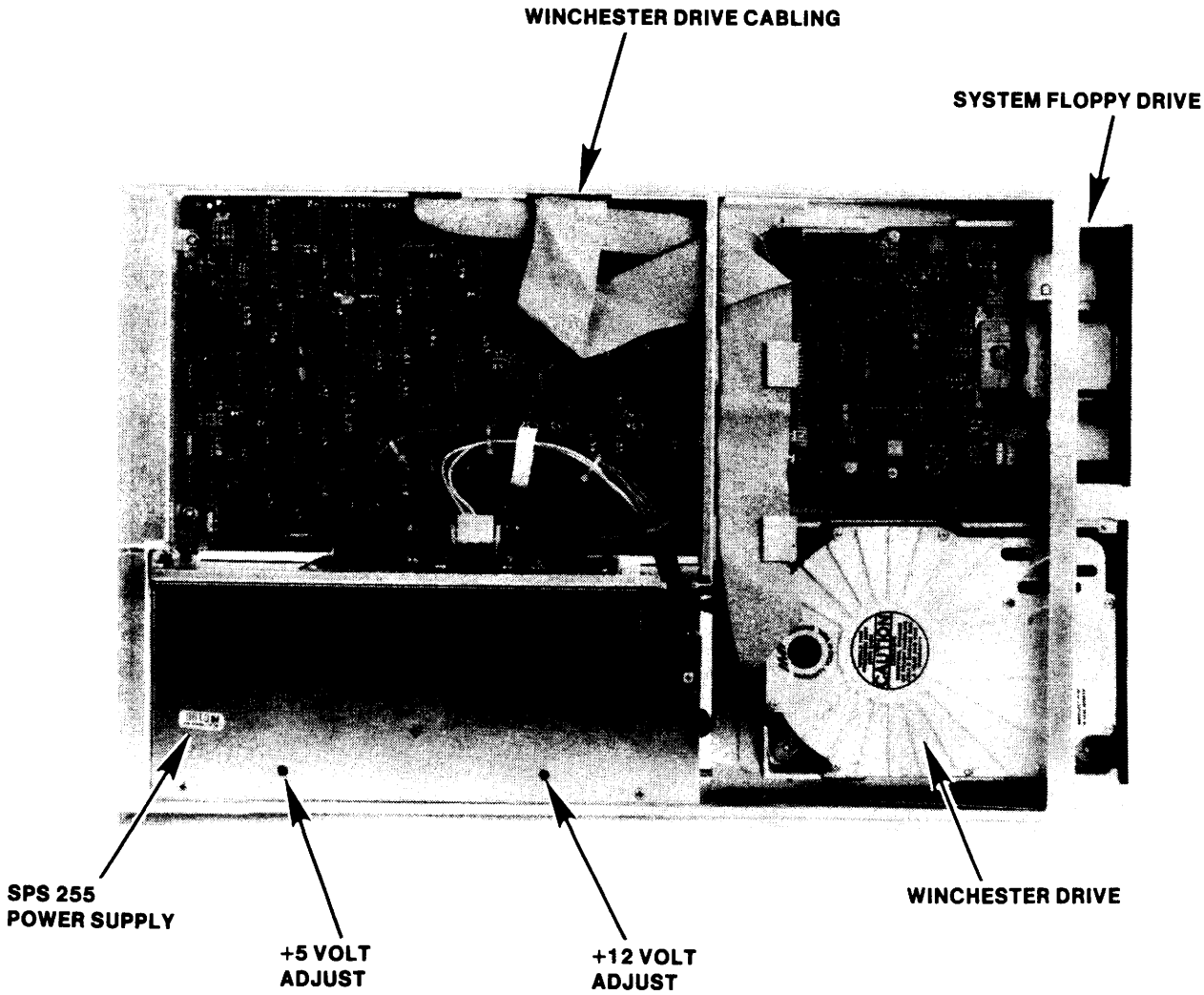


Figure 4-5. Expanded Chassis Base Unit with Cover Removed

4.6.3 SPS255 Power Supply (270-0890)

The SPS255 power supply is unique to the Expanded Chassis PC. This power supply can not be interchanged with the power supply used in the 5-slot PC.

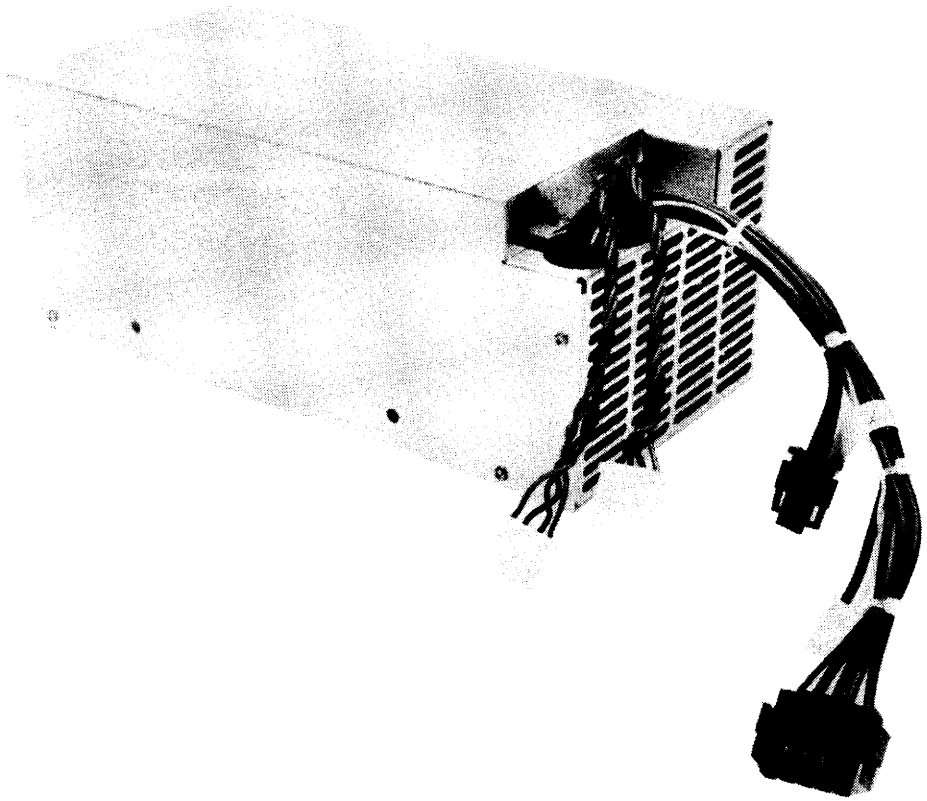
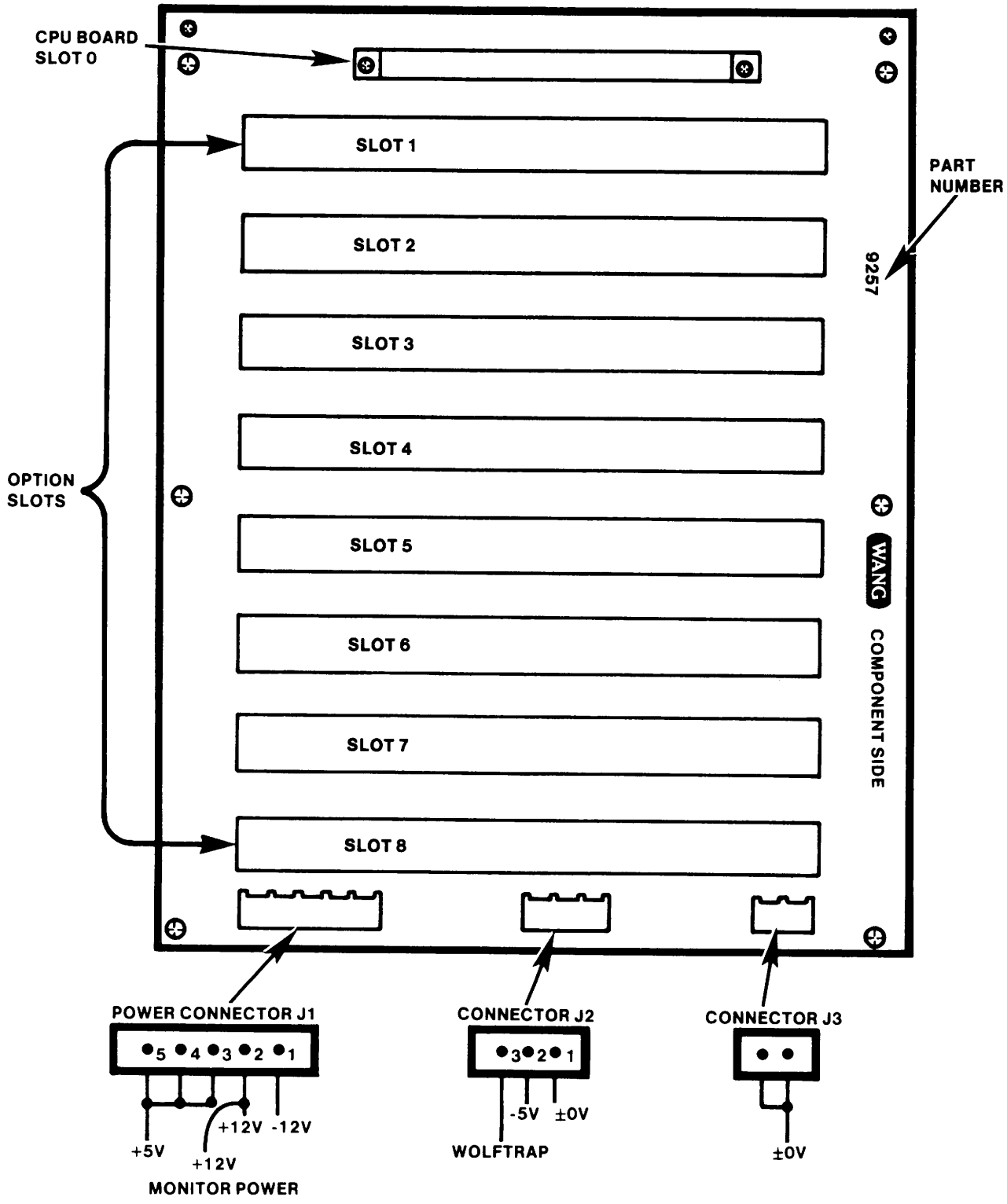


Figure 4-6. SPS255 Switching Power Supply (270-0890)

4.6.3 Motherboard (210-9257)

The Motherboard (9257) is unique to the Expanded Chassis PC. This PCA is not interchangeable with the 5-slot PC due to physical differences. Both Motherboards are electrically compatible.



4.7 SWITCH SETTINGS

Before powering-up the System, ensure that the switch settings are set as described below. There are two switch settings that should be checked. These are:

SW1 Located on the CPU/System Board
115V/230V Switch located on the Switching Power Supply (accessible through cut-out provided in rear of chassis)

4.7.1 CPU/System Board Switch Setting

The CPU/System Board 4-Position DIP Switch SW1 is the Baud Rate Default Select for RS232 Asynchronous communications. The Baud Rate is software selectable and can override the Default Switch setting. This switch should be set according to the Baud transmit rate as determined by the protocol used. Refer to the Professional Computer manual for switch location and baud rate selection.

4.7.2 115/230V Switch Setting

Located on the Power Supply (accessible through a cut-out provided in the rear of the chassis, refer to Figure 4-8) is the 115V/230V Voltage Select Switch SW1. This switch should be checked for the proper setting dependent upon the input voltage level. Use the blade of a screwdriver to change voltage setting if required. This switch has two setting, these are:

115V showing denotes 115V ac power source input.
230V showing denotes 230V ac power source input.

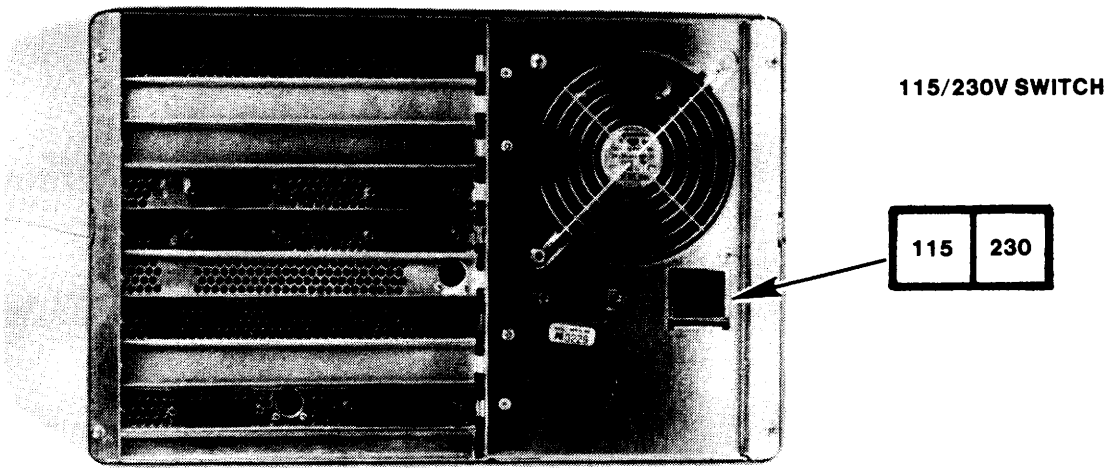


Figure 4-8. 115V/230V Switch Location

4.8.1 System Unit Installation

Ensure that the Electronics unit contains all the PCBs that are required for operation of your system configuration. The Medium Resolution Character Generator board 210-8645 must be installed if the monochrome monitor is used.

4.8.2 Connecting the Keyboard

Locate the keyboard connector on the back panel of the Electronics Unit labeled J3. See Figure 4-4. Connect the plug on the end of the keyboard cable to the keyboard connector located on the back panel. The Keyboard connector and the Keyboard cable plug are DIN connectors allowing the plug to be installed in only one way. Be sure to align the pins in the plug to the connector to prevent damaging either of the two.

4.8.3 Connecting the Monitor Cable to the Electronics Unit

The Character Resolution board 210-8243/8343 has two connectors on it as shown in Figure 4-4. This card can be installed in any one of the eight slots within the electronics unit and not necessarily where shown.

Locate the two connectors at the end of the monitor's cable. Connect the Video plug (8-pin) into the 8-pin DIN connector located on the Medium Character Resolution board. Connect the Voltage plug (3-pin) into the bottom connector labeled J2 on the Medium Character Resolution board.

4.8.4 Connecting the AC Power Cord

```
**********************************************************
*                      CAUTION                           *
*                                                        *
*  BEFORE CONNECTING THE AC POWER CORD, BE SURE THE      *
*  POWER SUPPLY ASSEMBLY IS SET FOR THE APPROPRIATE      *
*  VOLTAGE RATING AS DESCRIBED IN PARAGRAPH 4.7.2.       *
*                                                        *
**********************************************************
```

Connect the 12 foot ac power cable to the three prong ac power connector located on the rear of the Electronics Unit. See Figure 4-4. Secure the power cord to the back panel by screwing the two flathead screws to the posts on each side of the power cord connector. BE SURE THAT THE ON/OFF SWITCH LOCATED ON THE FRONT OF THE ELECTRONICS ENCLOSURE IS OFF (O) POSITION. Connect the three prong ac plug into an ac wall receptacle to complete the installation.

The monitor and the keyboard are now connected to the electronics unit. The power switch (RED) located on the electronics unit controls the power sent to all three components. As a result, whenever you Power-On the Electronics Unit both the Monitor and the Keyboard are also powered-on.

4.8.5 Connecting the Monitor Cable to the Monitor

Two connectors are located on the left rear underside of the monitor case. One is the TTL Video, the other is the monitor power DIN connector. Refer to Figure 4-9. Connect the Video plug into the video connector. Connect the other plug (Voltage) into the power connector. Both connectors are keyed allowing the plugs to be installed in only one way.

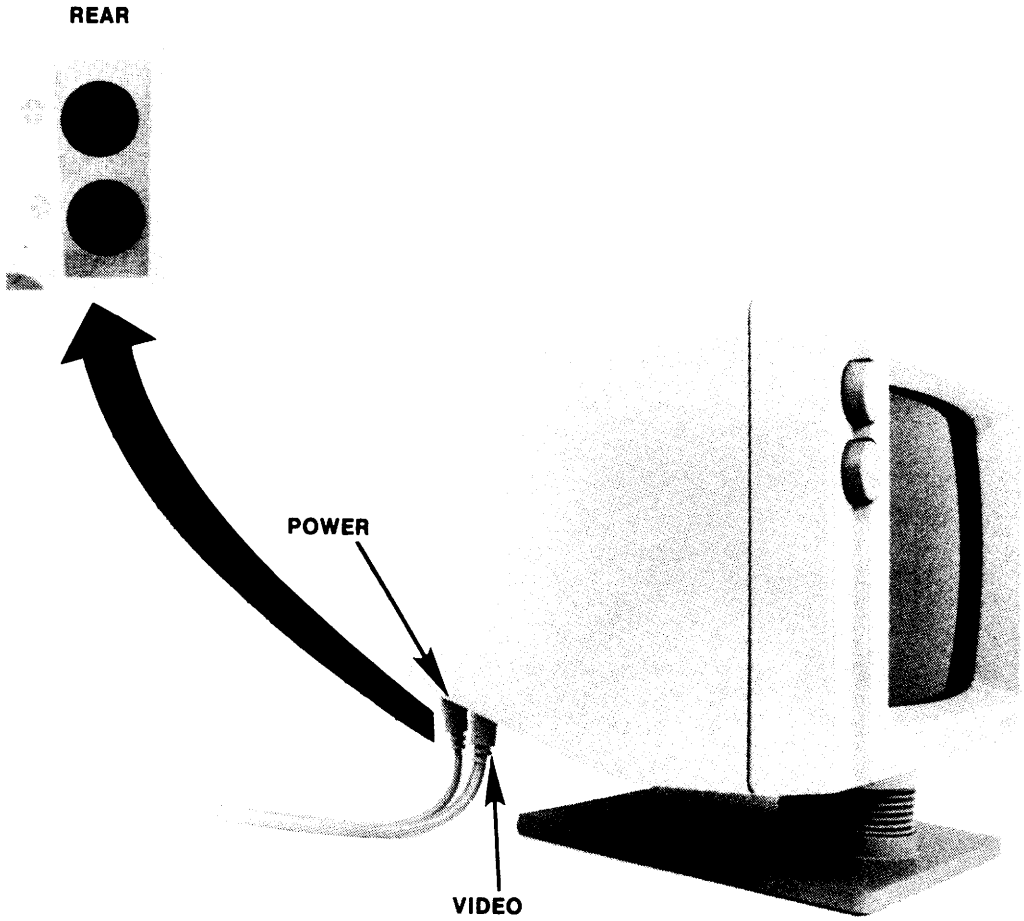


Figure 4-9. Connecting the Monitor's Cables

4.9 SYSTEM EXPANSION

The Expanded Chassis PC system can be expanded in two ways; the addition of Option PCBs and the addition of a second diskette drive (Drive B) or a Winchester Drive (Drive C). System expansion for the Expanded Chassis PC is performed the same as for the 5-slot PC. Refer to the Professional Computer manual for system expansion procedures. Note that 8 option slots are available within the Expanded Chassis PC.

4.10 SYSTEM POWER-ON

```
**********************************************************
*                      CAUTION                           *
*                                                        *
* BEFORE LOADING ANY DISKETTES, ENSURE THE SHIPPING      *
* PROTECTOR(S) ARE REMOVED FROM THE FLOPPY DRIVE(S).     *
*                                                        *
**********************************************************
```

Power-On the System by moving the power switch to the On (1) position.

When power is first applied, the System Unit's fan starts, a short beep will sound, the Boot PROM diagnostics will run, and the Keyboard LEDs will flash on.

Now, load the System diskette into Drive A. To load the diskette, open Drive A's door and slide in the System diskette. Be sure the recording slot of the diskette goes into the drive first. Use the Insert and Up arrows on the orientation label to confirm that the positioning of the diskette is correct as you insert it in the drive. Slide the diskette completely into the drive and close the drive's door.

After a short time, the Floppy's LED will illuminate and the system will execute the IPL (Initial Program Load). If your system is operating correctly, the indicator lights will all go off after ten seconds to a maximum of 30 seconds (depending on the options installed) and the start-up display message will appear on the screen as shown below.

```
WANG PROFESSIONAL COMPUTER REV x.xx

01 WILL START FROM DRIVE A
```

When this is displayed, a BEEP will be emitted from the keyboard. The beep informs the operator that operator intervention is now possible. If there is no operator intervention, then after a five (5) second delay the following will be displayed and the system will now attempt to load from drive A.

```
WANG PROFESSIONAL COMPUTER REV x.xx

01 WILL START FROM DRIVE A

02 STARTING FROM DRIVE A
```

During the 5 second delay (after the beep is heard), the operator can perform one of five operator options. These are:

- o Depress the "P" key
- o Depress the "G" key
- o Depress the "D" key
- o Depress the "Q" key
- o Depress the "M" key

Depressing the "P" key prompts the system to Re-IPL. If this key is depressed, the system will again run the power-up diagnostics and the start-up message will be displayed.

Depressing the "G" key prompts the system to proceed to load the software without waiting for the delay.

Depressing the "D" key prompts the system to re-direct the start to a different drive device. When this key is depressed the following is displayed:

```
:D
03 RE-DIRECT START
:_
```

Enter the new drive device nomenclature (B or W if previously started from Drive A).

To re-direct to Drive B, type in "B" and depress the "RETURN" key. The system will now attempt to load the system software from Drive B.

To re-direct to the Winchester, type in "W" and the decimal slot identification (ID) number the Winchester Controller board is located in (08 for expanded chassis), then depress the "RETURN" key (see example). The system will now attempt to load the system software from the Winchester.

Example: With the Winchester Controller PCB located in slot 8, enter:

W08 "RETURN"

Depressing the "Q" key executes a warm start. A warm start is the system Re-IPL without running power-up diagnostic. The warm start is further discussed in paragraph 4.11.

Depressing the "M" key displays the following Diagnostic Menu:

```
1 - RECAL
2 - CYL 1
3 - CYL 16
4 - CYL 40
5 - RS232 LOOP
6 - RE-RUN BIT
```

To return to the start-up menu depress the number "6" key to rerun the power-up diagnostic.

If the message in Figure 4-10 is displayed, this means that the computer can not do anything until the System Software is loaded. Ensure the System Diskette is installed in Drive A. Then depress the "R" key. The system will now attempt a Re-try (Re-IPL).

```
WANG PROFESSIONAL COMPUTER REV x.xx

*** 40 NO AUTO-START DEVICE
:_
```

Figure 4-10. The Non-Start Display

The System Software diskette contains all of the files that are necessary to start the system including the operating system and System Menu programs. In order to start the system you must use the System Software diskette or a diskette that has the system files on it. If another diskette is used the system will display the following message on the Monitor:

```
WANG PROFESSIONAL COMPUTER REV x.xx

01 WILL START FROM DRIVE A

02 STARTING FROM DRIVE A

***41 START FAILED
   71 DRIVE A NO WANG START TRACK
   :_
```

If this situation occurs, remove the disk in Drive A (or the selected default drive) and insert the system diskette. Depress the letter "R" key to re-IPL the system.

NOTE

DRIVE A IS THE START-UP DEFAULT DRIVE UNLESS A WINCHESTER IS IS INSTALLED AND NO DISK IS IN DRIVE A. THE SYSTEM ASSUMES DRIVE A TO BE THE DEFAULT DRIVE UNLESS THE INSTRUCTIONS FOR THE DEFAULT DRIVE ARE ALTERED THROUGH THE SYSTEM UTILITIES MENU -- SET DEFAULT DRIVE.

The Time and Date screen below will appear automatically every time you start your system with the System Software diskette. To set the date and time simply fill in the information, the correct format is automatically provided. Once the time and date is set, an organizational and historical record of the files on that particular diskette is recorded. Depressing the "HELP" key will give an explanation of how to set the time and date.

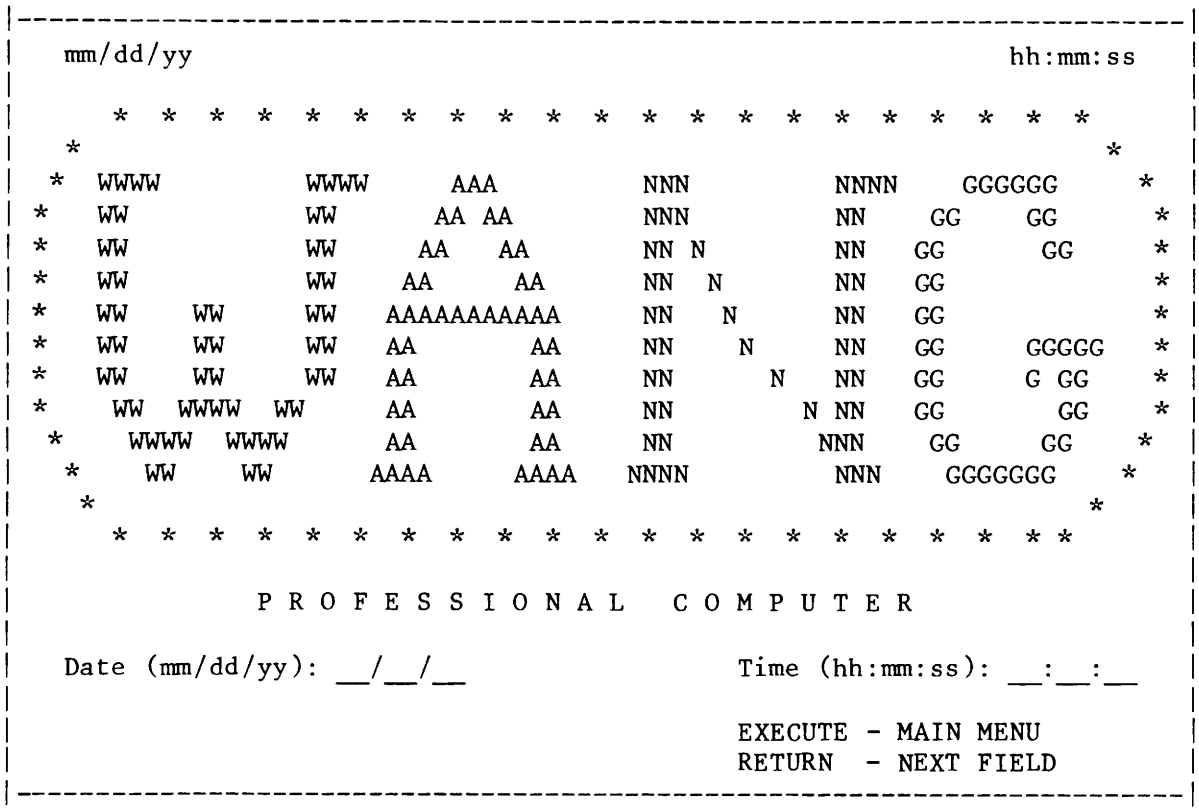


Figure 4-11. The Date and Time Screen

However, the time and date does not have to be set each time you start the system. Note: If the time and date is not set, the file creation date recorded defaults to 01/01/XX. If the time and date are not to be set depress the "EXECUTE" key to proceed to the Main System Menu as shown in Figure 4-12.

NOTE

FOR THE PURPOSE AND CLARITY OF THIS MANUAL, SOFTWARE RELEASE LEVELS ARE DENOTED x.x. THE ACTUAL RELEASE LEVEL DISPLAYED DENOTES THE LEVEL OF SOFTWARE BEING RUN. THE SYSTEM SCREEN LOADS DISPLAYED ARE SYSTEM SCREENS AS OF THIS WRITING, ACTUAL SCREEN LOADS MAY VARY PER CUSTOMER.

```
mm/dd/yy          Wang Professional Computer          hh:mm:ss
                M A I N   S Y S T E M   M E N U
                          Release x.x

Select an Item and Proceed

                    _ Applications
                    _ Conversion Aids
                    _ System Utilities
                    _ Program Development
                    _ Communications
                    _ DOS Command Processor
                    _ Other

                                  SPACE BAR - Item Select
                                  EXECUTE   - Proceed
```

Figure 4-12. The Main System Menu Display

4.11 SYSTEM RESTART (Warm Start)

The System can be restarted (Warm Started) by reinserting the System Software diskette in Drive A (if removed) and depressing the following keys:

Hold down the "2ND" key and depress the "COMMAND" key.
Release both keys, then depress the "CANCEL" key.

This results in the system running the IPL sequence without running the power-up diagnostics.

4.12 MAIN SYSTEM MENU OPTIONS

Various menus can be displayed when properly selected from the Main System Menu. The Main System Menu is shown in Figure 4-12. By positioning the acceptance block to the option you want and depressing the "EXECUTE" key, that menu will be appear on the screen.

A definition of a menu option is obtainable by positioning the acceptance block (using the SPACE BAR) to the option you want and depressing the "HELP" key.

The option selected will be described on the HELP screen. To return to the previous menu from the Help Screen, press the "CANCEL" key. Refer to the Wang PC Introductory Guide 700-7590 for applications of the various menu options.

4.13 POWER-UP DIAGNOSTIC

The Power-Up diagnostics perform the same function for the Expanded Chassis PC as for the 5-slot PC. Refer to the Professional Computer maintenance manual for error definitions and diagnostic test available.

CHAPTER 5
PREVENTIVE AND CORRECTIVE MAINTENANCE

5.1 PREVENTIVE MAINTENANCE

No scheduled preventive maintenance is required for the Expanded Chassis Professional Computer.

5.2 CORRECTIVE MAINTENANCE

The Corrective Maintenance section provides information pertaining to the electrical and mechanical adjustments of the expanded chassis PC. The mechanical adjustments are the same as for the 5-slot PC. Mechanical adjustments are not included in this addendum. Refer to the PC Maintenance manual for all mechanical adjustments.

5.2.1 Special Tools

No special tools are required to perform corrective maintenance on the expanded chassis PC. All maintenance performed can be accomplished with the Wang Standard Tool Kit WLI P/N 726-9401.

5.3 ELECTRICAL ADJUSTMENTS

The SPS-255 Power Supply is a switching power supply which is a completely enclosed unit. Two field adjustments (other than setting the 115/230v input voltage select switch) can be made on the power supply assembly, +5 volts adjust and +12 volts adjust. The Power Supply Unit contains EXTREMELY DANGEROUS VOLTAGE AND CURRENT LEVELS, CAUTION should be exercised when adjusting and/or taking measurements.

A Power Distribution and Interconnection Diagram is contained in Figure 5-1. This figure will be referenced within the preceding text.

5.3.1 Electrical Measurements, Checks and Adjustments

There are four voltage levels that can be checked. These are:

+5 Vdc $\pm$ 0.25 volts
-5 Vdc $\pm$ 0.25 volts
+12 Vdc $\pm$ 0.6 volts
-12 Vdc $\pm$ 0.6 volts

The +5 volts and the +12 volts output are field adjustable. The +5 volts must be adjusted first, then the +12 volts can be adjusted. These voltages must be checked/adjusted from inside the Electronics Enclosure. Refer to paragraph 5.3.1 System Unit Disassembly for enclosure removal.

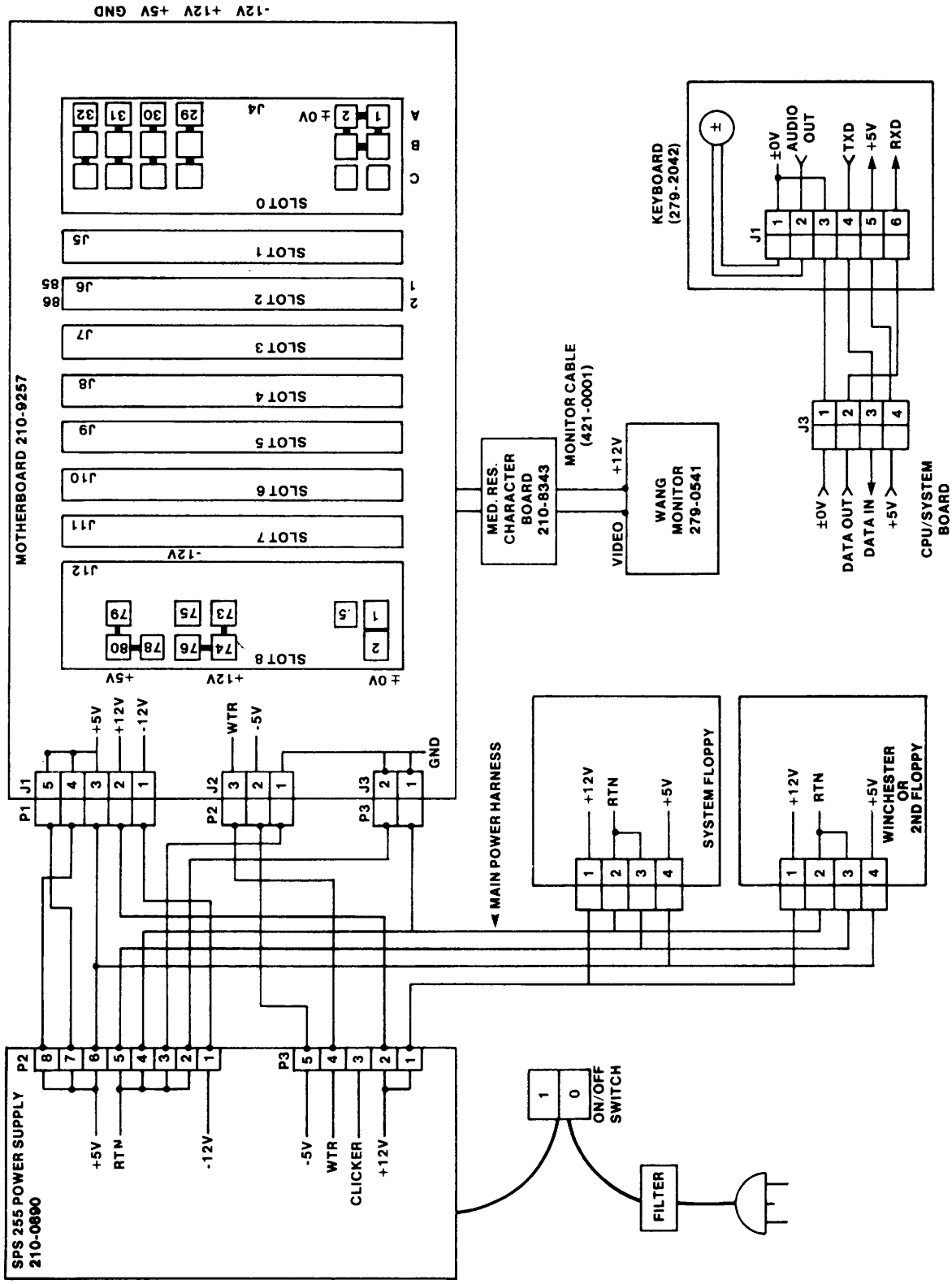


Figure 5-1. Power Distribution and Interconnection Diagram

After the enclosure cover is removed, locate the motherboard located near the Switching Power Supply. Using a digital voltmeter measure the following voltages. See Figure 5-1 for power distribution and connector locations.

Voltmeter setting:

20 Volt Scale dc

Table 5-1. Voltage Adjustment/Measurement Table

Voltage	Test Point Leads Positive	Negative	Voltage Level
+5 Vdc	P1 Pin 3	P3 Pin 1	+5 ± .25 (adjustable)
-5 Vdc	P2 Pin 2	P3 Pin 1	-5 ± .25
+12 Vdc	P1 Pin 2	P3 Pin 1	+12 ± .60 (adjustable)
-12 Vdc	P1 Pin 1	P3 Pin 1	+12 ± .60

5.3.2 Measurement/Adjustment Procedure

a. +5 Volt

( ) Place the red lead (positive) on the Motherboard connector P1 pin 3. Place the black lead (negative) on the Motherboard connector P3 pin 1. Read the voltage level displayed, it should be +5 Volts ± .25. If the voltage is out of adjustment, using a non-metalic screwdriver adjust the +5 adjustment to bring it into tolerance. See figure 5-2 for adjustment location.

b. -5 Volt

( ) Place the Red lead (positive) on the Motherboard Connector P2 pin 2. Place the black lead (negative) on the Motherboard connector P3 pin 1. Read the voltage level displayed, it should be -5 Volts ± .25V.

c. +12 Volt

( ) Place the Red lead (positive) on the Motherboard connector P1 pin 2. Place the black lead (negative) on the Motherboard connector P3 pin 1. Read the voltage level displayed, it should be +12 Volts ± .6V. If the voltage is out of adjustment, using a non-metalic screwdriver adjust the +12 adjustment to bring it into tolerance. See figure 5-2 for adjustment location.

d. -12 Volt

( ) Place the Red lead (positive) on the Motherboard Connector P1 pin 1. Place the black lead (negative) on the Motherboard connector P3 pin 1. Read the voltage level displayed, it should be -12 Volts ± .6V.

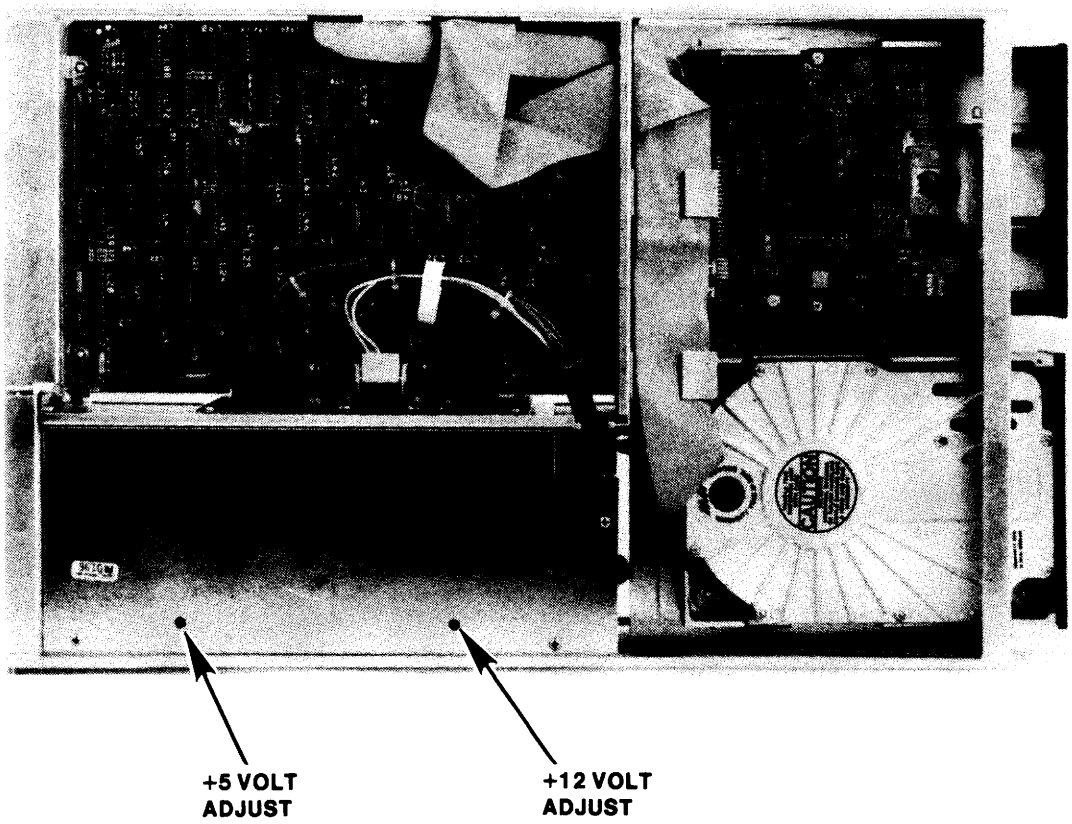


Figure 5-2. Expanded Chassis Switching Power Supply Adjustment Locations

If any voltage is missing or the +5 and/or +12 volts can not be adjusted, remove all PCB boards (refer to paragraph 5.x.1 Option board removal) and perform the adjustment procedure again. If the voltage can be adjusted, one or more PCB board is causing the problem. Re-insert the PCBs into the motherboard one at a time until the defective board is found. Replacement of the defective board is required.

If the voltage problem exist with no PCB boards installed, replacement of the Switching Power Supply is required. Refer to the Removal and Replacement procedure as described in paragraph 5.3.1.1.

5.4 REMOVAL AND REPLACEMENT PROCEDURES

The Removal and Replacement procedures will enable the AFET to remove and replace defective units to the Field Repair level.

5.4.1 System Unit Disassembly

1) Turn the Power Switch (labeled I/O located on the front panel) to the OFF (0) position. Disconnect all the cables (ie. ac power cable, keyboard cable, monitor cable, etc) from the rear of the System Unit.

2) Position the System Unit horizontally (air vents pointing down) and remove the four Phillips-head screws from the rear panel. (see Figure 5-3).

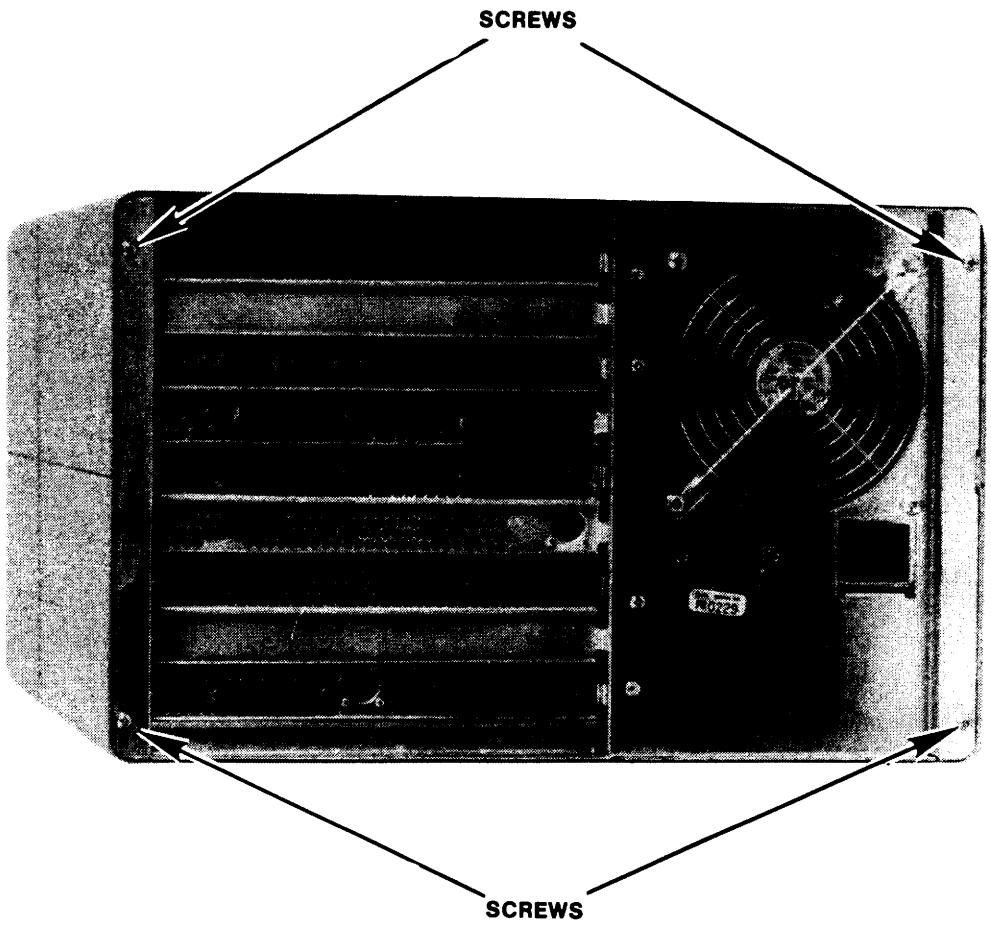


Figure 5-3. System Unit Cover Removal

3) Carefully stand the Electronics Unit on its rear panel and lift the enclosure cover up and off of the unit. Set the cover to the side.

4) Now set the Electronics Unit in the Vertical position (see Figure 5-4) with the power supply down and carefully remove the System Floppy Drive ribbon cable from the top left connector J5 and remove Drive B ribbon cable (if any) from connector J6 located on the 8221 CPU/System board. Pull enough ribbon cable slack to move the connectors out of the way.

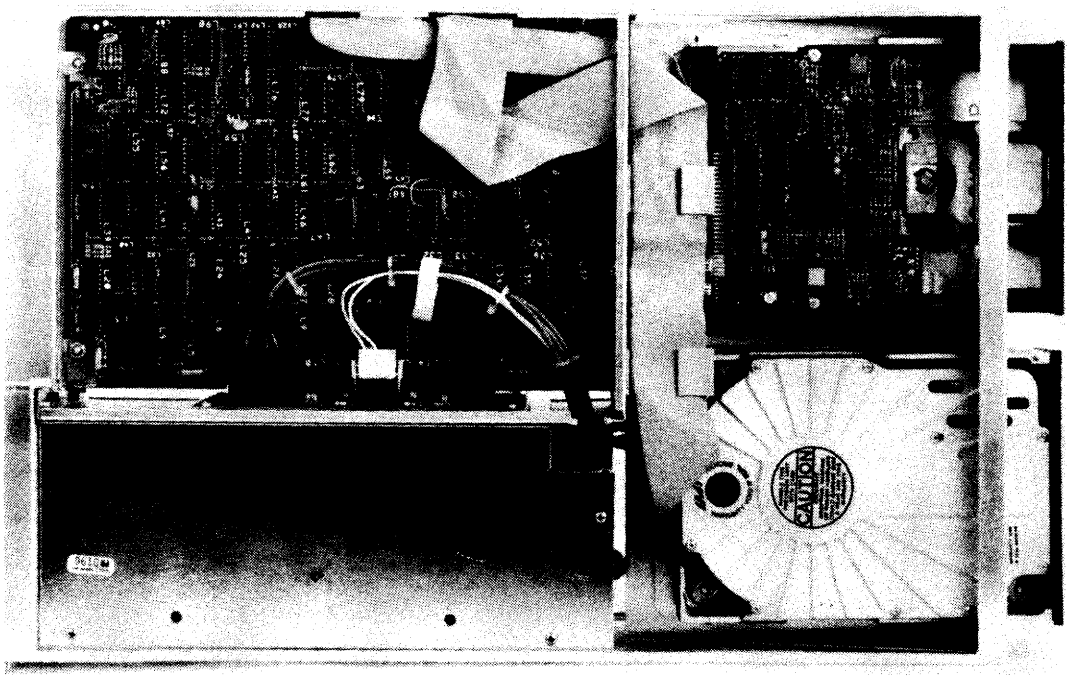


Figure 5-4. Electronic Unit in Vertical Position

5) Remove the Phillips head screw from the RF shield that secures the CPU/System board into the motherboard. Remove the CPU/System board by placing your fingers between the CPU/system board and the top of the power supply. Push up on the CPU/system board in order to free it from the motherboard connector. Carefully pull the CPU/System board up until it clears the card guides. Be sure the floppy drive ribbon cables are out of the way to prevent the cables from being damaged.

6) To install a CPU/System board, reverse the procedures in steps 4 and 5. Note: When installing the CPU/System Board, ensure the internal ac power cable is not twisted or has any slack. Hold the cable against the chassis with a blunt instrument, such as an unsharpened pencil, to ease installation.

Option Board Removal and Replacement

7) To remove option boards, remove the screw that secures the PCB to be removed in place. Remove the option board by pulling up on one side then the other in order to free it from the motherboard connector. Then slide the option board out of the card guides. Repeat this procedure for other option boards that are to be removed.

8) To install an option board, reverse the procedure in step 7. Ensure the PCB is aligned above the motherboard connector and slides freely in the card guides. The component side of the PCB faces away from the CPU/System board.

5.4.2 Power Supply Removal and Replacement

```
**********************************************************************
*                              CAUTION                               *
*                                                                    *
*  AFTER POWERING DOWN THE UNIT AND DISCONNECTING THE AC POWER       *
*  PLUG FROM THE AC POWER RECEPTACLE,  ALLOW ONE MINUTE BEFORE       *
*  REMOVING THE POWER SUPPLY TO PROVIDE  ADEQUATE TIME FOR ANY       *
*  RESIDUAL VOLTAGE TO DRAIN THROUGH THE BLEEDER RESISTORS.          *
*                                                                    *
**********************************************************************
```

1) Remove the ac cable from the power supply (if not previously removed). With the System unit in the vertical position (power supply down) and the Electronic Unit cover removed, remove the two screws at the rear of the unit that secure the power supply to the system rear panel. Be sure not to remove the two screws that mount the fan guard to the power supply. Remove the screw located on the side of the power supply directly below the non-component side of the system board. A total of three screws must be removed. See Figure 5-5.

2) Remove the main harness assembly connectors from the Motherboard connectors J1, J2, and J3. Remove the main harness connector (power) from the System Floppy Drive and optional floppy drive (if any). Disconnect the ac input to the power supply. See Figure 5-5 for ac input connector.

3) Facing the rear of the unit, slide the power supply and harness assembly to the right and out of the unit. Snake the drive's power cables through the slot provide. Note that the harness assembly is removed with the power supply.

4) Before replacing the power supply, check for the proper voltage switch setting as discussed in Chapter 4 paragraph 4.x.x. To replace the Power Supply, reverse the procedure as describe above.

5) After the power supply is replaced perform the measurement/adjustment procedure described in paragraph 5.2.1.

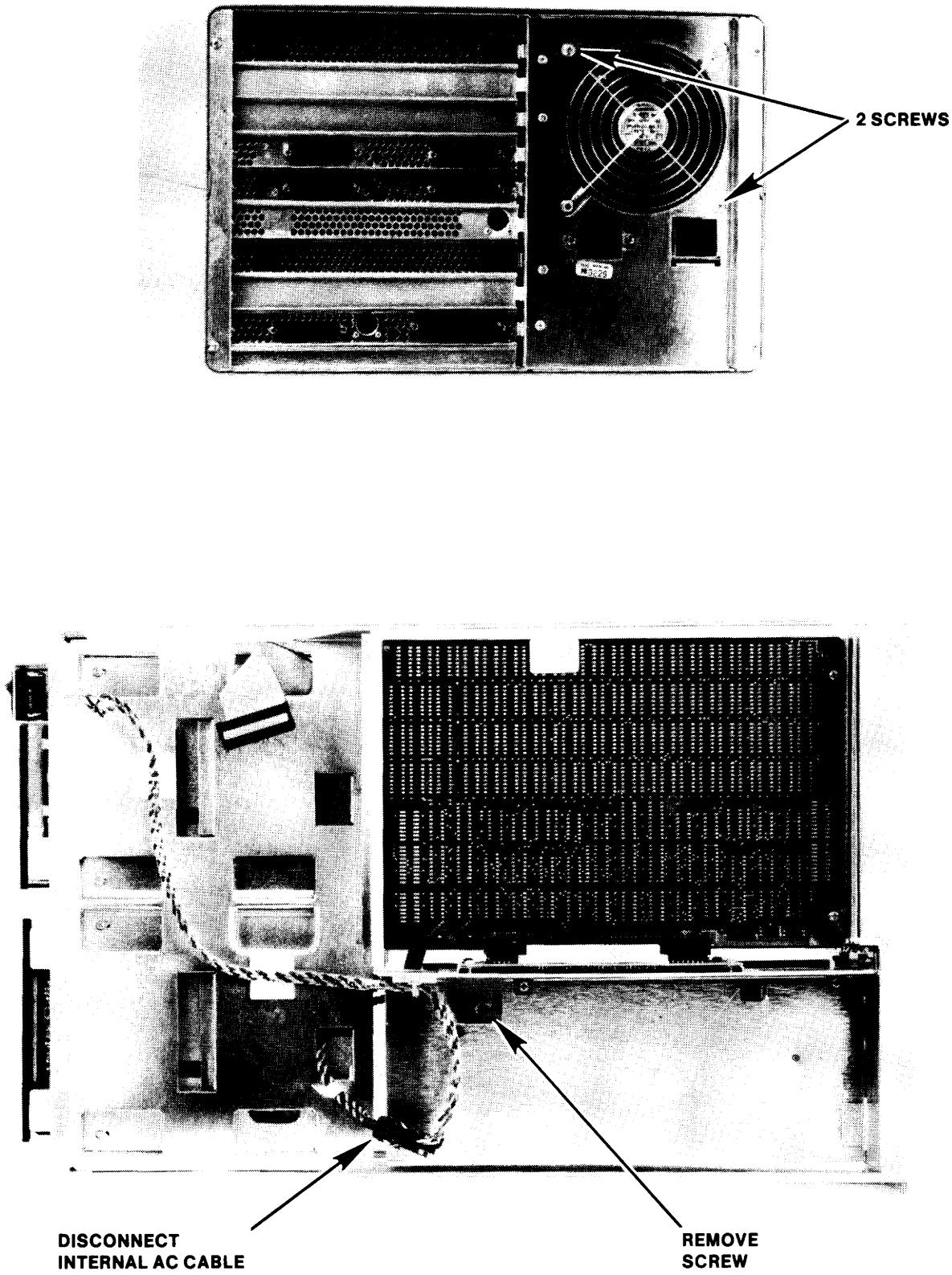


Figure 5-5. Power Supply removal/Replacement

5.4.3 Floppy Drive Removal and Replacement

1) Remove the Electronics Unit cover as described in paragraph 5.5.1 steps 1 thru 3.

2) With the Electronics Unit in the vertical position (power supply down) remove the screw securing the floppy drive to be removed in place. See Figure 5-6.

3) Slide the drive out far enough to enable the removal of the power cable and the ribbon cable. Once removed slide the drive out of the unit.

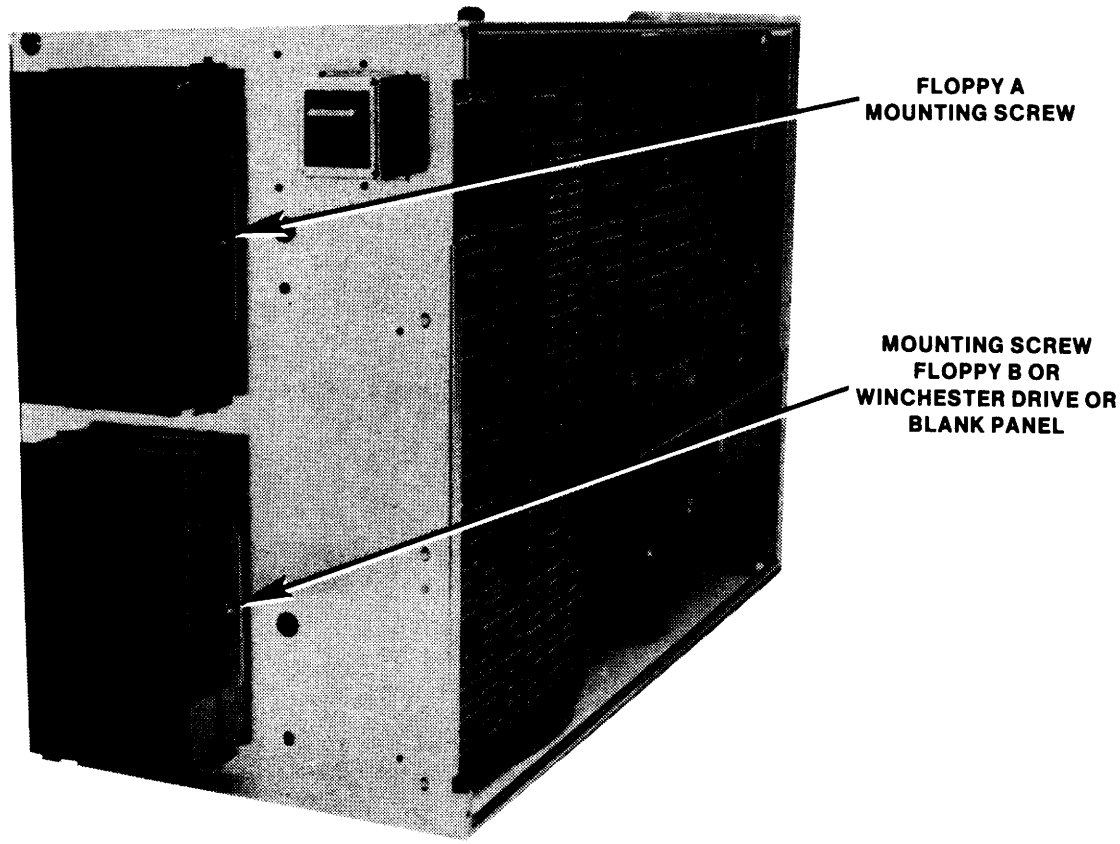


Figure 5-6. Floppy Drive Removal/Replacement Screw Location

4) When replacing the drive, ensure the drive's metal plate is attached. If not, remove the metal plate from the previously removed drive and attach it to the drive to be installed. Four screws secure the drive metal plate to the drive. Ensure all four screws are installed.

5) Ensure the drive's PCB is configured properly, refer to paragraph 4.x.x for the correct configuration in regard to vendor and whether the drive is to be installed in Drive A or Drive B.

6) Slide the drive partially into the System Unit being sure the drives metal plate is sliding in the nylon guide provided. Now reconnect the two cables (power and ribbon) removed in step 3.

7) Slide the drive the rest of the way into the System Unit being careful not to crimp either of the two cables. Secure the drive in place with the screw removed in step 2.

5.5 REASSEMBLY CHECKOUT PROCEDURE

1) Connect the monitor cable and the keyboard cable to the system unit. Connect the ac power cord to the system unit. Ensure the power switch (1/0) is in the Off (0) position and plug the ac power cord into the wall outlet.

2) Power-On the system by position the On/Off Switch to the On (1) position. When power is first applied, the System Unit's fan starts, a short beep will sound, the Boot PROM diagnostics will run, and the Keyboard LEDs will flash on.

3) Now insert the MS-DOS diskette into Floppy Drive A and latch the door closed. After a short time the Floppy's LED will illuminate and the system will execute the IPL (Initial Program Load). After the IPL is completed, the Floppy LED will go out and the Monitor will display the MS-DOS program title and request that the Time and Date be entered. After entering the time and date, the Main Menu will be displayed on the monitor. This denotes a successful power-up.

CHAPTER 6
SCHEMATICS

6.1 SCOPE

The schematics pertaining to the Expanded Chassis Professional Computer are contained in the Professional Computer Schematic Manual WLI part number 729-1241.

CHAPTER 7
ILLUSTRATED PARTS BREAKDOWN

7.1 SCOPE

The following Illustrated Parts Breakdown (IPB) provides reference to assemblies that are identified for maintenance procedures. IPB included in this manual addendum is:

- Figure 7-1. Expanded Chassis Electronics Enclosure

The Part Numbers followed by double asterisk (**) are RSL Items.

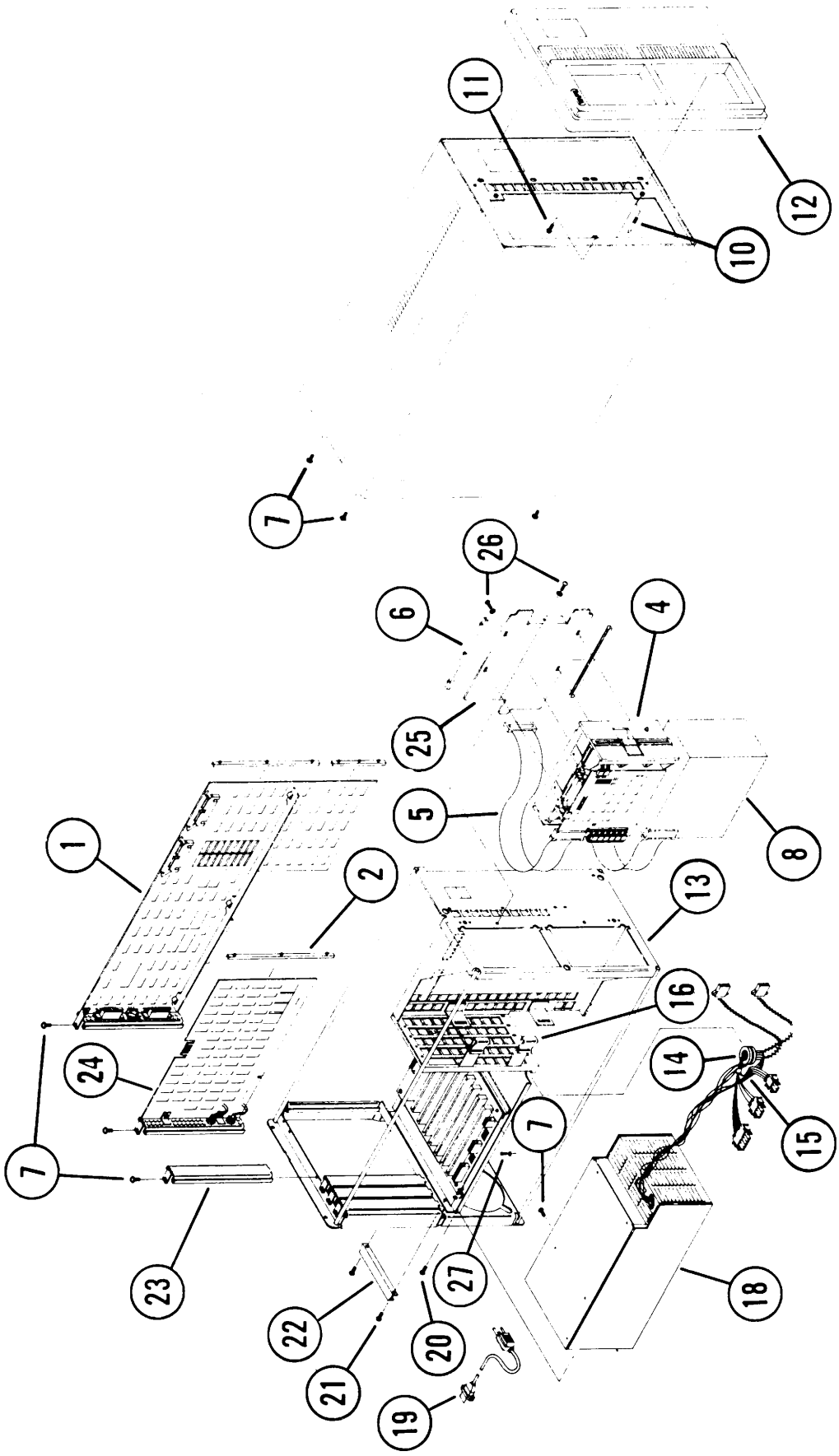


Figure 7-1. Expanded Chassis PC IPB

EXPANDED CHASSIS ELECTRONICS ENCLOSURE (CPU)

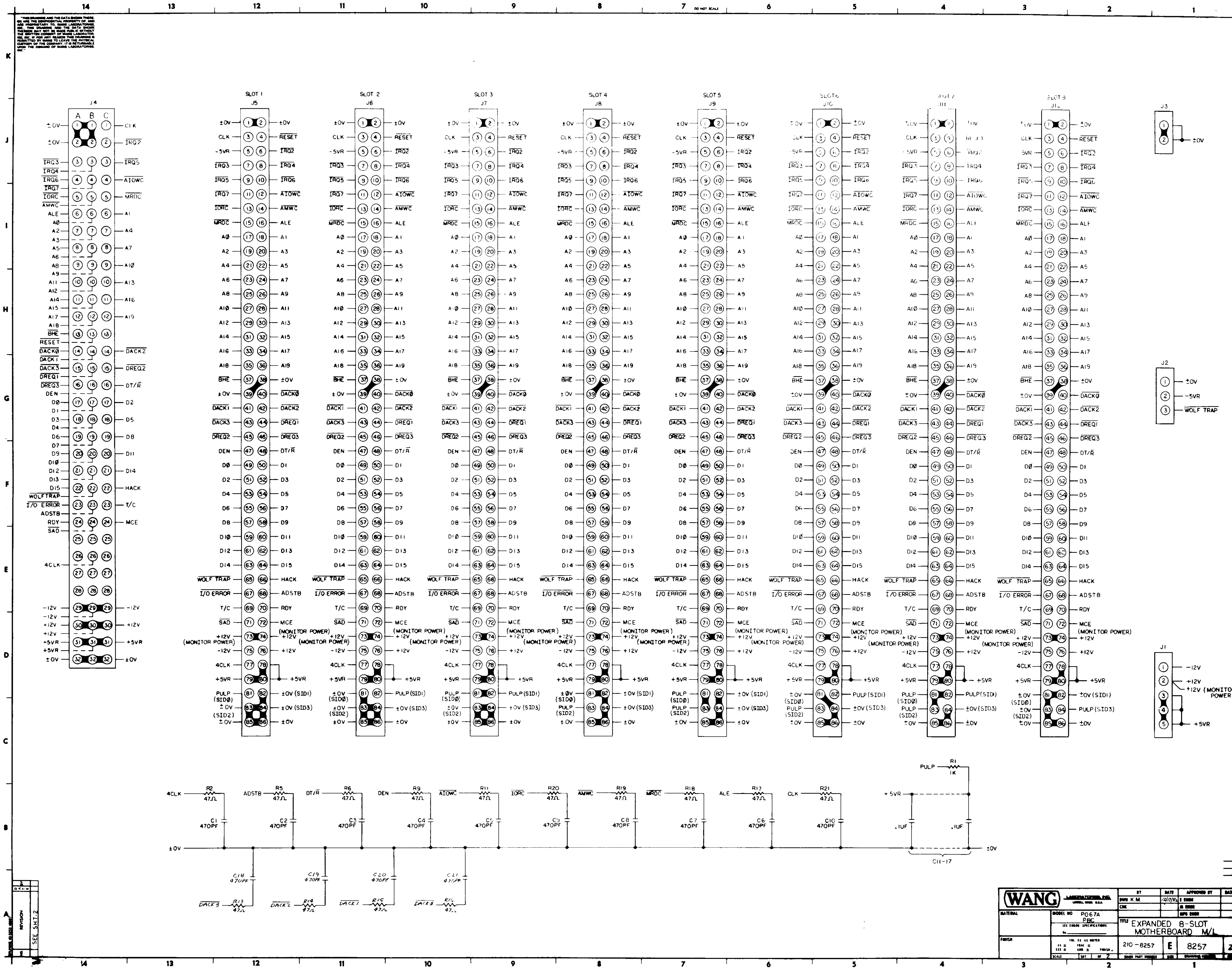
ITEM	PART NO.	DESCRIPTION
1	210-8221-A**	PCA, CPU/MEMORY BOARD
2	465-1243	CARD GUIDE, NYLON WHITE 8 IN.
3	452-4042	CARD GUIDE, NYLON WHITE 4 IN.
4	278-4026**	DISKETTE DRIVE, DSDD 48TPI
5	220-3239**	CABLE, SYSTEM DRIVE (USE WITH ITEM 4)
6	465-1242	CARD GUIDE, NYLON WHITE 6 IN.
7	650-3080	SCREW, 6-32 x 1/4 PAN HD. PHIL.
8	450-0153	BEZEL, BLANK OR
	278-4026**	DISKETTE DRIVE DSDD 48TPI (USE CABLE 220-3240**) OR
	278-4030**	WINCHESTER DRIVE 10MB (USE "A" CABLE 220-3240**)(USE "B" CABLE 220-3238**)
9	458-3323	ENCLOSURE, EXPANDED CPU (WELD)
10	478-0822	PIN GUIDE
11	651-0006	SCREW, #6 SELF TAP 1/2 IN. LONG
12	449-0714-XC	BEZEL, EXPANDED CPU
13	458-3324-XC	CHASSIS, EXPANDED CPU
14	654-1205	GROMMET
15	270-3331	HARNESS ASSY. (INCLUDES ITEM 14)
16	449-0671	CABLE CLAMP
17	210-9257**	PCA, MOTHERBOARD
18	270-0890**	POWER SUPPLY, SWITCHING SPS 255
19	420-2019	POWER CORD
20	651-0070	SCREW, #8 SELF TAP x 5/8 IN.
	653-4000	#8 FLAT WASHER
21	650-3120	SCREW, 6-32 x 3/8 IN.
	653-3000	FLAT WASHER
	653-3001	LOCK WASHER
22	445-9106	HANDLE, CHASSIS PULL
23	452-3009	RF SHIELD, BLANK
24	LISTED BELOW	
25	452-0284	PLATE, MOUNTING DRIVE
26	650-3120	SCREW, 6-32 X 3/8
	653-3000	#6 FLAT WASHER
27	650-3080	SCREW 6-32 X 1/4 PAN HD.
	653-3000	#6 FLAT WASHER

24* LISTED BELOW ARE OPTION BOARDS

210-8222-A**	COLOR AND GRAPHICS BOARD
210-8225-A**	WINCHESTER CONTROLLER BOARD
210-8233**	GRAPHICS DISPLAY ADAPTER
210-8243/8343-A**	CHARACTER DISPLAY ADAPTER
210-8245-A**	LOCAL COMMUNICATIONS BOARD (DATA LINK)
210-8246-A**	LOCAL COMMUNICATIONS BOARD (CPU)
220-3281**	CABLE ASSY FOR LOCAL COMM. BOARDS
210-8248-A**	CP/M-80 EMULATOR BOARD
210-8242**	EXPANDED MEMORY BOARD 128K
210-8242-1**	EXPANDED MEMORY BOARD 256K
210-8242-2**	EXPANDED MEMORY BOARD 512K
210-8232-A**	REMOTE COMMUNICATIONS BOARD
210-8252-A**	X.21 REMOTE COMMUNICATION BOARD
210-8251**	MULTIPORT COMMUNICATIONS CONTROLLER

** DENOTES RSL ITEMS

TABLE OF CONTENTS



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SLOT 2 J6
SLOT 3 J7
SLOT 4 J8
SLOT 5 J9
SLOT 6 J10
SLOT 7 J11
SLOT 8 J12
J1
J2
J3
R2 47Ω
R5 47Ω
R6 47Ω
R9 47Ω
R11 47Ω
R20 47Ω
R19 47Ω
R18 47Ω
R17 47Ω
R21 47Ω
R1 1K
C1 470PF
C2 470PF
C3 470PF
C4 470PF
C6 470PF
C7 470PF
C8 470PF
C10 470PF
C11-17
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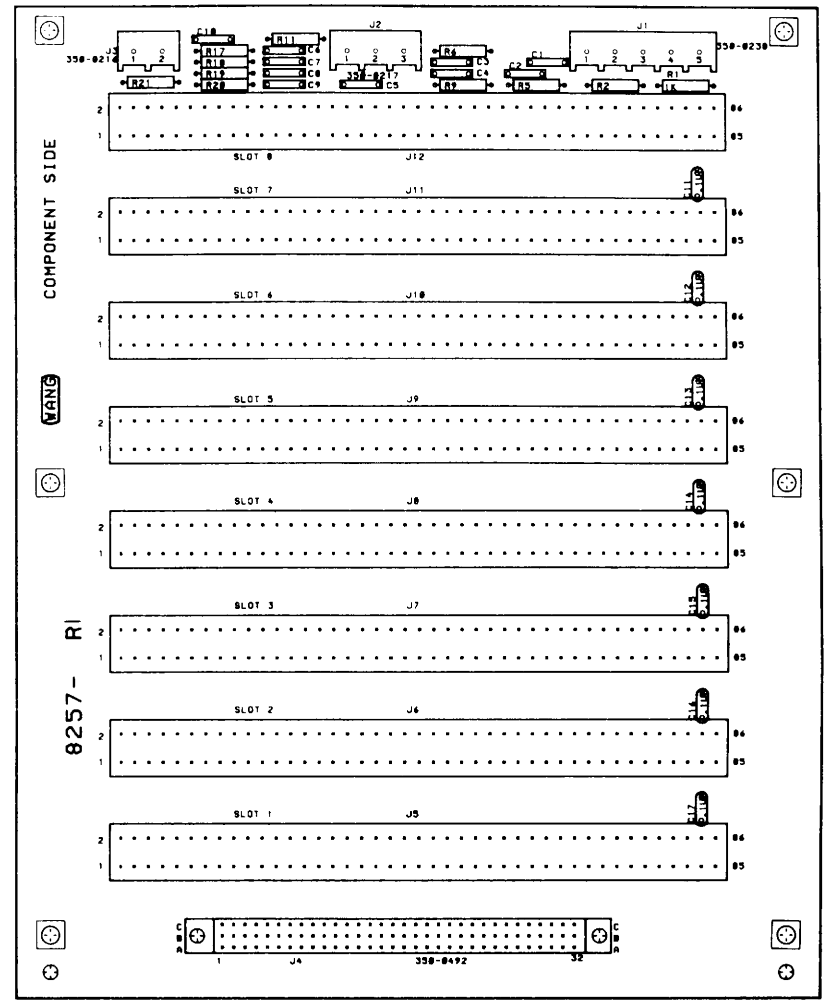
PO67A
PBC
EXPANDED 8-SLOT MOTHERBOARD M/L
DRWN K.M.
210-8257
E
8257
2



COMPONENT	TYPE	WL PART NO
R1	1K 1/4W 5%	330-3011
R2,5,6,9,11,13-21	47Ω 1/4W 5%	330-1048
C1-10	470PF 500V	300-1470
C11-17	.1UF 50V(HF)	300-1930
C18-21	470PF 50V	300-1093
J1	CONN.5PIN	350-0238
J2	CONN.3PIN	350-0217
J3	CONN.2PIN	350-0216
J4	CONN.96PIN	350-0492
J5-12	CONN.86PIN	350-0473

NOTES:
1. ALL RES ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

E-REV 1

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0	ORIGINATED PER DWR#E186 APP'D:	K.M.	12/14/82
1	REVISED PER ECO # 28027 APP'D: 6/1/83	KTH	6/17/83
2	REVISED PER ECO# 29329 APP'D: 9/13/83		9/2/83

WANG LABORATORIES, INC.
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MODEL NO. PO67A PBC
210-8257 E 8257 2
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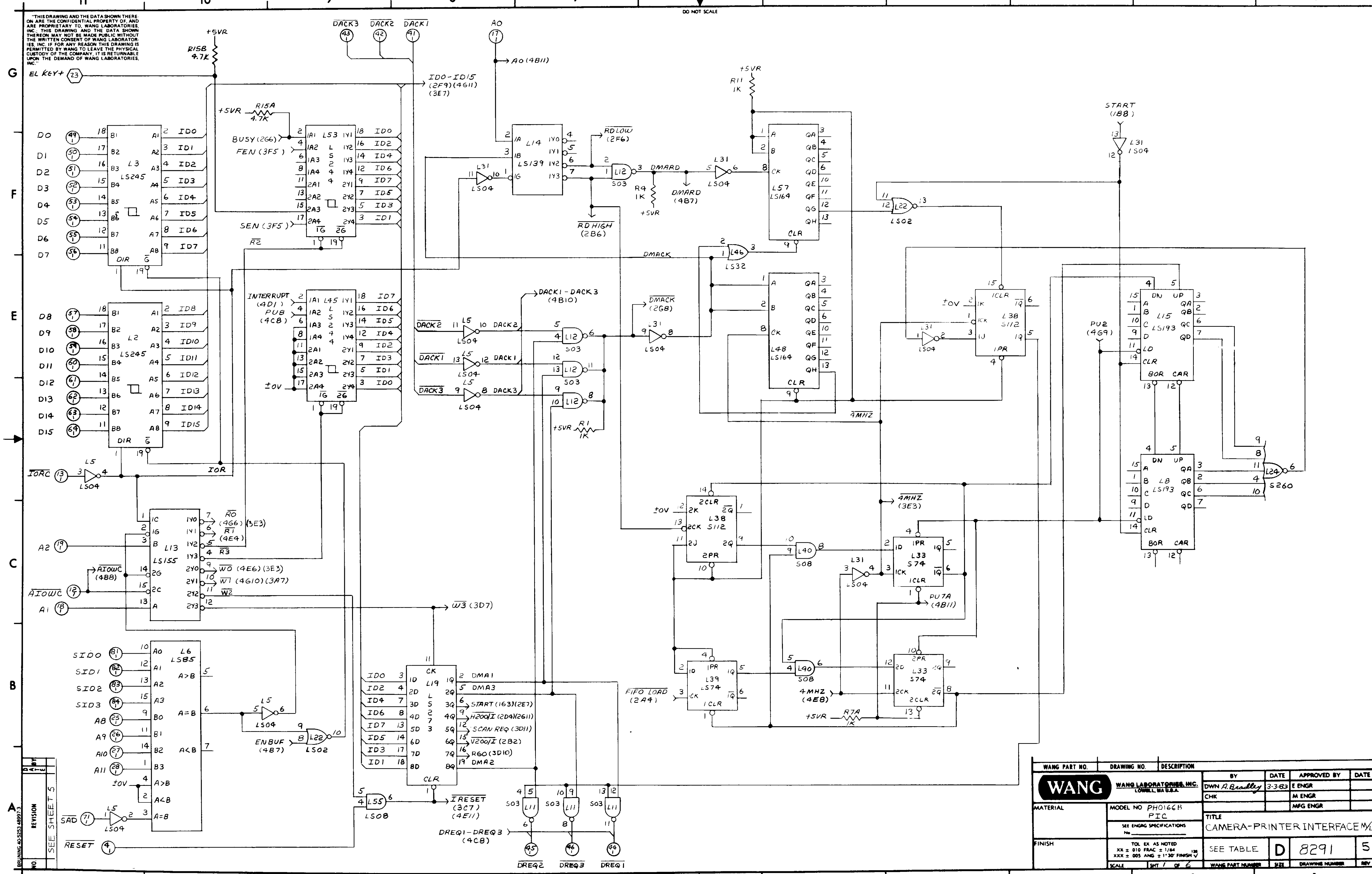
E 8257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DO NOT SCALE
REVISION
SEE SHEET 5
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DWN A. Bradley 3-3-83
TITLE CAMERA-PRINTER INTERFACE M/L
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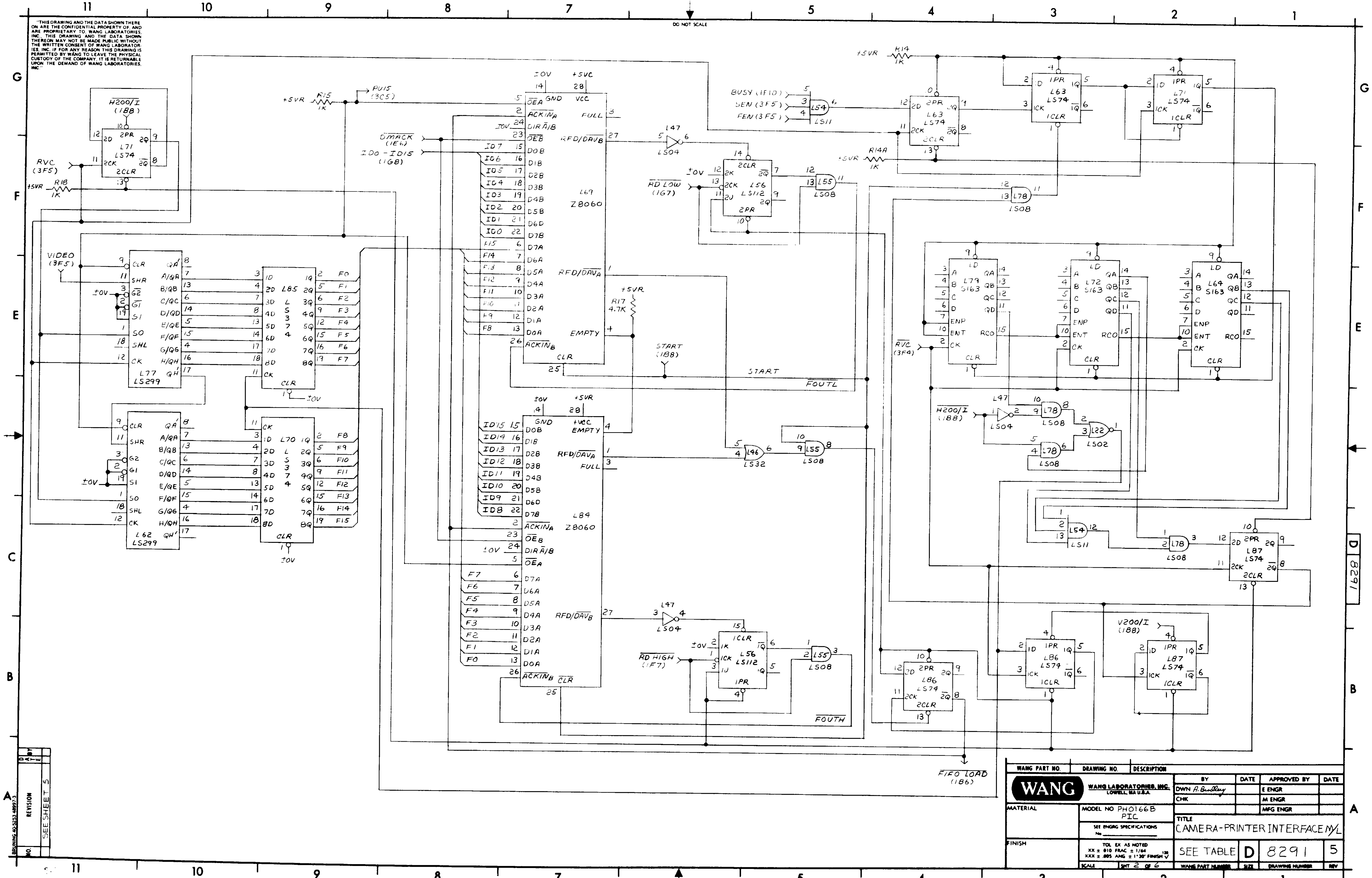

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MODEL NO PHO166B PIC
TITLE CAMERA-PRINTER INTERFACE M/L
SEE TABLE D 8291 5
SHT 2 OF 6
SEE SHEET 5
DO NOT SCALE
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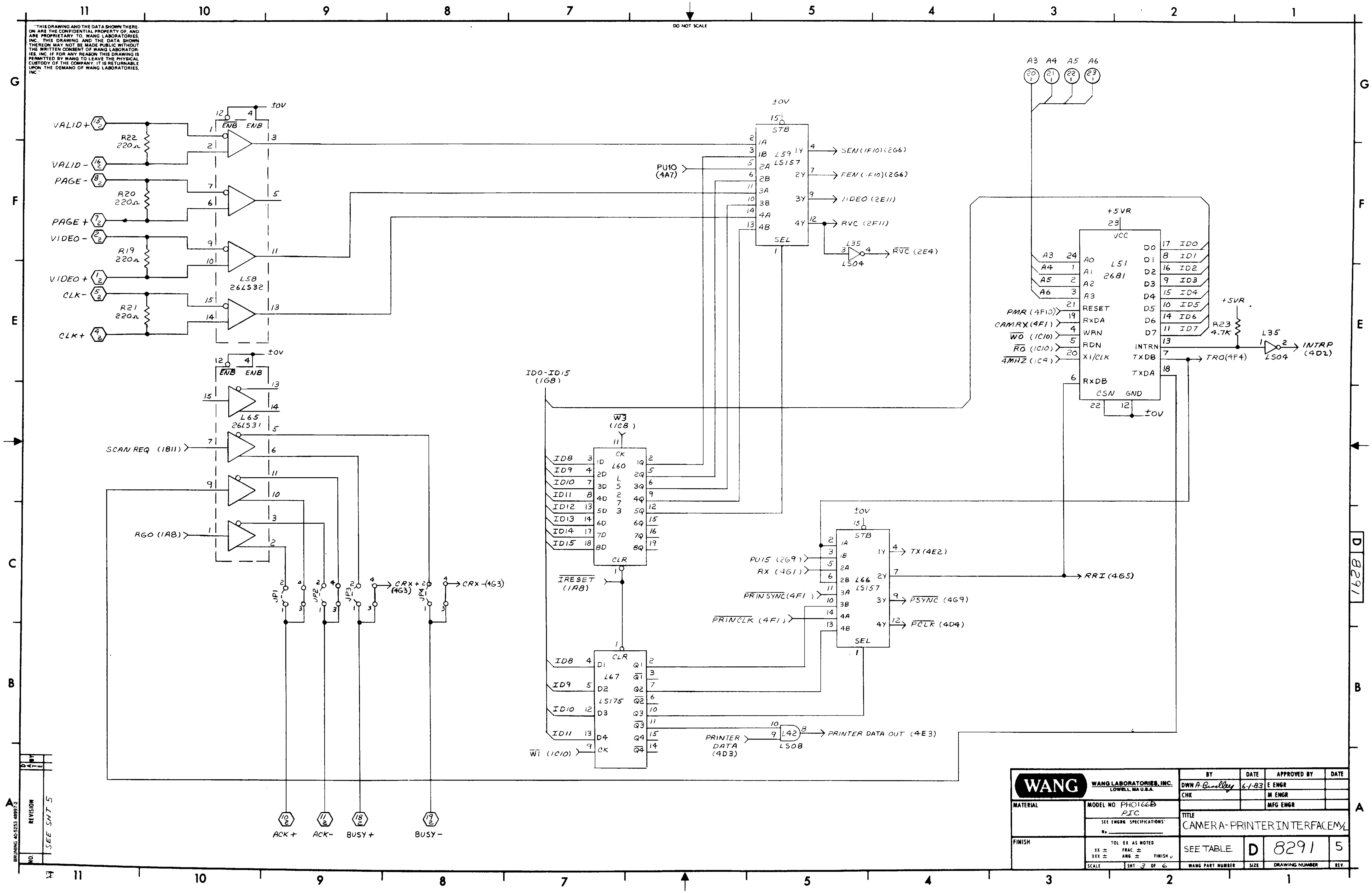
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VALID+
VALID-
PAGE-
PAGE+
VIDEO-
VIDEO+
CLK-
CLK+
R22 220Ω
R20 220Ω
R19 220Ω
R21 220Ω
L58 26LS32
L65 26LS31
SCAN REQ (1B11)
RGO (1A8)
JP1
JP2
JP3
JP4
CRX+ (4G3)
CRX- (4G3)
ACK+
ACK-
BUSY+
BUSY-
PU10 (4A7)
L59 LS157
SEN(1F10)(2G6)
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L35
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W3 (1C8)
L60 LS273
IRESET (1A8)
L67 LS175
W1 (1C10)
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LS08
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RX (4G1)
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PRINCLK (4F1)
L66 LS157
TX (4E2)
RRI (4G5)
PSYNC (4G9)
PCLK (4D4)
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+5VR
L51 2681
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DWN A. Bradley 6-1-83 E ENGR
CHK M ENGR
MFG ENGR
TITLE CAMERA-PRINTER INTERFACE
SEE TABLE
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SIZE D
DRAWING NUMBER 8291
REV. 5

DO NOT SCALE

IDO-ID15 (16B)

+5VR 2.2 1K → PU2 (1E3)

WI (1C10)

L29 LS 2 3 (CK, 1D–8D, 1Q–8Q, CLR)
ID6 3 · ID4 4 · ID2 7 · IDO 8 · ID1 13 · ID3 14 · ID5 17 · ID7 18
→ INT1 (4D2) (4E4)
→ INTO (4C2) (4E4)
→ DM2 (4E4)
→ DM0 (4E4)
→ DM1 (4E4)
L47 LS04 → PMR (3E3)
IRESET (1A8)
→ MR (4E9)

PSYNC (3C4) · L35 LS04 · L21 LS32 · L46 LS32 · L32 LS08

L7 LS74 (IPR, ICK, ICLR, IQ)

L30 LS175 (D1–D4, CLR, CK, Q1–Q4, Q1–Q4)

4CLK (7) · L42 LS08 · 4MHZ

L9 LS 3 7 3 (OC, 1D–8D, ENB, 1Q–8Q)
ID8 3 · ID10 4 · ID12 7 · ID14 8 · ID15 13 · ID13 14 · ID11 17 · ID9 18
→ PR0 · PR2 · PR4 · PR6 · PR7 · PR5 · PR3 · PR1

L10 LS 3 7 3 (OC, 1D–8D, ENB, 1Q–8Q)
IDO 3 · ID2 4 · ID4 7 · ID6 8 · ID7 13 · ID5 14 · ID3 17 · ID1 18
→ PR0 · PR2 · PR4 · PR6 · PR7 · PR5 · PR3 · PR1

→ 4MHZ (1B5)(4A8)

+5VR RB 1K · L37 LS163 (LD, ENP, ENT, CK, A–D, RCO, QA–QD, CLR) · L47 LS04 · 10V

+5VR R5 1K · L17 LS74 (2PR, 2D, 2CK, 2CLR, 2Q, 2Q)

+5VR R2A 1K

→ PU8 (1E9)

PBREQ · S03 L4 · S03 L20 · DREQ3 · DREQ1 · DREQ2 → DREQ1 – DREQ3 (1A8)

DACK 3 · DACK 1 · DACK 2 → DACK 1–DACK 3 (1E7)

AO (1G8) · L17 LS74 (2PR, 2CK, 2CLR, 2Q) · PU7A (1C4)

AIOWC (1C11) · L21 LS32 · L47 LS04 · DMARD (1F6) · L21 LS32 → ENBUF (1B9)

R3 560Ω +5VR

+5VR R10 1K

L43 LS193 (DN, UP, LD, CLR, A B C D, BOR, CAR, QA QB QC QD) · 10V

L36 LS193 (DN, UP, LD, CLR, A B C D, BOR, CAR, QA QB QC QD) · 10V

L27 LS21 · L18 LS74 (1PR, 1D, 1CK, 1CLR, 1Q, 1Q) · 4MHZ (4E8) → PU10 (3F6)

L1A 28060 (IOV, +5VR, OEB, DIR A/B, OEA, RFD/DAV A, EMPTY, ACKINB, FULL, ACKINA, RFD/DAV B, F00–F07, D0A–D7A, D0B–D7B, CLR)
SIO–SI7 · ±0V

L1 28060 (IOV, OEB, DIR A/B, OEA, RFD/DAV B, EMPTY, ACKINB, FULL, ACKINA, RFD/DAV A, D0B–D7B, CLR)
PR7–PR0 · ±0V

L18 LS74 (2PR, 2D, 2CK, 2CLR, 2Q, 2Q) · L35 LS04 · L47 LS08 · L92

L16 LS166 (CK, SI, QH, A–H, SH/LD, INH, CLR) → PRINTER DATA (3B6) · ±0V

L17 LS74 (1PR, 1D, 1CK, 1CLR, 1Q, 1Q)

L25 LS161 (LD, ENP, ENT, CK, A–D, RCO, QA–QD, CLR) · L26 LS32

L28 26LS32 (1A1–1A4, 2A1–2A4, 1Y1–1Y4, 2Y1–2Y4, 1G, 2G)
DM1 (4F9) · INTO (4F10) · MR (4E10) · INT1 (4F10) · DM2 (4F9) · DM0 (4F9) · RI (1C10)
ID1 · ID3 · ID5 · ID7 · ID4 · ID2 · IDO

CLOCK PR · SYNC PF · CMX+ (3C8) · CMX− (3C8) · BX COM DATA
R1A 220Ω · R8A 220Ω · R2A 220Ω · R1B 220Ω

L41 26LS32 (ENB, ENB, IOV)
→ RX (3C5)
→ CAMRx (3E3)
→ PRIN SYNC (3C5)
→ PRINCLK (3C6)

L34 26LS31 (ENB, ENB, IOV)
TX (3C4) → TX COM DATA
PRINTER DATA OUT (3B5) → PRINT DATA

INTRP (3E1) · L32 LS32 → INTERRUPT (1E10)
R7 560Ω +5VR
INT1 (4F10) · INTO (4F10) · 123 156 · 26LS32
→ IRQ2 · IRQ3 · IRQ4

SEE SHEET 5

WANG PART NO.	DRAWING NO.	DESCRIPTION
WANG	WANG LABORATORIES, INC. LOWELL, MASS.	
MATERIAL	MODEL NO PH0166B PIC SEE ENGRG SPECIFICATIONS No.	TITLE CAMERA–PRINTER INTERFACE M/L
FINISH	TOL EX AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG ± 1°30' FINISH 125	SCALE SHT 4 OF 6

BY	DATE	APPROVED BY	DATE
DWN A. Cuilty		E ENGR	
CHK		M ENGR	
		MFG ENGR	

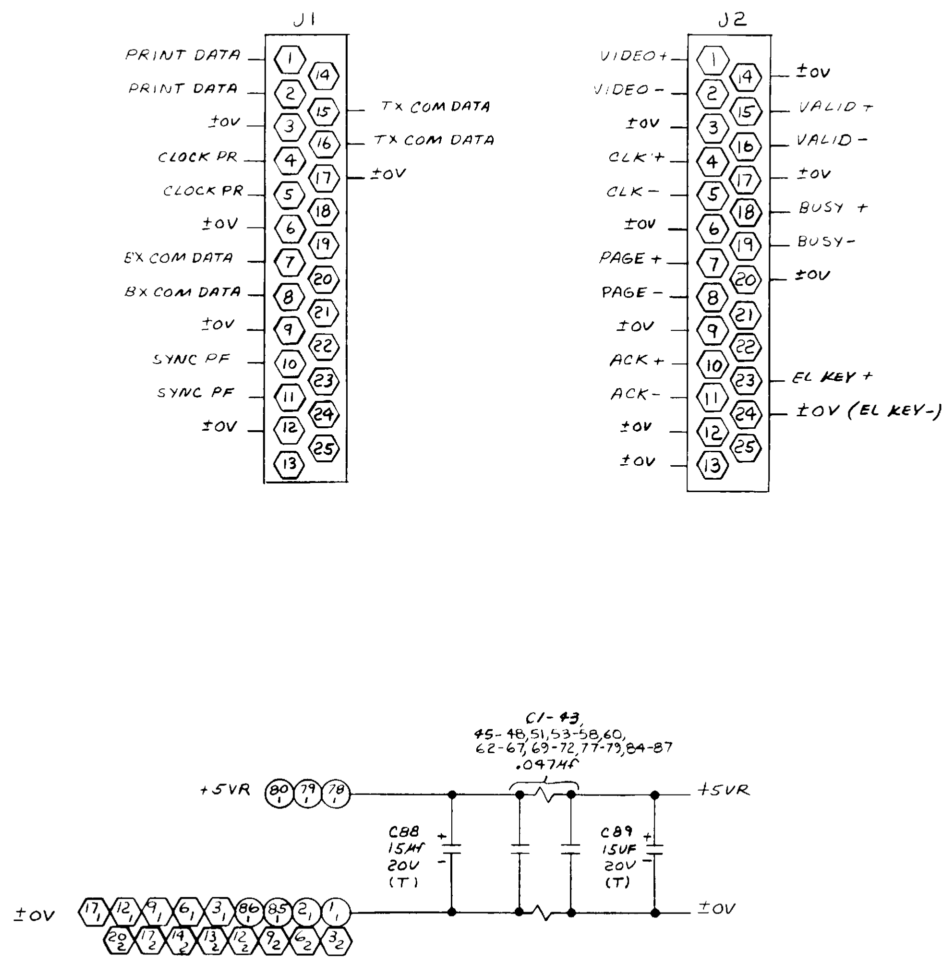
SEE TABLE | D | 8291 | 5
WANG PART NUMBER | SIZE | DRAWING NUMBER | REV

D 8291

BRUNING 40-2252-48997-3 · REVISION · NO.

DO NOT SCALE

I.C. TYPE	LOCATION	SPARES
74LS02	L22	2
74S03	L4	1
	L11	1
	L20	1
74LS04	L35	2
74S08	L40	2
74LS08	L42	1
74LS11	L54	1
74LS21	L27	1
7432	L26	2
74LS74	L39	1
74LS139	L14	1
74S260	L24	1
74LS08	L32	2
74LS32	L46	1



MNEMONICS	COORD.
A0	1G8
A1,A2	1C11
A3-A6	3G3
A8,A9	1B11
A10,A11	1A11
ACK+	3A9
ACK−	3A9
AIOWC	1C11
BUSY +	1A9
BUSY −	1A8
BX COM DATA	4G2
CLK+	3E11
CLK−	3E11
CLK PR	4G4
D0-D15	E11
DACK 1	1G8
DACK 2	1G9
DACK 3	1G9
DREQ1-DREQ3	1A7
EL KEY+	1G11
IORC	1D11
IORQ2-IORQ4	4D1
PRINT DATA	4E1
PAGE +	3F11
PAGE −	3F11
RESET	1A11
SAD	1A11
SID0-SID3	1B11
SYNC PF	4G3
TX COM DATA	4E1
VALID +	3G11
VALID −	3F11
VIDEO +	3E11
VIDEO −	3F11
4 CLK	4E11

210 = 209 + 377 OR 378			
210	209	L1,1A,69,84	L51
8291-A	8291	377-0517	377-0516

NOTE 1. ALL RES ARE 1/4W 5% UNLESS OTHERWISE SPECIFIED.

E-REV Ø

BRUNING 40-5253 48997-3

NO.	REVISION	DATE	BY
0/0	ORIGINATED PER ECO# E1937 APP'D 6/14/83	3.27.83	A.B
1/0	REVISED PER ECO# 27614 D APP'D 6/7/83	6-14-83	GHW
2/0	REVISED PER ECO# 28632 APPR'D 8/15/83	8/15/83	R
3/0	REVISED PER ECO# 29428 & 29672 APP'D: 10/7/83	10/5/83	KMS
4/0	REVISED PER ECO# 30036 APP'D: 11/7/83	11/3/83	KMS
5/0	REVISED PER ECO# 30712 APP'D 1/17/84	1-17-84	C.A.M

WANG PART NO.	DRAWING NO.	DESCRIPTION

WANG — WANG LABORATORIES, INC. LOWELL, MA U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN	A. Bradley	3.27.83	E ENGR C.M.	6/14/83
CHK		6/14/83	M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO H01668 PIC

SEE ENGNG SPECIFICATIONS No ____

TITLE CAMERA PRINTER INTRF M/L

FINISH

TOL EX AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG ± 1°30' FINISH 125

SCALE | SHT 5 OF 6

SEE TABLE (WANG PART NUMBER) | D (SIZE) | 8291 (DRAWING NUMBER) | 5 (REV)

D 8291

DO NOT SCALE

ITEM NO.	WANG PART NO.	DESCRIPTION	REFERENCE DESIGNATION(S)	QTY.
50	510-8291	P.C.B		1
49				
48				
47	SEE TABLE	I.C. Z8060	L1,1A,69,84	4
46	SEE TABLE	I.C. 2681	L51	1
45	376-0501	I.C. 74156	L23	1
44	376-0566	I.C. 74LS21	L27	1
43	376-0575	I.C. 74LS166	L16	1
42	376-0574	I.C. 74LS163	L37	1
41	376-0556	I.C. 74S03	L4,11,12,20	4
40	376-0512	I.C. 74LS112	L56	1
39	376-0509	I.C. 74S112	L38	1
38	376-0471	I.C. 26LS32	L41,58	2
37	376-0470	I.C. 26LS31	L34,65	2
36	376-0310	I.C. 74LS373	L9,10	2
35				
34	376-0303	I.C. 74LS299	L62,77	2
33	376-0302	I.C. 74LS273	L19,29,60	3
32	376-0288	I.C. 74LS244	L28,45,53	3
31	376-0286	I.C. 74LS374	L70,85	2
30	376-0285	I.C. 74LS245	L2,3	2
29	376-0236	I.C. 74LS164	L48,57	2
28	376-0235	I.C. 74S163	L64,72,79	3
27	376-0233	I.C. 74LS161	L25	1
26	376-0226	I.C. 74LS139	L14	1
25	376-0225	I.C. 74LS11	L54	1
24	376-0220	I.C. 74LS193	L8,15,36,43	4
23	376-0218	I.C. 74LS85	L6	1
22	376-0216	I.C. 74LS157	L59,66	2
21	376-0211	I.C. 74LS32	L21,26,46	3
20	376-0208	I.C. 74LS02	L22	1
19	376-0206	I.C. 74S260	L24	1
18	376-0202	I.C. 74S74	L33,	1
17	376-0200	I.C. 74S08	L40	1
16	376-0180	I.C. 74LS04	L5,31,35,47	4
15	376-0160	I.C. 74LS175	L30,67	2
14	376-0158	I.C. 74LS155	L13	1
13	376-0155	I.C. 74LS74	L7,17,18,39,63,71,86,87	8
12	376-0153	I.C. 74LS08	L32,42,55,78	4
11				
10	350-0548	25PIN, CONN.	J1	1
9	350-0520	25 PIN. CONN	J2	1
8				
7	330-3048	RES. 4.7K 1/4W 5%	R17,23,15A,15B	4
6	330-3011	RES. 1K 1/4W 5%	R1,2,4,5,6,8,10,11,14,15, 18,2A 7A,14A	14
5	330-2057	RES. 560Ω 1/4W 5%	R3,7	2
4	330-2023	RES. 220Ω 1/4W 5%	R1A,1B,8A,19-22,24	8
3				
2	300-4022	CAP. 15UF 20V T	C88,89	2
1	300-1966	CAP. .047UF	C1-43,45-48, 51,53-58,60,62-67, 69-72,77-79,84-87	72
ITEM NO.	WANG PART NO.	DESCRIPTION	REFERENCE DESIGNATION(S)	QTY.
58	652-0032	6-32 LOCK-NUT		1
57	650-3120	6-32x3/8 PAN HD		1
56	462-0611	STAND-OFF		4
55	376-9030	SKT. 28PIN	L1,1A,69,84	4
54	376-9079	SKT. 24PIN	L51	1
53				
52				
51	465-1250	EJECTOR		1

NO	REVISION	BY
A	SEE SHT 3	DEW

BIRLING 40-5253 4P972

	BY	DATE	APPROVED BY	DATE
WANG LABORATORIES, INC. LOWELL, MA U.S.A.	DWN A. Bradley	6-6-83	E ENGR	
	CHK		M ENGR	
			MFG ENGR	

MATERIAL

MODEL NO. 401668 P.I.C

SEE ENGRG SPECIFICATIONS No.

TITLE CAMERA PRINTER INTRF M/L

FINISH

TOL. EX. AS NOTED
XX ± FRAC. ±
XXX ± ANG. ± FINISH √

SCALE	SHT 6 OF 6	WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
		SEE TABLE	D	8291	5

D 8291