Terminal Computers
PTS 6000 Vol.1

Terminal Computers
PTS 6000 Vol.2

Field Service Manual
Terminal Computers
PTS 6810/11
6812
6813
6814
6824

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and Data Systems

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Great care has been taken to ensure that the information contained in this handbook is accurate and complete. Should any errors or omissions be discovered, however, or should any user wish to make a suggestion for improving this handbook, he is invited to send the relevant details to:

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1.1.1 Introduction

Figure 1.1-1

The basic purpose of the PTS 6000 System is to provide computerized terminals for the work positions in bank- and post offices etc. This requires, besides special equipment at each work position, a Terminal Computer which controls the transactions carried out and which either stores the transaction data (off-line systems) or transfers it via modems and telephone lines to a remote data centre (on-line systems).

Smaller offices, with 1-4 work positions, can share the computer with a bigger office. The work positions of the smaller office are then connected to the bigger office's computer in a way similar to the on-line connection, i.e. via modems and telephone lines. Such work positions are known as Remote Work Stations whilst the work positions at the computer site are known as Local Work Stations.

In certain cases, mainly when data exchange with other systems is required, it can be necessary to connect peripheral equipment (Magnetic Tape Unit, Disc Unit, Line Printer etc.) to the Terminal Computer.

This manual contains field service information for the Terminal Computers 6811 (also called 6810), 6812-6814 and 6824.

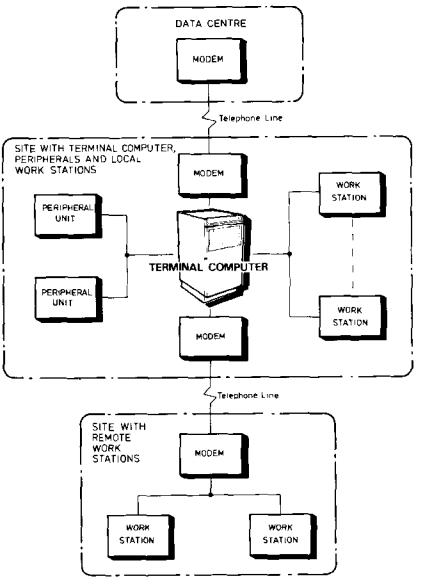


Figure 1.1-1 Basic System Configuration

1.1.2 Terminal Computer 6810/11

Figure 1.1-2

Physical Structure

The computer is contained in a cabinet where the logic modules are plugged into the backpanel of a 10-position rack. On this backpanel (1A) there is the General Purpose Bus that interconnects the logic modules. Smaller backpanels (1B, 1C) and some separate wires and flatcables are used for remaining interconnections.

Some of the additional interconnections are dependent on the specific computer configuration (master priority and break request wiring), and must often be made at the installation. This backpanel wiring is specified in section 2.5 of this manual.

Contained in the cabinet are also; one or two digital cassette recorders for program load and back-up, a control panel, a power supply unit and a cooling fan.

Processing Units & Memory System

The computer is based on a central processing unit (CPU) of type P852. An optional I/O processor (IOP 6827) can be added to increase the capacity of data transfers when heavy traffic is expected between memory and interface units along the GP bus.

The memory capacity is 8-32K 16-bit words, built to the desired range by plugging in one or two core memory modules. Two different modules are available; CMM 6822 with a capacity of 8K, and CMM 6823 with a capacity of 16K.

NOTE

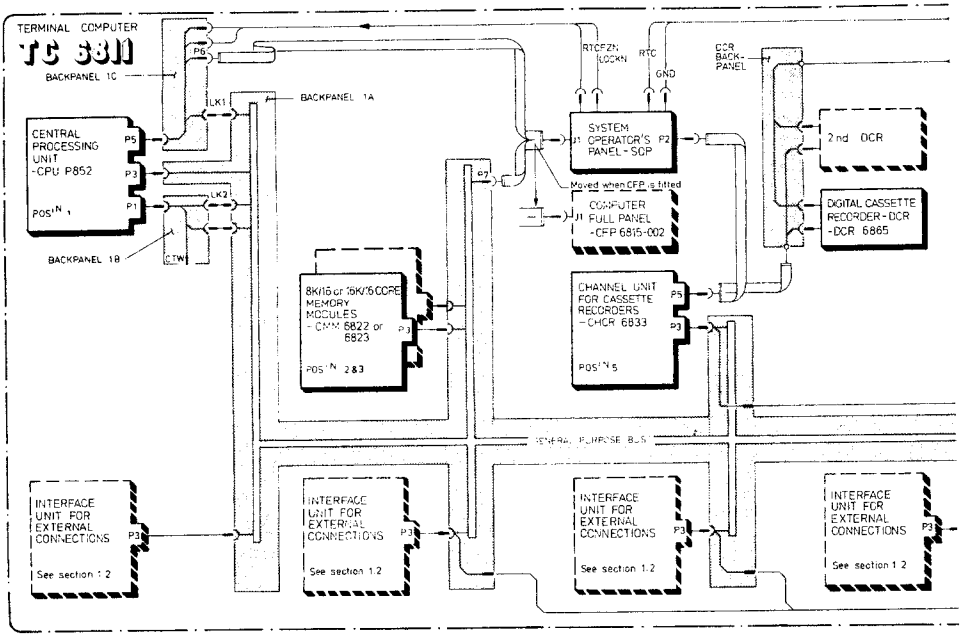
Some of the 6810/11 computers have been upgraded according to a modification kit known as UK01. These computers are using a CPU of type P857, two CMMs of type 6825 (each of 32K 16-bit words) and a memory management unit, MMU 6828. Processing and memory capacity has then been increased to the class of the TC 6813.

Program Load & Back-Up Medium

The cabinet is able to house up to two digital cassette recorders of type 6865 (6861 in earlier computer models). These recorders are controlled via the bus-connected interface unit CHCR 6833.

Control Panels

A system operator's panel (SOP) is always fitted to the computer. This panel provides the control and display facilities that are required for the daily routines and operates via the CHCR 6833. When extended control and display facilities are required, it is possible to add a computer full panel (CFP 6815-002).



External Interfaces

The interface units available for connecting work stations and peripherals to the computer, and for connecting the computer on-line to a data centre, are described in section 1.2; EXTERNAL CONNECTIONS.

Power Supply

The power supply unit (PSU) is available in two basic versions; one for mains sources of 100-127V/60Hz and another one for 200-240V/50Hz. Besides the required D.C. voltages the PSU also provides a real time clock signal (RTC), a power failure alarm (PWFN) and a system reset signal (RSLN).

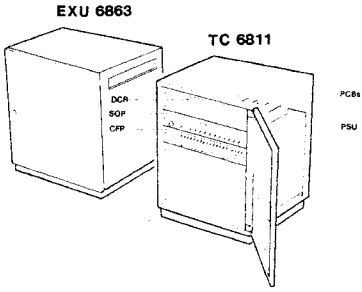
Extension Unit

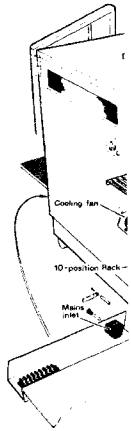
Interface units that (because of space, power or cabling reasons) cannot be contained in the computer cabinet, can instead be put into an extension unit, EXU 6863. This is a stripped computer cabinet where the rack with backpanel 1A and the PSU have been retained.

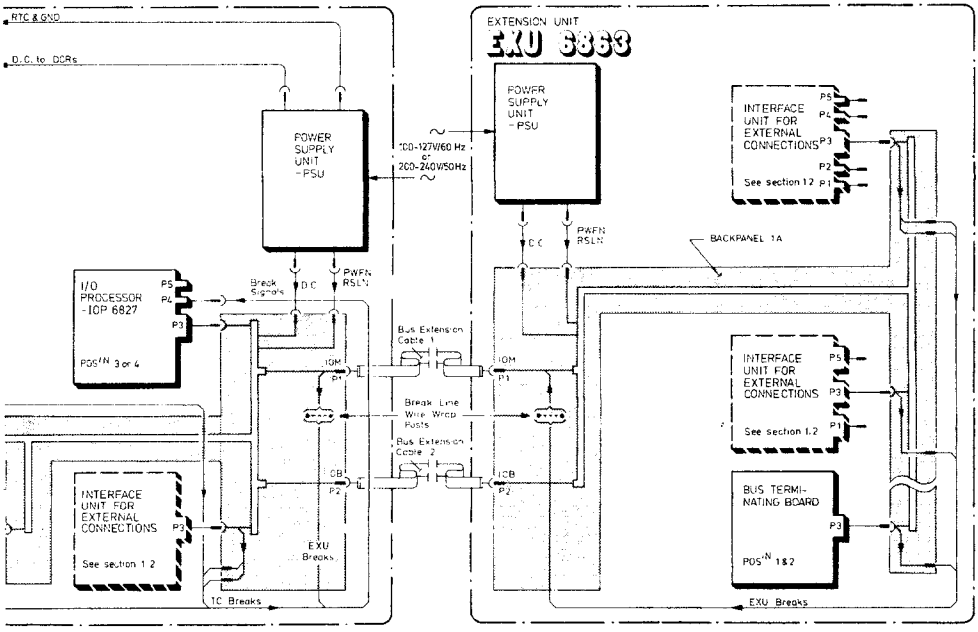
The TC and EXU cabinets are interconnected via two bus extension cables. Besides extending the bus to the EXU, these cables also provide a possibility to link other lines between the cabinets, e.g. break lines from the EXU to an IOP in the TC cabinet. Such lines are in both cabinets terminated on wire wrap posts close to the extension plugs on backpanel 1A.

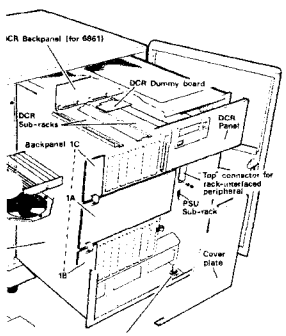
The bus extension cables also interconnect each one of the PWFN and RSLN signals with corresponding signal from the other cabinet. Each twin-source signal then operates in a wired-or manner within the extended system.

A limited outfit in the extension cabinet and limitations in the extended bus lead to some restrictions. The following computer sub-modules can NOT be placed in an extension unit; CPU, IOP, CMM, MMU and CHCR.









TC & EXU CABINETS – Front view of backpanels and connectors

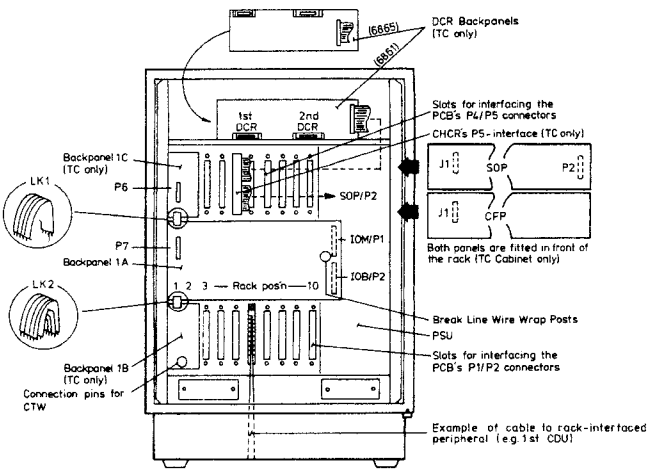


Figure 1.1-2 TC 6811/EXU 6863 - Basic Configuration

SUBNUMBER LIST

Subnumber	Description (main characteristics)	Comments
001	220/200–240 V, 50 Hz, DCR 1 (CPU P852)	Replaced by 6811–301 in the beginning of 1979.
101	100–127 V, 60 Hz, DCR 3, UL/CSA (CPU P852)	
102	= 101 excl. DCR unit	Special version.
201	220/200–240 V, 50 Hz, DCR 1 + UK01 (CPU P857)	Arise only in field. UK01 = Upgrading Kit 6810–601
301	200–240 V, 50 Hz, DCR 3 (CPU P852)	Present standard version. Replaces 6811–001.
401	200–240 V, 50 Hz, DCR 3 + UK01 (CPU P857) excl. CMM	6811–301 excl. CPU P852 and CMM, modified with Upgrading Kit 6810–601 UK01.
402	100–127 V, 60 Hz, DCR 3, UL/CSA + UK01 (CPU P857) excl. CMM	6811–101 excl. CPU P852 and CMM, modified with Upgrading Kit 6810–601 UK01.
501	200–240 V, 50 Hz, DCR 3 excl. CPU and CMM	Special version of 6811–301.

DCR 1 = PTS 6861 DCR
DCR 3 = PTS 6865 DCR

1.1.3 Terminal Computer 6812

Figure 1.1-3

Physical Structure

The computer is contained in a cabinet where the logic modules are plugged into the backpanel of a 10-position rack. On this backpanel (1A) there is the General Purpose Bus that interconnects the logic modules. Smaller backpanels (1B, 1C, 1D) and some separate wires and flatcables are used for remaining interconnections.

Some of the additional interconnections are dependent on the specific computer configuration (master priority and break request wiring), and must often be made at the installation. This backpanel wiring is specified in section 2.5 of this manual.

Contained in the cabinet are also; program load and back-up media (cassette recorders and/or flexible disc drives), a control panel, a power supply unit and a cooling fan.

Processing Units & Memory System

The computer is based on a central processing unit (CPU) of type P852. An optional I/O processor (IOP 6827) can be added to increase the capacity of data transfers when heavy traffic is expected between memory and interface units along the GP bus.

The memory capacity is fixed to 32K 16-bit words by a single core memory module, CMM 6825.

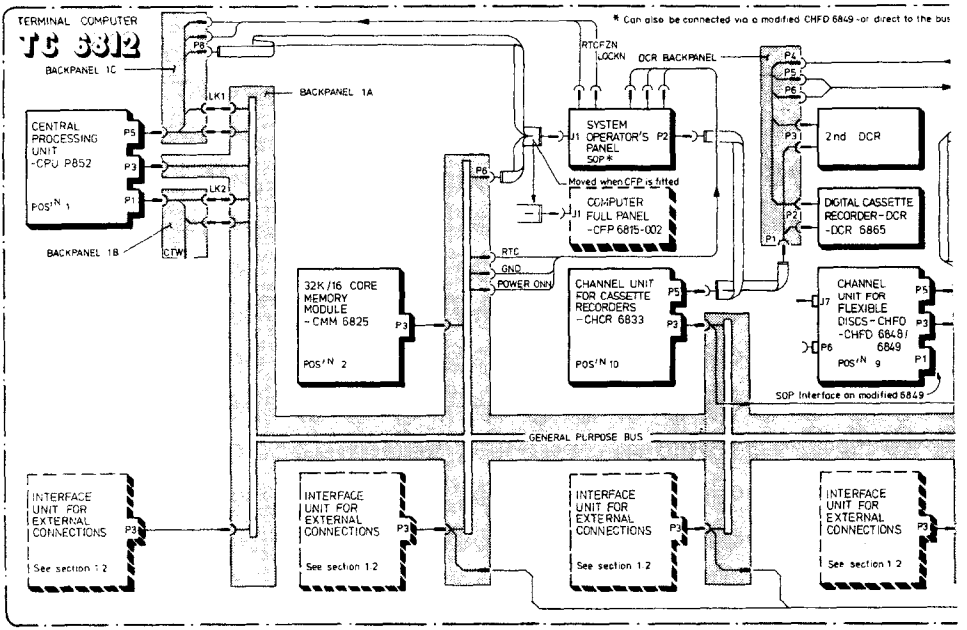
Program Load & Back-Up Media

The cabinet is able to house up to two digital cassette recorders, DCR 6865, and up to two flexible disc drives, FDD 6867 (250 Kbytes) or FDD 6791 (1 Mbyte). The recorders are controlled via the busconnected interface unit CHCR 6833, and the flexible disc drives via CHFD 6848 (for FDD 6867) or CHFD 6849 (for FDD 6791).

Control Panels

A system operator's panel (SOP), that provides the control and display facilities required for the daily routines, is always fitted to the computer. This panel can be connected in three different ways; via the CHCR 6833 as shown in figure, via a modified CHFD 6849 (in both cases a 'passive' SOP), or direct to the backpanel ('active' SOP, modified according to an upgrading kit to get an integrated interface logic, CUSOP).

When extended control and display facilities are required, it is possible to add a computer full panel (CFP 6815-002). However, this cabinet is not prepared for any permanent use of this panel (the size of cover plates adapted to the extended full panel, EFP, used in TC 6813).



External Interfaces

The interface units available for connecting work stations and peripherals to the computer, and for connecting the computer on-line to a data centre, are described in section 1.2; EXTERNAL CONNECTIONS.

Power Supply

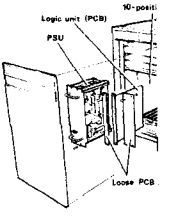
The power supply unit (PSU) can be adapted to either of the mains sources; 100-127V/60Hz, or 200-240V /50Hz. Besides the required D.C. voltages the PSU also provides a real time clock signal (RTC), a power failure alarm (PWFN), a system reset signal (RSLN) and a power on indication (POWER ONN).

Extension Unit

Interface units that (because of space, power or cabling reasons) cannot be contained in the computer cabinet, can instead be put into an extension unit, EXU 6864. This is a stripped computer cabinet where the rack with backpanel 1A and the PSU have been retained.

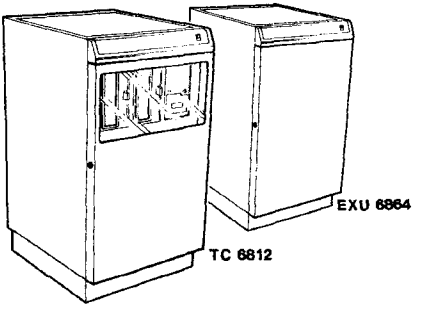
The TC and EXU cabinets are interconnected via two bus extension cables. Besides extending the bus to the EXU, these cables also provide a possibility to link other lines between the cabinets, e.g. break lines from the EXU to an IOP in the TC cabinet. Such lines are in both cabinets terminated on wire wrap posts close to the extension plugs on backpanel 1A.

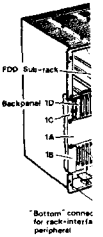
The bus extension cables also interconnect each one of the PWFN and RSLN signals with corresponding signal from the other cabinet. Each twin-source signal then operates in a wired-or manner within the extended system.

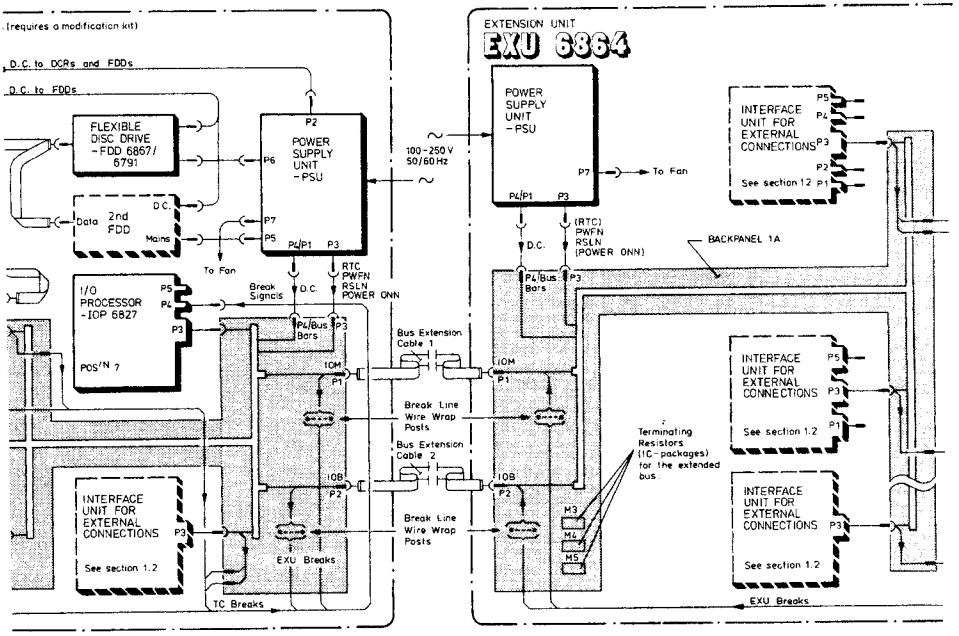


NOTE

When required it is also possible to add a second EXU 6864. The extension cables are then further extended from the cable interface in the first EXU.







TC & EXU CABINETS - Front view of backpanels and connectors

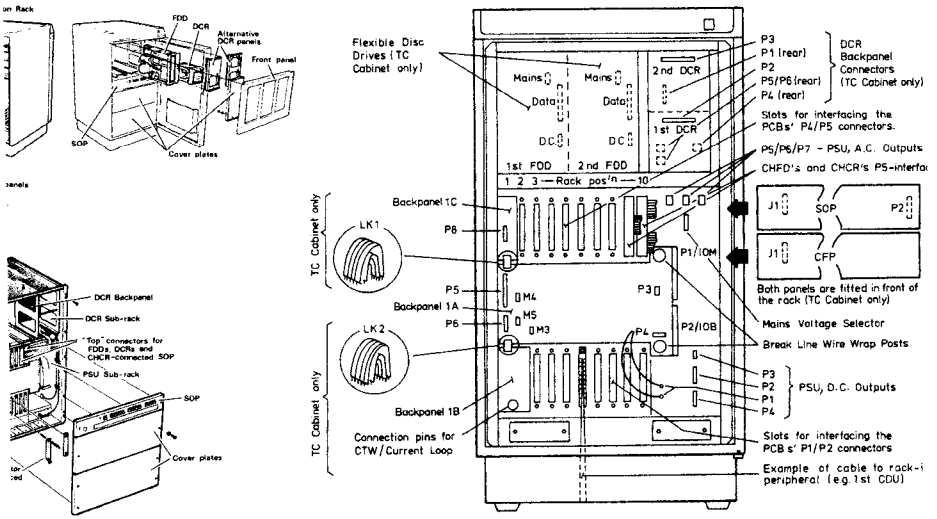


Figure 1.1-3 TC 6812/EXU 6864 - Basic Configur

SUBNUMBER LIST

Subnumber					
Mains connection			Configuration of back-up / progr. loading media		
European 200–240 V 50 Hz	UL/CSA 100–130 V 60 Hz	UL/CSA 200–240 V 60 Hz	FDD / DCR / CHFD		
001	101	201	1 FDD		CHFD
002	102	202		1 DCR	
003	103	203	1 FDD	1 DCR	CHFD
004	104	204	2 FDD		CHFD
005	105	205		2 DCR	
006	106	206	2 FDD	1 DCR	CHFD
007	107	207	1 FDD	2 DCR	CHFD

Special versions receive subnumbers starting with 5 = 6812 – 5XX

Subnumber	
501–507	Equal to 001–007 excl. CMM

1.1.4 Terminal Computer 6813

Figure 1.1-4

Physical Structure

The computer is contained in a cabinet where the logic modules are plugged into the backpanel of a 10-position rack. On this backpanel (1A) there is the General Purpose Bus that interconnects the logic modules. Smaller backpanels (1B, 1C, 1D) and some separate wires and flatcables are used for remaining interconnections.

Some of the additional interconnections are dependent on the specific computer configuration (master priority and break request wiring), and must often be made at the installation. This backpanel wiring is specified in section 2.5 of this manual.

Contained in the cabinet are also; program load and back-up media (cassette recorders and/or flexible disc drives), a control panel, a power supply unit and a cooling fan.

Processing Units & Memory System

The computer is based on a central processing unit (CPU) of type P857. One or two optional I/O processors (IOP 6827) can be added to increase the capacity of data transfers when heavy traffic is expected between memory and interface units along the GP bus.

The memory capacity is 32-128K 16-bit words, built to the desired range by plugging in 1-4 core memory modules of type 6825 (each of 32K). When more than one CMM are fitted, the computer must also be equipped with a memory management unit, MMU 6828.

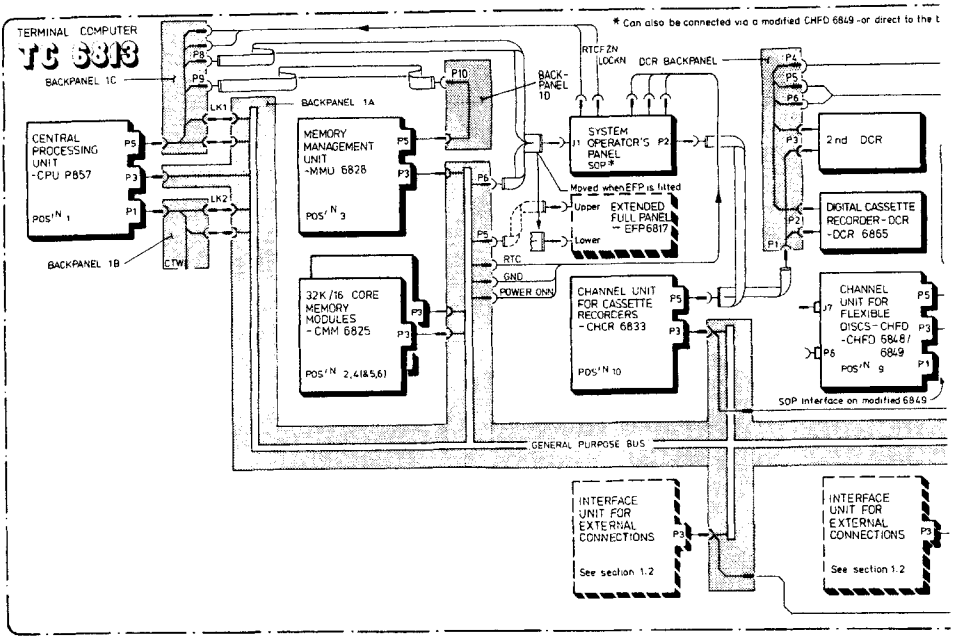
Program Load & Back-Up Media

The cabinet is able to house up to two digital cassette recorders, DCR 6865, and up to two flexible disc drives, FDD 6867 (250 Kbytes) or FDD 6791 (1 Mbyte). The recorders are controlled via the busconnected interface unit CHCR 6833, and the flexible disc drives via CHFD 6848 (for FDD 6867) or CHFD 6849 (for FDD 6791).

Control Panels

A system operator's panel (SOP), that provides the control and display facilities required for the daily routines, is always fitted to the computer. This panel can be connected in three different ways; via the CHCR 6833 as shown in figure, via a modified CHFD 6849 (in both cases a 'passive' SOP), or direct to the backpanel ('active' SOP, modified according to an upgrading kit to get an integrated interface logic, CUSOP).

When extended control and display facilities are required, it is possible to add an extended full panel (EFP 6817) in addition to the SOP.



External Interfaces

The interface units available for connecting work stations and peripherals to the computer, and for connecting the computer on-line to a data centre, are described in section 1.2; EXTERNAL CONNECTIONS.

Power Supply

The power supply unit (PSU) can be adapted to either of the mains sources; 100-127V/60Hz, or 200-240V /50Hz. Besides the required D.C. voltages the PSU also provides a real time clock signal (RTC), a power failure alarm (PWFN), a system reset signal (RSLN) and a power on indication (POWER ONN).

Extension Unit

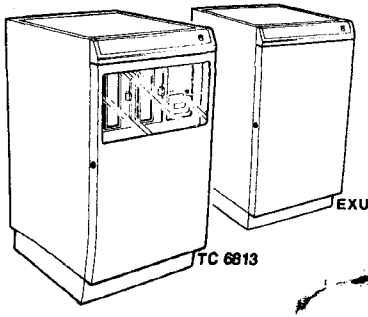
Interface units that (because of space, power or cabling reasons) cannot be contained in the computer cabinet, can instead be put into an extension unit, EXU 6864. This is a stripped computer cabinet where the rack with backpanel 1A and the PSU have been retained.

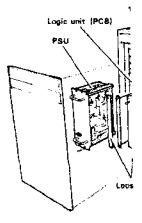
The TC and EXU cabinets are interconnected via two bus extension cables. Besides extending the bus to the EXU, these cables also provide a possibility to link other lines between the cabinets, e.g. break lines from the EXU to an IOP in the TC cabinet. Such lines are in both cabinets terminated on wire wrap posts close to the extension plugs on backpanel 1A.

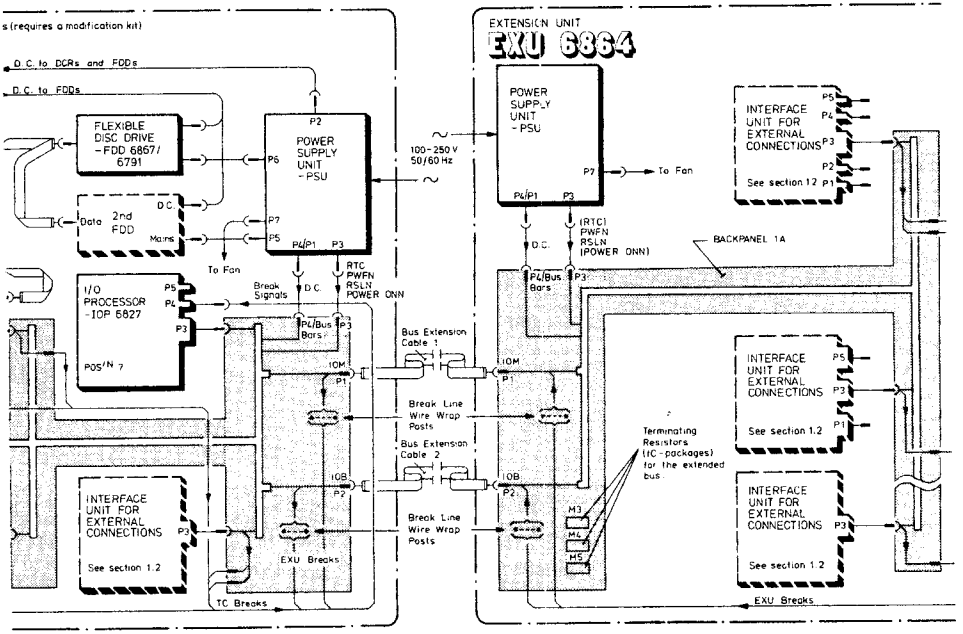
The bus extension cables also interconnect each one of the PWFN and RSLN signals with corresponding signal from the other cabinet. Each twin-source signal then operates in a wired-or manner within the extended system.

NOTE

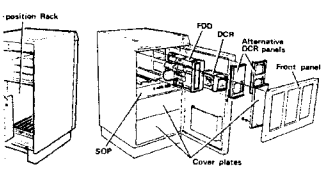
When required it is also possible to add a second EXU 6864. The extension cables are then further extended from the cable interface in the first EXU.

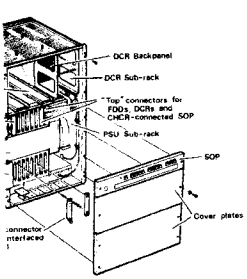






TC & EXU CABINETS - Front view of backpanels and connectors





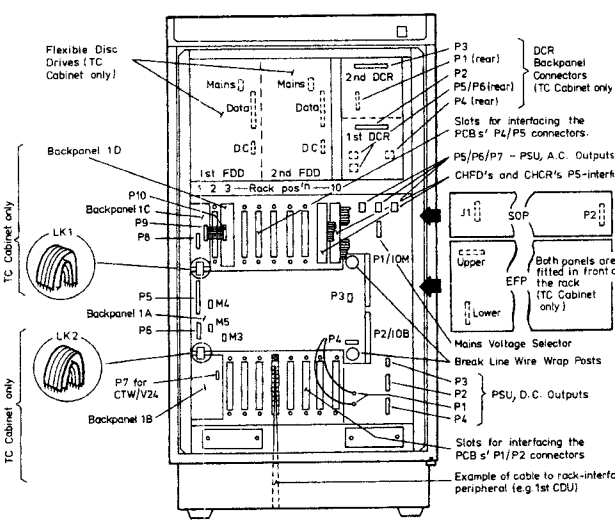


Figure 1.1-4 TC 6813/EXU 6864 - Basic Configurati

I TC 6813 basic unit incl. PSU, SOP, CPU

Subnumber			
Mains connection			Cabinet version
200–240 V 50 Hz Euro-plug	100–130 V 60 Hz US-plug	200–240 V 60 Hz US-plug	Cabinet prepared for
011	111	211	1 (or 1/4) MB FDD + DCR
012	112	212	1 (or 1/4) MB FDD (NO DCR)
013	113	213	1/4 MB FDD + DCR

II TC 6813 basic unit incl. PSU, SOP, CPU, CMM 6825, MMU 6828, CHCR 6833, CHLT 6831

Subnumber					
Mains connection			Configuration of back-up and progr. loading media		
200–240 V 50 Hz Euro-plug	100–130 V 60 Hz US-plug	200–240 V 60 Hz US-plug	FDD / DCR / CHFD		
001	101	201	1 FDD		CHFD
002	102	202		1 DCR	
003	103	203	1 FDD	1 DCR	CHFD
004	104	204	2 FDD		CHFD
005	105	205		2 DCR	
006	106	206	2 FDD	1 DCR	CHFD
007	107	207	1 FDD	2 DCR	CHFD
	108				CHFD

501–507		Equal to 001–007 excl. CMM
551		Special version for the Hugin-project

1.1.5 Terminal Computer 6814

Figure 1.1-5

Physical Structure

The computer is contained in a cabinet where the logic modules are plugged into the backpanel of a 10-position rack. On this backpanel (1A) there is the General Purpose Bus that interconnects the logic modules. Smaller backpanels (1B and 1C) and some separate wires and flatcables are used for remaining interconnections.

Some of the additional interconnections are dependent on the specific computer configuration (master priority and break request wiring), and must often be made at the installation. This backpanel wiring is specified in section 2.5 of this manual.

Contained in the cabinet are also; one or two flexible disc drives, a control panel, a power supply unit and a cooling fan.

Processing Unit & Memory System

The computer is based on a central processing unit (CPU) of type P857R or P857RA. This CPU also includes an I/O processor and a memory management unit. The integrated IOP function has a capacity equal to two IOPs of type 6827, and the memory management is able to address 1Mbyte.

The memory capacity is 32-128K 16-bit words, built to the desired range by plugging in 1-4 core memory modules of type 6825 (each of 32K).

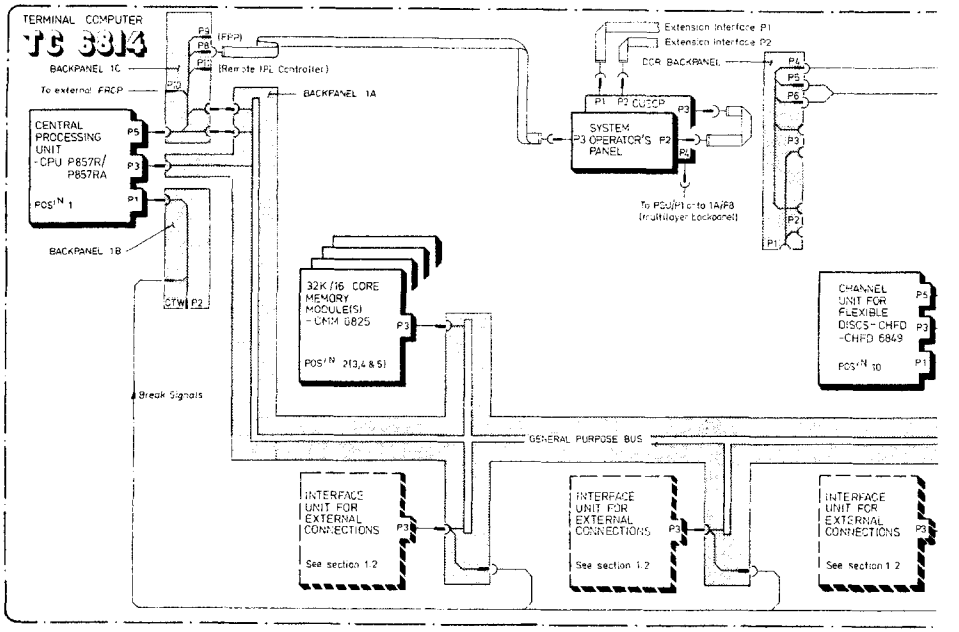
Program Load & Back-Up Media

The cabinet is able to house up to two flexible disc drives, FDD 6791 (1Mbyte). The drives are controlled via the busconnected interface unit CHFD 6849. However, if desired, the cabinet can instead be equipped with drives of type FDD 6867 (250 Kbyte) and a controller of type CHFD 6848. It is even possible to install up to two digital cassette recorders (DCR 6865) with necessary controller, CHCR 6833.

Control Panels

A system operator's panel (SOP), that provides the control and display facilities required for the daily routines, is always fitted to the computer. This panel has now got an integrated interface unit (Control Unit SOP, CUSOP) that makes it independent of other units like CHCR and CHFD.

When extended control and display facilities are required, it is possible to connect an external Full Refreshed Control Panel, FRCP 6981.



External Interfaces

The interface units available for connecting work stations and peripherals to the computer, and for connecting the computer on-line to a data centre, are described in section 1.2: EXTERNAL CONNECTIONS.

Power Supply

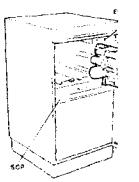
The power supply unit (PSU) can be adapted to either of the mains sources: 100-127V/60Hz, or 200-240V /50Hz. Besides the required D.C. voltages the PSU also provides a real time clock signal (RTC), a power failure alarm (PWFN), a system reset signal (RSLN) and a power on indication (POWER ONN).

Extension Unit

Interface units that (because of space, power or cabling reasons) cannot be contained in the computer cabinet, can instead be put into an extension unit, EXU 6864. This is a stripped computer cabinet where the rack with backpanel 1A and the PSU have been retained.

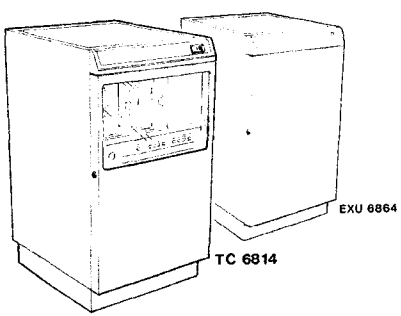
The TC and EXU cabinets are interconnected via two bus extension cables. Besides extending the bus to the EXU, these cables also provide a possibility to link other lines between the cabinets, e.g. break lines from the EXU to the CPU in the TC cabinet. Such lines are in both cabinets terminated on extension posts close to the extension plugs on backpanel 1A.

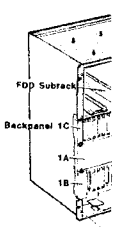
The bus extension cables also interconnect each one of the PWFN and RSLN signals with corresponding signal from the other cabinet. Each twin-source signal then operates in a wired-or manner within the extended system.



NOTE

When required it is also possible to add a second EXU 6864. The extension cables are then further extended from the cable interface in the first EXU.





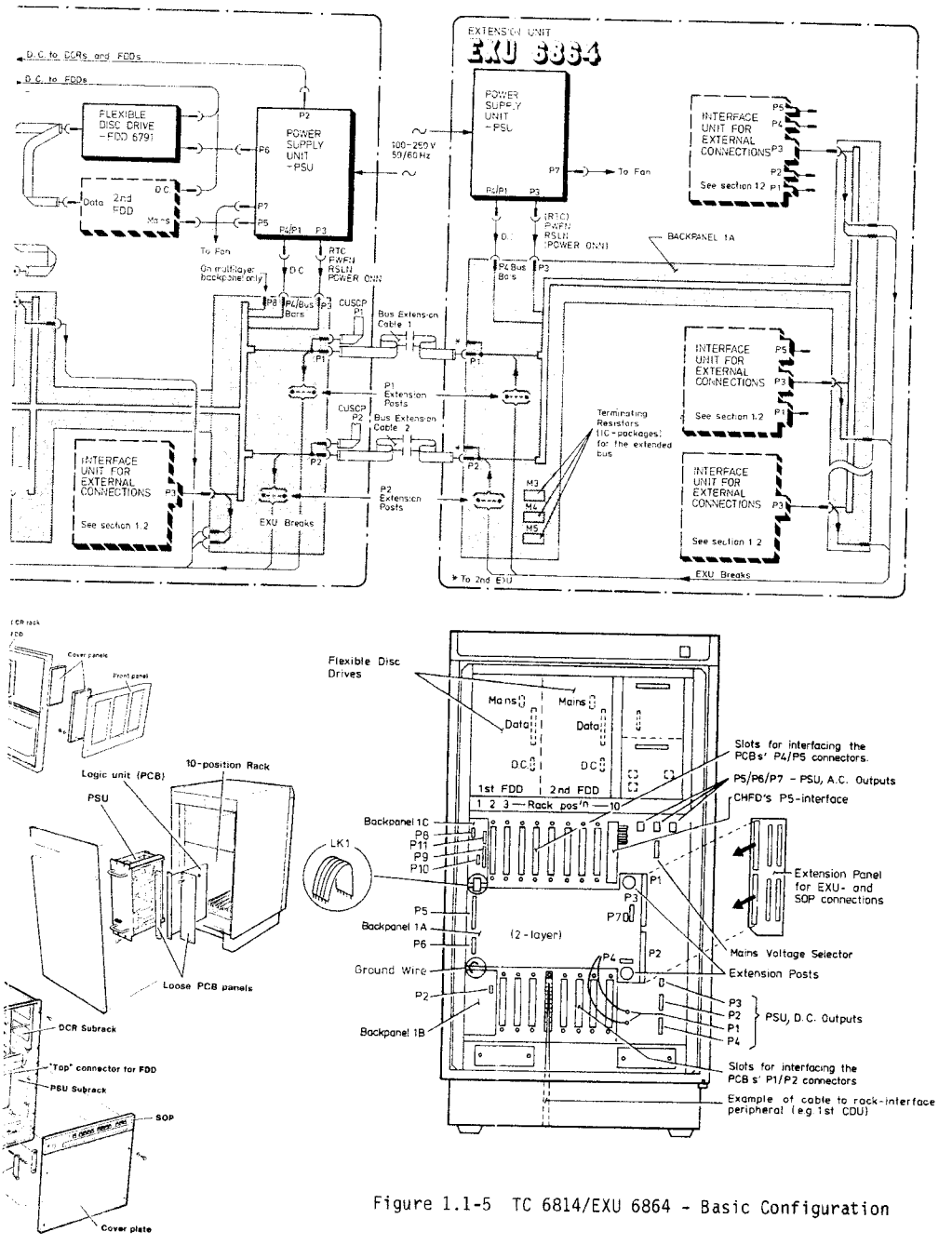


Figure 1.1-5 TC 6814/EXU 6864 - Basic Configuration

1.1.6 Terminal Computer 6824

Figure 1.1-6

Physical Structure

The computer is contained in a cabinet where the logic modules are plugged into the backpanel of a 10-position rack. On this backpanel (1A) there is the General Purpose Bus that interconnects the logic modules. Smaller backpanels (1B and 1C) and some separate wires and flatcables are used for remaining interconnections.

Some of the additional interconnections are dependent on the specific computer configuration (master priority and break request wiring), and must often be made at the installation. This backpanel wiring is specified in section 2.5 of this manual.

Contained in the cabinet are also; one or two flexible disc drives, a control panel, a power supply unit with battery back-up, and finally a cooling fan. The cooling system is here of a new type where the air enters and leaves the cabinet via the extended back section.

Processing Unit & Memory System

The computer is based on a central processing unit (CPU) of type P857RA. This CPU also includes an I/O processor and a memory management unit. The integrated IOP function has a capacity equal to two IOPs of type 6827, and the memory management is able to address 1Mbyte.

The memory capacity is 128-512K 16-bit words, built to the desired range by plugging in 1-4 semiconductor memory modules of type 6781 (each of 128K). The battery back-up provided is capable of maintaining a maximum memory configuration for at least 0.6 hours.

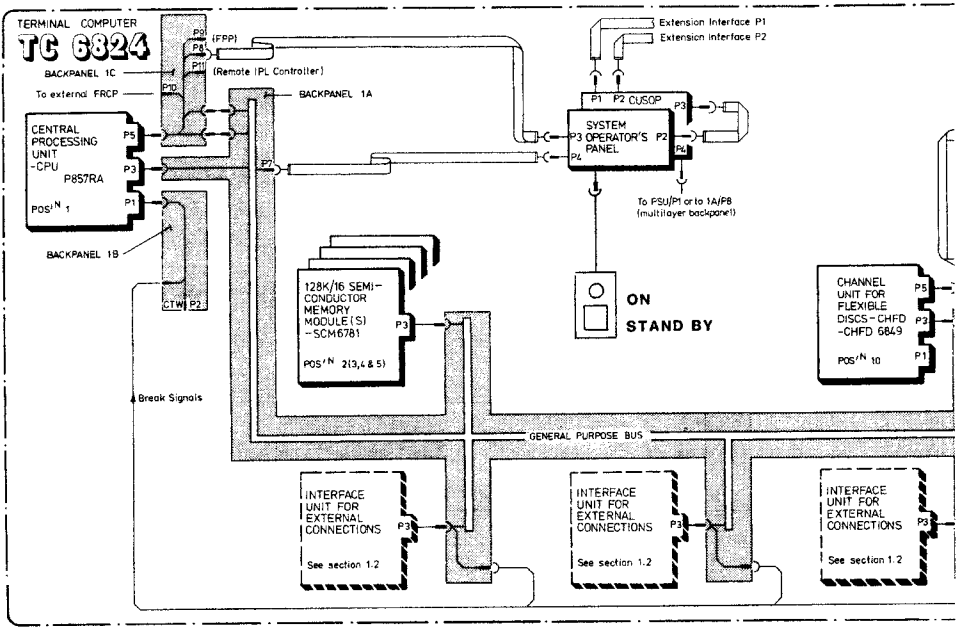
Program Load & Back-Up Media

The cabinet is able to house up to two flexible disc drives, FDD 6791 (1Mbyte). The drives are controlled via the busconnected interface unit CHFD 6849. However, if desired, the cabinet can instead be equipped with drives of type FDD 6867 (250 Kbyte) and a controller of type CHFD 6848.

Control Panels

A system operator's panel (SOP), that provides the control and display facilities required for the daily routines, is always fitted to the computer. This panel has an integrated interface unit (Control Unit SOP, CUSOP) that makes it independent of other units like CHCR and CHFD.

When extended control and display facilities are required, it is possible to connect an external Full Refreshed Control Panel, FRCP 6981.



External Interfaces

The interface units available for connecting work stations and peripherals to the computer, and for connecting the computer on-line to a data centre are described in section 1.2; EXTERNAL CONNECTIONS.

Power Supply

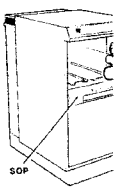
The power supply unit (PSU) can be adapted to either of the mains sources; 100-127V/60Hz, or 200-240V /50Hz. Besides the required D.C. voltages the PSU also provides a real time clock signal (RTC), a power failure alarm (PWFN), a system reset signal (RSLN) and a power on indication (POWER ONN). Battery back-up is provided for the semiconductor memory system. For maximum memory configuration the back-up time is more than 0.6 hours.

Extension Unit

Interface units that (because of space, power or cabling reasons) cannot be contained in the computer cabinet, can instead be put into an extension unit, EXU 6864. This is a stripped computer cabinet of type 6812/13/14 where the rack with backpanel 1A and the PSU have been retained.

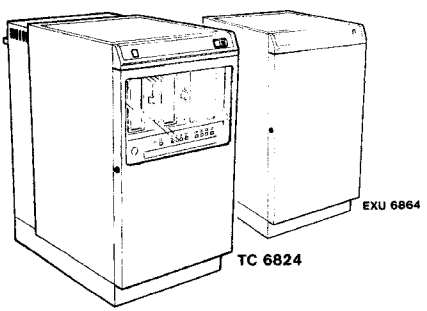
The TC and EXU cabinets are interconnected via two bus extension cables. Besides extending the bus to the EXU, these cables also provide a possibility to link other lines between the cabinets, e.g. break lines from the EXU to the CPU in the TC cabinet. Such lines are in both cabinets terminated on extension posts close to the extension plugs on backpanel 1A.

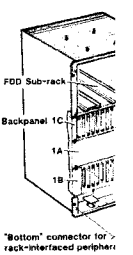
The bus extension cables also interconnect each one of the PWFN and RSLN signals with corresponding signal from the other cabinet. Each twin-source signal then operates in a wired-or manner within the extended system.

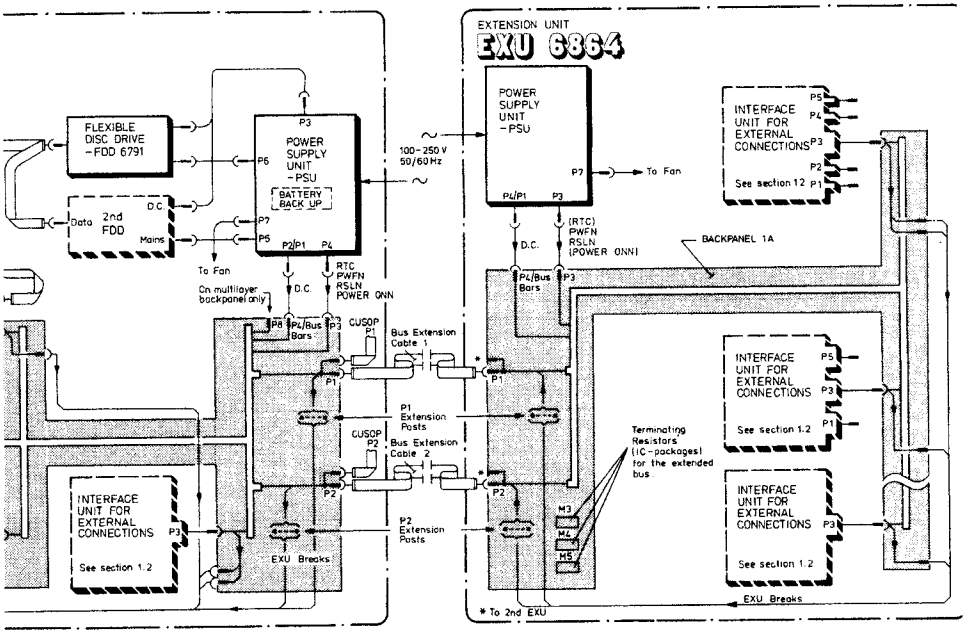


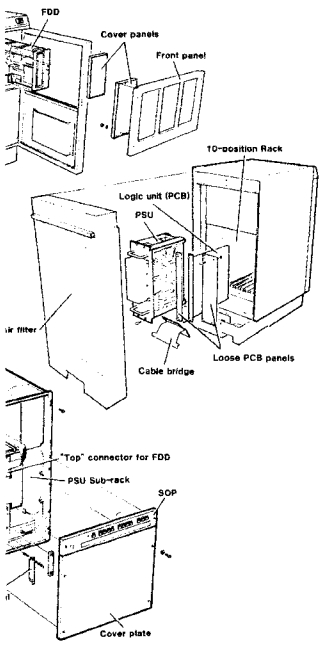
NOTE

When required it is also possible to add a second EXU 6864. The extension cables are then further extended from the cable interface in the first EXU.









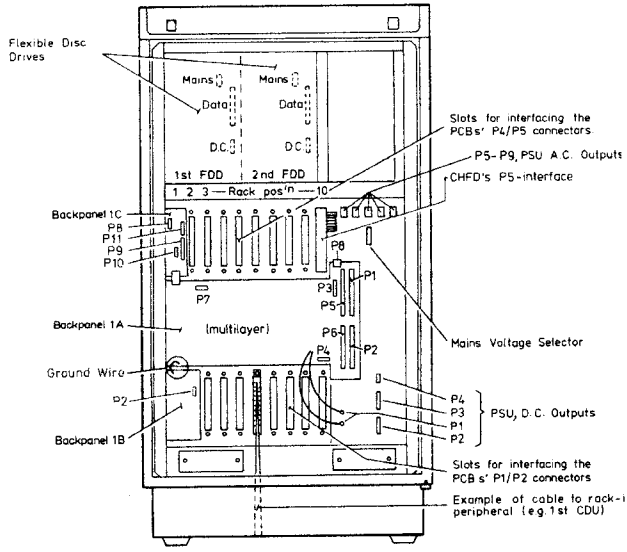


Figure 1.1-6 TC 6824/EXU 6864 - Basic Configuration

1.1.7 GENERAL PURPOSE (GP) BUS

All transfers of information between elements of the P852M/P856M or P857M system take place via the GP bus, and the lines of the bus comprise the input and output signal and address lines necessary for the data transfer requirements of the system. The GP bus can be extended outside the basic mounting box to further equipment shelves by using 125 Ohm, flexible, plug-in, transmission lines. The lines can be extended to convenient lengths between equipment shelves up to a total maximum length of 14.5 metres. Line termination facilities are provided in the basic mounting box and, it required, in the equipment shelves.

Two types of signal are used to bus: command signals and data signals. Command signals are those which will cause an immediate action according to their change of state: these signals have no unknown state but are always either logic "1" or "0". Data signals carry the actual information exchanged amongst the system elements: these signals are permitted to adopt indeterminate values except when the information is actually being used in the processing.

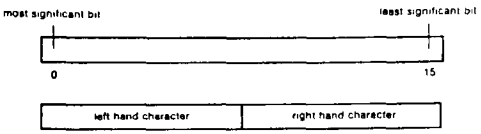
The signals carried by the GP bus lines are described below. When a mnemonic ends in "N" it means, in the case of a data signal, that the signal transmitted on the GP bus is the complementary value of the true signal. In the case of the control signal the "N" means that the signal performs its function on being set to "0" (active low). Most of the GP bus lines are used both inside and outside the basic mounting box. Where this does not apply it is indicated in the signal description given below.

GP Bus Signals

BI0 00N to BI0 15N

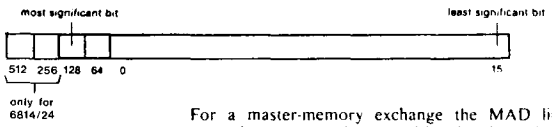
16 data lines which are used to carry data information between all system elements concerned with the transmission or reception of data signals.

The bit location is as follows:



MAD128, 64 and 00 to 15 (only MAD03, 04,08-15 used externally also)

18 address lines which carry different information according to the type of exchange. The bit location is as follows:



For a master-memory exchange the MAD lines carry the memory address and MAD15 is used as a character indicator. When set to 1 it indicates the right (least significant) character and when set to 0 the left (most significant) character.

For a master-control unit exchange the lines MAD10-15 carry the address of the control unit and lines MAD 04, 08 and 09 the function to be performed. MAD03 indicates whether or not the exchange in progress is the last. The functions are as listed below:

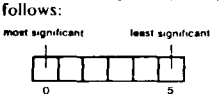
MAD04 = 0	exchange to control unit
MAD04 = 1	exchange to master
MAD08 = 0	data exchange (INR, OTR)
MAD08 = 1	command or status exchange
MAD09	special functions
MAD03 = 0	exchange not the last
MAD03 = 1	last exchange.

For a master-external register exchange the lines MAD08 to 15 carry the address of the external register. MAD04 is used to indicate whether it is a read or write operation as follows:

MAD04 = 0	write operation
MAD04 = 1	read operation.

BIEC 0 to BIEC 5

Six signal lines which represent in encoded form the interrupt raised (other than internal interrupts) having the highest priority. The format is as follows:



SCEIN

A signal *Scan External Interrupts* sent by the CPU to control units at the end of each instruction which places on the BIEC 0 to 5 lines the 6 bits representing the highest priority external interrupt detected.

ACN

A signal *function accepted* which is sent by a control unit to the CPU to indicate that the requested function is accepted by the control unit.

BUSRN

A signal *bus request* which is sent to the bus controller in the CPU by a master which requires control of the bus to effect an exchange.

BSYN

A signal *bus busy* which is shared by all masters. It is set to "0" by the master which has been given control of the bus so that the exchange can commence without interruption.

MSN

A signal *master selected* which is transmitted to all other masters by the master which has become master of the bus to block all activity of the priority selection chain. The signal is released when the master is ready for the next priority transaction.

SPYC

Internal use only (active low)

A signal *scan priority chain* sent by the bus controller to all masters in response to a BUSRN signal. The signal enables the highest priority master which has transmitted BUSRN to block the priority chain at its level.

OKO
(internal use only)

A signal generated by the bus controller after all masters have been alerted by SPYC. It is sent to the master having the highest priority (determined by hard wiring in the priority selection chain).

OKI
(internal use only)

A master which receives signal OKO regards the signal as OKI. It then retransmits a further OKO to the next master in the priority chain. The first master to receive OKI set to '1' and to retransmit OKO reset to '0' is next master of the bus.

CHA
(internal use only)

A signal *character* transmitted to the memory by the master which has control of the bus to indicate whether the exchange is to be by character or by word as follows:

CHA = 1 character operation
CHA = 0 word operation.

WRITE
(internal use only)

A signal *write* transmitted to the memory by the master which has control of the bus to write information into memory or to read information from memory as follows:

WRITE = 1 write into memory
WRITE = 0 read from memory.

CLEARN

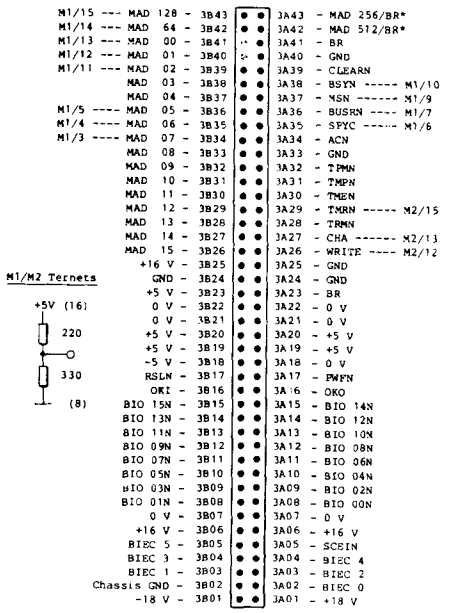
A signal *clear* transmitted by the CPU to all elements connected to the GP bus to cause a general reset to zero.

TMRN (internal use only)	A signal *master to memory* transmitted by a master to memory to validate the data on the BIO and MAD lines during an exchange. The signal also controls the timing of the exchange.
TMPN	A signal *master to peripheral* transmitted by a master to a peripheral CU to validate the address of the peripheral CU and to initialize the exchange.
TMEN	A signal *master to external register* transmitted by a master to a unit containing the addressed register to validate the address and data of the register and to control the timing of the exchange.
TRMN	A signal *register or memory to master* transmitted by a unit controlling a register or by memory in reply to TMEN or TMRN to indicate that the unit transmitting the signal is in a condition to be read. The signal is also used to terminate the exchange.
TPMN	A signal *peripheral to master* transmitted by the peripheral control unit concerned in reply to TMPN. It is also used to validate the response of the control unit and to terminate the exchange.
RSLN	An Earth signal *reset line* transmitted by the CPU power supply (or external rack power supplies) and used to protect the peripherals during the switching on and switching off power sequence. The signal is also used to generate CLEARN when switching on.
PWFN	A signal *power fail* transmitted by the CPU power supply (or external rack power supplies) to warn the CPU that power failure has been detected. The signal is also used as a facility to restart the system at the point where it has been stopped.
4 spare lines	There are 4 spare lines provided on the GP bus extension cable outside the CPU cabinet.

Backpanel 1A holds the signal-lines of the General Purpose Bus.

The following list shows the signal-names against the pin-numbers:

Note that the pins are numbered from bottom to top, the A-side at the right-hand side and the B-row at the left-hand side.



* Address lines in CPU and Memory positions,
Break outputs in other positions.

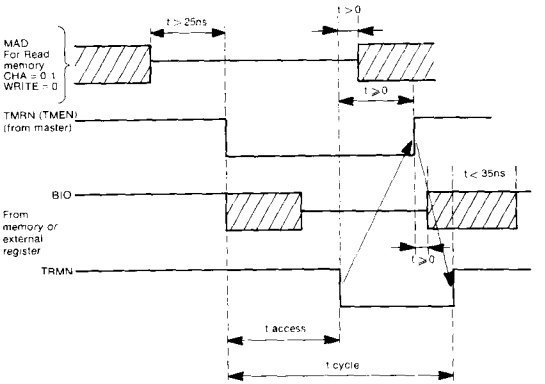


Figure 1.1-12 Timing Read Memory (or External Register)

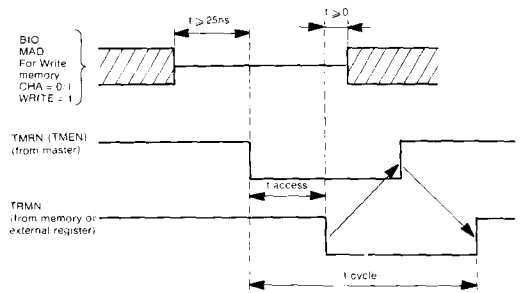
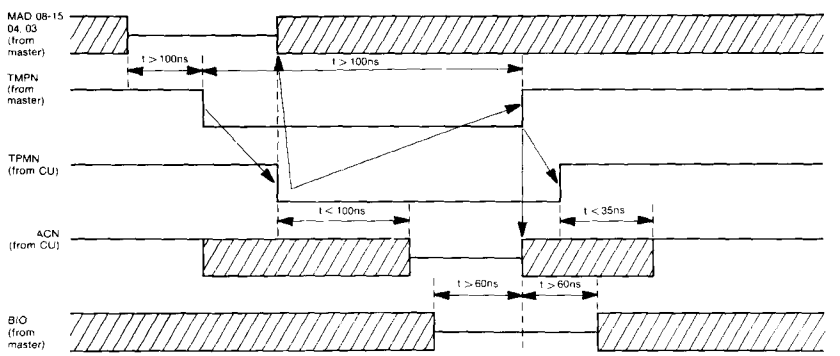


Figure 1.1-13 Timing Writing in Memory (or External Register)



Note: CU which recognises its address specifies accept or not accept function using ACN. If function accepted CU must statisize data presented at least 60 ns before TMPN goes high again. Data must remain present at least 60 ns after TMPN goes high.

Figure 1.1-14 Timing for an OTR Exchange

Priority level	Master	Remark
0	DMA (CURD 80 MDisc.)	Highest priority
1	IOP 1 (Dev. Addr. 08-0F)	
2	CHLW	
3	CHRW	
4	CPU (Except when PWF)	Not wired.

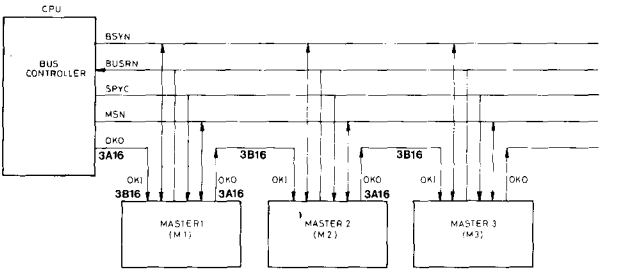


Figure 1.1-15 OKO-OKI WIRING

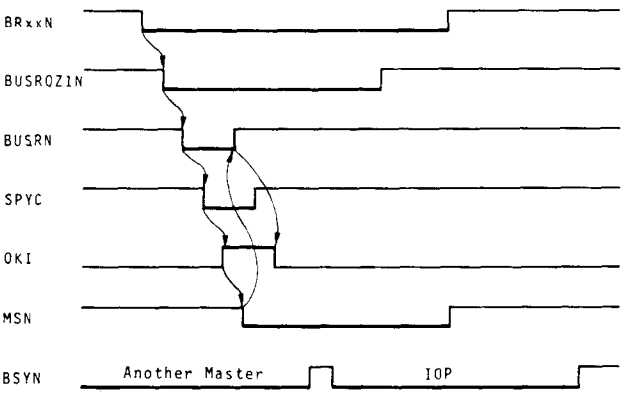
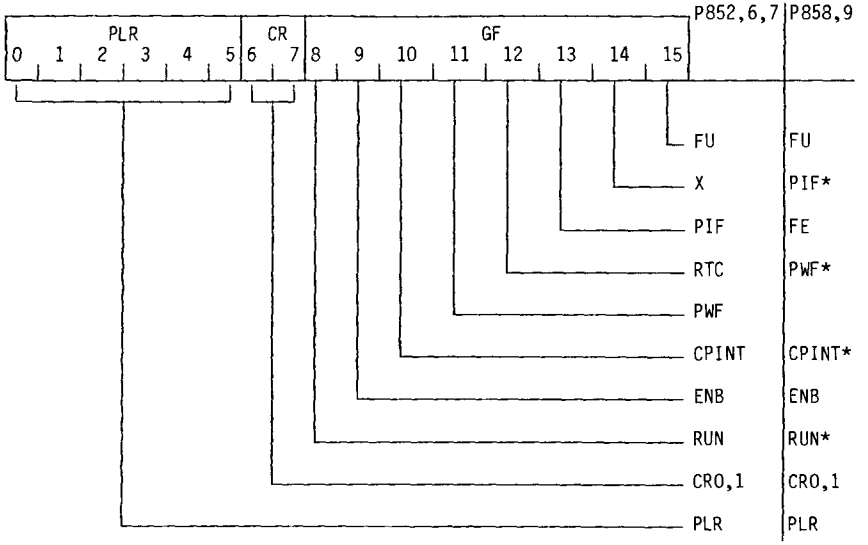


Figure 1.1-16 Busrequest and Selection

1.1.8 PROGRAM STATUS WORD (PSW)



FE : Extended System Mode
FU : User Mode
RTC : Real Time Clock
PWF : Power Failure Interrupt
CPint : Control Panel Interrupt
ENB : Interrupt ENable
RUN : CPU in RUN Mode
CR : Condition Register
PLR : Program Level Register
PIF : Program Interrupt, Stack Overflow**

* These bits are not displayable (blanked in microprogram).

CRO,1:

CRO CR1	ARITHMETIC	COMPARE	I/O
00	Zero	Equal	Accepted
01	Positive	Greater	Not Accepted
10	Negative	Less	--
11	Overflow	--	Device Address Unknown

** Stackoverflow if (A15) smaller than /100.

1.1.9 INTERRUPT SYSTEM

Interrupt levels internal

LEVEL HEX	DEC	Interr. control Address HEX	SOURCE
0	0	0	PF/AR
1	1	2	LKM/Stackoverflow;(A15),Less than /100
2	2	4	RTC
3	3	6	Not Used
4	4	8	Not Used
5	5	A	Not Used
6	6	C	Control Panel
7	7	E	Console Typewriter
.			
.			
.			
.			
1F	31	2E	Page Fault MMU for 6813 (depends on strap setting MMU)
.			
.	EXTERNAL LEVELS SEE CHAPTER 2.5		
.			
.			
.			
.			
.			
.			
.		7A*	TC6814/24 Page Fault Trap
		7C*	TC6814/24 D Type Trap
3E	63	7E*	Trap control address for invalid or priveleged instructions

* PLR not changed

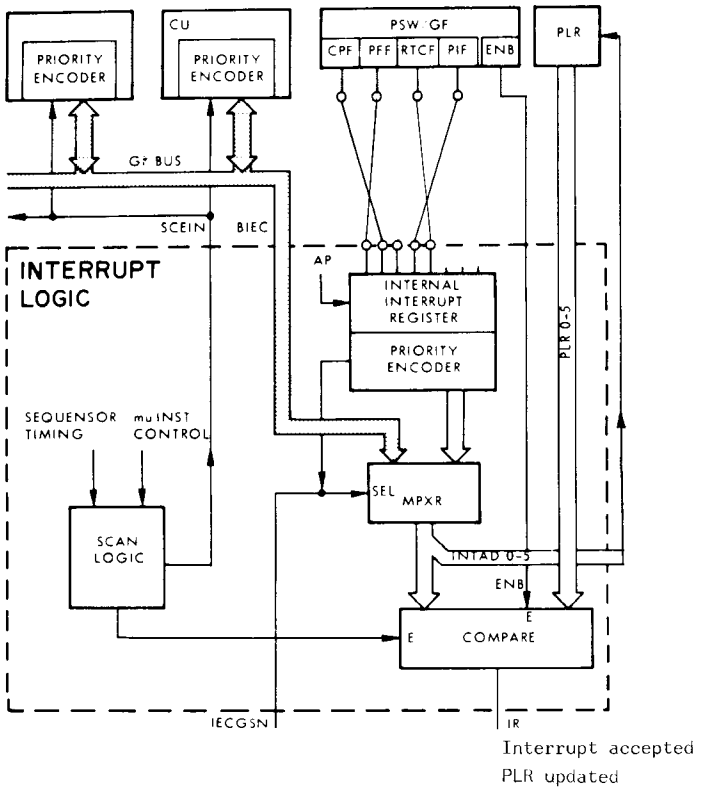
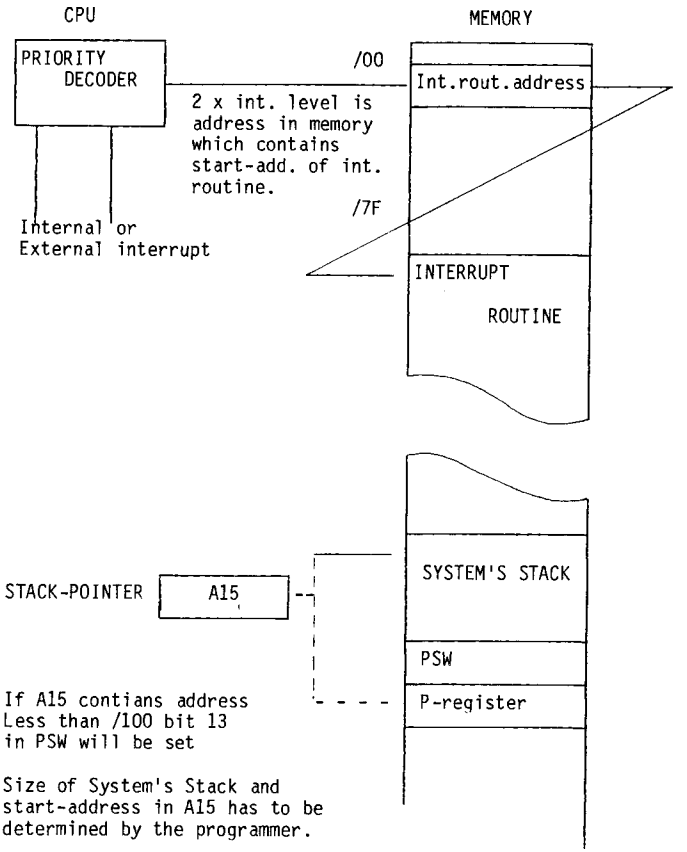


Figure 1.1-17 Interrupt System


CPU
MEMORY
PRIORITY
DECODER
/00
Int.rout.address
2 x int. level is
address in memory
which contains
start-add. of int.
routine.
/7F
Internal or
External interrupt
INTERRUPT
ROUTINE
SYSTEM'S STACK
STACK-POINTER
A15
PSW
P-register
If A15 contians address
Less than /100 bit 13
in PSW will be set
Size of System's Stack and
start-address in A15 has to be
determined by the programmer.

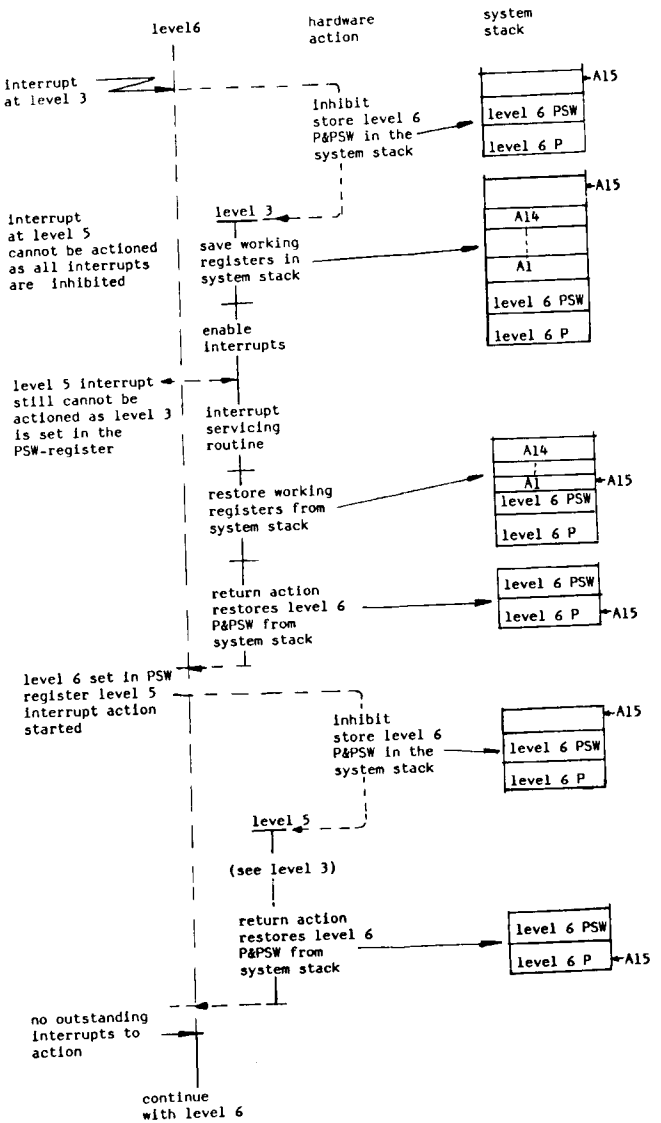


Figure 1.1-18 Diagram of Interrupt Sequence

1.1.10 I/O CHANNEL

Control Unit Modes:
Example:

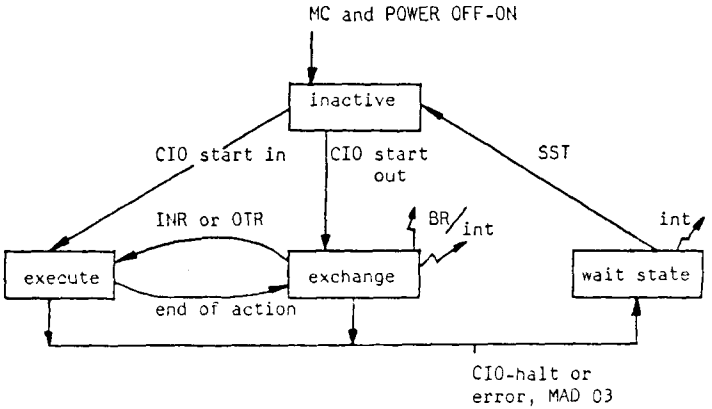
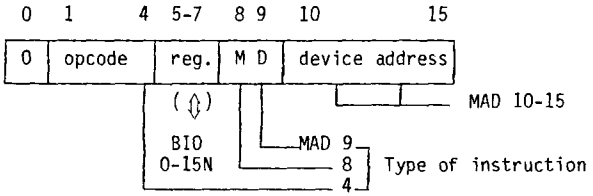


Figure 1.1-19 Control Unit Modes

I/O Instructions Format



Instruction Bits			4	8	9	
MAD Lines		03	04	08	09	Accepted in mode
CIO Start		0	0	1	1	Inactive
CIO Stop		0	0	1	0	Always
INR (Input Transfer)		0	1	0	0	Exchange
OTR (Output Transfer)		0	0	0	0	Exchange
TST (Test Status)		0	1	1	0	Always
SST (Send Status)		0	1	1	1	Wait state
INR (last) IOP		1	1	0	0	Exchange
OTR (last) IOP		1	0	0	0	Exchange

CONDITION REGISTER (DISPLAYS TPMN AND ACN - LINES)

0 0 = accepted
0 1 = not accepted
1 1 = device address not recognized

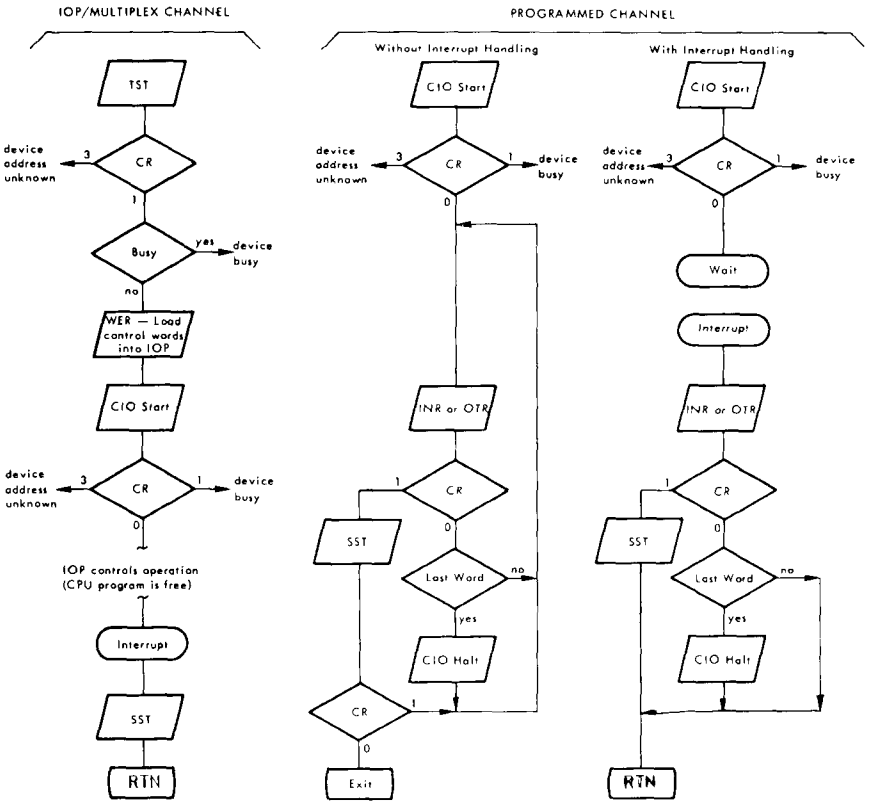


Figure 1.1-20 General Programming Sequence

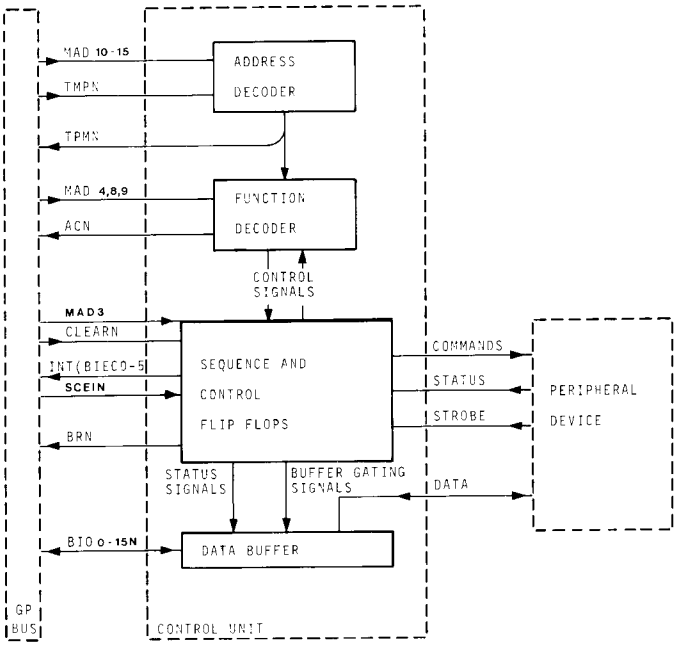
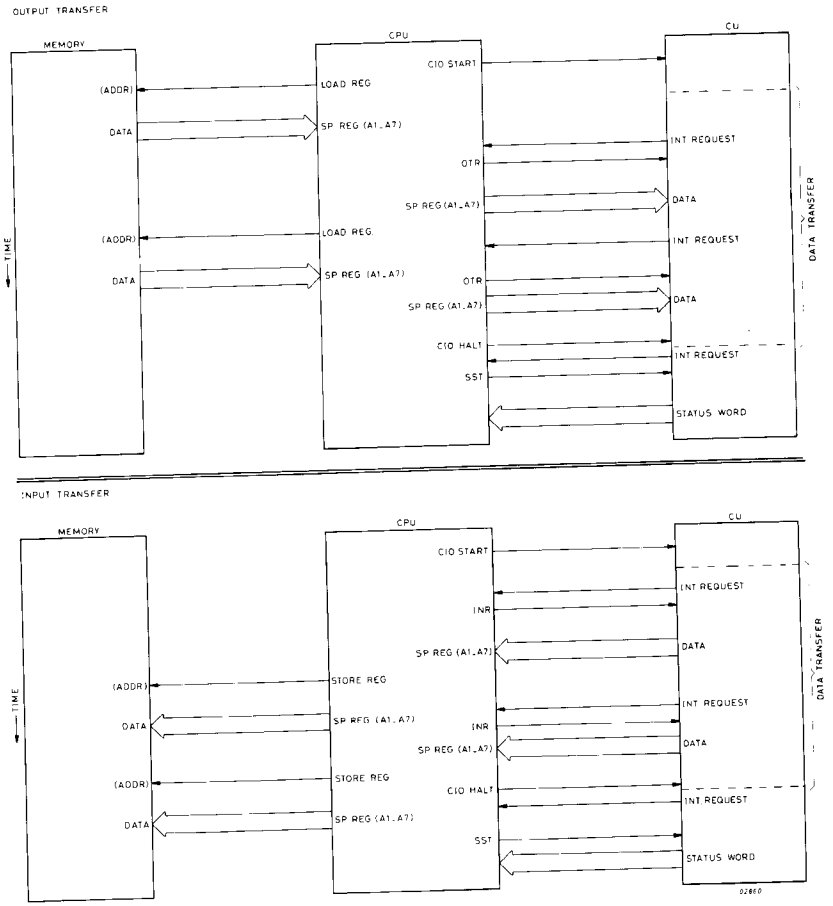
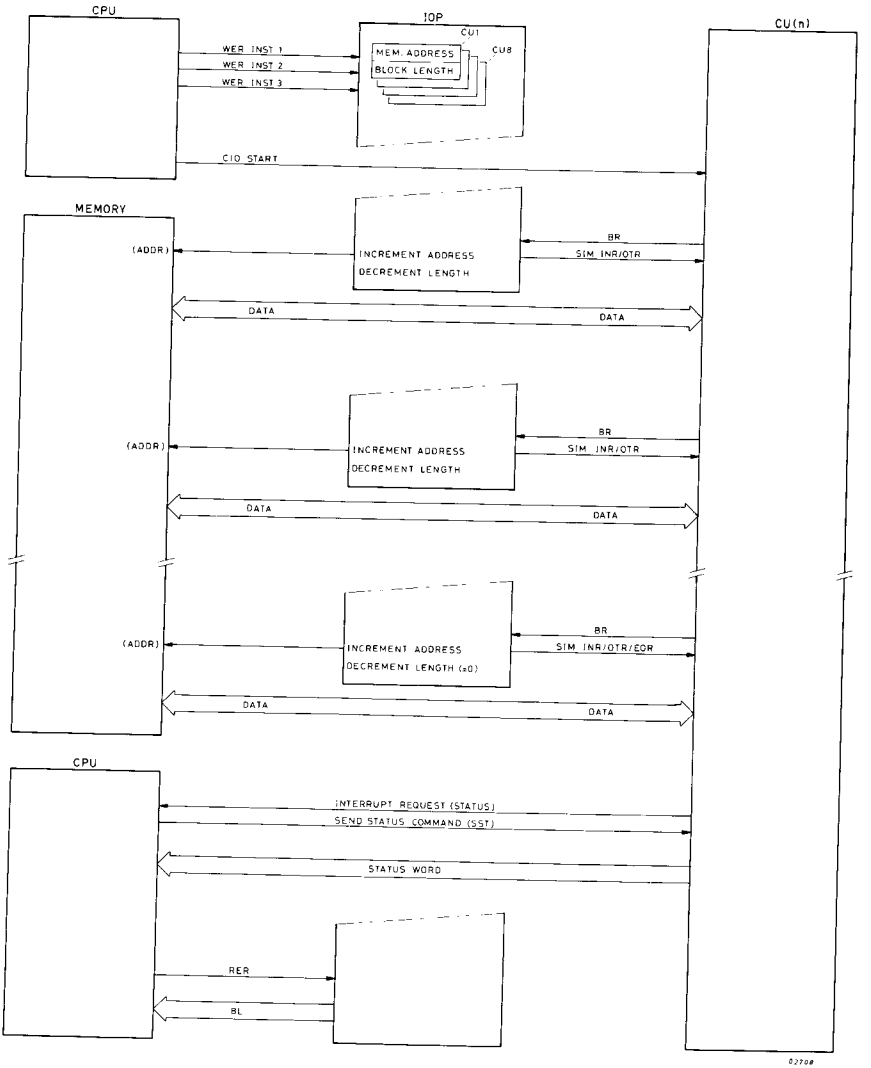


Figure 1.1-21 Block Diagram of Typical Control Unit



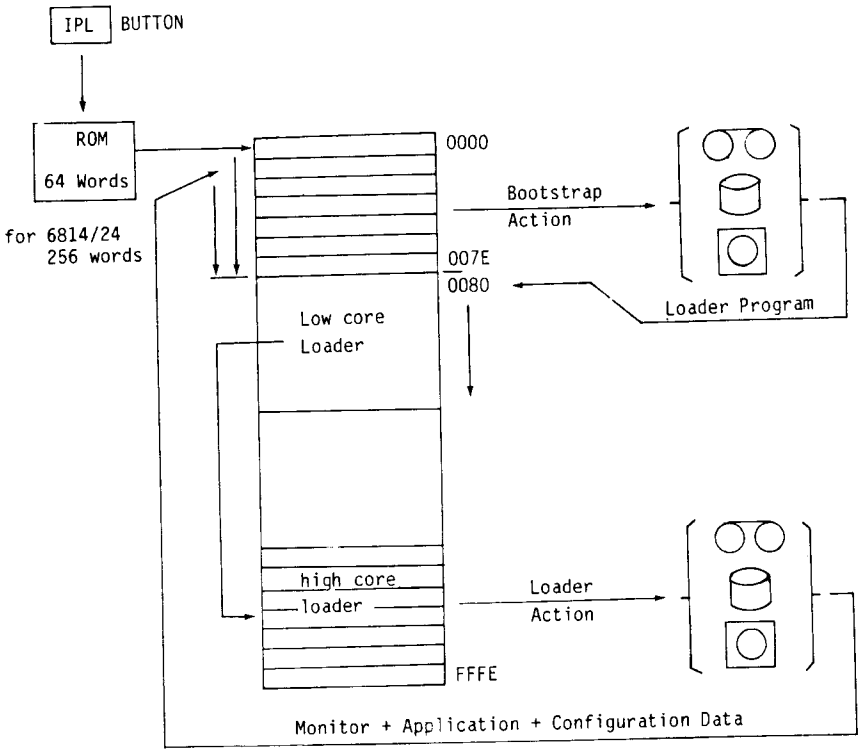
PROGRAMMED CHANNEL TRANSFERS

"Only 2 WER instructions for PTS6811/12/13"



Note-- This diagram shows the sequence for transferring a block of data between memory and single CU, (n). The IOP can multiplex up to eigth CUs; the operation shown is thus duplicated for each CU.

1.1.11 IPL PROCEDURE



```
0000                            IDENT   LOWCOR
0001                    *DATE: 820505 FOR PTS
0002                    *       EXAMPLE LOW CORE LOADER CASSETTE
0003                            AORG    /80
0004
0005 0080 FFFE          FLAG    DATA    /FFFE
0006 0082 0000                  DATA    0
0007 0084 90A1 0080     LOWSTA  IM      FLAG                    INCREMENT FLAG
0008 0088 501A                  RF(0)   SECOND                  IS IT FIRST OR SECOND TIME
0009                    *       FIND OUT MEMORY SIZE
0010 008A 8720 5555     FIRST   LDKL    A7,/5555
0011 008E 81A0 FF78             LDKL    A9,/FF78                ADDR HIGH CORE LOADER IF 32 KW MEM
0012 0092 8727          MSIZE   STR     A7,A9                   STORE (A7)
0013 0094 EF26                  CWR*    A7,A9                   CHECK IF MEM CONT IS (A7)
0014 0096 5006                  RF(0)   UPDREG                  YES UPDATE REG FOR HIGH CORE LOAD
0015 0098 99A0 1000     NO      SUKL    A9,/1000                DECREMENT ADDR HIGH CORE
0016 009C 5F0C                  RB      MSIZE
0017                    *       UPDATE REGISTERS TO LOAD HIGH CORE LOADER
0018 009E 0588          UPDREG  LDK     A5,/88                  NUMBER OF CHARACTERS HIGH CORE LOADER
0019 00A0 8606                  LDR     A6,A9                   FIRST ADDR HIGH CORE
0020 00A2 0F42                  AB      /42                     BRANCH TO BOOTSTRAP FOR HIGH CORE LOAD
0021                    *       START HIGHCORE LOADER
0022 00A4 8120 0400     SECOND  LDKL    A1,/0400
0023 00A8 412E                  OTR     A1,0,/2E                LIGHT LOAD LAMP ON SOP
0024 00AA 8386                  LDR     A11,A9                  SAVE HIGH CORE START ADDR
0025 00AC 9986                  SUR     A9,A9                   CLEAR A9
0026 00AE 9C92                  SUR     A12,A12                 CLEAR A12
0027 00B0 86A0 FFF8             LDKL    A14,/FFF8
0028 00B4 8F0E                  ABR     A11                     BRANCH TO HIGH CORE LOADER
0029                            END     FLAG
```

```
          DATE  82-05-05        IDENT    HIGHCOR

                                IDENT    HIGHCOR
0000
0001                    *DATE: 820505 FOR PTS
0002                            AORG     /FF78
0003                    *       EXAMPLE HIGH CORE LOADER FOR CASSETTE
0004
0005 FF78 8500          HIGHST  LDR      A5,0             SAVE HIGH CORE START ADDR
0006 FF7A 1D02                  SUK      A5,2
0007 FF7C 02C0                  LDK      A2,/C0
0008 FF7E 3B64                  SRL      A3,4
0009 FF80 2301                  ANK      A3,/01
0010 FF82 920C                  ADR      A2,A3
0011 FF84 8306                  LDR      A3,A9
0012 FF86 0700                  LDK      A7,0
0013 FF88 0600          A3IA13  LDK      A6,0
0014 FF8A 840C                  LDR      A4,A3
0015 FF8C 010A          READH   LDK      A1,/0A           READ BLOCK
0016 FF8E 41CE                  CIO      A1,1,/0E
0017 FF90 490E          INRH    INR      A1,0,/0E
0018 FF92 5408                  RF(4)    SSTH
0019 FF94 EC14                  CWR      A4,A5            IS THERE MEMORY OVERFLOW
0020 FF96 505E                  RF(0)    MEMOFL
0021 FF98 E131          STPROG  SCR      A1,A4
0022 FF9A 1401                  ADK      A4,1             INCREMENT MEM ADDR
0023 FF9C 49CE          SSTH    SST      A1,/0E           STATUS?
0024 FF9E 5C10                  RB(4)    INRH
0025 FFA0 A120 FCFF     CHSTAT  ANKL     A1,/FCFF         CHECK ON STATUS ERROR
0026 FFA4 543A                  RF(4)    STATER
0027 FFA6 1C10                  SUK      A4,/10
0028 FFA8 8590                  LDR      A13,A4
0029 FFAA 1C02                  SUK      A4,2
0030 FFAC 1402                  ADK      A4,2
0031 FFAE 0610          A6ZERO  LDK      A6,/10
0032 FFB0 871C                  LDR      A7,A7
0033 FFB2 501E                  RF(0)    A7ZERO
0034 FFB4 8130                  LDR*     A1,A4
0035 FFB6 5606          CHA1    RF(6)    A1NEG
0036 FFB8 82AC                  LDR*     A10,A3
0037 FFBA 92B6                  ADR      A10,A9
0038 FFBC 5702                  RF       CONT
0039 FFBE 82AC          A1NEG   LDR*     A10,A3
0040 FFC0 82CD FFF8     CONT    ST       A10,/FFF8,A3
0041 FFC4 1302                  ADK      A3,2
0042 FFC6 EB16                  CWR      A3,A13
0043 FFC8 5B42                  RB(0)    A3IA13
0044 FFCA 1E01                  SUK      A6,1
0045 FFCC 5820                  RB(0)    A6ZERO
0046 FFCE 3941                  SLL      A1,1
0047 FFD0 5F1C                  RB       CHA1
0048 FFD2 872C          A7ZERO  LDR*     A7,A3
0049 FFD4 9706                  ADR      A7,A9
0050 FFD6 1308                  ADK      A3,8
0051 FFD8 1E04                  SUK      A6,4
0052 FFDA 8130                  LDR*     A1,A4
0053 FFDC 3944                  SLL      A1,4
0054 FFDE 5F2A                  RB       CHA1
0055 FFE0 39C3          STATER  SLC      A1,3
0056 FFE2 5610                  RF(6)    ERROR
0057 FFE4 462E                  OTR      A6,0,/2E
0058 FFE6 1B08                  SUK      A3,8
0059 FFE8 818C                  LDR      A9,A3
0060 FFEA 859C                  LDR      A13,A7
0061 FFEC 8492                  LDR      A12,A12
0062 FFEE 5402                  RF(4)    BRA12
0063 FFF0 BF16                  ABR      A13
0064 FFF2 BF12          BRA12   ABR      A12
0065 FFF4 1601          ERROR   ADK      A6,1
0066 FFF6 1601          MEMOFL  ADK      A6,1
0067 FFF8 E618                  ECR      A6,A6
0068 FFFA 462E                  OTR      A6,0,/2E         ERROR DISPLAY ONSOP
0069 FFFC 207F                  HLT                       ERROR STOP
0070 FFFE 5F88                  RB       HIGHST
#S     0000 5F88
*******                                  *
0071                            END      HIGHST
```

1.1.12 CONTENTS IPL PROM 5131 110 01142

```
          DATE  82-05-05          IDENT    B1142     820505


0000                              IDENT    B1142                  820505
0001                      *       FOR IPL FROM CASSETTE,2.5M AND 5M DISC AND MAGNETIC TAPE
0002                      *       CONTENTS OF A3 FOR SOP SWITCHES:
0003                      *SW1     /FE00    DCR DRIVE 0
0004                      *SW2     /FD00    DCR DRIVE 1
0005                      *SW3     /FC80    CARTRIDGE DISC DRIVE 0
0006                      *SW4     /FC40    FIXED DICS DRIVE 0
0007                      *SW5     /FC20    MAGNETIC TAPE DRIVE 0
0008                      *SW6     /FC10    NOT USED
0009                      *SW7     /FC08    NOT USED
0010                      *SW8     /FC04    NOT USED
0011                      *SW9     /FC02    NOT USED
0012                      *SW10    /FC01    NOT USED
0013
0014
0015 0000 41EE            BOOT     CIO      A1,1,/2E               START SOP
0016 0002 4B2E                     INR      A3,0,/2E               READ SOP SWITCH
0017 0004 5C04                     RB(NA)   *-2
0018 0006 41AE                     CIO      A1,0,/2E               STOP SOP
0019 0008 3BA4                     SRN      A3,A1                  WHAT SWITCH
0020 000A 1905                     SUK      A1,5                   IS THE SWITCH LEGAL?
0021 000C 5A0E                     RB(N)    BOOT                   NO READ NEXT SWITCH
0022 000E E444 0022 R              LC       A4,DEVADR,A1           LOAD DEVICE ADDRESS
0023 0012 243F                     ANK      A4,/3F
0024 0014 0278                     LDK      A2,SIO1-BOOT           ADDRESS OF CIO START
0025 0016 AC29                     ORRS     A4,A2                  CHANGE DEVICE ADDRESS IN CIO
0026 0018 027A                     LDK      A2,SSTI-BOOT           ADDRESS OF SST
0027 001A AC29                     ORRS     A4,A2                  CHANGE DEVICE ADDR IN SST
0028 001C B7A0 63CB                LDKL     A15,/63CB              INIT A15 FOR DISC IPL
0029 0020 AF90                     ORR      A15,A4                 MODIFY BY DA
0030 0022 0420            DEVADR   DATA     /0420                  USED FOR DEV ADDR EXECUTED AS LDK A2,/20
0031 0024 0806                     DATA     /0806                  EXECUTED AS AB(0) /06 IS NOP
0032 0026 06B0                     LDK      A6,/B0                 BASE ADDRESS LOW CORE LOADER
0033 0028 0278                     LDK      A2,EXCOM-BOOT          START ADDRESS COMMAND ROUTINE
0034 002A 1901                     SUK      A1,1                   IS IT MAGNETIC TAPE
0035 002C 5224                     RF(N)    MTAP
0036 002E 1902                     SUK      A1,2                   IS IT DISC
0037 0030 5234                     RF(N)    DISC
0038 0032 3101            CASS     XRK      A1,1                   SELECT DRIVE
0039 0034 F409                     CFR      A4,A2
0040 0036 0102                     LDK      A1,2                   LOCK SELECTED DRIVE
0041 0038 F409                     CFR      A4,A2
0042 003A 0108                     LDK      A1,8                   SEARCH BEGIN OF TAPE
0043 003C F409                     CFR      A4,A2
0044 003E 010C                     LDK      A1,/C                  SEARCH TAPE MARK
0045 0040 F409                     CFR      A4,A2
0046 0042 010A            CASS10   LDK      A1,/A                  READ 1 BLOCK
0047 0044 41CE                     CIO      A1,1,/0E               START CHCR
0048 0046 490E            CASS20   INR      A1,0,/0E               READ CHARACTER
0049 0048 5404                     RF(NA)   CASS30                 IF NOT ACCEPTED CHECK STATUS
0050 004A E139                     SCR      A1,A6                  STORE CHARACTER IN MEMORY
0051 004C 1601                     ADK      A6,1                   INCREMENT MEM ADDRESS
0052 004E 49CE            CASS30   SST      A1,/0E                 GET STATUS
0053 0050 5C0C                     RB(NA)   CASS20                 IF NOT ACCEPTED READ NEXT CHARACTER
0054 0052 0F84                     AB       /84                    START LOW CORE LOADER
0055 0054 0151            MTAP     LDK      A1,/51                 ON LINE
0056 0056 F409                     CFR      A4,A2
0057 0058 0124                     LDK      A1,/24                 SEARCH FILE MARK
0058 005A F409                     CFR      A4,A2
0059 005C 05FF                     LDK      A5,/FF                 FIRST CONTROL WORD IOP
0060 005E 7518                     WER      A5,/18                 WRITE FIRST CONTROL WORD
0061 0060 7619                     WER      A6,/19                 SECOND CONTROL WORD
0062 0062 0102                     LDK      A1,2                   READ 1 BLOCK
0063 0064 570E                     RF       EXIT
0064 0066 0103            DISC     LDK      A1,3                   SEEK TO ZERO
0065 0068 F409                     CFR      A4,A2
0066 006A B120 80CD                LDKL     A1,/80CD               FIRST CONTROL WORD
0067 006E 7110                     WER      A1,/10                 WRITE FIRST CONTROL WORD TO IOP
0068 0070 7611                     WER      A6,/11                 AND THE SECOND
0069 0072 010C                     LDK      A1,/C                  READ SECTOR NUMBER 3
0070 0074 F409            EXIT     CFR      A4,A2
0071 0076 0F84                     AB       /84                    START LOW CORE LOADER
0072      0078            EXCOM    EQU      *
0073 0078 41C8            SIO1     CIO      A1,1,8                 START CONTROLLER
0074 007A 4BC8            SSTI     SST      A3,8                   GET STATUS
0075 007C 5C04                     RB(NA)   *-2
0076 007E F030                     RTN      A4
0077
0078
0079
0080                              END      BOOT
```

1.1.13 CONTENTS IPL PROM 4011P

```
        DATE  82-05-05        IDENT    B4011P


0000                          IDENT    B4011P
0001                    *DATA: 820505 FOR PTS
0002                    *      FOR IPL FROM CASSETTE, FLEX DISC AND 2.5 AND 5M DISC
0003                    *      CONTENTS OF A5 FOR SOP SWITCHES
0004                    *SW1   /FE00    DCR DRIVE 0
0005                    *SW2   /FD00    DCR DRIVE 1
0006                    *SW3   /FC80    CARTRIDGE DISC DRIVE 0
0007                    *SW4   /FC40    FIXED DISC DRIVE 0
0008                    *SW5   /FC20    FLD DRIVE 0 (MUX)
0009                    *SW6   /FC10    FLD DRIVE 1 (MUX)
0010                    *SW7   /FC08    FLD DRIVE 0 (PC)
0011                    *SW8   /FC04    FLD DRIVE 1 (PC)
0012                    *SW9   /FC02    NOT USED
0013                    *SW10  /FC01    NOT USED
0014
0015
0016 0000 44EE          START  CIO      A4,1,/2E              START SOP
0017 0002 4D2E                 INR      A5,0,/2E              READ SOP SWITCH
0018 0004 5C04                 RB(4)    *-2
0019 0006 44AE                 CIO      A4,0,/2E              STOP SOP
0020 0008 3DB0                 SRN      A5,A4                 WHAT SWITCH IS DEPRESSED
0021 000A E350 001B            LC       A3,/1B,A4
0022 000E 233F                 ANK      A3,/3F
0023 0010 0254                 LDK      A2,/54                ADDR CIO INSTR
0024 0012 AB29                 ORRS     A3,A2                 MODIFY CIO START
0025 0014 0660                 LDK      A6,/60                ADDR SST INSTR
0026 0016 AB39                 ORRS     A3,A6                 MODIFY SST
0027 0018 8520 80CD            LDKL     A5,/80CD              FIRST CONTR. WORD IOP FOR DISC
0028 001C E719                 DATA     /E719                 EXECUTED AS ECR A7,A6
0029 001E 0911                 AB(1)    /11
0030 0020 0120                 LDK      A1,/20                STACKPOINTER
0031 0022 0806                 AB(0)    /6
0032 0024 0680                 LDK      A6,/80                FIRST ADDRESS OF LOW CORE LOADER
0033 0026 1C04                 SUK      A4,4                  IPL FROM WHAT DEVICE
0034 0028 5240                 RF(2)    FLDPC
0035 002A 1C02                 SUK      A4,2
0036 002C 5248                 RF(2)    FLDMUX
0037 002E 1C02                 SUK      A4,2
0038 0030 5214                 RF(2)    DISC
0039 0032 3401          CASS   XRK      A4,1                  DRIVE 0 OR 1
0040 0034 F109                 CFR      A1,A2                 SELECT CASS DRIVE
0041 0036 0402                 LDK      A4,2                  LOCK CASS DRIVE
0042 0038 F109                 CFR      A1,A2
0043 003A 0408                 LDK      A4,8                  SBOT SEARCH BEGIN OF TAPE
0044 003C F109                 CFR      A1,A2
0045 003E 040C                 LDK      A4,/C                 STMF SEARCH TAPE MARK FORW
0046 0040 F109                 CFR      A1,A2
0047 0042 040A                 LDK      A4,/0A                READ 1 BLOCK
0048 0044 570A                 RF       READ
0049 0046 0403          DISC   LDK      A4,3                  SEEK TO CYL 0
0050 0048 F109                 CFR      A1,A2
0051 004A 7519                 WER      A5,/10                IOP CW1
0052 004C 7611                 WER      A6,/11                IOP CW2
0053 004E 040C                 LDK      A4,/C                 READ SECTOR 3
0054 0050 F109          READ   CFR      A1,A2
0055 0052 AF8C                 ORR      A15,A3                PRESET REG A15
0056 0054 0F84          EXIT   AB       /84                   GOTO LOW CORE LOADER
0057 0056 44C8          CIO    CIO      A4,1,/08              SUBROUTINE
0058 0058 4C0E          INR    INR      A4,0,/0E              READ DATA
0059 005A 5404                 RF(4)    SST
0060 005C E439                 SCR      A4,A6                 STORE DATA IN MEMORY
0061 005E 1601                 ADK      A6,1                  INCREMENT MEMORY ADDRESS
0062 0060 4CC8          SST    SST      A4,/08                STATUS?
0063 0062 5C0C                 RB(4)    INR
0064 0064 87A0 63C8            LDKL     A15,/63C8             LOAD A15
0065 0068 F024                 RTN      A1
0066                    *      FLEX DISC PROGRAMMED CHANNEL
0067 006A 0459          FLDPC  LDK      A4,/59                ADDR BIT 8-15 INR INSTR
0068 006C E331                 SCR      A3,A4                 MODIFY INR INSTR
0069 006E 045C                 LDK      A4,/5C
0070 0070 B731                 XRRS     A7,A4                 CHANGE SCR IN STR INSTR
0071 0072 045E                 LDK      A4,/5E
0072 0074 9031                 IMR      A4                    CHANGE ADK A6,1 IN ADK A6,2
0073                    *      FLEX DISC HARDWARE CHANNEL(MUX)
0074 0076 7512          FLDMUX WER      A5,/12                IOP CW 1
0075 0078 7613                 WER      A6,/13                IOP CW 2
0076 007A 8420 C020            LDKL     A4,/C020              READ 4 SEGMENT FROM SEGM 4
0077 007E 5F30                 RB       READ
0078                           END      START
```

1.1.14 CONTENTS IPL ROM B5300 (5131 194 35300/66)

```
        DATE  82-03-06          IDENT    B5300


0000                            IDENT    B5300
0001                    *       DATE: 82 06 02 FOR PTS 6814/24
0002                    *       FOR IPL FROM CASSETTE, FLEX DISC AND 2.5 AND 5M DISC
0003                    *       AND BIG DISC
0004                    *       CONTENTS OF A5 FOR SOP SWITCHES
0005                    *SW1    /FE00    DCR DRIVE 0
0006                    *SW2    /FD00    DCR DRIVE 1
0007                    *SW3    /FC80    CARTRIDGE DISC DRIVE 0
0008                    *SW4    /FC40    FIXED DISC DRIVE 0
0009                    *SW5    /FC20    BIGD DRIVE 0
0010                    *SW6    /FC10    BIGD DRIVE 1
0011                    *SW7    /FC08    FLD DRIVE 0
0012                    *SW8    /FC04    FLD DRIVE 1
0013                    *SW9    /FC02    CARTRIDGE DISC DRIVE 1
0014                    *SW10   /FC01    FIXED DISC DRIVE 1
0015
0016 0000 57FE          START   RF       BEGIN
0017 0002 0680          SORT    LDK      A6,/80                  BASE ADDR LOW COR LOADER
0018 0004 EC20 0004             CWK      A4,4                    IS IT CASSETTE?
0019 0008 503A                  RF(E)    CASS
0020                    *UPDATE DEVICE ADDRESS IN CIO AND SST
0021 000A 3C42          NOCASS  SLL      A4,2
0022 000C 9310                  ADR      A3,A4
0023 000E E34C 0134 R           LC       A3,DA,A3                GET DEVICE PARAMETER
0024 0012 E329                  SCR      A3,A2                   MODIFY CIO
0025 0014 E341 006D R           SC       A3,SST+1                MODIFY SST
0026 0018 1400                  ADK      A4,0                    IS IT BIG DISC
0027 001A 5056                  RF(E)    BIGD
0028 001C AB20 6300     NOBIGD  ORKL     A3,/6300                MAKE PARAMETER FOR A15 WITH DISC
0029 0020 0403                  LDK      A4,3                    SEEK 0 COMMAND FOR FL1M AND DISC
0030 0022 F109                  CFR      A1,A2                   DO SEEK 0 COMMAND
0031 0024 2710                  ANK      A7,/10                  IF A7=/10 THEN IT SI NOT FL1M BUT FL0.25
0032 0026 545A                  RF(NZ)   FL0.25M
0033 0028 8720 5706             LDKL     A7,/5706                LOAD RF(7) =+8
0034 002C 8735                  STR      A7,A5                   CHANGE INR INTO RF
0035 002E A311                  TM       A3,A4                   IS IT FLIMCU OR DISC
0036 0030 540C                  RF(NZ)   FL1MCU
0037 0032 040C          DISC    LDK      A4,/C                   FOR READ SECTOR 3
0038 0034 7110                  WER      A1,/10                  FIRST CONTROL WORD IOP
0039 0036 7611                  WER      A6,/11                  SECOND CONTROL WORD IOP
0040 0038 B78C                  LDR      A15,A3                  PARAMETER /63XX IN A15 (AS PB00)
0041 003A F109          READ    CFR      A1,A2                   READ LOW COR LOADER OR ELSE
0042 003C 0F84                  AB       /84                     START LOW CORE LOADER
0043 003E 0410          FL1MCU  LDK      A4,/10                  READ FROM SECTOR 4
0044 0040 574C                  RF       CONT
0045 0042 5F0A                  RB       READ                    ?
0046 0044 E40B          CASS    ECR      A4,A2
0047 0046 AC41 0068 R           ORS      A4,STR                  CHANGE STR INSTR
0048 004A 840C                  LDR      A4,A3
0049 004C 2401                  ANK      A4,1                    DRIVE 0 OR 1
0050 004E F109          SEL     CFR      A1,A2                   SELECT DRIVE
0051 0050 0402                  LDK      A4,2                    LOCK
0052 0052 F109          LOCK    CFR      A1,A2                   LOCK SEL CASS
0053 0054 0408                  LDK      A4,8                    SEARCH BEGING OF TAPE
0054 0056 F109          SBOT    CFR      A1,A2
0055 0058 040C                  LDK      A4,/C                   READ TAPE MARK
0056 005A F109          STMF    CFR      A1,A2
0057 005C 040A                  LDK      A4,/A                   READ BLOCK
0058 005E 5F26                  RB       READ                    READ LOW  CORE LOADER
0059 0060 0000                  DATA     0
0060 0062 44CE          CIO     CIO      A4,1,/0E                START CONTROLLER
0061 0064 4F0E          INR     INR      A7,0,/0E                READ CHAR OR WORD PC
0062 0066 5404                  RF(NA)   SST
0063 0068 8739          STR     STR      A7,A6                   STORE CHAR OR WORD
0064 006A 1601                  ADK      A6,1                    UPDATE ADDR
0065 006C 4FCE          SST     SST      A7,/0E                  ASK STATUS
0066 006E 5C0C                  RB(NA)   INR
0067 0070 F024                  RTN      A1
0068 0072 2701          BIGD    ANK      A7,1
0069 0074 3F44                  SLL      A7,4
0070 0076 851C                  LDR      A5,A7
0071 0078 AF41 012A R           ORS      A7,COMBIG+2
0072 007C 8420 0128 R           LDKL     A4,COMBIG               COMMAND BUFFER ADDR
0073 0080 5F48                  RB       READ                    READ SECTOR 0 FROM DISC
0074 0082 233F          FL0.25M ANK      A3,/3F                  TAKE DEVICE ADDRESS
0075 0084 E335                  SCR      A3,A5                   UPDATE INR ISTR
0076 0086 046A                  LDK      A4,/6A
0077 0088 9031                  IMR      A4                      UPDATE ADK A6,1 IN ADK A6,2
0078 008A 8420 C020             LDKL     A4,/C020                READ 4 SEGMENTS FROM SEGM 4
0079 008E 7112          CONT    WER      A1,/12                  FIRST CONTROL WORD IOP
0080 0090 7613                  WER      A6,/13                  SECOND CONTROL WORD IOP
0081 0092 5F5A                  RB       READ                    READ LOW CORE LOADER
```

```
0082 0094 0000 0000              DATA    0,0,00,0,0,0,0,0,0
     0098 0000 0000
     009C 0000 0000
     00A0 0000 0000
     00A4 0000
0083 00A6 0000 0000              DATA    0,0,0,0,0,0,0,0,0
     00AA 0000 0000
     00AE 0000 0000
     00B2 0000 0000
     00B6 0000
0084 00B8 0000 0000              DATA    0,0,0,0,0,0,0,0,0
     00BC 0000 0000
     00C0 0000 0000
     00C4 0000 0000
     00C8 0000
0085 00CA 0000 0000              DATA    0,0,0,0,0,0,0,0,0
     00CE 0000 0000
     00D2 0000 0000
     00D6 0000 0000
     00DA 0000
0086 00DC 0000 0000              DATA    0,0,0,0,0,0,0,0,0
     00E0 0000 0000
     00E4 0000 0000
     00E8 0000 0000
     00EC 0000
0087 00EE 0000 0000              DATA    0,0,0,0,0,0,0,0,0
     00F2 0000 0000
     00F6 0000 0000
     00FE 0000
0088 0100 0263          BEGIN    LDK     A2,/63                  ADDR CIO DA
0089 0102 8120 8100              LDKL    A1,/8100                FIRST CW IOP READ 256 WORDS
0090 0106 44EE                   CIO     A4,1,/2E                START SOP
0091 0108 4D2E          READS    INR     A5,0,/2E                READ SOP SWITCH
0092 010A 5C04                   RB(NA)  READS
0093 010C 3DB0                   SRN     A5,A4                   WHAT SW
0094 010E 9C11                   NGR     A4,A4
0095 0110 1409                   ADK     A4,9
0096 0112 E350 014E R            LC      A3,NUMB,A4
0097 0116 23FF                   ANK     A3,/FF
0098 0118 E450 0144 R            LC      A4,NUM,A4
0099 011C 24FF                   ANK     A4,/FF
0100 011E 43AE                   CIO     A3,0,/2E                STOP SOP
0101 0120 4DC9                   SST     A5,9                    STATUS FLCU FLOPPY INSERTED AFTER IPL
0102 0122 0565                   LDK     A5,/65                  INR DA ADDR
0103 0124 870C                   LDR     A7,A3
0104 0126 0F02                   AB      2                       BRANCH TO SORT
0105 0128 E000          COMBIG   DATA    /E000                   SEEK TO 0
0106 012A 0800                   DATA    /0800                   READ SECTOR 0 HEAD 0
0107 012C 0180 0180              DATA    /180,/180               RECORD AND BLOCKLENGTH
0108 0130 0000 0000              DATA    /0000,/0000             BASE ADDRESS 0000
0109 0134 D7D7          DA       DATA    /D7D7                   BIG DISC DRIVE 0
0110 0136 F7F7                   DATA    /F7F7                   BIG DISC DRIVE 1
0111 0138 C9D9                   DATA    /C9D9                   FIRST AND SEC FLD
0112 013A E9F9                   DATA    /E9F9                   THIRT AND FOURTH FLD
0113 013C C8E8                   DATA    /C8E8                   DRIVE 0 DISC CARTR AND FIXED
0114 013E D8F8                   DATA    /D8F8                   DRIVE 1 DISC
0115 0140 D7F7                   DATA    /D7F7                   BIG DISC DRIVE 0,1
0116 0142 0000                   DATA    0
0117 0144 0404 0202     NUM      DATA    /0404,/0202,0,/0101,/0202
     0148 0000 0101
     014C 0202
0118 014E 0001 0001     NUMB     DATA    1,1,1,1,/203
     0152 0001 0001
     0156 0203
0119
0120
0121
0122                             END     START



          SYMBOL TABLE

  BEGIN   0100  R   BIGD    0072  R   CASS    0044  R   CID     0062  R
  COMBIG  0128  R   CONT    008E  R   DA      0134  R   DISC    0032  R
  FLO2SM  0082  R   FLIMCU  003E  R   INR     0064  R   LOCK    0052  R
  NOBIGD  001C  R   NOCASS  000A  R   NUM     0144  R   NUMB    014E  R
  READ    003A  R   READS   0108  R   SBOT    0056  R   SEL     004E  R
  SORT    0002  R   SST     006C  R   START   0000  R   STMF    005A  R
  STR     0068  R

          ASS.ERR.    0000

:EOF
PROG ELAPSED TIME:  00H-00M-34S-380MS-
```

1.1.15 CONTENTS IPL ROM BOOT 6A (5131 194 25900)

```
          DATE  82-03-30        IDENT    BOOT6A    81-08-07  POHO


0000                            IDENT    BOOT6A                81-08-07  POHO
0001
0002
0003                    *       THIS BOOTSTRAP IS RELATED TO
0004                    *       TSB 506/80 - BOOTSTRAP 64
0005
0006
0007                    *
0008                    *       B O O T S T R A P   6 0 0 0
0009                    *
0010
0011
0012
0013
0014
0015                    *       SOP SWITCH 1 :  CASSETTE UNIT 1
0016                    *                  2 :           UNIT 2
0017
0018                    *       SOP SWITCH 3 :  CARTRIDGE DISC 6875,6876
0019                    *                  4 :  FIXED     DISC 6875,6876
0020
0021                    *       SOP SWITCH 5 :  80MB DISC (OLD CU) UNIT 1
0022                    *                  6 :                     UNIT 2
0023
0024                    *       SOP SWITCH 7 :  FLOPPY DISC UNIT 1 (ALL TYPES)
0025                    *                  8 :              UNIT 2 (ALL TYPES)
0026
0027                    *       SOP SWITCH 9 :  NOT USED
0028                    *                 10 :  NOT USED
0029                            EJECT
0030      000E          CHCR    EQU     /0E
0031      002E          SOP     EQU     /2E
0032      0009          FDDA    EQU     9
0033      0012          FDIOP   EQU     /12
0034      0010          DKIOP   EQU     /10
0035      0084          IPLSTA  EQU     /84
0036                    *
0037                    *       READ SOP
0038                    *
0039      0000          BOOT    EQU     *
0040 0000 06B0                  LDK     A6,/80                  START ADDRESS OF IPL
0041 0002 02A3                  LDK     A2,SIOI+1-BOOT          SUBROUTINE ADDRESS
0042 0004 8120 8100             LDKL    A1,/8100                WER REGISTER AND STACK ADDRESS
0043 0008 E308                  ECR     A3,A2                   A3:=/6300
0044 000A 44EE                  CIO     A4,1,SOP
0045 000C 4D2E                  INR     A5,0,SOP
0046 000E 5C04                  RB(NA)  *-2
0047 0010 44AE                  CIO     A4,0,SOP
0048 0012 3D00                  SRN     A5,A4
0049 0014 0565                  LDK     A5,INRI+1-BOOT          ADDRESS TO INR INSTRUCTION
0050 0016 1C08                  SUK     A4,8
0051 0018 5830                  RF(NN)  CASS                    TAPE CASSETTE
0052 001A E350 0040             LC      A3,DEVADR-BOOT,A4       DEVICE ADDRESS
0053 001E E329                  SCR     A3,A2                   UPDATE ADDRESS IN CIO
0054 0020 E341 006D             SC      A3,SSTI+1-BOOT          UPDATE ADDRESS IN SST
0055                            EJECT
0056                    *
0057                    *       DISC
0058                    *
0059      0024          DISC    EQU     *
0060 0024 0403                  LDK     A4,3
0061 0026 F109                  CFR     A1,A2                   SEEK ZERO
0062 0028 2710                  ANK     A7,/10
0063 002A 5446                  RF(NZ)  FDPC                    0.25 MEG FLOPPY DRIVE
0064 002C A311                  TM      A3,A4
0065 002E 5410                  RF(NZ)  FD1M                    1 MEG FLOPPY
0066 0030 040C                  LDK     A4,/C                   SECTOR 3
0067 0032 7110                  WER     A1,DKIOP
0068 0034 7611                  WER     A6,DKIOP+1              BUFFER ADDRESS
0069 0036 B78C                  LDR     A15,A3                  PARAMETER TO IPL
0070 0038 570C                  RF      EXIT
0071                            EJECT
0072 003A D9C9                  DATA    /D9C9                   SOP SWITCH 8,7
0073 003C F7D7                  DATA    /F7D7                   SOP SWITCH 6,5
0074 003E EBCB                  DATA    /EBCB                   SOP SWITCH 4,3
0075      0040          DEVADR  EQU     *
0076                            EJECT
0077                    *
0078                    *       1 MEGABYTE FLOPPY
0079                    *
0080      0040          FD1M    EQU     *
0081 0040 0410                  LDK     A4,/10                  FIRST SECTOR TO READ=2
0082      0042          FDWER   EQU     *
0083 0042 7112                  WER     A1,FDIOP
0084 0044 7613                  WER     A6,FDIOP+1              BUFFER ADDRESS
```

```
          DATE  82-03-30          IDENT    BOOT6A    81-08-07  PDHD


0085                              EJECT
0086                    *
0087                    *         EXIT
0088                    *
0089          0046      EXIT      EQU      *
0090 0046 F109                    CFR      A1,A2                  READ
0091 0048 0F84                    AB       IPLSTA                 GO TO IPL
0092                    *
0093                    *         EXIT TO IPLSTA
0094                    *
0095                    *         TAPE CASSETTE                  A4=/000A
0096                    *         BRANCH TO ADDRESS /42 IN BOOTSTARP FROM CASSETTE IPL,A4 UNCHANGED
0097                    *
0098                    *         PTS 6875 FIXED DISC            A15=/63EB
0099                    *         PTS 6875 CARTRIDGE DISC        A15=/63C8
0100                    *
0101                    *         FLOPPY DISC 1 P C              A3=/0009
0102                    *         FLOPPY DISC 2 P C              A3=/0019
0103                    *         1 MEGABYTE FLOPPY DISC 1       A3=/XXC9
0104                    *         1 MEGABYTE FLOPPY DISC 2       A3=/XXD9
0105                              EJECT
0106                    *
0107                    *         CASSETTE
0108                    *
0109          004A      CASS      EQU      *
0110 004A AB41 0068               DRS      A3,SCRI-BOOT           STR CHANGED TO SCR IN READ ROUTINE
0111 004E 3401                    XRK      A4,1                   SELECT CASSETTE
0112 0050 F109                    CFR      A1,A2
0113 0052 0402                    LDK      A4,2                   LOAD
0114 0054 F109                    CFR      A1,A2
0115 0056 0408                    LDK      A4,8                   SEARCH BOT
0116 0058 F109                    CFR      A1,A2
0117 005A 040C                    LDK      A4,/C                  SEARCH TAPE MARK
0118 005C F109                    CFR      A1,A2
0119 005E 040A                    LDK      A4,/A                  READ ONE BLOCK
0120 0060 5F1C                    RB       EXIT
0121                              EJECT
0122                    *
0123                    *         SUBROUTINE TO READ
0124                    *
0125          0062      SIOI      EQU      *
0126 0062 44CE                    CIO      A4,1,CHCR
0127          0064      INRI      EQU      *
0128 0064 4F0E                    INR      A7,D,CHCR
0129 0066 5404                    RB(NA)   SSTI
0130          0068      SCRI      EQU      *
0131 0068 B739                    STR      A7,A6
0132          006A      ADKI      EQU      *
0133 006A 1601                    ADK      A6,1
0134          006C      SSTI      EQU      *
0135 006C 4F0E                    SST      A7,CHCR
0136 006E 5C0C                    RB(NA)   INRI
0137 0070 F024                    RTN      A1
0138                              EJECT
0139                    *
0140                    *         FLOPPY DISC
0141                    *
0142          0072      FDPC      EQU      *
0143 0072 23F                     ANK      A3,/3F
0144 0074 E335                    SCR      A3,A5                  UPDATE ADDRESS IN INR INSTRUCTION
0145 0076 046A                    LDK      A4,ADKI-BOOT
0146 0078 9031                    IMR      A4                     CHANGE TO ADK A6,2
0147 007A B420 C020               LDKL     A4,/C020               4 PHYS. SECTORS A 128 BYTES,START IN SEC
0148 007E 5F3E                    RB       FDWER
0149
0150
0151          0080      BOOTEND   EQU      *
0152                              END      BOOT

          SYMBOL TABLE

   ADKI    006A  R    BOOT    0000  R    BOOTEN  0080  R    CASS    004A  R
   CHCR    000E  A    DEVADR  0040  R    DISC    0024  R    DKIOP   0010  A
   EXIT    0046  R    FD1M    0040  R    FDDA    0009  A    FD1DP   0012  A
   FDPC    0072  R    FDWER   0042  R    INRI    0064  R    IPLSTA  0084  A
   SCRI    0068  R    SIOI    0062  R    SOP     002E  A    SSTI    006C  R


          ASS ERR     0000
 EOF
PROG ELAPSED TIME   00H-00M-22S-640MS-
```

1.1.16 CONTENTS IPL ROM BOOT 6C (5131 194 41700)

```
          DATE  82-03-30          IDENT    BOOT6C    81-10-07  POHO

0000                              IDENT    BOOT6C                 81-10-07  POHO
0001
0002
0003                      *       THIS BOOTSTRAP IS RELATED TO
0004                      *       TSB 506/80 - BOOTSTRAP 65
0005
0006
0007                      *
0008                      *       B O O T S T R A P   6 0 0 0
0009                      *
0010
0011
0012
0013
0014
0015                      *       SDP SWITCH 1    CARTRIDGE 16MB OR 80MB UNIT 1
0016                      *                  2    FIXED 16MB DISC        UNIT 1
0017
0018                      *       SDP SWITCH 3 :  CARTRIDGE DISC 6875.6876
0019                      *                  4 :  FIXED     DISC 6875.6876
0020
0021                      *       SDP SWITCH 5 :  CARTRIDGE DISC 6875.6876 UNIT 2
0022                      *                  6 :  FIXED     DISC 6875.6876 UNIT 2
0023
0024                      *       SDP SWITCH 7    FLOPPY DISC UNIT 1 (ALL TYPES)
0025                      *                  8                UNIT 2 (ALL TYPES)
0026
0027                      *       SDP SWITCH 9 :  NOT USED
0028                      *                 10 :  NOT USED
0029                              EJECT
0030      000E            CHCR    EQU      /0E
0031      002E            SDP     EQU      /2E
0032      0009            FDDA    EQU      9
0033      0012            FDIOP   EQU      /12
0034      0010            DKIOP   EQU      /10
0035      0084            IPLSTA  EQU      /84
0036                      *
0037                      *       READ SDP
0038                      *
0039      0000            BOOT    EQU      *
0040 0000 0680                    LDK      A6,/80                 START ADDRESS OF IPL
0041 0002 0263                    LDK      A2,SIOI+1-BOOT         SUBROUTINE ADDRESS
0042 0004 8120 8100               LDKL     A1,/8100               WER REGISTER AND STACK ADDRESS
0043 0008 E308                    ECR      A3,A2                  A3 =/6300
0044 000A 44EE                    CIO      A4,1,SDP
0045 000C 4D2E                    INR      A5,0,SDP
0046 000E 5C04                    RB(NA)   *-2
0047 0010 44AE                    CIO      A4,0,SDP
0048 0012 3D80                    SRN      A5,A4
0049 0014 0565                    LDK      A5,INRI+1-BOOT         ADDRESS TO INR INSTRUCTION
0050 0016 E350 0048               LC       A3,DEVADR-BOOT,A4      DEVICE ADDRESS
0051 001A E329                    SCR      A3,A2                  UPDATE ADDRESS IN CIO
0052 001C E341 006D               SC       A3,SSTI+1-BOOT         UPDATE ADDRESS IN SST
0053 0020 1C07                    SUK      A4,7
0054 0022 512E                    RF(P)    CDDISC                 16M OR 80M DISC
0055                              EJECT
0056                      *
0057                      *       DISC
0058                      *
0059      0024            DISC    EQU      *
0060 0024 0403                    LDK      A4,3
0061 0026 F109                    CFR      A1,A2                  SEEK ZERO
0062 0028 2710                    ANK      A7,/10
0063 002A 5446                    RF(NZ)   FDPC                   0.25 MEG FLOPPY DRIVE
0064 002C A311                    TM       A3,A4
0065 002E 540A                    RF(NZ)   FD1M                   1 MEG FLOPPY
0066 0030 040C                    LDK      A4,/C                  SECTOR 3
0067 0032 7110                    WER      A1,DKIOP
0068 0034 7611                    WER      A6,DKIOP+1             BUFFER ADDRESS
0069 0036 878C                    LDR      A15,A3                 PARAMETER TO IPL
0070 0038 5724                    RF       EXIT
0071                              EJECT
0072                      *
0073                      *       1 MEGABYTE FLOPPY
0074                      *
0075      003A            FD1M    EQU      *
0076 003A 0410                    LDK      A4,/10                 FIRST SECTOR TO READ=2
0077 003C 573C                    RF       FDWER
```

```
          DATE  82-03-30        IDENT    BOOT6C    81-10-07  PDHO


0078                            EJECT
0079                    *
0080                    *       READ TABLE FOR 16M AND 80M DISC
0081                    *
0082
0083      003E          SEEK    EQU      *
0084 003E E000                  DATA     /E000                 SEEK TO ZERO
0085      0040          READ12  EQU      *
0086 0040 0800                  DATA     /0800                 READ LOGICAL SECTOR 0,1 AND 2
0087 0042 0180                  DATA     /0180                 TOTAL LENGTH
0088 0044 0180                  DATA     /0180                 NO TRANSFER LOG. SEC. 0
0089 0046 0000 0000             DATA     0,0                   DUMMY ADDRESS
0090                            EJECT
0091      0048          DEVADR  EQU      *-2
0092 004A D9C9                  DATA     /D9C9                 SOP SWITCH 8,7
0093 004C FBDB                  DATA     /FBDB                 SOP SWITCH 6,5
0094 004E EBCB                  DATA     /EBCB                 SOP SWITCH 4,3
0095 0050 D7D7                  DATA     /D7D7                 SOP SWITCH 2,1
0096                            EJECT
0097                    *
0098                    *       16M OR 80M DISC
0099                    *
0100      0052          CDDISC  EQU      *
0101 0052 2401                  ANK      A4,1
0102 0054 3C44                  SLL      A4,4                  BIT IN POSITION DEVICE NUMBER
0103 0056 8510                  LDR      A5,A4                 FIX OR CARTRIDGE
0104 0058 AC41 0040             ORS      A4,READ12-BOOT        SET DEVICE NUMBER BIT
0105 005C 043E                  LDK      A4,SEEK-BOOT
0106                            EJECT
0107                    *
0108                    *       EXIT
0109                    *
0110      005E          EXIT    EQU      *
0111 005E F109                  CFR      A1,A2                 READ
0112 0060 0FB4                  AB       IPLSTA                GO TO IPL
0113                    *
0114                    *       EXIT TO IPLSTA
0115                    *
0116                    *       TAPE CASSETTE                 A4=/000A
0117                    *       BRANCH TO ADDRESS /42 IN BOOTSTARP FROM CASSETTE IPL,A4 UNCHANGED
0118                    *
0119                    *       PTS 6875 FIXED DISC           A15=/63E8
0120                    *       PTS 6875 CARTRIDGE DISC       A15=/63C8
0121                    *
0122                    *       FLOPPY DISC 1 P C             A3=/0009
0123                    *       FLOPPY DISC 2 P C             A3=/0019
0124                    *       1 MEGABYTE FLOPPY DISC 1      A3=/XXC9
0125                    *       1 MEGABYTE FLOPPY DISC 2      A3=/XXD9
0126                            EJECT
0127                    *
0128                    *       SUBROUTINE TO READ
0129                    *
0130      0062          SIOI    EQU      *
0131 0062 44CE                  CIO      A4,1,CHCR
0132      0064          INRI    EQU      *
0133 0064 4F0E                  INR      A7,0,CHCR
0134 0066 5404                  RF(NA)   SSTI
0135      0068          SCRI    EQU      *
0136 0068 8739                  STR      A7,A6
0137      006A          ADKI    EQU      *
0138 006A 1602                  ADK      A6,2
0139      006C          SSTI    EQU      *
0140 006C 4FCE                  SST      A7,CHCR
0141 006E 5C0C                  RB(NA)   INRI
0142 0070 F024                  RTN      A1
0143                            EJECT
0144                    *
0145                    *       FLOPPY DISC
0146                    *
0147      0072          FDPC    EQU      *
0148 0072 233F                  ANK      A3,/3F
0149 0074 E335                  SCR      A3,A5                 UPDATE ADDRESS IN INR INSTRUCTION
0150 0076 8420 C020             LDKL     A4,/C020              4 PHYS. SECTORS A 128 BYTES, START IN SEC
0151      007A          FDWER   EQU      *
0152 007A 7112                  WER      A1,FD1OP
0153 007C 7613                  WER      A6,FD1OP+1            BUFFER ADDRESS
0154 007E 5F22                  RB       EXIT
0155
0156
0157      0080          BOOTEND EQU      *
0158                            END      BOOT

          SYMBOL TABLE

  ADKI    006A  R   BOOT    0000  R   BOOTEN  0080  R   CDDISC  0052  R
  CHCR    000E  A   DEVADR  0048  R   DISC    0024  R   DKIOP   0010  A
  EXIT    005E  R   FD1M    003A  R   FDDA    0009  A   FDIOP   0012  A
  FDPC    0072  R   FDWER   007A  R   INRI    0064  R   IPLSTA  0084  A
  READ12  0040  R   SCRI    006B  R   SEEK    003E  R   SIOI    0062  R
  SOP     002E  A   SSTI    006C  R

          ASS.ERR.      0000
 EOF
PROG ELAPSED TIME   00H-00M-23S-820MS~
```

1.2 EXTERNAL CONNECTIONS

1.2.1 Compatibility between Computers

All interface units described in this section are hardware - compatible with all computers covered by this manual. With other words; all interface units can, from a HARDWARE point of view, be used in any of the computers 6810-6814 and 6824. Interface units that are classified as masters should, as far as possible, be located in the computer cabinet of an extended system. However, when required, it is now allowed to locate masters in extension cabinets of type 6864.

1.2.2 Star-Connected Work Stations

Definition of Star Network Figure 1.2-1

A star network is defined as an interconnecting system where a number of external points (in this case; work stations) are connected to a central junction (computer interface unit) VIA SEPARATE LINES, see Figure 1.2-1. This method of connecting work stations to computers is well-known from earlier PTS 6000 installations.

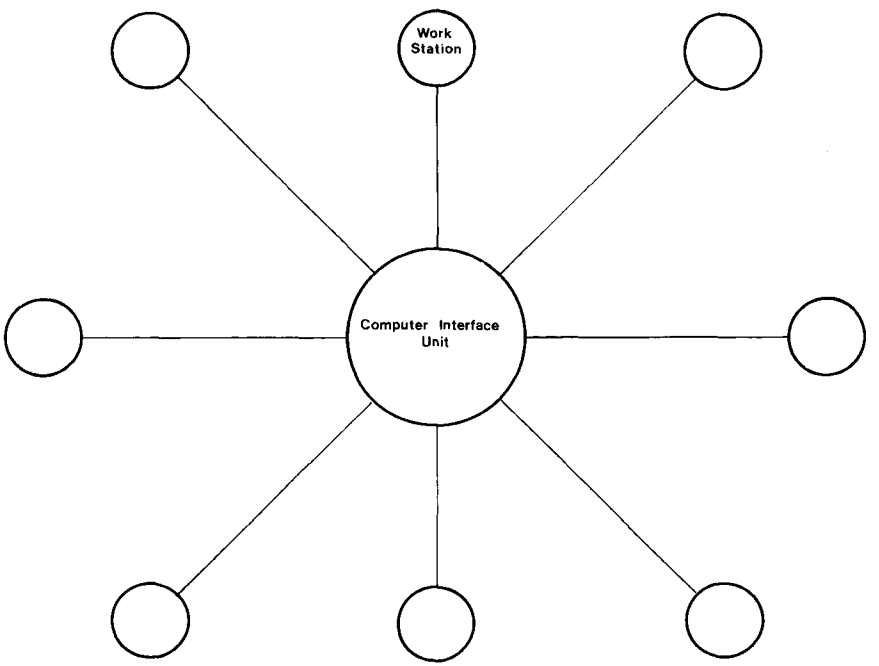


Figure 1.2-1 Definition of Star Network

Local Work Stations Figure 1.2-2

Up to eight local work stations can be connected via the computer interface unit CHLT 6831, located in a computer or an extension cabinet. The lines exit via eight plugs, vertically fitted at the front edge of the CHLT. These plugs are addressed as Terminal 0-7, from bottom to top. The system is prepared for having two CHLTs, (enabling the connection of 16 local work stations), but the number of CHLTs can be extended to four.

Figure 1.2-2 shows three different work stations connected to the CHLT. These work stations have been chosen with the purpose to indicate the development towards more and more compact work station units.

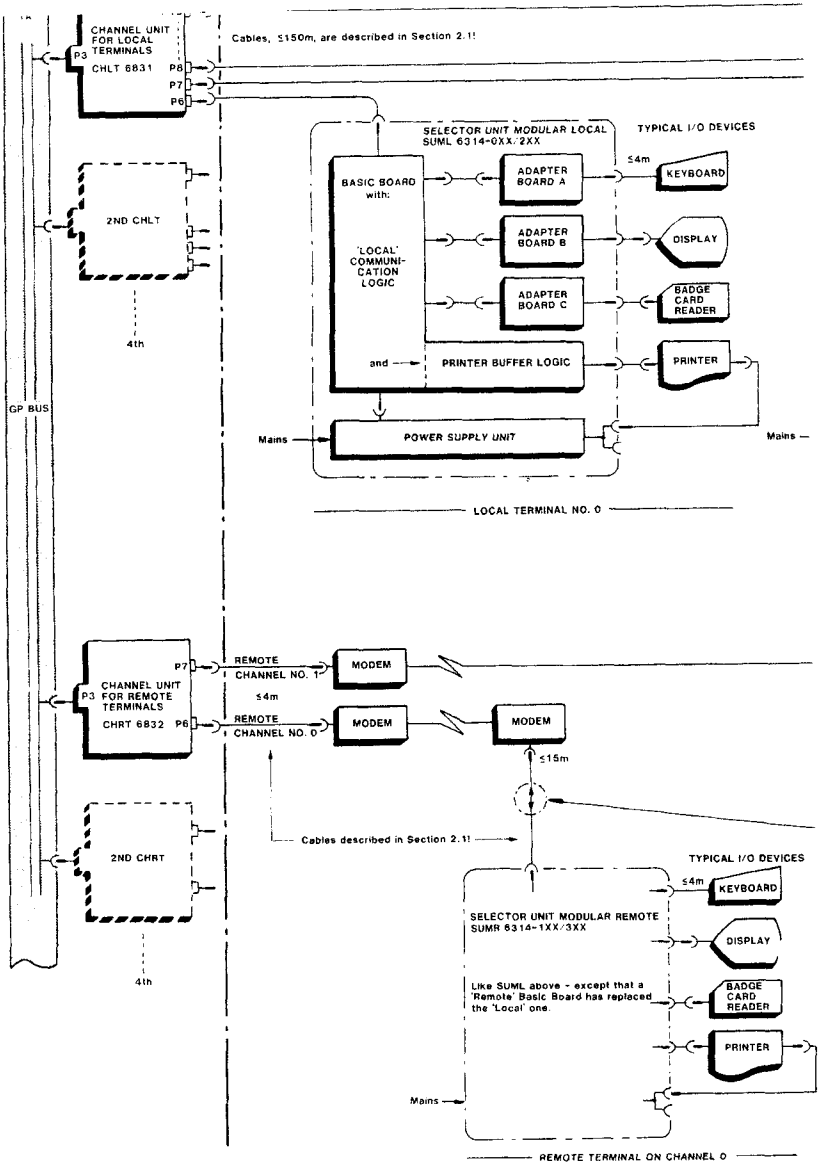
Work stations of earlier generations (terminal 0 in figure) had a separate communication unit (SUML) to which various I/O devices could be connected. In later generations of work stations (terminal 1 and 2 in figure) the communication part has been integrated in one of the I/O devices (TEP 6371/72) or together with several I/O devices in a compact desk top work station unit (CFT 6281/83).

Remote Work Stations Figure 1.2-2

One or two remote channels can be connected via the computer interface unit CHRT 6832, located in a computer or an extension cabinet. The channels exit via two plugs at the front edge of the CHRT; the bottom one being addressed as channel 0 and the top one as channel 1. The system is prepared for having two CHRTs, (enabling the connection of four remote channels), but the number of CHRTs can be extended to four.

Each channel is routed via a local modem, a telephone line and a remote modem to the remote work station. A remote work station of an earlier generation (on channel 0 in figure) is equipped with a separate communication unit (SUMR), similar to the local work station of the same generation. Remote work stations of later generations have the communication part integrated in one of the I/O devices, e.g. in a TEP 6371/72 as shown on channel 1.

The number of connectable work stations can be doubled if TFUs are used at the remote sites. Each TFU, connected after the remote modem, enables the connection of two work stations to each channel.


CHANNEL UNIT FOR LOCAL TERMINALS
P3
CHLT 6831
P8
P7
P6
Cables, ≤150m, are described in Section 2.1!
2ND CHLT
4th
GP BUS
SELECTOR UNIT MODULAR LOCAL
SUML 6314-0XX/2XX
TYPICAL I/O DEVICES
BASIC BOARD with:
'LOCAL' COMMUNI-CATION LOGIC
ADAPTER BOARD A
ADAPTER BOARD B
ADAPTER BOARD C
≤4m
KEYBOARD
DISPLAY
BADGE CARD READER
and
PRINTER BUFFER LOGIC
PRINTER
Mains
POWER SUPPLY UNIT
Mains
LOCAL TERMINAL NO. 0
CHANNEL UNIT FOR REMOTE TERMINALS
P3
CHRT 6832
P7
P6
REMOTE CHANNEL NO. 1
REMOTE CHANNEL NO. 0
MODEM
MODEM
MODEM
≤4m
≤15m
Cables described in Section 2.1!
2ND CHRT
4th
TYPICAL I/O DEVICES
≤4m
KEYBOARD
SELECTOR UNIT MODULAR REMOTE
SUMR 6314-1XX/3XX
DISPLAY
Like SUML above - except that a 'Remote' Basic Board has replaced the 'Local' one.
BADGE CARD READER
PRINTER
Mains
REMOTE TERMINAL ON CHANNEL 0

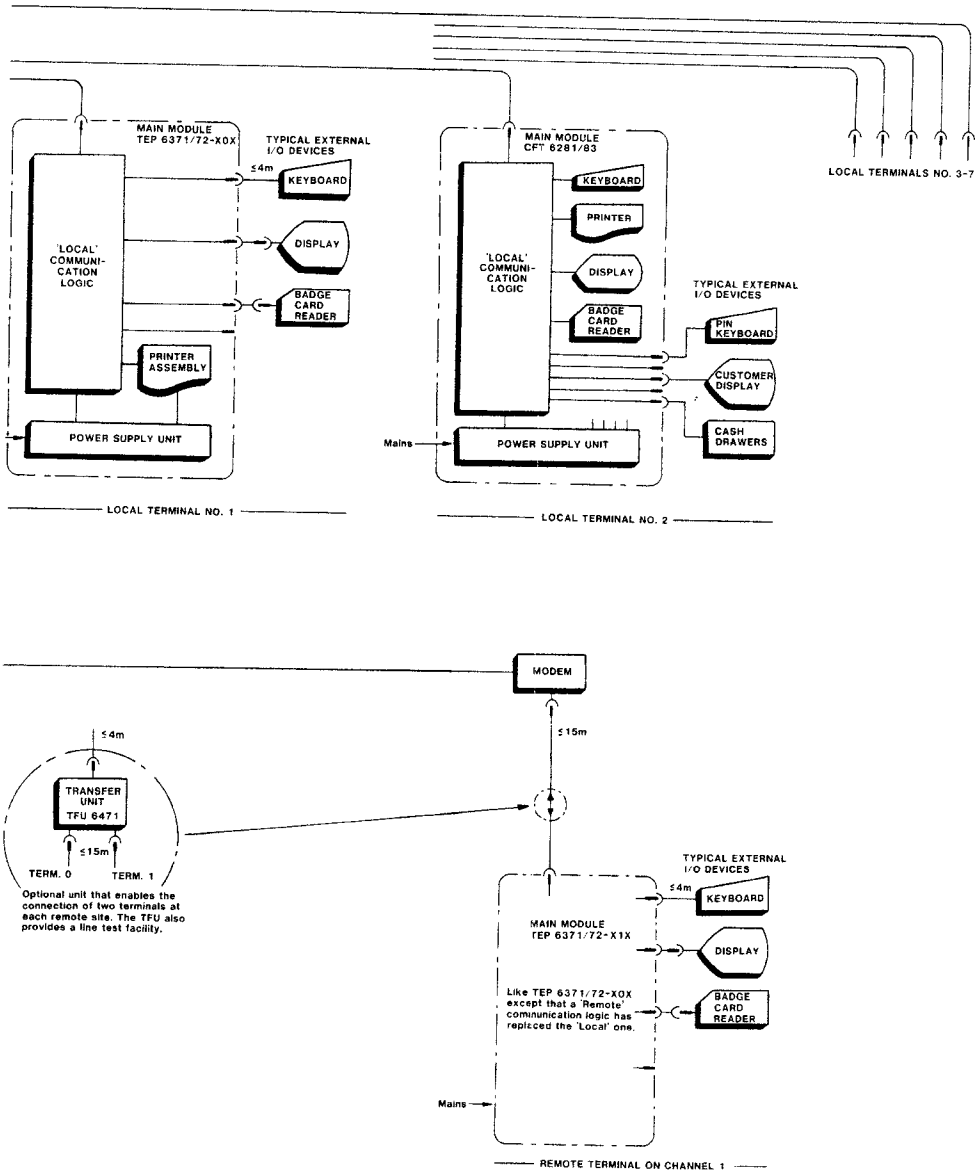


Figure 1.2-2 Star-Connected Work Stations

1.2.3 Multidrop-Connected Work Stations

Definition of Multidrop Network Figure 1.2-3

A multidrop network is defined as an interconnecting system where a number of external points (in this case; work stations) are connected to a central junction (computer interface unit) VIA A SINGLE LINE, see Figure 1.2-3. This method of connecting work stations, that will replace the former star method, has been introduced to increase the capacity and the reliability of the data transfers.

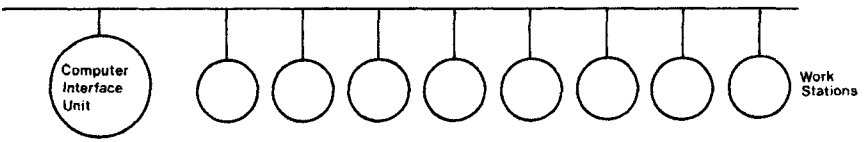


Figure 1.2-3 Definition of Multidrop Network

Local Work Stations Figure 1.2-4

Up to 32 work stations can be connected to the single multidrop line that is controlled by the computer interface unit CHLW 6895. However, in typical applications the number of work stations is limited to 6-8, due to performance reasons. The CHLW is classified as a master and should, if possible, be located in the computer cabinet (in TC 6810/11 systems it is absolutely necessary). The line exits via a plug at the front edge of the CHLW and can have a maximum length of 750 m. When being necessary the system can be equipped with more than one CHLW, up to a maximum of four.

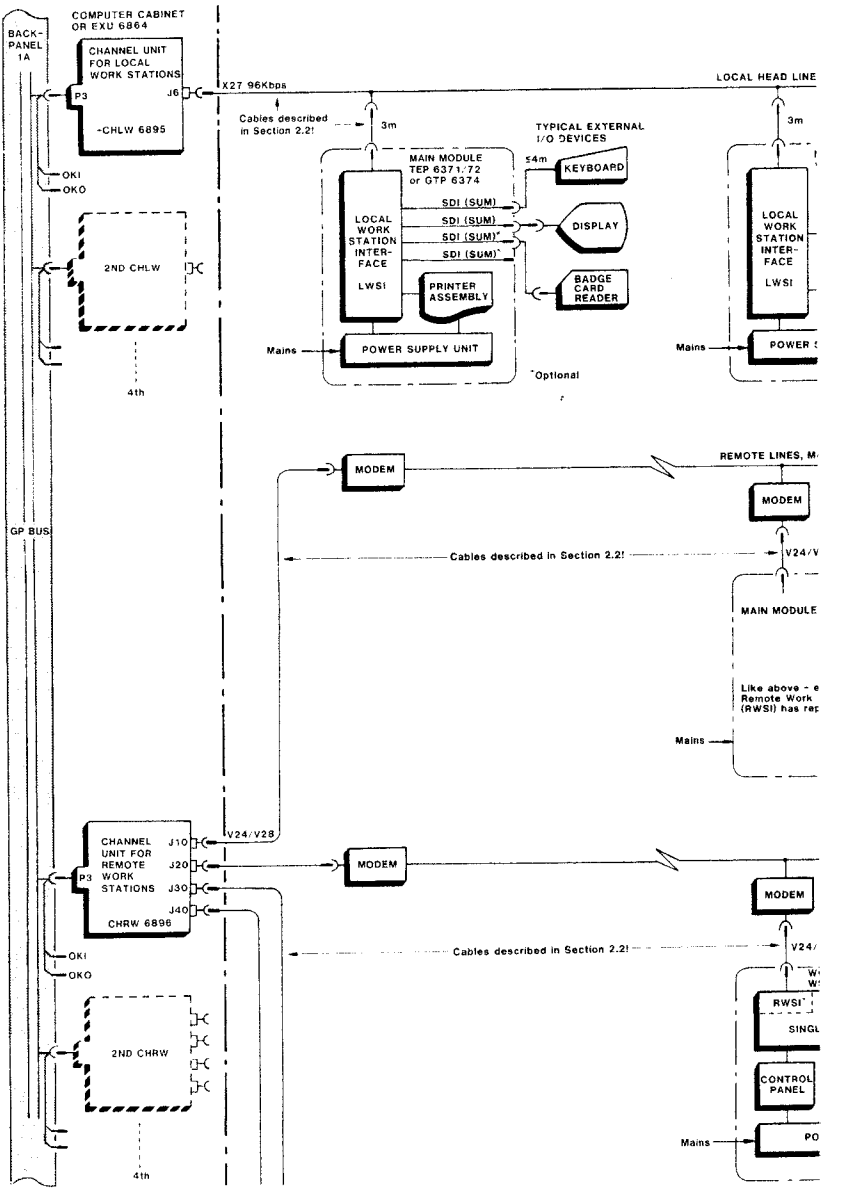
A work station connected to the multidrop line has usually an I/O device that includes the necessary communication interface, a Local Work Station Interface (LWSI). Such a device is known as the main module of the work station, and interconnects itself and other I/O devices with the multidrop line. Figure 1.2-4 shows the most common main modules.

A work station without any I/O main module is connected via a separate main module, a Modular Device Adapter - MDA 6411. The system function of this main module is similar to the former SUMLs; a communication interface interconnects line and I/O devices via adapter boards, and a power supply unit provides the necessary D.C. supply.

Remote Work Stations Figure 1.2-4

Up to four remote multidrop lines can be controlled by the computer interface unit CHRW 6896. This unit is classified as a master and should, if possible, be located in the computer cabinet (in TC 6810/11 systems it is absolutely necessary). The lines exit via four plugs at the front edge of the CHRW, the top one being addressed as line 0 and the bottom one as line 3. Line 0 can also be used for computer-to-computer communications. When being necessary the system can be equipped with more than one CHRW, up to a maximum of four.

Each line enters the PTT domain via a local modem that leads to a leased line. Up to eight drops are allowed on each line, either to single work stations or to work station controllers. However, in typical applications the number of drops is limited to 2-3, due to performance reasons.


COMPUTER CABINET OR EXU 6864
BACK-PANEL 1A
CHANNEL UNIT FOR LOCAL WORK STATIONS
P3
J6
-CHLW 6895
X27 96Kbps
LOCAL HEAD LINE
Cables described in Section 2.2!
3m
TYPICAL EXTERNAL I/O DEVICES
MAIN MODULE TEP 6371/72 or GTP 6374
≤4m
KEYBOARD
SDI (SUM)
SDI (SUM)
SDI (SUM)*
SDI (SUM)*
DISPLAY
BADGE CARD READER
LOCAL WORK STATION INTER-FACE
LWSI
PRINTER ASSEMBLY
Mains
POWER SUPPLY UNIT
*Optional
OKI
OKO
2ND CHLW
4th
GP BUS
MODEM
REMOTE LINES, M
MODEM
Cables described in Section 2.2!
V24/V
MAIN MODULE
Like above - e
Remote Work
(RWSI) has rep
Mains
CHANNEL UNIT FOR REMOTE WORK STATIONS
P3
J10
J20
J30
J40
CHRW 6896
V24/V28
MODEM
MODEM
Cables described in Section 2.2!
V24/
RWSI*
SINGL
CONTROL PANEL
Mains
OKI
OKO
2ND CHRW
4th

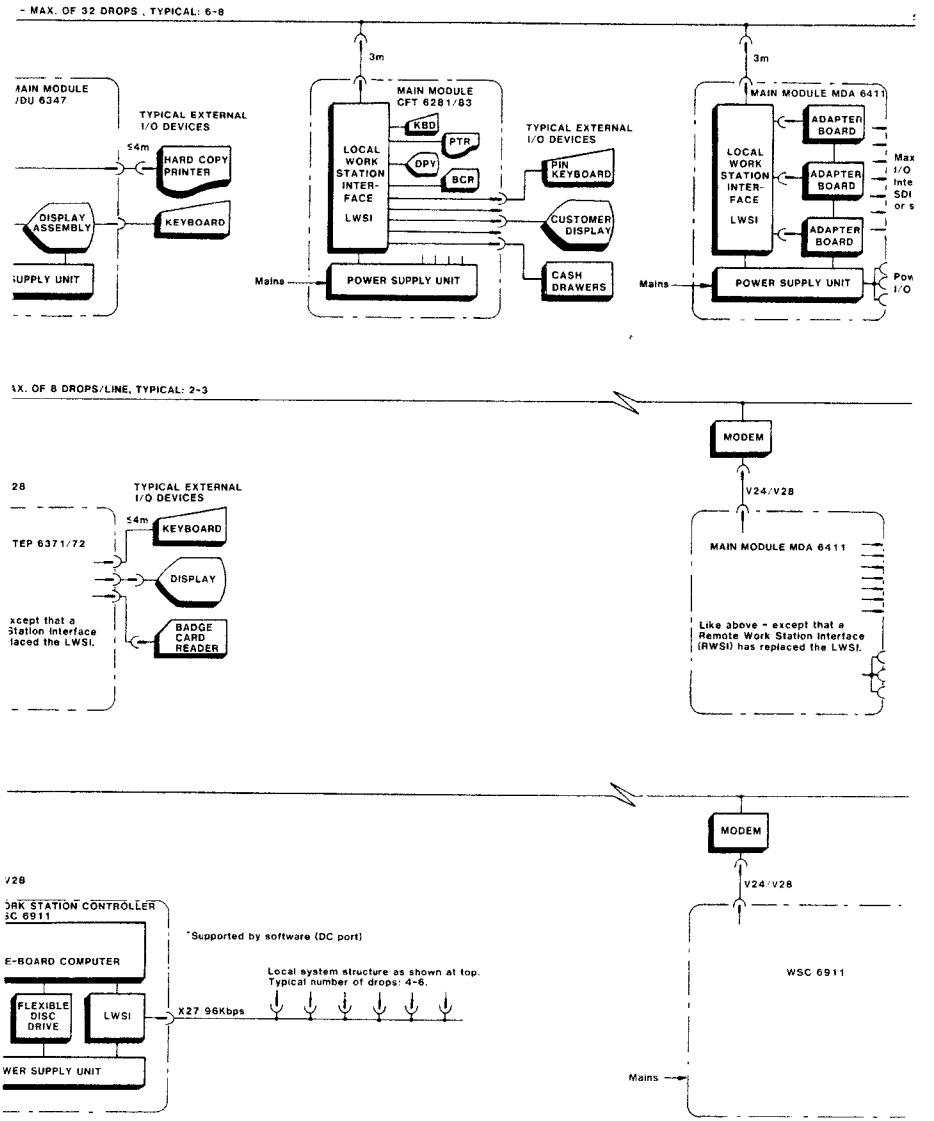


Figure 1.2-4 Multidrop-Connected Work Sta

A single work station has usually an I/O device that is classified as a main module, i.e. it includes the necessary communication interface; in this case a Remote Work Station Interface (RWSI). This interface connects the 'own' and other I/O devices to the line via a remote modem. A single work station without any I/O main module is connected via a separate main module, an MDA 6411 that is now equipped with an RWSI (compare with local work stations).

A work station controller is a small computer that can be used for converting a remote drop (via RWSI) into a local structure that is controlled via LWSI. This local structure is (except for performance) equivalent to the one controlled by CHLW at the site of the terminal computer.

1.2.4 Connection of Peripherals

Console Typewriter CTW 6862 Figure 1.2-5

A console typewriter of type 6862 can be connected to an interface circuit that is contained on the computers' CPU board. In the computers 6810-6812 (CPU P852) this interface operates according to the Current Loop method. The CTW must then be equipped with the same type of interface and is connected via a 2-wire cable (signal and ground) to fast-on pins on backpanel 1B.

An upgraded 6810/11 or computers of type 6813, 6814 or 6824 (CPU P857, P857R, P857RA) have instead a V24 interface. A CTW equipped with the same type of interface can then be connected via P7 on backpanel 1B.

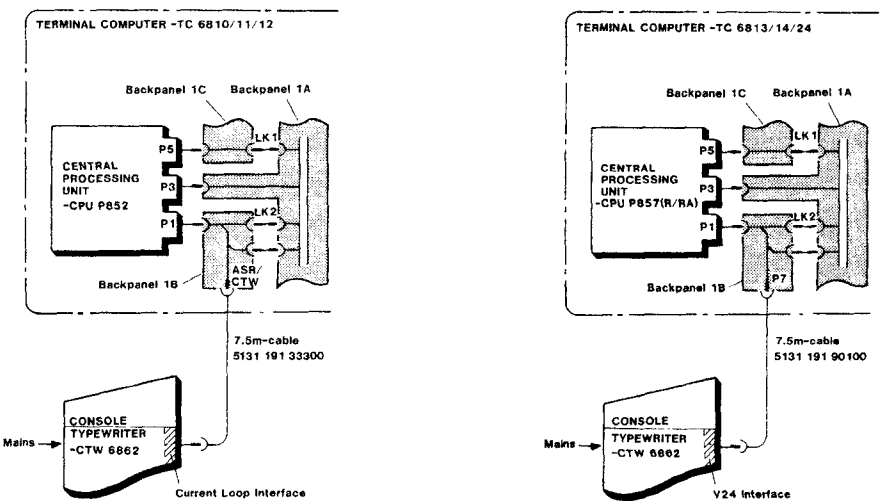


Figure 1.2-5 Connection of Console Typewriter

Flexible Disc Unit FDU 6879

Figure 1.2-6

An external flexible disc unit of type 6879 (primarily intended for TC 6810/11) can be controlled via the computer interface unit CHFD 6848. The FDU can be equipped with one or two flexible disc drives of type 6867 (each of 250 Kbytes) and is connected via two cables to front edge connectors on the CHFD.

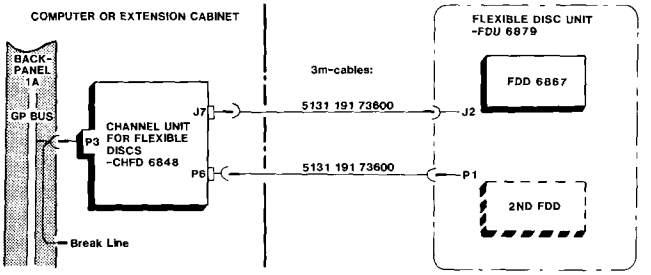


Figure 1.2-6 Connection of Flexible Disc Unit

Cartridge Disc Unit CDU 6875/76

Figure 1.2-7

Up to two cartridge disc units of type 6875/76 (2x3.1 Mbytes/2x6.25 Mbytes) can be controlled via the computer interface unit CHDU 6844. The CDUs are connected to the CHDU via two separate cables, terminated with sockets that are fixed to the rack for accepting the edge plugs P1 and P5 of the CHDU.

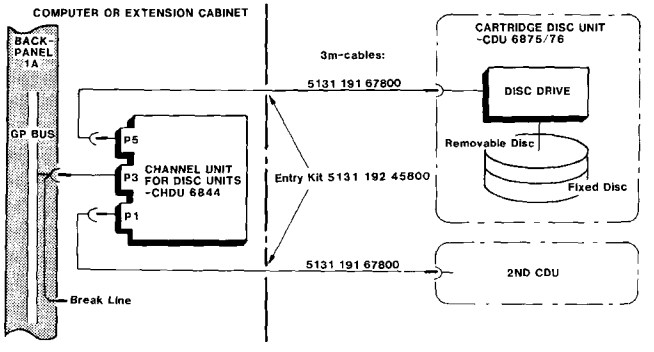
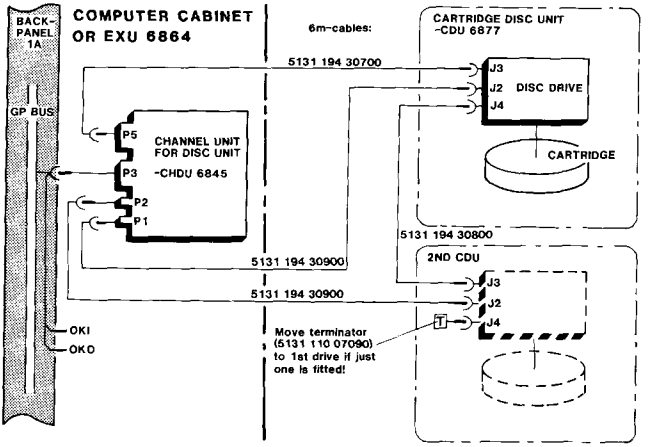


Figure 1.2-7 Connection of Cartridge Disc Unit(s), type 6875/76

Cartridge Disc Unit CDU 6877 Figure 1.2-8

One or two cartridge disc units of type 6877 (80 Mbytes) can be controlled via the computer interface unit CHDU 6845. This unit is classified as a master and should, if possible, be located in the computer cabinet (in TC 6810/11 systems it is absolutely necessary). The CDUs are connected via cables that are terminated with sockets, fixed to the rack for accepting the edge plugs P1, P2 and P5 of the CHDU.

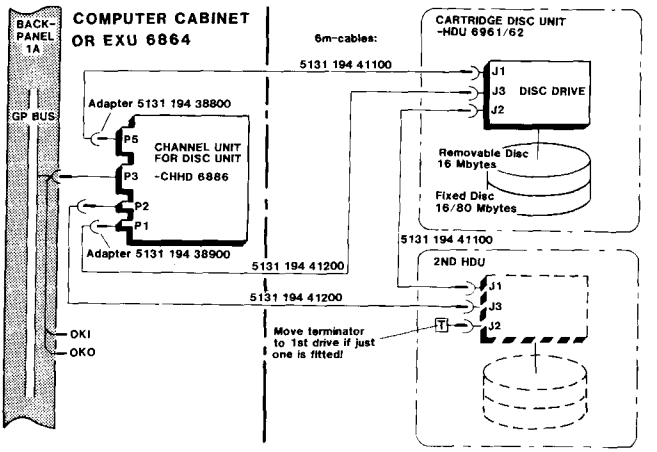
Figure 1.2-8 Connection of Cartridge Disc Unit(s), type 6877



Cartridge Disc Unit HDU 6961/62 Figure 1.2-9

Up to two cartridge disc units of type 6961/62 (16+16 Mbytes/16+80 Mbytes) can be controlled via the computer interface unit CHHD 6886. This unit is classified as a master and should, if possible, be located in the computer cabinet (in TC 6810/11 systems it is absolutely necessary). The HDUs are connected via cables that are terminated with sockets, fixed to the rack for accepting the edge plugs P1, P2 and P5 of the CHHD.

Figure 1.2-9 Connection of Cartridge Disc Unit(s), type 6961/6962



Matrix Line Printer MLP 6881/82
Card Reader CRD 6885 Figure 1.2-10

A matrix line printer of type 6881/82 (200/400 lpm) and a card reader of type 6885 can both be controlled via the computer interface unit CHCD 6847. Both units are connected via cables that are terminated with sockets, fixed to the rack for accepting the CHCD's edge plugs P1, P2 (CRD cable) and P4, P5 (MLP cable).

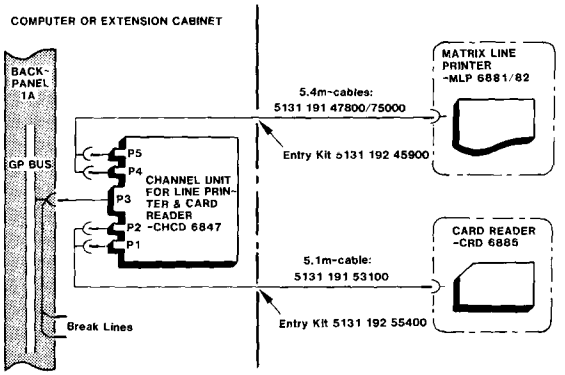


Figure 1.2-10 Connection of Matrix Line Printer and Card Reader

Magnetic Tape Unit MTU 6872 Figure 1.2-11

A magnetic tape unit of type 6872 can be controlled via the computer interface unit CHMT 6842. The tape unit is connected via four cables to front edge plugs on the CHMT. When required it is possible to connect a second MTU-cabinet with another tape transport.

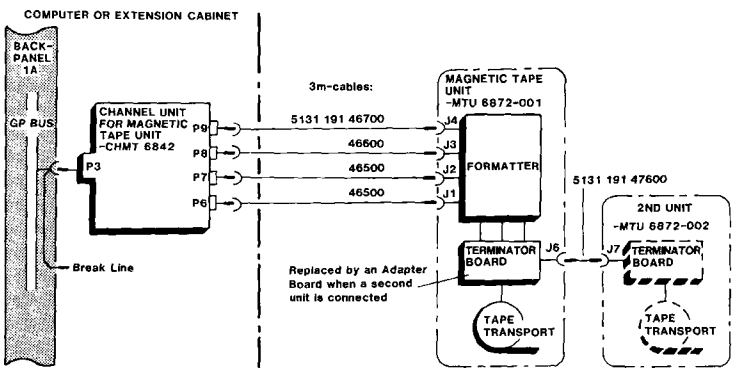


Figure 1.2-11 Connection of Magnetic Tape Unit(s)

1.2.5 On-Line Connections

General

There are several computer interface units available for communications with a remote data centre, each unit being designed for a specific line configuration and a certain communication procedure. The interface units can be separated in two categories; single-line controllers and multiple-line controllers.

Single-Line Controllers Figure 1.2-12

Four single-line controllers (CHLC 6834-6837) are available as single-board units, connecting to a local modem via a front edge plug. A fifth single-line controller (CHLC 6891) is composed of two parts:

- A line control unit designed in double Eurocard format
- A rack adapter board that enables the line control unit to be plugged into the computers 6810-6814 and 6824.

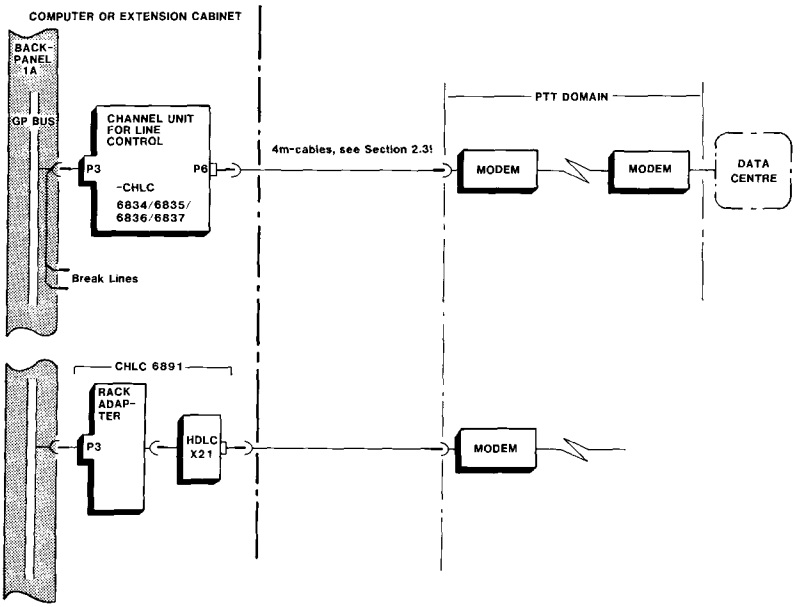


Figure 1.2-12 On-Line Connection via Single-Line Controllers

The main characteristics of the single-line controllers are:

- CHLC 6834, a synchronously operating unit for point to point or multidrop configurations. Line interface: V24/V28. Transfer rate: up to 4.800 bps. Possible procedures: Uniscope 100, BSC, ECMA 16 and others.

- CHLC 6835, a synchronously operating unit for loop configurations. Line interface: V24/V28. Transfer rate: up to 2.400 bps.

- CHLC 6836, a synchronously operating unit for point to point or multidrop configurations. Line interface: V24/V28. Transfer rate: up to 80.000 bps. Possible procedures: HDLC and SDLC.

- CHLC 6837, a synchronously operating unit for loop configurations. Line interface: V24/V28. Transfer rate: up to 4.800 bps. This unit is designed for a specific procedure known as the 'SHB Loop'.

- CHLC 6891, a synchronously operating unit for point to point or multidrop configurations. Line interface: X21/X24/X27. Transfer rate: up to 9.600 bps. Procedure: HDLC.

Multiple-Line Controllers Figure 1.2-13

There are two multiple-line controllers available (CHLC 6838/39), both being able to control two lines. However, in ordinary terminal computer applications there is usually just one line used.

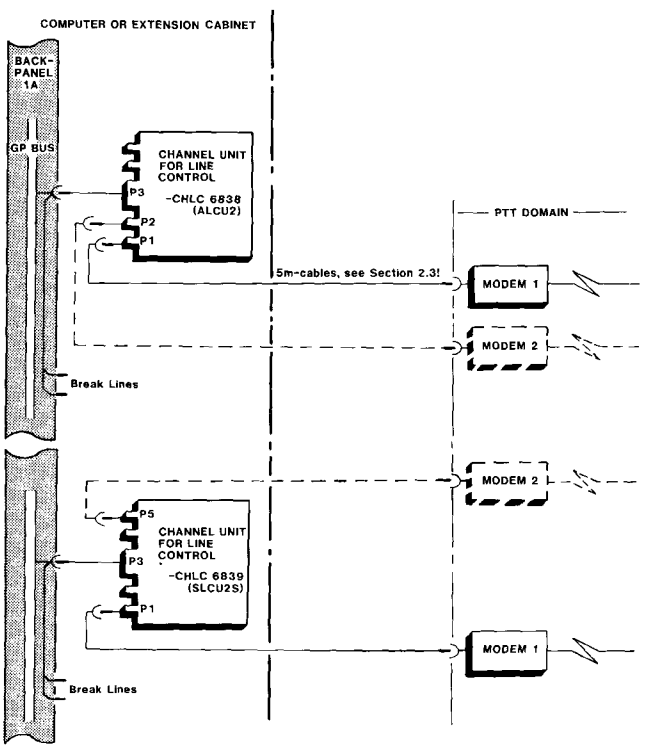
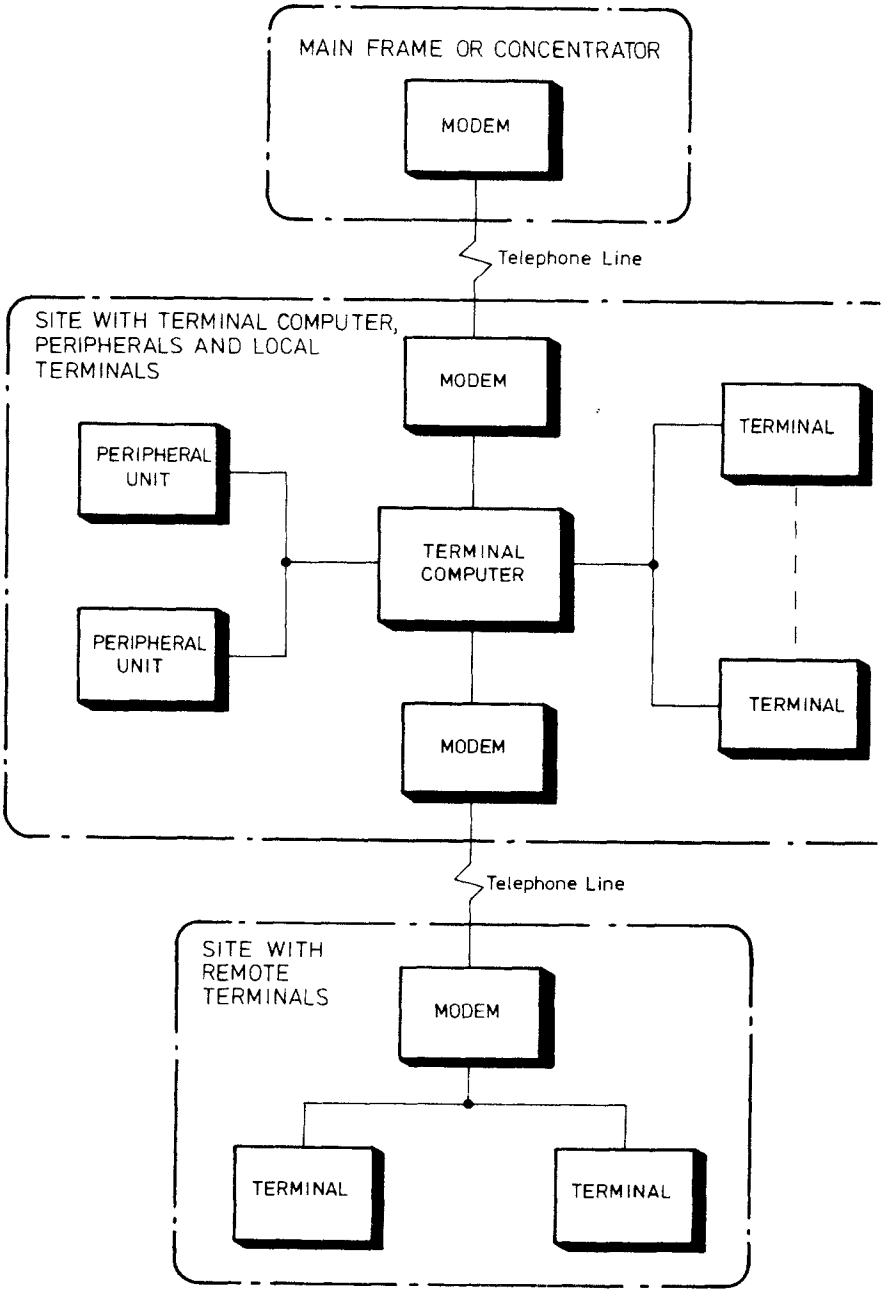


Figure 1.2-13 On-Line Connection via Multiple-Line Controllers

The local modems are connected via cables that are fitted with sockets, fixed to the rack for accepting the rear edge connectors of the controllers.

The main characteristics of the multiple-line controllers are:

- CHLC 6838, Asynchronous Medium Speed Line Control Unit (ALCU2). Line interface: V24. Transfer rate: up to 9.600 bps.
- CHLC 6839, Synchronous Line Control Unit (SLCU2S). Line interface: V24. Transfer rate: up to 9.600 bps.


MAIN FRAME OR CONCENTRATOR
MODEM
Telephone Line
SITE WITH TERMINAL COMPUTER, PERIPHERALS AND LOCAL TERMINALS
MODEM
PERIPHERAL UNIT
PERIPHERAL UNIT
TERMINAL COMPUTER
TERMINAL
TERMINAL
MODEM
Telephone Line
SITE WITH REMOTE TERMINALS
MODEM
TERMINAL
TERMINAL

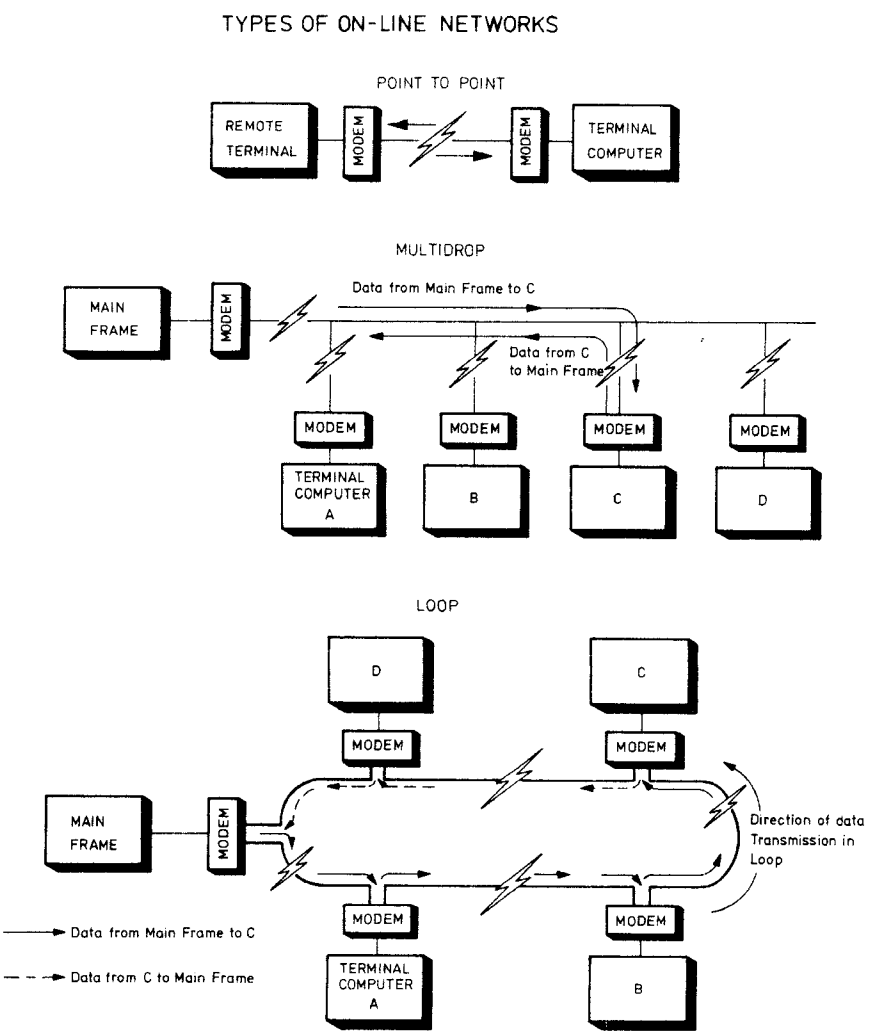


Figure 1.2-14 Basic Configuration and On-Line Networks

1.3 BASIC DATA TRANSMISSION TECHNOLOGY

1.3.1 Networks

Introduction

Modern data processing technics allow more data to be processed nowadays than was previously possible. To meet the requirement of transferring larger quantities of data faster the Public Data Network is added to the Public Telephone Network which is usually used for data transmission.

Public Telephone Network

Data transmitted over the Public Telephone Network is converted into analogue signals by means of modem and in the receiving end converted back to digital signals by another modem.

The maximum permissable transfer rate at present is 2400 bps using the 'switched' Public Telephone Network.

Using 'leased' telephone circuits it may be possible to attain rates upto 9600 bps and may be increased further on leased wideband circuits.

Public Data Network

The Public Data Network is designed for data transmission only. The network is a digital network providing synchronous data transmission, but it is possible to connect asynchronous data terminal equipment for lower transmission rate; 600 - 19.200 bps.

Data terminal equipment with CCITT X21 (X21 bis/X20 bis) interface may be connected to the network.

1.3.2 Transfer Techniques

HDLC Procedure (Protocol)

HDLC (High-level Data Link Control) is the procedure used in data communication

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Data terminal equipment with CCITT X21 (X21 bis/X20 bis) interface may be connected to the network.

1.3.2 Transfer Techniques

HDLC Procedure (Protocol)

HDLC (High-level Data Link Control) is the procedure used in data communication systems where a very reliable and high-volume transfer is required. (High-level means here that the procedure is intelligent).

The HDLC procedure synchronises the link and is capable of detecting errors in any kind of sequence and the only way to achieve this is to transmit data in blocks with a Cyclic Redundancy Check (CRC).

Therefore, in HDLC all transmissions are in form of frames as shown in X25 and the **information** can be in any form, length and code. To distinguish between flags and information the transmitter equipment inserts a "0" bit after all sequences of 5 consecutive "1" bits in all the information between the flags. These extra "0" bits are in the receiver removed so as the information is **transparently** (without any changes) transferred from one end to the other.

SDLC Procedure (Protocol)

While HDLC is the ISO's synchronous protocol the SDLC is IBM's bit-oriented synchronous protocol. They are basically the same except when it comes to extending address field or control field and aborting characters.

The SDLC uses address-bytes and max 256 bits while HDLC lets you extend its address and control fields unlimited.

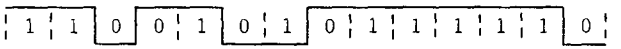
NRZI (Nonreturn-to-Zero Inverted)

The NRZI encoding and decoding lets the SDLC protocol to be used over links that are basically asynchronous.

Under NRZI coding the signals remain steady for transmitting a ONE and change for transmitting a ZERO.

Because of the "0"-bit insertion requirement strings longer than five "1"-bits are broken up. This means that the NRZI coding assures that, when active, the line will have at least one transition every five bit times. So strings of ZEROes are translated into transitions each bit time.

Asynchronous receivers, using either digital or analogue phase-locked loops, can usually extract the "bit-detection clock" from such data streams of NRZI.



NRZI coding, changing on ZEROes

Balanced and Unbalanced Lines

Balanced and unbalanced mean different things to hardware and software:

- Hardware — unbalanced circuits - are shown in V10 (X26)
  balanced circuits - can be seen in V11 (X27)
- Software — unbalanced mode - means that one master station communnicates with on or more slaves, as in PTS Interncom.
  balanced mode - means that any station connected to the line is able to communicate with any other station on the same line

1.3.3 International Standards

General

V and X series standards are recommendations of the CCITT (Consultative Committee for International Telephone and Telegraph) which is located in Switzerland and includes all countries in the world. This committee tries to adapt the V recommendations to other organizations´ standards, i.e. EIA (The Electronic Industries Association) which is the USA´s trade association of electronic

equipment manufacturers and IEEE (The Institute of Electrical and Electronic Engineers' Computer Society) concerned with computer and communication standards.

Another well known standard is the one from ISO (The International Organization for Standardization) where the membership is limited to 62 full members and 19 correspondent members. The job of ISO includes standards for communication through all types of telecommunication media.

There are 36 of these V series Recommendations which relate to the transmission of data over the **Public Telephone Network.**

The best known is V24 which specifies the use of interchange circuits at the interface between customer and administration equipment for transporting data in the "analogue" telephone network. Notice, however, that V24 is only a list of signals and the operation conditions of them. All are not used simultaneously by an equipment.

Notice also that V24 is not used by its own but combined with several of the other V recommendations; e.g. V27 telling the transfer baud rate and V28 telling the electrical characteristics for the interface circuits.

The X series Recommendation is applicable for data transmission over the **Public Data Network** which is a "digital" system with superior error performance and fast switching better suited to data transmissions.

Besides the use of different types of transmission networks the transfer procedure differs too, as the terminal equipment provided with a V24 interface uses about 10 separate lines but only 2 balanced lines (with a common return) are used when the equipment is provided with e.g. an X27 interface .

CCITT V Series Recommendations

V1 Equivalence between binary notation symbols and the significant conditions of a two-condition code

Digit "0" = Start / Space / Condition A
Digit "1" = Stop / Mark / Condition 2

V2 Power levels for data transmission over telephone lines. Measured in dB.

V3 International Alphabet No.5 (CCITT-5), see Table 1.3-1.

V4 General structure of signals of International Alphabet No. 5 code for data transmission over the public network order of the bit binary numbering. The low order bit should be transmitted first in serial transfer.

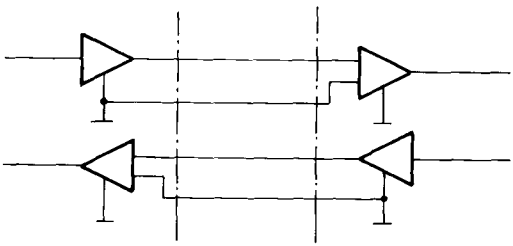
V5 Standardization of data-signalling rates for synchronous data transmission in the general switched telephone network.

V6 Standardization of data-signalling rates for synchronous data transmission of leased telephone-type circuits.

Table 1.3-1 International Alphabet No. 5 (V3)

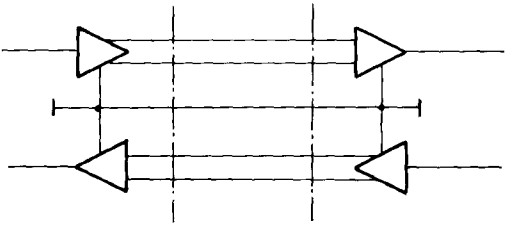
b_7	0	0	0	0	1	1	1	1
b_6	0	0	1	1	0	0	1	1
b_5	0	1	0	1	0	1	0	1
b_4 b_3 b_2 b_1	0	1	2	3	4	5	6	7
0 0 0 0	0	NUL	TC$_1$ (DLE)	SP	0	@	P	`	p
0 0 0 1	1	TC$_1$ (SOH)	DC$_1$	!	1	A	Q	a	q
0 0 1 0	2	TC$_2$ (STX)	DC$_2$	"	2	B	R	b	r
0 0 1 1	3	TC$_3$ (ETX)	DC$_3$	#	3	C	S	c	s
0 1 0 0	4	TC$_4$ (EOT)	DC$_4$	¤	4	D	T	d	t
0 1 0 1	5	TC$_5$ (ENQ)	TC$_8$ (NAK)	%	5	E	U	e	u
0 1 1 0	6	TC$_6$ (ACK)	TC$_9$ (SYN)	&	6	F	V	f	v
0 1 1 1	7	BEL	TC$_{10}$ (ETB)	'	7	G	W	g	w
1 0 0 0	8	FE$_0$ (BS)	CAN	(	8	H	X	h	x
1 0 0 1	9	FE$_1$ (HT)	EM	)	9	I	Y	i	y
1 0 1 0	10	FE$_2$ (LF)	SUB	*	:	J	Z	j	z
1 0 1 1	11	FE$_3$ (VT)	ESC	+	;	K	[	k	{
1 1 0 0	12	FE$_4$ (FF)	IS$_4$ (FS)	,	<	L	\	l	|
1 1 0 1	13	FE$_5$ (CR)	IS$_3$ (GS)	-	=	M	]	m	}
1 1 1 0	14	SO	IS$_2$ (RS)	.	>	N	^	n	~
1 1 1 1	15	SI	IS$_1$ (US)	/	?	O	_	o	DEL

V10(X26) Electrical characteristics for **unbalanced** double-current interchange circuits for general use with integrated circuit equipment in the field of data communications (identical to X26).



Interconnection example of signal common return

V11(X27) Electrical characteristics for **balanced** double-current interchange circuits for general use with integrated circuit equipment in the field of data communications (identical to X27).



Interconnection example of balanced interchange circuits

V15 Use of acoustic coupling for data transmission.

V19 Modems for parallel data transmission using telephone signalling frequencies.

V20 Parallel data transmission modems standardized for universal use in the general switched telephone network.

V21 200-baud modem standardized for use in the general switched telephone network.

V23 600/1200 baud modem standardized for use in the general switched telephone network.

V24 List of definitions for interchange circuits between data terminal equipment and data circuit-terminating equipment, see Table 1.3-2.

V25 Automatic calling and/or answering equipment on the general switched telephone network, including disabling of echo suppressors on manually established calls.

V26 2400 bits per second modem standardized for use on four-wire leased circuits.

V26bis 2400/1200 bits per second modem standardized for use in the general switched telephone network.

V27 4800 bits per second modem standardized for use on leased circuits.

V27bis 4800 bits per second modem with **automatic equalizer** standardized for use on leased circuits.

V27ter 4800/2400 bits per second modem standardized for use in the general switched telephone network.

V28 Electrical characteristics for **unbalanced** double-current interchange circuits. Significant levels:

Signal	<-3V	>+3V
Data	1	0
Control & Timing	Off	On

connecting cable, the additional connection considerations are part of Recommendation X24.

** Continuous isochronous transmission will be provided.

*** May be provided as an optional additional facility

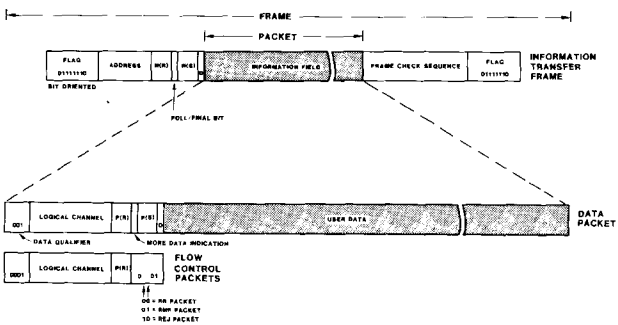
X21bis Use on public data networks of data terminal equipments which are designed for interfacing to synchronous V-series modems.

X24 List of definitions of interchange circuits between data terminal equipment and data circuit-terminating equipment on public data networks (compare V24).

Interchange circuit	Interchange circuit name	Data		Control		Timing	
		to DCE	from DCE	to DCE	from DCE	to DCE	from DCE
G	Signal ground or common return						
Ga	DTE common return			X			
Gb	DCE common return				X		
T	Transmit	X		X			
R	Receive		X		X		
C	Control			X			
I	Indication				X		
S	Signal element timing						X
B	Byte timing						X

X25 Interface between data terminal equipment and data circuit-terminating equipment for terminals operating in the packet mode on public data networks.

All transmissions are in frames conforming to one of the formats of Table 1/X25. The flag preceding the address field is defined as the opening flag.



X26 (V10) Electrical characteristics for **unbalanced** double-current interchange circuits for general use with integrated circuit equipment in the field of data communications (identical to V10).

X27 (V11) Electrical characteristics for **balanced** double-current interchange circuits for general use with integrated circuit equipment in the field of data communications (identical to V11).

X28 DTE/DCE interface for a start/stop mode data terminal equipment accessing the packet assembly/disassembly facility (PAD) on a public data network situated in the same country.

X29 Procedures for exchange of control information and user data between a packet mode DTE and a packet assembly/disassembly facility (PAD).

X92 Hypothetical reference connections for public synchronous data networks.

X95 Network parameters in public data networks.

X96 Call progress signals in public data networks.

ISO Standards for Connector Pin Assignments

This International Standard (ISO 2110-1972E) specifies the assignment of connector pin numbers at the interface between data terminal equipment (DTE) and data communication equipment (DCE) either **modems** or **automatic calling equipment** where CCITT-V24 is applicable.

In general 25 pin connectors are used and the male connector (plug) is associated with the DTE and the female connector (socket) with the DCE (modem). However, a 37 pin connector is standardized for the V24/X26 interfaces.

Pin assignment for the 25 pin connectors is given in Table 1.3-3.

The ISO standard 4903 assigns the pin number of the 15 pin connectors used at X20 and X21 interfaces, see Table 1.3-4.

Table 1.3-3 Pin assignment in 25-pin connectors

Pin number	Interchange circuit numbers and remarks											
	Voice band modems					Public data networks			Telegraph		Automatic calling	
	Asynchronous A V21	Asynchronous B V23	Synchronous C V26, V26 bis V27, V27 bis V27 ter, V29	Parallel D V19, V20 Instation	Parallel E V20 Outstation	F X20 bis	G X21 bis	H X20	I Telex	J Other	K Telephone V25	L Telex S16
1	101	101	101	101	101	101	101	101	101	101	212	212
2	103	103	103	Note	192-A	103	103	T	103	103	211	211
3	104	104	104	A1	A1	104	104	R	104	104	205	205
4	105	105	105	A2	A2	F	105	F	N	N	202	202
5	106	106	106	A3	A3	106	106	F	106	106	210	210
6	107	107	107	A4	B1	107	107	F	107	107	213	213
7	102	102	102	131	B2	102	102	G	102	102	201	201
8	109	109	109	109	B3	109	109	F	109	109	F	F
9	N	N	N	C1	C1	N	N	N	N	N	N	N
10	N	N	N	C2	C2	N	N	N	N	N	N	N
11	126	N	N	C3	C3	F	N	N	N	N	F	F
12	F	122	122	C4	192-B	F	F	N	F	F	F	F
13	F	121	121	B1	Note	F	F	N	F	F	204	204
14	F	118	118	B2	125-A	F	F	N	F	F	206	205
15	F	114	114	B3	125-B	F	114	N	F	F	207	207
16	F	119	119	B4	105-A	F	F	N	F	F	208	208
17	F	115	115	191-A	105-B	F	115	N	F	F	209	209
18	141	141	141	191-B	129-A	N	N	F	132	F	F	F
19	F	120	120	130	129-B	F	F	F	F	F	F	F
20	108/1 108/2	108/1 108/2	108/1 108/2	105	119-A	108/1 108/2	108/1 108/2	F	108/2	108/2	F	F
21	140	140	140	125	119-B	N	N	F	F	F	F	F
22	125	125	125	108/1 108/2	107-A	125	125	F	125	125	203	203
23	N	111	111	107	107-B	N	N	F	N	N	N	N
24	N	N	113	102	108-A	N	F	F	N	N	N	N
25	142	142	142	124	108-B	N	142	F	F	F	F	F
Electrical characteristics	V28	V28	V28	V28	V31	V28	V28	V28	V28	V28	V28	V28

N = Pin number permanently reserved for national use.
F = Pin number reserved for future International Standard and should not be used for national use.

The V24 signals 140, 141 and 142 are assigned to the pins 21, 18 and 25 in the columns A, B and C.

Table 1.3-4 Pin assignment in 15-pin connectors

Pin number	Interchange circuit assignment			
	X20		X21	
	X26	X27	X28	X27
1	*)	*)	*)	*)
2	T	T	T	T
3	-	-	C	C
4	R	R	R	R
5	-	-	I	I
6	-	-	S	S
7	-	-	S	S
8	G	G	G	G
9	Ga	T	Ga	T
10	-	-	Ga	C
11	Gb	R	R	R
12	-	-	I	I
13	-	-	S	S
14	-	-	B	B
15	Reserved for future use			

*) Pin 1 is assigned for connecting the shields between tandem sections of shielded interface cable. The shield may be connected either to protective ground or to signal ground at either the DTE or DCE or both in accordance with national regulations.

1.4 LWSI/RWSI COMMUNICATION METHODS

1.4.1 Introduction

HDLC Protocol

The data communication is full duplex and data is serially transferred at a speed of 96 kbit/sec. for LWSI and 600-19200 bit/sec. for RWSI.

The way of transferring data is decided by a procedure described in a protocol called HDLC (High-level Data Link Control). A Data Link is not only the hardware of the LWSI line but as well the procedure needed to establish the communication channel between a primary and a secondary unit.

Philips is not using the whole international standardized HDLC protocol but a real subset. The HDLC procedure synchronises the data link to the work stations and is capable of detecting errors in any kind of sequences.

The only way to achieve this is to transmit data in blocks, called frames, with a Cyclic Redundancy Check (CRC). The HDLC procedure provides the information block, called a data packet, with the necessary sync characters (flags) and control characters. The procedure also calculates the CRC-sum and inserts extra "zeroes" when transmitting data and removes them again in the receiving end. "Zero" insertion is done to allow data equal to flags to be sent in the data field without any effect.

The HDLC procedure permits any form of data to be transparently (without any changes) transferred from one end to the other. The frame structure is defined in the ISO 3309-1976(E) standard.

Polling

The communication between the TC and the work stations is performed by a polling procedure governed by the primary unit. This means that a work station cannot send anything until it is polled by the primary unit (TC or Work Station Controller). The poll frequency can be upto 35 Hz/WS.

1.4.2 Frames

Figure 1.4-1

Structure

The frames can be of any length upto 265 bytes. A frame begins and ends with one or more flag bytes (01111110) and contains always a workstation address byte, a control byte and two FCS bytes.

The data between the control and the FCS bytes is called a Packet consisting of a 3 byte Packet Header (device address and two more control bytes) and a variable length (max 256) of information to/from a device.

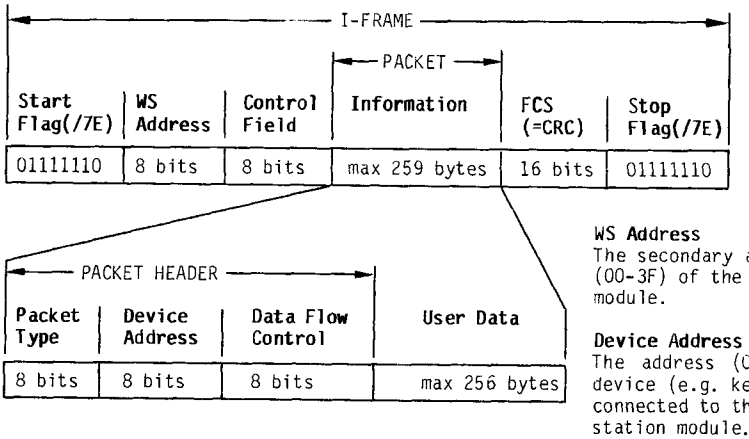


Figure 1.4-1 Frame structure

- Flag — The flag is used for frame synchronization and all stations hunt for this bit sequence. (The only byte which contains more than 5 ONEs in a sequence.)

- WS Address — identifies the work station address to/from which the frame is transferred. The address is calculated in the following way:
  2 x WS number - 1 = WS Address
  Example 1: WS number 11 has the address 2x11 - 1 = 21_{10} = 15_{16}
  Example 2: WS number 5 has the address 2x5 - 1 = 9_{10} = 09_{16}

- Control — This field contains commands/responses. The primary unit, the TC, uses this field to command the secondary unit, a work station, to perform a particular operation. The work station uses this field to respond to the TC.

- Information — This field, called packet, contains information to/from the WS. This field is in some frames not included and in others it only contains the packet header.

- FCS — means Frame Checking Sequence and is a type of CRC control to detect transmission errors.

Note: All bytes are transmitted on the line with low order bit (2^0) first. However, when looking at the data stream on the line by means of the LWSI Datascope this unit converts the bytes in the opposite order. Because of this, the bits within the bytes are in this manual presented with the least significant bit, 2^0, most to the right.

To ensure data bytes not being interpreted as flags the HDLC procedure at transmission inserts a "0" bit after all sequences of 5 continous "1" bits for all data between the flags.

At reception of a frame the HDLC procedure removes this extra "0" bits.

Types

There are three formats of frames used and they are defined by the HDLC control byte:

- I-Frames — numbered information frames, contains data to/from a device and the number of sent and received frames.

- S-Frames — numbered supervisory frames used to perform data link supervisory functions as:
  - acknowledge I-Frames (wnen it cannot be done in an I-Frame)
  - Polling
  - requesting retransmission of I-Frames
  - indicating "temporary not ready" to receive I-Frames

- U-Frames — unnumbered control frames. This format contains no sequence number of the frames. U-Frames are additional data link control functions such as:
  - open a data link by means of the SNRM* command
  - disconnect a work station
  - reject a frame
  - unnumbered acknowledge is the response to one of the other U-Frames.

*SNRM = Set Normal Response Mode, is a command sent from TC to open a data link between TC and a work station.

"Numbered frames" means that they in the control field contain a sequence number of messages sent, N(S), waiting to be acknowledged and a sequence number for next message to be received, N(R). The highest sequence number is 7, which means that max 7 frames could await to be acknowledged. However, there is a practical limit of 4 frames waiting for ACK and if this number is exceeded the next frame is rejected.

Packets

The information, "the Packet", is of two types:

- Type 1: (/11): Transmitted data, to which no acknowledgement is expected e.g. "Echo" to display. No flow control is implemented.

- Type 2 (/10): Transmitted data that must be acknowledged by the receiver when executed; e.g. a string of characters printed on the printer. These messages include a flow control byte.

Five different Type-2 messages can be sent:

1. Data packet
2. Receive Ready packet (RR)
3. Receive Not/Ready packet (RNR)
4. Reset packet (RES)
5. Reset Confirmation packet (RESC)

The packet header (the three first bytes of the packet) contains information for the PLSP (Philips Link Sharing Protocol = SLSP, Simple Link Sharing Protocol).

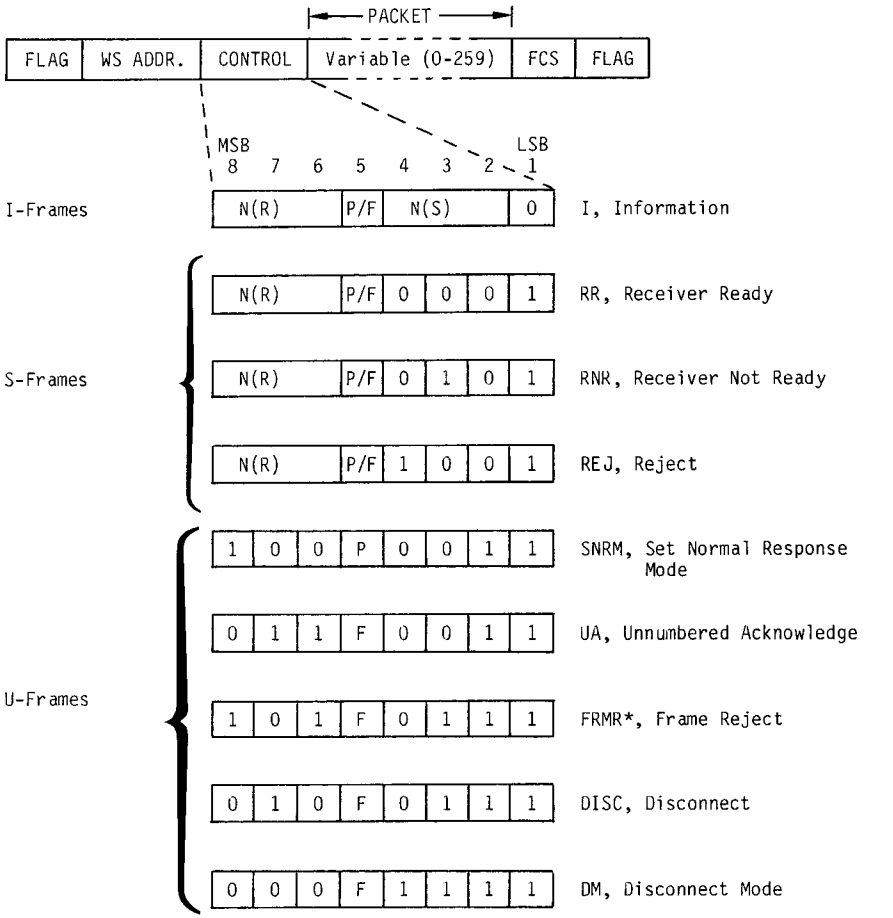
The meaning of these three bytes is shown in some examples below:

Packet Header			Meaning		
Byte 1	Byte 2	Byte 3	Byte 1	Byte 2	Byte 3
10	02	64	Type 2 data	Dev. Addr 2 (Printer)	Counter + Data pack.
10	01	81	Type 2 data	Dev. Addr 1 (Keyboard)	Counters + Flow Contr.
11	01	C0	Type 1 data	Dev. Addr 1	Counter

always "1"

even = Data packet
odd = Flow Control (e g. RR)

The HDLC control byte, the one after the WS address byte, determines which type of frame that is transferred.



* The FRMR contains three more information bytes

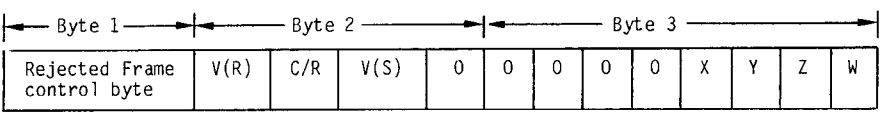


Figure 1.4-2 All Frame-types used at HDLC level (Level 2)

- Bit number 1 is "0" in an I-Frame and "1" in S- and U-Frames.
- Bit number 2 is "0" in an S-Frame and "1" in an U-Frame.
- Bits number 3 and 4 indicate in an S-Frame RR (00), RNR (10) and REJ (01).

BIT 4	BIT 3		Definition
0	0	RR	"Receive Ready Command and Response" used to indicate that the originating station is ready to receive an I-Frame and to acknowledge previously received I-Frames numbered upto N(R)-1.
0	1	RNR	"Received Not Ready Command and Response" used to indicate busy, i.e. temporary inability to accept additional incoming I-Frames. I-Frames upto N(R)-1 are acknowledged.
1	0	REJ	"Reject Command and Response" used to request retransmission of I-Frames starting with the frame N(R). I-Frames N(R)-1 and below are acknowledged.

In a U-Frame these bits together with the bits 6, 7, 8 are called modifier (M) bits.

- Bit number 5 in the control field is called P/F, Poll or Final.

The Poll bit is used in a command, from the TC to a WS, to request a response. This means that a work station cannot transmit until a command with the P bit set to ONE is received.

The Final bit is set in responses from a WS to TC. However, if there are several frames to be transmitted from the same work station, the bit is set to ONE only in the last frame of its response.

- N(S) is the sequence number of the last frame that is sent.
- N(R) is the number of the next frame to be received. The previous frames are acknowledged.

	CONTROL FIELD BIT ORDER							
Type of Frame	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
I-Frame	N(R)			P/F	N(S)			0
S-Frame	N(R)			P/F	S	S	0	1
U-Frame	M	M	M	P/F	M	M	1	1

Figure 1.4-3 Control Field Formats summary

Figure 1.4-4

Important Sequences in HDLC

In the table below is shown the direction of commands and responses. There is also the type of frame indicated.

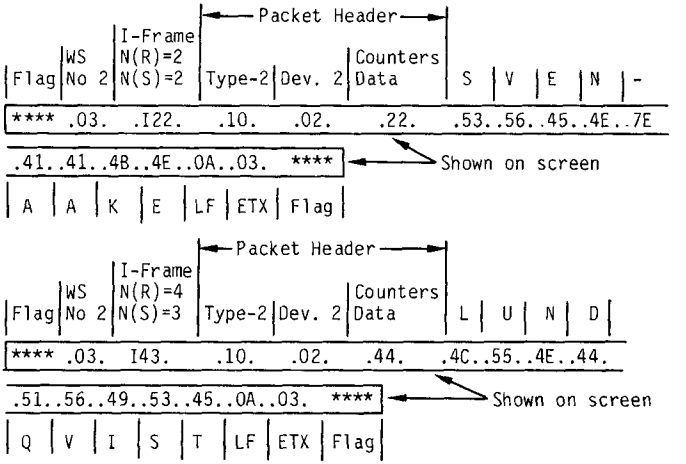
P=1 means polling
F=1 means the final bit in one or more frames from one WS.
I, 1, 3 means that N(R) = 1 and N(S) = 3
X means any number of frames.

	TC or WSC (Primary)	FRAME TYPE	WORK STATION, DLH (Secondary)	COMMENTS
Ex. 1	SNRM, P(=1)	U-	→	Data link opened and WS polled and reset.
		U-	UA, F(=1) ←	Unnumbered Acknowledge.
	RR, N(R)=0, P(=1)	S-	→	WS polled.
	3 possible answers	S-	RR, N(R)=0, F(=1) ←	WS ready, but has nothing to send.
		I-	I,0,0, + 0,1 + 0,2, F(=1) ←	3 I-Frames are sent as example.
		S-	RNR, 0, F(=1) ←	WS not ready and has nothing to send.
	I,X,0 P(=0)	I-	→	Answer in next I- or RR-Frame from WS.
Ex. 2	RR, N(R)=3, P(=1)	S-	→	WS polled.
		I-	I,1,3 + 1,4, F(=1) ←	2 I-Frames.
	REJ, 3. P(=1)	S-	→	Frame 3 is not received by TC so it is rejected.
		I-	I,1,3 + 1,4, F(=1) ←	Retransmission of I-Frames as from N(R)=3
Ex. 3	I,0,X+0,X+1 P(=0)	I-	→	I-Frame, no polling.
	RR N(R)=0 P(=1)	S-	→	WS polled.
		S-	REJ, X, F(=1) ←	Frame X is not received (but X+1 is).
	I,0,X+0,X+1 P(=0)	I-	→	Retransmission of the I-Frame X and X+1.
Ex. 4	RNR,X P(=1)	S-	→	The primary is not ready for more I-Frames, but can receive S-Frames.
		S-	RR, X, F(=1) ←	
		S-	RNR, X, F(=1) ←	
		S-	REJ, X, F(=1) ←	
Ex. 5	SNRM, P(=1)	U-	→	
		U-	FRMR, F(=1) ←	The frame is not correctly received so it is rejected.
	RR, N(R=6), P(=1)	S-	→	Upto frame 5 are acknowledged, polled WS in disconnect mode.
		U-	DM, F(=1) ←	
	DISC	U-	→	TC disconnects the WS.
		U-	UA, F(=1) ←	Frame acknowledged.

Figure 1.4-4 Transfer Sequences

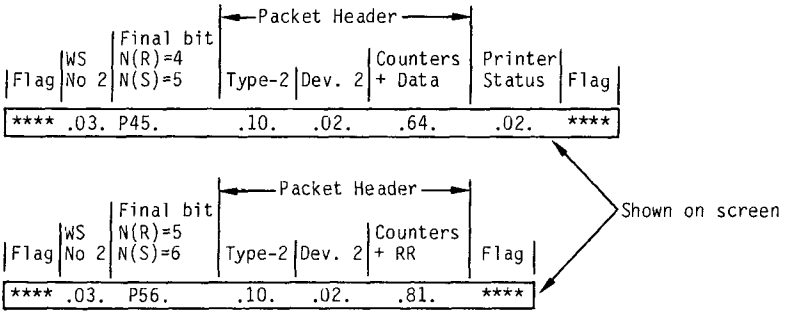
Monitoring LWSI Transmit Line

When using the LWSI Datascope to monitor the communication on an LWSI transmit line, the following picture may be seen. The example shows strings of characters to a printer (device address 2).



Monitoring LWSI Receive Line

When monitoring an LWSI receive line you may see the following examples of replies to strings sent to the printer.



1.4.4 Hierarchy of Control Protocols

Levels in LWSI/RWSI Figure 1.4-5

When a message is transferred between a primary and a secondary station the different parts of the frame is handled at different levels by hardware and program modules. To understand the use of levels we can make a comparison with a message sent from one boss to another.

LEVEL	Definition	Comparison
Level 3 (Highest)	Controls the traffic (PLSP), provides the message with device address (logical channel No.). Based on the CCITT rec. X25.	A boss which decides the contents of a message and to whom it will be sent.
Level 2	Transmission procedure (the HDLC) and Data Link Control provide the message with WS address, add flags, perform failure checks, i.e. format the frame.	The secretary who puts the message in an envelope, writes the address, puts on the stamp.
Level 1	The physical interconnection, the hardware characteristics of the line and interface circuits defined by X27 (V11).	The postal service which transports the envelope.

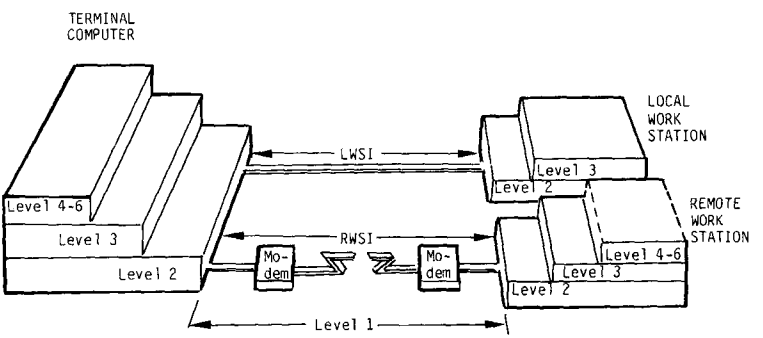


Figure 1.4-5 Data communication levels

Level	Definition	Terminal Computer	Local Work Station	Remote Work Station	Work Station Controller
6	Application	Customer appl.			Customer appl.
5	Device Drivers	Toss			Toss
4	Network Distrib.				
3	Line Driver	PLSP(=DRPL01)X25	PLSP(X25)	PLSP(X25)	
2	Data Link Handler	HDLC	HDLC	HDLC	HDLC
1	Physical Control	X27, V24-V28	X27	V24-V28	V24-V28. X27

Level 3 - PLSP (SLSP)

The Philips Link Sharing Protocol, PLSP, is used on Level 3 and is a real subset based on the CCITT X.25 Recommendations.

The PLSP defines the packet format. data multiplexing to devices, and flow control. All this information is implemented in the three bytes called "Packet Header". This means that the protocol describes how the Link (an established communication channel between a primary and a secondary) is shared between several, so called, "Logical channels".

A Logical Channel is the way for messages between a program module in the terminal computer and a device, and there is one Logical channel per device. The Logical channel is identified by the two first bytes in the packet header.

- the first byte — contains normally the Logical Channel Group Number (LCGN) indicated by 4 bits enabling upto 16 groups. PTS, however, uses only two of these to indicate Type-1 and Type-2 messages.

- the second byte — contains normally the Logical Channel Number (LCN) and by using all the 8 bits upto 256 channels may be addressed.

  LWSI uses this byte for the Device Address, 0-7.
  Device Address 1-7 addresses the devices as usual, i.e. keyboard =1, printer =2, VDU =3 etc. The Device Address 0 is used for commands to the main module itself, e.g. MDA 6411, that controls the communication with the devices.

The third byte in the packet header is used for the "Flow Control"., which means control of messages sent and received to/from a work station.

The byte contains counters for sent and received messages similar to the use of the control byte in the HDLC procedure at level 2. The reason for this flow control is to avoid overloading of the Link, by slowing-down the originator of the messages.

Counting of transferred messages is performed by ring counters counting upto 7 and thereafter starting from 0.

Though the counters can handle upto 7 messages to be sent without being immediately acknowledged, there are limits set by PTS. These limits called "windows" are the space of buffers available in respective primary and secondary unit.

- Windows on Level 3 & 2 Figure 1.4-6

There are different Windows (buffer sizes) used at level 3 and level 2.

- Level 3 windows *) (PLSP)
  1) Primary Secondary
  The window is 1 message except for output to VDU, where the window size is 2 messages.
  2) Secondary Primary
  At input to the primary the window size is 7.
- Level 2 (HDLC) windows
  Primary Secondary
  The window size is 4 messages in both directions.

The PLSP is in the primary unit handled by the program module "line driver DRPL01" and in the secondary units by the Logical Channel Handler, LCH (firmware module).

The DRPL01 supports both type-1 and type-2 packets. There are some limits in DRPL01 and packets that cannot be received by DRPL01 will be considered illegal, even if they are legal according to the SLSP definition.

Note: Toss releases 11 or above must be used.

*) These window sizes might be adapted for new devices.

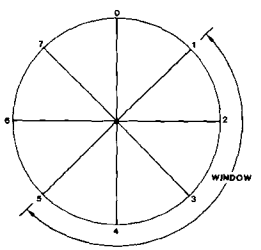


Figure 1.4-6 Message counter with a window of 4 messages

CONTENTS

LIST OF ILLUSTRATIONS & TABLES

2.1 PREPARING CABLES FOR STAR-CONNECTED WORK STATIONS

2.1.1 Specification of Required Materials

Figure 2.1-1

General

Most cables required for connecting work stations to a computer must be prepared at the installation site. Figure 2.1-1 illustrates the different types of cables that may be required when work stations are star-connected to a computer.

PLEASE NOTE THE MAXIMUM LENGTHS INDICATED!

Two types of cables and six types of connectors are used, see following specifications.

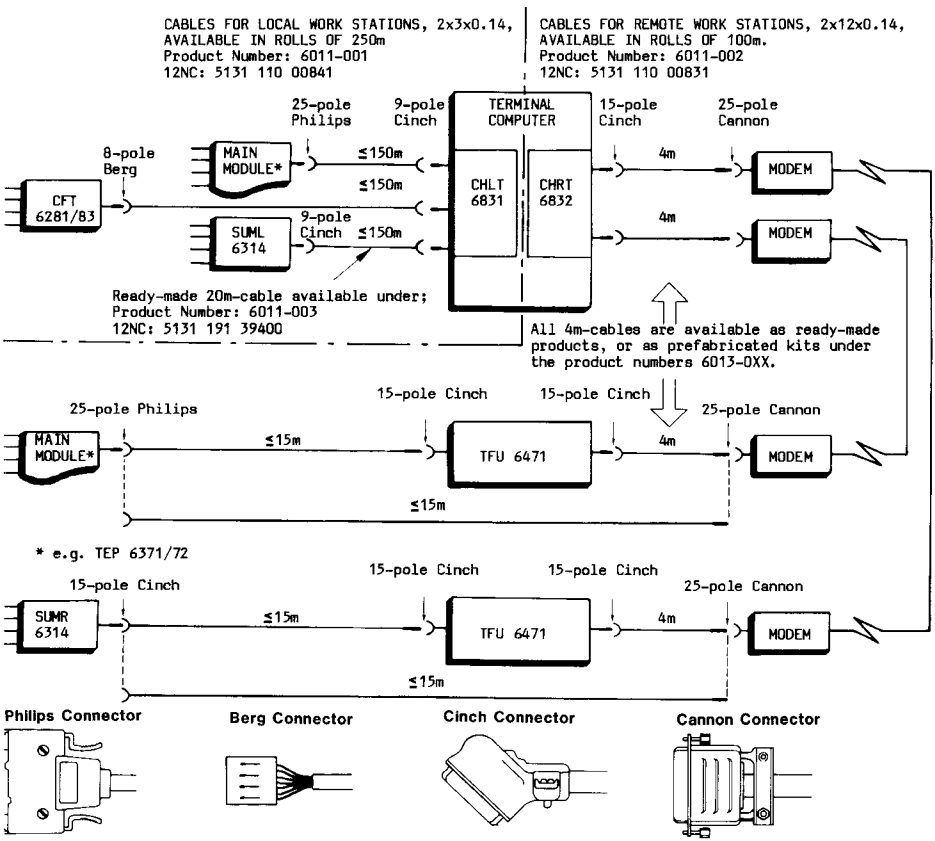


Figure 2.1-1 Cables for Star-Connected Work Stations

Cables for Local Work Stations

The cables for local work stations have 3 twisted pairs of conductors and are screened. Required specification and a typical manufacturer's (Kromberg & Schubert) part number is:

3 x 2 x 0.14 mm, grey, outside diameter 5.6 ± 0.4 mm
Kroshu type 37 080 30

Other cable to the same specification, and made by any other manufacturer, may be used instead.

Within Philips the cable is available in 6kg-rolls of 250 m under;

Product number: 6011-001
12NC: 5131 110 00841

Cables for Remote Work Stations

The cables for remote work stations have 12 twisted pairs of conductors and are screened.

Required specification and a typical manufacturer's (Kromberg & Schubert) part number is:

12 x 2 x 0.14 mm, grey, outside diameter 9.1 ± 0.4 mm
Kroshu type 37 081 20

Other cable to the same specification, and made by any other manufacturer, may be used instead.

Within Philips the cable is available in 8kg-rolls of 100 m under;

Product number: 6011-002
12NC: 5131 110 00831

9-pole Cinch Connector

All cable ends that are to connect to the CHLT, or to a SUML, must be fitted with 9-pole female connectors consisting of:

- Cinch Shell R43 81960 00 000
- Cannon Connector DEC 9S-F0
- Cannon Sockets 030-1953 00 000

Kits containing all parts required to mount 50 connectors (excluding cable markers) are available under;

Product number: 6012-004
12NC: 5131 191 44500

15-pole Cinch Connectors

All cable ends that are to connect to the CHRT, a TFU or a SUMR must be fitted with 15-pole male/female connectors (1 male and 3 female terminations). These connectors consist of:

- Cinch Shell R43 81962 00 000 (with cable entry bored out to 12 mm diameter)
- Cannon Connector DAC 15C-F0
- Cannon Sockets 030-1953 00 000 (female terminations)
- Cannon Pins 030-1952 00 000 (male terminations)

Kits containing all parts required to mount 50 connectors (excluding cable markers) are available under;

	Female type	Male type
Product number:	6012-002	6012-003
12NC:	5131 191 44300	5131 191 44400

25-pole Philips Connector

A cable end that is to connect to a TEP 6371 must be fitted with a 25-pole female connector, consisting of:

- Philips Shell
- Cannon Connector DBC 25S-F0
- Cannon Sockets 030-1953 00 000

Kits containing all parts required to mount 50 connectors (excluding cable markers) are available under;

Product number: 6012-006
12NC: 5131 191 91100

25-pole Cannon Connector

A cable end that is to connect to a modem must often (exceptions occur) be fitted with a 25-pole male connector, consisting of:

- Cannon Shell DB 24659
- Cannon Connector DBC 25P-F0
- Cannon Pins 030-1952 00 000
- Lock D 20419

Kits containing all parts required to mount 50 connectors (excluding cable markers) are available under;

Product number: 6012-001
12NC: 5131 191 44200

8-pole Berg Connector

A cable end that is to connect to a CFT 6281/83 must be fitted with an 8-pole female connector, consisting of:

- Berg Connector Block 65043-033
- Berg Sockets 47712
- Philips Connector Unit

Kits containing all parts required to mount 50 connectors (excluding cable markers) are available under;

Product number: 6012-001
12NC: 5131 194 30200

Ready-Made or Prefabricated Cables

The following cables are available as ready-made products, or as prefabricated kits:

- Ready-made 20m-cable for CHLT-SUML.
  Product number: 6011-003
  12NC: 5131 191 39400

- Ready-made 4m-cable for CHRT/SUMR/TFU - Modem ITT, GH 2054.
  Product number: 6013-011
  12NC: 5131 191 33710

- Prefabricated 4m-cable for CHRT/SUMR/TFU - any modem (modem end open).
  Product number: 6013-002
  12NC: 5131 191 89700

- Prefabricated 4m-cable for modem connection, both cable ends open.
  Product number: 6013-001
  12NC: 5131 191 41700

2.1.2 Routing and Labelling

Figure 2.1-2

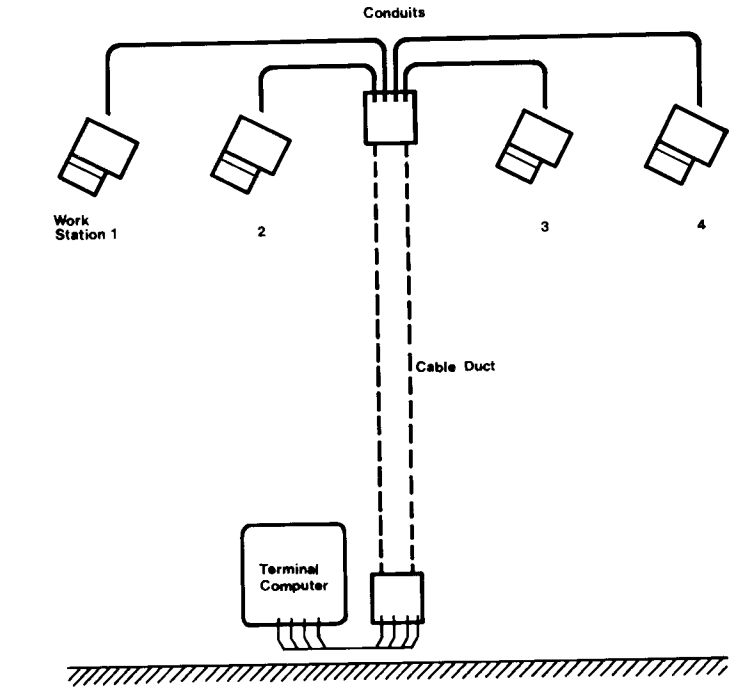
All cables longer than 4 m should be routed the shortest practical way between interconnecting units, but should be protected against mechanical damage by running them in ducts, where available, or in conduits (plastic or metal). The cable should emerge from this protection not more than 1 m from the unit it is to connect to at either end. This means that a combination of duct and conduit routing must sometimes be used.

If conduits are used, they must not be bent to a radius of less than 200 mm, and no more cables than can be easily accommodated, should be routed through each conduit. Note also that although normal mains cables and signal cables can be routed together through the same conduit, signal cables should not be closer than 30 mm to high voltage power cables, when parallel to them.

Crossing of high voltage cables is permitted, but the angle should be at approx. 90° to minimise interference effects.

Once the cables are laid in place, they should be cut to length, ensuring sufficient free cable to allow the units to be moved for service purposes.

All cables should be provided with a plain label at each end, and a cable drawing that illustrates the routing and fitted labels should be made up.



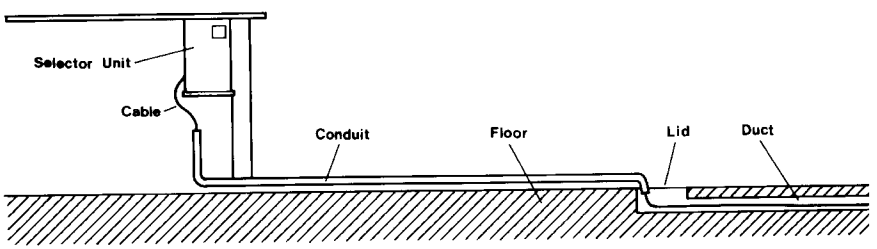


Figure 2.1-2 Examples of Cable Routing for Star-Connected Work Stations

2.1.3 Assembly Instructions

Special Tools Required

In addition to normal electricians tools, the following are required for mounting the connectors on the cables:

- Crimping tool for Cannon pins 030-1952-00-000 (AWG 20) and Cannon sockets 030-1953-00-000 (AWG 20), which can be either;
  MS-3193-1: Crimping tool plus Locator AWG 20 or,
  MS-3193-4 (MIL-T-22520) Crimping tools plus Turret (selectable wire dimensions).

  Such tools are manufactured by:

  a. Daniels Manufacturing Comp.
  b. Buchanan Electrical Products omp. Union
  c. Thomas & Bett

- Suitable insertion/removal tools such as Cannon CIET-20 MDB

- Equipment to heat shrink the tubings

- Crimping tool AMP 49935 (for AMP jointing sleeves, 34137)

- Crimping tool Berg 13921, for Berg connectors (CFT-cables)

Mounting Cinch Connectors Figure 2.1-3

- Cut the cable to its precise length (allowing for subsequent movement of equipment for servicing).

- Thread the cable marker(s), shrink tubing(s) and the connector shell onto the cable.

- Strip the cable end (A), apply the copper-foil tape (B), fold back the screen and secure with electro tape (C).

- For 15-pole connectors only; separate, cut and strip the return wires (see sub-section 2.1.4) and twist them together with the C-wire. Thread on and crimp the jointing sleeve and insulate with shrink tubing. Cut off wires not used at the end of the cable sheath (D), (see sub-section 2.1.4).

- Strip 4 mm of each wire end (including the C-wire in 15-pole connectors) and crimp on the sockets or the pins.

- Fit the sockets/pins into appropriate positions of the connector block according to sub-section 2.1.4.

- Fit the shell and shrink tubing(s), ensuring that there is good contact between the clamp and the cable screen (F, G).

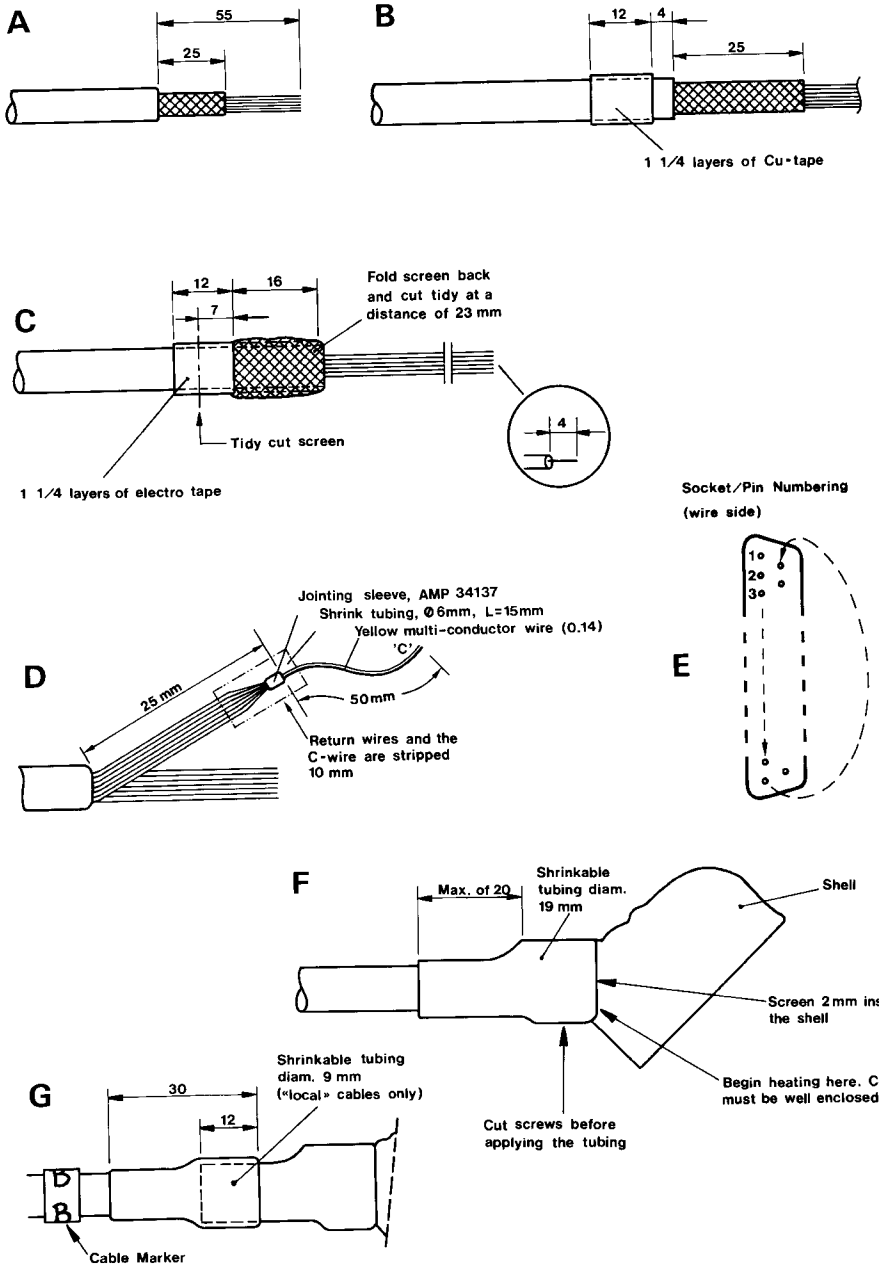


Figure 2.1-3 Mounting Cinch Connectors

Mounting Philips Connectors Figure 2.1-4

- Cut the cable to its precise length (allowing for subsequent movement of equipment for servicing).
- Thread the cable marker(s) and metal tubing D onto the cable (the wide tubing for 12-pair 'remote' cables, and the narrow tubing for 3-pair 'local' cables).
- Cut and remove 55 mm of the cable sheath. Adjust the metal tubing to be in line with the edge of the remaining cable sheath.
- Fold the screen back over the tubing, and cut it tidy at the rear edge of the tubing.
- For 12-pair 'remote' cables only; cut and strip the return wires (see sub-section 2.1.4) and twist them together with the C-wire. Thread on and crimp the jointing sleeve and insulate with shrink tubing. Cut off wires not used at the end of the cable sheath (see sub-section 2.1.4).
- Strip 4 mm of each wire end (including the C-wire in 12-pair cables) and crimp on the sockets. Thread the wires through connector support E and fit the sockets into appropriate positions of the connector block according to sub-section 2.1.4.
- Assemble connector block F, support E and springs G together with the base of the shell (H).
- Fix the cable to the base of the shell by screwing the two clamps (I) over the screen and the metal tubing (wide clamp groove against 12-pair 'remote' cables and narrow groove against 3-pair 'local' cables).
- Arrange a neat wire package behind the connector block, assemble the locking arms (J) with springs (K) and screw on the top of the shell (L).

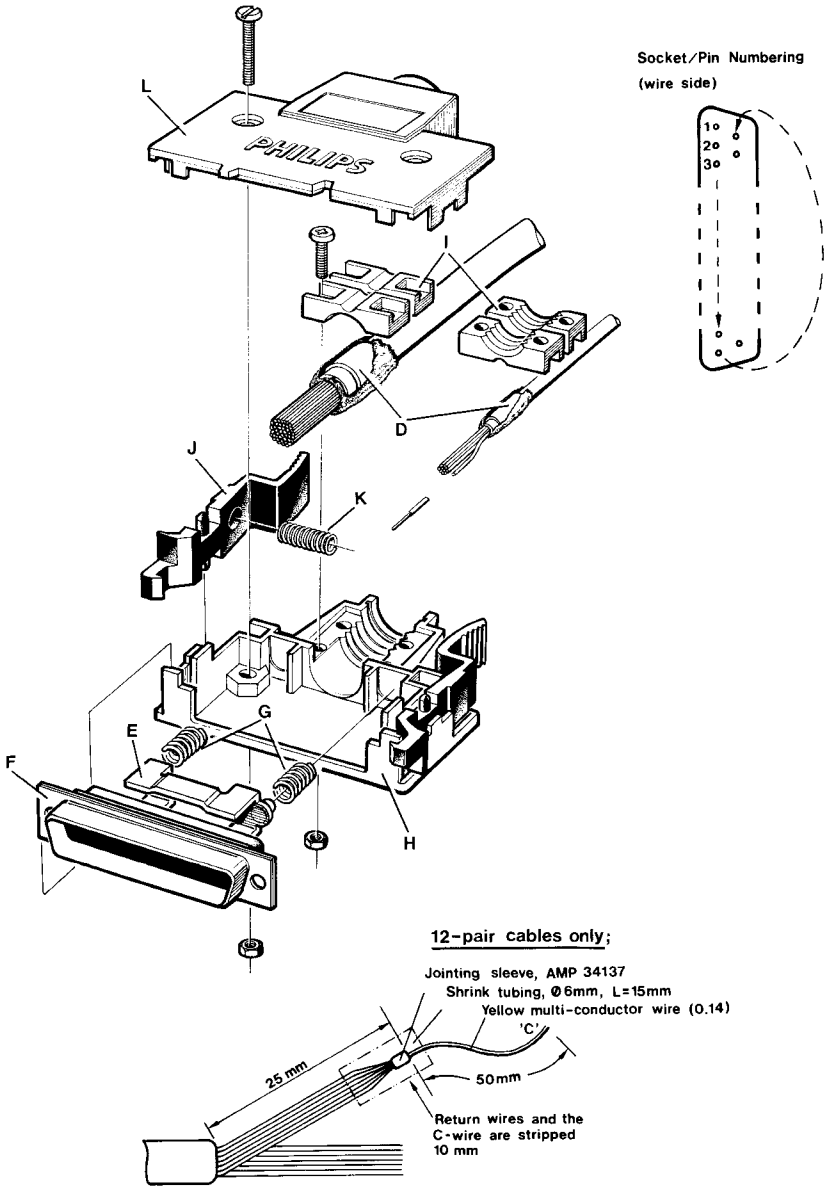
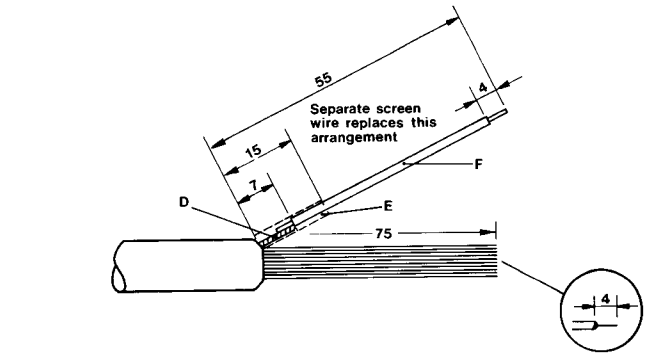
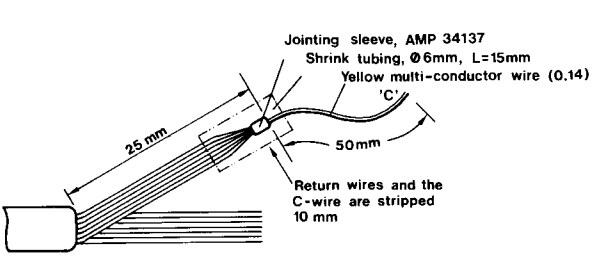


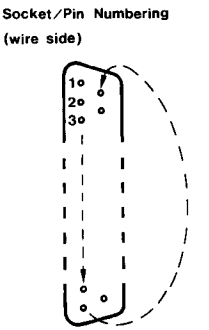
Figure 2.1-4 Mounting Philips Connectors

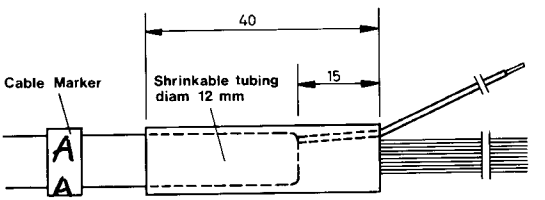
Mounting Cannon Connectors Figure 2.1-5

- Cut the cable to its precise length (allowing for subsequent movement of equipment for servicing).
- Thread cable marker(s), shrink tubing and connector shell on to the cable.
- Strip the cable end.
- For cables without separate screen wire; split the screen and twist it into a "wire" (D), solder the F-wire to the twisted part and insulate with PVC tubing (E).
- For cables with separate screen wire; cut the screen at the end of the cable sheath and cut the screen wire to a length of 55 mm, insulate with PVC tubing (diameter: 2.5 mm, length: 45 mm).
- Separate, cut and strip the return wires (see sub-section 2.1.4) and twist them together with the C-wire. Thread on and crimp the jointing sleeve and insulate with shrink tubing.
- Cut off wires not used at the end of the cable sheath (see sub-section 2.1.4).
- Strip 4 mm of remaining wires (including the C-wire and any F-wire) and crimp on Cannon pins.
- Fit the pins into appropriate positions of the connector block according to sub-section 2.1.4.
- Apply the shrink tubing and mount the shell.









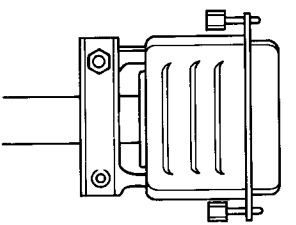
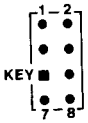


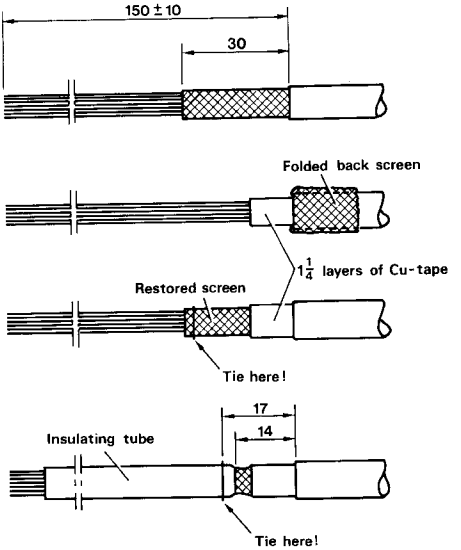
Figure 2.1-5 Mounting Cannon Connectors

Mounting Berg Connectors Figure 2.1-6

- Cut the cable to its precise length (allowing for subsequent movement of equipment for servicing).
- Thread on cable marker(s) and strip the cable end according to top figure.
- Fold screen back over the sheath and apply 1 1/4 layers of Cu-tape around the wires, close to the sheath.
- Restore the screen and apply another 1 1/4 layers of Cu-tape, now around the screen over the previous layers.
- Tie the fore part of the screen, thread on the insulating tube and tie it at the rear end.
- Strip 4 mm of the wire ends and crimp on the sockets.
- Fit the sockets into appropriate positions of the connector block according to sub-section 2.1.4.
- Mount the connector unit, ensuring that there is a good contact between the bare Cu-tape and the lower clamp.

Socket seen from wire side





PHILIPS CONNECTOR UNIT

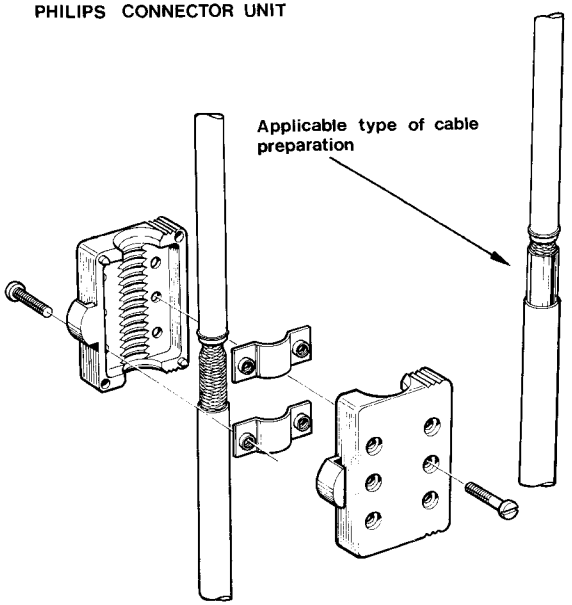


Figure 2.1-6 Mounting Berg Connectors

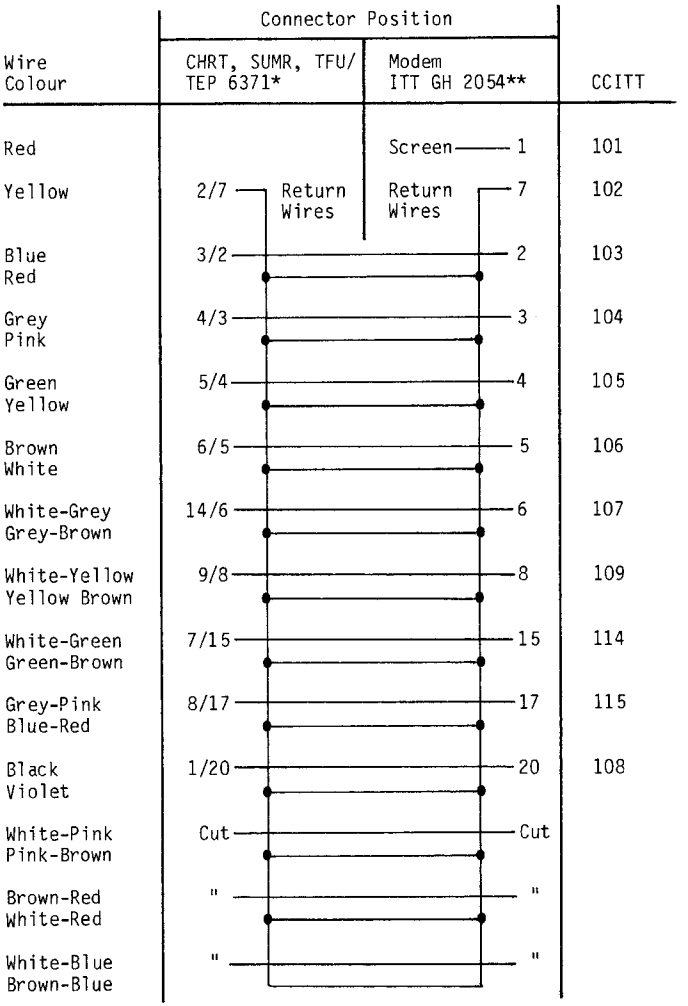
2.1.4 Interconnection Diagrams

Local Work Station Cables

Wire Colour	Connector Position: CHLT	Connector Position: SUML, Main Module/CFT 6281,6283*	Signal
Grey	1	1/1	Data in to TC
Pink	2	2/2	" " " "
Green	3	3/3	Data out from TC
Yellow	4	4/4	" " " "
Brown	5	5/7	Clock from TC
White	9	9/6	" " "

* First position number applicable for connectors that terminate at SUML or Main Module (e.g. TEP 6371/72). Second number applicable for terminations at CFT 6281 or CFT 6283.

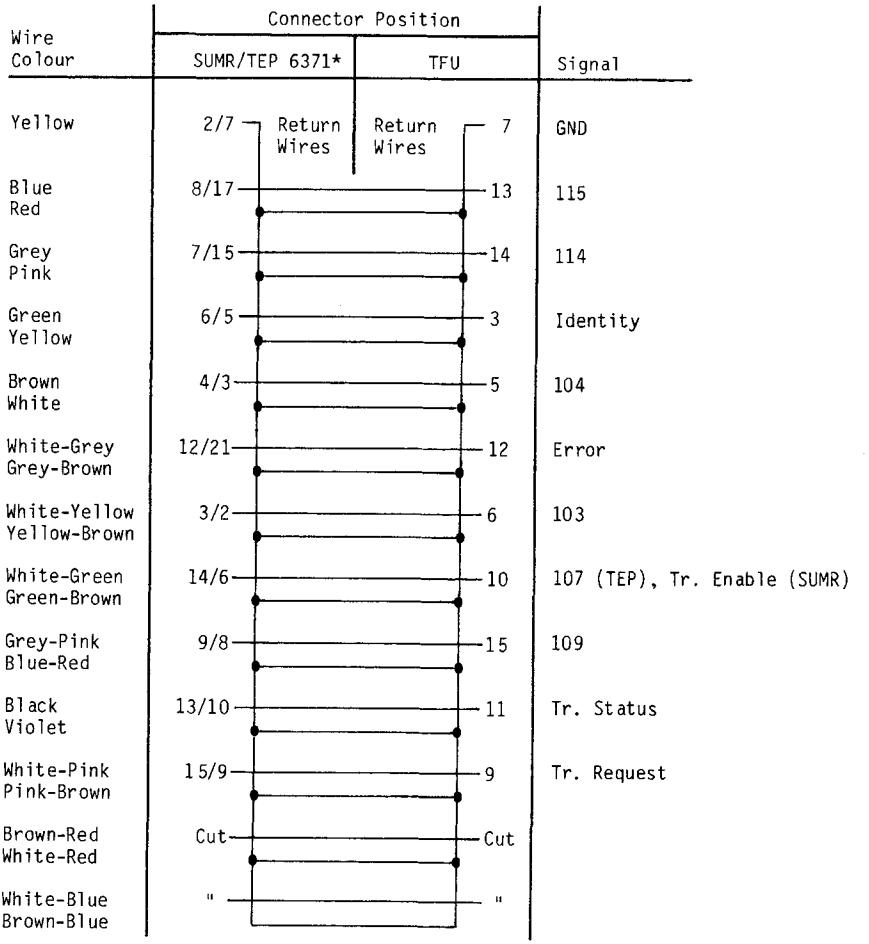
Modem Cables for Remote Work Stations



* First position number applicable for connectors that terminate at CHRT, SUMR or TFU. Second number applicable for TEP 6371 terminations.

** The pin numbers given for "Modem" are applicable for ITT GH 2054. If other modem is used; check the relation between pin numbers and "CCITT" numbers (connect against "CCITT" numbers)!

Cables Between Remote Work Stations and TFU



* First position number applicable for connector that terminates at SUMR, second number applicable for TEP 6371 termination.

2.2 PREPARING CABLES FOR MULTIDROP-CONNECTED WORK STATIONS

2.2.1 Basic Materials Required

Figure 2.2-1

General

Figure 2.2-1 illustrates the cabling necessary when work stations are multidrop-connected to a computer. The head line of a local network must always be prepared at the installation site, whilst the drop cables are available as ready-made accessories or prefabricated kits. This subsection defines the basic materials required for the interconnections shown in the figure.

> NOTE THE RELATION BETWEEN THE NUMBER OF WORK STATIONS AND THE MAXIMUM LENGTH OF LOCAL HEAD LINE!

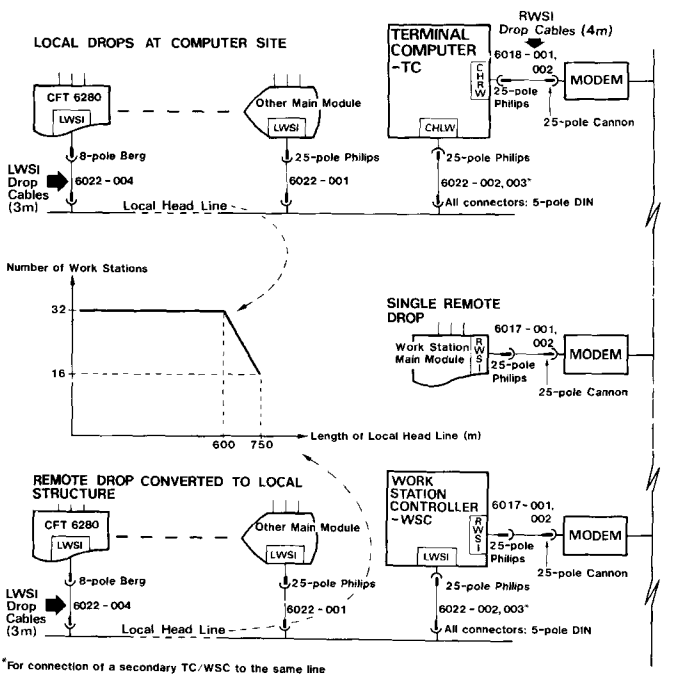


Figure 2.2-1 Cables for a typical Multidrop Configuration

Cable for Local Head Line

The head line of a local network is made up from the same cable type as the local star lines, see subsection 2.1.1 - Cables for Local Work Stations.

Connection Boxes

Figure 2.2-2

Each drop on a local head line is made via a connection box that allows the connection of one work station via a 3m drop cable. Kits containing all parts required to mount 50 connection boxes are available under;

Product number; 6021-001
12NC:

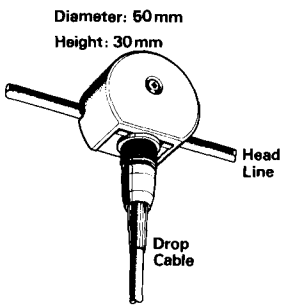


Figure 2.2-2 Connection Box

Terminating Resistors

Both ends of a local head line must be provided with two terminating resistors (even if the computer is connected to one of the ends). The resistor values depend on the number of connected work stations (via 3 m drop cables):

- 1-8 work stations = 270 ohm
- 9-32 work stations = 390 ohm

Ready-Made LWSI Drop Cables

The following 3m-cables are available as ready-made accessories for connecting computers and work stations to the head line of a local network:

- Cable to primary computer's interface, CHLW 6895
  Product number: 6022-002
  12NC: 5131 194 16900

- Cable to secondary computer's interface, CHLW 6895 (used for computer-to-computer communications)
  Product number: 6022-003
  12NC: 5131 194 38100

- Cable to the LWSI of a work station's main module (e.g. TEP 6371/72, GTP 6374, VDU 6347, MDA 6411)
  Product number: 6022-001
  12NC: 5131 194 16700

- Cable to the LWSI of a CFT 6280
  Product number: 6022-004
  12NC:

Ready-Made or Prefabricated RWSI Drop Cables

The following 4m-cables are available as ready-made accessories, or as prefabricated kits, for connecting computers and work stations to a remote line via modems:

- Prefabricated cable kit for connecting terminal computer (CHRW 6896) or work station controller to modem, modem end open.
  Product number: 6018-001
  12NC:

- Ready-made cable for connecting terminal computer (CHRW 6896) or work station controller to modem according to ECMA V23/V26.
  Product number: 6018-002
  12NC:

- Prefabricated cable kit for connecting a work station main module to modem, modem end open.
  Product number: 6017-001
  12NC:

- Ready-made cable for connecting a work station main module to a modem according to ECMA V23/V26.
  Product number: 6017-002
  12NC:

2.2.2 Detailed Specification of Drop Cable Materials

General

Although it is recommended to use ready-made or prefabricated drop cables, there may be circumstances that forces the installation engineer to make his own drop cables. This subsection therefore gives a detailed specification of the materials required for making such cables. However, keep in mind that:

> LOCAL DROP CABLES SHOULD NOT BE LONGER THAN 3 M, AND REMOTE DROP CABLES MUST NOT BE LONGER THAN 15 M, OTHERWISE THE SYSTEM'S PERFORMANCE WILL BE AFFECTED!

Cable for Local Drops

Local drop cables are made up from the same cable type as local star lines, see sub-section 2.1.1 - Cables for Local Work Stations.

Cable for Remote Drops

Remote drop cables are made up from the same cable type as remote star lines, see sub-section 2.1.1 - Cables for Remote Work Stations.

5-pole DIN Plug

All local drop cables are fitted with a 5-pole DIN plug at the end that matches the connection boxes of the local head line.

Kits containing all parts required to mount 50 plugs are available under;

Product number: 6012-008
12NC:

25-pole Philips Connectors

All drop cables, except for 6022-004 to CFT 6280, are fitted with Philips connectors at the end opposite to the local head line or the modem. Female connectors are used against work station main modules, male connectors against terminal computers and work station controllers.

Kits containing all parts required to mount 50 connectors are available under;

	Female type	Male type
Product number:	6012-006	6012-005
12NC:	5131 191 91100	5131 191 91000

8-pole Berg & 25-pole Cannon Connectors

A local drop cable for the CFT 6280 is fitted with an 8-pole female connector of type Berg at the device end, and remote drop cables are usually fitted with a 25-pole male connector of type Cannon at the modem end. Kits for mounting such connectors are defined in subsection 2.1.1.

2.2.3 Routing

Head Line

The head line of a local network should be routed the shortest practical way between the drop points (connection boxes), but should be protected against mechanical damage by running it in ducts, where available, or in conduits (plastic or metal). The line should emerge from this protection not more than 1 m from each connection box.

When routing the line in conduits built into the walls, it should be noted that the exits to connection boxes must easily accomodate two cables, one incoming to the box and one outgoing to the next box (see construction of connection box in Figure 2.2-3).

The head line is allowed to be routed in the same conduit as normal mains cables, and in parallel with high voltage power cables, only if they are not closer to each other than 30mm . Crossing of high voltage cables is permitted, but should be at approximately 90° to minimise interference effects.

> WHEN ROUTING THE CABLE BEFORE FITTING CONNECTION BOXES - MAKE SURE THAT A SUFFICIENT CABLE LOOP IS LEFT AT EACH DROP POINT!

Drop Cables

Local drop cables of 3 m-lengths are usually installed without any special protection against mechanical damage, i.e. these cables are usually not routed in conduits or similar aids. However, special circumstances that require such protections may be at hand, and in such cases you should pay the same attention to interference considerations as for the head line.

Remote drop cables, that are allowed to reach a length of 15 m, will more likely require some kind of protection, and the same interference considerations should be taken into account even here.

2.2.4 Assembly Instructions

Special Tools Required

For covering the full assembly work, including also the production of drop cables, you will need the tools defined in subsection 2.1.3.

Mounting Connection Boxes on Local Head Lines Figure 2.2-3

- Screw the base plate of the connection box onto the applicable surface, properly positioned to match the cable routing.
- Cut the cable and hold both ends in clamped positions according to the applicable alternative in Figure 2.2-3. Cut each end so that 50 mm remains after the second clamp.
- Strip the cable end, apply electro tape to level the cable sheath and fold back the screen. Cut the screen tidy to a length of 17 mm.
- Strip wire ends and rejoin the two cable ends by soldering the wires together in the DIN socket positions shown in Figure 2.2-3.
- Ensure that the locking tag of the DIN socket fits into the slot of the base plate, and screw the socket firmly to the plate.
- Fix the cables to the base plate by screwing on the two clamps. Ensure that no strands from screen or wires are able to cause short-curcuits.
- If the cable is routed on the surface; remove the two prepunched flaps from the cover to open the cable entries.
- Screw on the cover to the base plate.

NOTE

TERMINATING RESISTORS (VALUES ACCORDING TO SUBSECTION 2.2.1) MUST BE FITTED IN THE CONNECTION BOXES AT EACH END OF THE LINE. THE RESISTORS ARE SOLDERED IN BETWEEN THE SOCKET POSITIONS 1 AND 2, AND BETWEEN THE POSITIONS 4 AND 5.

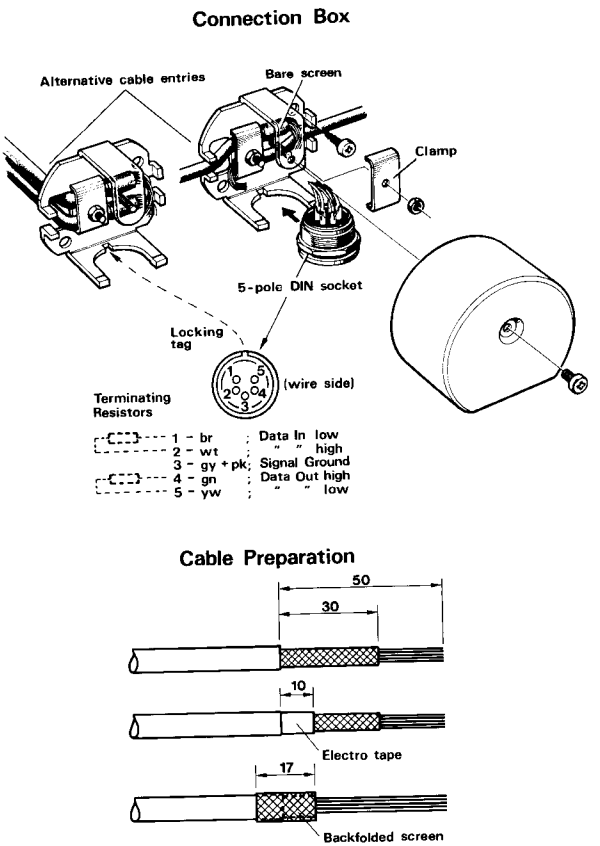
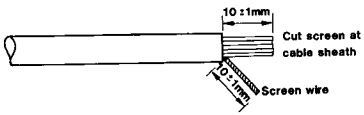
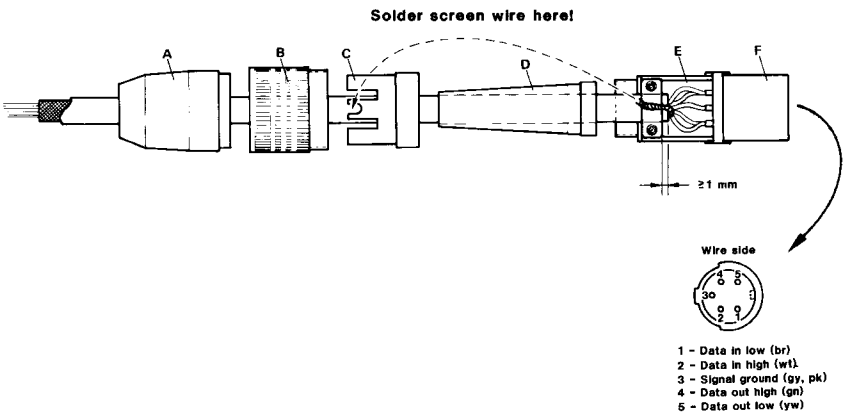


Figure 2.2-3 - Mounting Connection Boxes

Mounting DIN Plugs on Local Drop Cables Figure 2.2-4

- Thread connector parts A, B, C and D onto cable as shown in figure.
- Prepare cable end and strip wire ends.
- Loosen pin holder (F) and solder wires into appropriate plug positions.
- Fix cable in clamp holder (E), reassemble with pin holder (F) and push ground casing (C) onto the assembled holders.
- Solder screen wire to the ground casing (C) as shown in figure.
- Assemble complete plug by screwing the end piece (A) onto the clamp holder (E).





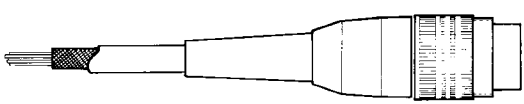


Figure 2.2-4 Mounting Din Plugs

Mounting Cannon Connectors Figure 2.2-5

- Thread shrink tubing and connector shell on to the cable, strip the cable end.
- For cables without separate screen wire; split the screen and twist it into two "wires" (D), solder the F- and G-wires to the twisted parts and insulate with PVC tubing (E).
- For cables with separate screen wire; cut the screen wire to a length of 55 mm, insulate with PVC tubing (diameter: 2.5 mm, length: 45 mm). Split the screen and twist it into one "wire" (D). Solder the G-wire to the twisted part and insulate with PVC tubing (E).
- Separate, cut and strip the return wires (see subsection 2.2.5) and twist them together with the C-wire. Thread on and crimp the jointing sleeve and insulate with shrink tubing.
- Strip 4 mm of wire ends (including the C-wire and any F-wire) and crimp on Cannon pins.
- Fit the pins into appropriate positions of the connector block according to subsection 2.2.5.
- Strip the G-wire and crimp on the screw terminal (H).
- Apply the shrink tubing and mount the shell, ensuring that the screw terminal is firmly fastened to the rear part of the shell.

Mounting other Connectors

Other drop cable connectors (Philips and Berg) are mounted according to the technique described in subsection 2.1.3, however, now consulting the Interconnection Diagrams in subsection 2.2.5.

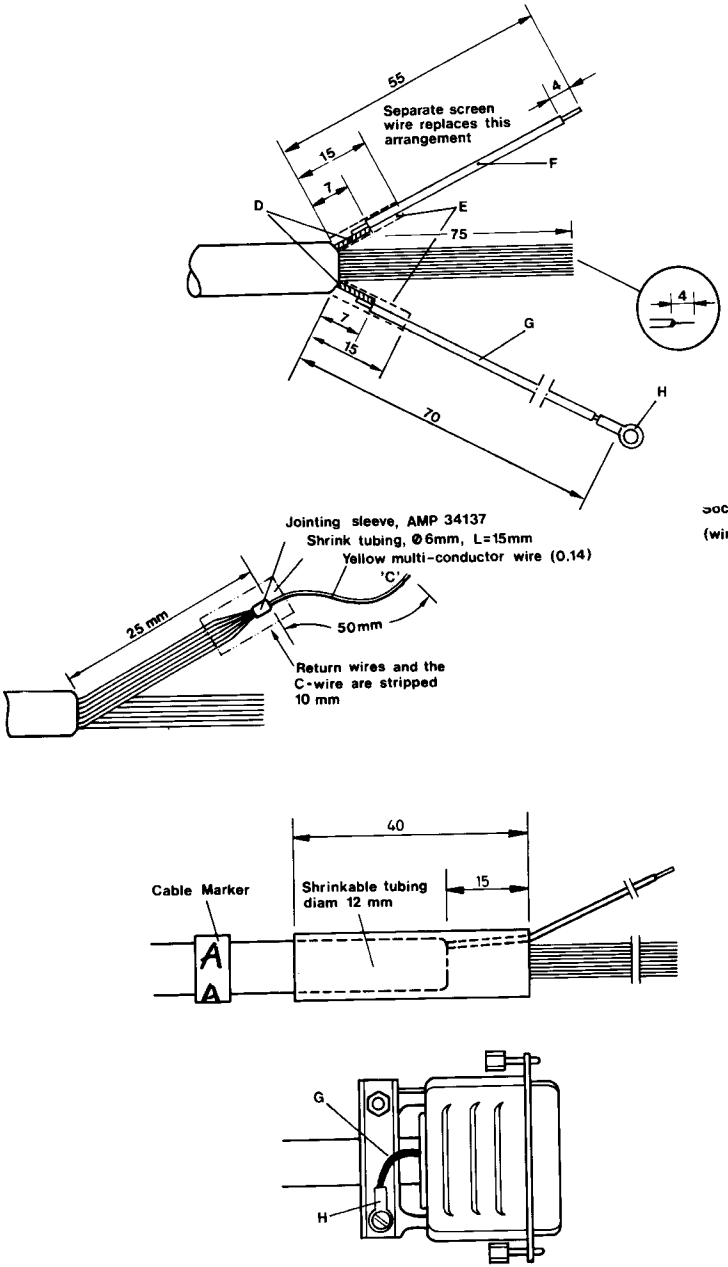


Figure 2.2-5 Mounting Cannon Connectors

2.2.5 Interconnection Diagrams

Local Drop Cables 6022-001/002

Wire Colour	Connector Position DIN	Philips	Signal
Grey	3	7	Signal Ground
Pink	3	7	Signal Ground
Green	4	3	Data Out-high
Yellow	5	5	Data Out-low
Brown	1	4	Data In-low
White	2	2	Data In-high

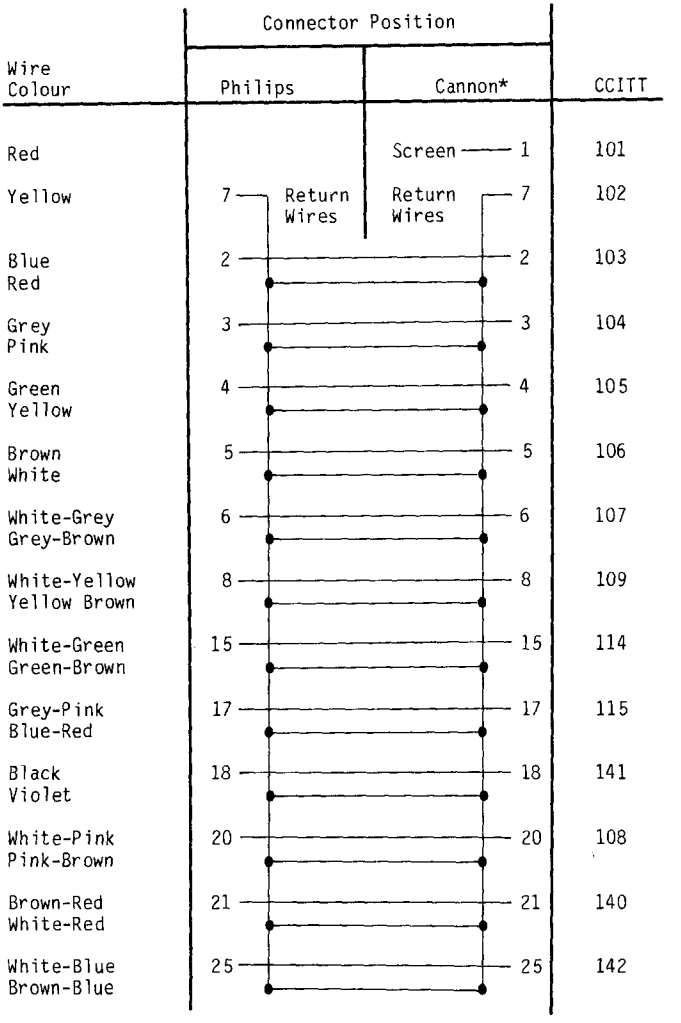
Local Drop Cable 6022-003

Wire Colour	Connector Position DIN	Philips	Signal
Grey	3	7	Signal Ground
Pink	3	7	Signal Ground
Green	4	4	Data Out-high
Yellow	5	2	Data Out-low
Brown	1	3	Data In-low
White	2	5	Data In-high

Local Drop Cable 6022-004

Wire Colour	Connector Position DIN	Berg	Signal
Grey	3	1	Signal Ground
Pink	3	7	Signal Ground
Green	4	4	Data Out-high
Yellow	5	5	Data Out-low
Brown	1	3	Data In-low
White	2	2	Data In-high

Remote Drop Cables 6017-001/002 and 6018-001/002



* Fitted only on 6017-002 and 6018-002, both 001-versions are open towards modem.

2.3 PREPARING CABLES FOR ON-LINE CONNECTIONS

2.3.1 Specification of Required Materials

General

Modem cables for on-line connections may appear in many different versions, depending on different types of line controllers and modems. Ready-made cables are available for the most common combinations of line controllers and modems, and prefabricated kits (with "open" connectors) are available for making cables for other combinations.

However, common for all cables is that they have a limited length (4-5 m) and are composed of the same basic elements;

- Cable consisting of 12 twisted pairs of conductors (12 x 2 x 0.14 mm, Kroshu type 37 081 20).
- 25-pole female connector of Cinch type for termination at CHLC-plug, or (for CHLC 6838/6839) a 26-pole female connector for rack mounting.
- 25-pole male connector of Cannon type for modem termination.

Ready-Made or Prefabricated Cables

The following ready-made or prefabricated cables are available:

CHLC Type	Modem Type or Interface	Cable Identifications	
		Product No.	12NC
Open (Cinch)	Open	6014-001	5131 191 41800
6834/6836	Open	6014-002	5131 191 89800
6834/6836	ITT GH 2054	6014-011	5131 191 34400
6835	ITT GH 2052C-16	6014-012	5131 191 47000
6835	24 LSI Racal Milgo	6014-013	5131 191 61900
6837	TSU	6014-014	5131 191 62000
6838/6839	Open	6015-002	5131 191 94300
6838/6839	See note	6015-003	5131 191 94400
6891	X21/HDLC	6016-002	5131 194 09300

Note: CHLT 6838 can be connected to an asynchronous V23 modem not using CCITT 115.
CHLC 6839 can be connected to a synchronous V23 modem not using CCITT 119.

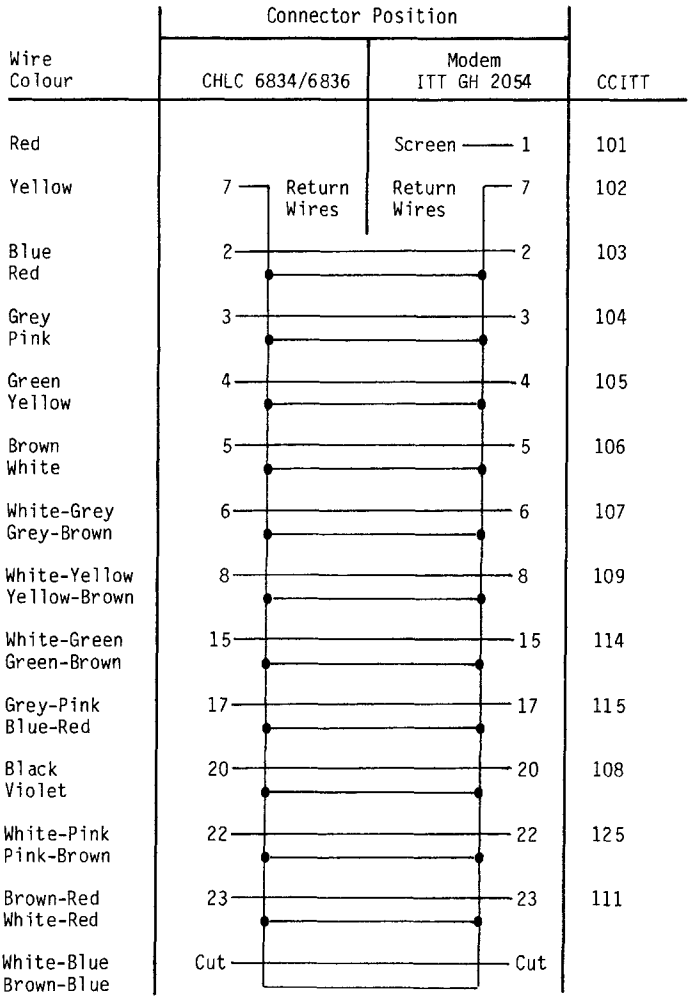
2.3.2 Assembly Instructions

When assembling prefabricated cables, you must have access to the special tools mentioned in sub-section 2.1.3.

Cinch- and Cannon connectors are mounted according to the technique described in sub-section 2.1.3, however, now consultating the Interconnection Diagrams in sub-section 2.3.3.

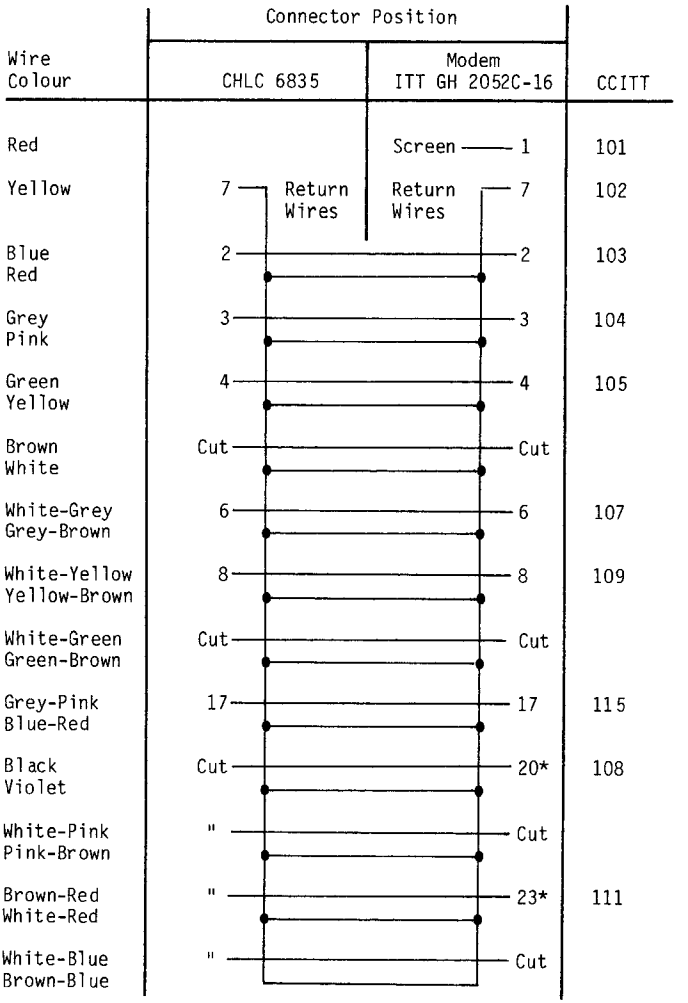
2.3.3 Interconnection Diagrams

Cable for CHLC 6834/6836 - Modem ITT GH 2054 (6014-011)



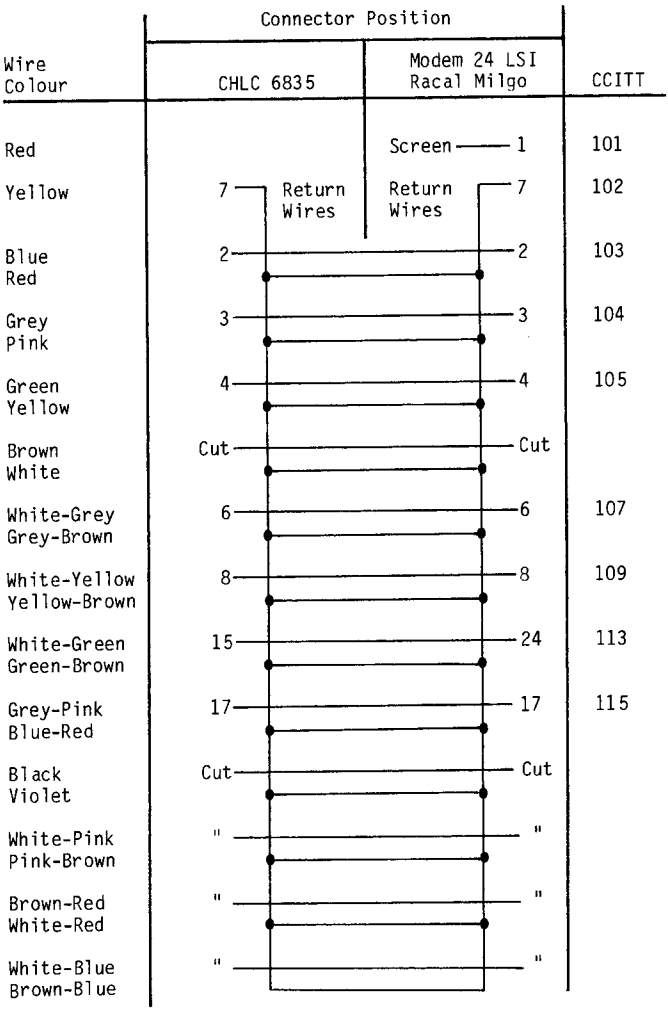
Note: Factory-made cables may have a different structure with cut return wires, a single-wire connection between the "7-pins" and a connection between screen and shell at the modem end. Even the wire colours may differ.

Cable for CHLC 6835 - Modem ITT GH 2052C-16 (6014-012)

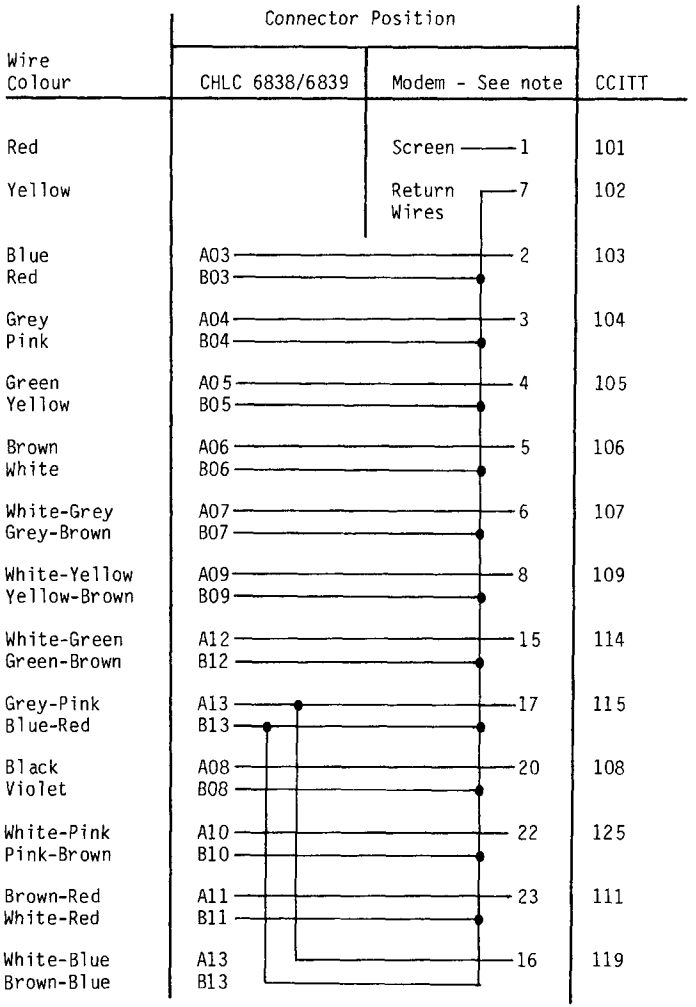


* Connected to pin 9 (+12V) in the modem connector.

Cable for CHLC 6835 - Modem 24 LSI Racal Milgo (6014-013)



Cable for CHLC 6838/6839 - Asynchronous/Synchronous Modem (6015-003)



Note: Cable fitted for 6838 and an asynchronous V23 modem not using CCITT 115, and for 6839 and a synchronous V23 modem not using CCITT 119. However, if the modem uses both signals, adjust modem or cable as follows:

- Adjust modem by removing; CCITT 115 in an asynchronous connection, CCITT 119 in a synchronous connection.
- Adjust cable by removing corresponding pins in the connector at the modem end (pin 17 or pin 16).

Cable for CHLC 6891 - X21/HDLC Interface (6016-002)

Wire Colour	Connector Position: CHLC 6891	Connector Position: X21/HDLC Interface	CCITT
	1 Screen	Screen 1	
Blue	2	2	
Red	9	9	
Grey	3	3	
Pink	10	10	
Green	4	4	
Yellow	11	11	
Brown	5	5	
White	12	12	
White-Grey	6	6	
Grey-Brown	13	13	
White-Yellow	7	7	
Yellow-Brown	14	14	
White-Green	15*	8	
Green-Brown	15*	15	
Grey-Pink	Cut	Cut	
Blue-Red	"	"	
Black	"	"	
Violet	"	"	
White-Pink	"	"	
Pink-Brown	"	"	
Brown-Red	"	"	
White-Red	"	"	
White-Blue	"	"	
Brown-Blue	"	"	

* Two wires in the same socket!

2.4 OTHER CABLING

2.4.1 Cables for Extension Units & Peripherals

The cables required for connecting extension units and peripherals to the computer are, with one exception, included as parts of the delivered units. The exception concerns cables for connecting a CTW to the computer; these cables are available as separate items:

- 5131 191 33300, for current loop interface (length 7.5 m)
- 5131 191 90100, for V24 interface (length 7.5 m)

The cables and mounting kits included in delivered units are specified in sections 1.1 and 1.2.

2.4.2 Mains Network

Figure 2.4-1

General Philosophy

The equipment in the PTS 6000 series is all designed to use standard domestic type power connections. Each mains-connected unit is supplied with a power cable having either a moulded on "Euro plug" (designed to fit the majority of European earthed power outlets) or an US (UL/CSA)-type of plug.

In installations where some different type of power outlet is used, which is not compatible with any of the standard plugs, an alternative EARTHED connector must be fitted by the installation personell to all pieces of equipment.

Mains Integrity

No special mains filtering is required as all equipment is protected against mains bourne interference.

No special "no break" or standby power sources are required since the equipment is fully protected against mains failure. As soon as power is resumed normal operation can recommence, no transaction data is ever lost. It is also possible to switch work stations off and on when required without effecting the system. Other equipment such as desk lamps, typewriters, cleaning equipment, etc. can be connected to the same mains network as the terminal system without fear of interference.

Power Requirements

Most mains-connected modules of the terminal system are adaptable to single phase AC supplies of 100-127V/60 Hz and 200-240V/50 Hz. Required voltage accuracy is ± 10% and required frequency accuracy is ± 2%. The maximum permitted harmonic distortion is 5%. Noise from the mains source should not exceed a transient amplitude of 1.2 kV with a rise time of 100 ns and a duration of 10 µs.

Power Outlets

Each terminal computer must be allocated an earthed outlet fed through a separate fuse, provided with a label marked 'Terminal Computer'. Close to this outlet, and on another fuse circuit, a further outlet should be provided, to enable connection of service equipment.

Consideration should always be given to service requirements and power outlet positions must be such that units can be moved for servicing without disconnecting the mains lead.

Each work station should have the required number of earthed power outlets within 1 m, including one spare for the connection of service equipment.

Any peripherals connected to the terminal computer should be provided with outlets in the same way.

Figure 2.4-1 shows an example of how the mains network for a terminal system might be layed out.

Earthing Requirements

The only requirement is that all power outlets used for the terminal system should be connected to the same safety earth.

Device per fuse

With the exception of the terminal computer, which must have a separate fused outlet, all other outlets can be connected to plain 10A slow-blow fuses in any configuration up to the maximum loading of each fuse, whilst allowing a 20% margin for connecting test equipment or maintenance aids.

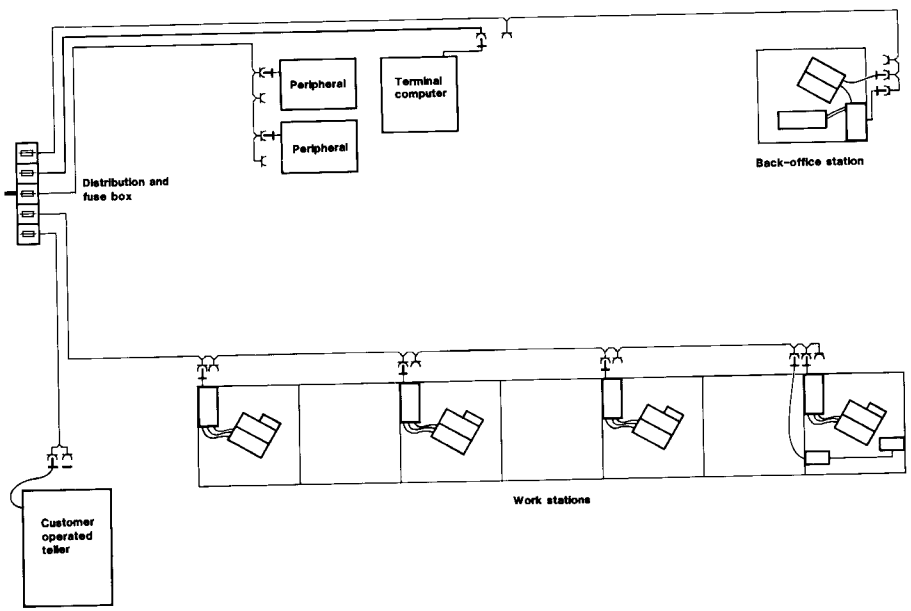


Figure 2.4-1 Example of the mains network for a terminal system. Note that each equipment position has a spare power outlet, and that the terminal computer has its own fuse - the service outlet being on another circuit.

2.5 INSTALLING COMPUTER & EXTENSION CABINETS

2.5.1 General

Unpacking Figure 2.5-1

When being delivered the cabinets are packed as illustrated in Figure 2.5-1. For unpacking; remove top lid and lift off the cardboard that encloses the cabinet. The cabinet is then carefully lifted off the pallet and placed on the floor.

CAUTION

NEVER TRY TO TILT AND TURN THE CABINET TO GET IT DOWN FROM THE PLINTH, MAN MAY BE HURT OR EQUIPMENT DAMAGED! ALWAYS USE A SLING AND A PARTNER FOR LIFTING DOWN THE CABINET.

If an installed cabinet for some reason must be transported any longer distances, it should again be packed in the same manner.

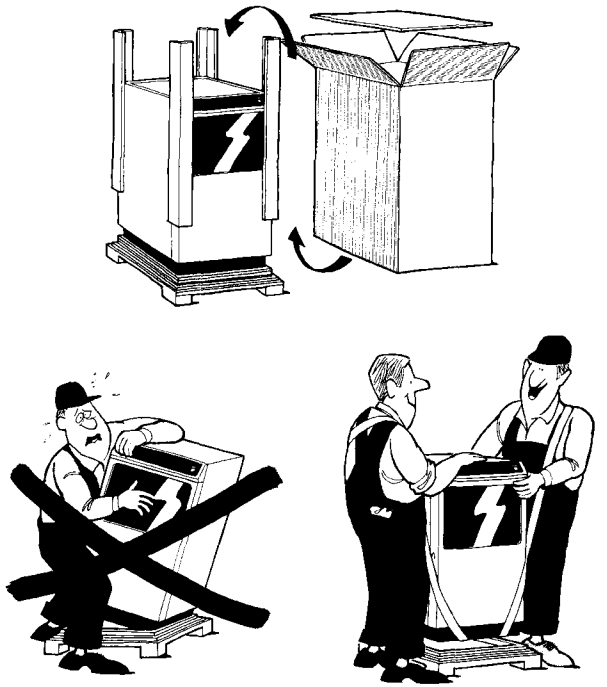


Figure 2.5-1 Unpacking Cabinets

Locating Cabinets Figure 2.5-2

Place the cabinet at the location settled beforehand, fixed by the routing selected for external cables. Ensure that a free area according to Figure 2.5-2 is available around the cabinet for servicing purposes. Pay also attention to any shelves etc. above the cabinet. a free space of 100 mm must be left above the cabinet. The same space must also be left behind the cabinet. However, the later type of cabinet (with air inlet via the rear cover) can be placed close to a wall, but must then have free access to air from the sides.

Now place the cabinet in service position, i.e. pulled out from the wall to get access to the rear.

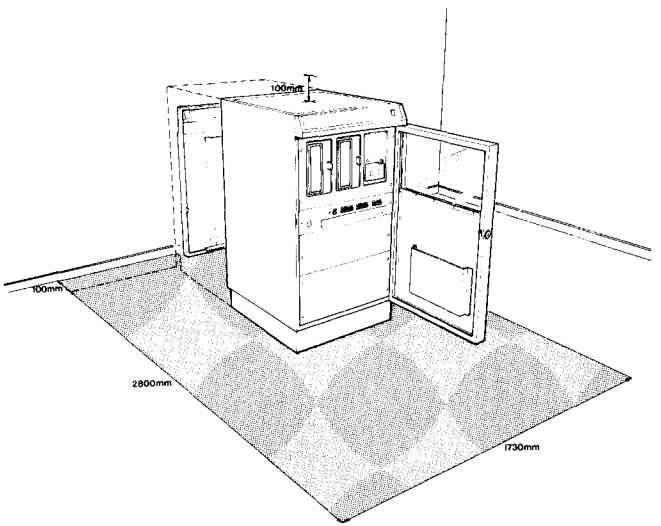
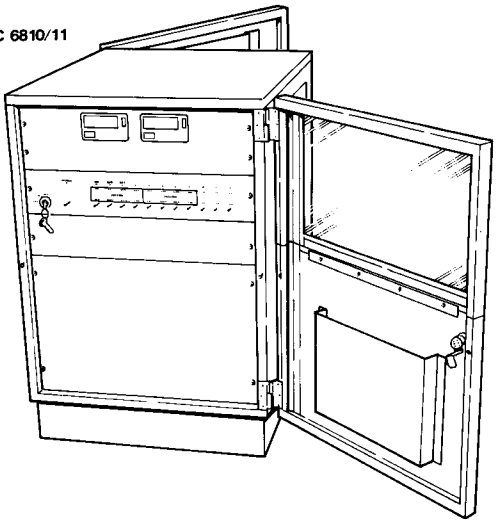


Figure 2.5-2 Locating Cabinets

Removing Covers Figure 2.5-3

TC 6810/11 and EXU 6863 have hinged doors both at the front and at the rear. Other cabinets have such a door only at the front. The rear cover is here of a type that can be lifted off, held in position by a mechanism that is released from the front, underneath the centre section of the "nose". These cabinets have also a removable top cover, released by pulling down two snap locks from inside at the rear edge (Figure 2.5-3).

TC 6810/11



TC 6812/13/14/24

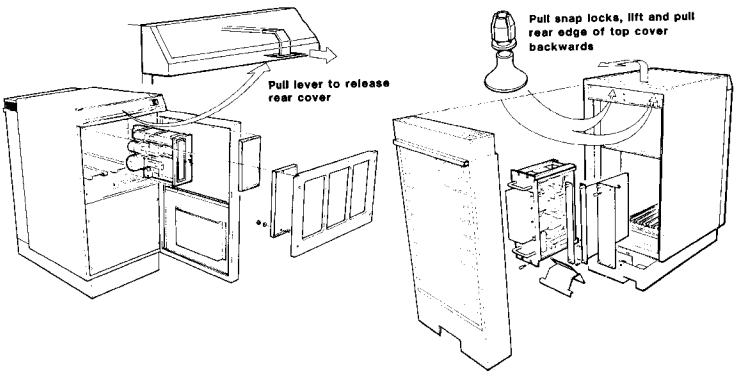


Figure 2.5-3 Cabinet Covers

2.5.2 Checking Submodules & Interconnections

General

The submodules of a computer system are usually fitted in the cabinets when these are delivered, but can under certain circumstances be delivered as separate items. Whether fitted or not, all submodules should be checked according to the following before the system is completed and started.

Rack Disposals

Figure 2.5-4/5

The basic units of the different computer configuration are located in the rack as shown in the Figures 2.5-4/5 (rear views). Undefined rack positions are freely disposed. However, master units and memory should, if possible, be located in TC cabinets (absolutely necessary in TC 6810/11 systems) and should be arranged in such a way that the OKI/OKO-wiring can be made in a sequential way from left to right on the backpanel, sub-section 2.5.4).

In EXU 6864 there are no rack positions allocated to certain units, however, note that the positions 1-2 are closer to each other than remaining positions, and cannot be used for units with fixed front panels.

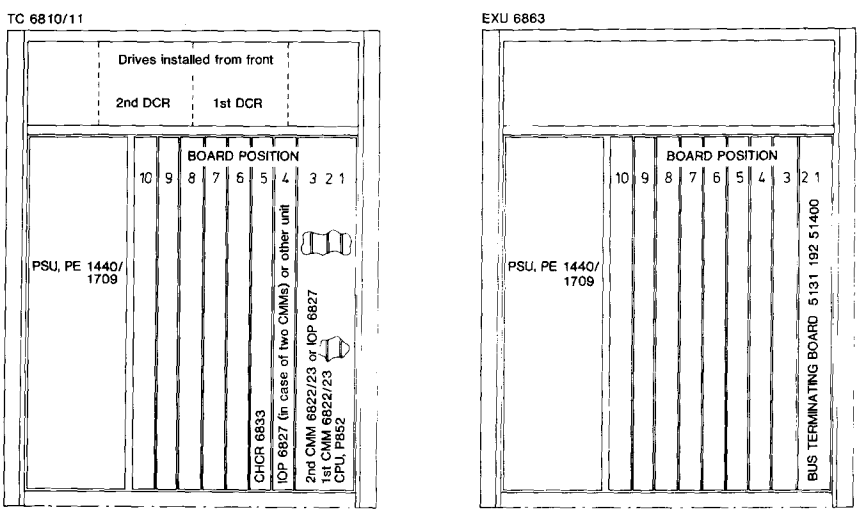


Figure 2.5-4 Rack Disposals in TC 6810/11 & EXU 6863

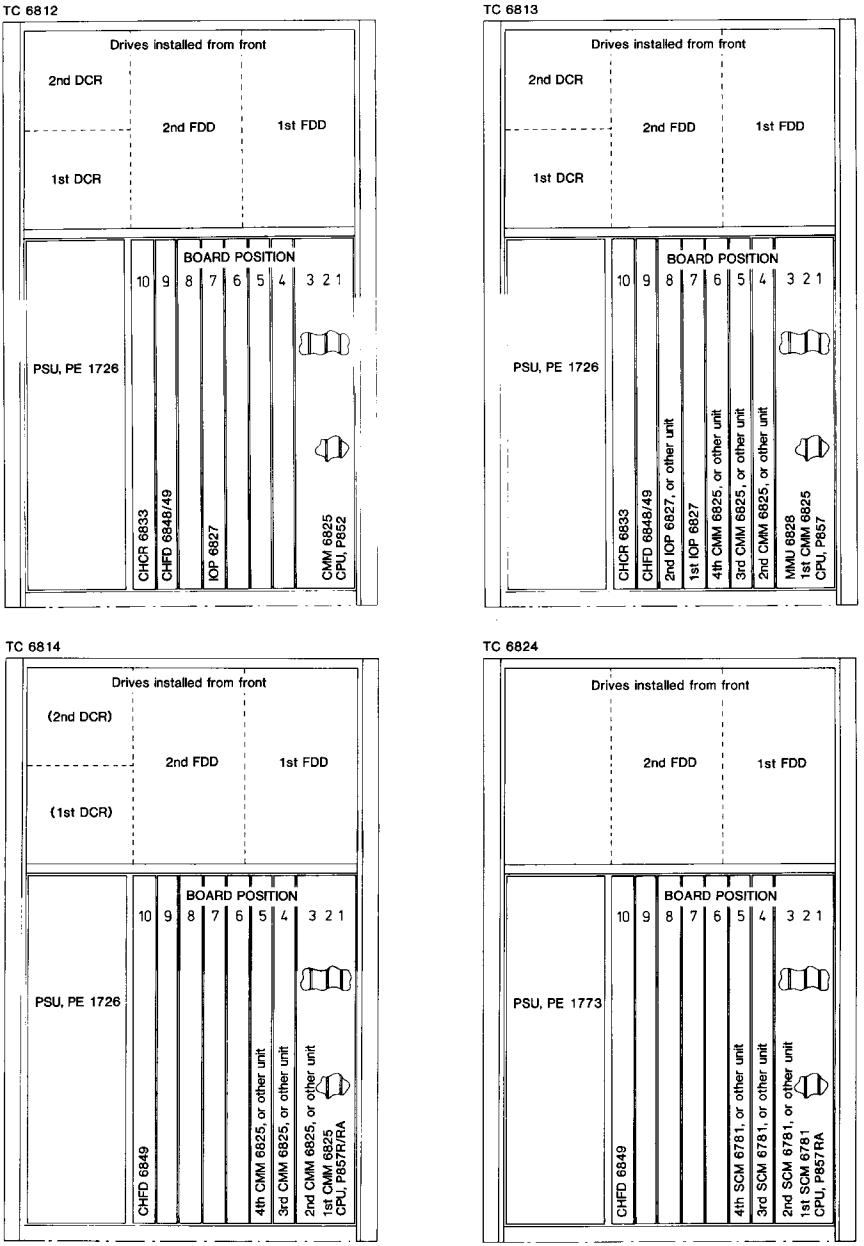


Figure 2.5-5 Rack Disposals in TC 6812/13/14 & TC 6824

Mains Voltage Adaptations

Ensure that the PSU of each cabinet is labelled for the mains source being at hand, and that any range and voltage selectors are set in correct positions:

- PE 1440, no selectors, just for 220V/50Hz
- PE 1709-01, voltage selector
- PE 1709-02, no selectors, just for 120V/60Hz
- PE 1726, range and voltage selectors
- PE 1773, range and voltage selectors

For detailed information, see chapter 7.

Mains Frequency Adaptations

The cabinets used for TC 6812/13, and early models of TC 6814 and EXU 6864, have a fan unit that is centered under the rack, and that requires different A.C. supply at different mains frequencies. Ensure that the fan motor is supplied with 140V at 50Hz and 180V at 60Hz. The selection is made on BU11 in the PSU PE 1726/02, see chapter 7. (A PSU of type PE 1726/01 may have been modified and has then a similar selection facility.)

Ensure that any flexible disc drives are labelled for the correct mains frequency. If necessary to convert from 50Hz to 60Hz (or vice versa), see chapter 12.

U-Link and Switch Settings

Most submodules of the computer system are equipped with U-links and/or switches, used for adapting certain performance characteristics to the requirements. You should ensure that links and switches are correctly positioned on:

- Board units plugged into the rack.
- Flexible disc drives.
- Rack Backpanels

All links and switches are specified in the relevant submodule chapter, from chapter 6 and onwards.

Interconnections & Special Items

Ensure that power- and signal cables are correctly fitted according to chapter 6. Also ensure that correct terminations are fitted in extended systems (sub-section 2.5.6) and that a bleeder resistor is connected to the +24V supply from power supply units in EXUs.

2.5.3 Installing Separately Delivered Submodules

General

Any submodules that have been separately delivered (and checked according to

subsection 2.5.2) are plugged into the appropriate rack positions, considering the allocations of certain rack positions for specific submodules (Figure 2.5-4/5). Any interconnection cables required are then fitted according to chapter 6 (Module Interconnections and Power Distribution).

Power Supply Unit & Battery Module

The PSU is fixed to the rack with four screws, two at the top and two at the bottom of its front panel. Then connect the A.C. input cable (with plug separated from source) and, CAREFULLY, the A.C./D.C. supply cables. Consult the relevant Power Distribution diagram in chapter 6, and the relevant PSU assembly in chapter 7.

The battery modules of a TC 6824, each including two 12V batteries, are fully charged at the time when they are leaving the factory and should be kept separately until the time for delivery to the customer. Before installation the batteries should be checked and if needed also charged (see chapter 7).

When installing the batteries, the red cable from the P10 connector is fixed on the positive pole of one battery, while the blue cable is fixed on the negative pole of the other battery. The loose white cable supplied is used to connect the remaining two poles, completing a series connection (see chapter 7).

The batteries are held in place by two pressure plates. A foam-rubber pad is placed between battery and plate. The plates fit into slots on one side of the battery box, while screws are used to fix the plates to the other side. Note that there are two possible positions for the pressure plates, allowing for different battery dimensions.

The battery box itself is fixed by screws to the front panel.

Board Units Plugged Into Rack

Board units that have an attached front panel are fixed to the rack with the top and bottom screws. Other boards must be covered with loose panels, fixed to the rack in the same way.

DCR Drives Figure 2.5-6

DCR drives are held in position by the panels fitted in front of them, screwed to the rack. When fitting just one DCR, it should be placed to the left in TC 6810/11 and in the lower position in TC 6812/13. The unused position is then covered with a blind panel. NOTE: An unused position for DCR 6861 (in TC 6810/11) should also be fitted with a dummy board; 5131 191 36300.

FDDs are secured by screws on top of rack (available when top cover has been removed) and the front panel screwed to the frame of the rack. When fitting just one FDD, it should be placed to the left with the righthand position covered by a blind panel (opposite to figure 2.5-6!).

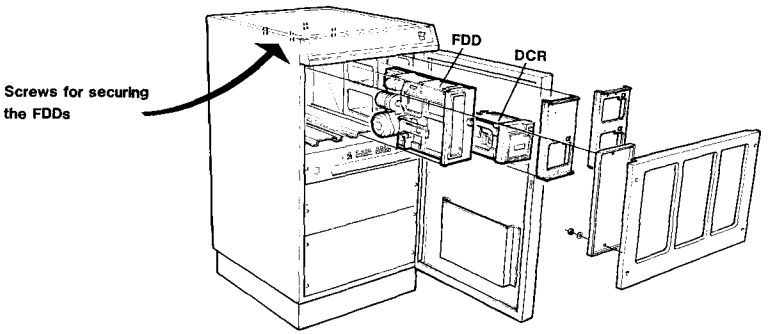


Figure 2.5-6 Installing DCRs & FDDs

Note that racks of later production date are equipped with FDD rails that can be adapted either to FDD 6867 (250 Kbytes), or to FDD 6791 (1 Mbyte). It's just a matter of turning the bottom stop block, and moving the top bracket to desired positions (Figure 2.5-7).

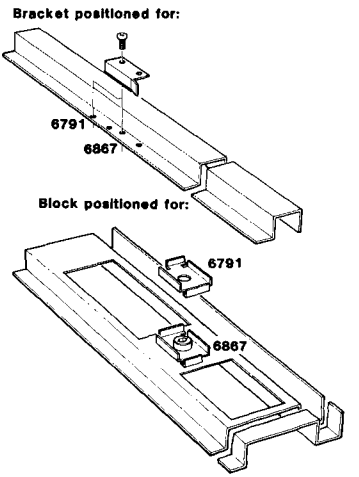


Figure 2.5-7 Adapting Rack to FDD 6867/6791

2.5.4 Additional Backpanel Wiring

Master Priority Chain

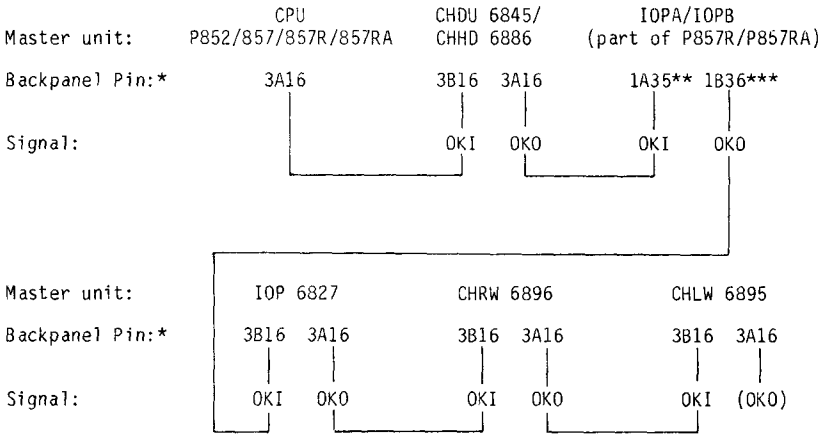
Computer sub-modules that are classified as masters, i.e. that are able to request the bus for direct access to the memory, must be arranged in a priority chain. This chain is basically defined as follows:

1st priority: CHDU 6845 or CHHD 6886
2nd " : IOPA/IOPB (portion of CPU P857R/857RA)
3rd " : IOP 6827
4th " : CHRW 6896
5th " : CHLW 6895
6th " : CPU P852, P857 or P857R/857RA

In systems where one or more of these masters are missing, the priority chain is condensed by linking together the remaining masters with their relative priorities maintained. Should a system be equipped with more than one master unit of the same type, the additional units are linked in "below" the first one of that type.

The priority chain is established by adding backpanel wires, on earlier backpanels by means of insulated 1/4 mm wires with wrapped connections. Later versions of backpanels have special "Master Priority Posts" that enable a faster and easier way of chaining; the interconnections are now made by means of ordinary U-links or (when longer distances) by socketed wire links, see chapter 6.

ENSURE THAT APPLICABLE UNITS ARE LINKED
INTO THE PRIORITY SYSTEM AS SHOWN BELOW
(FOR TC-EXU LINKS, SEE SUB-SECTION 2.5.6)



* For physical pin locations see chapter 6!
** Also available on post OKIA on Backpanel 1B
*** Also available on post OKOB on Backpanel 1B

Table 2.5.1, continued

Computer Interface Unit	Hexadec Address Code	Dec Break Level	Break Output Pin	Break Input Pin 6827 1:=1st* 2:=2nd*	Break Input Pin P857R(A) A=IOPA B=IOPB	Decimal Interrupt Level	Note
CHDU 6845	17	---------- Master Unit ----------				48	1st disc
	37					48	2nd disc
CHCD 6847	0D	--	--	--	--	35	Card Reader
	0F	15	3A43	2:4B06	B:1A26	34	Line Printer
CHFD 6848	09	09	3A43***	2:4B12	B:1A20	30	1st disc
	19						2nd disc
	(29	---------- Not supported with liability ----------					3rd disc)
	(39	---------- Not supported with liability ----------					4th disc)
CHFD 6849	09	09	3A43	2:4B12	B:1A20	30	1st disc
	19						2nd disc
	(29	---------- Not supported with liability ----------					3rd disc)
	(39	---------- Not supported with liability ----------					4th disc)
	2E	--	--	--	--	09	SDP Control
CHHD 6886	17	---------- Master Unit ----------				48	1st HDU
	37					48	2nd HDU
CHLC 6891	0A	--	--	--	--	12	Receiver
	0B	--	--	--	--	13	Transmitter
CHLW 6895	06	---------- Master Unit ----------				26	1st CHLW
	07	---------- Master Unit ----------				27	2nd CHLW
	26	---------- Master Unit ----------				24	3rd CHLW
	27	---------- Master Unit ----------				25	4th CHLW
CHRW 6896	3A	---------- Master Unit ----------				18	1st CHRW
	3B	---------- Master Unit ----------				19	2nd CHRW
	2A	---------- Master Unit ----------				20	3rd CHRW
	2B	---------- Master Unit ----------				21	4th CHRW

* See previous definition
** Addresses within parentheses are used when operating on IOP channels
*** Operation on IOP channel should be avoided

Table 2.5.2 Bus Addresses, Break & Interrupt Levels defined for concentrator applications

Computer Interface Unit	Hexadec Address Code	Dec Break Level	Break Output Pin	Break Input Pin 6827 1:=1st* 2:=2nd*	Break Input Pin P857R(A) A:=IOPA B:=IOPB	Decimal Interrupt Level	Note
CHLT 6831	03	--	--	--	--	24	1st CHLT
	13	--	--	--	--	25	2nd CHLT
CHRT 6832	01	--	--	--	--	16	1st CHRT
	11	--	--	--	--	17	2nd CHRT
CHCR 6833	0E	14	3A43	2:4B07	B:1A25	08	DCR Control
	2E	--	--	--	--	09	SDP Control
CHMT 6842	0C	12	3A43	2:4B09	B:1A23	44	IOP mandatory
CHDU 6844	08	08	3A43	2:4B13	B:1A19	40	1st disc
	18						2nd disc
	28						3rd disc
	38						4th disc
CHCD 6847	0F	15	3A43	2:4B06	B:1A26	34	Line Printer
CHFD 6848	09	09	3A43**	2:4B12	B:1A20	30	1st disc
	19						2nd disc
	(29	---------- Not supported with liability ----------					3rd disc)
	(39	---------- Not supported with liability ----------					4th disc)
CHFD 6849	09	09	3A43	2:4B12	B:1A20	30	1st disc
	19						2nd disc
	(29	---------- Not supported with liability ----------					3rd disc)
	(39	---------- Not supported with liability ----------					4th disc)
CHLC No. 1	02	--	--	--	--	12	Receiver
	12	--	--	--	--	13	Transmitter
CHLC No. 2	22	--	--	--	--	14	Receiver
	32	--	--	--	--	15	Transmitter
CHLC No. 3	04	--	--	--	--	10	Receiver
	14	--	--	--	--	11	Transmitter
CHLC No. 4	05	--	--	--	--	18	Receiver
	15	--	--	--	--	19	Transmitter
CHLC No. 5	06	--	--	--	--	20	Receiver
	16	--	--	--	--	21	Transmitter
CHLC No. 6	07	--	--	-	--	22	Receiver
	17	--	--	--	--	23	Transmitter
CHLC No. 7	20	--	--	--	--	26	Receiver
	30	--	--	--	--	27	Transmitter
CHLC No. 8	21	--	--	--	--	28	Receiver
	31	--	--	--	--	29	Transmitter
CHLC No. 9	23	--	--	--	--	32	Receiver
	33	--	--	--	--	33	Transmitter
CHLC No.10	24	--	--	--	--	36	Receiver
	34	--	--	--	--	37	Transmitter
CHLC No.11	25	--	--	--	--	38	Receiver
	35	--	--	--	--	39	Transmitter
CHLC No.12	26	--	--	--	--	42	Receiver
	36	--	--	--	--	43	Transmitter
CHLC No.13	27	--	--	--	--	46	Receiver
	37	--	--	--	--	47	Transmitter
CHLC No.13	0A	10	***	2:4B11	B:1A21	46	Receiver
TRUNK	0B	11	***	2:4B10	B:1A22	47	Transmitter

* See previous definition
** Operation on IOP channel should be avoided
*** See applicable CHLC in Table 2.5-1

Memory Address Lines (TC 6824) Figure 2.5-8

When using a memory capacity that exceeds 256 kByte in TC 6824, it is necessary to extend the memory address lines to the memory module(s), AND TO ALL MASTER UNITS! This is done by adding U-links on backpanel 1A as shown in Figure 2.5-8. With a maximum memory capacity of 0.5 MByte it is sufficient to link MAD 256; with even bigger memory (max. 1 MByte), it is necessary to link both MAD lines.

> CAUTION!
> When using a master with less address range than provided memory, disable excessive memory range by grounding applicable address input(s) in memory positions (A42 for a master range of 0.5 MByte, A42 and A43 for 256 kByte).

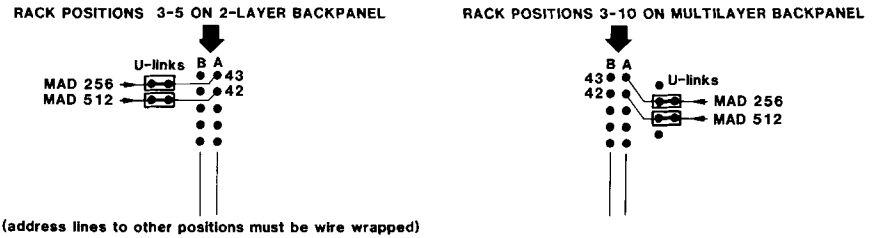


Figure 2.5-8 Extending Memory Address Lines in TC 6824

2.5.5 Optional Control Facilities

Power Control in TC 6812/13/14 Figure 2.5-9

The A.C. supply to the FDDs can be switched on/off by applying +5V/0V to wire wrap post FDD (S1N) on backpanel 1A, see Figure 2.5-9.

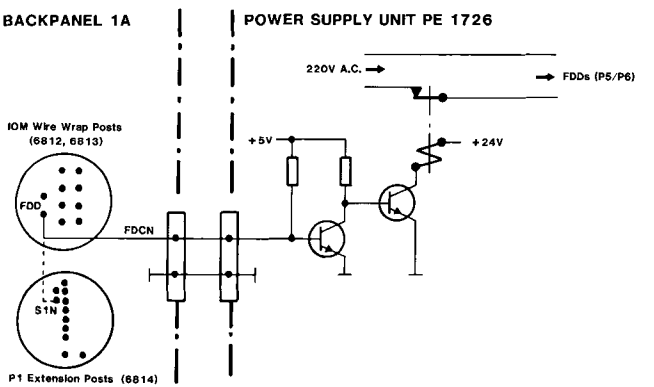


Figure 2.5-9 Controlling A.C. Supply to FDDs in TC 6812/13/14

Power Control in TC 6824 Figure 2.5-10

TC 6824 provides a possibility to connect a remote ON/STAND BY switch for controlling the computer´s A.C. and D.C. supply. The remote switch is connected to the free fast-on pins at the rear of the SOP, and is enabled when the SOP´s rotary switch is set in position REMOTE. When enabled the remote switch operates in the same manner as the local ON/STAND BY switch (this one enabled when the rotary switch is set in position ON LOCK). An enabled switch in ON state means full A.C. and D.C. supply from the PSU, whilst the STAND BY state means that the PSU is only supporting the memories with maintained charging of batteries.

The A.C. supply to the FDDs can be switched on/off by applying +5V/0V to extension post SON on backpanel 1A. The optional A.C. supply via P8/P9 can be controlled in the same manner via extension post S1N.

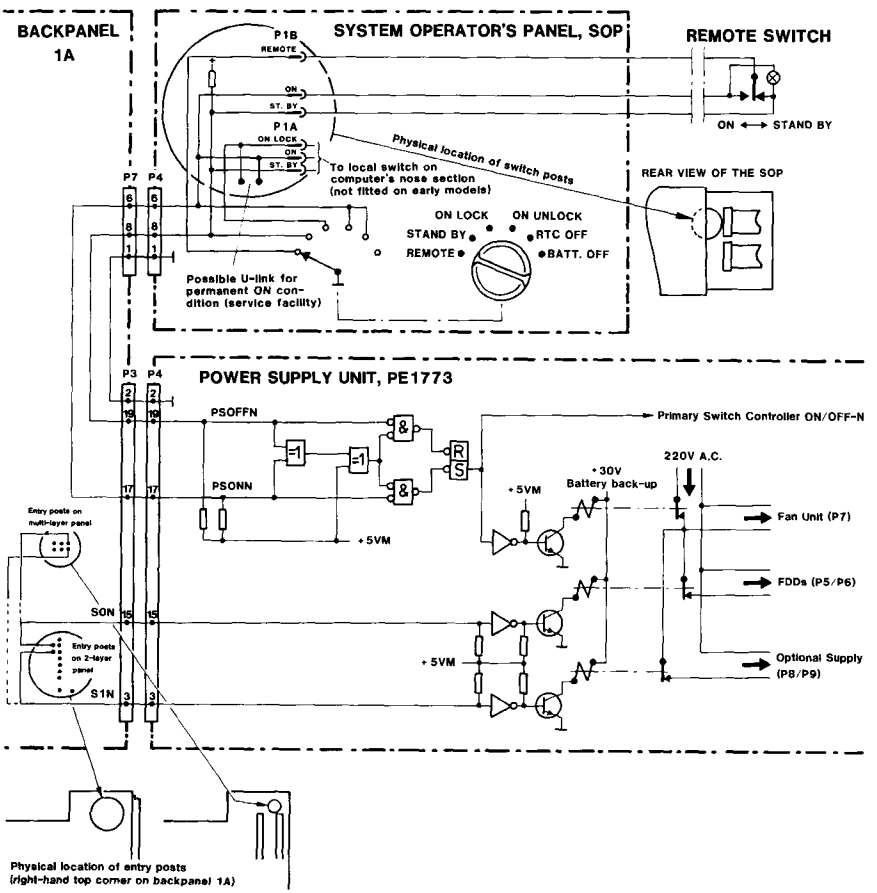


Figure 2.5-10 Optional Power Control in TC 6824

Software Command Exits, TC (6812, 6813) & 6814, 6824 Figure 2.5-11

The control unit integrated in the SOP assembly (CUSOP) provides four control lines that are under software command. These lines can be used for controlling the A.C. supply to FDDs and any optional devices connected to P^{o}/P^{o} on the PSU, see previous pages.

The four lines, software controlled via BIO 00-03 on the ordinary SOP address (usually 2E in hexcode), terminate at the P1 Extension Posts on backpanel 1A. The line sources are all of open-collector-type. which means that the posts can still be used for break extensions etc. if no software commands are used.

Note that the control path represented by BIO 00 is permanently available (intended for FDD control), but remaining control paths must be enabled by a U-link on the CUSOP.

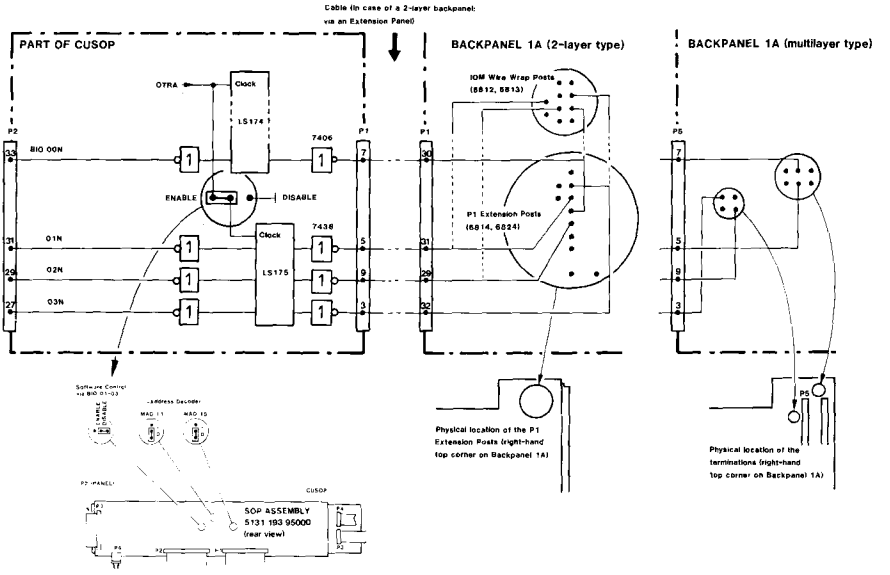


Figure 2.5-11 Software Command Exits in TC (6812, 6813) & 6814, 6824

2.5.6 Connecting External Cables

External Interfaces

Basically there are three types of external interfaces in TC and EXU cabinets:

- Some rack-located board units are using the rear edge connectors (P1,P2/P4, P5) as interfaces. These connectors are facing the backplane of the rack (front of cabinets) and require that necessary sockets are mounted to the backplane.
- Other rack-located board units have the necessary interface connectors fitted on their vertical front plates (facing the rear of the cabinets).
- Extension cables between TC and EXU cabinets are using interface connectors on the rack backpanels (front of cabinets).

Basic Routing Figure 2.5-12

External cables to the rack backplane area (front of cabinet) are routed under the cabinet (in later type of cabinets; through two 'tunnels' along the sides). These cables are entered into the cabinet by removing small bottom plates in front of the rack backplane, below the rack positions where the cables are to be connected. A removed plate is then replaced by another plate, supplied as a part of an entry kit together with the cable. This new plate is (together with other details of the kit) used for grounding the cable screen and securing the cable to the cabinet. Different types of entry kits are described below, under 'Installing Backplane Cables'.

Other cables, to front plate connectors on rack-located board units, are entered into the cabinet through the lower part of the rear cover. In earlier cabinets it's just a slot in the bottom edge of the covers. However, in the later type of cabinet the rear cover is more than just a cover; it controls the air flow into and out of the cabinet and stands over the fan unit in the extended base section. The cables are now routed on a removable bridge over the fan unit, and through a matching tunnel in the cover. Note the U-shaped metal clip that holds the cables in correct position when the cover is lifted onto the base section.

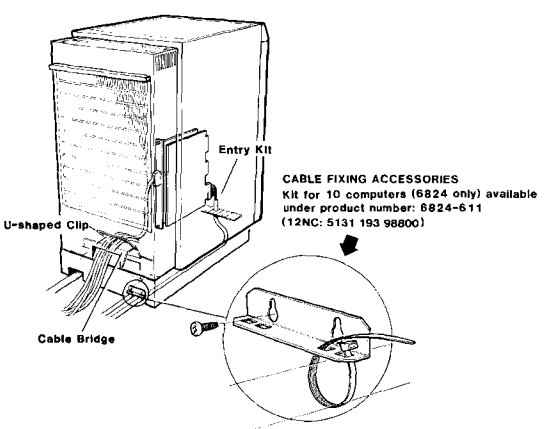


Figure 2.5-12 Basic Routing of External Cables

Basic Installation of Backplane Cables Figures 2.5-13/14

All external cables for backplane installations are delivered with fitted sockets and the necessary entry kits. The sockets are (except for extension cables) basically fixed to the backplane as shown in Figure 2.5-13:

- Screw the supplied studs into top and bottom hole at the appropriate backplane slot. When supplied; fit also the springs shown in figure.
- Thread socket onto the studs, apply supplied washers and lock the socket with the circlips.

Sockets installed in this way will have a small play to match the tolerances of the board edge connectors that are to plug into the sockets. A basic entry kit for grounding screen and securing cable to the cabinet is shown in Figure 2.5-14.

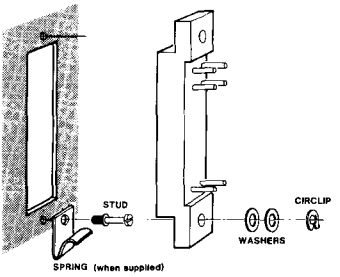


Figure 2.5-13 Basic Installation of Backplane Socket

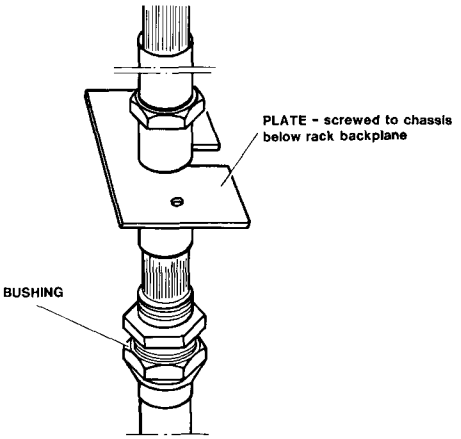


Figure 2.5-14 Basic Entry Kit for Backplane Cables

Extension Cables with Break Lines Figures 2.5-15/16/17

The sockets fitted on bus extension cables are not fixed to the backplane, but connected to appropriate plugs. In TC 6810/11 and EXU 6863 these plugs are located behind the righthand edge of backpanel 1A (Figure 2.5-15). Each specific break line wire wrap post is interconnected with corresponding post in the other cabinet. A break line that originates in the EXU must be wired to one of the EXU posts, and is then picked up from corresponding post in the TC.

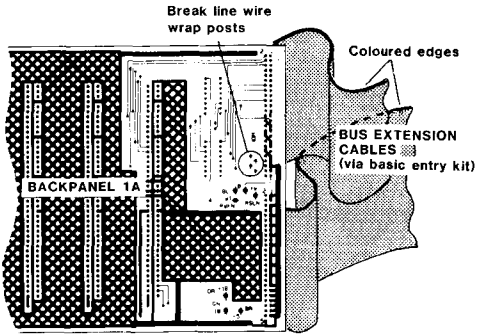


Figure 2.5-15 Connection of Extension Cables in TC 6810/11 & EXU 6863 Cabinets

In other cabinets the extension cables are either connected to an extension panel that is plugged into the edge connectors of backpanel 1A (2-layer type of backpanel), or direct to plugs on backpanel 1A (multilayer type) - see Figure 2.5-16.

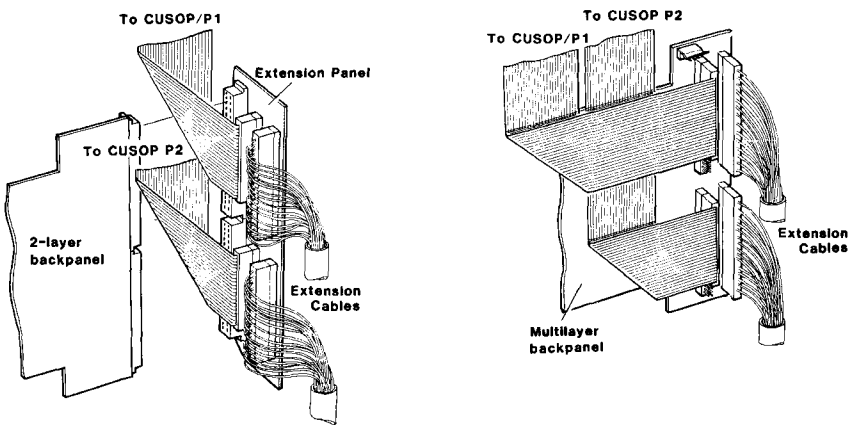


Figure 2.5-16 Connection of Extension Cables in TC 6812/13/14/24 & EXU 6864

Extending Master Bus Signals Figures 2.5-17/18/19

It is now possible to run masters in the first EXU of an extended system, provided that there are no masters with lower priority in the TC (OKO/OKI line not returned from EXU to TC). This requires that some extra master bus signals are linked over to the first EXU cabinet. When using TC and EXU cabinets that are equipped with the new multilayer backpanel (1A), this linking is easily arranged by means of ordinary U-links, see Figures 2.5-17/18. A detailed scheme of the link arrays is shown in Figure 2.5-19.

It should be noted that these master links occupy so many wires that there are just two left for carrying Break signals from the EXUs!

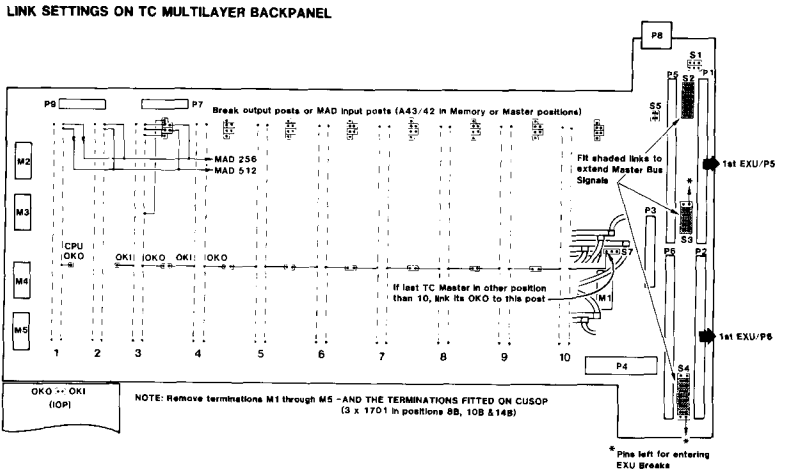


Figure 2.5-17 Master Linking on TC Multilayer Backpanel

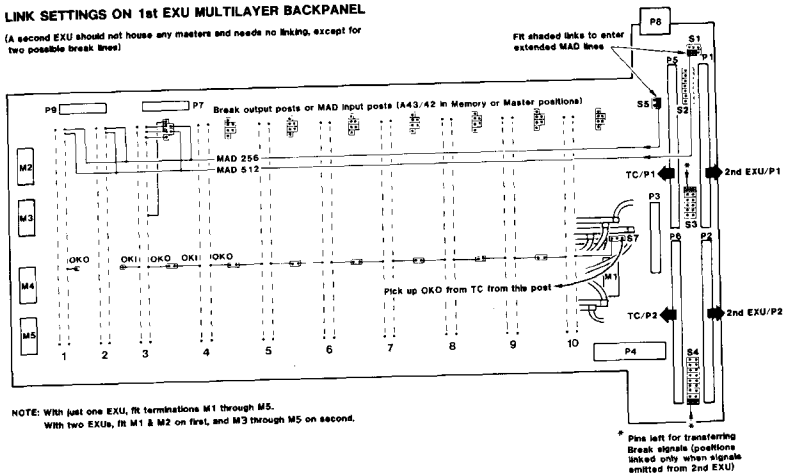


Figure 2.5-18 Master Linking on EXU 1 Multilayer Backpanel

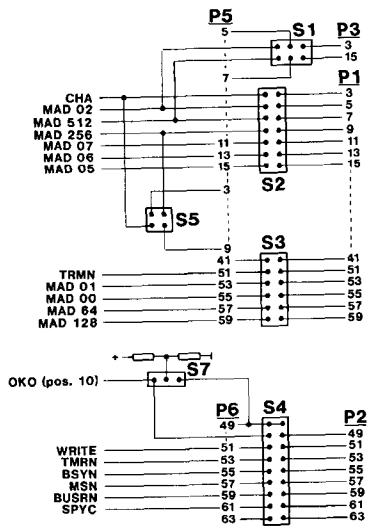


Figure 2.5-19 Multilayer Link Array for Master Bus Signals

In TC and EXU cabinets where one or more racks are equipped with the former 2-layer backpanel, it is still possible to arrange a corresponding master linking. This is now established by using the 2-layer panels' Wire Wrap/Extension posts, earlier used for Break linking. However, in this case there are some restrictions that should be noted:

- TC 6810/11 and EXU 6863 are always excluded from this facility.
- A master EXU cannot be followed by a slave EXU unless both are equipped with multilayer backpanels.
- When memory capacity exceeds 0.5 Mbyte, there is no line left for carrying Break signals from EXU to TC (last line required for MAD 512).

Taking all these restrictions into account, the master signals are routed as follows on 2-layer backpanels (shown routing matches 2-layer panels with multilayer panels):

Signal name	Bus connection, slot-pin	Routed via post*	Notes
CHA	10-3A27	IOM/P1 - 32	
MAD 02	10-3B39	" - 31	
(MAD 512	1-3A42)**	" - 30	
(MAD 256	1-3A43)**	" - 29	Upper
MAD 07	10-3B34	" - 28	Post
MAD 06	10-3B35	" - 27	Array
MAD 05	10-3B36	" - 26	
MAD 01	10-3B40	" - 5	
MAD 00	10-3B41	" - 4	
OKO/OKI (TC to EXU)	X-3A16/3B16	IOB/P2 - 7	
WRITE	10-3A26	" - 6	
TMRN	10-3A29	" - 5	
BSYN	10-3A38	" - 4	Lower
MSN	10-3A37	" - 3	Post
BUSRN	10-3A36	" - 2	Array
SPYC	10-3A35	" - 1	
MAD 128	10-3B43	IOM/P1 - 2	
MAD 64	10-3B42	" - 3	

* For physical positions, see chapter 6!
** When necessary, otherwise available for Break signals from EXU to TC.

Bus Signal Terminations Figure 2.5-20

Figure 2.5-20 shows how to terminate the bus signals in different configurations of TC and EXU cabinets (6810/11 & 6863 excluded). M1 through M5 are the terminator positions on rack backpanel 1A. Please note that CUSOP is also provided with termination facilities (fitted only in case of a single TC). All terminators used are of type 1701.

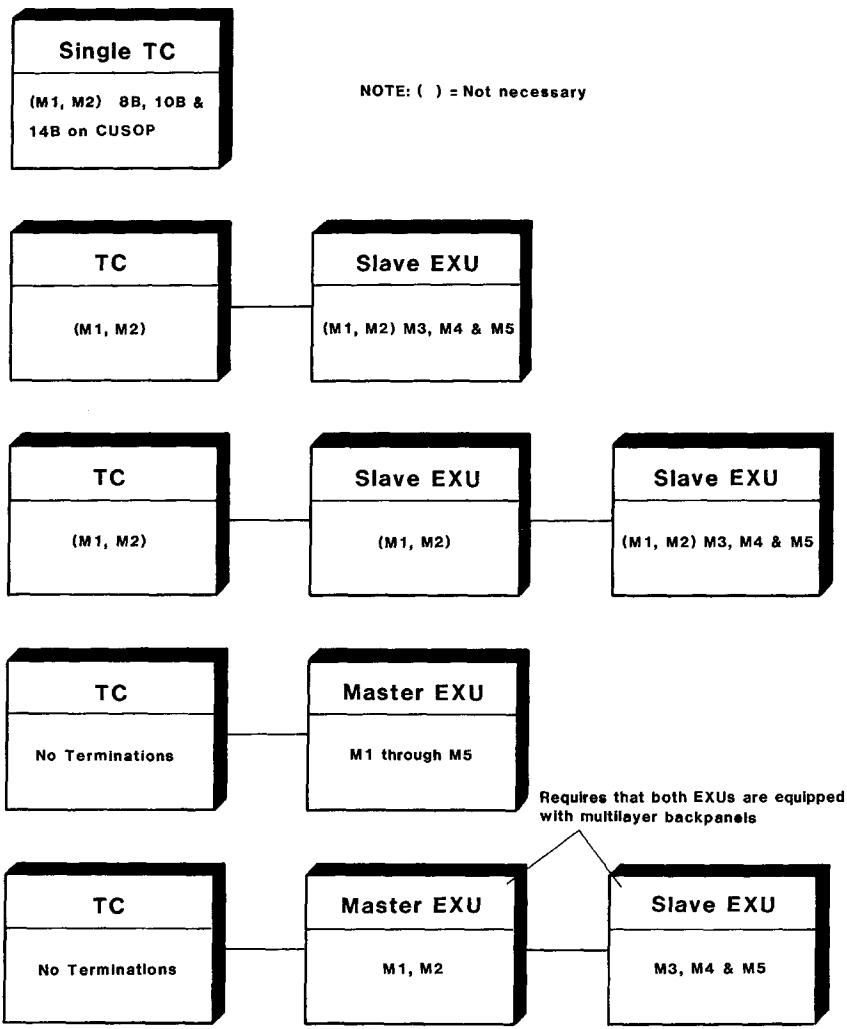


Figure 2.5-20 Bus Signal Terminations

2.5.7 CONNECTOR DETAILS FOR PRINTED CIRCUIT BOARDS

The boards are indentified by the connector layout as shown in Figure:

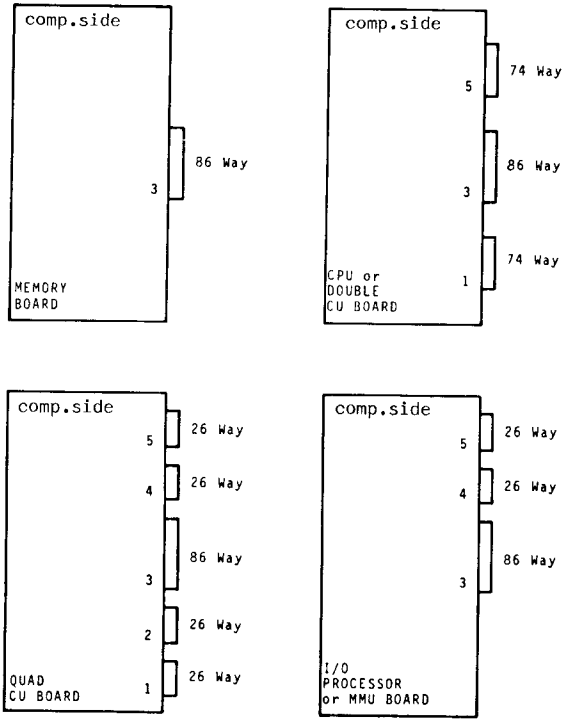
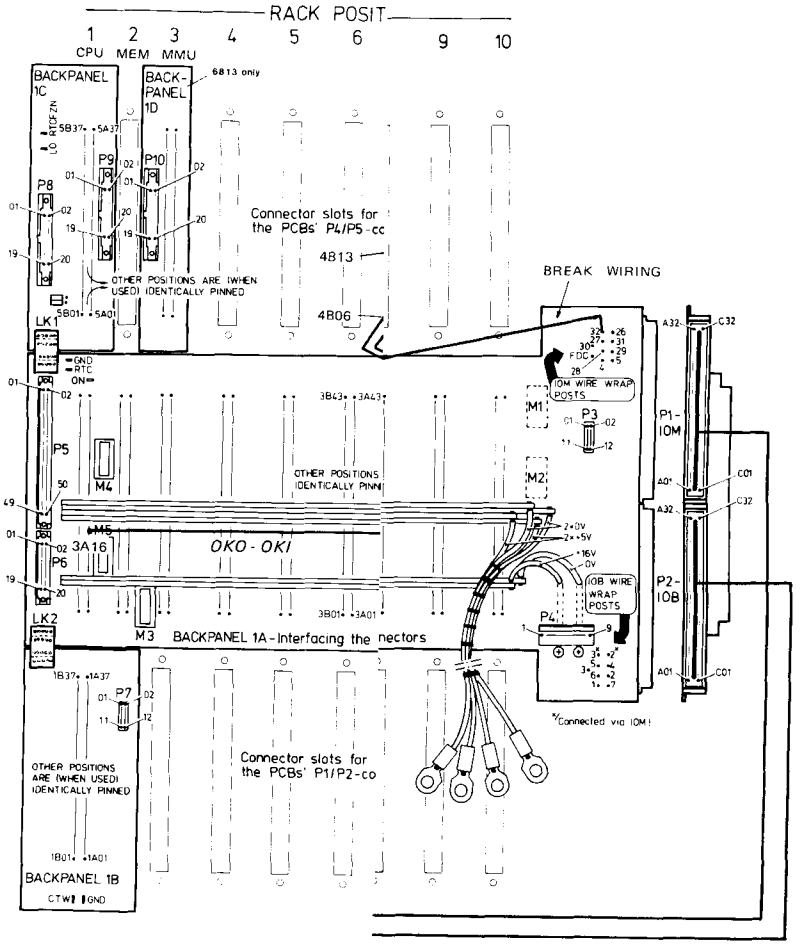


Figure 2.5.21 PRINTED WIRING BOARD-CONNECTOR LAYOUT



ECTION EXTENSION UNIT AND BREAK WIRING

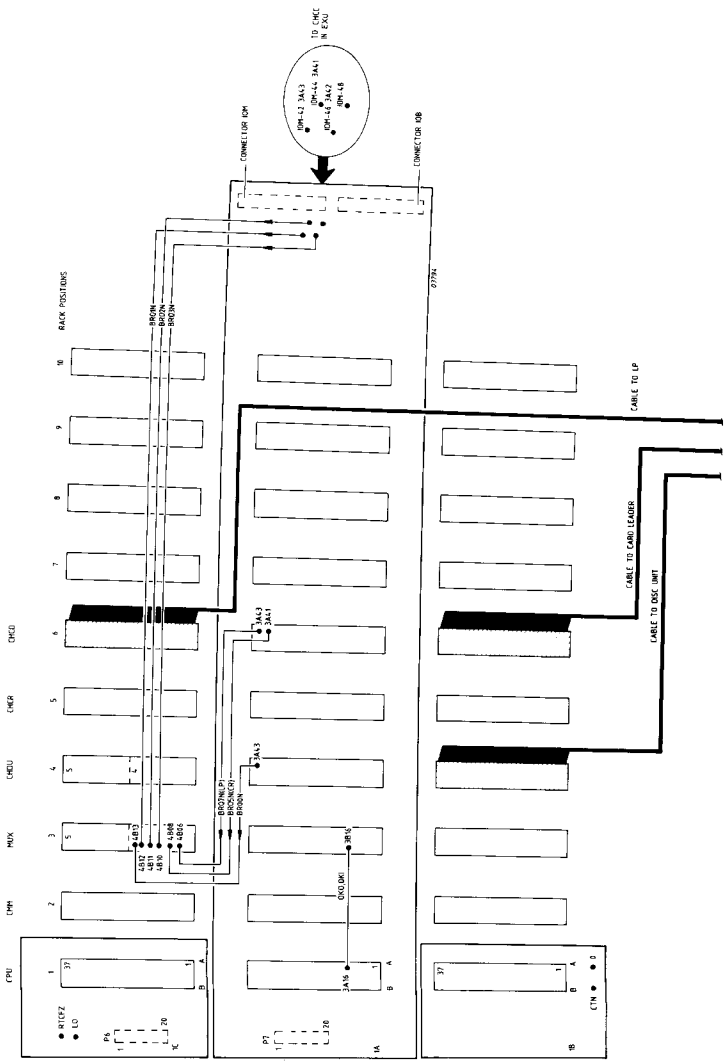


Figure 2.5.23 EXAMPLE BREAKWIRING 6810

TC 6814, 6824

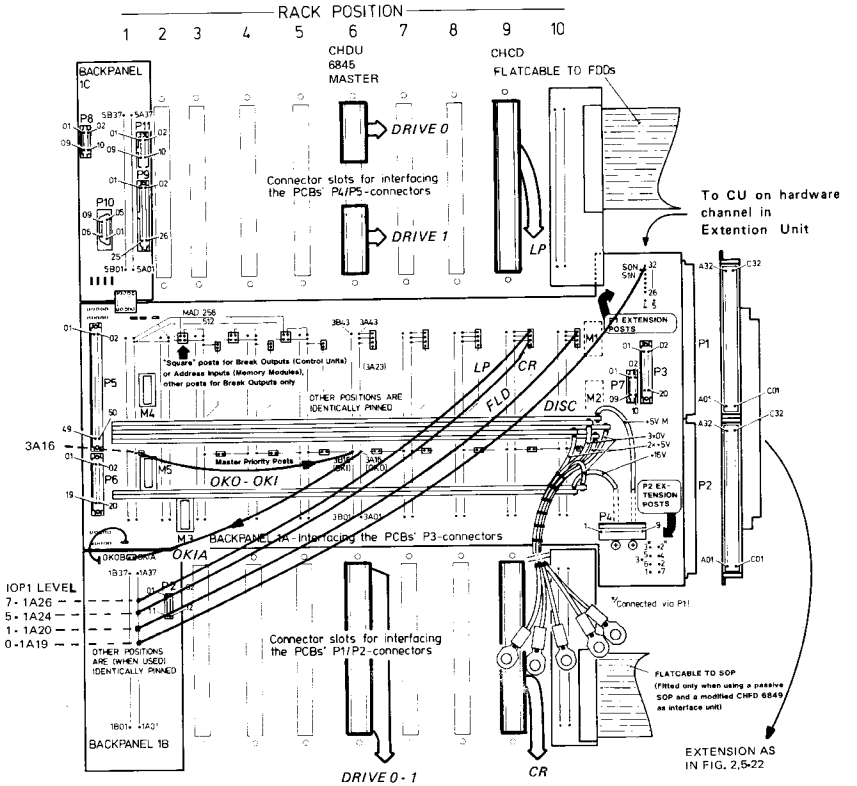


Figure 2.5.24 EXAMPLE BREAK AND OKO-OKI WIRING TC6814/24

CONTENTS

LIST OF ILLUSTRATIONS & TABLES

3.1 SYSTEM OPERATOR PANELS

3.1.1 *Common* Display & Control Facilities

Figure 3.1-1

Although there are some differences between the SOPs used for different computers, they are all basically providing the same display and control facilities.

POWER ON INDICATOR - sensing either a control signal from the PSU, or the panel's +5V supply. In the latter case the indicator is not effective if a CFP/EFP is also fitted to the computer.

RUN INDICATOR (not on TC 6810/11) - indicates that the computer operates in run mode. Not effective when a CFP/EFP is also fitted to the computer (6812/13).

SYSTEM INDICATORS - eleven indicators that are program controlled via address 2E (hex code) and the BIO lines 05-15. Always effective when power is on.

IPL SWITCH - when effective and operated this switch will load the initial program. Not effective in LOCK mode (see sub-sections 3.1.2 and 3.1.3), or when a CFP/EFP is also fitted to the computer (6811/12/13).

INTERRUPT SWITCHES - ten switches that are all interrupting on level 9 (decimal), but are individually recognizable in the data word fetched via the BIO lines 06-15. Always effective when power is on.

TEST SWITCH - lights all indicators on the panel. Always effective when power is on.

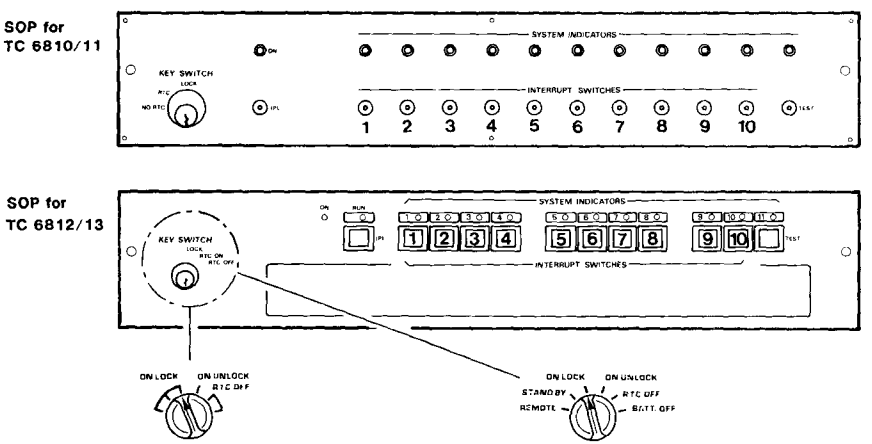


Figure 3.1-1 Existing versions of the SOP

All panels are also equipped with a mode control switch (a rotary switch, on early models controlled by a key), and here you will find the most significant differences.

3.1.2 Mode Control from SOP in TC 6810-6814

The SOPs used in TC 6810-6814 enable the selection of three different modes (each mode named in different ways on different panels):

NO RTC/RTC OFF - the computer is able to run with the Real Time Clock inhibited (necessary for certain test programs that cannot handle RTC interrupts).

RTC/RTC ON/ON UNLOCK - like above, except that the Real Time Clock is now enabled.

LOCK/ON LOCK - the computer is able to run with the Real Time Clock enabled. The IPL switch on the SOP is now inhibited, and so are all switches except INT on a fitted CFP/EFP/FRCP.

3.1.3 Mode Control from SOP in TC 6824

The SOP used in TC 6824 enables the selection of six different modes:

REMOTE - an optional remote ON/STAND BY switch is now enabled to control the computers D.C. and A.C. supply. With the switch in ON-state the PSU provides full supply; the Real Time Clock is enabled and the IPL switch is disabled. With the remote switch in state STAND BY, the PSU is only supporting the memories with maintained charging of batteries.

STAND BY - the PSU is only supporting the memories with maintained charging of batteries.

ON LOCK - like 'REMOTE', except that the remote ON/STAND BY switch is now replaced by the local one, fitted to the left on the computer's nose section.

ENSURE ON-STATE BEFORE RETURNING ROTARY SWITCH TO 'ON LOCK' AFTER PROGRAM LOADING!

ON UNLOCK - the PSU provides full supply regardless of ON/STAND BY switches; the Real Time Clock is enabled and so is the IPL switch.

RTC OFF - like 'ON UNLOCK', except that the Real Time Clock is now inhibited (necessary for certain test programs that cannot handle RTC interrupts).

BATT. OFF - disconnects battery from load to prevent discharging when the EMERGENCY mains switch is set in position OFF and no back-up is wanted.

3.2 BASIC PROGRAM LOADING

3.2.1 General

Programs can be loaded from three different media; cassette tape, flexible disc and peripheral disc (cartridge or fixed). The following sub-section describes how to operate the different drives.

3.2.2 Operating Media Drives

Cassette Drive 6861 Figure 3.2-1

Turn the cassette side to be loaded upwards, and the open edge towards the right. Push in the cassette until it is catched by the drive mechanism. To release a cassette; wait until the drive's indicator is switched off, then press the eject button fitted on the drive.

Cassette Drive 6865 Figure 3.2-1

Open the drive's door by pressing the eject knob to the right. Turn the cassette such that the side to be loaded faces the operator, and that the open edge is upwards. Place the cassette in the door and push the door to close. To release a cassette; wait until the drive's indicator is switched off, then press the eject knob to the right.

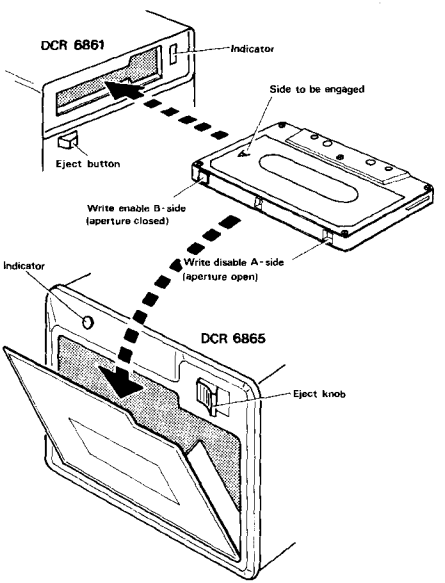


Figure 3.2-1 Operating Cassette Drives

Flexible Disc Drives Figure 3.2-2

Open door by pressing the adjacent button. Turn the flexible disc such that the label is to the left, push in the disc and close the door. To release a flexible disc; wait until the drive's indicator is switched on, open door and pull out the disc.

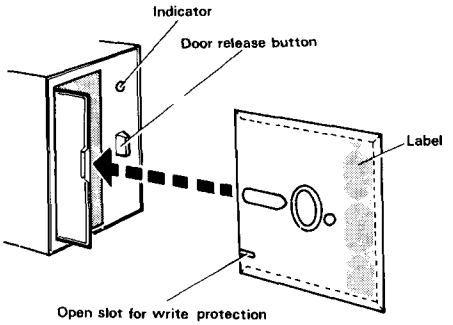


Figure 3.2-2 Operating Flexible Disc Drives

Cartridge Disc Units 6875/6876 Figure 3.2-3

To install a cartridge:

- Switch on power and ensure that the disc unit indicates CARTRIDGE EXCHANGE.
- Lift the top cover of the disc unit and press the two drive clamps outwards (at each side of the cartridge well).
- Push the de-coupler of the cartridge handle to the side, lift the handle and remove the bottom cover.
- With extreme care; place the cartridge into the drive and fold the handle into its recess. The characteristics of the correct position is that the cartridge cannot be rotated or tilted.
- Turn the bottom cover upside down and place it on top of the cartridge. Close the two drive clamps and lower the top cover of the disc unit.
- Press the START/STOP button and wait for the UNIT READY indication.

To remove a cartridge:

- Press the START/STOP button and wait for the indication CARTRIDGE EXCHANGE.
- Lift the top cover of the disc unit, press the two drive clamps outwards and remove the bottom cover.
- Push the de-coupler of the cartridge handle to the side, lift the handle and remove the cartridge with extreme care.
- Place the cartridge into its bottom cover and fold the handle into its recess.

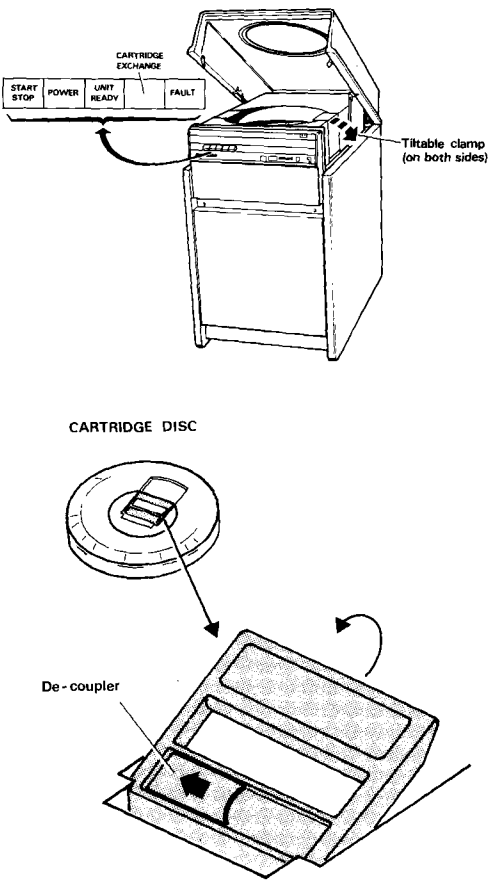


Figure 3.2-3 Operating Cartridge Disc Units, type 6875/6876

To install a disc pack:

- Make certain that the disc pack to be installed has been maintained according to the preventive maintenance instructions.
- Ensure that AC POWER is ON and raise pack access cover.
- Lift disc pack by plastic canister handle.
- Disengage bottom dust cover from disc pack by turning canister handle counterclockwise or, for newer disc packs, squeeze the levers in the center of the bottom dust cover. Set cover aside in an uncontaminated area.

CAUTION

Avoid abusive contact between the disc pack and the spindle. The read/write heads are sometimes manually positoned during maintenance procedures. Make certain that the heads are fully retracted.

- Place disc pack onto spindle. A spindle lock mechanism is actuated when the disc pack canister cover is on the spindle. The mechanism holds the spindle stationary while loading or unloading a disc pack.
- Twist canister handle clockwise to lock disc pack in place. A click may be heard as the spindle lock mechanism engages.
- Lift canister clear of disc pack, place bottom dust cover on canister, and set aside in an uncontaminated area.
- Close pack access immediately to prevent entry of dust and contamination of disc surfaces.

To remove a disc pack:

- Press the operator panel START switch to extinguish the START indicator.
- Check that disc pack rotation has stopped. (Stopping time is approximately 1.5 minutes without brake and 20 seconds with brake.)
- Raise access cover.

CAUTION

The read/write heads are sometimes manually positioned during maintenance procedures. Make certain that the heads are fully retracted.

- Place plastic canister over mounted disc pack so that post protruding from center of disc pack is received into canister handle.
- Twist canister handle counterclockwise until disc pack is free of spindle.

CAUTION

Avoid abusive contact between the disc pack and the spindle assembly.

- Lift canister and disc pack clear of spindle and close access cover.
- Place bottom dust cover in position on disc pack and lock it.

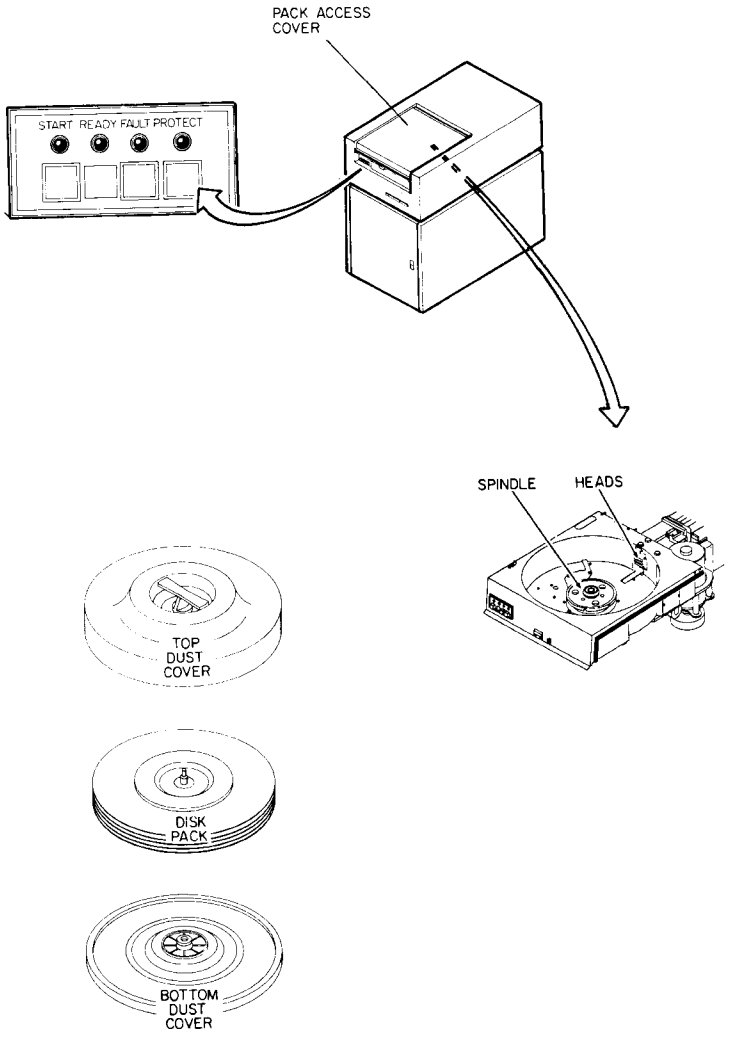


Figure 3.2-4 Operating Disc Unit, type 6877

To install a cartridge:

- Make certain that; the power is on, the START/STOP switch is out and that the indicators READY and FAULT are off.
- Release latch under lip of access door recess and pull down cartridge access door.
- To separate dust cover from the disc cartridge, push cover release button on the bottom dust cover toward the center of the cartridge.
- Disengage dust cover from disc cartridge. Set cover aside upside down to prevent dust from collecting with the cover.
- Slide the disc cartridge into the receiver track in the direction of the plastic arrow on the top dust cover, so tnat the guide pins on the top dust cover ride smoothly in the receiver track. Use the cartridge handle to insure proper horinzontal insertion of the cartridge and engagement of the guide pins in the receiver track.
- Push the top-cover handle down. Push the cartridge rearward until it stops.
- Close the cartridge access door and press the door closed until it is latched. The cartridge slides into place and centers on the spindle automatically as the access door is closed.
- Store cartridge cover upside down in some convenient location.
- Operate START/STOP switch to apply power to spindle motor.

NOTE

If the spindle motor will not rotate, disc cartridge access door may not be completely closed, the cartridge may not be properly seated on the spindle chuck or the cartridge receiver/base may not be all the way down on the lower chassis.

To remove a cartridge:

- Operate START/STOP switch to STOP (out).
- Pull down the cartridge access door after the READY indicator ceases blinking and extinguishes entirely.
- Grasp the cartridge handle and pull the cartridge out of the receiver with sufficient force to overcome the detent action.
- Replace the bottom dust cover by lining up the arrows on the top and bottom covers, so that the guide bars on the bottom cover slip into the slots on the top cover.
- When the covers are properly aligned they will lock automatically with a gentle downward pressure on the top cover.

NOTE

A disc cartridge should be installed at all times, whether operating or not, to insure proper sealing of the shroud area from environmental contaminents.

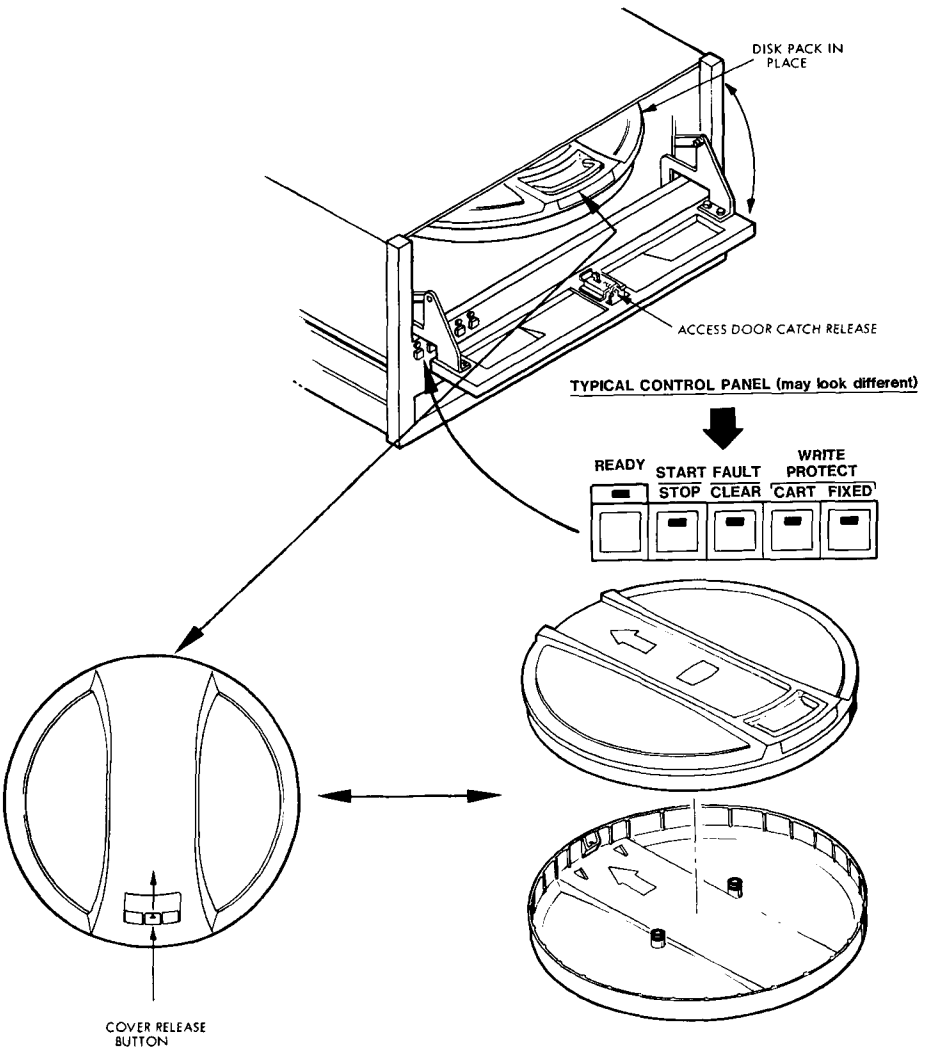


Figure 3.2-5 Operating Cartridge Disc Units, type 6961/6962

3.2.3 Control Panel Operations

The program loading is controlled from the SOP and (when fitted) from the CFP/EFP in the following manner:

- Switch on the RTC from the SOP.
- Operate the IPL switch on the SOP or, when a CFP/EFP is also fitted, the following keys in sequence on that panel: RST, MC and IPL (ERCP INST, MC and IPL).
- Set the SOP's RTC switch in position LOCK and start the prepared drive by operating the appropriate SOP switch according to Table 3.2-1.

NOTE

Flexible or peripheral discs may contain several programs, introduced by an auxiliary IPL program that enables a selection of the next program to be loaded. When the auxiliary program has been loaded the drive stops and the SOP indicators 1-10 are all lit. The selection of the next program to be loaded is made by operating another SOP switch according to a label that should be fitted on the program medium.

Table 3.2-1 Relations between SOP switches and IPL PROMS

PROGRAM LOAD SYSTEM		TYPE OF IPL PROM ON CPU BOARD*				
Media Drive	Channel**	5131 110 01142	MI-7610-5 or 4011P	5131 194 24900	5131 194 41700	5131 194 35300/66
1st DCR - left/lower	PC	Switch 1	Switch 1	Switch 1	Switch -	Switch 1
2nd DCR - right/upper	PC	2	2	2	-	2
1st FDD - left	PC	-	7***	7	7	7
" " "	IOP	-	5***	-	-	-
2nd FDD - right	PC	-	8***	8	8	8
" " "	IOP	-	6***	-	-	-
1st CDU 6875/76 - cartridge	IOP	3	3	3	3	3
" " " - fixed	IOP	4	4	4	4	4
2nd CDU 6875/76 - cartridge	IOP	-	-	-	5	9
" " " - fixed	IOP	-	-	-	6	10
1st CDU 6877	Master	-	-	5	-	-
2nd CDU 6877	Master	-	-	6	-	-
1st HDU 6961/62 - cartridge	Master	-	-	-	1	5
" " " - fixed	Master	-	-	-	2	6
Magnetic Tape	IOP	5	-	-	-	-

* When necessary; identify applicable type of PROM, positioned in co-ordinate F3 (P852), P9 (P857) or M8 (P857R/RA).

** PC = Programmed Channel, IOP = I/O Processor Channel

*** Only for FDD 6867 (250 kByte)

3.2.4 Codes Displayed on SOP Lamps

When a system is halted due to a serious error, an error code is displayed on the SOP lamps. This code should be noted and can be used later as an aid in analyzing the dump. The following lamps may be lit (lamp 1 is leftmost on the SOP panel).

- MONITOR

  SOP LAMP NUMBERS (x = lit)

7	8	9	10	11	
			x	x	No currency buffer available.
		x		x	Illegal interrupt.
		x	x	x	Stack overflow.
	x			x	Instruction not accepted. *
	x		x	x	No blocks available.
	x	x		x	Invalid instruction (trap).
	x	x	x	x	Requested LKM processor not in monitor.
x				x	Data management (SYSGEN) error.

* SST, OTR, or INR not accepted due to a hardware error.

However, in some cases the RUN lamp is off and the SOP lamps give no indication of the cause of the problem.

- DURING IPL OR SYSLOAD

  SOP LAMP NUMBERS (x = lit)

1	2	3	
x			Load
	x		I/O error
		x	Memory overflow

SOP Lamps Codes REL. 12

Error Messages	SOP lamps										
IPL	1	2	3	4	5	6	7	8	9	10	11
IPL error (file not found or Read error)	X										X
SYSLOAD											
Read error	X									X	
Memory overflow	X									X	X
Format error	X								X		
Terminal ident error	X								X		X
User of swappable work block error	X								X	X	
MMTAB overflow	X								X	X	X
Illegal page size	X							X			
Illegal monitor option	X							X			X
Data communication block error in configuration file	X							X		X	
MONITOR											
Illegal interrupt		X									X
Stack overflow		X								X	
Instruction not accepted *)		X								X	X
No block available		X							X		
Invalid instruction (trap)		X							X		X
Request LKM processor missing		X							X	X	
Error when reading overlay segment		X							X	X	X
DATA MANAGEMENT											
DM task not found (SYSGEN errro)		X					X				X
DM core pool too small		X					X			X	
Log file size error		X					X			X	X
Log file protected		X					X		X		
Segment loding error		X					X		X		X
T.Log file I/O error		X					X		X	X	
F.Log file I/O error		X					X		X	X	X

*) SST, OTR, INT not accepted due to hardware error

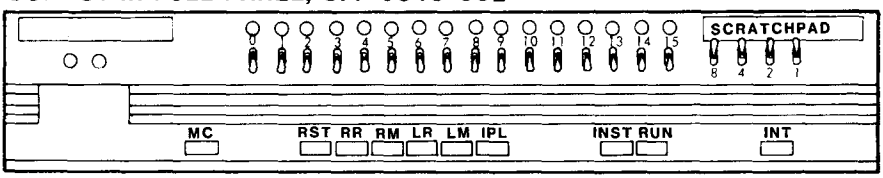
3.3 SERVICE CONTROL PANELS

3.3.1 Available Models

Three models of optional service control panels are available within the computer systems:

- Computer Full Panel, CFP 6815-002, for rack mounting in TC 6811/12
- Extended Full Panel, EFP 6817-001, for rack mounting in TC 6813
- Full Refreshed Control Panel, FRCP 6981, table-top-model for TC 6814 and 6824

COMPUTER FULL PANEL, CFP 6815-002



EXTENDED FULL PANEL, EFP 6817-001

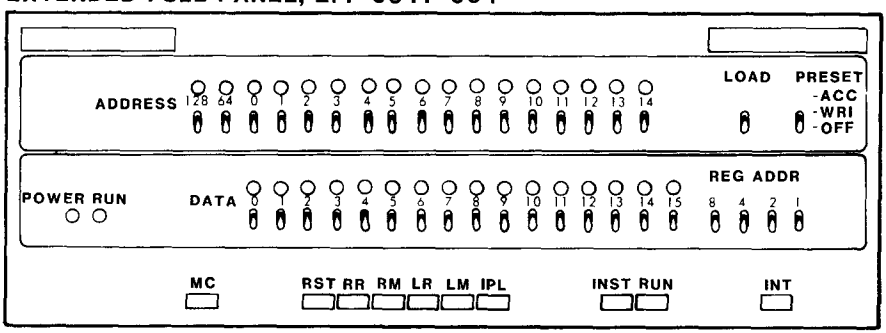


Figure 3.3-1 Computer Full Panel, CFP (top)
& Extended Full Panel, EFP (bottom)

3.3.2 Operating EFP/CP

MC — Master Clear: Clears or resets most hardware logic. Activates the GP Bus signal CLEARN, and the CPU signals MCL, MCLN.

RUN — Begins the program. The RUN switch sends the momentary signal START and the flip-flop signal RUNN to the CPU RUNF logic. Minipanel RUN performs IPL function.

INST — Instruction Step: Each time INST is pressed, the CPU performs the one instruction indicated by the program counter (P) and then halts. INST may be used to step the computer through a program (or part of one) instruction-by-instruction. The INST switch resets the control panel RUNN flip-flop, and sends a 113 usec. START signal to the RUNF logic.

RST — Read Status. The contents of the program status word are displayed on the DATA lamps.

RR — Read Register. The contents of the scratchpad register (AØ-A15) selected by the SCRATCHPAD switches are displayed on the DATA lamps.

RM — Read Memory. The contents of memory are displayed on the DATA lamps. Consecutive words can be read by repeated pressing of the RM button.
Std CP: memory address is selected by the program counter (P), and P is incremented with each RM.
EXt CP: memory address is selected by the ADDRESS switches.
The panel address register is automatically incremented; the program counter (P) is not used or affected. 1)

LR — Load Register. The word code set on the DATA switches is loaded into the scratchpad register (AØ-A15) specified by the SCRATCHPAD switches.

LM — Load Memory. The word code set on the DATA switches is loaded into memroy. Consecutive words can be loaded by repeated pressing of LM.
Std CP: memory address is selected by the program counter (P), and P is incremented with each LM.
Ext CP: memory address is selected by the ADDRESS switches.
The panel address register is automatically incremented; the program counter (P) is not used or affected. 1)

IPL — Initial Program Loaded. An initial bootstrap program located in a hardware read only memory is loaded into memory word locations 00 to 063_{10} (characters 00 to $7E_{hex}$).

INT — Interrupt. This button generates a level-1 Interrupt Request for the Operator's interrupt. The same interrupt can be set by the I/O console via the integral serial control unit. The interrupt may be used by the operator, for example, to change the running program with information supplied by the operator.

Data

DATA — The 16 DATA switches are used to set a data word onto the Bus BIO lines during load register (LR) and load memory (LM) operations. For all computer operations, the DATA lamps display the contents of the Bus BIO lines. When a running computer stops, the DATA lamps display the contents of the next instruction. For RR and LR operations, the DATA lamps display the contents of the scratchpad register (AØ-A15) selected by

Scratchpad Register

SCRATCHPAD — These four switches select one of the scratchpad register (AØ-A15) to be accessed by the read register (RR) or load register (LR) operation.

Address Section (Extended CP only)

ADDRESS — The ADDRESS switches are used to select an initial memory address for read memory (RM) and load memory (LM) operations. For all computer operations except RM and LM, the ADDRESS lamps display the contents of the Bus MAD lines, via the panel address register. When a running computer stops, the ADDRESS lamps display the address of the next instruction. For RM and LM operations, the ADDRESS lamps display the contents of the panel address register, which is loaded from the ADDRESS switches and incremented by the RM and LM operations. No control is provided for bit 15 (character selector) because the panel accessed only memory word addresses.

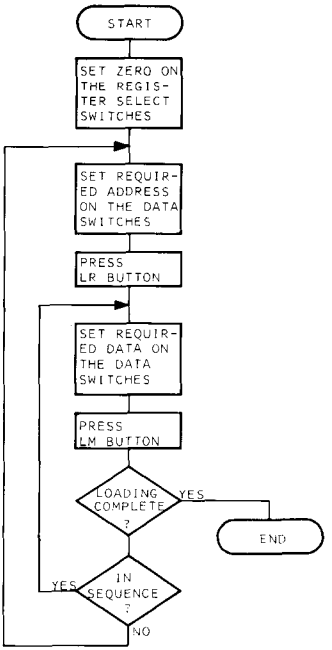
LOAD ADDR — When this button is pressed, the code set on the ADDRESS switches is immediately loaded into the panel address register. This address is incremented by successive RM or LM operations; the address register is reloaded from the MAD lines for any other operation.

PRESET — This switch is used to select a Stop On Address mode. The stop will occur when the MAD-line address, via the panel address regster, compares with the code set on the ADDRESS switches.

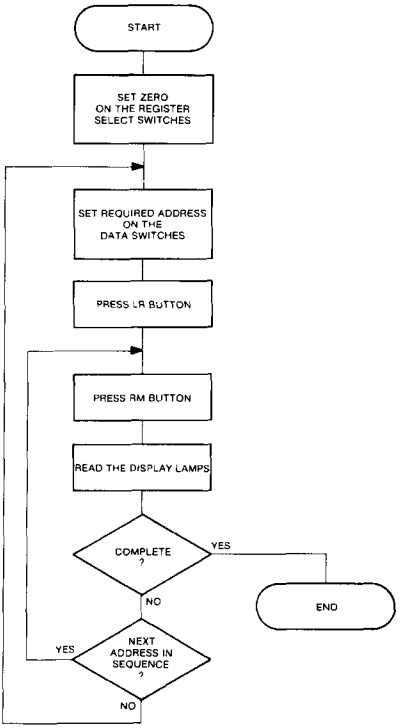
- OFF — Normal operation. Do not stop on address.
- ACC — Stop On Address, Access. Stop when any memory operation accesses the address set on the ADDRESS switches.
- WRITE — Stop On Address, Write. Stop when any memory operation writes at the location set on the ADDRESS switches.

1) To start a program load register AO(P) with the start-address as well as on the standard controlpanel as on the extended controlpanel.

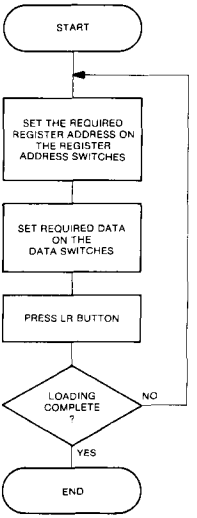
LOAD MEMORY (FULL CONTROL PANEL)



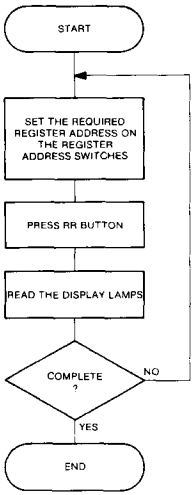
READ MEMORY (FULL CONTROL PANEL)



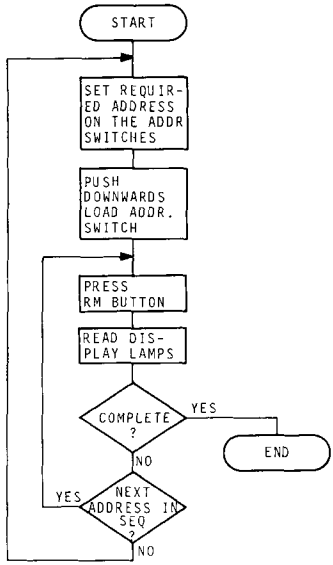
LOAD REGISTER



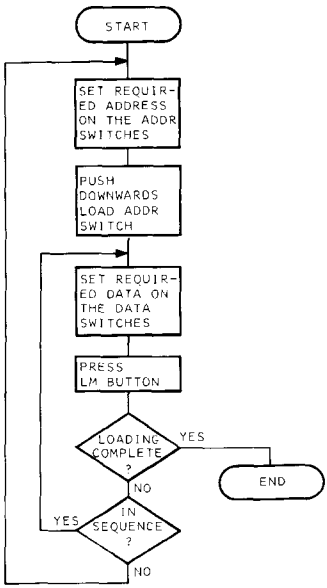
READ REGISTER



READ MEMORY (EXTENDED CONTROL PANEL)



LOAD MEMORY (EXTENDED CONTROL PANEL)



Panel Lock and RTC Switches

The slide switch LOCK operates in conjunction with the LOCK function on the system operator's panel, SOP. If both panels are set in position LOCK (on FRCP; righthand switch position), all panel functions except for the INT actions are inhibited.

The slide switch RTCE (Real Time Clock Enable) operates in conjunction with the RTC switching on the SOP. If both panels are in enable mode (on FRCP; righthand switch position), the real time clock interrupts are enabled.

Hexadecimal Key Array

The hexadecimal key array (0-F) enables the operator to enter hexadecimal address and data characters. The characters of a certain category are sequentially entered, starting with the most significant digit. Entered characters are shifted from right to left into the righthand display section.

Before entered characters are made effective, by operating a function key, it is possible to cancel the characters by operating the key CLD (Clear Data).

Program Load & Control Functions

MCL Master Clear. Before starting any operation it is recommended to press the key MCL. This will clear or reset most hardware logic.

IPL Initial Program Loading. The bootstrap, contained in ROM, is read into the memory.

INT Interrupt. Generates a control panel interrupt, not recognized by ordinary application programs, but accepted by certain test programs.

INST Instruction Step. Stops a running program and switches the CPU into the idle mode. The program can now be stepped instruction-by-instruction by repeated operations of the INST key. After each key operation the address and contents of the next instruction are shown on the lefthand and righthand displays respectively.

RUN Switches the CPU into run mode, starting with the instruction defined by register 0 (program counter). The word 'run' is shown on the righthand display.

Stop On Preset Address

With the CPU in idle mode; enter the wanted stop address from the hexadecimal key array. Then press either of:

PACC Preset Access Stop. The program is prepared to stop for <u>any</u> memory access to the entered address.

PWR Preset Write Stop. The program is prepared to stop only on write access to the entered address.

The program is then started by operating the RUN key (possibly after a new address loading into register 0, the program counter). During run time the righthand display indicates a preset address by the letter 'P', and the address itself is shown on the lefthand display.

When the stop address is met, the CPU switches into the idle mode and the displays show the address (left) and contents (right) of the next instruction. For recalling the stop address; just press the key RPA (Read Preset Address).

A prepared stop action can be inhibited by operating the key POFF (Preset Address Stop Off).

Read Register

- With CPU in idle mode; enter the wanted register number from the hexadecimal key array.
- Operate the key RR (Read Register).

The register number is now shown on the lefthand display, and its contents on the righthand display.

Read Memory

- With CPU in idle mode; enter the wanted memory address from the hexadecimal key array.
- Operate the key LA (Load Address), and the chosen address is shown on the lefthand display.
- Read addressed memory location by operating the key RM (Read Memory).

The read information is now shown on the righthand display, and the address on the lefthand display is increased by 2 (note that the contents of the program counter is not changed).

For reading sequential memory locations, just repeat the RM operations.

Read Status

With CPU in idle mode; operate the key RST (Read Status). The CPU status word is now shown on the righthand display.

Load Register

- With CPU in idle mode; enter the register number from the hexadecimal key array.
- Operate the key RR (Read Register), and the displays show the number (left) and contents (right).
- Enter wanted data from the hexadecimal key array.
- Operate the key LR (Load Register).

The lefthand display still shows the register number, and the righthand display shows the entered data, now also loaded into the register.

Load Memory

- With CPU in idle mode; enter the wanted memory address from the hexadecimal key array.
- Operate the key LA (Load Address), and the chosen address is shown on the lefthand display.
- Enter wanted data from the hexadecimal key array.
- Operate the key LM (Load Memory)

The address on the lefthand display is now increased by 2 (without affecting the program counter), and the righthand display shows the entered data, now also loaded into the addressed memory location.

For loading sequential memory locations, just repeat the last two steps.

Calculator Mode

The FRCP also provides a calculation facility for hexadecimal operands with a maximum length of 8 digits. The calculation mode is entered by operating the keys INST and 0 at the same time. The lefthand display will then indicate calculator mode by presenting the letter 'C' in its leftmost position.

The panel is now ready for calculations. To cope with 8-digit numbers, the righthand display (6 positions) is now extended with the two rightmost positions of the lefthand display. Five function keys may be used in the calculator mode:

MLC:	Clear all (display dark)
CLD:	Clear entry (display = 00 000000)
RR:	+
RM:	-
INT:	=

Consecutive operations are allowed and the last operand is memorized, see following example:

Operation	Display
A - 5 + C - B + 3 +	9
+	C
+	F
+	12
=	15
+	15
FC	FC
=	111

To leave the calculator mode; just press the INST key.

Test Functions

By operating the key TEST you can check the displays; all segments should now be illuminated. If the keys TEST and 0 are operated at the same time, you will start a microdiagnostic routine. See chapter 4, Manintenance.

FULL REFRESHED CONTROL PANEL, FRCP 6981

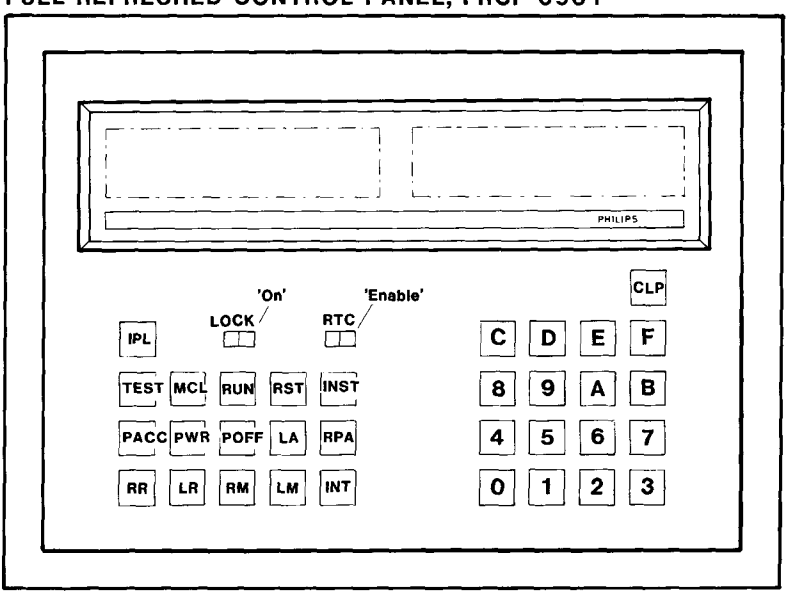


Figure 3.3-2 Full Refreshed Control Panel, FRCP

CONTENTS

LIST OF ILLUSTRATIONS & TABLES

4.1 PREVENTIVE MAINTENANCE

4.1.1 Replacing Cabinet Air Filters

Figure 4.1-1

Once a year, or when otherwise required, the air filter should be replaced. In the TCs 6810-6814 the filters are pulled out/pushed in at the rear of the cabinets' base section. In TC 6824 the filter is placed at the rear of the back cover and is loosened by pressing the holder down and tilting it backwards.

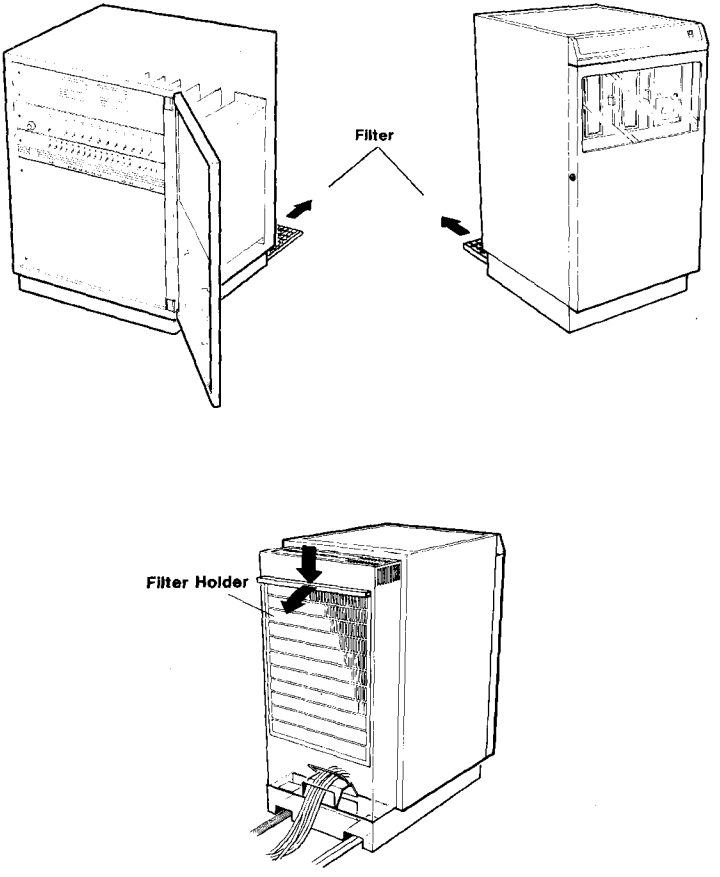


Figure 4.1-1 Replacing Air Filters

4.1.2 Preventive Actions to DCR 6861

Figure 4.1-2

Every Week

Clean the head and the capstan, the tape guides and the pinch rollers with Philips wet cleaning cassette (5322 397 34004). This cleaning operation should be a part of the operators' working routines and not a business of service technicians!

Every 6 Months

- Clean the capstan, the pinch rollers and the read/write head; all with cotton wool buds or chamois leather cloth and isopropanol.
- Clean the chassis from wear and dust particles with a brush.
- Clean the BOT/EOT detector (49) with a dry brush and replace the BOT/EOT lamp assembly (69).
- Clean the gear wheels (78) with a brush.
- Clean the belt (62) with isopropanol and check the condition (if necessary; replace the belt).
- Grease the following points with Molycote BR2:

  a) The contact-faces of the retrieval segment (107) and latch assembly (96) with the cassette holder top section (106).

  b) The contact-faces of the retrieval arm (102) with the A-side lever (112) and write-enable lever (113).

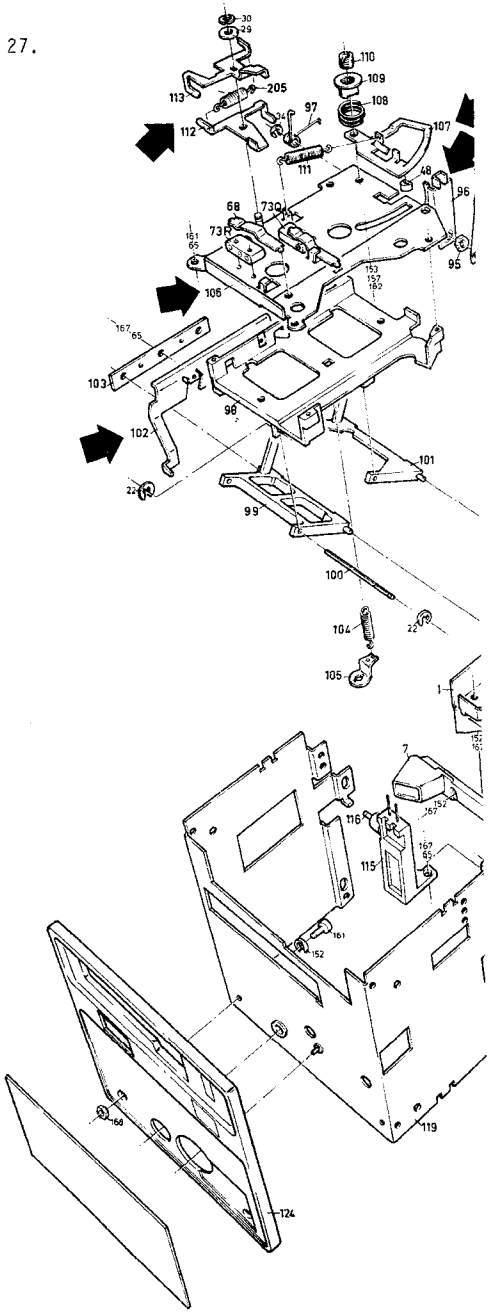
  c) The contact-faces of the two clamps (58A,B) with the nipples (56A,B).

Every 12 Months

Grease (with Molycote BR2) the following pivots of the cassette holder lift section:

- lift levers (99) and (101) with the cassette holder bottom section (98),
- lift levers (99) and (101) with the chassis (1),
- two guides (76A) and (76B),
- contact-face of the retrieval lever (2) with the chassis (1),
- contact-face of the lock slide (8) with the chassis (1),
- contact-face of the lever (51) with the chassis (1),
- pivots of the four solenoid flap assemblies (11A), (11B), (11C) and (12),
- pivot of the rod (33) with the rocker arm assembly (35),
- contact-face of the nipple (26) with the rod (33).

Lubricate the spindles (39,40) with Tegula 27.



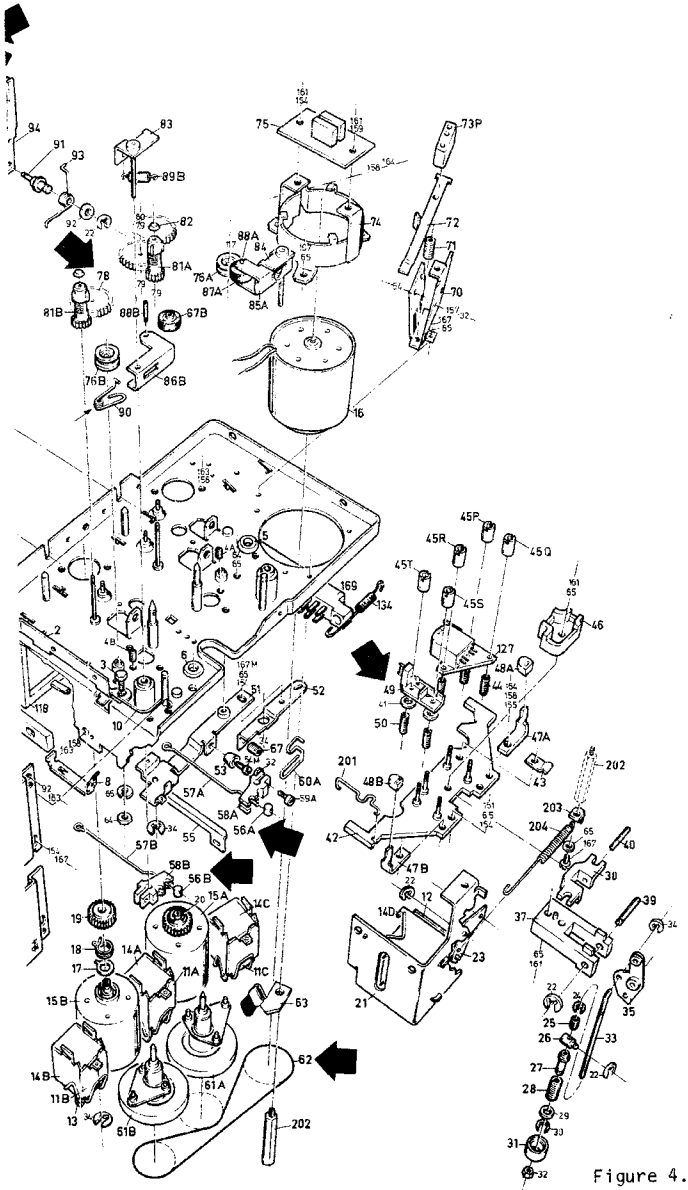


Figure 4.1-2 Exploded View of DCR 6

4.1.3 Preventive Actions to DCR 6865

Every Week

Clean the head and the capstan, the tape guides and the pinch rollers with Philips wet cleaning cassette (5322 397 34004). This cleaning operation should be a part of the operators' working routines and not a business of service technicians!

Every 5000 Hours

- Clean the chassis from wear and dust particles with a dry brush.
- Clean the pulleys, the head, the capstan and the pinch rollers with isopropanol.
- Clean the openings for the BOT LED and the photocell by means of a soft brush.

4.1.4 Preventive Actions to FDD 6867

Every 600 Hours Figure 4.1-3

Inspect the head load pad. If pad is worn, dirty, torn or loose it should be replaced as follows:

CAUTION

Do not raise the head-load arm to the 90-degree position and then release it; damage to the load-arm spring and/or to the head (core and ceramics) could result.

a. Remove power from the unit.

b. Move the carriage assembly to its rear most position (towards the stepper motor) by turning the back part of the stepper motor shaft. This will provide clearance for lifting the head load arm.

c. Lift the head load arm until the head load pad is visible.

d. If head load arm is a 77603108 (the type shown in Figure 4.1-3) proceed to step h, if not go to step e.

e. Remove the used pad with a sharp tool, if necessary, and discard. Be sure to remove all of the old pad and adhesive. Alcohol may be used to remove the old adhesive.

f. Remove the protective backing from the new head load pad and position pad in centre of recess of head load arm. Press pad firmly to insure adhesion with a clean tongue depressor or with thumb using a lint free cloth to protect the pad from grease or dirt.

g. Go to step n.

h. Loosen clamping screw holding rim of head load pad.

i. Insert screw driver and rotate head load pad so flattened side will clear clamping screw.

j. Remove Pad Holder Assembly.

k. Insert new Assembly, with flat side towards clamping screw.

l. Assuring that head load pad is fully seated, rotate pad 180°.

m. Tighten clamping screw to hold pad in place.

n. Lower arm gently onto head.

Inspect the read/write head. If cleaning is required, proceed as follows:

CAUTION

Do not smoke while cleaning. Do not touch a head surface with fingers. Do not leave residue or lint on the head surfaces. Residual particles can result in a scored disc and/or loss of a head.
Do not raise head-load arm to the 90-degree position and then release it; damage to the load-arm spring and/or to the head (core and ceramics) could result.

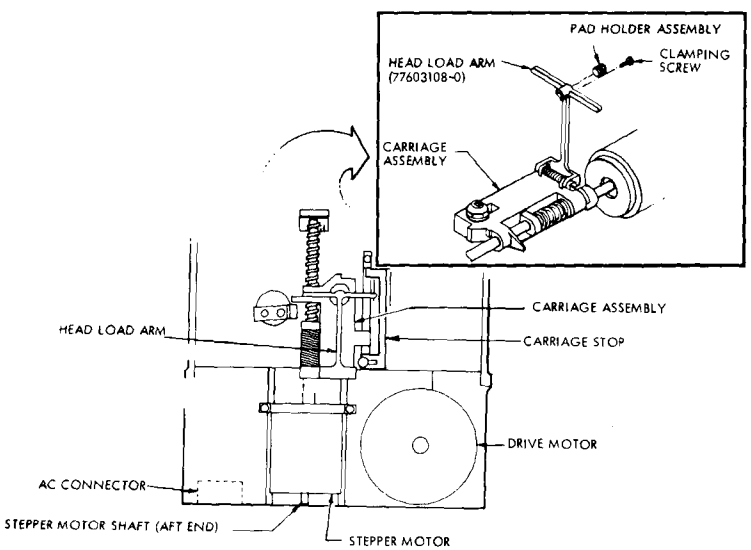


Figure 4.1-3 Head Load Pad Replacement

a. Use lint-free cloth to lightly drybuff head surface. Cleaning is completed if deposits are removed.

b. If oxide deposits were not removed in step (a), dampen (do not soak) cloth with cleaning solution (91% isopropyl alcohol) and wipe head surface. Finish by lightly dry buffing again to ensure that the head is dry and no alcohol residue is left.

4.1.5 Preventive Actions to Battery Modules (TC 6824)

Approved Battery Types

There are three types of 12V-batteries approved for use in TC 6824:

- Chloride - Gates X016 ABS Case
- SAFT PA 1204
- Sonnenshein Dryfit A300

Two batteries in series are required to build up the 24V module used in the computer.

Maintaining Stored Batteries

The battery module should be kept separately until the computer is delivered to customer. The batteries should not be left without charge for more than 4 weeks to prevent excessive discharge and/or increased internal resistance.

A charging voltage of 2.3V per cell or 13.8V for a 12V battery (common for all types) is recommended. The recommended batteries are completely sealed and no gas is emitted when under charge. A charging unit where the batteries in store can continously be charged is convenient.

Before delivery the batteries should be checked with a load of about 0.5A. The battery voltage should then be at least 2.05V per cell or 12.3V for a charged 12V battery.

Adjusting Charging Voltage in PSU

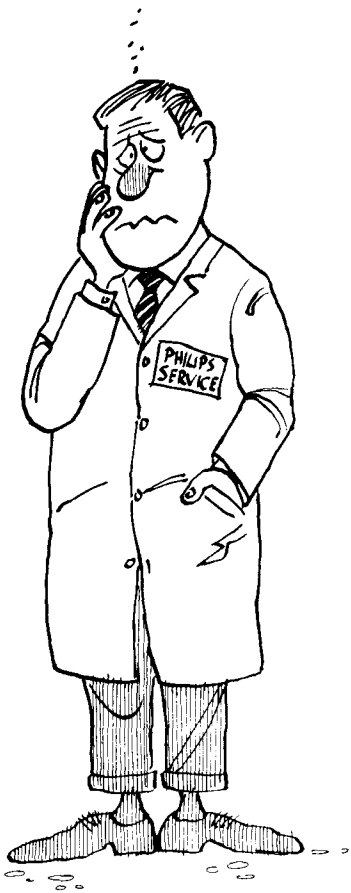
When changing computer-installed batteries from the Chloride type to the SAFT/ Sonnenschein type, or vice versa, it is necessary to adjust the charging voltage supplied by the PSU. The adjustment is made by means of potentiometer R153, see chapter 7! The charging voltage should be 28.4V for a Chloride module, and 27.0V for SAFT/Sonnenschein modules.

4.2 TROUBLESHOOTING

4.2.1 General

The aim of corrective field service is to find and replace faulty subunits in the shortest time possible. It is useless to try to create any kind of fault finding scheme, because every service technician has developed his own methods of troubleshooting. However, mind the following basic rules:

- Ask operators for symptoms; same or similar symptoms at several work stations indicate computer error.
- Use your eyes, ears and nose!
- Where available; run the diagnostics programs built into the equipment (subsections 4.2.2 & 4.2.3).
- If necessary; simplify the system by unplugging all unnecessary subunits. Load a few instructions via a service control panel and test the system instruction by instruction (chapter 3).
- Mind U-links and switches on subunits and on computer rack backpanels.
- Inspect "weak" components; fuses, switches, cables and lamps.
- After repair; run rest programs (chapter 5) to verify proper functions.



CAUTION

Switch off power before unplugging subunits. Bus transceivers are otherwise easily blown and may block the complete bus!

```
**********************************************************************
* THE BEST SERVICE TECHNICIAN IS NOT THE ONE WHO CAN IN DETAIL EXPLAIN THE *
* CAUSE OF A TROUBLE, BUT THE ONE WHO REPAIRS IT IN THE SHORTEST TIME!    *
**********************************************************************
```

The service policy is: KEEP THE CUSTOMER SATISFIED!

4.2.2 Diagnostics Aids in TC 6813

General Figure 4.2-1

To make use of the diagnostics aids of the TC 6813 (CPU P857), it is necessary to have access to an Extended Full Panel (EFP) and to set the CPU in diagnostics mode.

The diagnostics mode is set by moving the upper U-link on backpanel 1C from position NORM to position DIAGNOS.

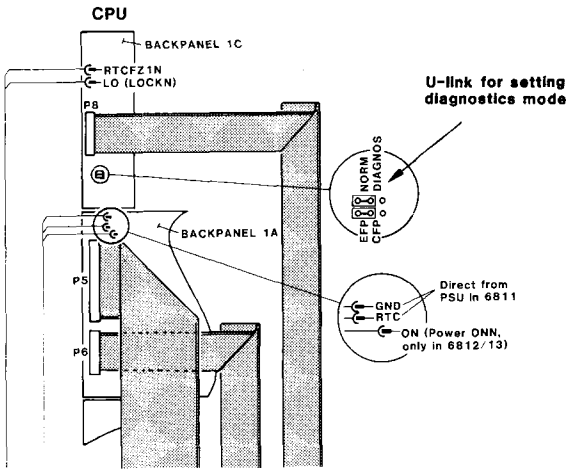


Figure 4.2-1 U-Link for Diagnostics Mode in TC 6813

Basic Test

With the U-link in position DIAGNOS:

a. Operate each DATA switch and check that corresponding indicators are lit.

b. Press the LR button, operate each DATA switch and check that corresponding indicators are lit.

c. Repeat actions according to b.

d. Repeat the b-actions another time.

These tests exercise all switch- and indicator positions of the panel, as well as the data path. Some functions are also tested in the registers L, M and Q, in the ALU and in the selectors C and D.

Go/No-Go Test

With the U-link in position DIAGNOS:

a. Set DATA switch 0 to position 0 and press the RUN button.

b. Wait for the DATA display: 0000 0000 0000 ●000 (● = dark indicator).
   If expected display, proceed with c, otherwise; replace the CPU board.

c. Set address of existing control unit (channel unit) on DATA switches 02-07, press the LM button.

d. Wait for the DATA display: 0000 0000 0000 0000 (all indicators lit).
   Expected display indicates correct memory operations and correct communications with the addressed control unit (channel unit).

4.2.3 Diagnostics Aids in TC 6814 & TC 6824

Full refreshed Control Panel, FRCP

To make use of the diagnostics aids of the TCs 6814 and 6824 (CPU 857R/857RA), it is necessary to have an FRCP connected to P10 on backpanel 1C.

Automatic Power-On Test

An automatic test is executed at the power-on time. It tests the major part of the CPU, the FRCP interface, a part of the FRCP itself and its cable. A correct test result is indicated by the code FFFC on the righthand part of the display, provided that the panel is not in LOCK state.

This automatic part of the test is of "go-no go" type. If the expected code is not displayed it is not possible to distinguish if the problem is due to the CPU, to the FRCP or its cable, and it is not possible to run further tests.

Operator-Controlled Test

Further tests can be started by the operator, provided that the automatic test indicated correct function. These additional tests are started by pressing the FRCP buttons TEST and 0 simultaneously. The result of these tests is indicated by one of five possible codes, shown on the righthand part of the display:

Code 0001 = CPU Error
     0002 = Bus or Control Unit Error
     XX03 = Bus or RAM Error
     YY04 = Correct Function
     0010 = MMU/IOP Error (or absent)

Note: XX = 8 most significant bits of the memory address causing the error

YY = 8 most significant bits of the last memory address

The address causing the bus/memory error can be read from A1 by the operator, and the contents of this address can be read from A2 by the CPU.

4.3 REPLACEMENT INSTRUCTIONS

4.3.1 Cabinet & Rack Assemblies, TC 6812/13/14/24

Removing Back- and Top Covers Figure 4.3-1

The back- and top covers of the cabinets are removed in the following way:

- Open the front door.
- Pull forward the release lever of the back cover (at the underpart of the nose section).
- Disconnect the earth wire from the back cover and lift it off. ENSURE THAT THE WIRE IS RECONNECTED WHEN THE COVER IS REFITTED!
- Pull down the two snap locks of the top cover (inside the rear of the cabinet).
- Lift the rear edge of the top cover and pull it backwards.

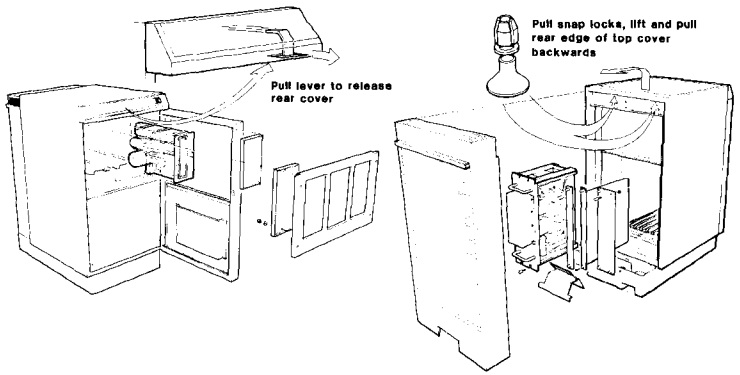


Figure 4.3-1 Removing Back- and Top Covers

Removing Nose Section

The nose section, containing the mains switch (magnetic circuit breaker), removed in the following way:

- Remove the back- and top covers according to description above.
- ENSURE THAT THE CABINET IS DISCONNECTED FROM MAINS SOURCE!
- Loosen the nose section by removing the six screws from inside.

> CAUTION!
>
> HOLD THE FRONT DOOR FIRMLY DURING THE FINAL PHASE, BECAUSE ITS UPPER HINGE PIN IS FITTED INTO THE NOSE SECTION AND WILL NOW BECOME LOOSE.

- Lift off the door and disconnect the wires from the mains switch in the n section. ENSURE THAT ALSO THE EARTH WIRE IS RECONNECTED WHEN THE NOSE SECTI IS REFITTED!

Removing the Rack

The main rack of the cabinets is removed in the following way:

- Remove the back- and top covers according to previous description.
- ENSURE THAT THE CABINET IS DISCONNECTED FROM MAINS SOURCE!
- Disconnect and remove the control panel(s) together with the blind panel(s)
- Disconnect all external cables screwed onto the rack front, or plugged PCB front panel connectors.
- Remove the rear grid or plate behind the FDDs (and the DCRs).
- Disconnect and remove the heavy submodules, i.e. PSU, FDDs and DCRs.
- Loosen the rack by removing the six screws along the vertical front edg and carefully pull the rack out of the cabinet.

Removing the Fan Unit (TC 6812/13/14)

The fan unit, fitted in the base section of the cabinets, is removed following way:

- Remove the rack according to description above.
- Loosen the fan unit by removing the six screws that fix the chassis t base section.
- Disconnect the earth wire, the mains cables and lift up the fan unit. E THAT THE EARTH WIRE IS RECONNECTED WHEN REFITTING THE FAN UNIT!

Replacing the DCR Backpanel (TC 6812/13/14)

The backpanel at the rear of the DCR sub-rack is replaced in the following way:

- Remove the back- and top covers according to previous description.
- Remove the rear grid or plate behind the FDDs and DCRs.
- ENSURE THAT THE CABINET IS DISCONNECTED FROM MAINS SOURCE!
- Disconnect the cables from the backpanel and loosen it by removing the nuts from the rear.

Replacing the Rack Backpanels 1B, 1C and 1D

Pull out all boards plugged into the rack and remove the rack according to previous description. Remove all interconnections between the backpanels and loosen panels by removing their top and bottom brackets inside the rack.

Replacing the Rack Backpanel 1A

- Remove backpanel 1B (bottom one) according to instructions above.
- Unscrew and remove the edge connector guide along the bottom of backpanel 1A (inside the rack), and take care of the washers fitted.
- Slide down the backpanel and lift it out (if necessary; loosen also the top guide - but do not remove it).
- When refitting a new backpanel - do not forget the washers!

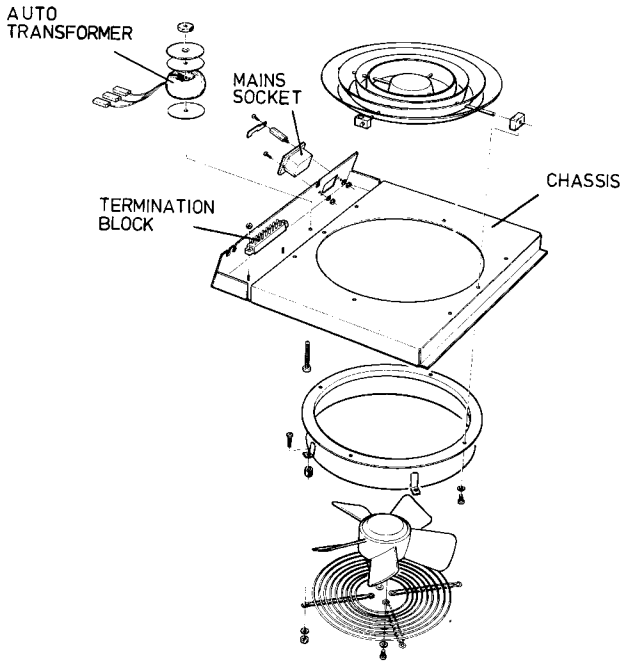
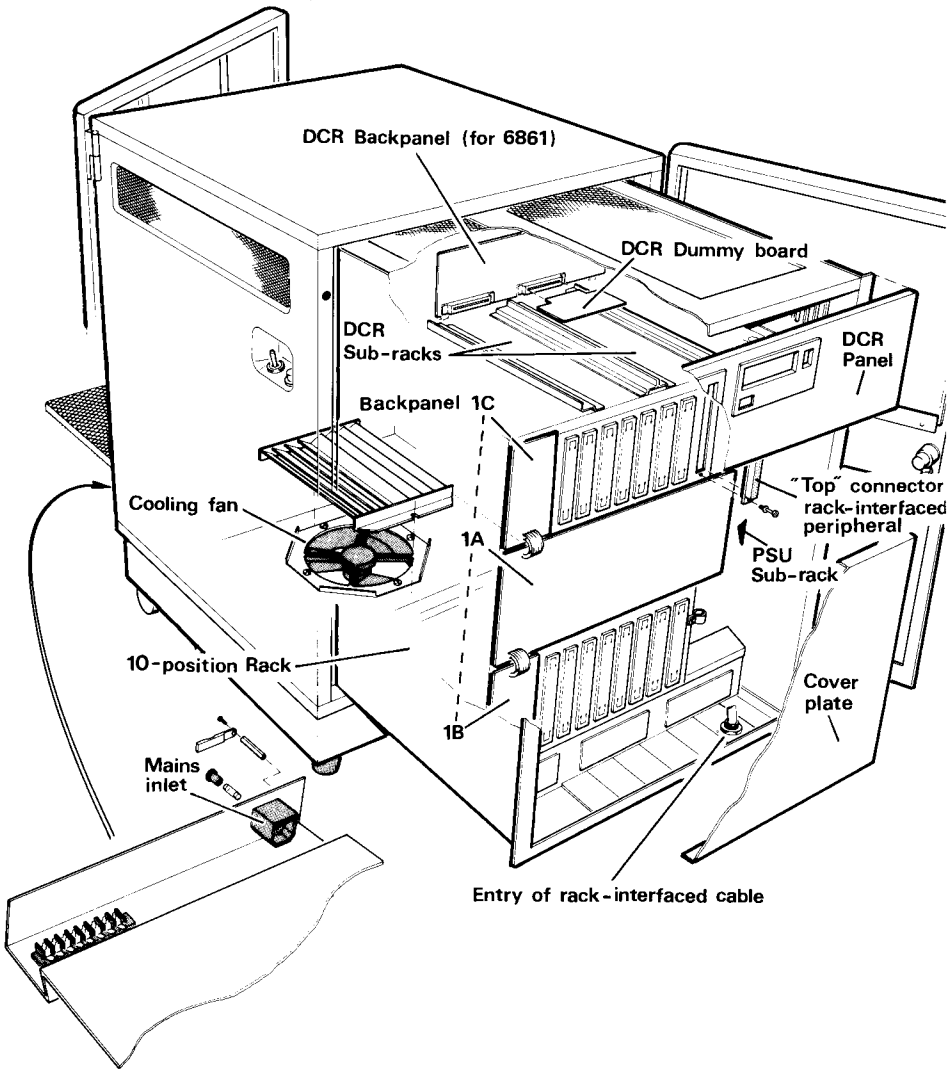


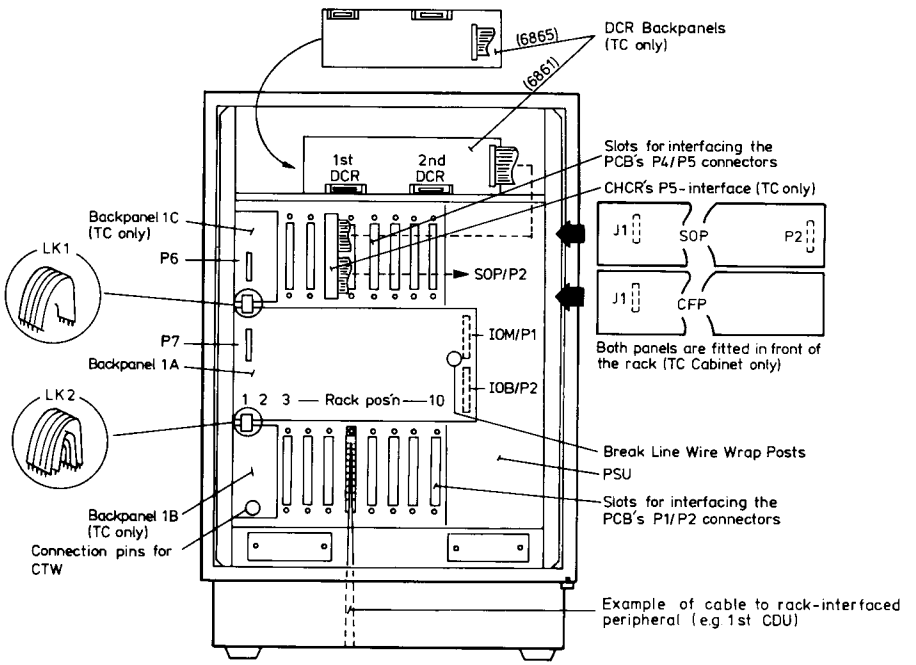
Figure 4.3.2 FAN-UNIT & FILTER

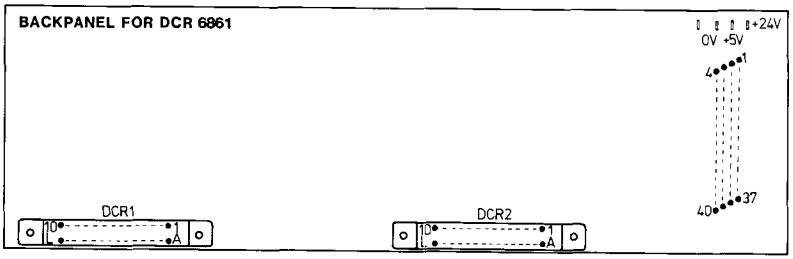
CONTENTS

* To be supplied.

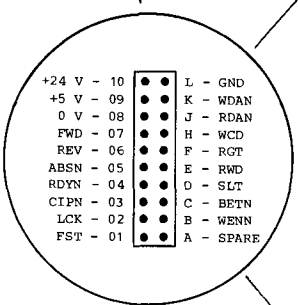

DCR Backpanel (for 6861)
DCR Dummy board
DCR
Sub-racks
DCR
Panel
Backpanel 1C
"Top" connector
rack-interfaced
peripheral
Cooling fan
1A
PSU
Sub-rack
10-position Rack
Cover
plate
1B
Mains
inlet
Entry of rack-interfaced cable

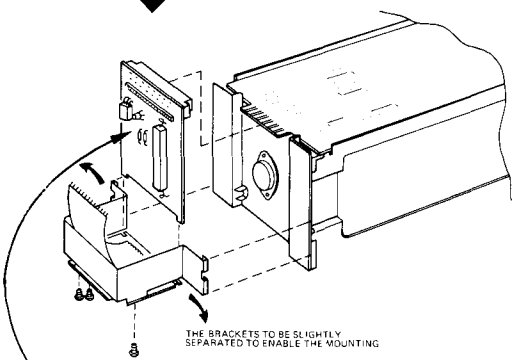
TC & EXU CABINETS — Front view of backpanels and connectors



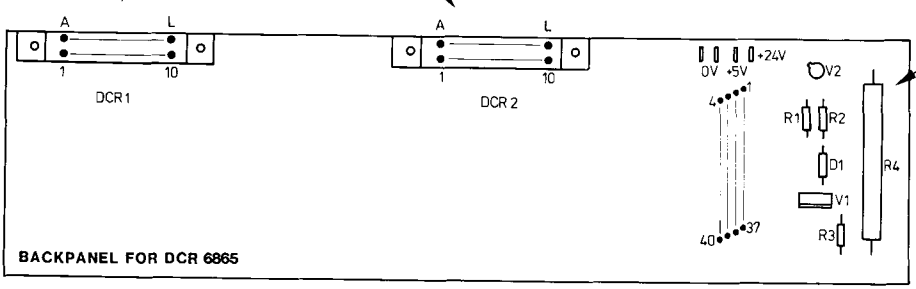


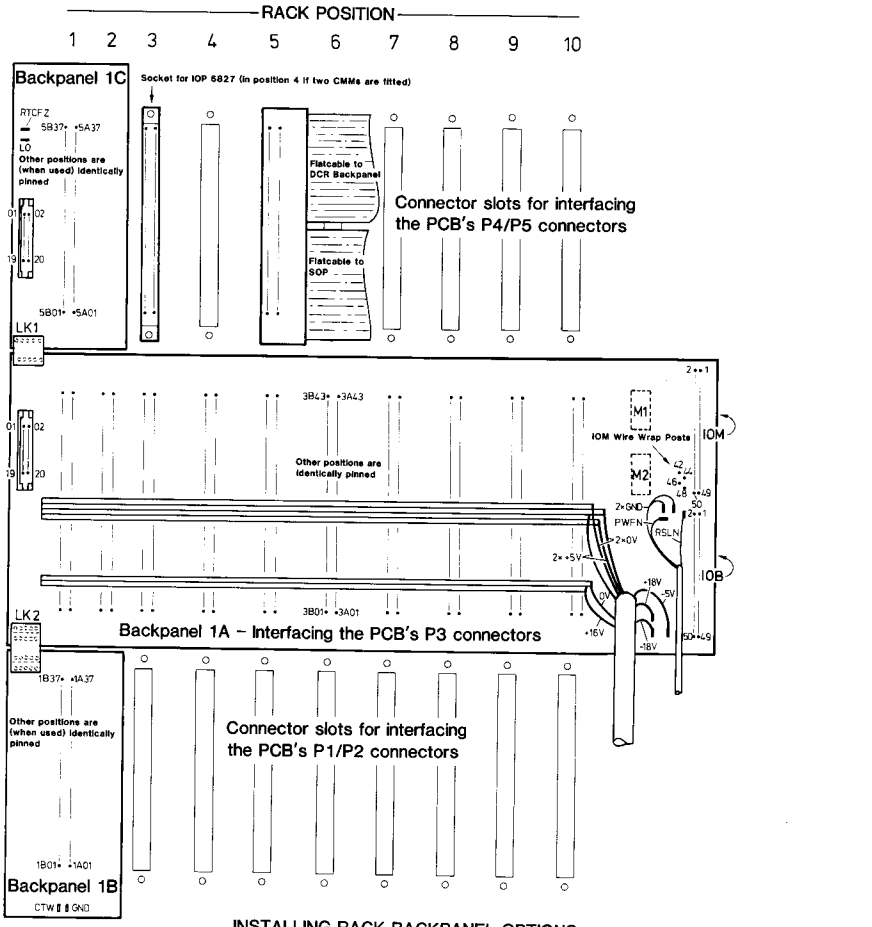
Modification kit for adapting DCR 6865 to the original backpanel (for DCR 68





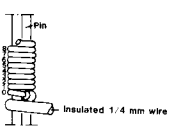
Control circuit for 24V, see Power Distribution



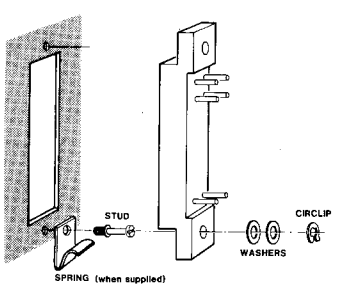


INSTALLING RACK BACKPANEL OPTIONS

Additional wire wrap connections



Socket for P1/P2 or P4/P5 connectors



P5 - CPU P852

INSTN - 5B37	● ●	5A37 - READRN
READMN - 5B36	● ●	5A36 - LOADMN
RCP 02N - 5B35	● ●	5A35 - RCP 03N
RCP 01N - 5B34	● ●	5A34 - READSTN
RUNFA - 5B33	● ●	5A33 - LOADRN
CPINT - 5B32	● ●	5A32 - RCP 00N
START - 5B31	● ●	5A31 - RUNN
IPL - 5B30	● ●	5A30 - UNLOCKN
CPMCN - 5B29	● ●	5A29 - BIOEKEY
SPARE - 5B28	● ●	5A28 - SPARE
" - 5B27	● ●	5A27 - "
" - 5B26	● ●	5A26 - "
" - 5B25	● ●	5A25 - "
" - 5B24	● ●	5A24 - "
" - 5B23	● ●	5A23 - "
" - 5B22	● ●	5A22 - "
" - 5B21	● ●	5A21 - "
" - 5B20	● ●	5A20 - "
" - 5B19	● ●	5A19 - "
" - 5B18	● ●	5A18 - "
" - 5B17	● ●	5A17 - "
" - 5B16	● ●	5A16 - "
" - 5B15	● ●	5A15 - "
" - 5B14	● ●	5A14 - "
" - 5B13	● ●	5A13 - "
" - 5B12	● ●	5A12 - "
" - 5B11	● ●	5A11 - "
" - 5B10	● ●	5A10 - "
" - 5B09	● ●	5A09 - "
" - 5B08	● ●	5A08 - "
" - 5B07	● ●	5A07 - "
" - 5B06	● ●	5A06 - "
" - 5B05	● ●	5A05 - "
" - 5B04	● ●	5A04 - "
" - 5B03	● ●	5A03 - "
" - 5B02	● ●	5A02 - "
" - 5B01	● ●	5A01 - "

P4/P5 - IOP 6827

NOT USED - 5B13	● ●	5A13 - NOT USED
" " - 5B12	● ●	5A12 - " "
" " - 5B11	● ●	5A11 - " "
" " - 5B10	● ●	5A10 - " "
" " - 5B09	● ●	5A09 - " "
" " - 5B08	● ●	5A08 - " "
" " - 5B07	● ●	5A07 - " "
" " - 5B06	● ●	5A06 - " "
" " - 5B05	● ●	5A05 - " "
" " - 5B04	● ●	5A04 - " "
" " - 5B03	● ●	5A03 - " "
" " - 5B02	● ●	5A02 - " "
" " - 5B01	● ●	5A01 - " "

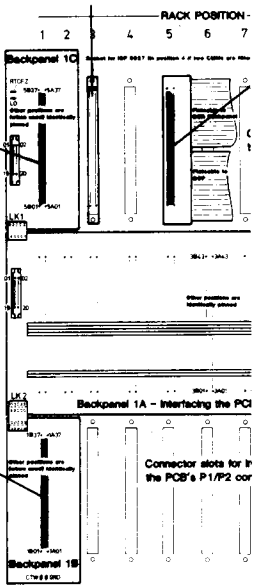
No board connector in this section

BR 00N - 4B13	● ●	4A13 - NOT USED
BR 01N - 4B12	● ●	4A12 - " "
BR 02N - 4B11	● ●	4A11 - " "
BR 03N - 4B10	● ●	4A10 - " "
BR 04N - 4B09	● ●	4A09 - " "
BR 05N - 4B08	● ●	4A08 - " "
BR 06N - 4B07	● ●	4A07 - " "
BR 07N - 4B06	● ●	4A06 - " "
SPARE - 4B05	● ●	4A05 - " "
" - 4B04	● ●	4A04 - " "
" - 4B03	● ●	4A03 - " "
" - 4B02	● ●	4A02 - " "
" - 4B01	● ●	4A01 - " "

NOTE: BR 07 - BR 15 on the same pins on a 2nd I

P1 - CPU P852

SPARE - 1B37	● ●	1A37 - SPARE
" - 1B36	● ●	1A36 - "
" - 1B35	● ●	1A35 - "
" - 1B34	● ●	1A34 - "
" - 1B33	● ●	1A33 - "
" - 1B32	● ●	1A32 - "
" - 1B31	● ●	1A31 - "
" - 1B30	● ●	1A30 - "
" - 1B29	● ●	1A29 - "
" - 1B28	● ●	1A28 - "
" - 1B27	● ●	1A27 - "
" - 1B26	● ●	1A26 - "
" - 1B25	● ●	1A25 - "
" - 1B24	● ●	1A24 - "
" - 1B23	● ●	1A23 - "
" - 1B22	● ●	1A22 - "
" - 1B21	● ●	1A21 - "
" - 1B20	● ●	1A20 - "
" - 1B19	● ●	1A19 - "
" - 1B18	● ●	1A18 - "
" - 1B17	● ●	1A17 - "
" - 1B16	● ●	1A16 - "
" - 1B15	● ●	1A15 - "
" - 1B14	● ●	1A14 - "
" - 1B13	● ●	1A13 - "
" - 1B12	● ●	1A12 - INTASRN/IS 07N
IS 00N - 1B11	● ●	1A11 - IS 01N/PIFN
IS 07N - 1B10	● ●	1A10 - IS 03N
BIEC 0 - 1B09	● ●	1A09 - IS 06N/CPFN
BIEC 3 - 1B08	● ●	1A08 - BIEC 5
BIEC 1 - 1B07	● ●	1A07 - BIEC 2
RTCFZ1N - 1B06	● ●	1A06 - BIEC 4
IS 04N - 1B05	● ●	1A05 - PFFN/IS 00N
IS 05N - 1B04	● ●	1A04 - IS 02N/RTCAN
SCEIN - 1B03	● ●	1A03 - CPFN/IS 06N
RTCAN - 1B02	● ●	1A02 - PIFN/IS 01N
ASR LINE - 1B01	● ●	1A01 - 0 V



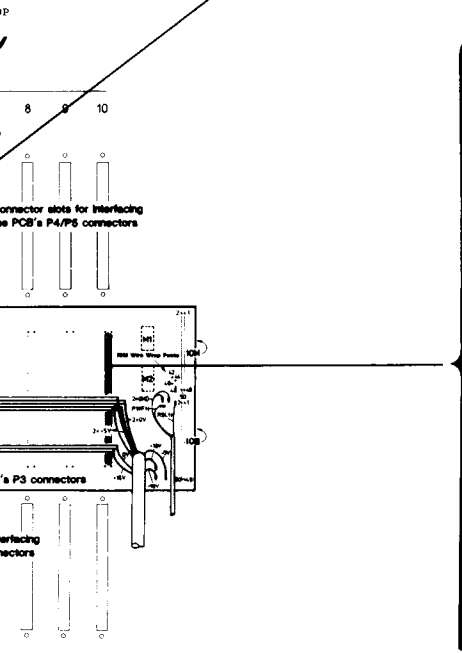
Rack Interfaces for Basic Control Units

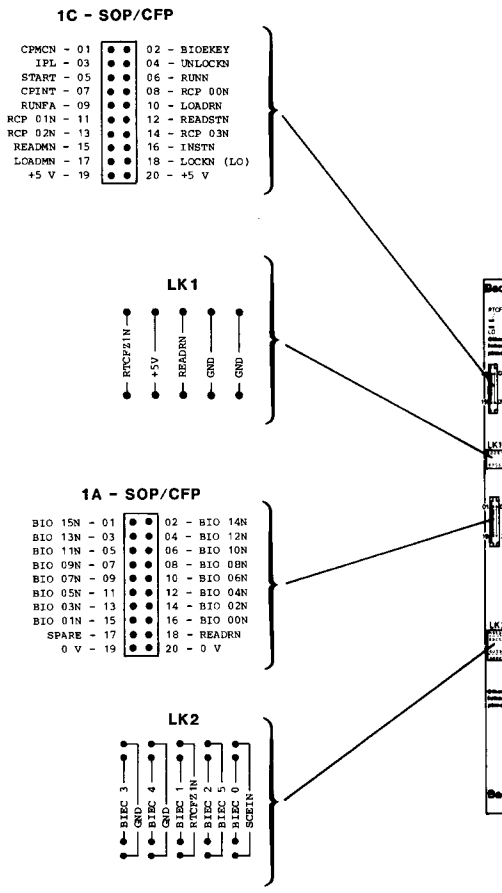
P5 - CHCR 6833

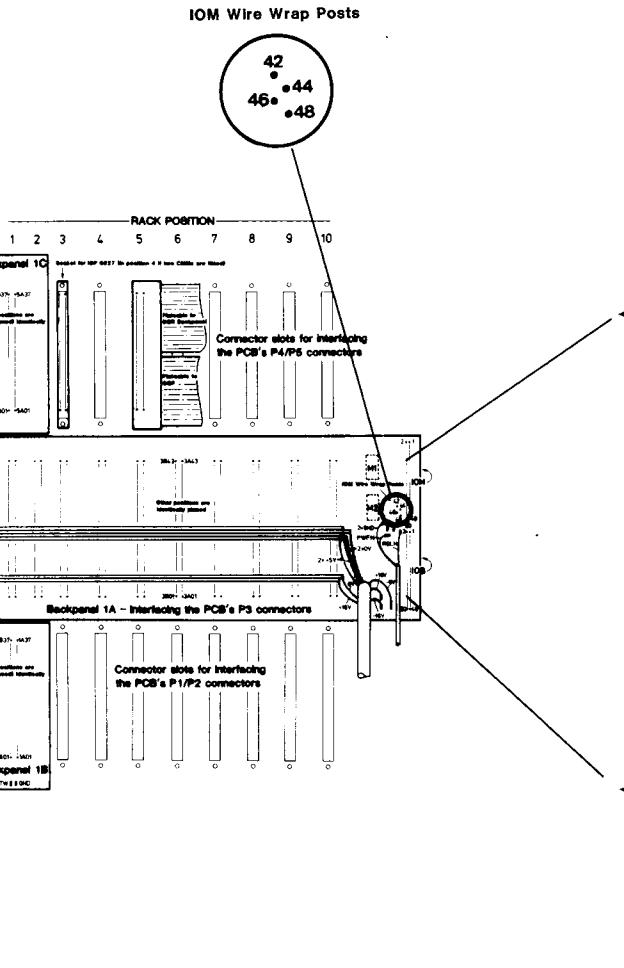
WEN 1N - 5B37	●	●	5A37 - WEN 0N
CIP 0N - 5B36	●	●	5A36 - GND
CIP 1N - 5B35	●	●	5A35 - RDY 0N
RDY 1N - 5B34	●	●	5A34 - GND
ABS 0N - 5B33	●	●	5A33 - "
ABS 1N - 5B32	●	●	5A32 - "
WDAN - 5B31	●	●	5A31 - "
BET 0N - 5B30	●	●	5A30 - "
BET 1N - 5B29	●	●	5A29 - "
RDA 0N - 5B28	●	●	5A28 - "
RDA 1N - 5B27	●	●	5A27 - "
FST - 5B26	●	●	5A26 - LCK 0
GND - 5B25	●	●	5A25 - LCK 1
REV - 5B24	●	●	5A24 - GND
FWD - 5B23	●	●	5A23 - SLT 0
GND - 5B22	●	●	5A22 - SLT 1
RGT - 5B21	●	●	5A21 - GND
RWD - 5B20	●	●	5A20 - "
WCD - 5B19	●	●	5A19 - LED 13N
+5 V - 5B18	●	●	5A18 - +5 V
LED 15N - 5B17	●	●	5A17 - LED 10N
LED 14N - 5B16	●	●	5A16 - SPARE
LED 12N - 5B15	●	●	5A15 - LED 11N
LED 09N - 5B14	●	●	5A14 - SPARE
LED 08N - 5B13	●	●	5A13 - "
LED 07N - 5B12	●	●	5A12 - "
LED 06N - 5B11	●	●	5A11 - LED 05N
DSW 06N - 5B10	●	●	5A10 - SPARE
CHAIN ENDN - 5B09	●	●	5A09 - "
DSW 07N - 5B08	●	●	5A08 - "
DSW 15N - 5B07	●	●	5A07 - CHAIN BEGINN
DSW 14N - 5B06	●	●	5A06 - SPARE
DSW 13N - 5B05	●	●	5A05 - "
SPARE - 5B04	●	●	5A04 - "
DSW 12N - 5B03	●	●	5A03 - "
DSW 11N - 5B02	●	●	5A02 - DSW 10N
DSW 09N - 5B01	●	●	5A01 - DSW 08N

P3 - GENERAL

M1/15 --- MAD 128 - 3B43	●	●	3A43 - BR
M1/14 --- MAD 64 - 3B42	●	●	3A42 - BR
M1/13 --- MAD 00 - 3B41	●	●	3A41 - BR
M1/12 --- MAD 01 - 3B40	●	●	3A40 - GND
M1/11 --- MAD 02 - 3B39	●	●	3A39 - CLEARN
MAD 03 - 3B38	●	●	3A38 - BSYN ----- M1/10
MAD 04 - 3B37	●	●	3A37 - MSN ------ M1/9
M1/5 ---- MAD 05 - 3B36	●	●	3A36 - BUSRN ---- M1/7
M1/4 ---- MAD 06 - 3B35	●	●	3A35 - SPYC ----- M1/6
M1/3 ---- MAD 07 - 3B34	●	●	3A34 - ACN
MAD 08 - 3B33	●	●	3A33 - GND
MAD 09 - 3B32	●	●	3A32 - TPMN
MAD 10 - 3B31	●	●	3A31 - TMPN
MAD 11 - 3B30	●	●	3A30 - TMEN
MAD 12 - 3B29	●	●	3A29 - TMRN ----- M2/15
MAD 13 - 3B28	●	●	3A28 - TRMN
MAD 14 - 3B27	●	●	3A27 - CHA ------ M2/13
MAD 15 - 3B26	●	●	3A26 - WRITE ---- M2/12
+16 V - 3B25	●	●	3A25 - GND
M1/M2 Ternets GND - 3B24	●	●	3A24 - GND
+5 V - 3B23	●	●	3A23 - BR
+5V (16) 0 V - 3B22	●	●	3A22 - 0 V
0 V - 3B21	●	●	3A21 - 0 V
220 +5 V - 3B20	●	●	3A20 - +5 V
+5 V - 3B19	●	●	3A19 - +5 V
-5 V - 3B18	●	●	3A18 - 0 V
330 RSLN - 3B17	●	●	3A17 - PWFN
OKI - 3B16	●	●	3A16 - OKO
(8) BIO 15N - 3B15	●	●	3A15 - BIO 14N
BIO 13N - 3B14	●	●	3A14 - BIO 12N
BIO 11N - 3B13	●	●	3A13 - BIO 10N
BIO 09N - 3B12	●	●	3A12 - BIO 08N
BIO 07N - 3B11	●	●	3A11 - BIO 06N
BIO 05N - 3B10	●	●	3A10 - BIO 04N
BIO 03N - 3B09	●	●	3A09 - BIO 02N
BIO 01N - 3B08	●	●	3A08 - BIO 00N
0 V - 3B07	●	●	3A07 - 0 V
+16 V - 3B06	●	●	3A06 - +16 V
BIEC 5 - 3B05	●	●	3A05 - SCEIN
BIEC 3 - 3B04	●	●	3A04 - BIEC 4
BIEC 1 - 3B03	●	●	3A03 - BIEC 2
Chassis GND - 3B02	●	●	3A02 - BIEC 0
-18 V - 3B01	●	●	3A01 - +18 V




1C - SOP/CFP
CPMCN - 01
IPL - 03
START - 05
CPINT - 07
RUNFA - 09
RCP 01N - 11
RCP 02N - 13
READMN - 15
LOADMN - 17
+5 V - 19
02 - BIOEKEY
04 - UNLOCKN
06 - RUNN
08 - RCP 00N
10 - LOADRN
12 - READSTN
14 - RCP 03N
16 - INSTN
18 - LOCKN (LO)
20 - +5 V
LK1
RTCPZ1N
+5V
READRN
GND
GND
1A - SOP/CFP
BIO 15N - 01
BIO 13N - 03
BIO 11N - 05
BIO 09N - 07
BIO 07N - 09
BIO 05N - 11
BIO 03N - 13
BIO 01N - 15
SPARE - 17
0 V - 19
02 - BIO 14N
04 - BIO 12N
06 - BIO 10N
08 - BIO 08N
10 - BIO 06N
12 - BIO 04N
14 - BIO 02N
16 - BIO 00N
18 - READRN
20 - 0 V
LK2
BIEC 3
GND
BIEC 4
GND
BIEC 1
RTCPZ1N
BIEC 2
BIEC 5
BIEC 0
SCEIN



IOM - EXU 6863

MAD 04	02	01	GND
MAD 03	04	03	"
MAD 08	06	05	"
MAD 09	08	07	"
MAD 10	10	09	"
MAD 11	12	11	"
MAD 12	14	13	"
MAD 13	16	15	"
MAD 14	18	17	"
MAD 15	20	19	"
ACN	22	21	"
GND	24	23	"
"	26	25	"
"	28	27	CLEARN
TPMN	30	29	GND
GND	32	31	"
"	34	33	TMPN
TMEN	36	35	GND
GND	38	37	"
"	40	39	TRMN
IOM Wire Wrap Post	42	41	GND
" " "	44	43	"
" " "	46	45	"
" " "	48	47	"
SPARE	50	49	"

IOB - EXU 6863

RSLN	02	01	GND
PWFN	04	03	"
BIO 15N	06	05	"
BIO 14N	08	07	"
BIO 13N	10	09	"
BIO 12N	12	11	"
BIO 11N	14	13	"
BIO 10N	16	15	"
BIO 09N	18	17	"
BIO 08N	20	19	"
BIO 07N	22	21	"
BIO 06N	24	23	"
BIO 05N	26	25	"
BIO 04N	28	27	"
BIO 03N	30	29	"
BIO 02N	32	31	"
BIO 01N	34	33	"
BIO 00N	36	35	"
BIEC 5	38	37	"
SCEIN	40	39	"
BIEC 3	42	41	"
BIEC 4	44	43	"
BIEC 1	46	45	"
BIEC 2	48	47	"
BIEC 0	50	49	"

P5 - CPU P852

INSTN - 5B37		5A37 - READRN
READMN - 5B36		5A36 - LOADMN
RCP 02N - 5B35		5A35 - RCP 03N
RCP 01N - 5B34		5A34 - READSTN
RUNFA - 5B33		5A33 - LOADRN
CPINT - 5B32		5A32 - RCP 00N
START - 5B31		5A31 - RUNN
IPL - 5B30		5A30 - UNLOCKN
CPMCN - 5B29		5A29 - BIOEKEY
SPARE - 5B28		5A28 - SPARE
" - 5B27		5A27 - "
" - 5B26		5A26 - "
" - 5B25		5A25 - "
" - 5B24		5A24 - "
" - 5B23		5A23 - "
" - 5B22		5A22 - "
" - 5B21		5A21 - "
" - 5B20		5A20 - "
" - 5B19		5A19 - "
" - 5B18		5A18 - "
" - 5B17		5A17 - "
" - 5B16		5A16 - "
" - 5B15		5A15 - "
" - 5B14		5A14 - "
" - 5B13		5A13 - "
" - 5B12		5A12 - "
" - 5B11		5A11 - "
" - 5B10		5A10 - "
" - 5B09		5A09 - "
" - 5B08		5A08 - "
" - 5B07		5A07 - "
" - 5B06		5A06 - "
" - 5B05		5A05 - "
" - 5B04		5A04 - "
" - 5B03		5A03 - "
" - 5B02		5A02 - "
" - 5B01		5A01 - "

P4/P5 - IOP 6827

NOT USED - 5B13		5A13 - NOT USED
" " - 5B12		5A12 - " "
" " - 5B11		5A11 - " "
" " - 5B10		5A10 - " "
" " - 5B09		5A09 - " "
" " - 5B08		5A08 - " "
" " - 5B07		5A07 - " "
" " - 5B06		5A06 - " "
" " - 5B05		5A05 - " "
" " - 5B04		5A04 - " "
" " - 5B03		5A03 - " "
" " - 5B02		5A02 - " "
" " - 5B01		5A01 - " "

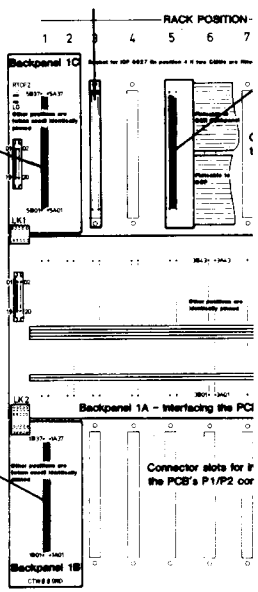
No board connector in this section

BR 00N - 4B13		4A13 - NOT USED
BR 01N - 4B12		4A12 - " "
BR 02N - 4B11		4A11 - " "
BR 03N - 4B10		4A10 - " "
BR 04N - 4B09		4A09 - " "
BR 05N - 4B08		4A08 - " "
BR 06N - 4B07		4A07 - " "
BR 07N - 4B06		4A06 - " "
SPARE - 4B05		4A05 - " "
" - 4B04		4A04 - " "
" - 4B03		4A03 - " "
" - 4B02		4A02 - " "
" - 4B01		4A01 - " "

NOTE: BR 07 - BR 15 on the same pins on a 2nd I

P1 - CPU P852

SPARE - 1B37		1A37 - SPARE
" - 1B36		1A36 - "
" - 1B35		1A35 - "
" - 1B34		1A34 - "
" - 1B33		1A33 - "
" - 1B32		1A32 - "
" - 1B31		1A31 - "
" - 1B30		1A30 - "
" - 1B29		1A29 - "
" - 1B28		1A28 - "
" - 1B27		1A27 - "
" - 1B26		1A26 - "
" - 1B25		1A25 - "
" - 1B24		1A24 - "
" - 1B23		1A23 - "
" - 1B22		1A22 - "
" - 1B21		1A21 - "
" - 1B20		1A20 - "
" - 1B19		1A19 - "
" - 1B18		1A18 - "
" - 1B17		1A17 - "
" - 1B16		1A16 - "
" - 1B15		1A15 - "
" - 1B14		1A14 - "
" - 1B13		1A13 - "
" - 1B12		1A12 - INTASRN/IS 07N
IS 00N - 1B11		1A11 - IS 01N/PIFN
IS 07N - 1B10		1A10 - IS 03N
BIEC 0 - 1B09		1A09 - IS 06N/CPFN
BIEC 3 - 1B08		1A08 - BIEC 5
BIEC 1 - 1B07		1A07 - BIEC 2
RTCFZ1N - 1B06		1A06 - BIEC 4
IS 04N - 1B05		1A05 - PFFN/IS 00N
IS 05N - 1B04		1A04 - IS 02N/RTCAN
SCEIN - 1B03		1A03 - CPFN/IS 06N
RTCAN - 1B02		1A02 - PIFN/IS 01N
ASR LINE - 1B01		1A01 - 0 V



Rack Interfaces for Basic Control Units

P5 - CHCR 6833

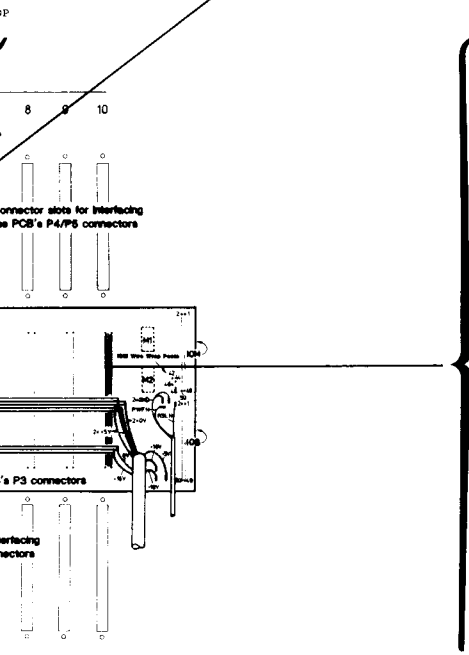
WEN 1N - 5B37	● ●	5A37 - WEN ON
CIP ON - 5B36	● ●	5A36 - GND
CIP 1N - 5B35	● ●	5A35 - RDY ON
RDY 1N - 5B34	● ●	5A34 - GND
ABS ON - 5B33	● ●	5A33 - "
ABS 1N - 5B32	● ●	5A32 - "
WDAN - 5B31	● ●	5A31 - "
BET ON - 5B30	● ●	5A30 - "
BET 1N - 5B29	● ●	5A29 - "
RDA ON - 5B28	● ●	5A28 - "
RDA 1N - 5B27	● ●	5A27 - "
FST - 5B26	● ●	5A26 - LCK 0
GND - 5B25	● ●	5A25 - LCK 1
REV - 5B24	● ●	5A24 - GND
FWD - 5B23	● ●	5A23 - SLT 0
GND - 5B22	● ●	5A22 - SLT 1
RGT - 5B21	● ●	5A21 - GND
RWD - 5B20	● ●	5A20 - "
WCD - 5B19	● ●	5A19 - LED 13N
+5 V - 5B18	● ●	5A18 - +5 V
LED 15N - 5B17	● ●	5A17 - LED 10N
LED 14N - 5B16	● ●	5A16 - SPARE
LED 12N - 5B15	● ●	5A15 - LED 11N
LED 09N - 5B14	● ●	5A14 - SPARE
LED 08N - 5B13	● ●	5A13 - "
LED 07N - 5B12	● ●	5A12 - "
LED 06N - 5B11	● ●	5A11 - LED 05N
DSW 06N - 5B10	● ●	5A10 - SPARE
CHAIN ENDN - 5B09	● ●	5A09 - "
DSW 07N - 5B08	● ●	5A08 - "
DSW 15N - 5B07	● ●	5A07 - CHAIN BEGINN
DSW 14N - 5B06	● ●	5A06 - SPARE
DSW 13N - 5B05	● ●	5A05 - "
SPARE - 5B04	● ●	5A04 - "
DSW 12N - 5B03	● ●	5A03 - "
DSW 11N - 5B02	● ●	5A02 - DSW 10N
DSW 09N - 5B01	● ●	5A01 - DSW 08N

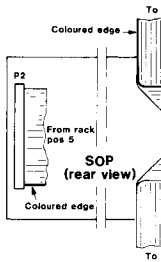
P3 - GENERAL

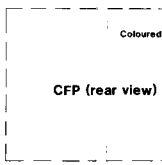
M1/15 --- MAD 128 - 3B43	● ●	3A43 - BR
M1/14 --- MAD 64 - 3B42	● ●	3A42 - BR
M1/13 --- MAD 00 - 3B41	● ●	3A41 - BR
M1/12 --- MAD 01 - 3B40	● ●	3A40 - GND
M1/11 --- MAD 02 - 3B39	● ●	3A39 - CLEARN
MAD 03 - 3B38	● ●	3A38 - BSYN ----- M1/10
MAD 04 - 3B37	● ●	3A37 - MSN ------ M1/9
M1/5 ---- MAD 05 - 3B36	● ●	3A36 - BUSRN ---- M1/7
M1/4 ---- MAD 06 - 3B35	● ●	3A35 - SPYC ----- M1/6
M1/3 ---- MAD 07 - 3B34	● ●	3A34 - ACN
MAD 08 - 3B33	● ●	3A33 - GND
MAD 09 - 3B32	● ●	3A32 - TPMN
MAD 10 - 3B31	● ●	3A31 - TMPN
MAD 11 - 3B30	● ●	3A30 - TMEN
MAD 12 - 3B29	● ●	3A29 - TMRN ----- M2/15
MAD 13 - 3B28	● ●	3A28 - TRMN
MAD 14 - 3B27	● ●	3A27 - CHA ------ M2/13
MAD 15 - 3B26	● ●	3A26 - WRITE ---- M2/12
+16 V - 3B25	● ●	3A25 - GND
GND - 3B24	● ●	3A24 - GND
+5 V - 3B23	● ●	3A23 - BR
0 V - 3B22	● ●	3A22 - 0 V
0 V - 3B21	● ●	3A21 - 0 V
+5 V - 3B20	● ●	3A20 - +5 V
+5 V - 3B19	● ●	3A19 - +5 V
-5 V - 3B18	● ●	3A18 - 0 V
RSLN - 3B17	● ●	3A17 - PWFN
OKI - 3B16	● ●	3A16 - OKO
BIO 15N - 3B15	● ●	3A15 - BIO 14N
BIO 13N - 3B14	● ●	3A14 - BIO 12N
BIO 11N - 3B13	● ●	3A13 - BIO 10N
BIO 09N - 3B12	● ●	3A12 - BIO 08N
BIO 07N - 3B11	● ●	3A11 - BIO 06N
BIO 05N - 3B10	● ●	3A10 - BIO 04N
BIO 03N - 3B09	● ●	3A09 - BIO 02N
BIO 01N - 3B08	● ●	3A08 - BIO 00N
0 V - 3B07	● ●	3A07 - 0 V
+16 V - 3B06	● ●	3A06 - +16 V
BIEC 5 - 3B05	● ●	3A05 - SCEIN
BIEC 3 - 3B04	● ●	3A04 - BIEC 4
BIEC 1 - 3B03	● ●	3A03 - BIEC 2
Chassis GND - 3B02	● ●	3A02 - BIEC 0
-18 V - 3B01	● ●	3A01 - +18 V

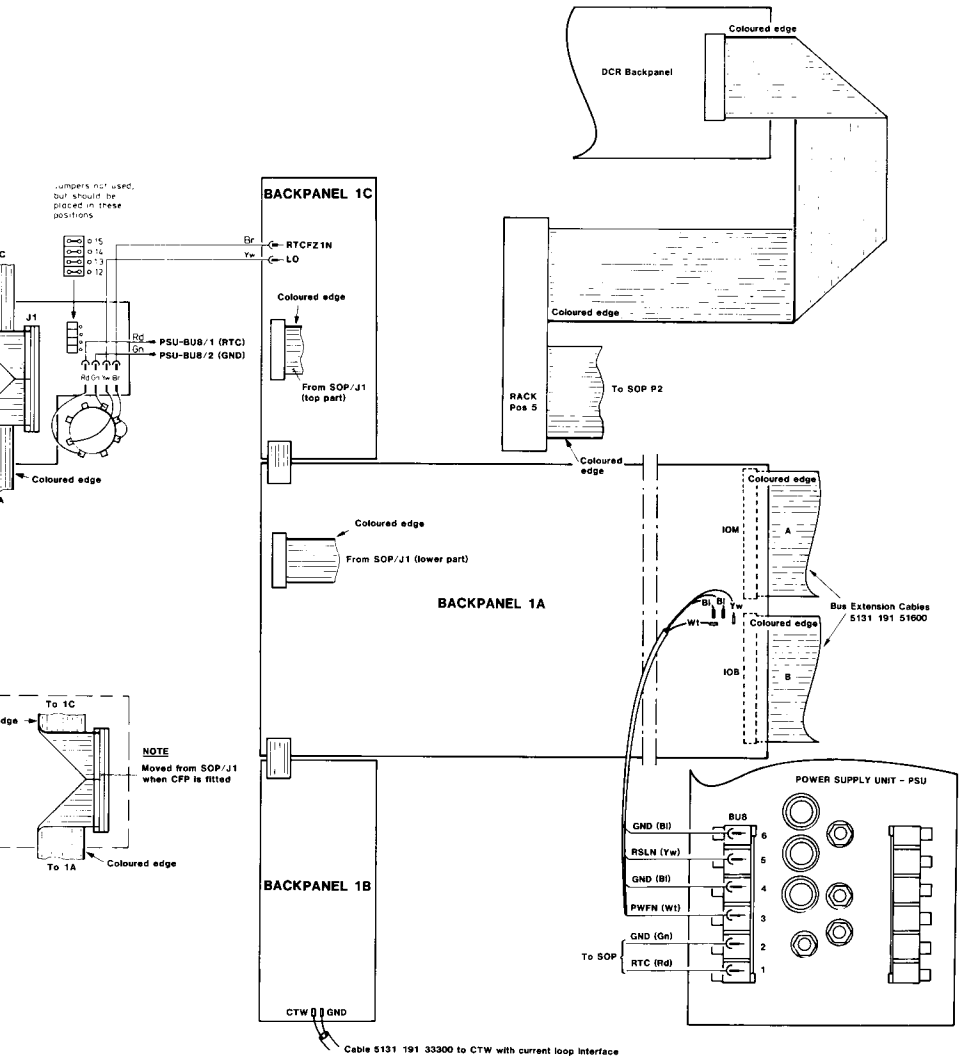
M1/M2 Ternets

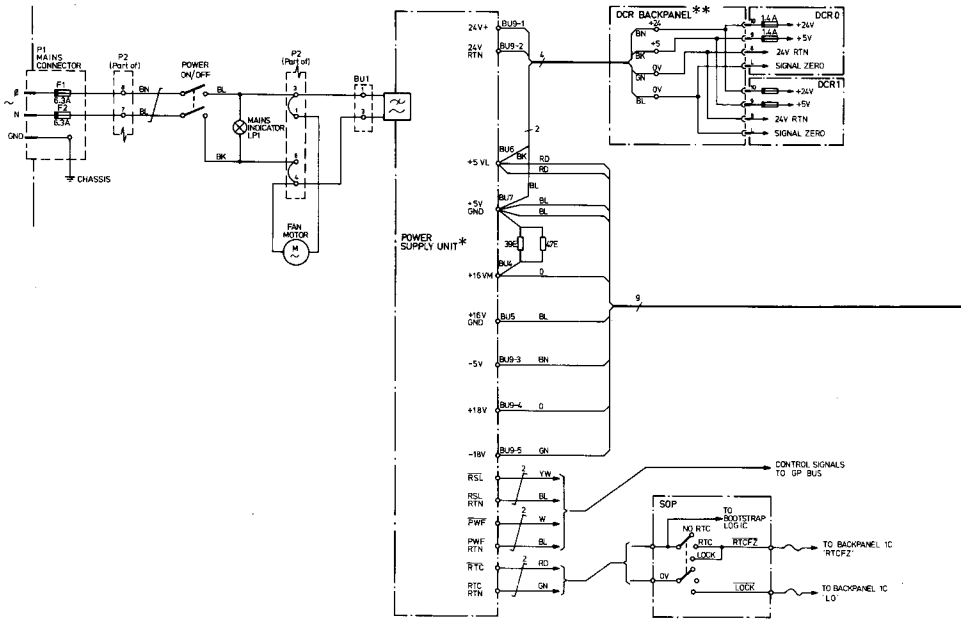
+5V (16) — 220 — 330 — (8)




To
Coloured edge
P2
From rack pos 5
SOP (rear view)
Coloured edge
To

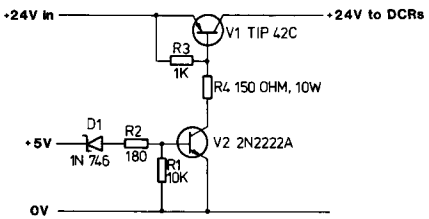

Coloured
CFP (rear view)


Coloured edge
DCR Backpanel
Coloured edge
BACKPANEL 1C
Jumpers not used, but should be placed in these positions
Br
Yw
RTCFZ1N
LO
Coloured edge
From SOP/J1 (top part)
J1
Rd
Gn
PSU-BU8/1 (RTC)
PSU-BU8/2 (GND)
Coloured edge
RACK Pos 5
To SOP P2
Coloured edge
Coloured edge
From SOP/J1 (lower part)
BACKPANEL 1A
Coloured edge
IOM
A
Bl
Bl
Yw
Wt
Bus Extension Cables 5131 191 51600
Coloured edge
IOB
B
To 1C
NOTE
Moved from SOP/J1 when CFP is fitted
To 1A
Coloured edge
POWER SUPPLY UNIT - PSU
BU8
GND (Bl)
RSLN (Yw)
GND (Bl)
PWFN (Wt)
GND (Gn)
RTC (Rd)
To SOP
6
5
4
3
2
1
BACKPANEL 1B
CTW
GND
Cable 5131 191 33300 to CTW with current loop interface

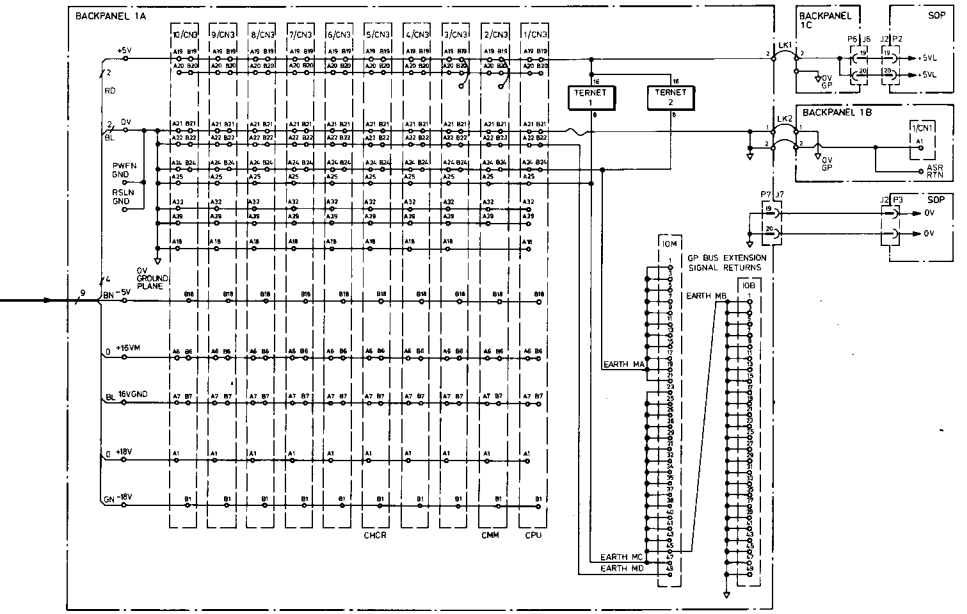


*Type PE 1440 or PE 1709/01, 02

**Backpanels for DCR 6865 are equipped with the following control circuit for 24V

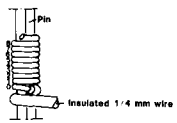


D1 = ZENER

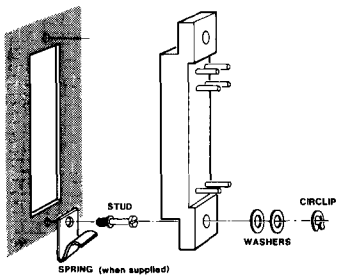

BACKPANEL 1A
10/CN3
9/CN3
8/CN3
7/CN3
6/CN3
5/CN3
4/CN3
3/CN3
2/CN3
1/CN3
+5V
RD
0V
BL
PWFN GND
RSLN GND
0V GROUND PLANE
-5V
BN
+15VM
BL
15VGND
+18V
GN
-18V
CHCR
CMM
CPU
TERNET 1
TERNET 2
BACKPANEL 1C
LK1
P6
J6
J2
P2
+5VL
+5VL
0V GP
BACKPANEL 1B
LK2
1/CN1
A1
0V GP
ASR RTN
P7
J7
J2
P3
SOP
0V
0V
10M
GP BUS EXTENSION SIGNAL RETURNS
EARTH MB
10B
EARTH MA
EARTH MC
EARTH MD

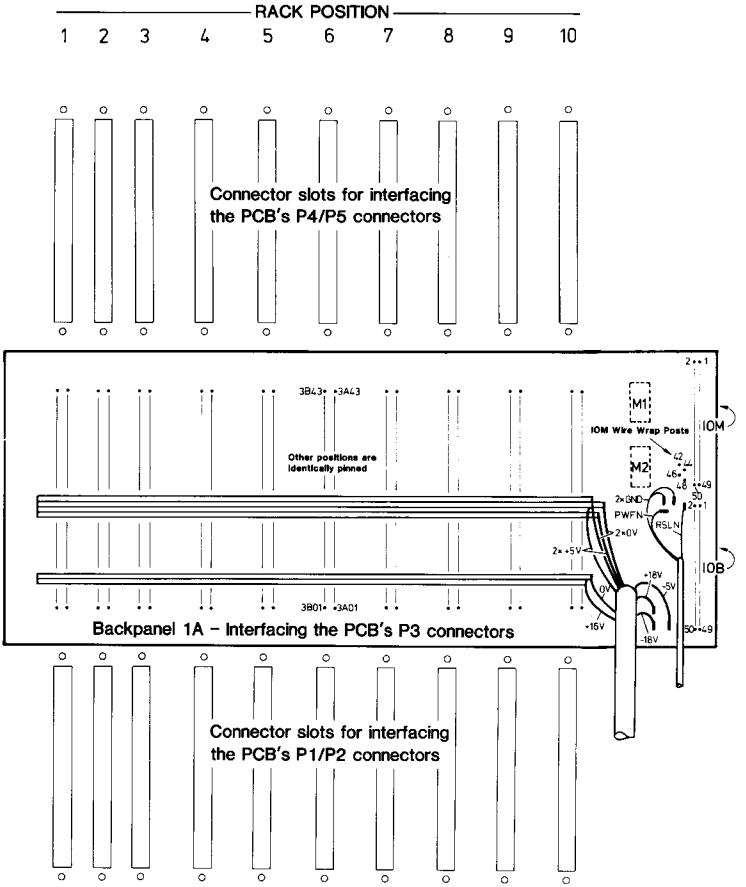
INSTALLING RACK BACKPANEL OPTIONS

Additional wire wrap connections

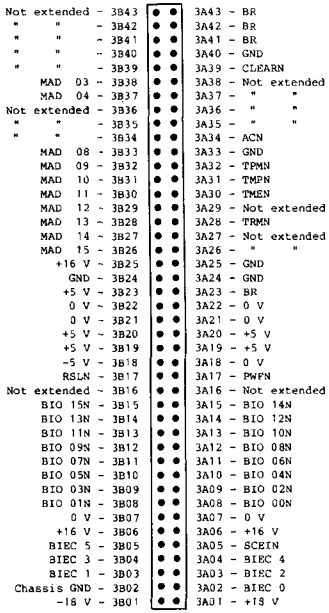


Socket for P1/P2 or P4/P5 connectors

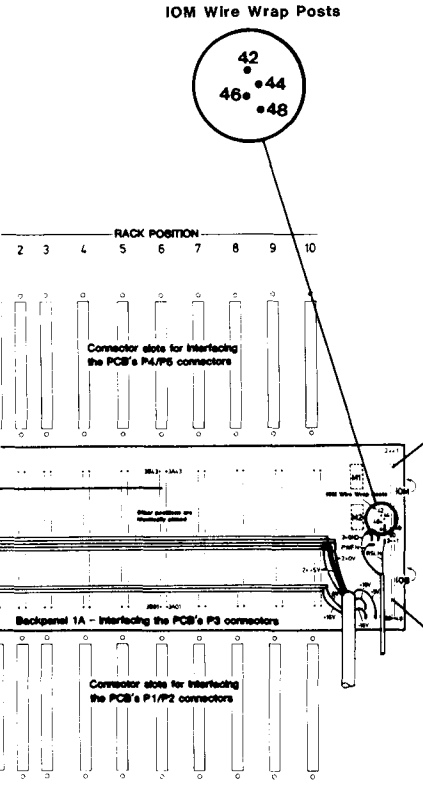



RACK POSITION
1 2 3 4 5 6 7 8 9 10
Connector slots for interfacing the PCB's P4/P5 connectors
3B43 • 3A43
Other positions are identically pinned
M1
M2
IOM Wire Wrap Posts
IOM
IOB
2 • GND
PWFN
RSLN
2 • 0V
2 • +5V
+18V
-5V
0V
+16V
-16V
3B01 • 3A01
Backpanel 1A – Interfacing the PCB's P3 connectors
Connector slots for interfacing the PCB's P1/P2 connectors

P3 - GENERAL



NOTE: All extended bus signals are terminated on the Termination Board in rack position 1/2.

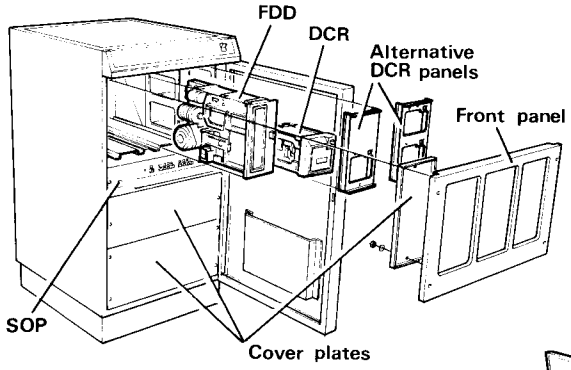


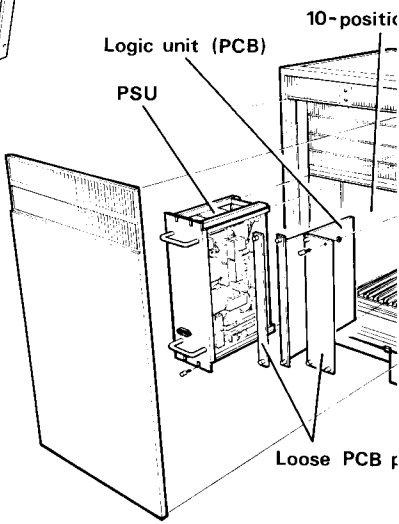
IOM - TC 6810/11

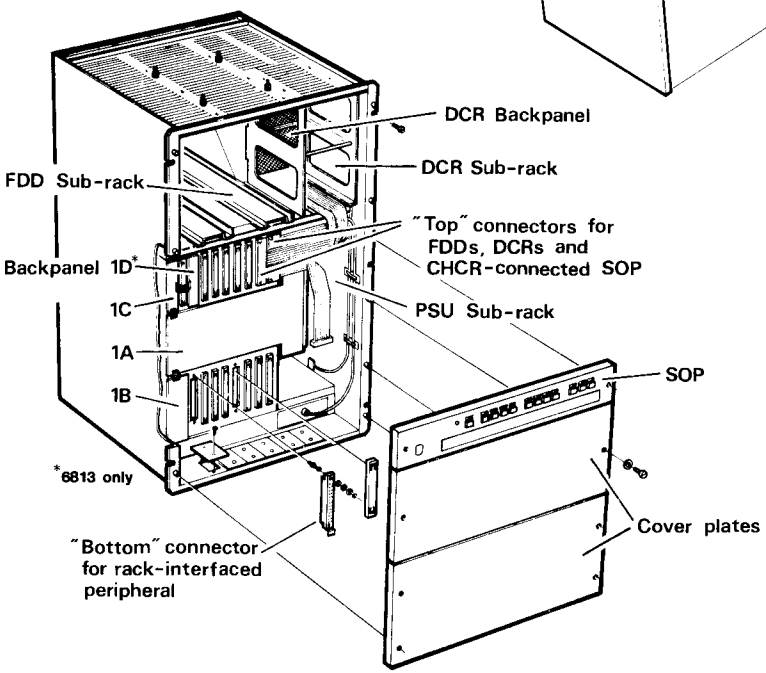
MAD 04 ~ 02	● ●	01 ~ GND
MAD 03 ~ 04	● ●	03 ~ "
MAD 08 ~ 06	● ●	05 ~ "
MAD 09 ~ 08	● ●	07 ~ "
MAD 10 ~ 10	● ●	09 ~ "
MAD 11 ~ 12	● ●	11 ~ "
MAD 12 ~ 14	● ●	13 ~ "
MAD 13 ~ 16	● ●	15 ~ "
MAD 14 ~ 18	● ●	17 ~ "
MAD 15 ~ 20	● ●	19 ~ "
ACN ~ 22	● ●	21 ~ "
GND ~ 24	● ●	23 ~ "
" ~ 26	● ●	25 ~ "
" ~ 28	● ●	27 ~ CLEARN
TPMN ~ 30	● ●	29 ~ GND
GND ~ 32	● ●	31 ~ "
" ~ 34	● ●	33 ~ TMPN
TMEN ~ 36	● ●	35 ~ GND
GND ~ 38	● ●	37 ~ "
" ~ 40	● ●	39 ~ TRMN
IOM Wire Wrap Post ~ 42	● ●	41 ~ GND
" " " " ~ 44	● ●	43 ~ "
" " " " ~ 46	● ●	45 ~ "
" " " " ~ 48	● ●	47 ~ "
SPARE ~ 50	● ●	49 ~ "

IOB - TC 6810/11

RSLN ~ 02	● ●	01 ~ GND
PWFN ~ 04	● ●	03 ~ "
BIO 15N ~ 06	● ●	05 ~ "
BIO 14N ~ 08	● ●	07 ~ "
BIO 13N ~ 10	● ●	09 ~ "
BIO 12N ~ 12	● ●	11 ~ "
BIO 11N ~ 14	● ●	13 ~ "
BIO 10N ~ 16	● ●	15 ~ "
BIO 09N ~ 18	● ●	17 ~ "
BIO 08N ~ 20	● ●	19 ~ "
BIO 07N ~ 22	● ●	21 ~ "
BIO 06N ~ 24	● ●	23 ~ "
BIO 05N ~ 26	● ●	25 ~ "
BIO 04N ~ 28	● ●	27 ~ "
BIO 03N ~ 30	● ●	29 ~ "
BIO 02N ~ 32	● ●	31 ~ "
BIO 01N ~ 34	● ●	33 ~ "
BIO 00N ~ 36	● ●	35 ~ "
BIEC 5 ~ 38	● ●	37 ~ "
SCEIN ~ 40	● ●	39 ~ "
BIEC 3 ~ 42	● ●	41 ~ "
BIEC 4 ~ 44	● ●	43 ~ "
BIEC 1 ~ 46	● ●	45 ~ "
BIEC 2 ~ 48	● ●	47 ~ "
BIEC 0 ~ 50	● ●	49 ~ "


FDD
DCR
Alternative
DCR panels
Front panel
SOP
Cover plates


10-positio
Logic unit (PCB)
PSU
Loose PCB p

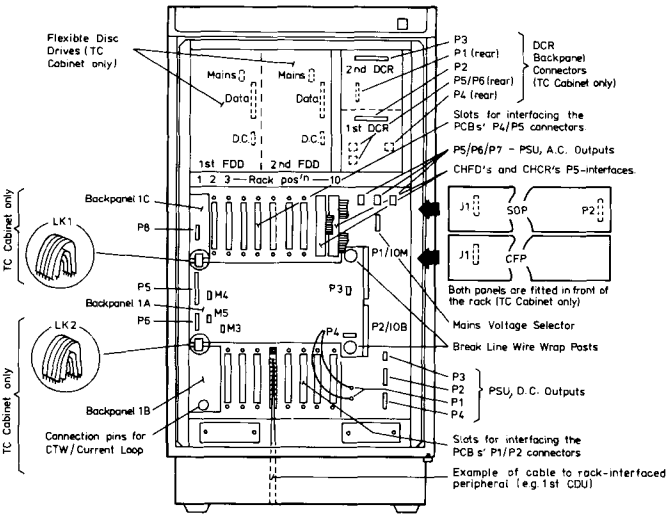

DCR Backpanel
DCR Sub-rack
FDD Sub-rack
"Top" connectors for
FDDs, DCRs and
CHCR-connected SOP
Backpanel 1D*
1C
PSU Sub-rack
1A
SOP
1B
*6813 only
Cover plates
"Bottom" connector
for rack-interfaced
peripheral

Physical Structure

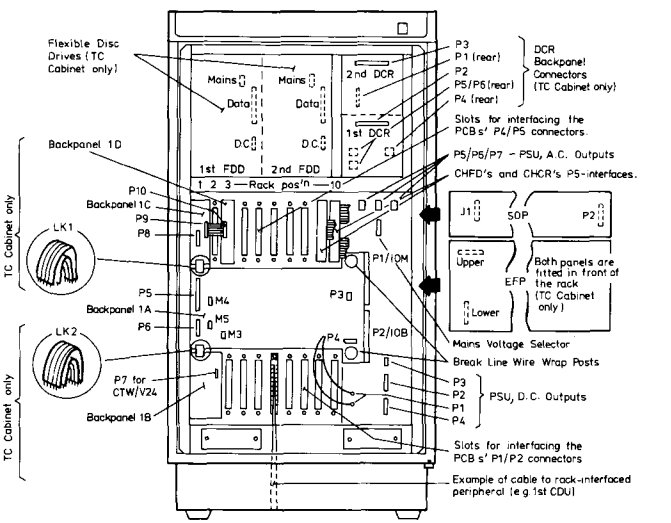
n Rack

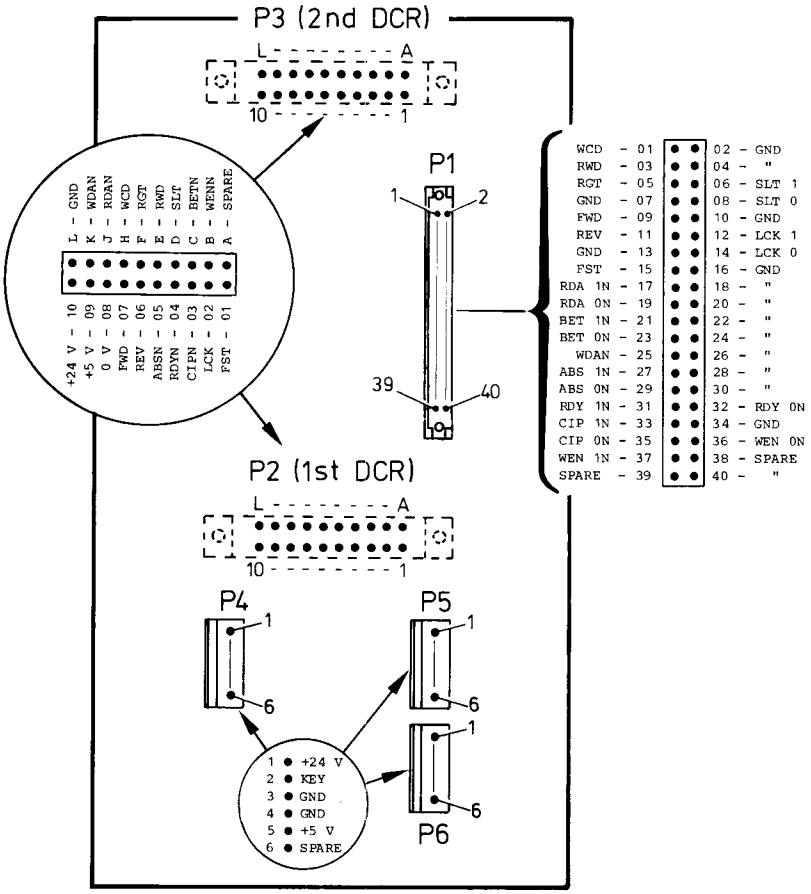
anels

TC 6812 & EXU 6864

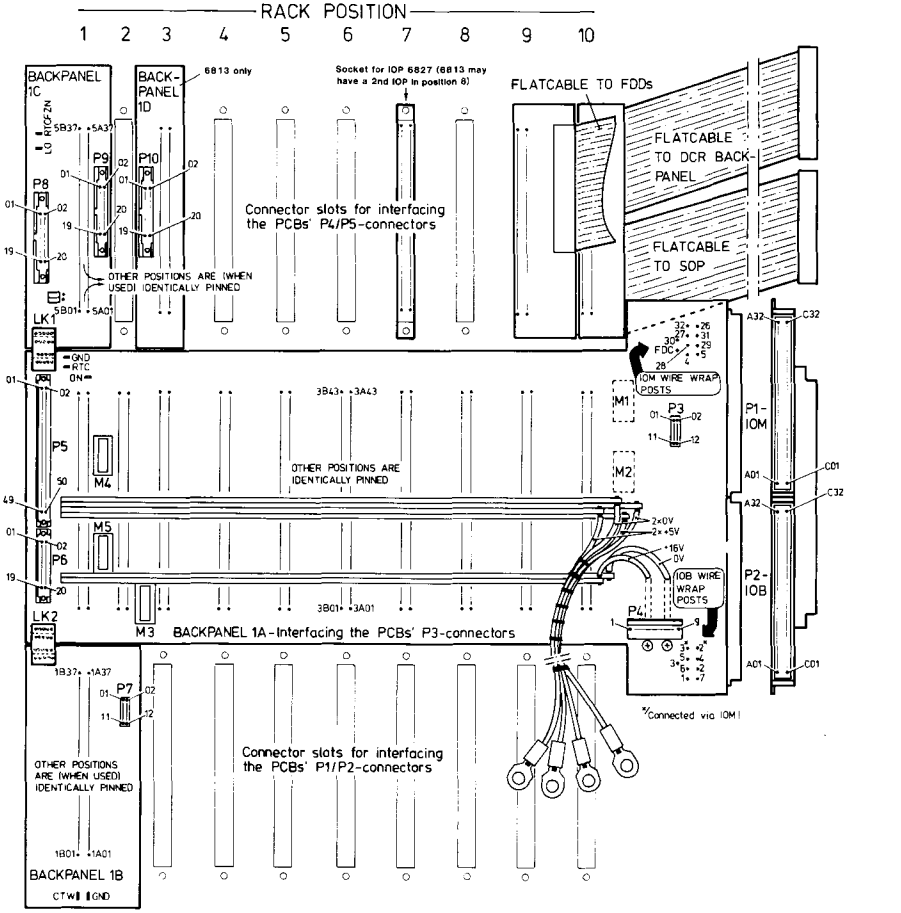


TC 6813 & EXU 6864



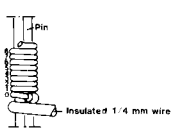


The control circuit for 24V (fitted on the panel) is shown on the sheet Power Distribution

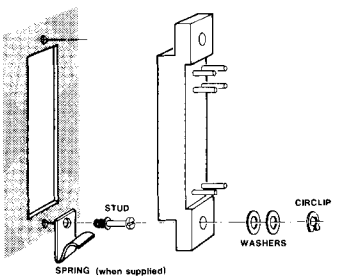


INSTALLING RACK BACKPANEL OPTIONS

Additional wire wrap connections



Socket for P1/P2 or P4/P5 connectors



P5 - CPU P852/57

INSTN - 5B37		5A37 - READRN
READMN - 5B36		5A36 - LOADMN
RCP 02N - 5B35		5A35 - RCP 03N
RCP 01N - 5B34		5A34 - READSTN
RUNFA - 5B33		5A33 - LOADRN
CPINT - 5B32		5A32 - RCP 00N
START - 5B31		5A31 - RUNN
IPL - 5B30		5A30 - UNLOCKN
CPMCN - 5B29		5A29 - BIOEKEY
+5 V - 5B28		5A28 - +5 V
0 V - 5B27		5A27 - 0 V
SPARE - 5B26		5A26 - SPARE
TMMU - 5B25		5A25 - SP 02
TMMN - 5B24		5A24 - S 03
S 02 - 5B23		5A23 - S 01
S 00 - 5B22		5A22 - FU
SPARE - 5B21		5A21 - BOMFN
MFAULTN - 5B20		5A20 - DONEMN
SPARE - 5B19		5A19 - MMUABS
" - 5B18		5A18 - SPARE
MOSCFLO - 5B17		5A17 - OSCFLO
SPARE - 5B16		5A16 - SPARE
FPPABS - 5B15		5A15 - FLOCR1
PLOCRO - 5B14		5A14 - DONEFN
BOFFN - 5B13		5A13 - GFETCH
TMFN - 5B12		5A12 - BSYCPUAN
SP 01 - 5B11		5A11 - FLOACTN
SP 04 - 5B10		5A10 - SP 03
SPARE - 5B09		5A09 - SPARE
" - 5B08		5A08 - "
" - 5B07		5A07 - "
" - 5B06		5A06 - "
TESTN - 5B05		5A05 - "
CPBABS - 5B04		5A04 - "
PREQN - 5B03		5A03 - "
GBCPFN - 5B02		5A02 - "
SP 05 - 5B01		5A01 - "

5A/5B01-5A/5B28 applicable only for PTS 6813.

P5 - MMU 6828 (6813 only)

SPARE - 5B37		5A37 - SPARE
" - 5B36		5A36 - "
" - 5B35		5A35 - "
" - 5B34		5A34 - "
" - 5B33		5A33 - "
" - 5B32		5A32 - "
" - 5B31		5A31 - "
" - 5B30		5A30 - "
" - 5B29		5A29 - "
" - 5B28		5A28 - "
" - 5B27		5A27 - "
" - 5B26		5A26 - "
TMMU - 5B25		5A25 - "
TMMN - 5B24		5A24 - S 03
S 02 - 5B23		5A23 - S 01
S 00 - 5B22		5A22 - FU
SPARE - 5B21		5A21 - BOMFN
MFAULTN - 5B20		5A20 - DONEMN
SPARE - 5B19		5A19 - MMUABS
" - 5B18		5A18 - SPARE
GND - 5B17		5A17 - OSCFLO
SPARE - 5B16		5A16 - SPARE
" - 5B15		5A15 - "
" - 5B14		5A14 - "
" - 5B13		5A13 - GFETCH
" - 5B12		5A12 - BSYCPUAN
" - 5B11		5A11 - SPARE
" - 5B10		5A10 - "
" - 5B09		5A09 - "
" - 5B08		5A08 - "
" - 5B07		5A07 - "
" - 5B06		5A06 - "
" - 5B05		5A05 - "
" - 5B04		5A04 - "
" - 5B03		5A03 - "
" - 5B02		5A02 - "
" - 5B01		5A01 - "

P4/P5 -

NOT USED - 5B13	
" " - 5B12	
" " - 5B11	
" " - 5B10	
" " - 5B09	
" " - 5B08	
" " - 5B07	
" " - 5B06	
" " - 5B05	
" " - 5B04	
" " - 5B03	
" " - 5B02	
" " - 5B01	

No board conne

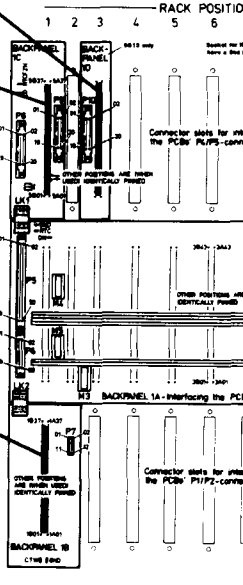
BR 00N - 4B13	
BR 01N - 4B12	
BR 02N - 4B11	
BR 03N - 4B10	
BR 04N - 4B09	
BR 05N - 4B08	
BR 06N - 4B07	
BR 07N - 4B06	
SPARE - 4B05	
" - 4B04	
" - 4B03	
" - 4B02	
" - 4B01	

NOTE: BR 07 - BR 15 on

P1 - CPU P852/57

GND - 1B37		1A37 - CT 133
" - 1B36		1A36 - CT 109
" - 1B35		1A35 - CT 107
" - 1B34		1A34 - CT 108
" - 1B33		1A33 - CT 106
" - 1B32		1A32 - CT 103
" - 1B31		1A31 - CT 104
SPARE - 1B30		1A30 - GND
" - 1B29		1A29 - SPARE
" - 1B28		1A28 - "
" - 1B27		1A27 - "
" - 1B26		1A26 - "
" - 1B25		1A25 - "
" - 1B24		1A24 - "
" - 1B23		1A23 - "
" - 1B22		1A22 - "
" - 1B21		1A21 - "
" - 1B20		1A20 - "
" - 1B19		1A19 - "
" - 1B18		1A18 - "
" - 1B17		1A17 - "
" - 1B16		1A16 - "
" - 1B15		1A15 - "
" - 1B14		1A14 - "
" - 1B13		1A13 - "
" - 1B12		1A12 - INTASRN/IS 07N
ISOON/PFFN - 1B11		1A11 - IS 01N/PIFN
ISO7N/INTASR- 1B10		1A10 - IS 03N
BIEC 0 - 1B09		1A09 - IS 06N/CPFN
BIEC 3 - 1B08		1A08 - BIEC 5
BIEC 1 - 1B07		1A07 - BIEC 2
RTCFZIN - 1B06		1A06 - BIEC 4
IS 04N - 1B05		1A05 - PFFN/IS 00N
IS 05N - 1B04		1A04 - IS 02N/RTCAN
SCRIN - 1B03		1A03 - CPFN/IS 06N
RTCAN/ISO2 - 1B02		1A02 - PIFN/IS 01N
ASR LINE - 1B01		1A01 - 0 V

PTS 6813 only



Rack Interfaces for Basic Control Units

IOP 6827

5A13	NOT USED
5A12	" "
5A11	" "
5A10	" "
5A09	" "
5A08	" "
5A07	" "
5A06	" "
5A05	" "
5A04	" "
5A03	" "
5A02	" "
5A01	" "

or in this section

4A13	NOT USED
4A12	" "
4A11	" "
4A10	" "
4A09	" "
4A08	" "
4A07	" "
4A06	" "
4A05	" "
4A04	" "
4A03	" "
4A02	" "
4A01	" "

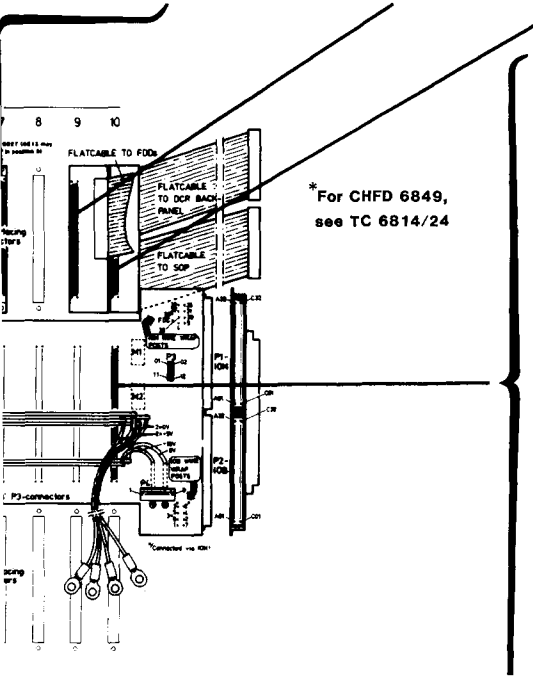
he same pins on a 2nd IOP

P5 - CHFD 6848*

SPARE - 5B37	5A37	- RDLN
" - 5B36	5A36	- HEADLN
" - 5B35	5A35	- TRON
" - 5B34	5A34	- INDN
" - 5B33	5A33	- LWCN
" - 5B32	5A32	- STEPN
" - 5B31	5A31	- DIRN
" - 5B30	5A30	- WEN
" - 5B29	5A29	- WDLN
" - 5B28	5A28	- SEL 0N
" - 5B27	5A27	- SEL 1N
" - 5B26	5A26	- SEL 2N
" - 5B25	5A25	- SEL 3N
" - 5B24	5A24	- SPARE
" - 5B23	5A23	- "
" - 5B22	5A22	- "
" - 5B21	5A21	- "
" - 5B20	5A20	- "
" - 5B19	5A19	- "
" - 5B18	5A18	- "
" - 5B17	5A17	- "
" - 5B16	5A16	- "
" - 5B15	5A15	- "
" - 5B14	5A14	- "
" - 5B13	5A13	- "
" - 5B12	5A12	- RDY 0N
" - 5B11	5A11	- RDY 1N
" - 5B10	5A10	- RDY 2N
" - 5B09	5A09	- RDY 3N
" - 5B08	5A08	- WRPN
" - 5B07	5A07	- SPARE
" - 5B06	5A06	- UNLOCK 0N
" - 5B05	5A05	- UNLOCK 1N
" - 5B04	5A04	- SPARE
" - 5B03	5A03	- "
" - 5B02	5A02	- UNLOCK 2N
" - 5B01	5A01	- UNLOCK 3N

P5 - CHCR 6833

WEN 1N - 5B37	5A37	- WEN 0N
CIP 0N - 5B36	5A36	- GND
CIP 1N - 5B35	5A35	- RDY 0N
RDY 1N - 5B34	5A34	- GND
ABS 0N - 5B33	5A33	- "
ABS 1N - 5B32	5A32	- "
WDAN - 5B31	5A31	- "
BET 0N - 5B30	5A30	- "
BET 1N - 5B29	5A29	- "
RDA 0N - 5B28	5A28	- "
RDA 1N - 5B27	5A27	- "
FST - 5B26	5A26	- LCK 0
GND - 5B25	5A25	- LCK 1
REV - 5B24	5A24	- GND
FWD - 5B23	5A23	- SLT 0
GND - 5B22	5A22	- SLT 1
RGT - 5B21	5A21	- GND
RWD - 5B20	5A20	- "
WCD - 5B19	5A19	- LED 13N
+5 V - 5B18	5A18	- +5 V
LED 15N - 5B17	5A17	- LED 10N
LED 14N - 5B16	5A16	- SPARE
LED 12N - 5B15	5A15	- LED 11N
LED 09N - 5B14	5A14	- SPARE
LED 08N - 5B13	5A13	- "
LED 07N - 5B12	5A12	- "
LED 06N - 5B11	5A11	- LED 05N
DSW 06N - 5B10	5A10	- SPARE
CHAIN ENDN - 5B09	5A09	- "
DSW 07N - 5B08	5A08	- "
DSW 15N - 5B07	5A07	- CHAIN BEGINN
DSW 14N - 5B06	5A06	- SPARE
DSW 13N - 5B05	5A05	- "
SPARE - 5B04	5A04	- "
DSW 12N - 5B03	5A03	- "
DSW 11N - 5B02	5A02	- DSW 10N
DSW 09N - 5B01	5A01	- DSW 08N

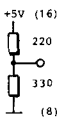


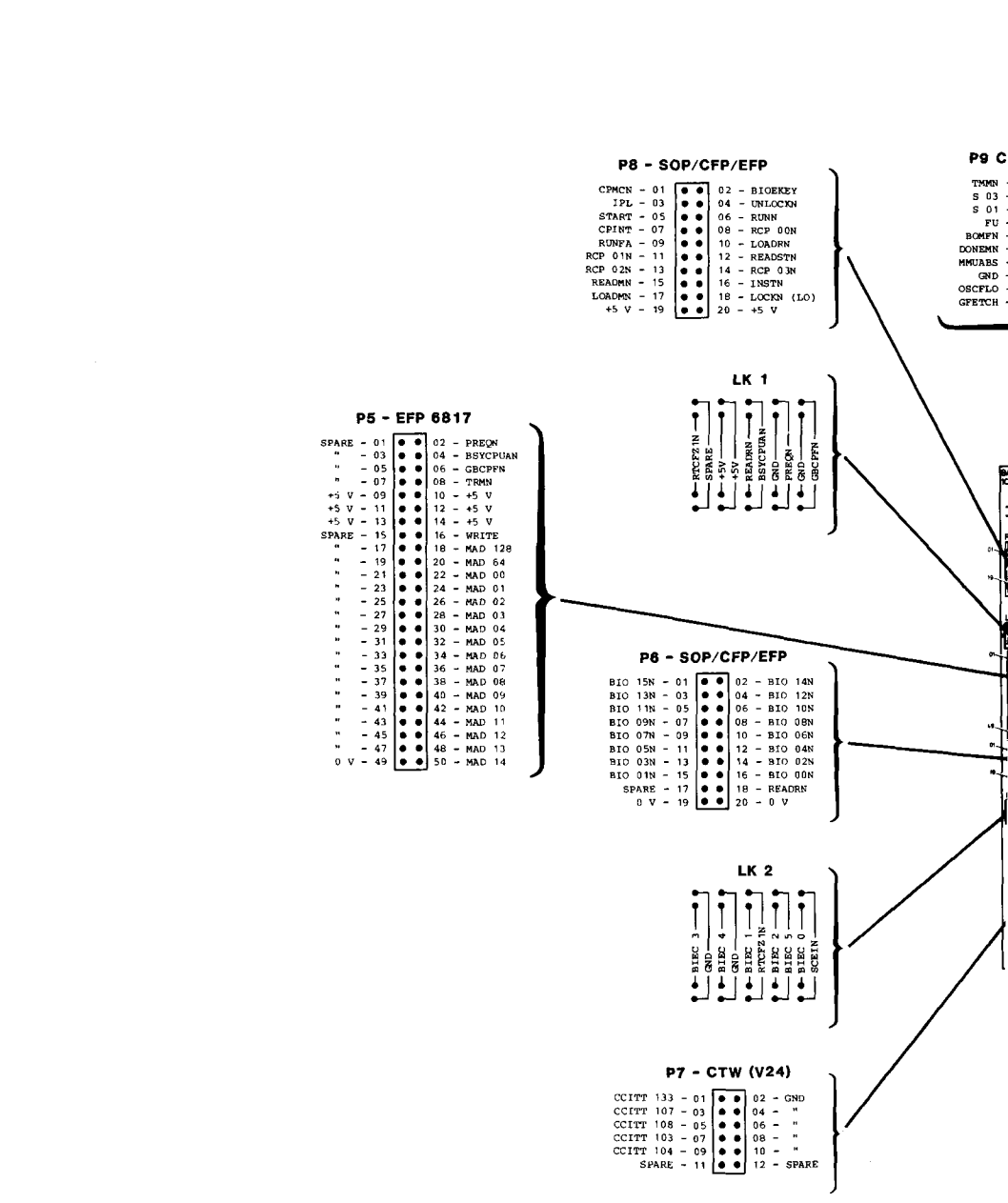
*For CHFD 6849, see TC 6814/24

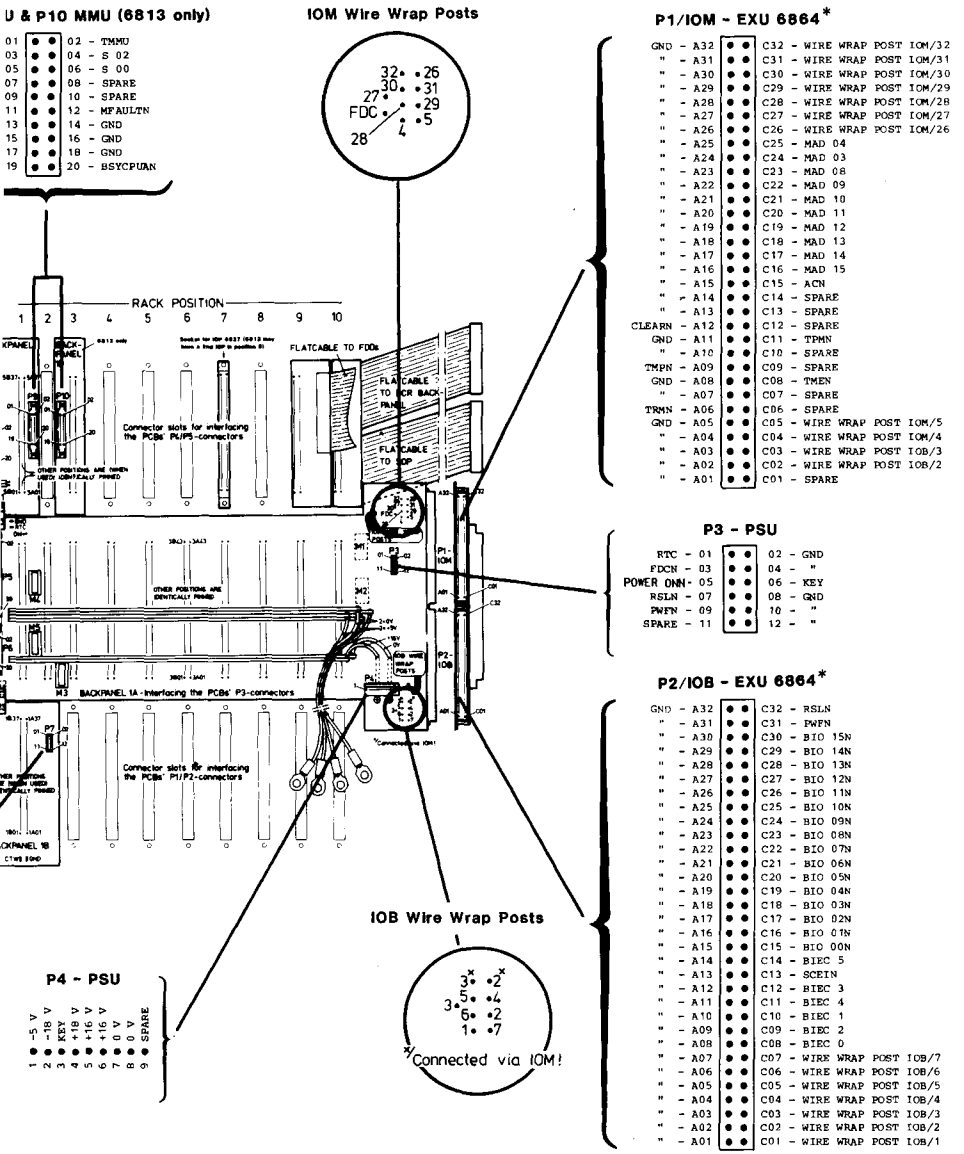
P3 - GENERAL

M1/15 --- MAD 128 - 3B43	3A43	- BR	
M1/14 --- MAD 64 - 3B42	3A42	- BR	
M1/13 --- MAD 00 - 3B41	3A41	- BR	
M1/12 --- MAD 01 - 3B40	3A40	- GND	
M1/11 --- MAD 02 - 3B39	3A39	- CLEARN	
MAD 03 - 3B38	3A38	- BSYN -----	M1/1C
MAD 04 - 3B37	3A37	- MSN ------	M1/9
M1/5 ---- MAD 05 - 3B36	3A36	- BUSRN ----	M1/7
M1/4 ---- MAD 06 - 3B35	3A35	- SPYC -----	M1/6
M1/3 ---- MAD 07 - 3B34	3A34	- ACN	
MAD 08 - 3B33	3A33	- GND	
MAD 09 - 3B32	3A32	- TPMN	
MAD 10 - 3B31	3A31	- TMPN	
MAD 11 - 3B30	3A30	- TMEN	
MAD 12 - 3B29	3A29	- TMRN -----	M2/15
MAD 13 - 3B28	3A28	- TRMN	
MAD 14 - 3B27	3A27	- CHA ------	M2/13
MAD 15 - 3B26	3A26	- WRITE ----	M2/12
+16 V - 3B25	3A25	- GND	
GND - 3B24	3A24	- GND	
+5 V - 3B23	3A23	- BR	
0 V - 3B22	3A22	- 0 V	
0 V - 3B21	3A21	- 0 V	
+5 V - 3B20	3A20	- +5 V	
+5 V - 3B19	3A19	- +5 V	
-5 V - 3B18	3A18	- 0 V	
RSLN - 3B17	3A17	- PWFN	
OKI - 3B16	3A16	- OKO	
BIO 15N - 3B15	3A15	- BIO 14N	
BIO 13N - 3B14	3A14	- BIO 12N	
BIO 11N - 3B13	3A13	- BIO 10N	
BIO 09N - 3B12	3A12	- BIO 08N	
BIO 07N - 3B11	3A11	- BIO 06N	
BIO 05N - 3B10	3A10	- BIO 04N	
BIO 03N - 3B09	3A09	- BIO 02N	
BIO 01N - 3B08	3A08	- BIO 00N	
0 V - 3B07	3A07	- 0 V	
+16 V - 3B06	3A06	- +16 V	
BIEC 5 - 3B05	3A05	- SCEIN	
BIEC 3 - 3B04	3A04	- BIEC 4	
BIEC 1 - 3B03	3A03	- BIEC 2	
Chassis GND - 3B02	3A02	- BIEC 0	
-18 V - 3B01	3A01	- +18 V	

M1/M2 Ternets




P8 - SOP/CFP/EFP
CPMCN - 01
IPL - 03
START - 05
CPINT - 07
RUNFA - 09
RCP 01N - 11
RCP 02N - 13
READMN - 15
LOADMN - 17
+5 V - 19
02 - BIOEKEY
04 - UNLOCKN
06 - RUNN
08 - RCP 00N
10 - LOADRN
12 - READSTN
14 - RCP 03N
16 - INSTN
18 - LOCKN (LO)
20 - +5 V
P9 C
TMMN
S 03
S 01
FU
BOMFN
DONEMN
MMUABS
GND
OSCFLO
GFETCH
LK 1
MXCPZ1N
SPARE
+5V
+5V
READRN
BSYCPUAN
GND
PREQN
GND
GBCPFN
P5 - EFP 6817
SPARE - 01
" - 03
" - 05
" - 07
+5 V - 09
+5 V - 11
+5 V - 13
SPARE - 15
" - 17
" - 19
" - 21
" - 23
" - 25
" - 27
" - 29
" - 31
" - 33
" - 35
" - 37
" - 39
" - 41
" - 43
" - 45
" - 47
0 V - 49
02 - PREQN
04 - BSYCPUAN
06 - GBCPFN
08 - TRMN
10 - +5 V
12 - +5 V
14 - +5 V
16 - WRITE
18 - MAD 128
20 - MAD 64
22 - MAD 00
24 - MAD 01
26 - MAD 02
28 - MAD 03
30 - MAD 04
32 - MAD 05
34 - MAD 06
36 - MAD 07
38 - MAD 08
40 - MAD 09
42 - MAD 10
44 - MAD 11
46 - MAD 12
48 - MAD 13
50 - MAD 14
P6 - SOP/CFP/EFP
BIO 15N - 01
BIO 13N - 03
BIO 11N - 05
BIO 09N - 07
BIO 07N - 09
BIO 05N - 11
BIO 03N - 13
BIO 01N - 15
SPARE - 17
0 V - 19
02 - BIO 14N
04 - BIO 12N
06 - BIO 10N
08 - BIO 08N
10 - BIO 06N
12 - BIO 04N
14 - BIO 02N
16 - BIO 00N
18 - READRN
20 - 0 V
LK 2
BIBC 3
GND
BIBC 4
GND
BIBC 1
MXCPZ1N
BIBC 2
BIBC 5
BIBC 0
SCBIN
P7 - CTW (V24)
CCITT 133 - 01
CCITT 107 - 03
CCITT 108 - 05
CCITT 103 - 07
CCITT 104 - 09
SPARE - 11
02 - GND
04 - "
06 - "
08 - "
10 - "
12 - SPARE



P1/IOM - EXU 6864*

GND	A32	C32	WIRE WRAP POST IOM/32
"	A31	C31	WIRE WRAP POST IOM/31
"	A30	C30	WIRE WRAP POST IOM/30
"	A29	C29	WIRE WRAP POST IOM/29
"	A28	C28	WIRE WRAP POST IOM/28
"	A27	C27	WIRE WRAP POST IOM/27
"	A26	C26	WIRE WRAP POST IOM/26
"	A25	C25	MAD 04
"	A24	C24	MAD 03
"	A23	C23	MAD 08
"	A22	C22	MAD 09
"	A21	C21	MAD 10
"	A20	C20	MAD 11
"	A19	C19	MAD 12
"	A18	C18	MAD 13
"	A17	C17	MAD 14
"	A16	C16	MAD 15
"	A15	C15	ACN
"	A14	C14	SPARE
"	A13	C13	SPARE
CLEARN	A12	C12	SPARE
GND	A11	C11	TPMN
"	A10	C10	SPARE
TMPN	A09	C09	SPARE
GND	A08	C08	TMEN
"	A07	C07	SPARE
TRMN	A06	C06	SPARE
GND	A05	C05	WIRE WRAP POST IOM/5
"	A04	C04	WIRE WRAP POST IOM/4
"	A03	C03	WIRE WRAP POST IOB/3
"	A02	C02	WIRE WRAP POST IOB/2
"	A01	C01	SPARE

P3 - PSU

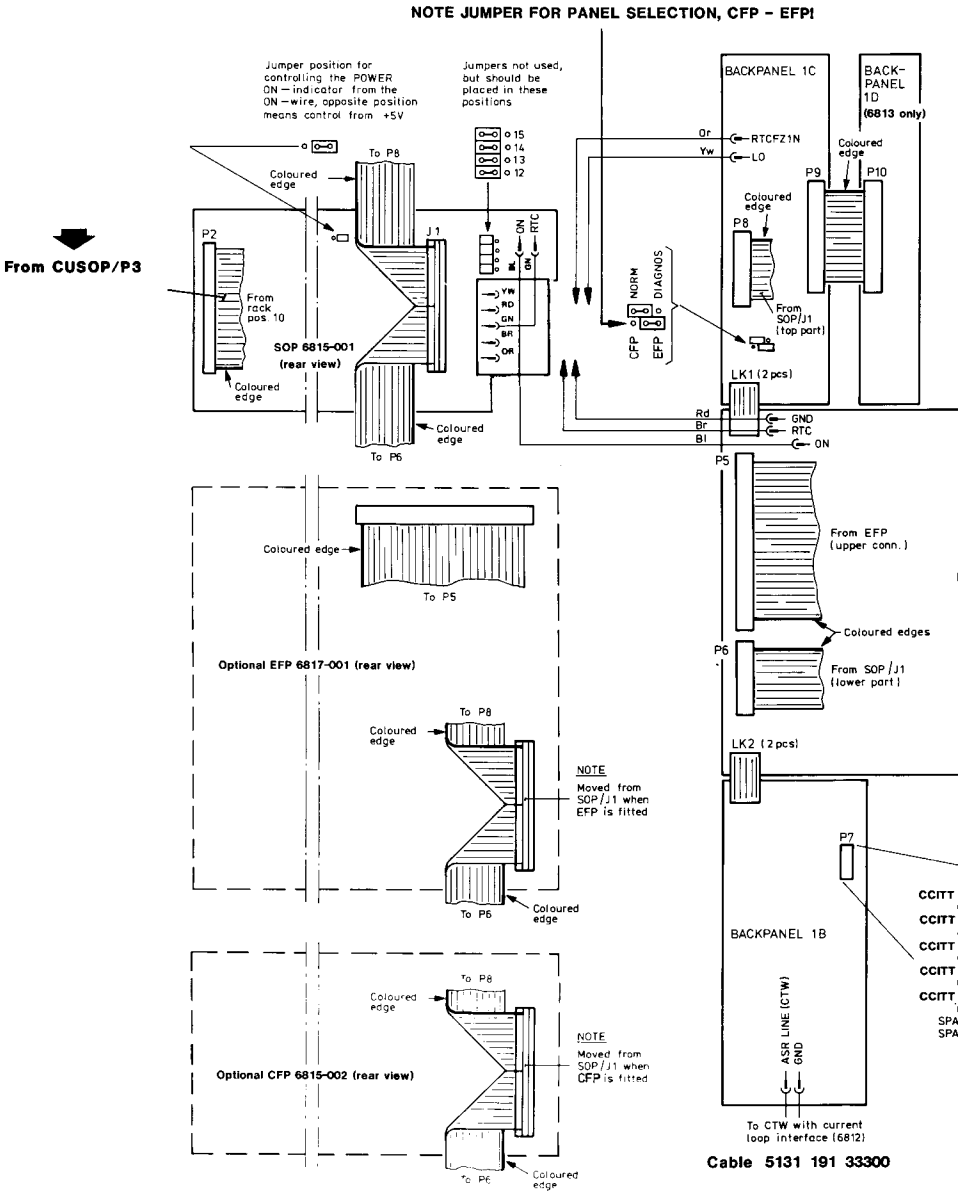
RTC	01	02	GND
FDCN	03	04	"
POWER ONN	05	06	KEY
RSLN	07	08	GND
PWFN	09	10	"
SPARE	11	12	"

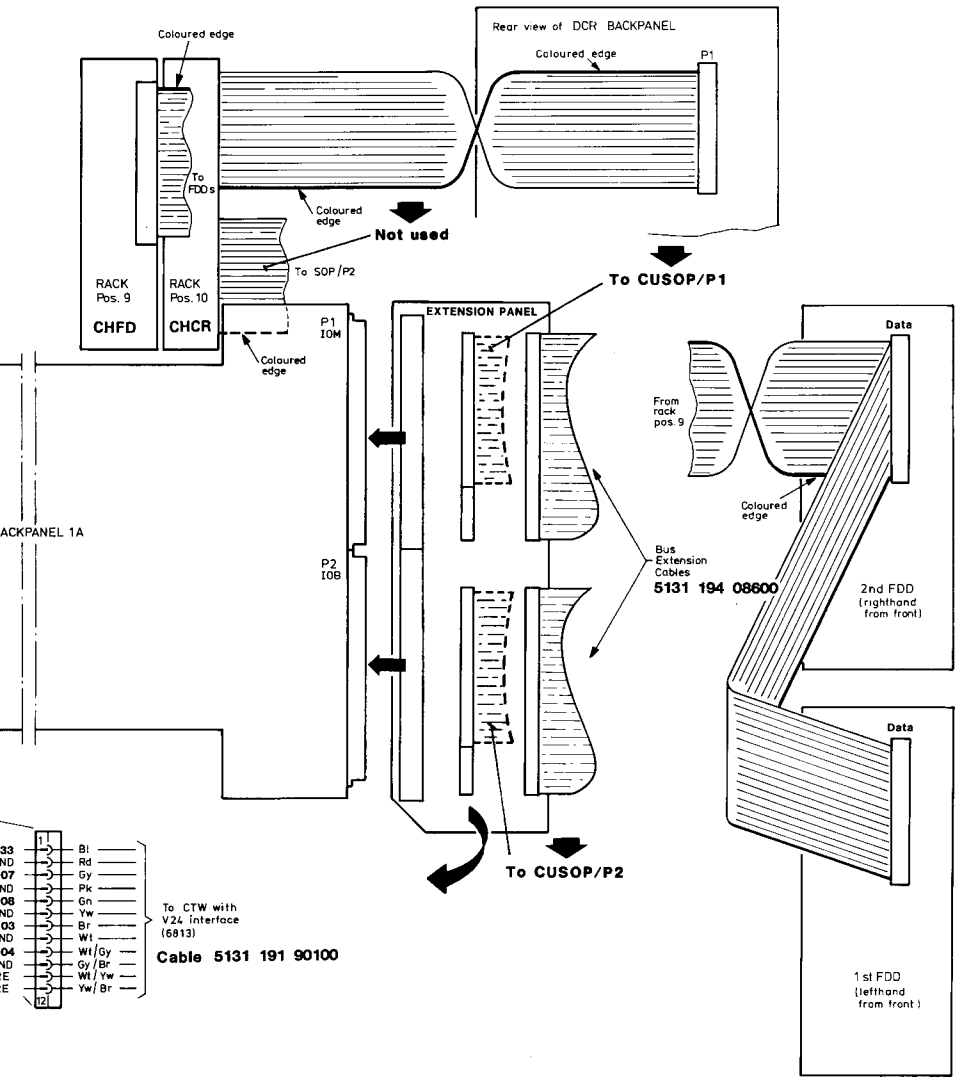
P2/IOB - EXU 6864*

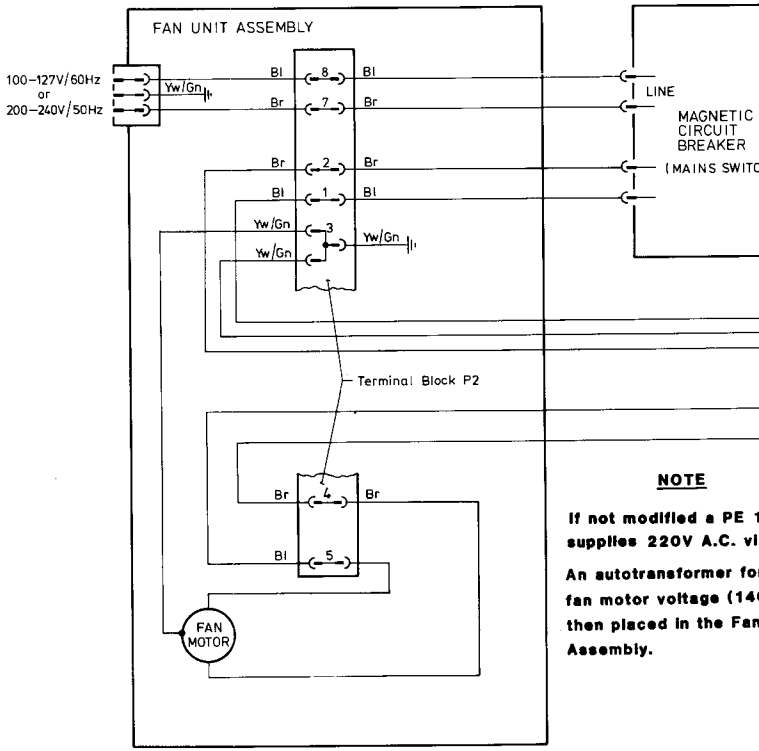
GND	A32	C32	RSLN
"	A31	C31	PWFN
"	A30	C30	BIO 15N
"	A29	C29	BIO 14N
"	A28	C28	BIO 13N
"	A27	C27	BIO 12N
"	A26	C26	BIO 11N
"	A25	C25	BIO 10N
"	A24	C24	BIO 09N
"	A23	C23	BIO 08N
"	A22	C22	BIO 07N
"	A21	C21	BIO 06N
"	A20	C20	BIO 05N
"	A19	C19	BIO 04N
"	A18	C18	BIO 03N
"	A17	C17	BIO 02N
"	A16	C16	BIO 01N
"	A15	C15	BIO 00N
"	A14	C14	BIEC 5
"	A13	C13	SCEIN
"	A12	C12	BIEC 3
"	A11	C11	BIEC 4
"	A10	C10	BIEC 1
"	A09	C09	BIEC 2
"	A08	C08	BIEC 0
"	A07	C07	WIRE WRAP POST IOB/7
"	A06	C06	WIRE WRAP POST IOB/6
"	A05	C05	WIRE WRAP POST IOB/5
"	A04	C04	WIRE WRAP POST IOB/4
"	A03	C03	WIRE WRAP POST IOB/3
"	A02	C02	WIRE WRAP POST IOB/2
"	A01	C01	WIRE WRAP POST IOB/1

*Via an Extension Panel, see Chapter 2!

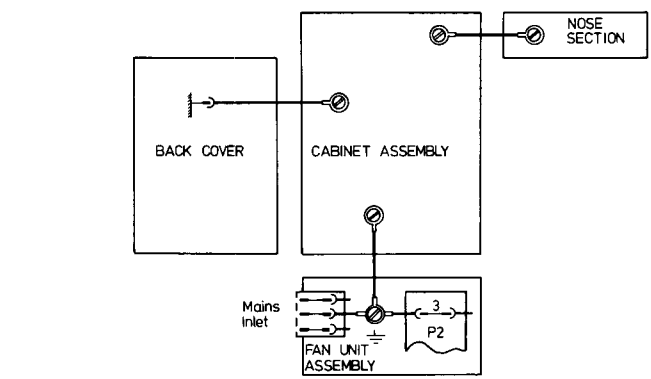
Notes applicable when using an upgraded SOP (including a CUSOP)

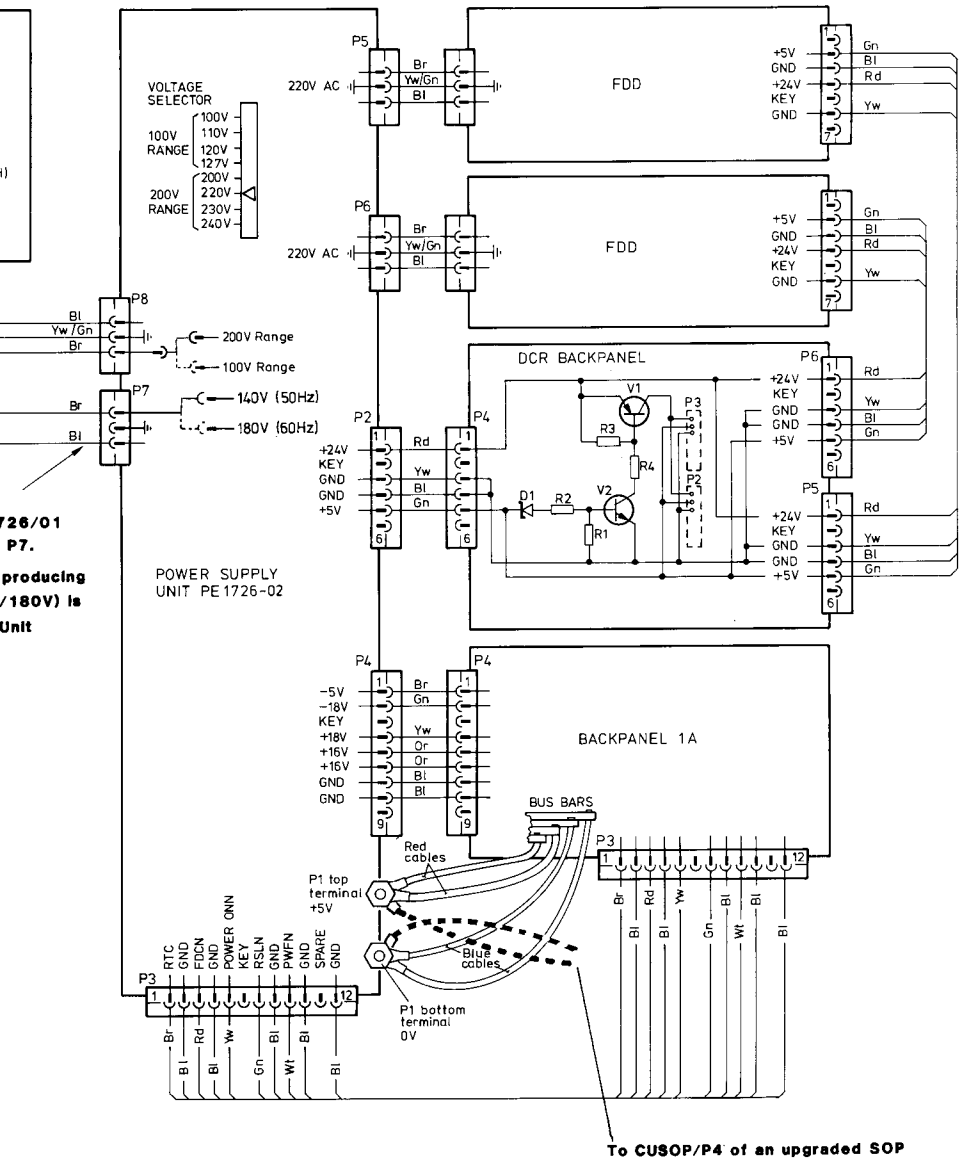



Coloured edge
Rear view of DCR BACKPANEL
Coloured edge
P1
To FDDs
Coloured edge
Not used
To SOP/P2
RACK Pos. 9
CHFD
RACK Pos. 10
CHCR
To CUSOP/P1
EXTENSION PANEL
P1 IOM
Coloured edge
Data
From rack pos. 9
Coloured edge
ACKPANEL 1A
P2 IOB
Bus Extension Cables
5131 194 08600
2nd FDD (righthand from front)
Data
To CUSOP/P2
1 st FDD (lefthand from front)
33
ND
07
ND
08
ND
03
ND
04
ND
E
E
1
12
Bl
Rd
Gy
Pk
Gn
Yw
Br
Wt
Wt/Gy
Gy/Br
Wt/Yw
Yw/Br
To CTW with V24 interface (6813)
Cable 5131 191 90100

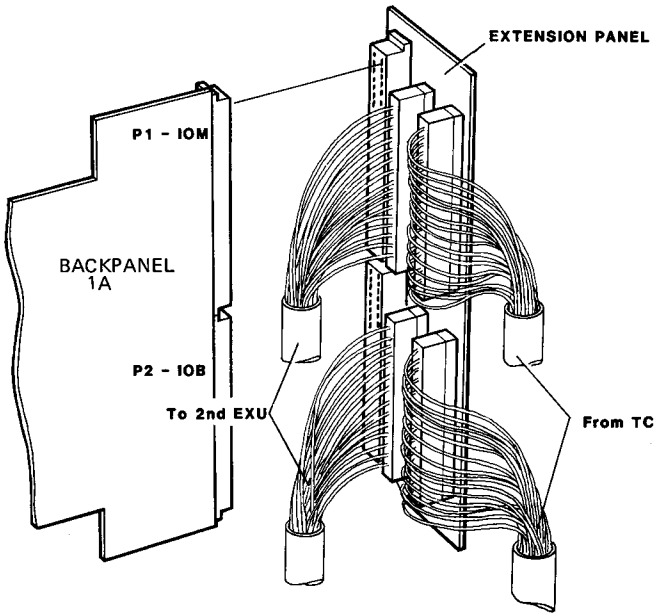


PROTECTIVE EARTH SYSTEM




VOLTAGE SELECTOR
100V RANGE
100V
110V
120V
127V
200V RANGE
200V
220V
230V
240V
220V AC
P5
P6
Br
Yw/Gn
Bl
FDD
+5V
GND
+24V
KEY
GND
Gn
Bl
Rd
Yw
P8
P7
200V Range
100V Range
140V (50Hz)
180V (60Hz)
DCR BACKPANEL
P2
P4
P6
P5
V1
V2
R1
R2
R3
R4
D1
P3
+24V
KEY
GND
GND
+5V
POWER SUPPLY UNIT PE1726-02
BACKPANEL 1A
-5V
-18V
KEY
+18V
+16V
+16V
GND
GND
Or
BUS BARS
Red cables
Blue cables
P1 top terminal +5V
P1 bottom terminal 0V
RTC
GND
FDCN
GND
POWER QNN
KEY
RSLN
GND
PWFN
GND
SPARE
GND
To CUSOP/P4 of an upgraded SOP

CABLING FROM TC/TO 2ND EXU



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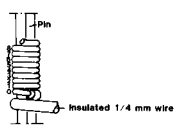
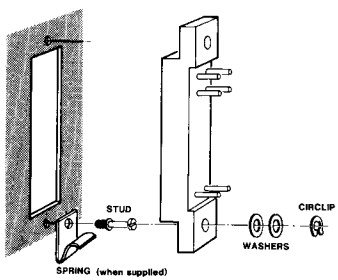
(5322 209
for extend

INSTALLING RACK BACKPANEL OPTIONS

Additional wire wrap connections

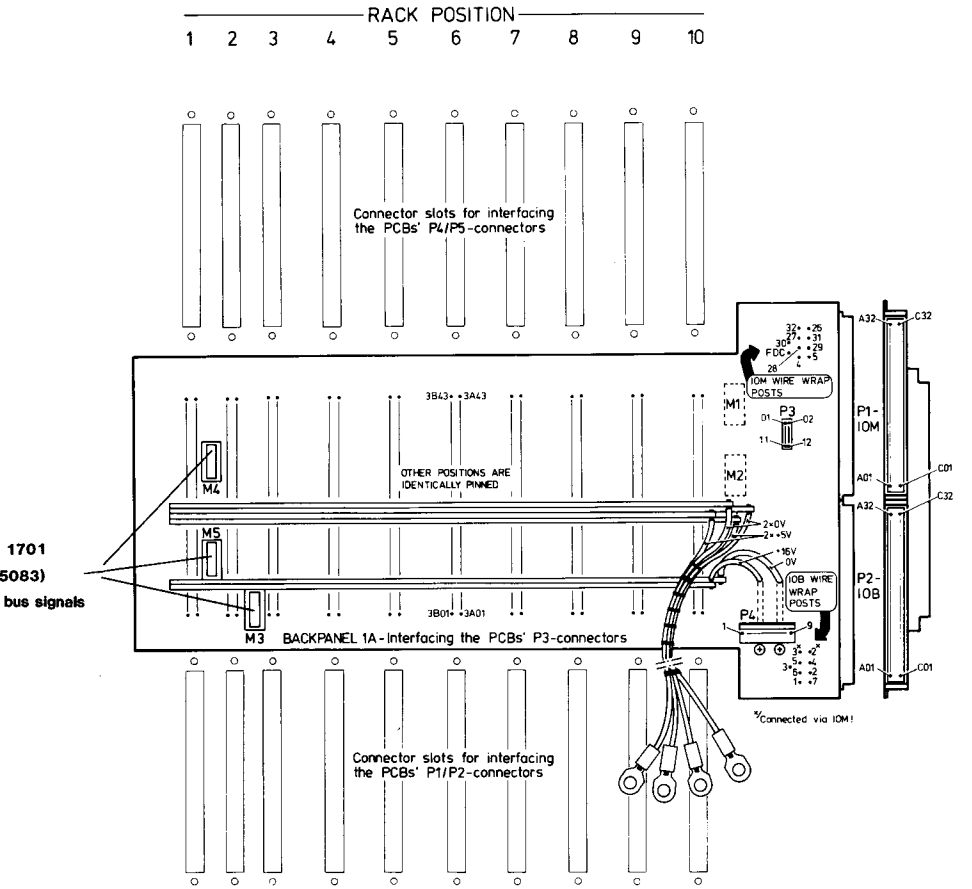


Socket for P1/P2 or P4/P5 connectors

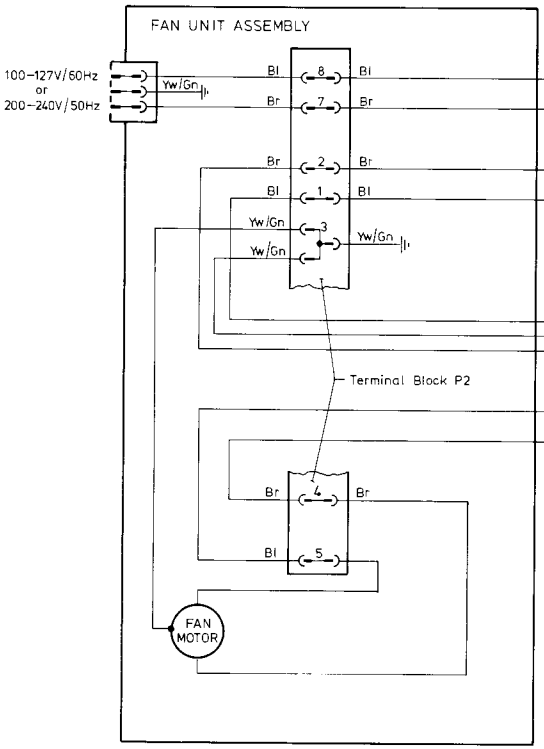


EXU 6864

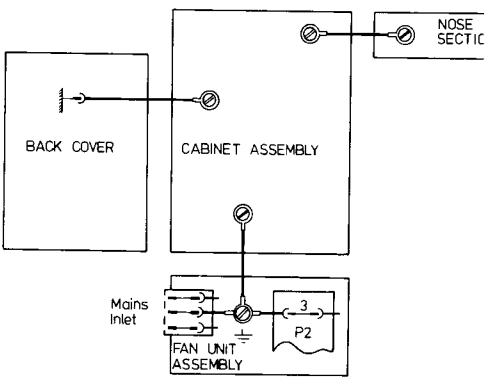
2-layer Backpanel



For multilayer type, see page 6.4-4!

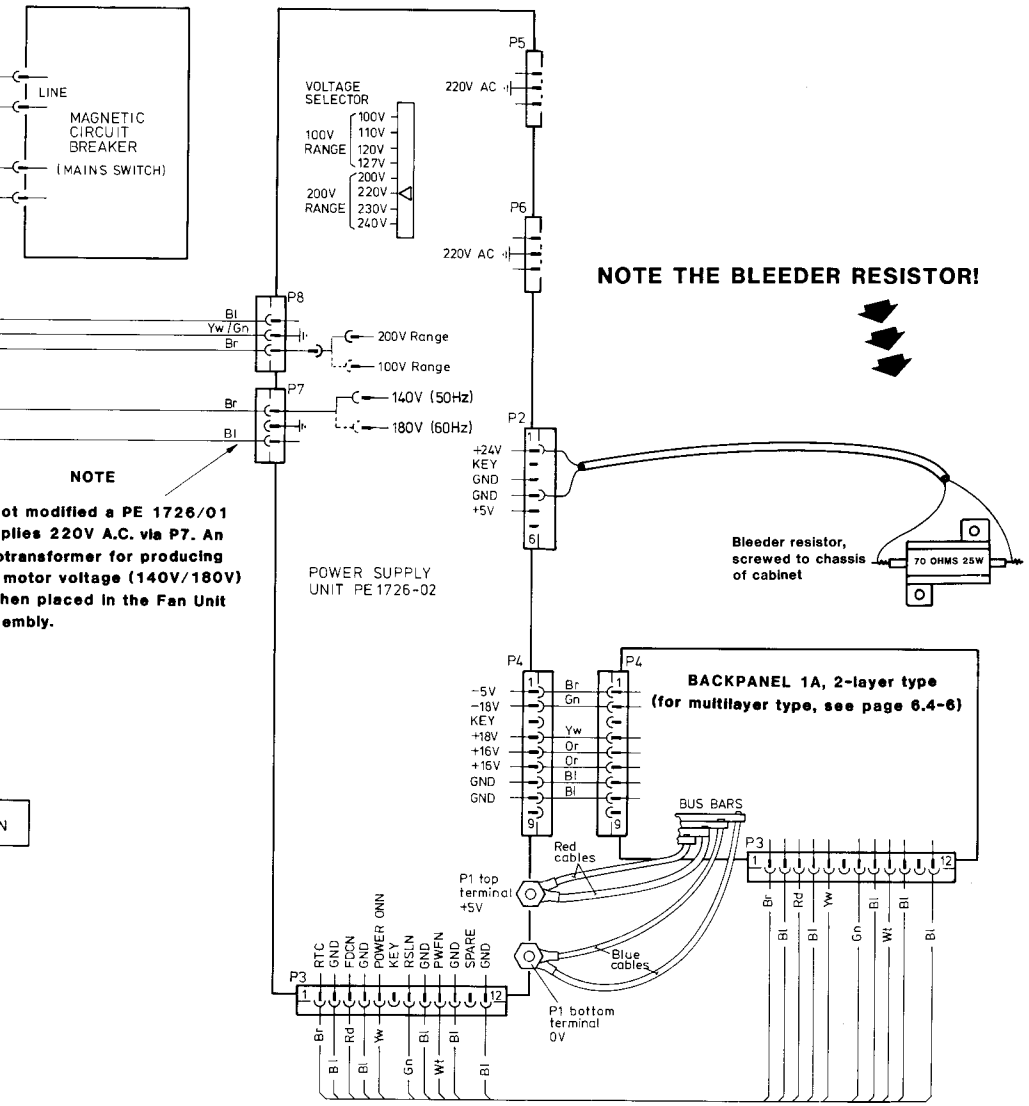


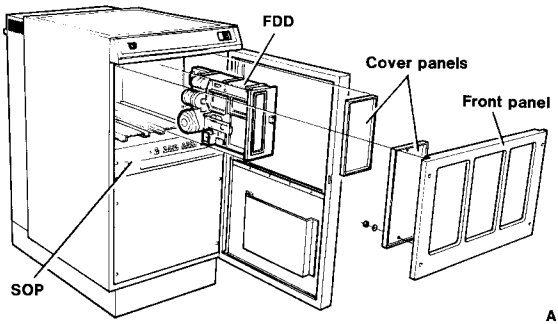
PROTECTIVE EARTH SYSTEM



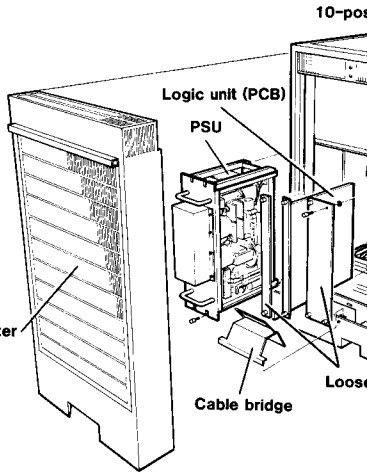
EXU 6864

Power Distribution
(2-layer backpanel)

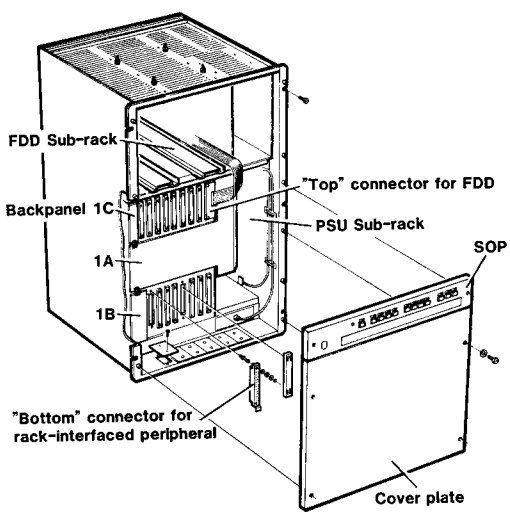




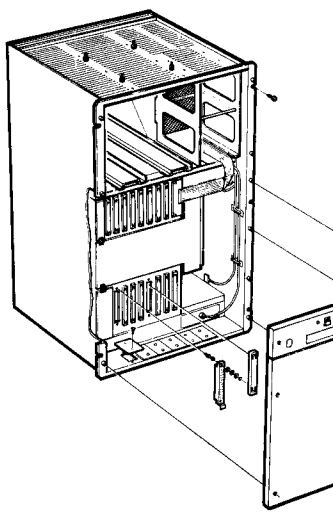
SHOWN CABINET IS FOR TC 6824, TC 6814 IS HOUSED IN THE SAME TYPE OF CABINET AS TC 6812/13



RACK FOR TC 6824, WITHOUT DCR SUB-RACK

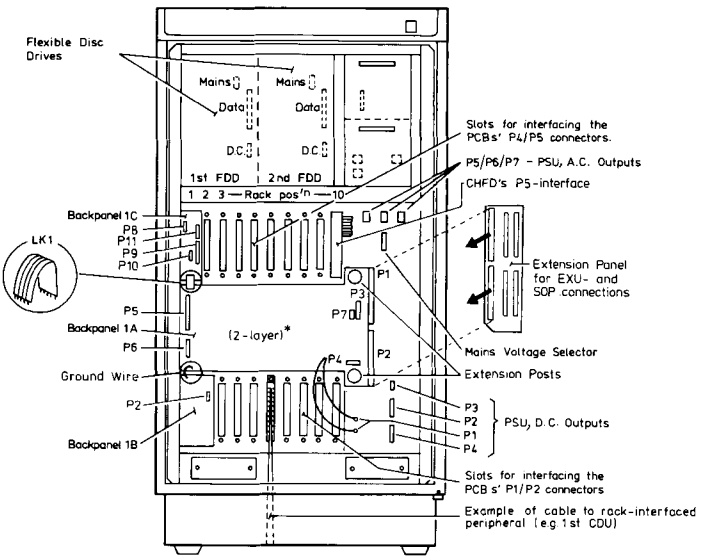


RACK FOR TC 6814, WITH DCR SUB-RACI

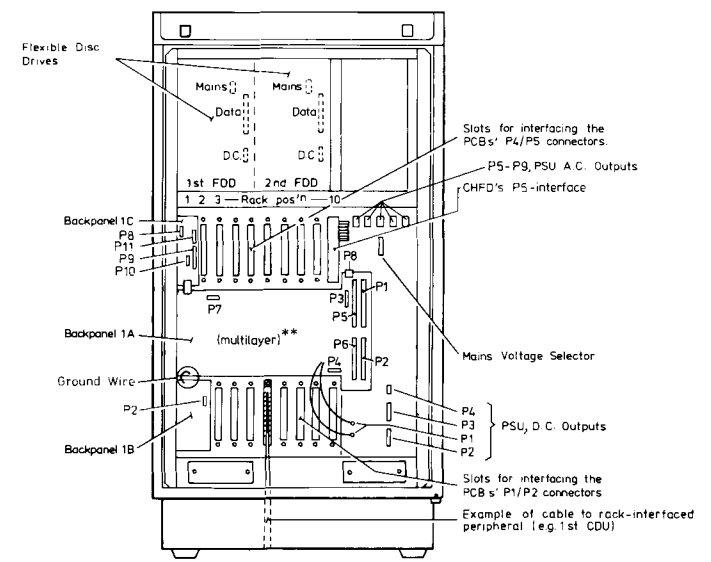


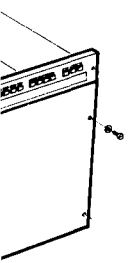
Physical Structure

TC 6814

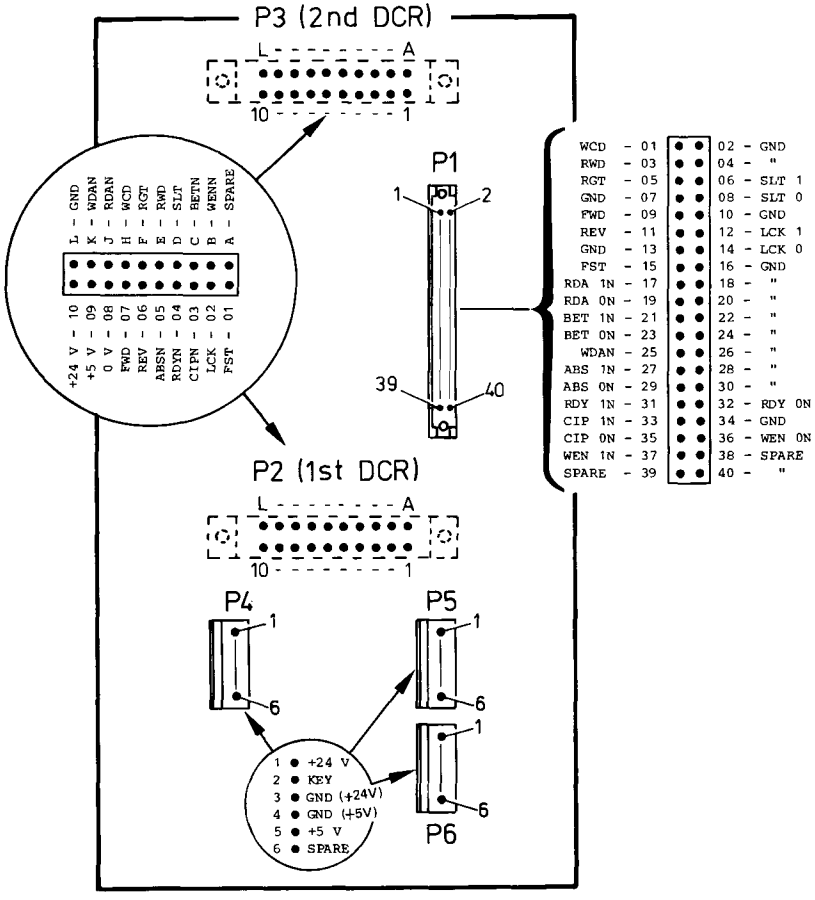


TC 6824





*or multilayer, see 6824 **or 2-layer, see 6814

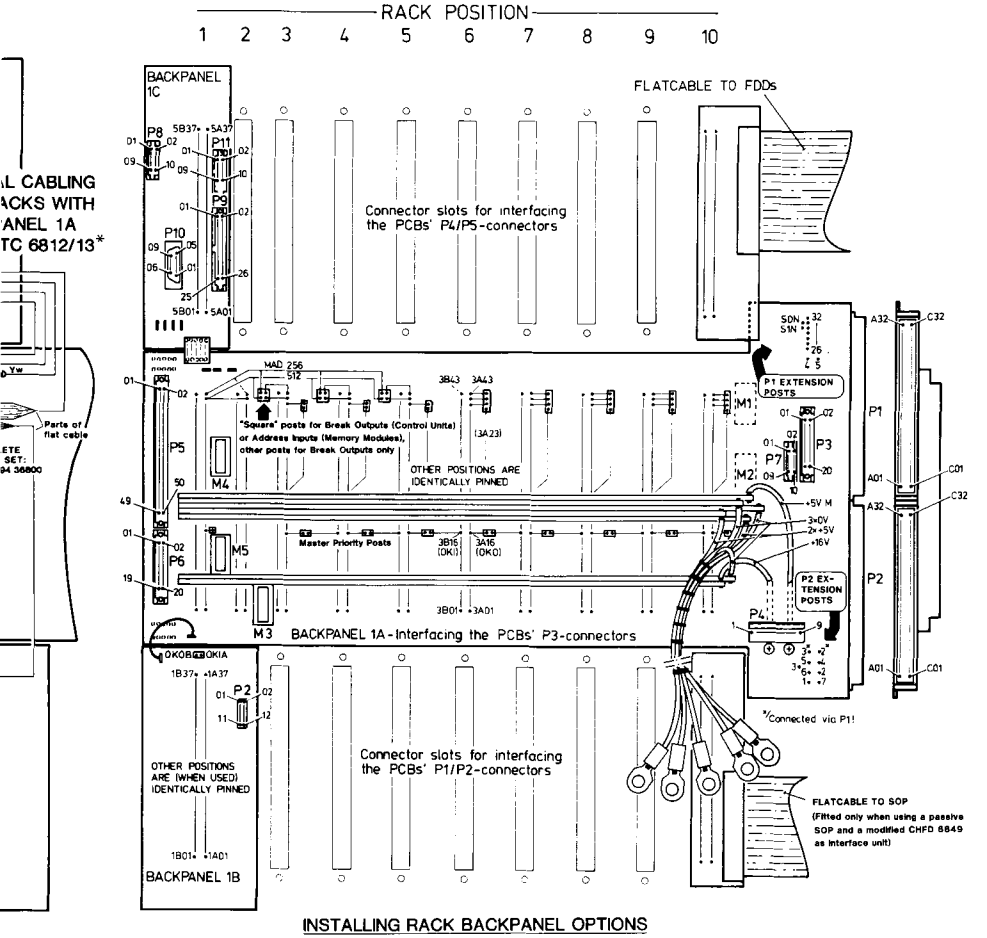


*In cabir

NOTE

See Page 6.5-5/6 for rack backpanel assembly with 1A of multilayer type!

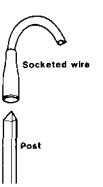
DCR Backpanel (6814 only) and 2-layer Rack Backpanels



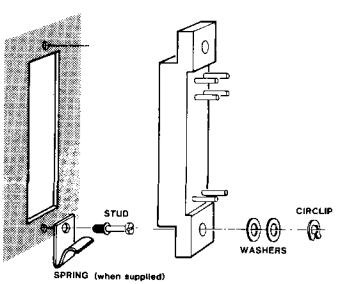
ets of type 5131 193 92900

INSTALLING RACK BACKPANEL OPTIONS

Additional connections with socketed wires between special posts



Socket for P1/P2 or P4/P5 connectors



P5 - CPU P857R/RA

-12 V	5B37	5A37	SPARE
SPARE	5B36	5A36	SPARE
+12 V	5B35	5A35	RTCE
RESETN	5B34	5A34	SDMP
+5 V	5B33	5A33	SPARE
IPLN	5B32	5A32	IPLRMTN
GND	5B31	5A31	SDPM
IPL	5B30	5A30	LOCK
OPS0N	5B29	5A29	SPARE
OPS1N	5B28	5A28	"
OPS2N	5B27	5A27	"
OPS3N	5B26	5A26	"
RTCZ1N	5B25	5A25	"
SPARE	5B24	5A24	"
BAWOFN	5B23	5A23	"
SPARE	5B22	5A22	"
"	5B21	5A21	"
PAFN	5B20	5A20	"
SPARE	5B19	5A19	"
"	5B18	5A18	"
"	5B17	5A17	OSC
"	5B16	5A16	SPARE
FPPABS	5B15	5A15	FLOCR 1
FLOCRO	5B14	5A14	DONEFN
BOFFN	5B13	5A13	GFETCH
TMFN	5B12	5A12	BSYCPUN
SPARE	5B11	5A11	FLOACT
"	5B10	5A10	SPARE
"	5B09	5A09	"
"	5B08	5A08	"
"	5B07	5A07	IS07N
INTSERN	5B06	5A06	IS06N
CPINTN	5B05	5A05	IS05N
SPARE	5B04	5A04	IS04N
"	5B03	5A03	IS03N
"	5B02	5A02	SPARE
"	5B01	5A01	"

P1 - CHFD 6E

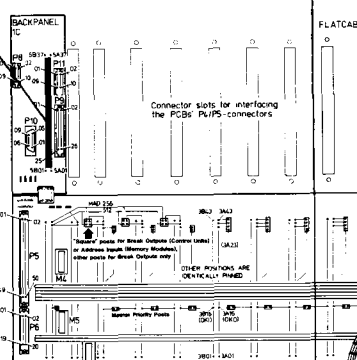
SPARE	1B37		1A3
"	1B36		1A3
"	1B35		1A3
"	1B34		1A3
"	1B33		1A3
"	1B32		1A3
"	1B31		1A3
"	1B30		1A3
"	1B29		1A2
"	1B28		1A2
"	1B27		1A2
"	1B26		1A2
"	1B25		1A2
"	1B24		1A2
"	1B23		1A2
"	1B22		1A2
"	1B21		1A2
LED13N	1B20		1A2
+5V	1B19		1A1
LED10N	1B18		1A1
LED14N	1B17		1A1
0V	1B16		1A1
LED11N	1B15		1A1
0V	1B14		1A1
0V	1B13		1A1
0V	1B12		1A1
LED05N	1B11		1A1
0V	1B10		1A1
0V	1B09		1A0
0V	1B08		1A0
CHAIN BEGINN	1B07		1A0
0V	1B06		1A0
0V	1B05		1A0
0V	1B04		1A0
0V	1B03		1A0
DSW10N	1B02		1A0
DSW08N	1B01		1A0

*Used only for connection of a passive SOP (type 5131 193 83300)

P1 - CPU P857R/RA

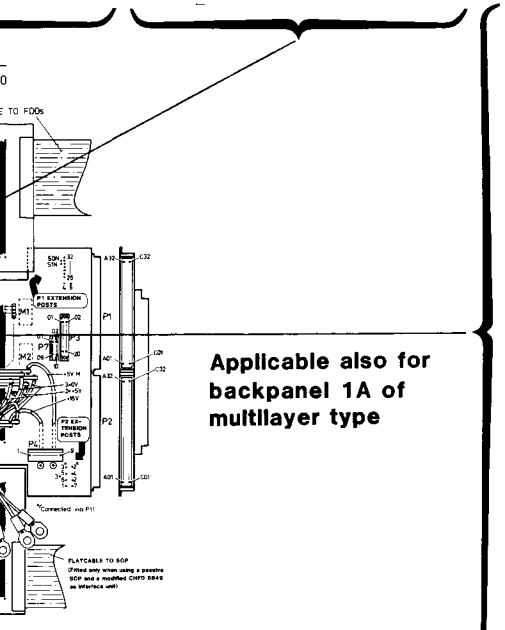
SPARE	1B37	1A37	SPARE
OK0B	1B36	1A36	OK1B
OK0A	1B35	1A35	OK1A
SPARE	1B34	1A34	SPARE
"	1B33	1A33	"
"	1B32	1A32	"
"	1B31	1A31	"
"	1B30	1A30	"
"	1B29	1A29	"
"	1B28	1A28	"
"	1B27	1A27	"
"	1B26	1A26	BR15N
"	1B25	1A25	BR14N
"	1B24	1A24	BR13N
"	1B23	1A23	BR12N
"	1B22	1A22	BR11N
"	1B21	1A21	BR10N
"	1B20	1A20	BR09N
"	1B19	1A19	BR08N
"	1B18	1A18	BR07N
"	1B17	1A17	BR06N
"	1B16	1A16	BR05N
"	1B15	1A15	BR04N
"	1B14	1A14	BR03N
"	1B13	1A13	BR02N
"	1B12	1A12	BR01N
"	1B11	1A11	BR00N
"	1B10	1A10	SPARE
"	1B09	1A09	"
"	1B08	1A08	"
"	1B07	1A07	CCITT 133
"	1B06	1A06	SPARE
"	1B05	1A05	CCITT 108
"	1B04	1A04	CCITT 107
"	1B03	1A03	SPARE
"	1B02	1A02	CCITT 103
GND	1B01	1A01	CCITT 104

NOTE: 1B35 - 1A36: AT BACKPANEL 1B
PROTO TYPES: WIRE WRAPPED AT CONNECTOR



P5 - CHFD 6849

49*						
7 - SPARE	GND -	5B37	● ●	5A37	-	RDLN
6 - "	" -	5B36	● ●	5A36	-	HLN
5 - "	" -	5B35	● ●	5A35	-	TRON
4 - "	" -	5B34	● ●	5A34	-	INDN
4 - "	" -	5B33	● ●	5A33	-	LWCN
2 - "	" -	5B32	● ●	5A32	-	STEPN
1 - "	" -	5B31	● ●	5A31	-	DIRN
1 - "	" -	5B30	● ●	5A30	-	WEN
9 - "	" -	5B29	● ●	5A29	-	WDN
8 - "	" -	5B28	● ●	5A28	-	SEL0N
7 - "	" -	5B27	● ●	5A27	-	SEL1N
6 - "	" -	5B26	● ●	5A26	-	SEL2N
5 - "	" -	5B25	● ●	5A25	-	SEL3N
4 - "	SPARE -	5B24	● ●	5A24	-	SPARE
3 - "	" -	5B23	● ●	5A23	-	"
2 - "	" -	5B22	● ●	5A22	-	"
1 - "	" -	5B21	● ●	5A21	-	"
0 - +5V	" -	5B20	● ●	5A20	-	"
9 - LED15N	" -	5B19	● ●	5A19	-	"
8 - LED10N	" -	5B18	● ●	5A18	-	"
7 - LED14N	" -	5B17	● ●	5A17	-	"
6 - LED12N	" -	5B16	● ●	5A16	-	"
5 - LED11N	" -	5B15	● ●	5A15	-	"
4 - LED09N	" -	5B14	● ●	5A14	-	"
3 - LED08N	" -	5B13	● ●	5A13	-	"
2 - LED07N	" -	5B12	● ●	5A12	-	"
1 - LED06N	GND -	5B11	● ●	5A11	-	RDY1N
0 - DSW06N	" -	5B10	● ●	5A10	-	RDY2N
9 - CHAIN ENDN	" -	5B09	● ●	5A09	-	RDY3N
8 - DSW07N	" -	5B08	● ●	5A08	-	WRPN
7 - DSW15N	" -	5B07	● ●	5A07	-	RDY0N
6 - DSW14N	" -	5B06	● ●	5A06	-	DC40N
5 - DSW13N	" -	5B05	● ●	5A05	-	DC42N
4 - 0V	" -	5B04	● ●	5A04	-	SPARE
3 - DSW12N	DC45N -	5B03	● ●	5A03	-	"
2 - DSW11N	DC47N -	5B02	● ●	5A02	-	DC48N
1 - DSW09N	GND -	5B01	● ●	5A01	-	DC50N



Applicable also for backpanel 1A of multilayer type

P3 - GENERAL

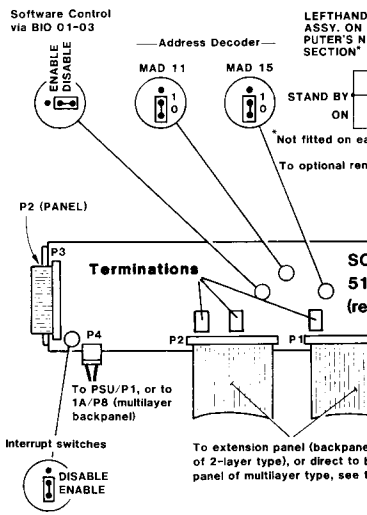
M1/15 --- MAD	128 -	3B43	● ●	3A43	-	MAD 256/BR*
M1/14 --- MAD	64 -	3B42	● ●	3A42	-	MAD 512/BR*
M1/13 --- MAD	00 -	3B41	● ●	3A41	-	BR
M1/12 --- MAD	01 -	3B40	● ●	3A40	-	GND
M1/11 --- MAD	02 -	3B39	● ●	3A39	-	CLEARN
MAD	03 -	3B38	● ●	3A38	-	BSYN ----- M1/10
MAD	04 -	3B37	● ●	3A37	-	MSN ------ M1/9
M1/5 ---- MAD	05 -	3B36	● ●	3A36	-	BUSRN ---- M1/7
M1/4 ---- MAD	06 -	3B35	● ●	3A35	-	SPYC ----- M1/6
M1/3 ---- MAD	07 -	3B34	● ●	3A34	-	ACN
MAD	08 -	3B33	● ●	3A33	-	GND
MAD	09 -	3B32	● ●	3A32	-	TPMN
MAD	10 -	3B31	● ●	3A31	-	TMPN
MAD	11 -	3B30	● ●	3A30	-	TMEN
MAD	12 -	3B29	● ●	3A29	-	TMRN ----- M2/15
MAD	13 -	3B28	● ●	3A28	-	TRMN
MAD	14 -	3B27	● ●	3A27	-	CHA ------ M2/13
MAD	15 -	3B26	● ●	3A26	-	WRITE ---- M2/12
+16 V -		3B25	● ●	3A25	-	GND
M1/M2 Ternets GND -		3B24	● ●	3A24	-	GND
+5 V -		3B23	● ●	3A23	-	BR
+5V (16) 0 V -		3B22	● ●	3A22	-	0 V
0 V -		3B21	● ●	3A21	-	0 V
220 +5 V -		3B20	● ●	3A20	-	+5 V
+5 V -		3B19	● ●	3A19	-	+5 V
-5 V -		3B18	● ●	3A18	-	0 V
330 RSLN -		3B17	● ●	3A17	-	PWFN
OKI -		3B16	● ●	3A16	-	OKO
(8) BIO 15N -		3B15	● ●	3A15	-	BIO 14N
BIO 13N -		3B14	● ●	3A14	-	BIO 12N
BIO 11N -		3B13	● ●	3A13	-	BIO 10N
BIO 09N -		3B12	● ●	3A12	-	BIO 08N
BIO 07N -		3B11	● ●	3A11	-	BIO 06N
BIO 05N -		3B10	● ●	3A10	-	BIO 04N
BIO 03N -		3B09	● ●	3A09	-	BIO 02N
BIO 01N -		3B08	● ●	3A08	-	BIO 00N
0 V -		3B07	● ●	3A07	-	0 V
+16 V -		3B06	● ●	3A06	-	+16 V
BIEC 5 -		3B05	● ●	3A05	-	SCEIN
BIEC 3 -		3B04	● ●	3A04	-	BIEC 4
BIEC 1 -		3B03	● ●	3A03	-	BIEC 2
Chassis GND -		3B02	● ●	3A02	-	BIEC 0
-18 V -		3B01	● ●	3A01	-	+18 V

* Address lines in CPU and Memory positions, Break outputs in other positions.

IMPORTANT!

When installing this SOP assembly in an extended system (TC with one or two EXUs) - remove the terminations fitted on CUSOP, positions 8B, 10B & 14B!

Appl
only



NOTE

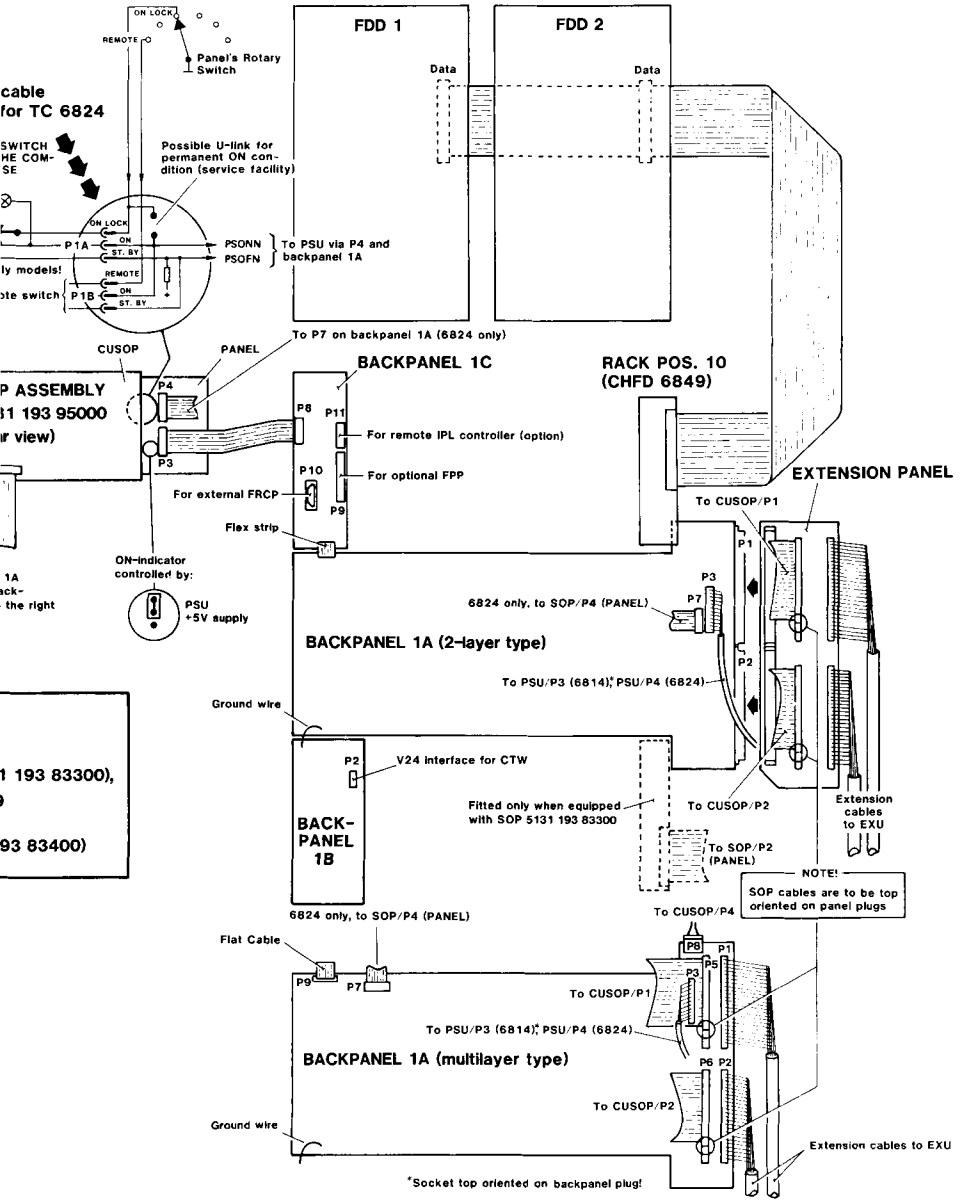
Early deliveries of TC 6814 may have:

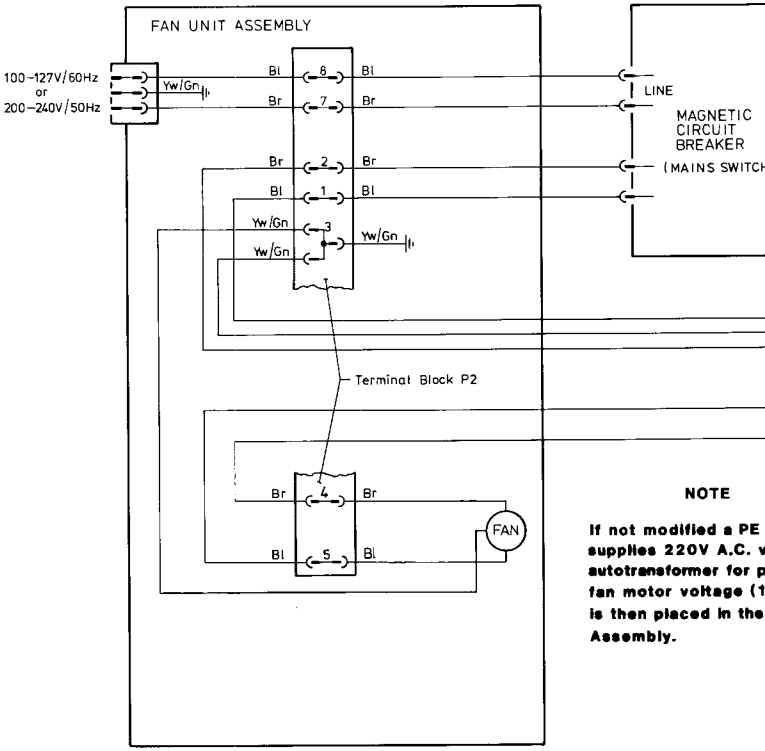
a) a key-operated SOP without CUSOP (513
connected to P1 of a modified CHFD 684

b) a key-operated SOP with CUSOP (5131

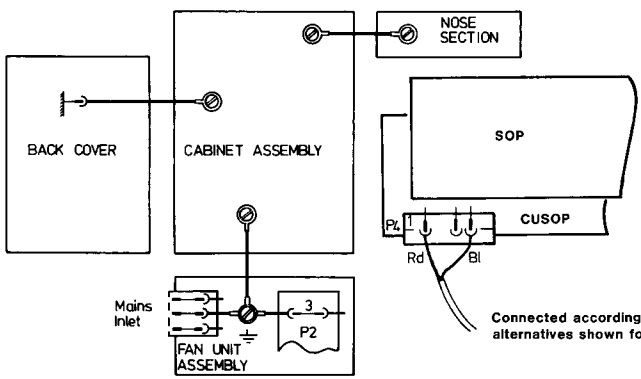
TC 6814, 6824

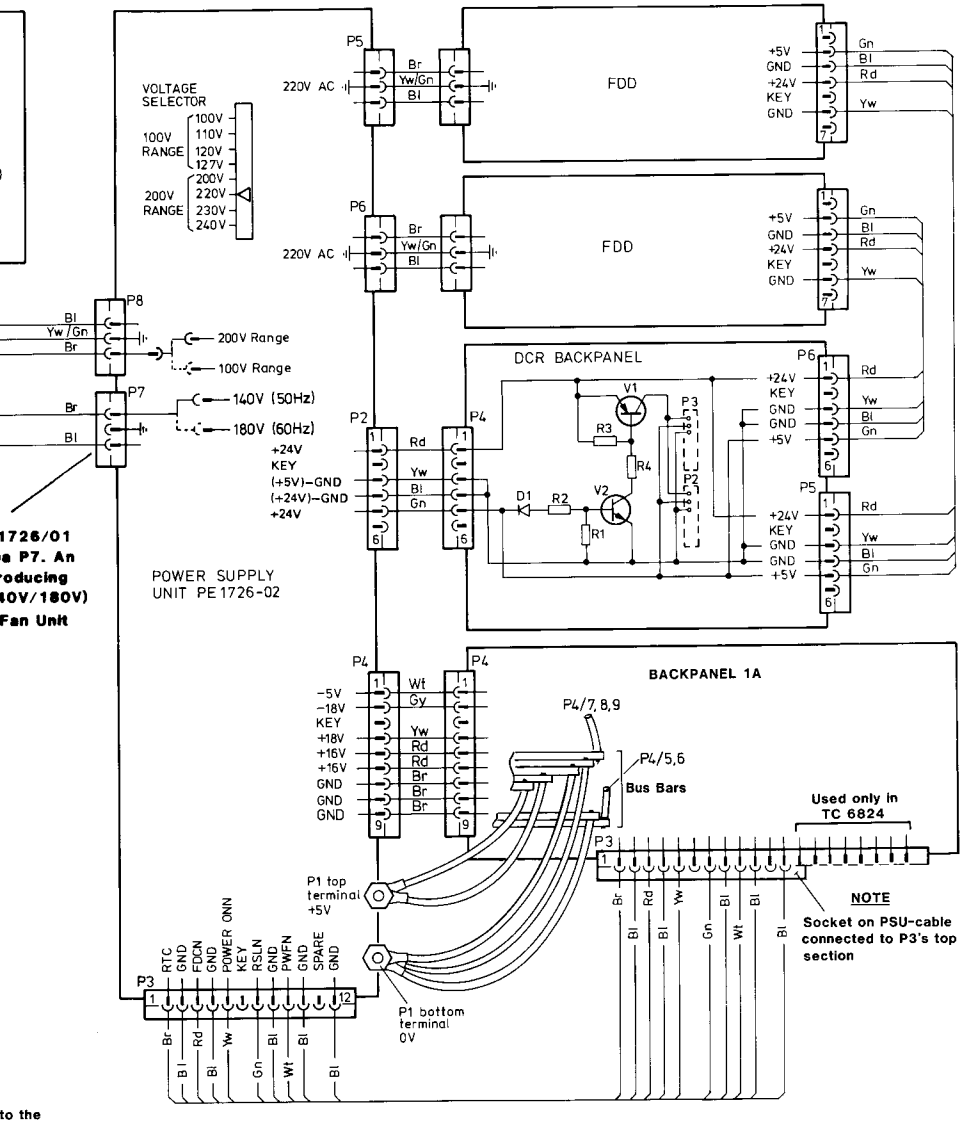
Module Interconnections





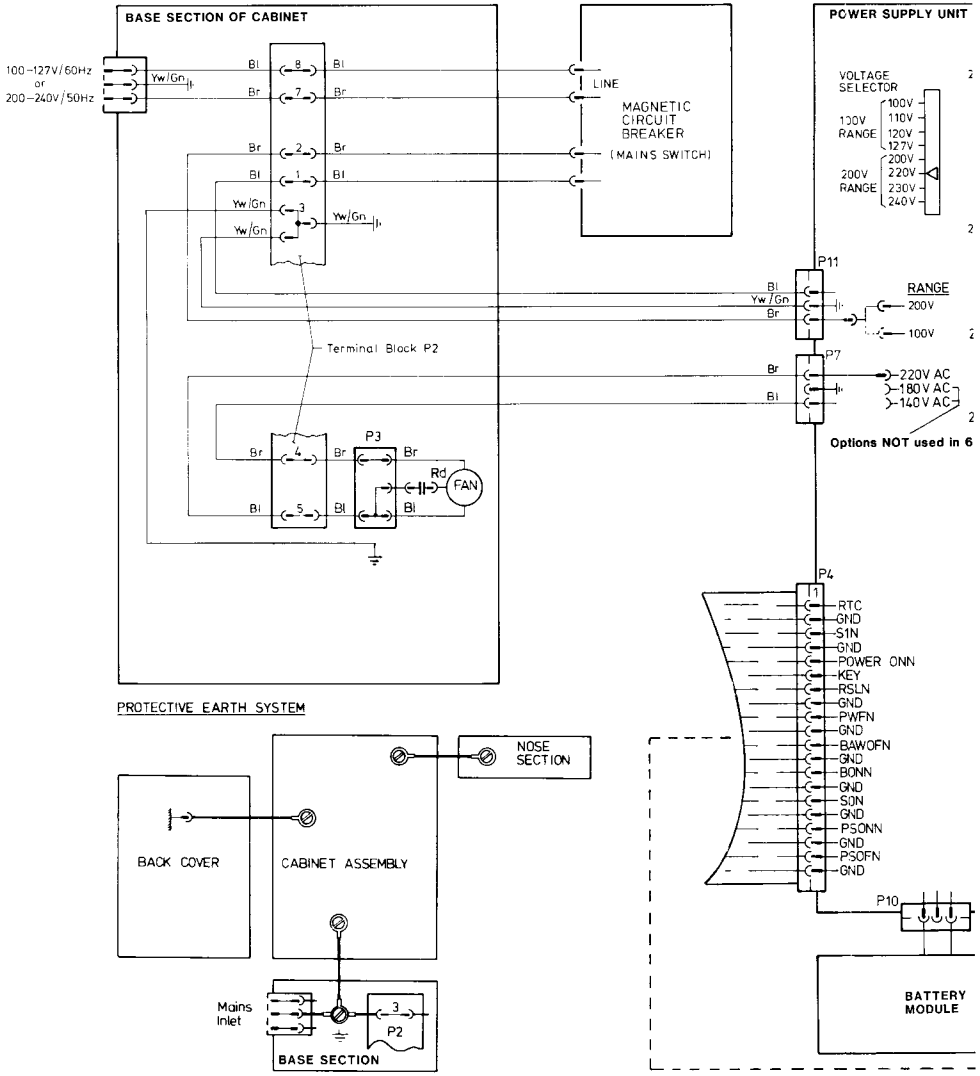
PROTECTIVE EARTH SYSTEM

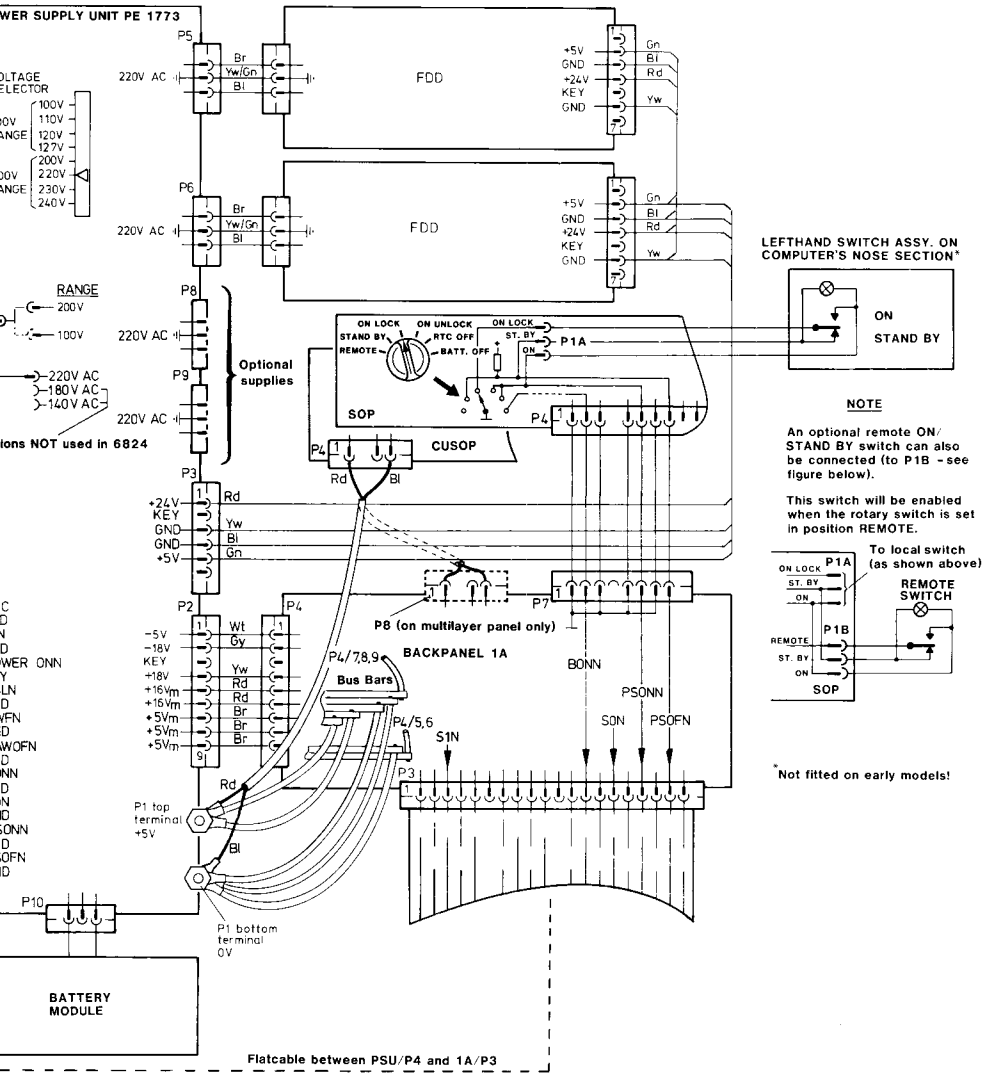




1726/01
e P7. An
roducing
40V/180V)
Fan Unit

to the
TC 6824


BASE SECTION OF CABINET
POWER SUPPLY UNIT
100–127V/60Hz
or
200–240V/50Hz
Yw/Gn
Bl
Br
LINE
MAGNETIC
CIRCUIT
BREAKER
(MAINS SWITCH)
VOLTAGE
SELECTOR
100V
RANGE
110V
120V
127V
200V
RANGE
220V
230V
240V
P11
RANGE
200V
100V
Terminal Block P2
P7
220V AC
180V AC
140V AC
Options NOT used in 6
P3
Rd
FAN
P4
RTC
GND
S1N
GND
POWER ONN
KEY
RSLN
GND
PWFN
GND
BAWOFN
GND
BONN
GND
S0N
GND
PSONN
GND
PSOFN
GND
P10
BATTERY
MODULE
PROTECTIVE EARTH SYSTEM
NOSE
SECTION
BACK COVER
CABINET ASSEMBLY
Mains
Inlet
P2
BASE SECTION


WER SUPPLY UNIT PE 1773
P5
220V AC
Br
Yw/Gn
Bl
FDD
+5V
GND
+24V
KEY
GND
Gn
Bl
Rd
Yw
P6
220V AC
FDD
RANGE
200V
100V
220V AC
180V AC
140V AC
ions NOT used in 6824
P8
P9
220V AC
220V AC
Optional supplies
ON LOCK
STAND BY
REMOTE
ON UNLOCK
RTC OFF
BATT. OFF
ON LOCK
ST. BY
ON
P1A
SOP
P4
CUSOP
P3
+24V
KEY
GND
GND
+5V
Rd
Yw
Bl
Gn
P2
P4
P7
P8 (on multilayer panel only)
BACKPANEL 1A
P4/7,8,9
Bus Bars
P4/5,6
S1N
BONN
PSONN
SON
PSOFN
-5V
-18V
KEY
+18V
+16Vm
+16Vm
+5Vm
+5Vm
+5Vm
Wt
Gy
Yw
Rd
Rd
Br
Br
Br
P1 top terminal +5V
P1 bottom terminal 0V
P10
BATTERY MODULE
Flatcable between PSU/P4 and 1A/P3
LEFTHAND SWITCH ASSY. ON COMPUTER'S NOSE SECTION*
ON
STAND BY
NOTE
An optional remote ON/STAND BY switch can also be connected (to P1B - see figure below).
This switch will be enabled when the rotary switch is set in position REMOTE.
To local switch (as shown above)
ON LOCK
ST. BY
ON
P1A
REMOTE SWITCH
REMOTE
ST. BY
ON
P1B
SOP
*Not fitted on early models!

CONTENTS

LIST OF ILLUSTRATIONS & TABLES

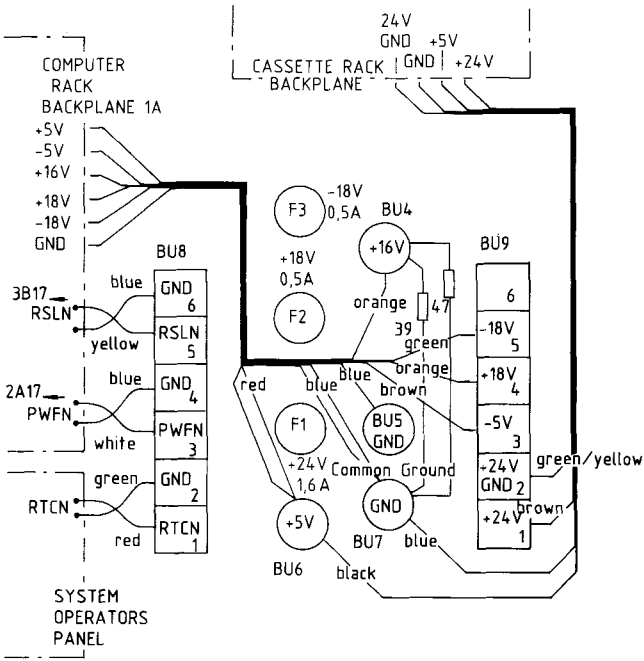
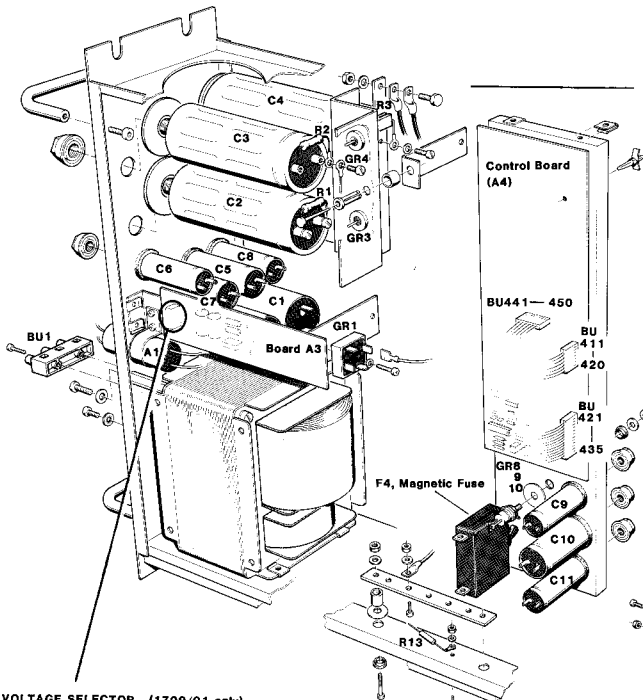
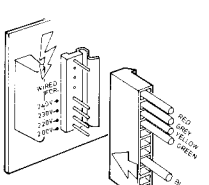


Figure 7.1.1 Connections PSU 1440



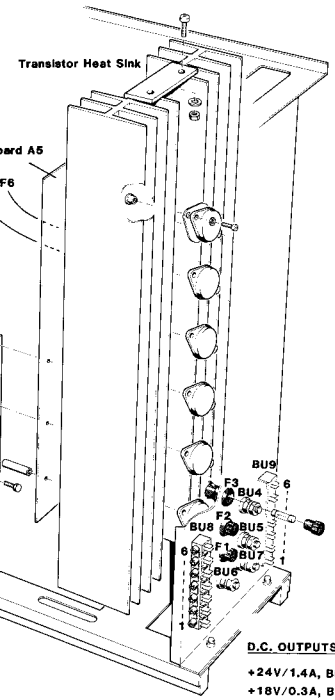


MAINS INPUT (BU1)

PE 1440 - 220V, 50Hz
PE 1709/01 - 200/220/230/240V, 50Hz
PE 1709/02 - 120V, 60Hz

Figure 7.1.2 Physical S

GULATOR

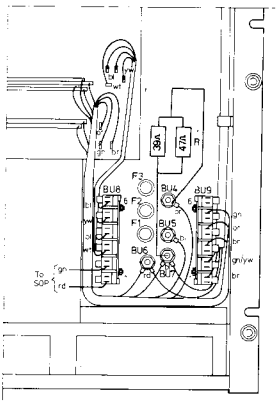


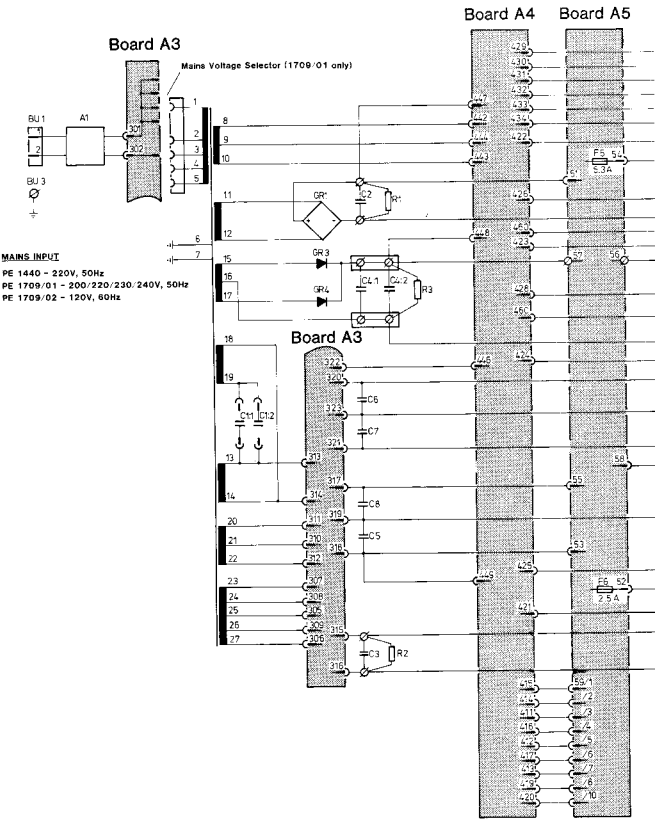
D.C. OUTPUTS (ALL MODELS)

+24V/1.4A, BU9/1 & 2 (GND)
+18V/0.3A, BU9/4
+16V/4.5A, BU4 & BU5 (GND)
+5V/30A, BU6 & BU7 (GND)
-5V/1.3A, BU9/3
-18V/0.3A, BU9/5

ure & Main Characteristics

Later version




Board A4
Board A5
Board A3
Mains Voltage Selector (1709/01 only)
BU1
A1
BU 3
MAINS INPUT
PE 1440 - 220V, 50Hz
PE 1709/01 - 200/220/230/240V, 50Hz
PE 1709/02 - 120V, 60Hz
GR1
C2
R1
GR3
GR4
C4.1
C4.2
R3
Board A3
C11
C12
C6
C7
C8
C5
C3
R2
F5
5.3A
F3
2.5A

REGULATOR

CONNECTOR LOCATIONS

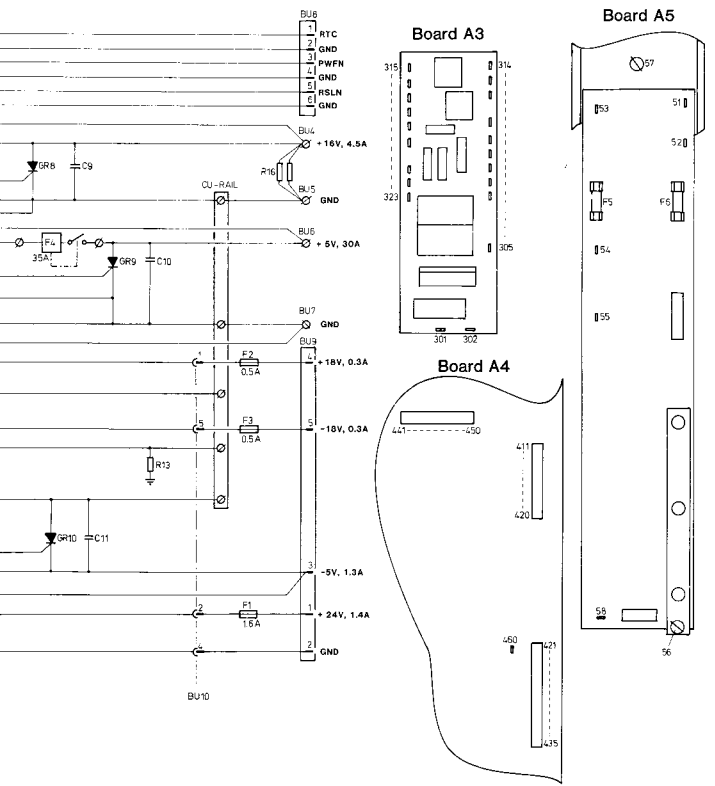
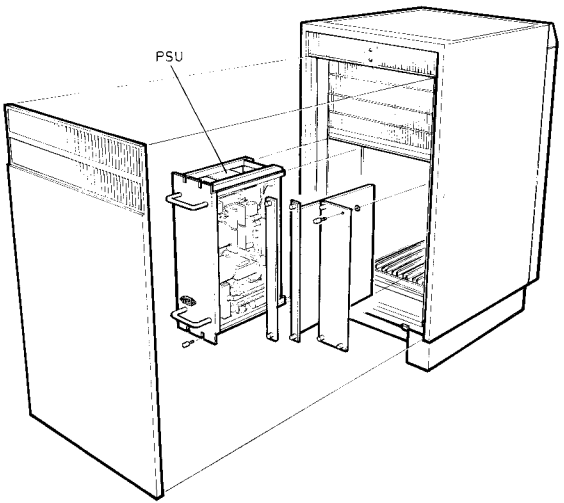


Figure 7.1.3 Submodules & Interconnections

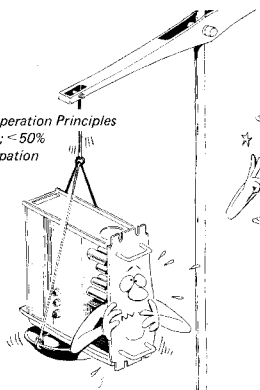


The PE 1726 is a modern, light-weight and high-efficient Power Supply Unit (PSU), that operates according to the switching mode principle. The unit is primarily designed for the Terminal Computers PTS 6812/6813 and the Extension Unit PTS 6864. However, the PSU is a complete sub-module for rack mounting and may also be used in other systems were requirements correspond to the PSU's performance.

Mains Input

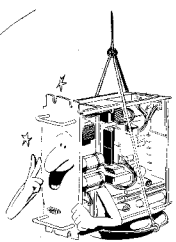
The PSU can be adapted to mains voltages of 100-127V/60Hz or 200-240V/50Hz. An internal strap is used to adapt the unit to either the 100V-range or to the 200V-range. The specific voltage being at hand is then set with a mains voltage selector which can be operated from the outside. This selector can be set to either of the following voltages; 100V, 110V, 120V, 127V, 200V, 220V, 230V and 240V.

The mains voltage should be supplied via an external Magnetic Cicuit Breaker, that switches off at approximately 7.5A.



Earlier PSUs

Conventional Operation Principles
Low Efficiency; <50%
High Heat Dissipation
High Weight



PE 1726

Switching Mode Principle
High Efficiency; >70%
Low Heat Dissipation
Low Weight; 12 kg

Power Supply Unit PE 1726 compared with earlier types of similar PSUs

Output Voltages

Three outputs are provided for suppling 220V AC, two of which can be remotely switched on and off. The switching mode principle of operation is used to produce six D.C. outputs; +24V, ±18V, +16V and ±5V.

TECHNICAL DATA

Mains Requirements

Range 100V: 60Hz ± 2%, 100/110/120/127V ± 10%
Range 200V: 50Hz ± 2%, 200/220/230/240V ± 10%

A.C. Outputs & Remote Control

Supplied Voltages: 3 x 220V ± 10% / 0.4A (in total), 60 or 50Hz ± 2%

Control Signal : FDCN, operating within ordinary TTL levels (0 to +5V). Low level switches off two A.C. outputs.

Switch Frequency

The switch frequency, used for chopping the rectified mains voltage, is 25kHz

D.C. Outputs

Voltage	Accuracy	Maximum Load	Note
+24V	± 5%	2.4A	
+18V	± 5%	0.3A	
-18V	± 5%	0.3A	
+16V	± 2%	6.6A	"Crow bar" at output
+5V	± 3%	43.0A	
-5V	± 5%	1.2A	

Clock and Power Status Signals

The PSU also generates a clock signal (RTC = Real Time Clock) and three power status signals for the supplied computer logic. The RTC frequency is equal to the mains frequency being at hand.

One of the power status signals, POWER ONN, indicates that all D.C. voltages are present. The other two are used to reset the logic (RSLN) and to prewarn the computer of a coming power failure (PWFN).

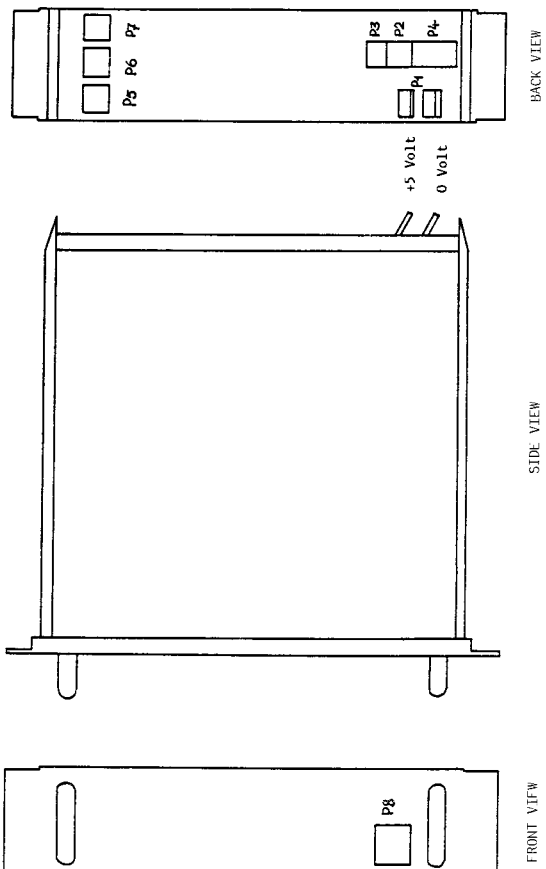


Figure 7.2.1a Connectors on PE 1726

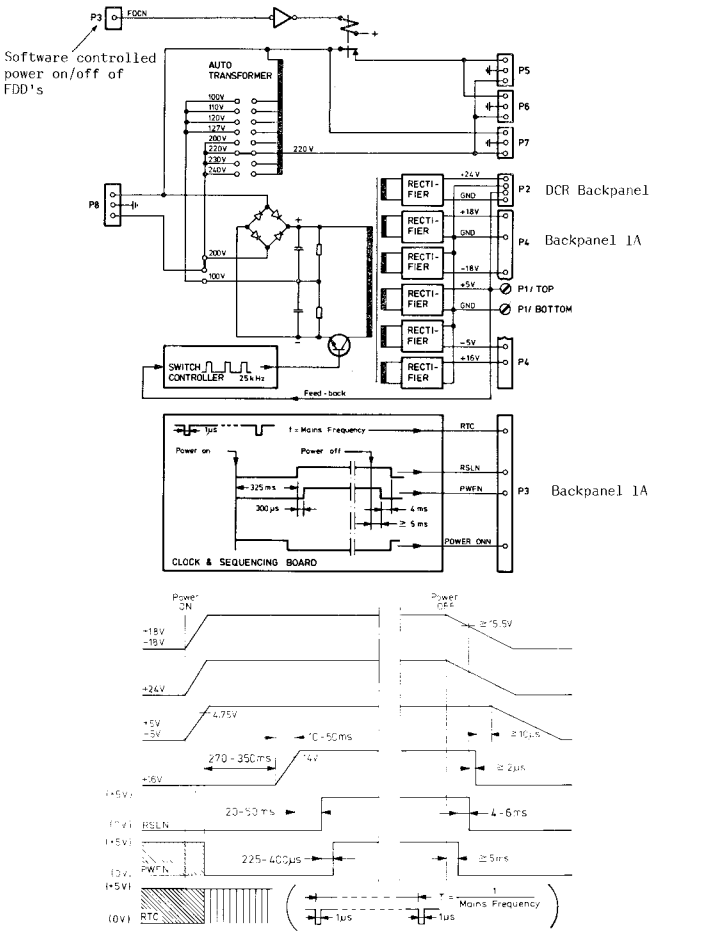


Figure 7.2.1b Sequencing of output voltages at on/off switchings

MAINS VOLTAGE SELECTION

Before connecting the PSU to a mains source the unit must be adapted to the voltage being at hand. First of all the internal strap, Figure 5-1, must be set into the appropriate position;

- Position 100V for mains voltages of 100-127V/60Hz
- Position 200V for mains voltages of 200-240V/50Hz

The mains voltage selector (available at the rear of the PSU) must then be set to the specific voltage being at hand; 100V, 110V, 120V, 127V (lower range) or to 200V, 220V, 230V, 240V (upper range).

CAUTION!

NEVER CHANGE STRAP OR SELECTOR POSITIONS WITH POWER CONNECTED

A.C. Outputs & Remote Control

The autotransformer supplies 220V A.C. via three output plugs. Two of these outputs can be remotely switched on and off via a relay, controlled by the FDCN signal. These outputs are intended for Flexible Disc Drives.

The third A.C. output cannot be controlled and is intended for a fan unit.

Generating D.C. Voltages

The switching mode principle of operation is used to generate the D.C. voltages. This means that the incoming mains voltage is rectified, chopped and transformed into desired low voltages.

Because of the voltage doubling in the 100V range (sub-section 1.4.1), the rectified voltage to be chopped is roughly the same in both the ranges. The chopping is controlled by a 25 kHz switch circuit that senses a feed-back from the +5V output. With the guidance of this feedback the switch circuit can regulate the pulse width, and thereby control the amount of energy transformed to the secondary side.

The low voltages obtained at the secondary side are then rectified and supplied via screw terminals (+5V) and output plugs.

Clock & Power Status Signals

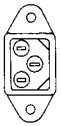
The RTC pulses generated have a duration of 1 µs and are repeated with the mains frequency being at hand.

From the instant of switching on the mains voltage the RSLN signal remains low for about 325 ms. The PWFN remains low for another 300 µs, but at this instant all D.C. voltages have been raised in the required sequence, and the supplied computer logic can start to work.

EXTERNAL INTERFACES

Mains Inlet

The mains inlet (P8) is a male connector, type: Otto Heil 6051-5-4.8.



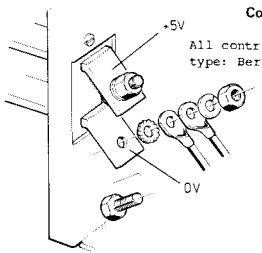
A.C. Outputs

All A.C. outputs (P5, P6 and P7) are male connectors, type: AMP 350547-1.

D.C. Outputs

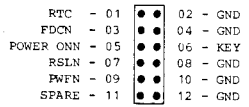
The D.C. voltages are supplied via screw terminals (P1) and two male connectors, P2 (type: Molex 09-81-1061) and P4 (type: Molex 09-81-1091).

Screw Terminal P1

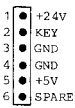


Control Signal Interface

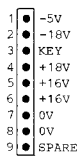
All control signals are taken via the male connector P3, type: Berg 75789-101-12.



Connector P2



Connector P4

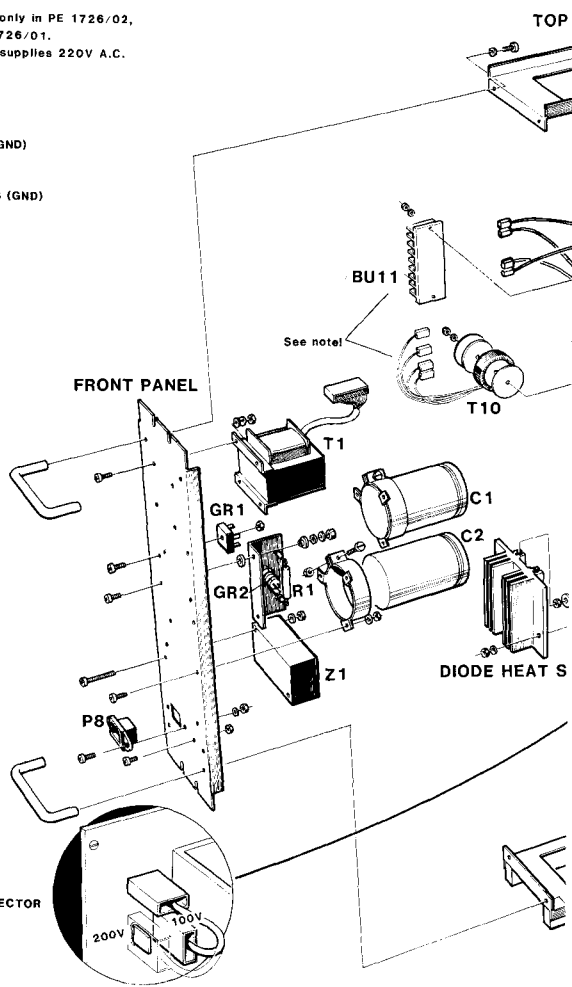


NOTE

T10 and BU11 fitted only in PE 1726/02, or in a modified PE 1726/01. When missing the P7 supplies 220V A.C.

D.C. OUTPUTS

+24V/2.4A, P2/1 & 2 (GND)
+18V/0.3A, P4/4
+16V/6.6A, P4/5,6
+5V/43A, P1, P2/5 & 6 (GND)
-5V/1.2A, P4/1
-18V/0.3A, P4/2
GND, P4/7, 8, 9



MAINS INPUT (P8)

100 - 127V, 60Hz
200 - 240V, 50Hz

PSU – PE 1726/01, 02

Physical Structure & Main Characteristics

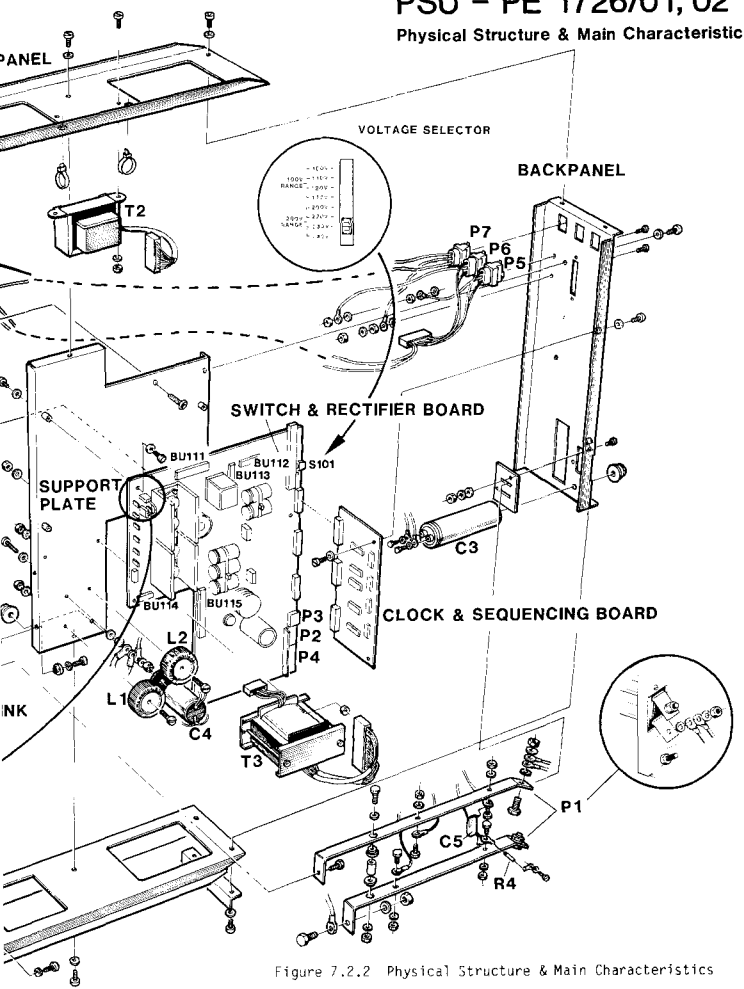
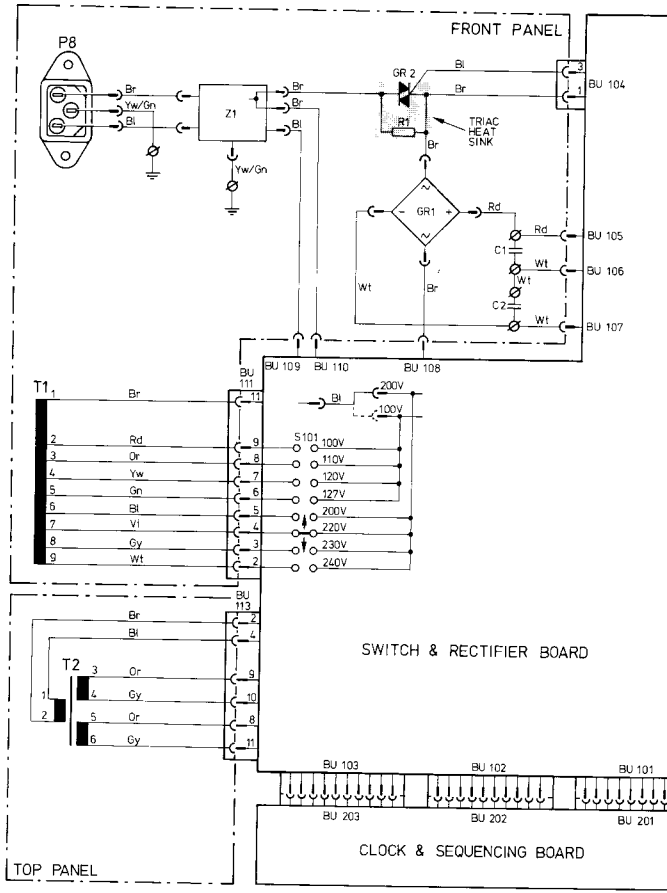


Figure 7.2.2 Physical Structure & Main Characteristics


FRONT PANEL
P8
Br
Yw/Gn
Bl
Z1
Br
Br
Bl
Yw/Gn
GR 2
Bl
Br
R1
TRIAC
HEAT
SINK
Br
3
1
BU 104
GR1
Rd
Rd
C1
BU 105
Wt
BU 106
Wt
Wt
Br
C2
Wt
BU 107
BU 109
BU 110
BU 108
BU
111
T1
1
Br
Bl
200V
100V
2
Rd
3
Or
4
Yw
5
Gn
6
Bl
7
Vl
8
Gy
9
Wt
S101
100V
110V
120V
127V
200V
220V
230V
240V
BU
113
Br
Bl
T2
3
Or
4
Gy
1
2
5
Or
6
Gy
SWITCH & RECTIFIER BOARD
BU 103
BU 102
BU 101
BU 203
BU 202
BU 201
CLOCK & SEQUENCING BOARD
TOP PANEL

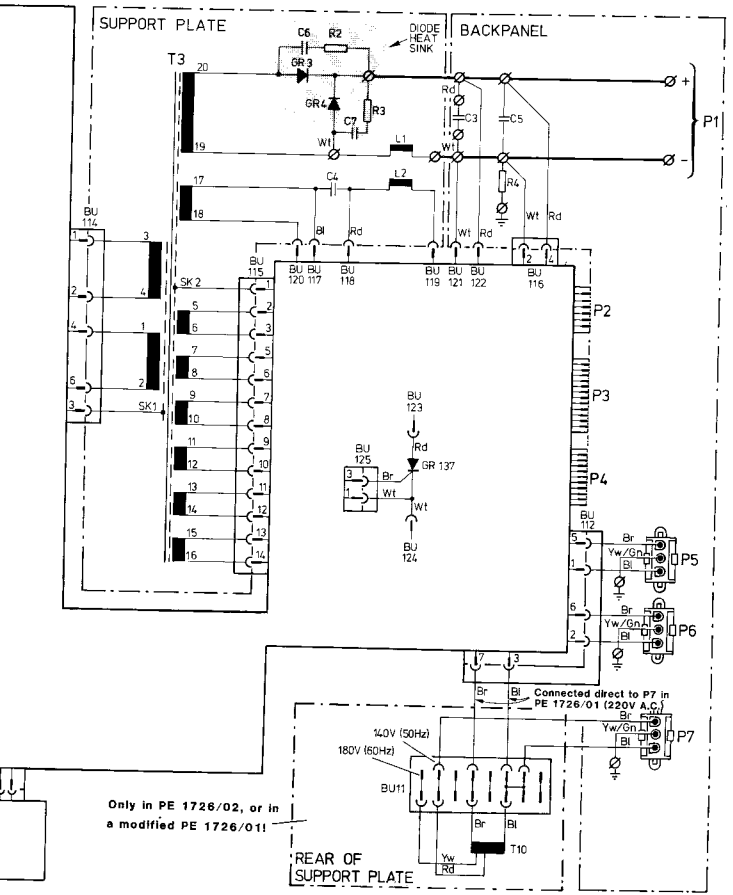
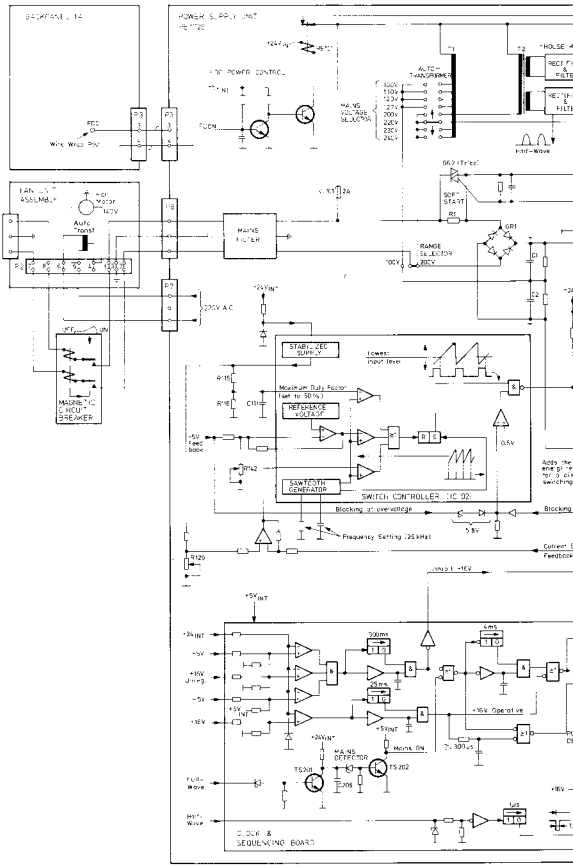


Figure 7.2.3 Submodules & Interconnections


BACKPANEL 1-12
POWER SUPPLY UNIT
FIP POWER CONTROL
MAINS VOLTAGE SELECTOR
AUTO-TRANSFORMER
HOUSE K
RECT FIL
FILTE
Wire Wrap Pin
FAN
Auto Transf
MAINS FILTER
MAGNETIC CIRCUIT BREAKER
RANGE SELECTOR
SOFT START
STABILIZED SUPPLY
Lowest input level
Maximum Duty Factor fixed to 50%
REFERENCE VOLTAGE
SAWTOOTH GENERATOR
SWITCH CONTROLLER (IC 02)
Blocking at overvoltage
Frequency Setting (25 kHz)
Adds the error signal for duty cycle switching
Current Feedback
30ms
4ms
+16V Operative
MAINS DETECTOR
Mains ON
TS 202
TS 201
TS 205
Half-Wave
CLOCK & SEQUENCING BOARD

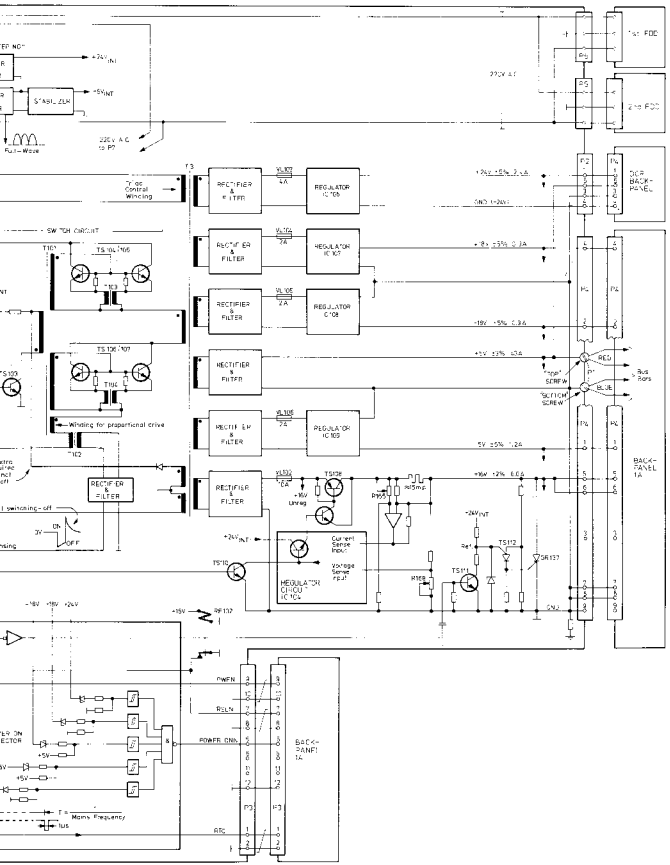


Figure 7.2.4 Functional Block Diagram of the PE 1726

FUNCTIONAL DESCRIPTION

Mains Input

The mains voltage coming in to the computer cabinet is connected to terminal block P2 on the fan unit assembly, and is then wired to a magnetic circuit breaker at the fore top part of the cabinet. The return wires from the breaker are then, via the terminal block, connected to the PSU.

The magnetic circuit breaker is a manually operated ON/OFF switch which automatically goes to the OFF state in case of overloading (> 7.5A).

Primary Rectifying

Range Selection

The mains voltage from the terminal block is taken in via P8 and a mains filter. Depending on the voltage range it is then connected to one of two possible branches. Voltages within the range 200-240V are connected to a full wave rectifier (GR1) and to the upper range input of the autotransformer T1.

A mains voltage between 100V and 127V is instead connected to a branch which leads to the lower range input of T1, and which makes the rectifier circuit operate like a voltage doubler (using just the two "upper" diodes of GR1). This voltage doubling means that the D.C. output of the rectifier circuit is roughly the same for both the mains voltage ranges.

Smooth Start Control

It should be noted that the series resistor R1 limits the starting-up current through the rectifier. The capacitors C1 and C2 would otherwise cause an unpermitted peak current at the instant of switching on the unit. However, when the unit has started to operate, the resistor will successively be short-circuited by a triac (GR2), which is controlled from an auxiliary winding on transformer T3.

Autotransformer & 220V Supply

At the input of the autotransformer T1 there is the Mains Voltage Selector which can be set to eight different voltages, four of each range. Any of the specified input voltages makes the autotransformer produce a 220V A.C. output. This output is used to supply two Flexible Disc Drives (via P5/P6) and a Fan Unit (via P7).

The outputs via P5/P6 are controlled by means of relay RE101. A low input signal (FDCN) on P3/3 stops the 220V supply by energizing the relay.

Internal D.C. Supply

Two voltages, +24V and +5V, are required for internal use within the power supply unit. These voltages are produced at the secondary side of transformer T2. The primary side of this transformer is fed with 200V from the autotransformer T1.

Two unfiltered signals are taken from the +5V rectifier, one Half-Wave and one Full-Wave. These signals are used on the Clock & Sequencing Board and are described later on.

Chopping The Rectified Mains Voltage

The rectified mains voltage is connected across a circuit consisting of a transformer winding provided with two switch transistors in parallel at each end. The winding is the primary one of T3; the transformer which supplies the low-voltages for producing the D.C. outputs.

Each pair of switch transistors is controlled from a separate winding on the secondary side of transformer T101. The primary winding is controlled by a pulse repetition frequency of 25 kHz via transistor TS103. When this transistor is switched on the switch transistors are cut off and vice versa. The emitter transformers T103/T104 are used to equalize the current through the switch transistors.

A third secondary winding of T101 makes the switch circuit operate proportionally, i.e. alterations in the current through the switch transistors (caused by load variations) are reflected back to the base currents.

An auxiliary winding on T3 supplies a voltage which is connected across the primary winding of T101 and transistor TS103. This arrangement gives the extra energi required to distinctly cut off the switch transistors when TS103 is switched on.

Secondary Rectifying & Regulation

General

Six secondary windings on T3 supplies suitable A.C. voltages for producing the six D.C. outputs. All A.C. voltages are rectified and filtered and all except +5V are regulated on the secondary side. The +5V is, as will be explained later, fed back for controlling the switch circuit and is consequently regulated from the primary side of T3.

Regulating +16V

Four of the five secondary regulators just consist of single IC chips, whilst the fifth (for +16V) is more complicated. The +16V is regulated by controlling the series transistor TS108 via a Regulator Circuit. This circuit has one current sense input and one voltage sense input. The current is sensed as a voltage drop across a series resistor of approximately 15 mOhms (part of the PCB foil). A differential amplifier then compares the sensed voltage with a fixed level (set with R165) and provides an amplified difference signal to the Regulator Circuit.

The voltage sense input is supplied from a voltage divider where the sense level may be adjusted with R168.

Across the +16V output there is also a "crow bar", i.e. a thyristor which short-circuits the output in case of over-voltage. The thyristor (GR137) is fired if the voltage exceeds 17.2V, because the uni-junction transistor TS112 is then switched on. Other circuits at the +16V output are explained later on.

Feedbacks to the Switch Controller

There are three feedbacks to the Switch Controller. Besides the +5V output from the secondary side (previously mentioned) there are two feedbacks from the primary side.

One of the primary feedbacks is a current sensing branch in the switch transistor loop. The sensing device is a current transformer (T102) that senses a reflection of the +5V load on the secondary side (other voltages are secondarily regulated and have a small influence on the primary side). The transformer supplies a voltage which, after rectifying and filtering, is compared with a reference voltage (set with R129). The comparison takes place in a differential amplifier that provides an amplified difference signal to the Switch Controller.

The second feedback from the primary side is obtained from another auxiliary winding on T3. This winding supplies a positive pulse each time the switch transistors are cut off.

Switch Controlling

Sawtooth Generator

The Switch Controller (IC102) contains a sawtooth generator that operates with a frequency of 25 kHz (set by means of an external RC network). Each time the generator starts a new ramp, the leading edge of a switch controlling pulse is raised by setting an internal latch element.

Maximum Duty Factor

The duration of this pulse is then depending on the feedback signals, but can never be more than 50% of the period time. This limit, the Maximum Duty Factor, prevents the transformer core from being saturated and is set by the voltage divider R115/R116. The level defined by these resistors is compared with the sawtooth waveform in a differential amplifier. When the sawtooth ramp comes to the fixed level, a signal is obtained which resets the latch element and thereby ends the switch controlling pulse. The capacitor C111 gives a smooth start, i.e. the pulse width is successively increased to the maximum.

Current Sense Feedback

The amplified difference signal from the current sense feedback is similarly compared with the sawtooth waveform in a second amplifier. The difference signal, decreasing when the current increases and vice versa, is scaled to operate below the Maximum Duty Factor. An increasing current will therefore shorten the switch controlling pulses and a decreasing current will make the pulses longer. In this way the Switch Controller regulates the amount of energy transformed to the secondary side.

+5V Feedback

A similar regulation is also effected by the +5V fed back. A part of this voltage (set with R142) is compared with a reference voltage and an amplified difference signal is obtained. This signal, also scaled to operate below the Maximum Duty Factor, controls the width of the switch controlling pulses in the same way as the current sense feedback. A raising voltage results in shorter pulses and a falling voltage gives longer pulses.

Overvoltage Feedback

The +5V fed back is also used to inhibit the output of the Switch Controller in case of over-voltage. If the voltage exceeds +6.4V the output gate will be blocked. This inhibiting method is also used to ensure that no pulse will be let through immediately after cutting off the switch transistors. An auxiliary winding on T3 (previously mentioned) supplies the inhibiting pulse.

Sequencing at Power Start

At the instant of switching on the Power Supply Unit the signal RSLN is active (connected to signal ground via RE102), whilst the signal PWFN is undefined because of no +5V supply. Both signals, generated on the Clock & Sequencing Board, are used for controlling the computer logic during Power Start/Stop sequences.

However, when the +5V output has raised to approximately 4.75V, the internal +5V supply is also operative and the PWFN signal is defined as active (low level). Simultaneously the following also takes place:

- The signal Inhibit +16V is raised and cuts off the series transistor (TS108) at the +16V output.
- A 300 ms monostable flip-flop is triggered (provided that the -5V output and the unregulated +16V are both operative) and maintains the inhibit signal during that period of time.

When the inhibit signal has been ended and the +16V output has come to approximately +14V, a 25 ms monostable flip-flop will be triggered. After these 25 ms the RSLN signal goes high (RE102 now also energized) and after another 300 µs the PWFN signal also goes high.

The power start sequence is now ended and the supplied computer logic can start to work. The reason for delaying the +16V is to establish a well defined reset state of the logic before the memory is made operative with the +16V supply. Otherwise there is a risk of having irrelevant information written into the memory.

Sequencing at Power Stop

When the Power Supply Unit is switched off the capacitor C205 on the Clock & Sequencing Board will be continuously charged (otherwise repeatedly discharged by the Full-Wave signal). The time constant is chosen such that at least 5 ms must elapse before the transistor TS202 switches on and indicates Mains Off. This delay means that mains interrupts shorter than 5 ms will not affect the power supply.

However, when Mains Off is indicated, the PWFN signal goes low and a 4 ms monostable flip-flop is triggered. After these 4 ms the RSLN signal also goes low and switches on the transistor TS111 at the +16V output. This means that the reference voltage to the uni-junction transistor TS112 is lowered to a level which makes the transistor switch on. The "crow bar" is therefore fired and the +16V output is consequently short-circuited. It should be noted that the +5V supply is maintained for another 10 µs, i. e. the memory is made inoperative before a falling +5V may cause an undefined reset state in the logic.

Power On Detector

The six D.C. voltages supplied are all sensed on the Clock & Sequencing Board. If the voltages are close to their nominal values (the accuracy is insufficient to indicate - "within specifications"), Schmitt-triggers will switch and open an AND-gate that indicates Power On. This signal is used to lit an indicator on the System Operator's Panel.

Generating Real Time Clock

The Clock & Squencing Board also contains a circuit for generating a Real Time Clock, a clock signal to the computer logic. This signal is obtained by triggering a 1 µs monostable flip-flop with the mains frequency. The Half-Wave signal previously mentioned is "square formed" by a zener diode and is then used as a trigger pulse.

7.3 PSU PE 1773, for TC 6824

The PSU is built into a frame assembly consisting of a front panel and a back panel, held together by a top and a bottom plate.

The bottom plate is provided with two runners on which the unit can be slid into the computor rack, and on which the unit then stands. The top and bottom of the front panel has screw slots for fixing the unit to the rack. The front panel also has two handles.

The battery module is located externally on the front panel, with the battery input socket above and the mains input socket below. All other external connectors are located on the rear panel.

Three printed circuit boards are included in the PSU; the main board containing switch & rectifier components, one board containing clock and sequencing circuits and a third one containing secondary switch circuits for the back-up voltages. Some components are located directly on the frame.

MAINS INPUT (P11)

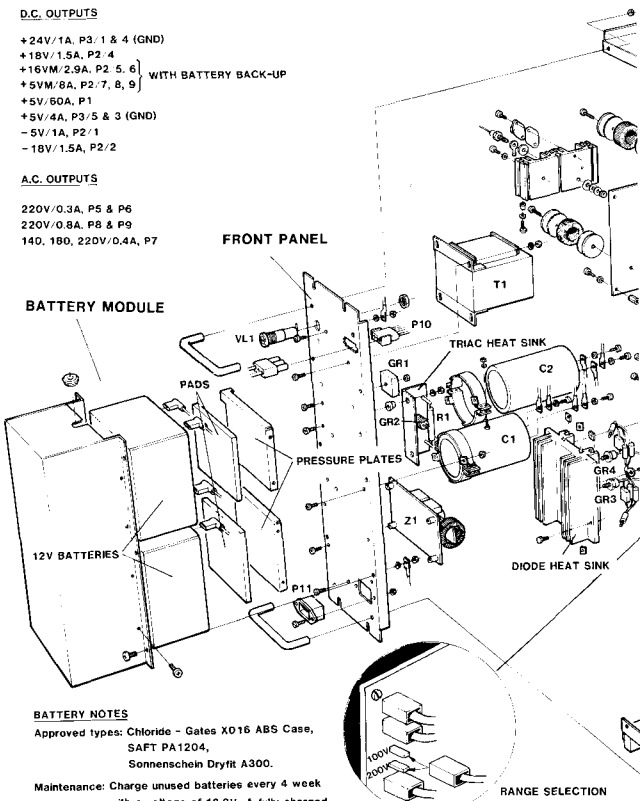
100 - 127V 60Hz
200 - 240V 50Hz

D.C. OUTPUTS

+24V/1A, P3/1 & 4 (GND)
+18V/1.5A, P2/4
+16VM/2.9A, P2/5, 6 } WITH BATTERY BACK-UP
+5VM/8A, P2/7, 8, 9 }
+5V/60A, P1
+5V/4A, P3/5 & 3 (GND)
-5V/1A, P2/1
-18V/1.5A, P2/2

A.C. OUTPUTS

220V/0.3A, P5 & P6
220V/0.8A, P8 & P9
140, 180, 220V/0.4A, P7



BATTERY NOTES

Approved types: Chloride - Gates X016 ABS Case,
SAFT PA1204,
Sonnenschein Dryfit A300.

Maintenance: Charge unused batteries every 4 week with a voltage of 13.8V. A fully charged battery should give at least 12.3V at a load of 0.5A.

PSU – PE 1773

Physical Structure & Main Characteristics

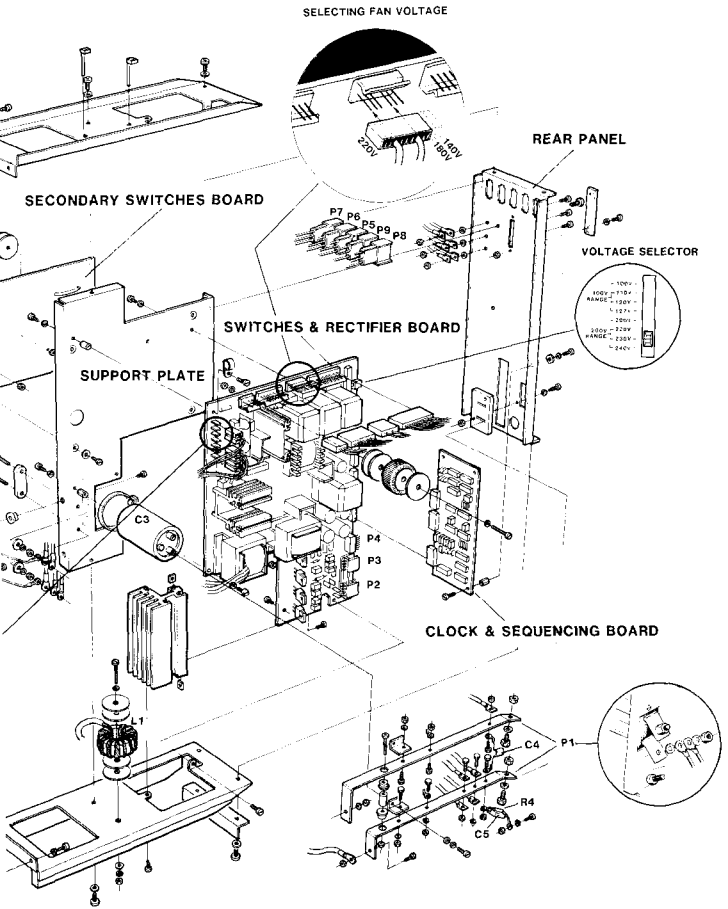
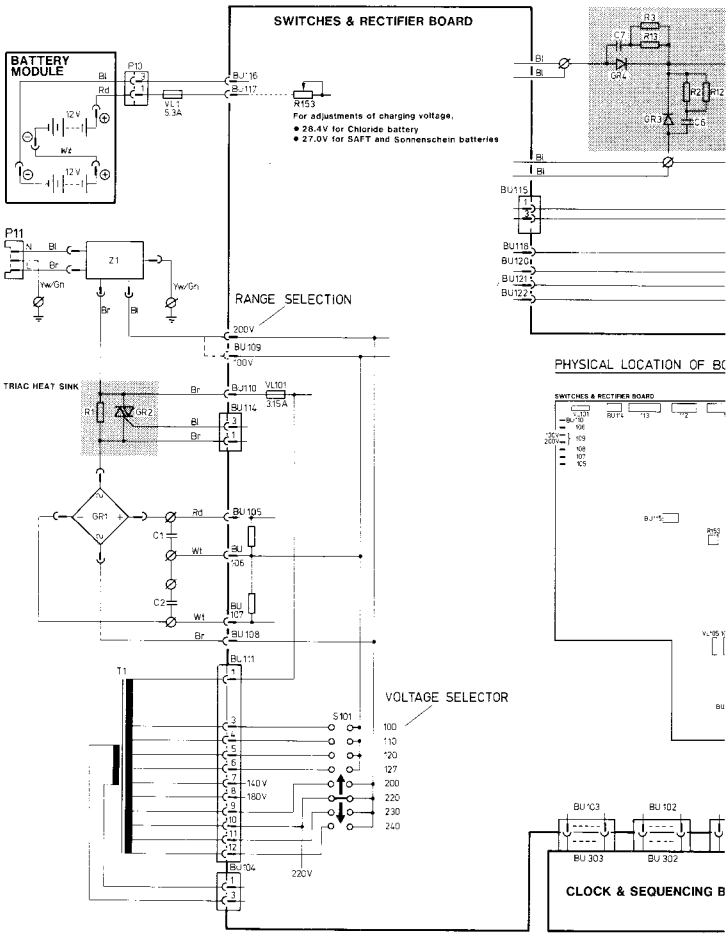


Figure 7.3.1 Assembly PE 1773


SWITCHES & RECTIFIER BOARD
BATTERY MODULE
12 V
12 V
P10
VL1
5.3A
R153
For adjustments of charging voltage,
• 28.4V for Chloride battery
• 27.0V for SAFT and Sonnenschein batteries
R3
R13
GR4
R2
R12
GR3
C6
BU115
BU118
BU120
BU121
BU122
P11
Z1
RANGE SELECTION
200V
BU 109
0V
PHYSICAL LOCATION OF BO
SWITCHES & RECTIFIER BOARD
TRIAC HEAT SINK
R1
GR2
BU110
VL101
3.15A
BU 114
GR1
C1
C2
BU 105
BU 106
BU 107
BU 108
BU 111
T1
VOLTAGE SELECTOR
S101
100
110
120
127
200
220
230
240
140 V
180V
220V
BU 104
BU 103
BU 102
BU 303
BU 302
CLOCK & SEQUENCING B

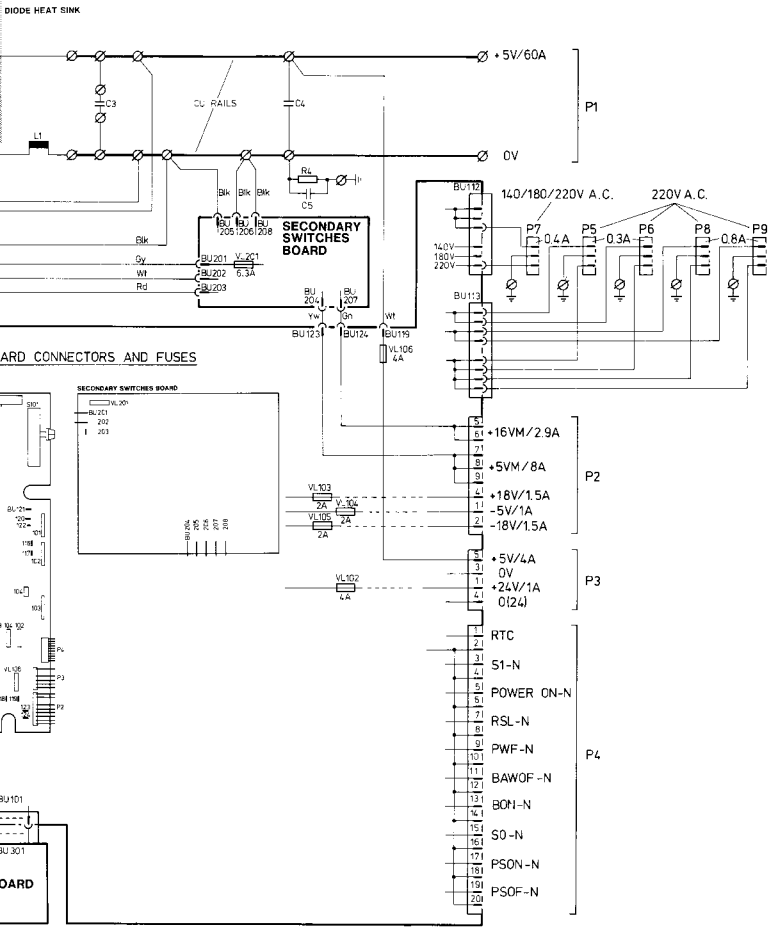


Figure 7.3.2 Internal Interfaces PE 1773

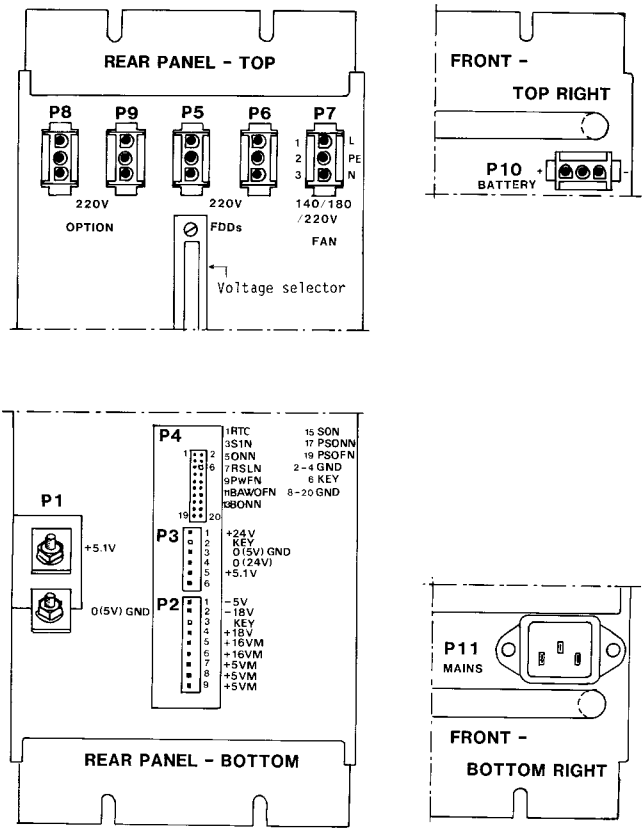


Figure 7.3.4 External Connectors

Rack Mounting

The PSU is slid into the rack on its runners, and is fixed by two screws at the top and the bottom of the front panel.

Connecting Rear Panel Plugs

Figure 7.3.4/5

When the PSU is fitted in the rack, the appropriate sockets can be connected to the PSU's output plugs. Ensure that:

- FDDs are supplied with 220V AC from the plugs P5 and P6.
- Optional equipment should be supplied with 220V from the plugs P8 and P9.
- The fan unit is supplied from plug P7.
- The cables for heavy +5V (5.1V) supply are screwed to terminal P1 as shown in figure

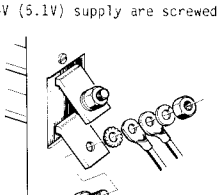


Figure 7.3.5 Fixing Heavy +5V Cables

Installing the Battery

Figure 7.3.6

The battery module, including the two 12V batteries, is delivered separately. The batteries are fully charged at the time when they are leaving the factory.

The batteries should be kept separately until the time for delivery to the customer. Before installation the batteries should be checked and if needed also charged. If the type of batteries is changed the charging voltage may have to be adjusted

When installing the batteries, the red cable from the P10 connector is fixed on the positive pole of one battery, while the blue cable is fixed on the negative pole of the other battery. The loose red cable supplied is used to connect the remaining two poles, completing a series connection.

The batteries are held in place by two pressure plates. A foam-rubber pad is placed between battery and plate. The plates fit into slots on one side of the battery box, while screws are used to fix the plates to the other side. Note that there are two possible positions for the pressure plates, allowing for different battery dimensions.

The battery box itself is fixed by screws to the front panel.

Connecting Front Panel Plugs

Connect the mains plug to the socket P11 and the battery plug to the socket P10 on the front panel.

The PSU is now installed and the terminal computor may be started from the operator's panel.

> **NOTE!**
>
> **The frequency on the RTC line is equal to the mains frequency. The TOSS version used by the system should include the applicable routine for calculating real time.**

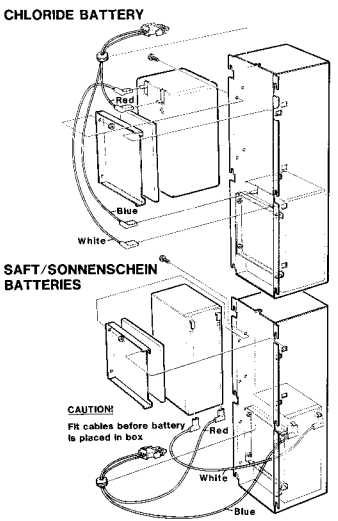


Figure 7.3.6 Battery Module

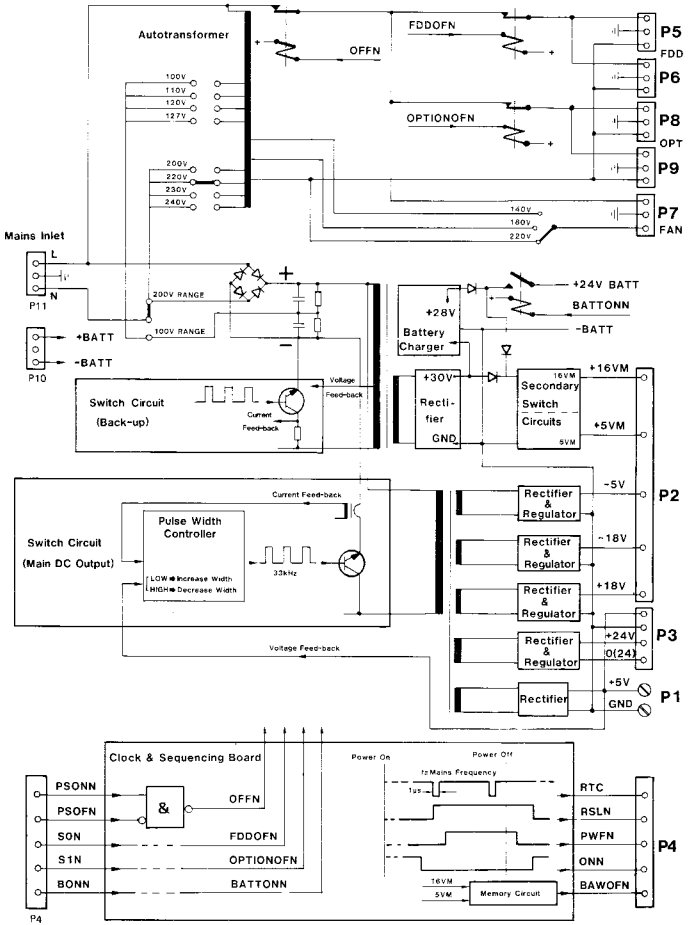
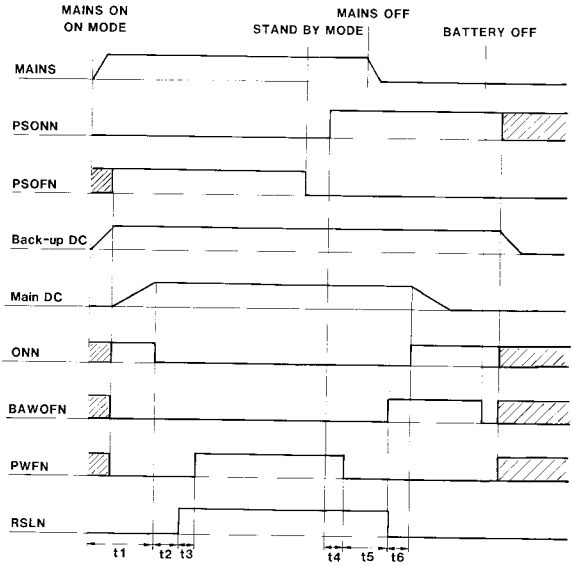


Figure 7.3.7 Block Diagram PE1773



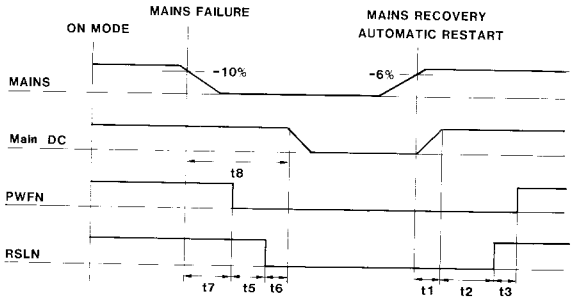


Figure 7.3.8 Sequence of Signals

8.1.1 INSTALLATION Figure 8.1.1

SOP FOR TC 6811

Before fitting the SOP to the computer, ensure that:

- The appropriate text panel is screwed to the front panel.
- The connections between the SOP´s key switch and PCB are made according to Figure.
- The jumpers for selecting loading media are set according to Figure.

Then connect the "lower" flat cable from rack position 5 (CHCR) to P2, and the separate wires terminating on the PCB´s fast-on pins, see Figure.

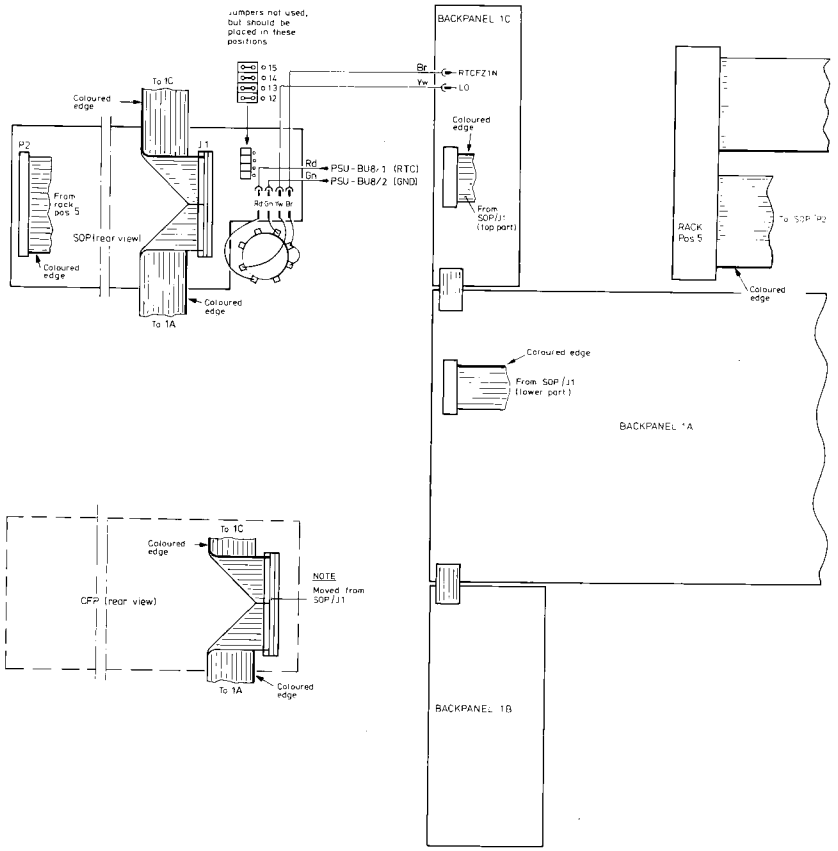


Figure 8.1.1 Installing the SOP for TC 6811

If no CFP is to be fitted, connect also the flat cable from the backpanels 1A and 1C to SOP/J1 (connected to CFP when such a panel is also fitted).

The SOP is then finally screwed to the rack below the digital cassette recorders.

SOP FOR TC 6812/6813 Figure 8.1.2

Before fitting the SOP to the computer, ensure that:

- The appropriate text strip is stuck to the front panel.
- The jumpers for selecting loading media are set according to Figure
- The jumper for selecting operation mode of the ON indicator is set in the desired position, see Figure

Then connect the "lower" flat cable from rack position 10 (CHCR) to P2, and the separate wires terminating on the key switch board and the main PCB, see Figure

If no EFP is to be fitted, connect also the flat cable from P6/P8 to SOP/J1 (connected to EFP when such a panel is also fitted).

NOTE

IF A CFP/EFP IS TO BE FITTED, ENSURE THAT THE LOWER JUMPER ON BACKPANEL 1C IS SET IN THE APPROPRIATE POSITION (FIGURE 8.1.2).

The SOP is then finally screwed to the rack below the flexible disc drives and the cassette recorders.

For SOP-CU straps see CHFD (IN) or CHCR Chapter 17 or 15

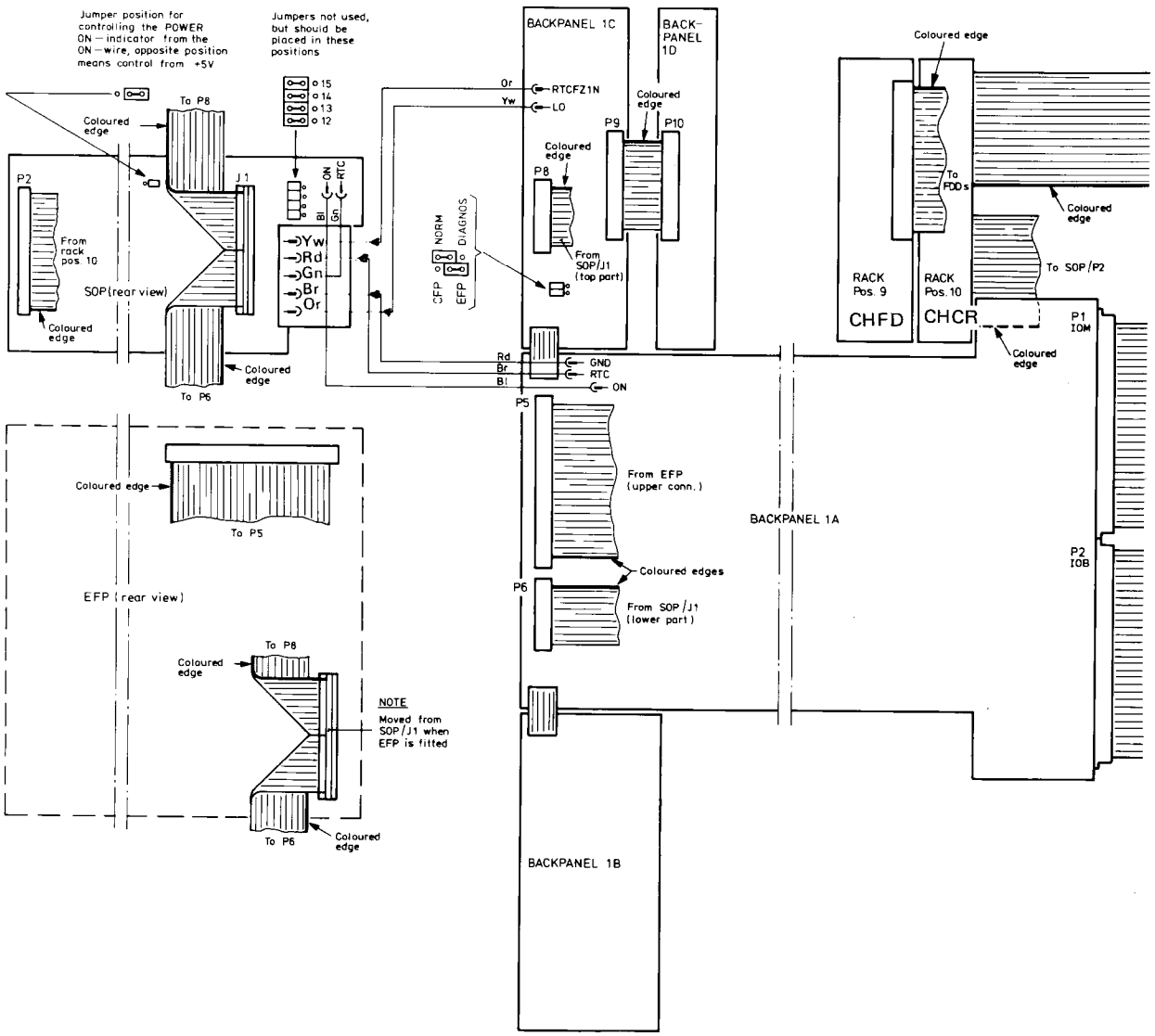


Figure 8.1.2 Installing the SOP for TC 6812/6813

EXTERNAL INTERFACES

Unique Interfaces in SOP for TC 6811

The key switch and J1 interfaces of a SOP for TC 6811 are shown in Figure 8.1.3 The key switch interface is completely unique for this panel, whilst there is a minor difference in the J1 interface, see below.

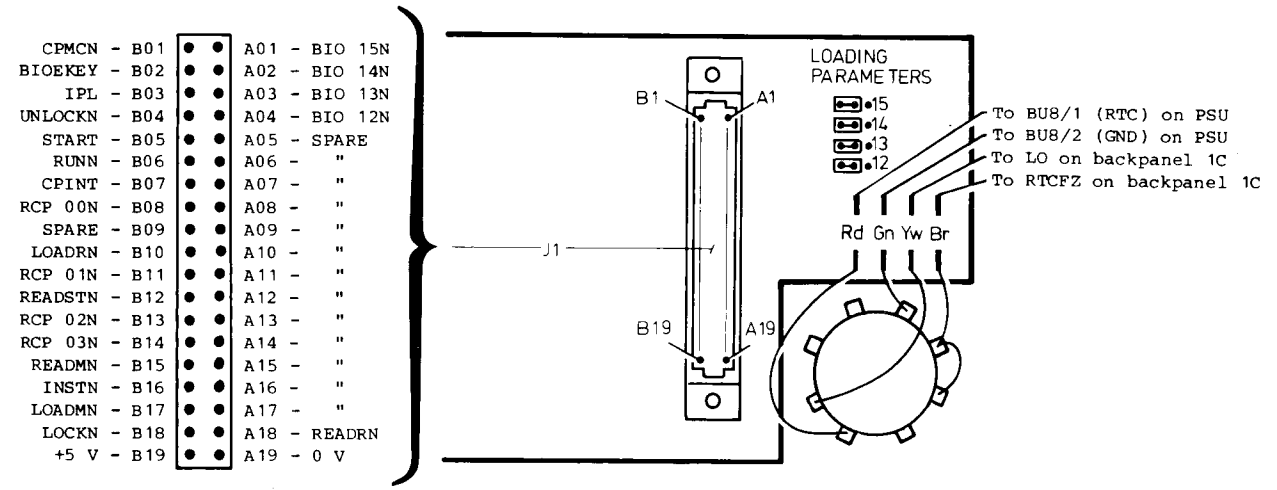


Figure 8.1-3 Interface SOP for TC 6811

Interfaces in SOP for TC 6812/6813

Figure 8.1.4

The interfaces of a SOP for TC 6812/6813 are shown in Figure. Completely unique are here the key switch interface and the connections for controlling the operation mode of the ON indicator. The J1 interface differs just on pin B09, which is here used for the RUNFA signal.

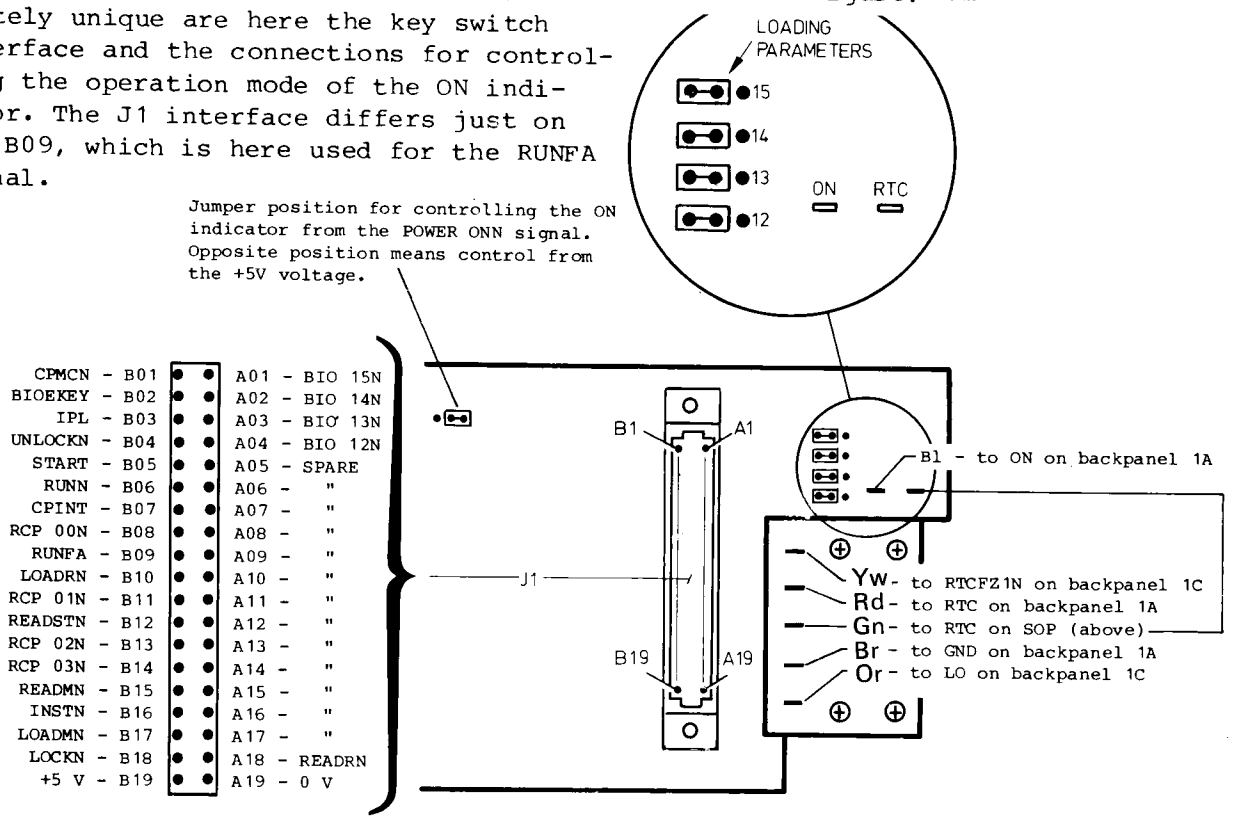


Figure 8.1.4 Interface SOP for TC 6812/6813

Indentical P2 Interfaces

The P2 interfaces of the two panels are identical, see Figure 8.1.5.

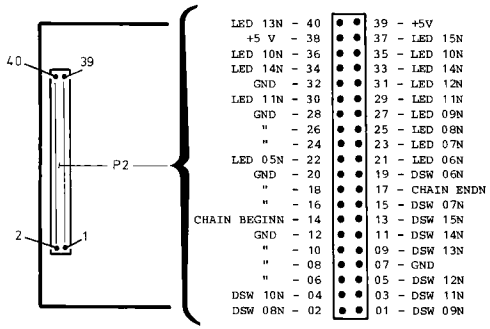


Figure 8.1.5 The P2-interface for both panels

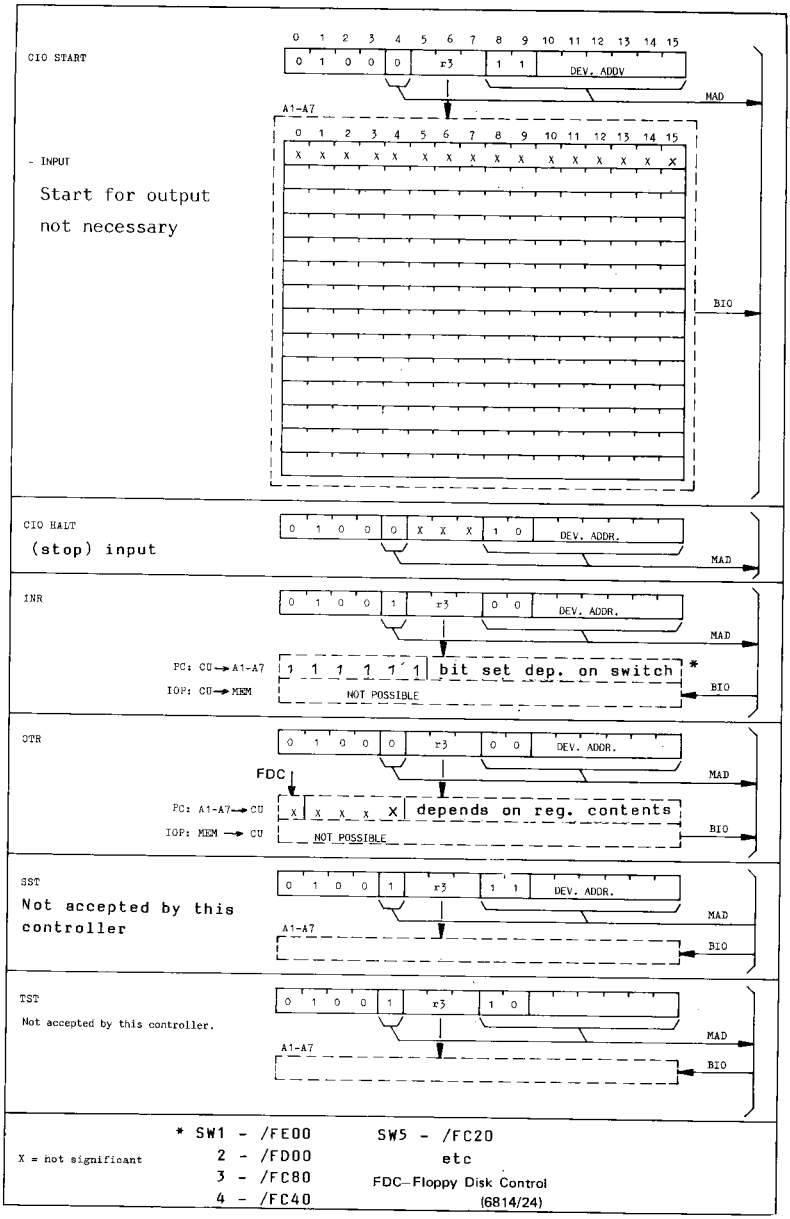


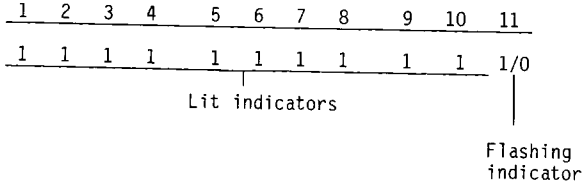
Figure 8.1.6 Instruction-/Command-word Formats

8.1.4 SHORT DESCRIPTION TESTPROGRAM

SOPTSC (rel. 2)

The test program SOPTSC Release 2 can be used for testing the SOP switches and associated indicators on the computers 6805 and 6810-6813.

After loading from cassette or diskette drive (RTC switch in position ON) the SOP indicators 1-10 are all lit and indicator 11 is flashing, indicating that the RTC is enabled.



It should be noted that the program is executed in level 3. Only PWF, RTC, LKM/STACK OVERFLOW can interrupt the program.

2 TEST PROCEDURE

Test the SOP functions as follows:

- Operate the SOP switches 1-10 in turn and check that associated indicators are switched off.
- Operate SOP which 11 and check that the indicators 1-11 are all lit.
- Set the RTC switch in position OFF and check that SOP indicator 11 stops flashing.
- Set the RTC switch in position LOCK and check that SOP indicator 11 is again flashing. Switch the power supply off/on and check that SOP indicator 11 is still flashing.
- Set the RTC switch in position ON. Switch the power supply off/on and check that the program is NOT automatically restarted.

8.1.5 SHORT ROUTINE

```
         DATE  82-05-12          IDENT    SOPTST


0000                             IDENT    SOPTST
0001                    *DATA: 82 05 12 FOR PTS
0002                    *THIS PROGRAM LIGHTS THE LAMP ABOVE THE
0003                    *DEPRESSED SOP SWITCH.  LAMP 11 IS LIT AFTER
0004                    *LOADING
0005                             AORG     /80
0006
0007
0008 0080 FFFF 0000              DATA     /FFFF,0
0009 0084 20BF          START    INH                          NO INTERRUPTS
0010 0086 0101                   LDK      A1,1                TO LIGHT SOPLAMP 11
0011 0088 412E          LIGHT    OTR      A1,0,/2E            LIGHT LAMP
0012 008A 41EE                   CIO      A1,1,/2E            START FOR INPUT
0013 008C 492E                   INR      A1,0,/2E            READ SOP SWITCH
0014 008E 5C04                   RB(NA)   *-2
0015 0090 3941                   SLL      A1,1
0016 0092 5F0C                   RB       LIGHT
0017
0018
0019
0020                             END      START
```

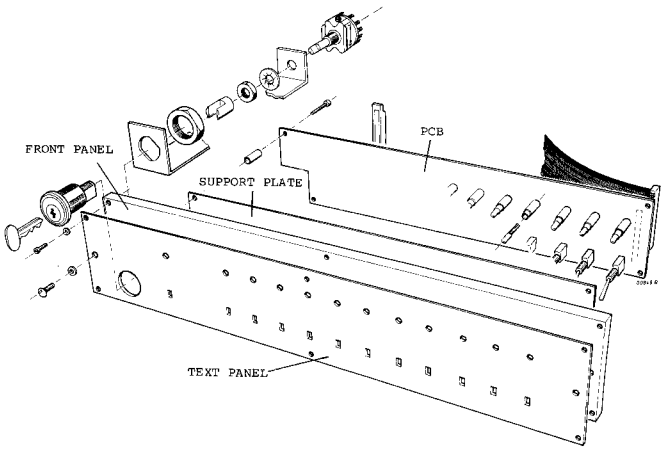


Figure 8.1.7 SOP for TC 6811, Assembly

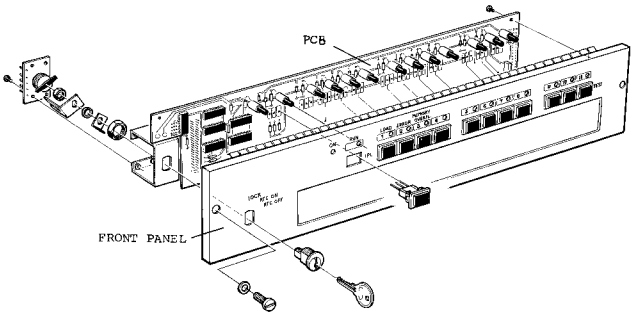


Figure 8.1.8 SOP for TC 6812/6813, assembly

8.1.6 MAINTENANCE

TOOLS

No special tools are required for maintenance actions on the SOPs.

PREVENTIVE MAINTENANCE

Every time a SOP is used, the indicators should be checked by operating the TEST switch.

TROUBLESHOOTING PROCEDURES

The logic circuits of a SOP are of a comparatively low complexity and should not cause any great problems at troubleshooting. No special troubleshooting procedure is therefore advised.

REMOVALS AND REPLACEMENTS

SOP for TC 6811 Figure 8.1.7

The PCB components, including the indicators and toggle switches, are made accessible in the following way:

- Remove connections between PCB and key switch.
- Loosen the four screws at the rear of the PCB, and remove the front panel with attached key switch.
- Unscrew the support plate from the toggle switches and remove it.

Assembling is then made in the opposite order.

SOP for TC 6812/6813 Figure 8.1.8

The PCB components and the push button switches are made accessible by unscrewing and removing the PCB from the front panel.

A push button switch can then be easily pressed out of the front panel from the rear.

When assembling the unit; lay the front panel upside-down and carefully press the PCB on the pins of the switches.

CUSOP Interfaces

P1

SPARE - 01*	●	●	02 - GND
SW3N - 03	●	●	04 - "
OPCN - 05	●	●	06 - "
FDCN - 07	●	●	08 - "
SW2N - 09	●	●	10 - "
SPARE - 11	●	●	12 - "
" - 13	●	●	14 - "
" - 15	●	●	16 - "
MAD04 - 17	●	●	18 - "
SPARE - 19	●	●	20 - "
MAD08 - 21	●	●	22 - "
MAD09 - 23	●	●	24 - "
MAD10 - 25	●	●	26 - "
MAD11 - 27	●	●	28 - "
MAD12 - 29	●	●	30 - "
MAD13 - 31	●	●	32 - "
MAD14 - 33	●	●	34 - "
MAD15 - 35	●	●	36 - "
ACN - 37	●	●	38 - "
SPARE - 39	●	●	40 - "
" - 41	●	●	42 - "
CLEARN - 43	●	●	44 - "
TPMN - 45	●	●	46 - "
TMPN - 47	●	●	48 - "
SPARE - 49	●	●	50 - "

*Top right

P2

SPARE - 01*	●	●	02 - GND
BIO 15N - 03	●	●	04 - "
BIO 14N - 05	●	●	06 - "
BIO 13N - 07	●	●	08 - "
BIO 12N - 09	●	●	10 - "
BIO 11N - 11	●	●	12 - "
BIO 10N - 13	●	●	14 - "
BIO 09N - 15	●	●	16 - "
BIO 08N - 17	●	●	18 - "
BIO 07N - 19	●	●	20 - "
BIO 06N - 21	●	●	22 - "
BIO 05N - 23	●	●	24 - "
SPARE - 25	●	●	26 - "
BIO 03N - 27	●	●	28 - "
BIO 02N - 29	●	●	30 - "
BIO 01N - 31	●	●	32 - "
BIO 00N - 33	●	●	34 - "
BIEC 05 - 35	●	●	36 - "
SCEI - 37	●	●	38 - "
BIEC 03 - 39	●	●	40 - "
BIEC 04 - 41	●	●	42 - "
BIEC 01 - 43	●	●	44 - "
BIEC 02 - 45	●	●	46 - "
BIEC 00 - 47	●	●	48 - "
SPARE - 49	●	●	50 - "

*Top right

P3

LED 13N - 40	●	●	39 - +5V
+5V - 38	●	●	37 - LED 15N
LED 10N - 36	●	●	35 - LED 10N
LED 14N - 34	●	●	33 - LED 14N
GND - 32	●	●	31 - LED 12N
LED 11N - 30	●	●	29 - LED 11N
GND - 28	●	●	27 - LED 09N
" - 26	●	●	25 - LED 08N
" - 24	●	●	23 - LED 07N
LED 05N - 22	●	●	21 - LED 06N
GND - 20	●	●	19 - DSW 06N
" - 18	●	●	17 - CHAIN ENDN
" - 16	●	●	15 - DSW 07N
CHAIN BEGINN - 14	●	●	13 - DSW 15N
GND - 12	●	●	11 - DSW 14N
" - 10	●	●	09 - DSW 13N
" - 08	●	●	07 - GND
" - 06	●	●	05 - DSW 12N
DSW 10N - 04	●	●	03 - DSW 11N
DSW 08N - 02	●	●	01* - DSW 09N

*Bottom right

P4

- 1* - +5V
- 2 - KEY
- 3 - SPARE
- 4 - GND

*Right

PANEL Interfaces

P2

(equal to CUSOP/P3)

P3

KEY - 01*	●	●	02 - RTCE
GND - 03	●	●	04 - IPLRMTN
" - 05	●	●	06 - LOCK
" - 07	●	●	08 - GFETCH
" - 09	●	●	10 - ONN

*Top left

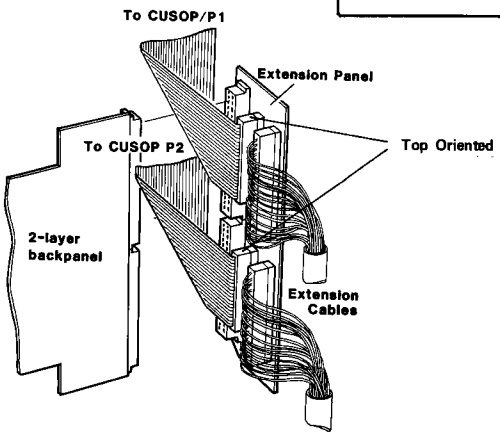
P4

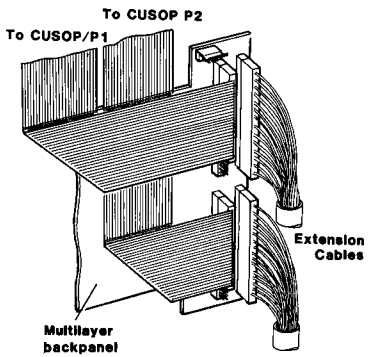
GND - 01*	●	●	02 - BONN
" - 03	●	●	04 - KEY
" - 05	●	●	06 - PSONN
" - 07	●	●	08 - PSOFFN
SPARE - 09	●	●	10 - SPARE

*Top left

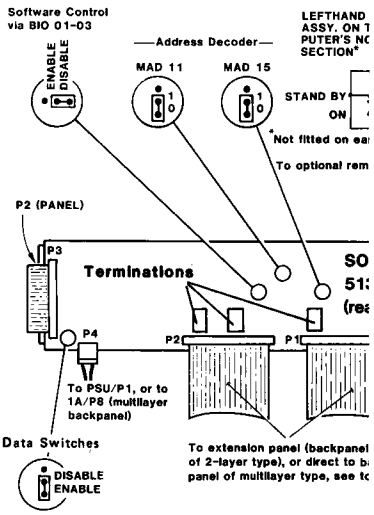
IMPORTANT!

When installing this SOP Assembly in an extended system (TC with one or two EXUs) - remove the terminations fitted on CUSOP, positions 8B, 10B and 14B!





Appli only



NOTE

Early deliveries of TC 6814 may have:

a) a key-operated SOP without CUSOP (513

connected to P1 of a modified CHFD 684

b) a key-operated SOP with CUSOP (5131 1

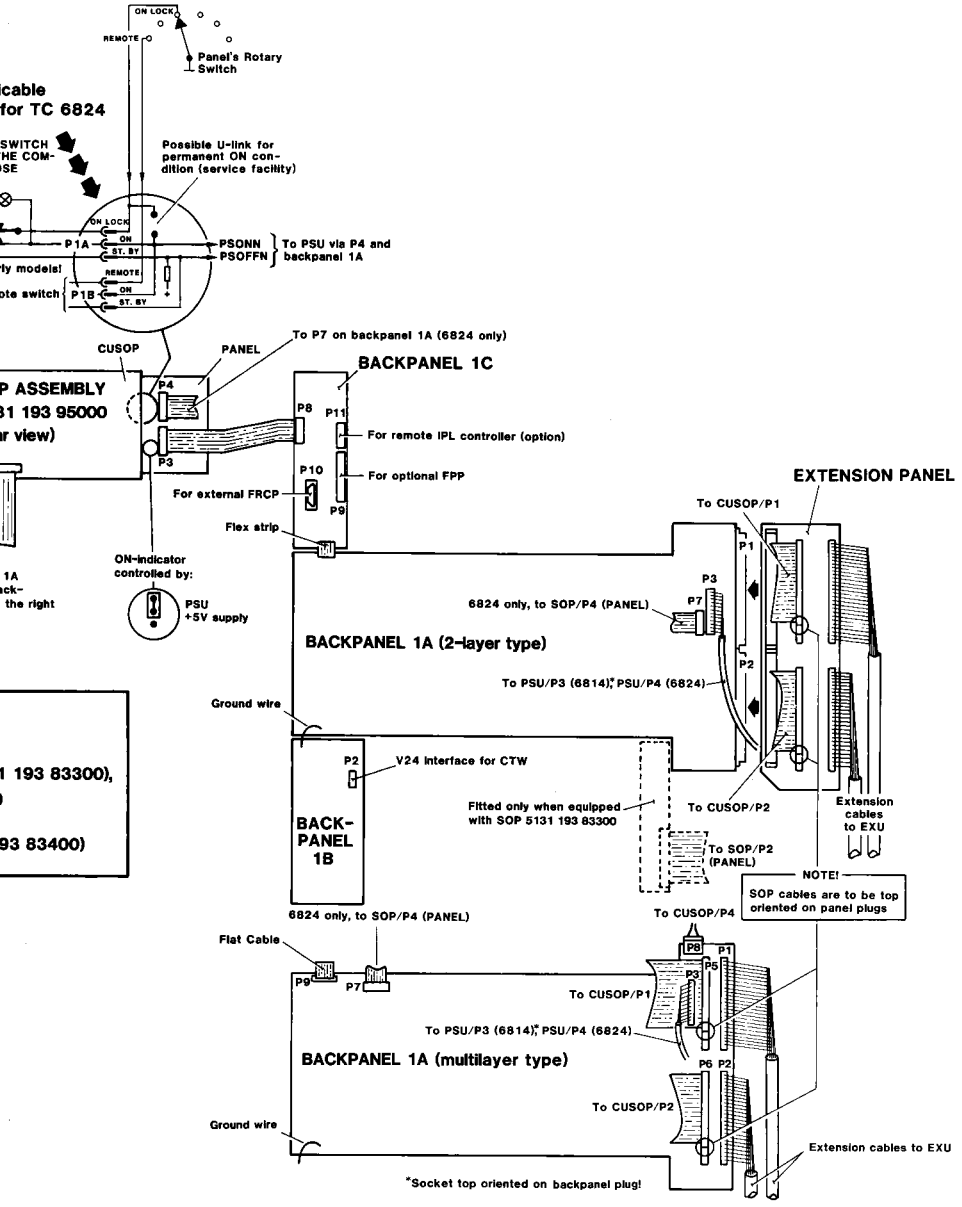
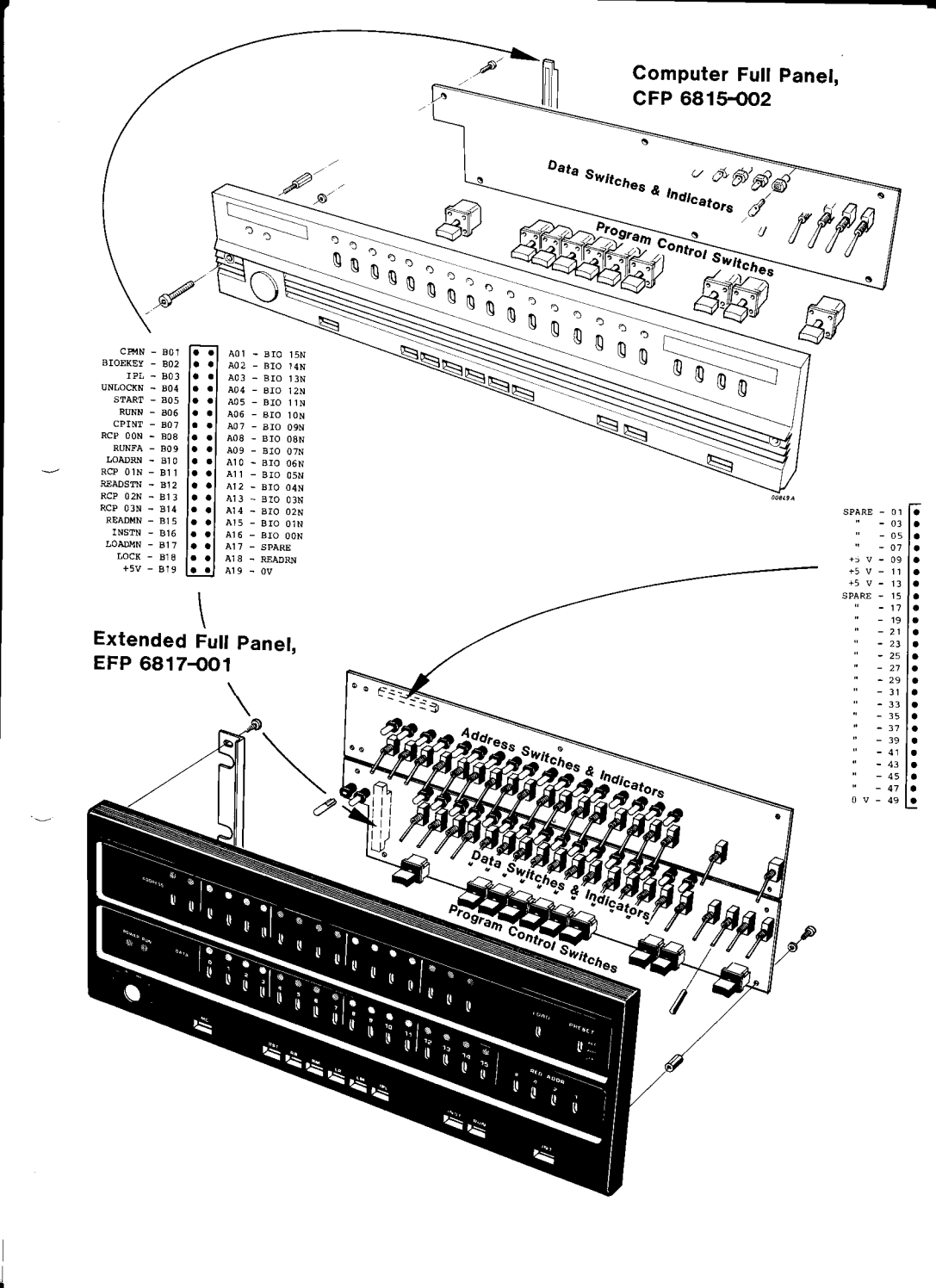


Figure 8.2.2 Interconnections


Computer Full Panel,
CFP 6815-002
Data Switches & Indicators
Program Control Switches
00849A
CPMN - B01
BIOEKEY - B02
IPL - B03
UNLOCKN - B04
START - B05
RUNN - B06
CPINT - B07
RCP 00N - B08
RUNFA - B09
LOADRN - B10
RCP 01N - B11
READSTN - B12
RCP 02N - B13
RCP 03N - B14
READMN - B15
INSTN - B16
LOADMN - B17
LOCK - B18
+5V - B19
A01 - BIO 15N
A02 - BIO 14N
A03 - BIO 13N
A04 - BIO 12N
A05 - BIO 11N
A06 - BIO 10N
A07 - BIO 09N
A08 - BIO 08N
A09 - BIO 07N
A10 - BIO 06N
A11 - BIO 05N
A12 - BIO 04N
A13 - BIO 03N
A14 - BIO 02N
A15 - BIO 01N
A16 - BIO 00N
A17 - SPARE
A18 - READRN
A19 - 0V
SPARE - 01
" - 03
" - 05
" - 07
+5 V - 09
+5 V - 11
+5 V - 13
SPARE - 15
" - 17
" - 19
" - 21
" - 23
" - 25
" - 27
" - 29
" - 31
" - 33
" - 35
" - 37
" - 39
" - 41
" - 43
" - 45
" - 47
0 V - 49
Extended Full Panel,
EFP 6817-001
Address Switches & Indicators
Data Switches & Indicators
Program Control Switches

SERVICE CONTROL PANELS–TC 6811/12/13

CFP/EFP, assemblies & interconnections

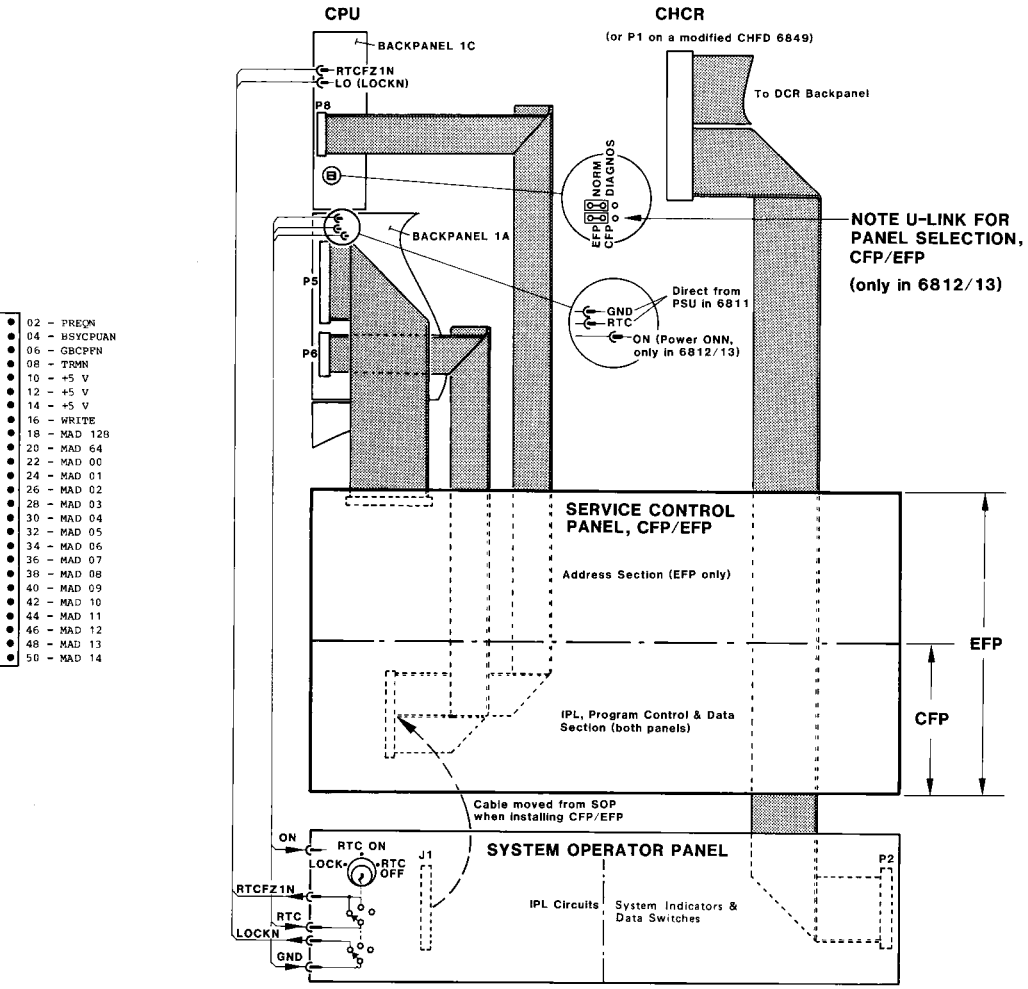


Figure 8.3.1 CFP/EFP, Assembly & Interconnections

8.4 SERVICE CONTROL PANEL - TC 6814/24

The FRCP provides the controls and indicators that enable a user to operate and monitor the system. The pushbuttons are in two groups: the left-side group is used to select system functions; the right-side group to select hexadecimal address and data digits. The left-side indicator is mainly used to display memory and register addresses, the right-side indicator to display memory and register data.

PHYSICAL DESCRIPTION

The FRCP is housed in a box and which can be used up to 10 metres away from the connecting panel.

Note: Before the FRCP is disconnected from the system, the LOCK button must be set rightward to the lock position also for when it has to be connected.

TECHNICAL DATA

PERFORMANCE DATA

Serial Data Interface: V24/28: Transmission Rate = 4.8K baud
Logic Levels : logical 0 = +12V
: logical 1 = -12V

POWER REQUIREMENTS

Voltage	: +5V ± 0.25V	+12V ± 1.2V	-12V ±1.2V
Current (max.)	: 800mA	150mA	20mA

INTERFACE

Pin No.	Signal	Function
J1-1	LOCK	When LOCK = 1, FRCP is inhibited except for INT
2	SDMP	Serial Data Master to Panel
3	OV(GND)	
4	+5V	(for remote version, down to +4V (V_{LINE})
5	+12V	Logic level 0 of serial data
6	SDPM	Serial Data Panel to Master
7	RTCE	Real Time Clock Enable (active at "1")
8	RESETN	Reset Not
9	-12V	Logic level 1 of serial data

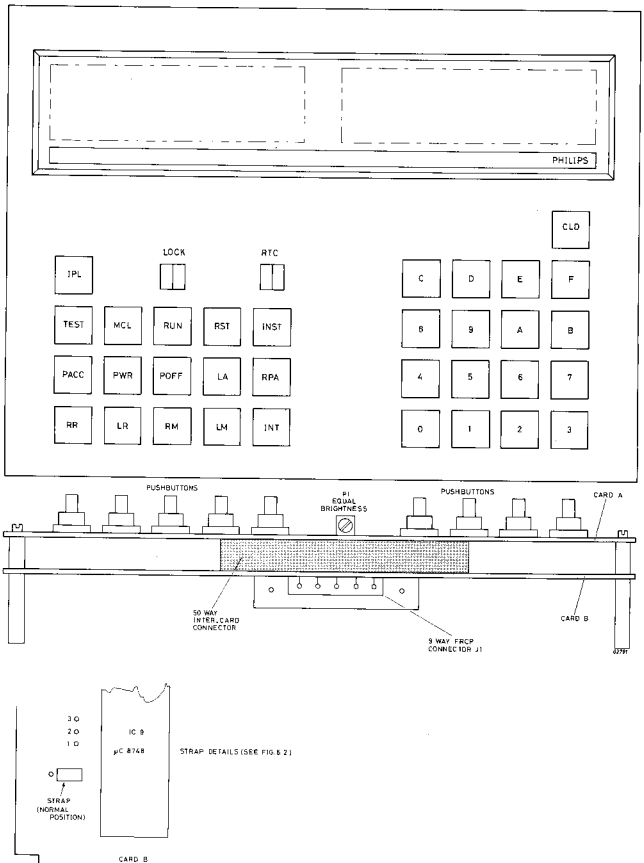


Figure 8.4.1 FRCP Details

SWITCH SELECTION:	HEXADECIMAL CODE:
0 to F	Address: / Bx Bx Bx Bx Bx Bx (leading zeros are not keyed in) Red Addr. / 3x Data: / 3x 3x 3x 3x (leading zeros are not keyed in) where x is the selected hex. digit in the range 0 to F.
MCL	/40
LR	/41
RR	/42
RST	/43
IPL	/44
LM(1)	/45
LM(2)	/55
INT	/46
RM(1)	/47
RM(2)	/57
LA	/48
INST	/49
RPA	/4A
RUN	/4B
PACC	/4C
PWR	/4D
POFF	/4F
TEST	/4E
Serial Data Panel-to-Master Codes	

SDPM CODES

FUNCTION NAME	FUNCTION	HEXADECIMAL CODE
RUNZO	CPU mode changed from RUN to IDLE	/40
RUNZ1	CPU mode changed from IDLE to RUN	/41
TEST	Production testing only	/42

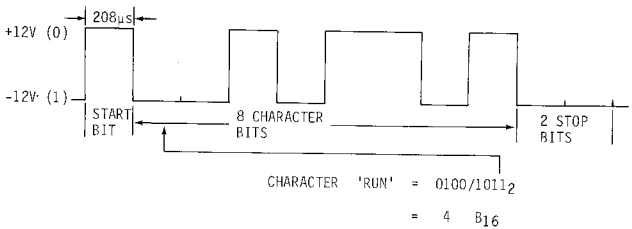
Serial Data Master-to-Panel Codes

Note: To distinguish between master-to-panel data and hand-entered data, the display of master -to-panel data is preceded by two small zeros e.g.: □□1625.
When the preset stop-on-address function is operative, the display of master-to-panel data is preceded by 'P' and one small zero e.g.: P□1625.

HEXADECIMAL CODE FORMAT

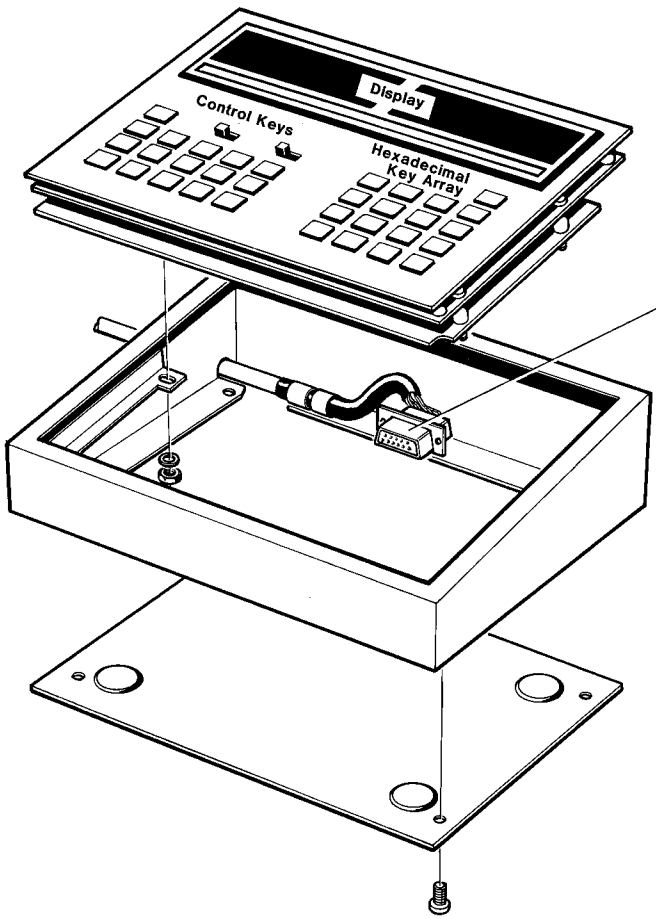
1 start bit, 8 character bits, 2 stop bits

EXAMPLE:



Note that the least significant bit is transmitted first.

Figure 8.4.2 SDMP Codes and Code Formats


Display
Control Keys
Hexadecimal
Key Array
-12V - 09
RESETN - 08
RTCE - 07
SDPM - 06

Connection to Backplane of TC 6814/24

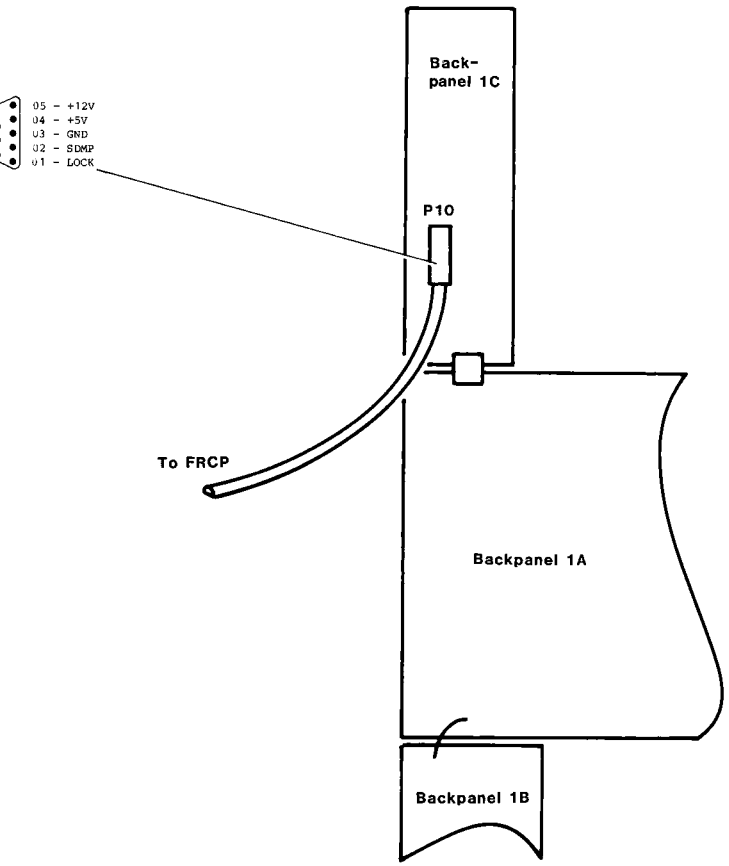
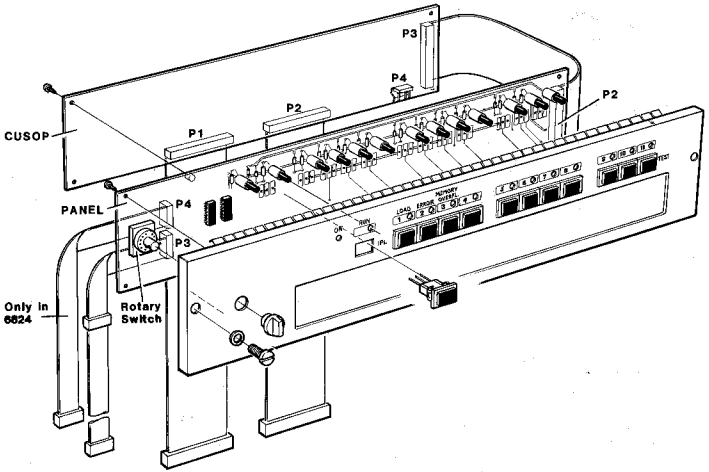


Figure 8.4.3 FRCP, Assembly & Interconnection

SOP Assembly 5131 193 95000 with integrated Control Unit (CUSOP)



NOTE

Early deliveries of TC 6814 may have:

a) a key-operated SOP without CUSOP (5131 193 83300), connected to P1 of a modified CHFD 6849

b) a key-operated SOP with CUSOP (5131 193 83400)

Figure 8.2.1 Assembly & Interfaces

9.1 CPU 852-6810/12

LIST OF ILLUSTRATIONS

LIST OF TABLES

9.1 CPU 852-6810/12 IDENTIFICATIONS

P852 CPU-board (CPA) with intergrated Ser. Cu (current loop)
Type-number: see chapter 1: for P6810 and 6812

Test-programs:

CPU	-	CPUTSC
Intgr. CU	-	PERTST

Devices:

PER 3100	-	PTS 6862-001

Power consumption +5V 6A

9.2 INSTALLATION DETAILS

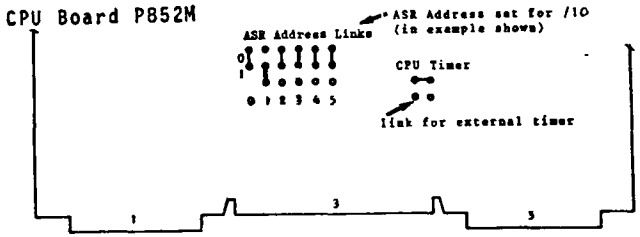


Figure 9.1 STRAPSETTING ON CPU 852 BOARD

9.3 INTERFACE CONNECTIONS

1A01	0V
1A02	PIFN
1A03	CPFN
1A04	ISO2N
1A05	PFFN
1A06	BIEC4
1A07	BIEC2
1A08	BIEC5
1A09	ISO6N
1A10	ISO3N
1A11	ISO1N
1A12	INTASRN
1A13	
1A14	
1A15	
1A16	
1A17	
1A18	
1A19	
1A20	
1A21	
1A22	
1A23	
1A24	
1A25	
1A26	
1A27	
1A28	
1A29	
1A30	
1A31	
1A32	
1A33	
1A34	
1A35	
1A36	
1A37	

1B01	ASR LINE
1B02	RTC AN
1B03	SCEIN
1B04	ISO5N
1B05	ISO4N
1B06	RTCFZ1N
1B07	BIEC1
1B08	BIEC3
1B09	BIEC0
1B10	ISO7N
1B11	ISOON
1B12	
1B13	
1B14	
1B15	
1B16	
1B17	
1B18	
1B19	
1B20	
1B21	
1B22	
1B23	
1B24	
1B25	
1B26	
1B27	
1B28	
1B29	
1B30	
1B31	
1B32	
1B33	
1B34	
1B35	
1B36	
1B37	

Table 9.1 CPU-A, CONNECTOR 1 (ASR CU)

5A01		5B01	
5A02		5B02	
5A03		5B03	
5A04		5B04	
5A05		5B05	
5A06		5B06	
5A07		5B07	
5A08		5B08	
5A09		5B09	
5A10		5B10	
5A11		5B11	
5A12		5B12	
5A13		5B13	
5A14		5B14	
5A15		5B15	
5A16		5B16	
5A17		5B17	
5A18		5B18	
5A19		5B19	
5A20		5B20	
5A21		5B21	
5A22		5B22	
5A23		5B23	
5A24		5B24	
5A25		5B25	
5A26		5B26	
5A27		5B27	
5A28		5B28	
5A29	BIOEKEY	5B29	CPMCN
5A30	UNLOCKN	5B30	IPL
5A31	RUNN	5B31	START
5A32	RCPOON	5B32	CPINT
5A33	LOADRN	5B33	RUNFA
5A34	READSTN	5B34	RCPO1N
5A35	RCPO3N	5B35	RCPO2N
5A36	LOADDMN	5B36	READMN
5A37	READRN	5B37	INSTN

Table 9.2 CPU-A, CONNECTOR 1 (ASR CU)

Signal name	Pin No. (Line Connector P5)	CPU
Transmitted Data (V24)	2	
Received data (V24)	3	
+5V	16	
Output Ground	15	1A01
Output Line	14	1B01
Output Line	13	
Output Source	12	
Input Ground	11	
Input Line	10	
Input Line	9	
Input Source	8	
Ground	6	
Source	5	
Protective ground	1	
Signal Ground	7	

Table 9.3 PER 3100 INTERFACE

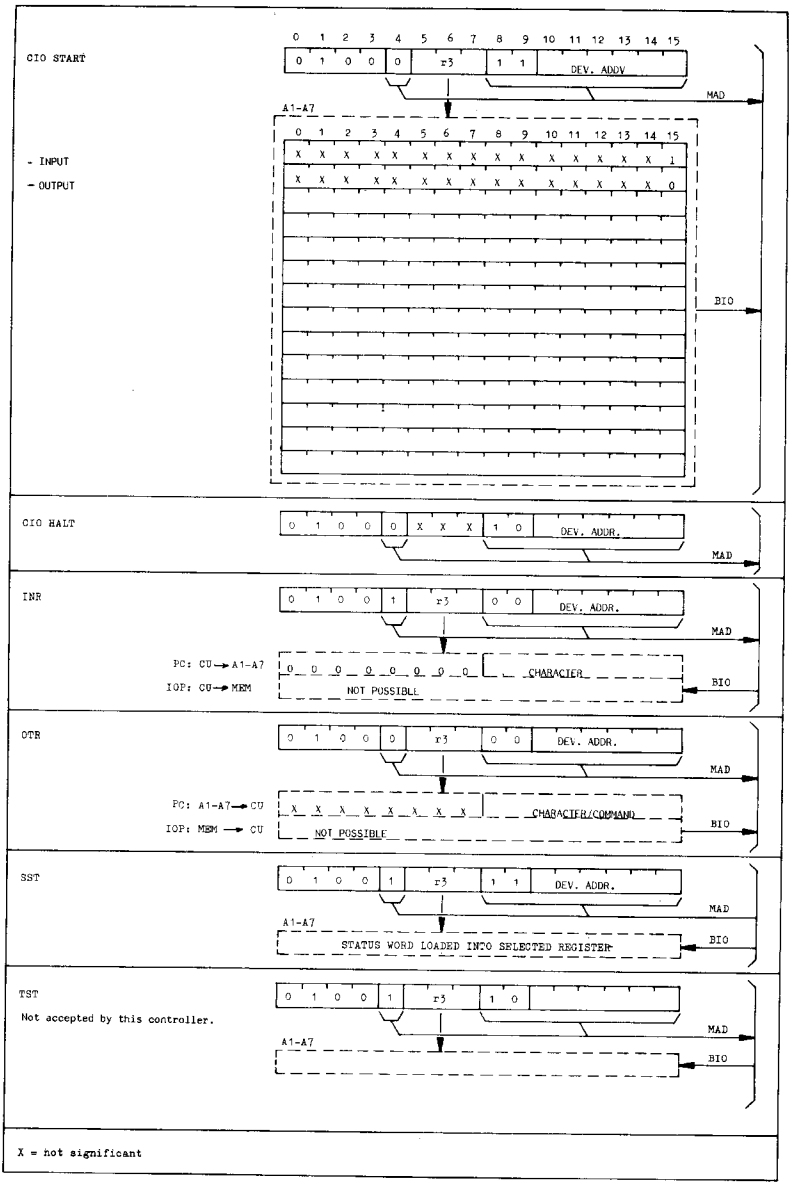


Figure 9.2 INSTRUCTION-/COMMAND-WORD FORMATS

9.4.1 STATUSWORD:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

No error detection by the Controller

9.5 SHORT DESCRIPTION TESTPROGRAM CPU TSC (REL 2)

The test program CPUTSC Release 2 can be used for testing the CPU functions in the following computers:

- 6805 (CPU: P851)
- 6810/11/12 (CPU: P852)
- 6810/11 upgraded with UK 01 (CPU: P857)
- 6813 (CPU: P857)

Basic testing requires no extra equipment, a cassette or diskette drive and the SOP provide the necessary man-to-machine interfaces.

Program Load & Initiation

When the program has been loaded from a cassette or a diskette drive, it will automatically start a short sequence for initiating timers and identifying the type of CPU. Then it stops and lights the following SOP indicators (marked with 1):

1	2	3	4	5	6	7	8	9	10	11
1	1	0	0	0	X	X	X	0	0	0
					↓	↓	↓			
					0	0	0	: CPU = P852		
					0	0	1	: CPU = P851		
					1*	1	0	: CPU = P857		

*When testing a 6810/11 that has been upgraded with UK 01, reset this position by operating SOP switch 6. (Changes the parameter '4 ms' to '2 ms', see section 3.1)

Program Run & Error Indications

Start the program by operating SOP switch 1. The program will now run in loop mode until an error is found, or until it is stopped by another operation of SOP switch 1.

Each cycle of the loop takes about 1 ms, and the number of completed cycles is continously counted in binary form on the SOP indicators 1-8.

To test the power on/off handling; switch the computer's power off/on whilst the program is running (ensure that the RTC switch is set in position LOCK).

If the program stops on an error, the three right-most SOP indicators will display the main function that has failed:

9	10	11	
0	0	1	= Power On/Off Error
0	1	1	= Invalid Instruction Code
1	0	1	= Unwanted Interrupt
1	1	1	= Processing Error

PERTST

Codes 40 - 48 see PERTST

ASR, PTS 3100, and DISPLAY

These peripherals and their CU's can be checked with the aid of two small programs called Line, and Echo, if the standard test program either cannot be loaded or if it will not run.

Program Line

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	20BF		INH	
0088	0200		LDK	A2,0
008A	4BD0		SST	A3,/10
008C	42D0		CIO	A2,1,/10
008E	5C04		RB(NA)	* -2
0090	8520	OUTCR	LDKL	A5,/0A0D
0092	0A0D			
0094	4510	OUT	OTR	A5,0,/10
0096	5C04		RB(NA)	* -2
0098	3D68		SRL	A5,8
009A	5C08		RB(NZ)	OUT
009C	4610	OUTCH	OTR	A6,0,/10
009E	5C04		RB(NA)	* -2
00A0	1201		ADK	A2,1
00A2	EA1C		CWR	A2,A7
00A4	5C0A		RB(NE)	OUTCH
00A6	0200		LDK	A2,0
00A8	5F1A		RB	OUTCR

- Load the ASCII character in register A6.
- Load the number of times you wish the character to be repeated into register A7.
- Load the start address of the program into register A0. (/0086)
- Push the RUN button.

Program Echo

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	20BF		INH	
✳ 0088	0201	IN	LDK	A2,1
008A	42D0		CIO	A2,1,/10
008C	5C04		RB(NA)	* -2
008E	4B10		INR	A3,0,/10
0090	5C04		RB(NA)	* -2
0092	4290		CIO	A2,0,/10
0094	4CD0		SST	A4,/10
0096	5C04		RB(NA)	* -2
0098	0200		LDK	A2,0
009A	42D0		CIO	A2,1,/10
009C	5C04		RB(NA)	* -2
009E	4310		OTR	A3,0,/10
00A0	5C04		RB(NA)	* -2
00A2	4290		CIO	A2,0,/10
00A4	4CD0		SST	A4,/10
00A6	5C04		RB(NA)	* -2
00A8	5F24		RB	IN

✳ change to 0088 0221 in LDK A2,/21 for 856/7

Program echo:

Once loaded and started any input character from the keyboard will be printed, displayed or executed on the device.

10 CPU 857-6813

LIST OF ILLUSTRATIONS

LIST OF TABLES

1A01	0V
1A02	PIFN
1A03	CPFN
1A04	IS02N
1A05	PFFN
1A06	BIEC4
1A07	BIEC2
1A08	BIEC5
1A09	IS06N
1A10	IS03N
1A11	IS01N
1A12	INTASRN (INTSERN)
1A13	
1A14	
1A15	
1A16	
1A17	
1A18	
1A19	
1A20	
1A21	
1A22	
1A23	
1A24	
1A25	
1A26	
1A27	0V
1A28	5V
1A29	
1A30	Mech. Ground
1A31	CT103
1A32	CT104
1A33	CT106
1A34	CT107
1A35	CT1082
1A36	CT109
1A37	CT133

1B01	ASR LINE
1B02	RTC AN
1B03	SCEIN
1B04	IS05N
1B05	IS04N
1B06	RTCFZ1N
1B07	BIEC1
1B08	BIEC3
1B09	BIEC0
1B10	IS07N
1B11	IS00N
1B12	
1B13	
1B14	
1B15	
1B16	
1B17	
1B18	
1B19	
1B20	
1B21	
1B22	
1B23	
1B24	
1B25	
1B26	
1B27	0V
1B28	5V
1B29	
1B30	
1B31	0V
1B32	0V
1B33	0V
1B34	0V
1B35	0V
1B36	0V
1B37	0V

Table 10.1 CPU B CONNECTOR 1 (V24 CU)

5A01		
5A02		
5A03		
5A04		
5A05		
5A06		
5A07		
5A08		
5A09		
5A10	*	SP03
5A11	*	FLOACTN
5A12	*	BSYCPUAN
5A13	*	GFETCH
5A14	*	DONEFN
5A15	*	FLOCR1
5A16		
5A17	*	OSCFLO
5A18		
5A19	*	MMUABS
5A20	*	DONEMN
5A21	*	BOMFN
5A22	*	FU
5A23	*	S01
5A24	*	S03
5A25	*	SP02
5A26		
5A27	*	0V
5A28	*	5V
5A29		BIOEKEY
5A30		UNLOCKN
5A31		RUNN
5A32		RCP00N
5A33		LOADRN
5A34		READSTN
5A35		RCP03N
5A36		LOADMN
5A37		READRN

5B01	*	SP05
5B02	*	GBCPFN
5B03	*	PREQN
5B04	*	CPBABS
5B05	*	TESTN
5B06		
5B07		
5B08		
5B09		
5B10	*	SP04
5B11	*	SP01
5B12	*	TMFN
5B13	*	BOFFN
5B14	*	PLOCR0
5B15	*	FPPABS
5B16		
5B17		OV
5B18		
5B19		
5B20	*	MFAULTN
5B21		
5B22	*	S00
5B23	*	S02
5B24	*	TMMN
5B25	*	TMMU
5B26		
5B27	*	0V
5B28	*	5V
5B29		CPMCN
5B30		IPL
5B31		START
5B32		CPINT
5B33		RUNFA
5B34		RCP01N
5B35		RCP02N
5B36		READMN
5B37		INSTN

Table 10.2 CPU B CONNECTOR 5

Notes: (device interfaces)

Signal Name	Pin No's (Line Connector P5)		CPU	Conn. P7
Ready for Receiving	25	CT 133	1A37	
Operational Signal	19			
Operational Signal	18			
Data Termin. Ready	20	CT 108-2	1A35	
Data Set Ready	6	CT 107	1A34	
Received Data	3	CT 104	1A32	
Transmitted Data	2	CT 103	1A31	
Protective Ground	1	CT 101		
Signal Ground	7	CT 102	1B31-1B37	

Table 10.3 PER 3100 INTERFACE

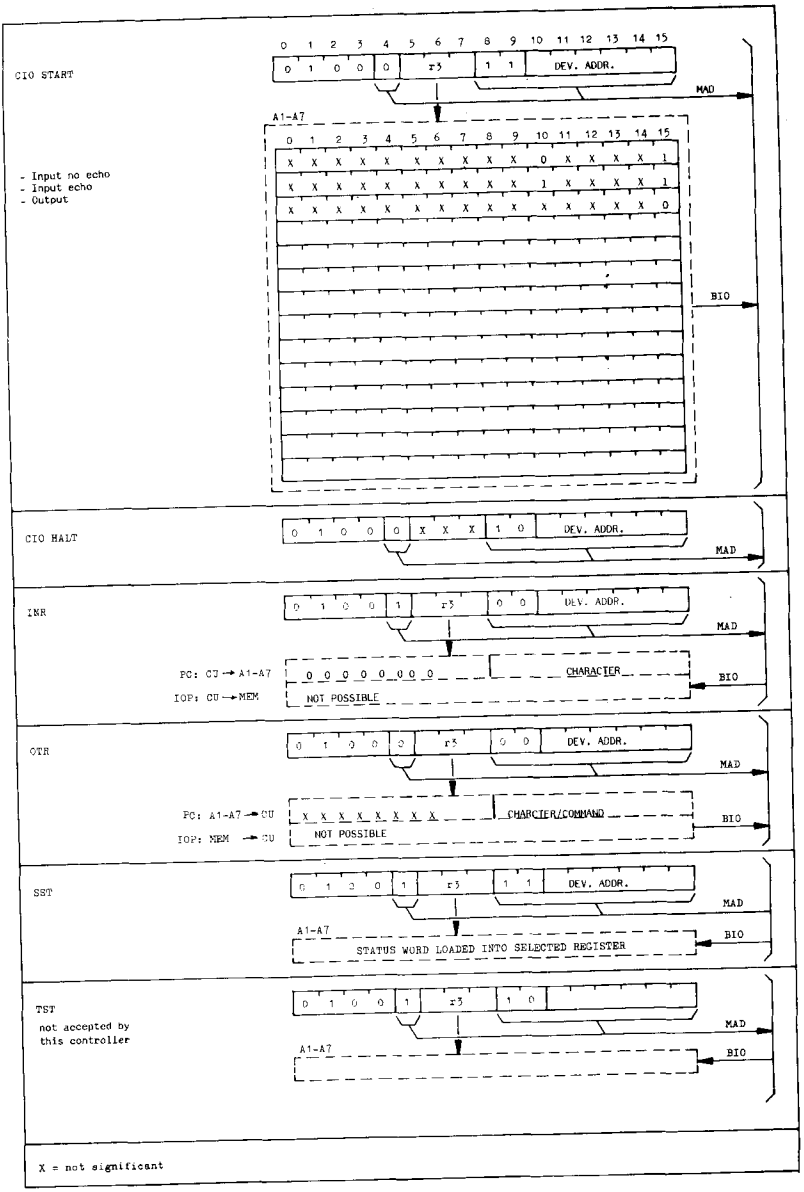
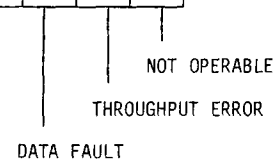


Figure 10.2 INSTRUCTION/COMMAND WORD FORMATS

10.4.1 STATUSWORD:

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0	0	0	0			



Not Operable

Bit 15 is set if the device is not connected or not operable.

Through put error

Bit 14 is set during input mode, if the interrupt is not yet answered by the CPU (INR) and the next input character arrives.

Parity error

Bit 13 is set when during input mode the received character has incorrect parity (not as is strapped).

10.5 SHORT DESCRIPTION TESTPROGRAMS

MICRODIAGNOSTICS

The P856M and the P857M contain an automatic testing feature in the form of a microprogrammed diagnostic built into the CPU logic. Sucessful running of the tests indicate that sufficient parts of the CPU function for loading of test programs.

The microdiagnostics for the P856M test the first 4k of memory and for the P857M the first 16k of memory. The prerequisite tool is the FULL CONTROL PANEL or the EXTENDED CONTROL PANEL, as the results of the tests are displayed on the data lamps.

About 100 words are reserved for the microdiagnostic program.
The test can only be performed when the jumper NORM/DIGNOS IS in the DIAGNOS position see figure 4.2-1 and an EFP or CFP is fitted (On 6810 UK and earlier models of PTS 6813 force pin 5B05 on backpanel 1C to ground).

TEST PROCEDURES

Before starting any test, except for steps A to D included in the Test 2. the user has to set a control unit address on data switches 2 to 7 included to check the dialogue through the Bus between the CPU and the control unit.

Test 1 Automatic Test
This is a fast check which automatically goes through a number of operations. If the tests have been satisfactory special codes are displayed on the data lamps.

- set data switch 0 to 0
- set a control unit address on data switches 2 thru 7
- press RUN button
- wait for display of code no 4
  code 4: data lamp 12 off
  all other lamps lit
  if this code is not displayed go to Test 2
- press LM button and wait for display of code 5
  code 5: all lamps lit
  If the code is not displayed go to Test 2.

Test 2 Step-by-step testing
This sequence may be used if Test 1 showed an erroneous display or if the user wishes to perform separate tests. In these tests the user verifies the operation of the control panel up to the memory.

A. Control Panel test
Each data key and the lamp above it are tested by setting the key in the 'up' position after which the lamp must be lit.
Press LR button to go to the next step.

B. L register test
This step includes the GP BUS and the L register in the test. The operator may use the switches in the same way as described under control panel. Press LR button to go to the M register test.

C. M register test
This step includes the M register (through the C selector and ALU) in the thest. The operator may use the switches in the same way as described under control panel. Press the LR button to go to the Q register test.

D. Q register test
This step includes the Q register in the test. The operator may use the switches in the same way as described under control panel.

From this moment on the operator may choose among three data path tests, an instruction simulation test or a memory test by setting on the data switches a hexadecimal number and a control unit address, followed by pressing the LR button.
If the relevant test is executed without errors the data lamps display a certain code.

It is possible to skip the visual tests A thru D. The user must then set switch 0 to 0, set a control unit address on switches 2 thru 7, and set switch 15 to 1. Next press the LR button 4 times. Then wait for display of code 1. Press LR button and wait for display of code 2. Press LR button and wait for display of code 3. Press LR (or RUN) button for display of code 4. Press LM (or LR) button for display of code 5.

Test 3 Chained test
In this mode the hardware is tested in a loop which may be stopped by operation of data switch 0.

- set data switch 0 to 1, a control unit address on switches 2 thru 7, and switch 15 to 1.
- press LR button 4 times. The microprogram starts looping.

To stop the loop:
- set switch 0 to 0.
  One of the 5 codes as listed above is displayed. If it is not code 5 press the LR button as many times until code 5 appears.

To restart the loop set switch 0 to 1.
To restart at the beginning of the test turn the key in the key switch to OFF and next to TEST. Set switch 0 to 1, set the control unit address, and set switch 15 to 1 and continue as described above.

	Hexa no on data switches	Test functions	Display on data lamps when no fault is found
data path test	/0001 + CU address	- shift left Q reg. - bus A selection - constant 'TWO' - QO test - A or B, A+B and B inverted ALU functions - ALU = 0	code 1 lamp 15 OFF all other lamps lit
data path test	/0002 + CU address	- shift right Q reg. - ALUZERO - A-B, A+B and crossed A ALU functions - constant 'TEN' - P reg. P - 2 function	code 2 lamp 14 OFF all other lamps lit
data path test	/0004 + CU address	- A operand shifted right - 4 x A function - reading and writing scratch pad	code 3 lamp 13 OFF all other lamps lit
instruction simulation	/0008 + CU address	DLA - K is loaded with DLA code - values loaded in A1 and A2 - branch to DLA micro program - return to microdiagnostic program RB K is loaded - RB microprogram next address generated by PLA	code 4 lamp 12 OFF all other lamps lit
memory test	/0010 + CU address	- bit 15 is set to 1 in all addresses of a 4k/16k block - the block is read and verified - the 1 is shifted left 1 position etc. next: - all words of a 4k/16k block receive their address values as contents these values are verified - tests the TMP-TPM dialogue	code 5 all lamps lit

SHORT DESCRIPTION TESTPROGRAM CPUTSC SEE CHAPTER 9.5

10.6 SHORT ROUTINES

SEE CHAPTER 9.6

11 MEMORY MANAGEMENT UNIT

LIST OF ILLUSTRATIONS

11.1 MMU-IDENTIFICATIONS

Type number : PTS 6828
Testprogram : MEMTSC (chapter14)

Power consumption : +5V 2.1A
used only for 6813

11.2 INSTALLATION DETAILS

- Straps external register address (standard /80)
- Straps interrupt level (page fault, standard /2F = 47_{10}

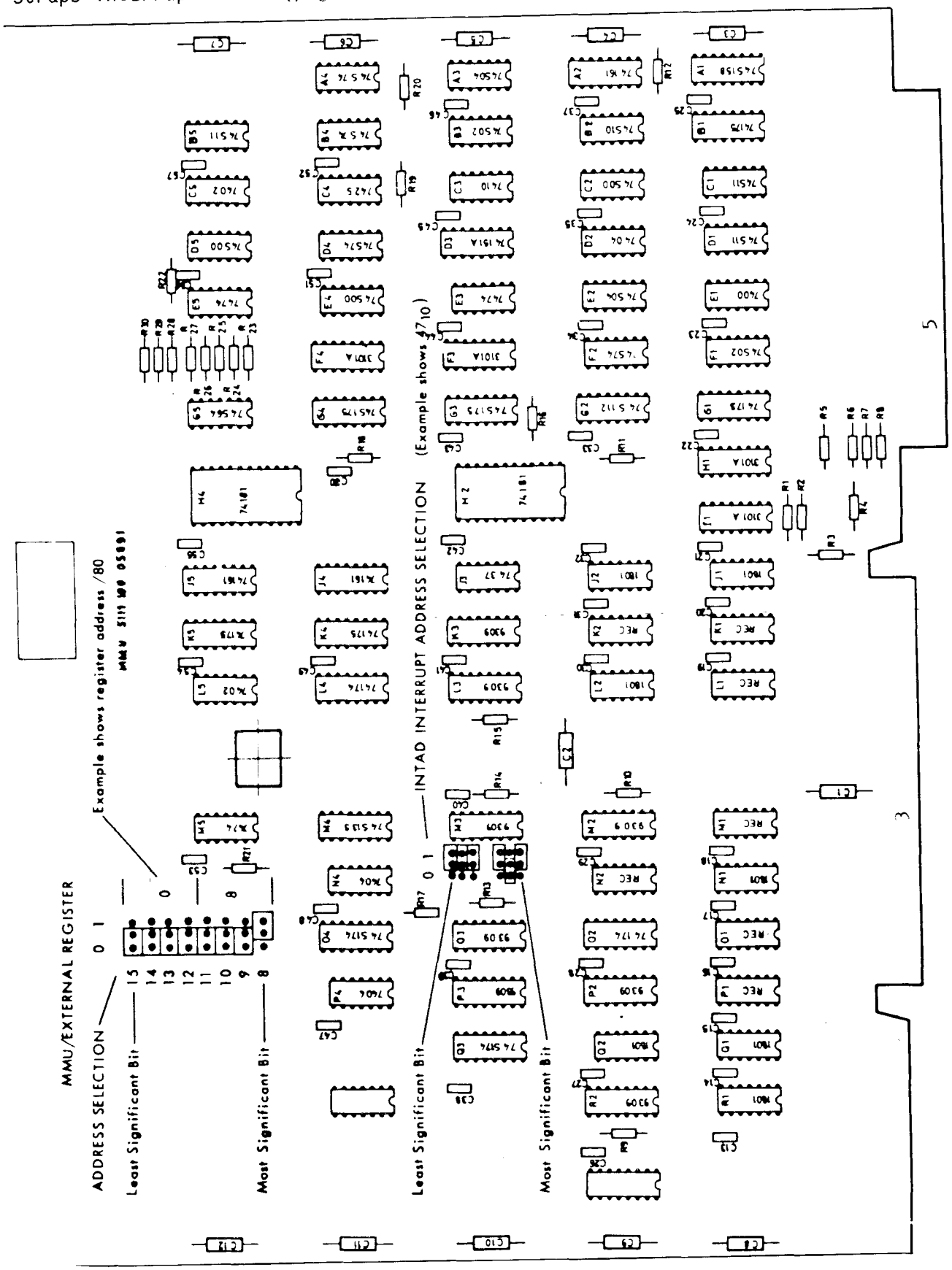


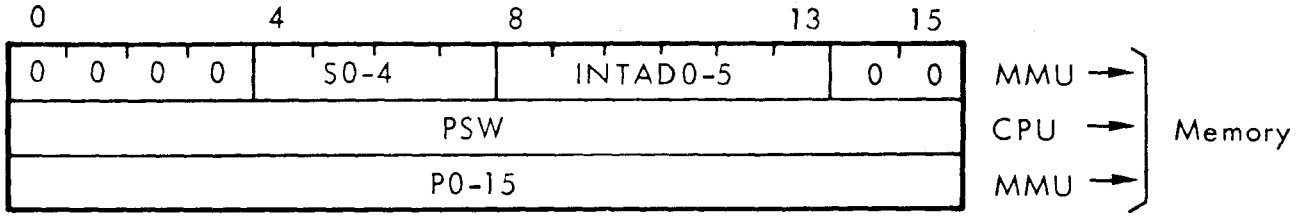
Figure 11.1 MMU CARD LAYOUT AND STRAPSETTING

11.3 INTERFACE CONNECTIONS

CPU-MMU Signals		MU/CPU CONN.
BSYCPUAN	CPU has Bus control. Validates Bus signals and controls all MMU operations.	5A12
BOMFN	Table Store control signal. Page-fault stack-loading control signal: 1st -- to read aborted instruction-counter value; 2nd -- to read logic page address which set page fault and the program level of the page-fault job, coded on the MMU card.	5A21
FU = 1 = 0	CPU in User Mode. Any memory violation sets page fault CPU in System Mode.	5A22
GFETCH	Fetch cycle is executed by CPU. Instruction counter value is loaded into MMU - P-Buf register.	5A13
OSCFLO	CPU clock signal, used by MMU for internal timing.	5A17
S00-03	Logical page address from CPU P-register.	5B22, 5A23
TMMN	Table Load control signal.	5B23, 5A24
TMMU	Translation control signal; for page-address translation, memory protection check, and memory activation by the MMU.	5B24 5B25
MMU - CPU Signals		
DONEMN	MMU reply during Table Load as each segment is loaded.	5A20
MFAULTN	Page fault is detected during translation.	5B20
MMUABS	Held at 0v (inactive) when MMU card is in place.	5A19
BUS - MMU Signals		
BIOON-15N	Data used during Table Load and WER operations.	
CLEARN	Clear signa for initializing system.	
TMEN	WER instruction timing for loading the software constant into the MMU BUFTIM register.	
TRMN	Memory reply: -- During Table Load and Table Store validates data. -- During translation releases memory activation.	
MAD04-15	Address line to: -- select the MMU during instruction, and -- store the CPU instruction-counter value during each Fetch instruction cycle.	
WRITE	CPU command for store cycles. Used during translation to test for page fault (read-only page and User Mode), and sets segment table Modified-Page bit (8) of accessed page (if no page fault).	

BIOON-15N	Data used during Table Store or Page-Fault stack loading operations.
MAD128,64 0-3	Memory address lines for physical page addresses from the segment table.
TMRN	Activates memory during page address translation, if there is no page fault.
TRMN	External register reply to CPU when software constant is loaded during WER instruction.

Stack after Page Fault Interrupt



S = page number
P = program counter or aborted instruction

Instructions : see P800M Programmer's Guide 1,2 and 3
Volume II Instruction set.

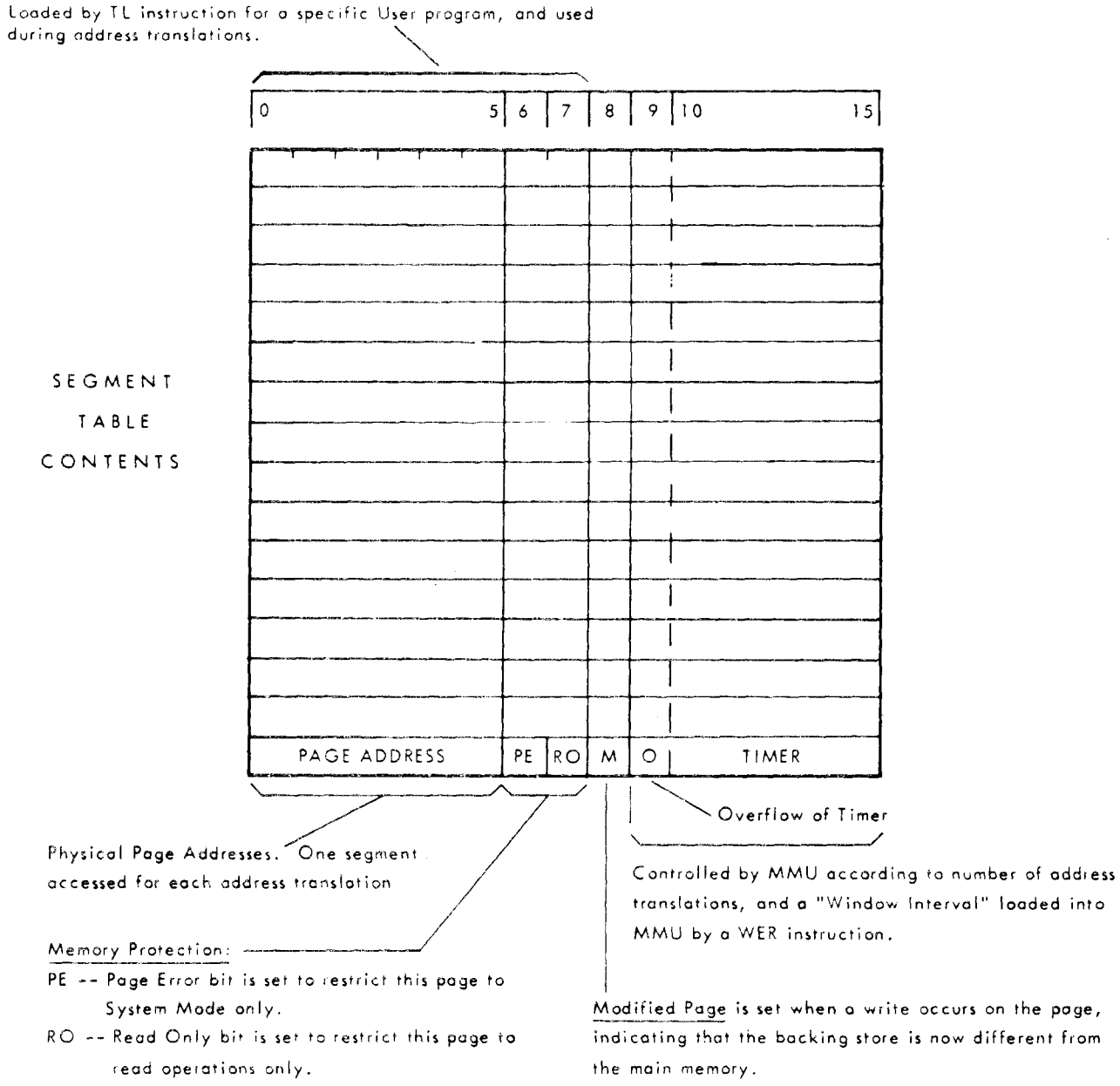


Figure 11.2 MMU SEGMENT TABLE

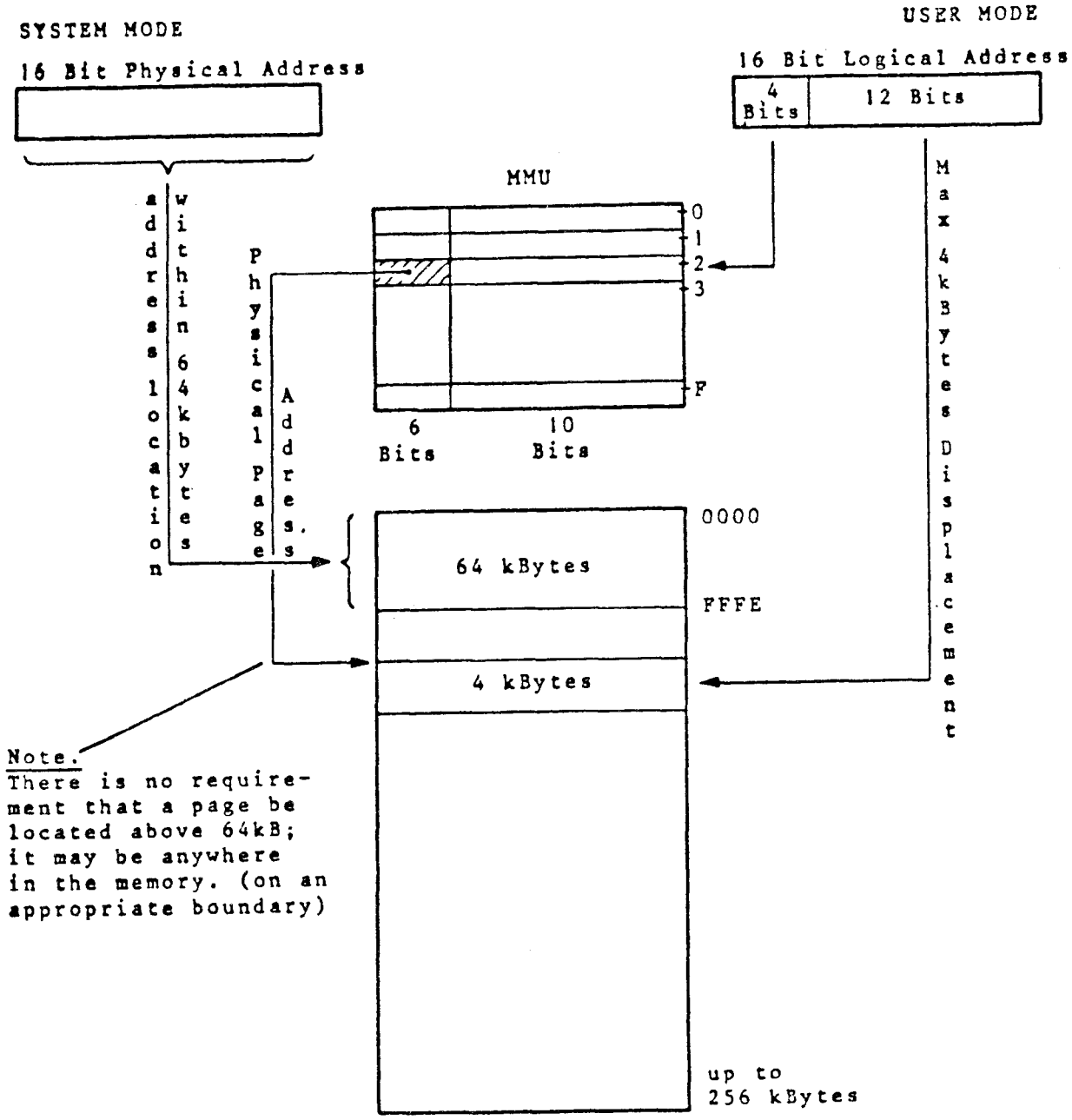


Figure 11.3 MMU MEMORY ADDRESSING

11.5 SHORT DESCRIPTION TESTPROGRAM

See MemTSC (rel.2) chapter 11

```
    DATE  04-01-80        IDENT    MMUA

                          IDENT    MMUA
                    *     THIS PROGRAM CHECKS THE TIMER OF THE MMU SEGMENT TABLE
                    *SYSTEM PROGRAM
                          AORG     /100
 0100  87A0       START   LDKL     A15,/400          LOAD STACKPOINTER
 0102  0400
 0104  8120              LDKL     A1,/140           PROGR INTERRUPT
 0106  0140
 0108  8141              ST       A1,2
 010A  0002
 010C  8120              LDKL     A1,/180           PAGE FAULT INT.
 010E  0180
 0110  8141              ST       A1,/5E
 0112  005E
 0114  0100              LDK      A1,0              SET TIMING CONSTANT 0,-/FF
 0116  7180              WER      A1,/80
 0118  0200              LDK      A2,0
 011A  8120              LDKL     A1,/2000          FOR SEGMENT TABLE WITH /2000
 011C  2000
 011E  8149              ST       A1,/200,A2        EVERY PAGE!
 0120  0200
 0122  1202              ADK      A2,2              16 MEM. WORDS/SECTOR TABLE
 0124  EA20              CWK      A2,/20
 0126  0020
 0128  5A0C              RB(2)    *-10
 012A  8840              TL       /200              LOAD SEGMENT TABLE IN MMU
 012C  0200
 012E  2801              SMD                        GO TO USER MODE
                    *USER PROGRAM                   NEXT INSTR: /130 LOG =/8130 PHYSICAL
                          AORG     /8130
 8130  0200              LDK      A2,0              NO OP
 8132  0355              LDK      A3,/55
 8134  0400              LDK      A4,0
 8136  8351              ST       A3,/3000,A4       /3000 LOG =/8000 PHYS.
 8138  3000
 813A  1402              ADK      A4,2
 813C  EC20              CWK      A4,/100
 813E  0100
 8140  5A0C              RB(2)    *-10
 8142  2804              LKM                        CAUSES PROGRAM INTERRUPT
 8144  0001              DATA     1
                    * INTERRUPT ROUTINE FOR PROGRAM INTERRUPT
                          AORG     /140
 0140  20FB              RIT      /1D               RESET INTERRUPT
 0142  8841              TS       /300              STORE MMU SEGMENT TABLE FROM /300 ON
 0144  0300
 0146  207F              HLT
                    *RESTART FROM ADDRESS /100 AFTER MASTER CLEAR
                    * INTERRUPT ROUTINE FOR PAGE FAULT
                          AORG     /180
 0180  8841              TS       /300              STORE SEGM TABLE MMU FROM /300 ON
 0182  0300
 0184  207F              HLT                        MIND PLR=/2F
                    *RESTART FROM ADDRESS /100 AFTER MASTER CLEAR
                          END      START
```

CHECK ON TIMER: preset software counter on /100 — Modified page *

info segment table 2000, 2039, 2039, 2081, 2038 2038
from add. /300

0	1	2	3	4	15
.	.	.	.	.	.
.	.	.	.	.	.

CHECK TIME ON OVERFLOW : change address /813E info /100 into /120

info segm. table 2000, 2040, 2040, 2081, 203F.....203F
from add. /300 — overflow! — counter top- - count.

CHECK ON READ ONLY : change address /11C into /2000 into /2100.
interrupt → page fault (mem prot. for USER program).

CHECK ON PE BIT : change address /11C info /2000 into /2200.
interrupt → page fault (mem. prot. for SYSTEM program)
- also for read in protected page -

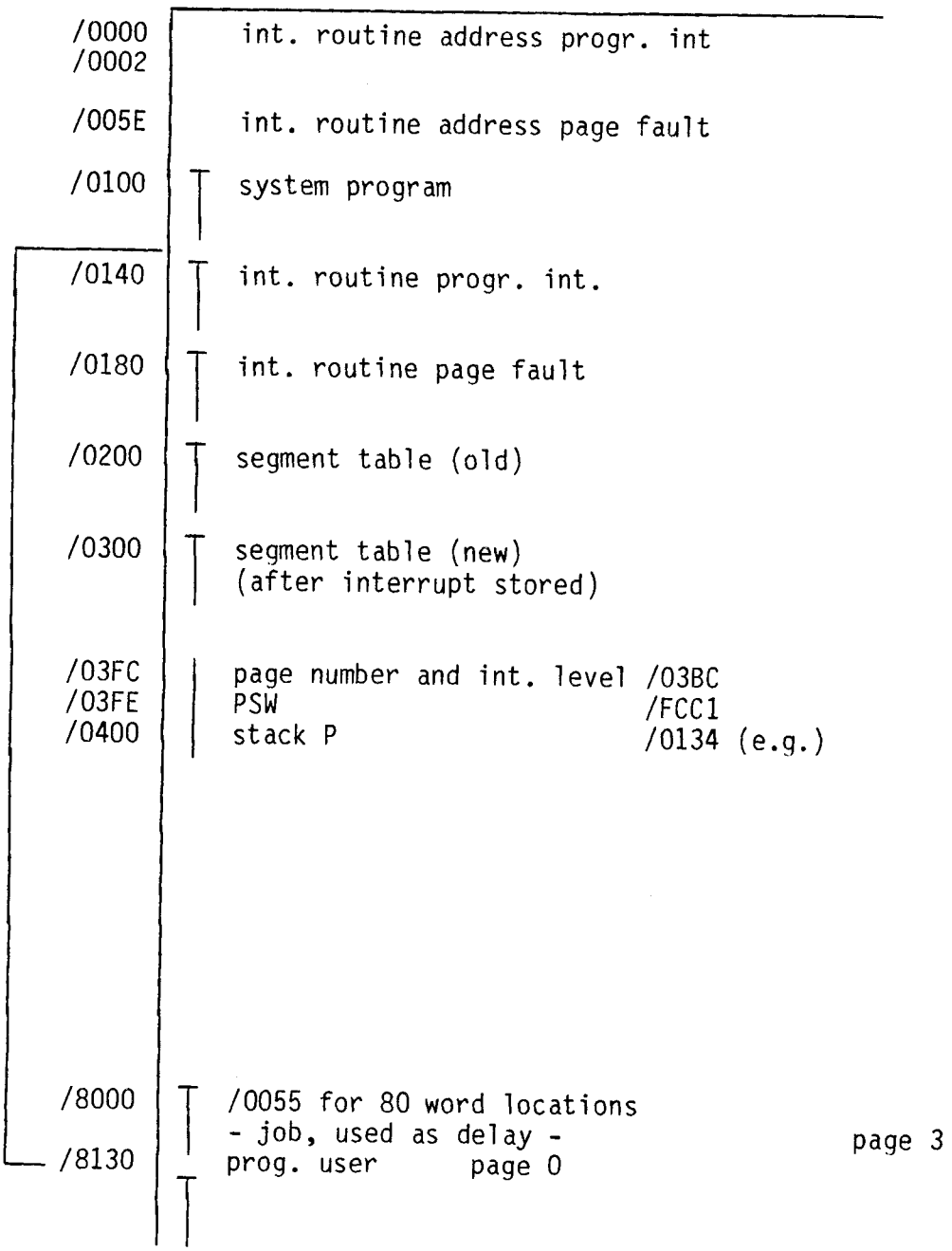


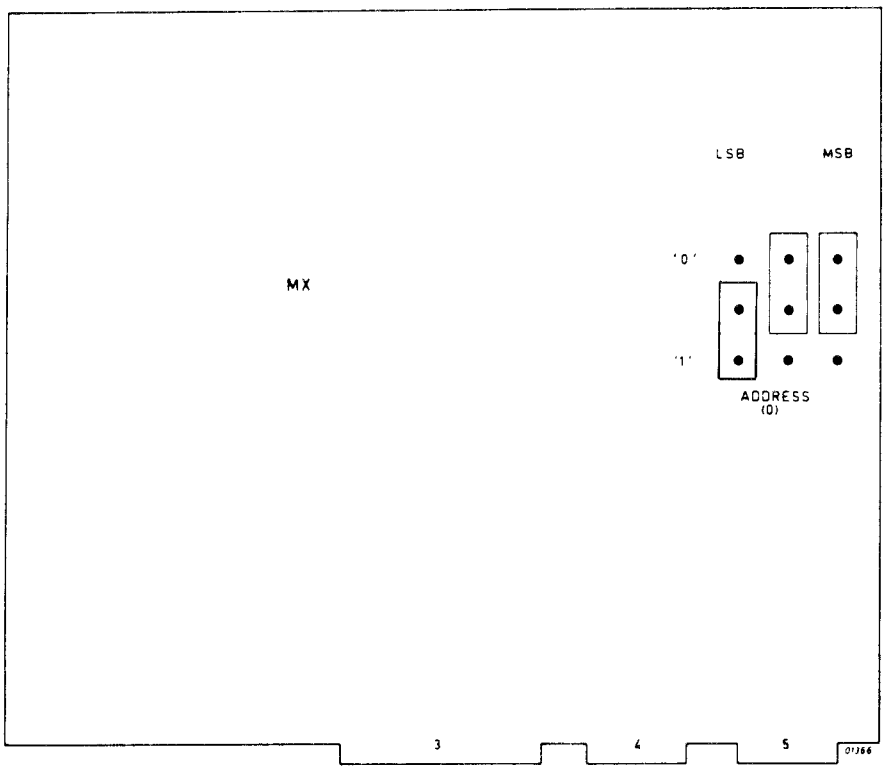
Figure 10.3 MEMORY USE OF MMUA

LIST OF ILLUSTRATIONS

LIST OF TABLES

12.1 IOP-IDENTIFICATIONS

Older version	:	MX only for 6810
	:	IOP PTS6827, P843-020
Power consumption	:	+5 Volt, 4 Amp.



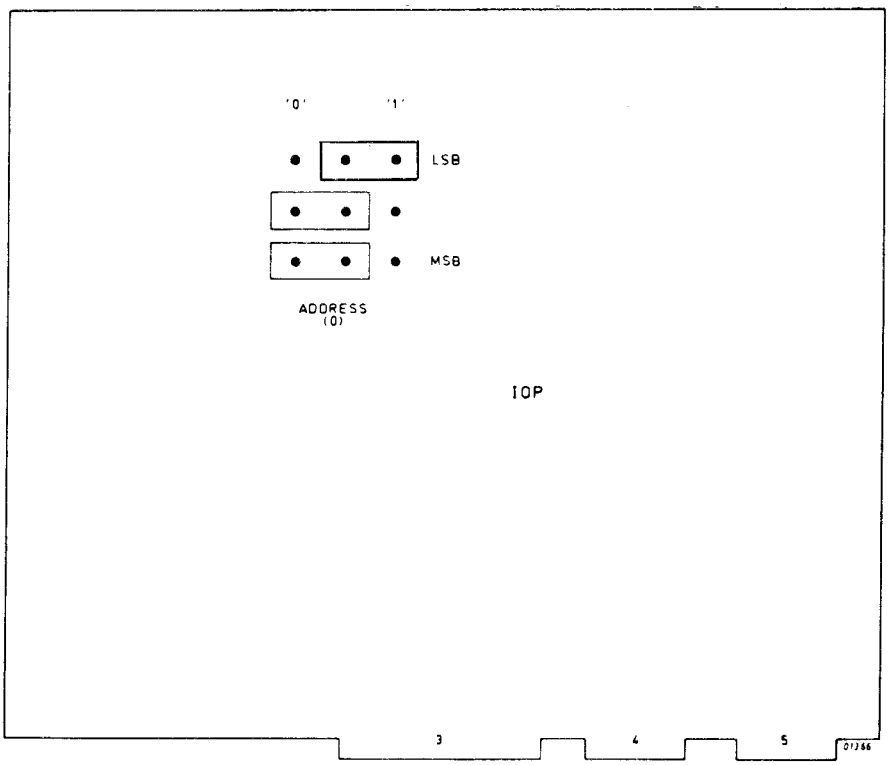


Figure 12.1 IOP/MX ADDRESS STRAPS

12.3 INTERFACE CONNECTIONS

Break Request Connections on I/O Processor Board

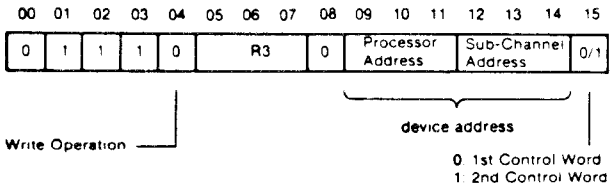
Signal	Pin No.		Signal	Pin No.
	5A01			5B01
	5A02			5B02
	5A03			5B03
	5A04			5B04
	5A05			5B05
BREX07N	5A06		0V	5B06
BREX06N	5A07		0V	5B07
BREX05N	5A08		0V	5B08
BREX04N	5A09		0V	5B09
BREX03N	5A10		0V	5B10
BREX02N	5A11		0V	5B11
BREX01N	5A12		0V	5B12
BREX00N	5A13		0V	5B13

Signal	Pin No.		Signal	Pin No.
BREX07N	4A06		BR07N	4B06
BREX06N	4A07		BR06N	4B07
BREX05N	4A08		BR05N	4B08
BREX04N	4A09		BR04N	4B09
BREX03N	4A10		BR03N	4B10
BREX02N	4A11		BR02N	4B11
BREX01N	4A12		BR01N	4B12
BREX00N	4A13		BR00N	4B13

Table 12.1 BREAK REQUEST CONNECTIONS TO CONNECTOR 4 AND 5

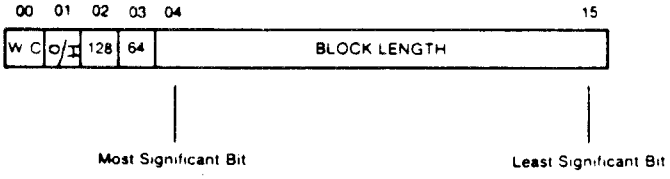
Initialization Operation

This operation is applied before commencing data transfer and the first part is controlled by the use of two write external register instructions WER to transfer two control words to the two working registers of the I/O processor subchannel. The instruction format is as shown below:



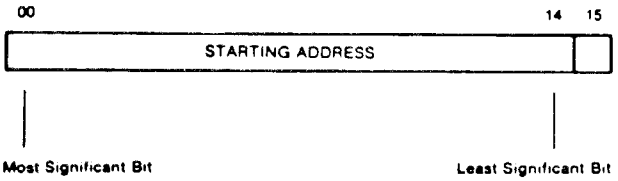
This instruction transfers the contents of the R3 field, previously loaded with a control word, to the external working register of the I/O processor specified by the device address bits 09 to 14.

The format of the first control word loaded is shown below:



Bit 00 = 1	Exchange is in word mode.
= 0	Exchange is in character mode.
Bit 01 = 1	Exchange is from memory to control unit.
= 0	Exchange is from control unit to memory.
Bits 04 to 15	specify the number of characters/words to be transferred.
Bits 02, 03	are positioned to become the two most significant bits of the second control word. (only for P-857)

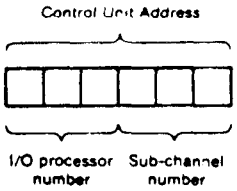
The format of the second control word loaded is as follows:



Bits 00 to 15	specify the starting address in memory.	
Bit 15 = 1	Right character is addressed	If transfer is
= 0	Left character is addressed	in character mode.

12.5 RELATIONSHIP BETWEEN BREAK SIGNAL AND CONTROL UNIT ADDRESS

An I/Q processor is coded with a 3-bit number which may range from 0 to 7 (coded by straps on the I/O processor) and each of the 8 subchannels associated with an I/O processor is also coded with a 3-bit number from 0 to 7. The combined 6-bit number gives the address of the peripheral control unit as shown below:



This address is used by the WER instruction to load the 2 control words into the working register of the I/O processor.

The 8 incoming break request signals BR00 to BR07 to each I/O processor correspond to each subchannel in the I/O processor as follows:

BR00N corresponds to subchannel 0
BR07N corresponds to subchannel 7

BR00N has the highest priority and BR07N the lowest.

13 CPU P6814/P6824 (CP7RA)

LIST OF ILLUSTRATIONS

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13.1 PTS6814/24 CPU IDENTIFICATIONS

Type number : CPU board CP7R (CP7RA) with integrated serial CU (V24).

Test Programs : CPU - TP57RE Mem TSC rel.4 see chapter 14
MIOP
Integrated CU
PER3100 - PERTST

Devices
PER3100 - PTS 6862-003

Power Consumption :

- +5VL 9A
- +12VL 50mA
- -12VL 50mA

Note: 12NC code on the sticker on the board.

CP7R : 5111 199 6758X
CP7RA : 5111 199 6201X (5322 216 21084)
CP7RA : 5131 194 44400 (PTS)

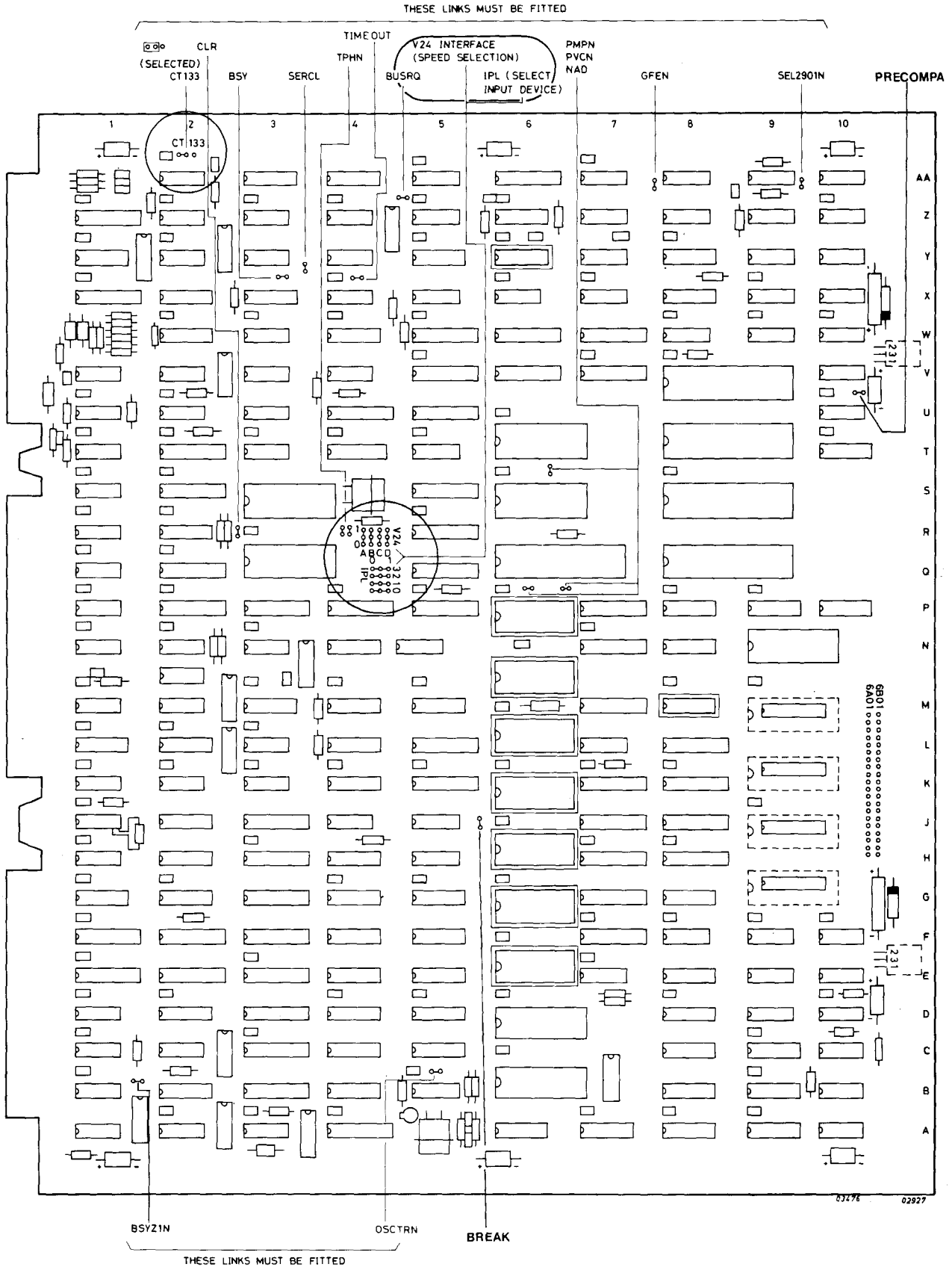
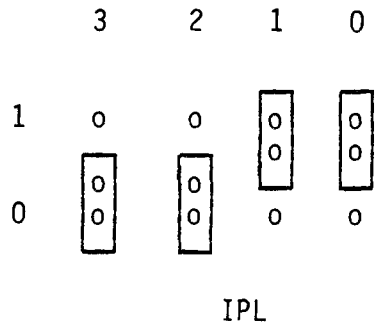


Figure 13.1 (CP7RA) LINK POSITIONS

3	2	1	0	WORD	IPL WORD	MEMORY ADDRESS HEX
OPS3N	OPS2N	OPS1N	OPSON			
0	0	0	0	0	255	1FE
0	0	0	1	1	254	1FC
0	0	1	0	2	253	1FA
0	0	1	1	3	252	1F8
0	1	0	0	4	251	1F6
0	1	0	1	5	250	1F4
0	1	1	0	6	249	1F2
0	1	1	1	7	248	1F0
1	0	0	0	8	247	1EE
1	0	0	1	9	246	1EC
1	0	1	0	10	245	1EA
1	0	1	1	11	244	1E8
1	1	0	0	12	243	1E6
1	1	0	1	13	242	1E4
1	1	1	0	14	241	1E2
1	1	1	1	15	240	1E0

Table 13.1 SELECT IPL INPUT DEVICE

The following diagram shows the identification that is silkscreened on the card and an example of word selection:



IPL

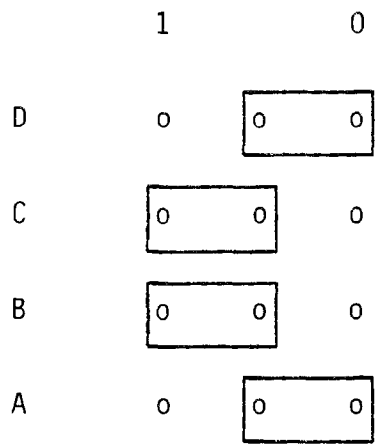
Example: word 3, memory address 1F8. The content of this word is loaded in register A15 during IPL.

In P6814/24 These Straps are set to '0'

Transmit/Receive U Link Positions				Baud Rate
D	C	B	A	
0	0	0	0	50
0	0	0	1	75
0	0	1	0	110
0	0	1	1	134.5
0	1	0	0	150
0	1	0	1	300
0	1	1	0	600
0	1	1	1	1,200
1	0	0	0	1,800
1	0	0	1	2,000
1	0	1	0	2,400
1	0	1	1	3,600
1	1	0	0	4,800
1	1	0	1	7,200
1	1	1	0	9,600
1	1	1	1	19,200

Table 13.2 V24 INTERFACE SPEED SELECTION

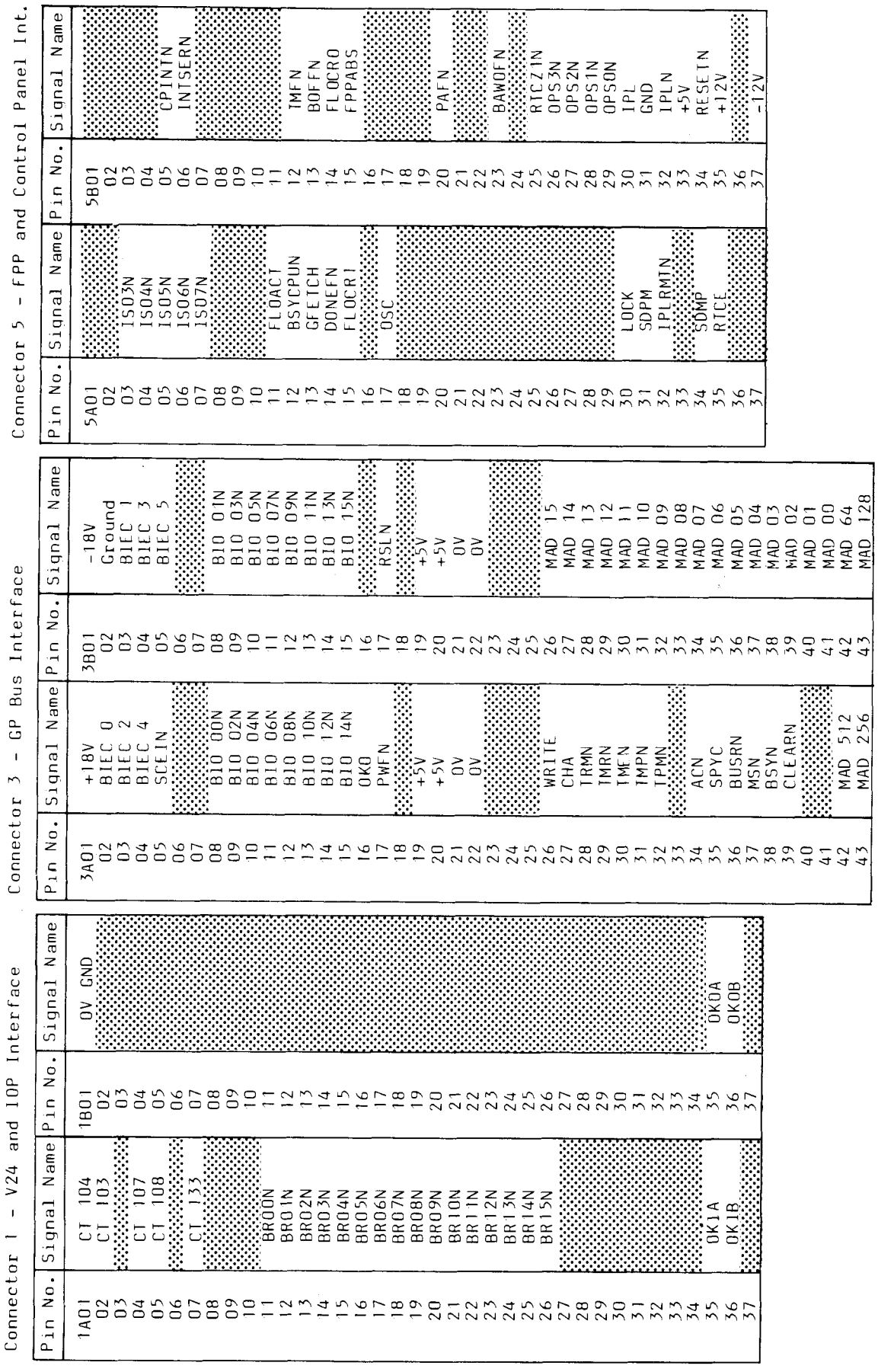
The following diagram shows the identification that is silkscreened on the card, and an example of speed selection:



Selected speed is 600 bauds (PER 3100)

Note: The maximum speed authorised for the PER 3100 is 600 bauds.

13.3 INTERFACE CONNECTIONS see also chapter 6



Connector 1 - V24 and IOP Interface

Pin No.	Signal Name	Pin No.	Signal Name
1A01	CT 104	1B01	0V GND
02	CT 103	02	
03		03	
04	CT 107	04	
05	CT 108	05	
06		06	
07	CT 133	07	
08		08	
09		09	
10		10	
11	BR00N	11	
12	BR01N	12	
13	BR02N	13	
14	BR03N	14	
15	BR04N	15	
16	BR05N	16	
17	BR06N	17	
18	BR07N	18	
19	BR08N	19	
20	BR09N	20	
21	BR10N	21	
22	BR11N	22	
23	BR12N	23	
24	BR13N	24	
25	BR14N	25	
26	BR15N	26	
27		27	
28		28	
29		29	
30		30	
31		31	
32		32	
33		33	
34		34	
35	OK1A	35	OK0A
36	OK1B	36	OK0B
37		37	

Connector 3 - GP Bus Interface

Pin No.	Signal Name	Pin No.	Signal Name
3A01	+18V	3B01	-18V
02	BIEC 0	02	Ground
03	BIEC 2	03	BIEC 1
04	BIEC 4	04	BIEC 3
05	SCEIN	05	BIEC 5
06		06	
07		07	
08	BIO 00N	08	BIO 01N
09	BIO 02N	09	BIO 03N
10	BIO 04N	10	BIO 05N
11	BIO 06N	11	BIO 07N
12	BIO 08N	12	BIO 09N
13	BIO 10N	13	BIO 11N
14	BIO 12N	14	BIO 13N
15	BIO 14N	15	BIO 15N
16	OKO	16	RSLN
17	PWFN	17	
18		18	
19	+5V	19	+5V
20	+5V	20	+5V
21	0V	21	0V
22	0V	22	0V
23		23	
24		24	
25		25	
26	WRITE	26	MAD 15
27	CHA	27	MAD 14
28	TRMN	28	MAD 13
29	TMRN	29	MAD 12
30	TMFN	30	MAD 11
31	TMPN	31	MAD 10
32	TPMN	32	MAD 09
33		33	MAD 08
34	ACN	34	MAD 07
35	SPYC	35	MAD 06
36	BUSRN	36	MAD 05
37	MSN	37	MAD 04
38	BSYN	38	MAD 03
39	CLEARN	39	MAD 02
40		40	MAD 01
41		41	MAD 00
42	MAD 512	42	MAD 64
43	MAD 256	43	MAD 128

Connector 5 - FPP and Control Panel Int.

Pin No.	Signal Name	Pin No.	Signal Name
5A01		5B01	
02		02	
03	ISO3N	03	
04	ISO4N	04	
05	ISO5N	05	CPINTN
06	ISO6N	06	INTSERN
07	ISO7N	07	
08		08	
09		09	
10	FLOACT	10	
11		11	IMFN
12	BSYCPUN	12	
13	GFETCH	13	BOFFN
14	DONEFN	14	FLOCRO
15	FLOCRI	15	FPPABS
16		16	
17	OSC	17	
18		18	
19		19	
20		20	PAFN
21		21	
22		22	
23		23	BAWOFN
24		24	
25		25	RICZIN
26		26	OPS3N
27		27	OPS2N
28		28	OPS1N
29		29	OPS0N
30	LOCK	30	IPL
31	SDPM	31	GND
32	IPLRMIN	32	IPLN
33		33	+5V
34	SDMP	34	RESETN
35	RTCE	35	+12V
36		36	
37		37	-12V

Figure 13.2 CP7RA CONNECTORS (REAR VIEW)

Signal Name	Source (Pin No)	Destination (Pin No)	Description
ACN	GPB C.U.s	CP7R/G (3A34)	Active low to indicate to the CPU that the C.U. accepts the request to carry out a designated function.
BROON-15N	IOP CUs	CP7R/E (1A11-26)	Break Request Lines active low, BR00 has the highest priority.
BAWOFN	Power Supply	CP7R/J (5B23)	When semi-conductor memories are employed, this signal (Battery Was Off) indicates that data has been lost.
BIEC 0-5	GPB C.U.s	CP7R/E (3A02-04 3B03-05)	Binary Coded Interrupts
BIO 00-15N	CP7R/D (3A08-15, 3B08-15)		Bidirectional data lines between CP7RA and all GPB Master and Slave Units.
BSYN	GPB Masters	CP7R/K (3A38)	A bidirectional line between all GPB Masters; when a Master has been selected this line is low to indicate Busy to other Masters.
BUSRN	GPB Masters	CP7R/K (3A36)	A bidirectional line between all GPB Masters; any Master may force this line low to request the Bus.
BOFFN	CP7R/G (5B13)	FPP	Active low to inhibit BIO and enable FPP to set BIO instead.
BSYCPUN	CP7R/K (5A12)	FPP	Active low indicates that the CPU is Busy with the Bus.
CHA	CP7R/I (3A27)	GP Bus	When received by the Memory CHA = 1 for Character Operation and CHA = 0 for Word Operation. For Control Units and External Registers CHA = 0.
CLEARN	CP7R/D (3A39)	GPB Masters and Slaves	General reset of all devices, active low for a minimum time of 90´S.
CPINTN	CP7R/E (5B05)	CP7R	Control Panel Interrupt, to be linked at the Back Panel to the Interrupt (IS) Lines.
CT103	CP7R/D (1A02)	D.T.E.	Serial data
CT104	D.T.E.	CP7R/D (1A01)	Serial data
CT107	D.T.E.	CP7R/D (1A04)	Modem ready
CT108	CP7R/D (1A05)	D.T.E	Connect Modem to Line

Table 13.2a INTERFACE SIGNALS (CONNECTORS 1,3,5)

Signal Name	Source (Pin No)	Destination (Pin No)	Description
CT133	D.T.E	CP7R/D (1A07)	Ready for Receiving
DONEFN	FPP	CP7R/A (5A14)	Indicates to the CPU that the FPP has finished the transfer.
FLOCRO-1	FPP	CP7R/G (5B14,5A15)	From the FPP Condition Register to the CPU Condition Register.
FLOACT	CP7R/G (5A11)	FPP	Sent at the beginning of an FPP instruc tion to time the actual processing and to synchronise the end of the operation.
FPPABS	FPP	CP7R/J (5B15)	When the FPP Card is inserted this signal is forced low.
GFETCH	CP7R/C (5A13)	CP7R/N	Indicates an Instruction Fetch cycle and restarts the CPU sequensor in some cases.
IPLRMTN	Remote Terminal	CP7R/J) (5A32))	These 3 signals are all associated with the same function, i.e. to indicate,to
IPL		CP7R/J)- (5B30))	the CPU External Test Logic that a code is to be received on Lines OPS OON-03N
IPLN		CP7R/J) (5B32))	
ISO3N-07N	CUs	CP7R/E (5A03-07)	Interrupt Request Lines
INTSERN	CP7R/D (5B06)	CP7R/	An Interrupt from the Operator Interface (Serial Interface) when either a Write, Read, Wait or Echo condition is active. This signal is linked on the Back Panel to the Interrupt IS Line
LOCK	Control Panel	CP7R/D (5A30)	LOCK = 0 means Control Panel functions are enabled; LOCK = 1 means Control Panel functions are inhibited.
MAD 00-15	CP7R/I (3B26-41)	GPB Slaves	Used with MAD 64-512 to represent a Memory Address in true value. MAD 00 is the most significant bit.
MAD 64-512	CP7R/I (3B42-43, 3A42-43)	GPB MENS	See above.
MSN	GPB Masters	CP7R/K (3A37)	A bidirectional line between all GPB Masters; originating from the Master selected to indicate to all other Master that a Master is selected.

Table 13.2a INTERFACE SIGNALS (CONNECTORS 1,3, 5)-CONT'D

Signal Name	Source (Pin No)	Destination (Pin No)	Description
OKO	CP7R/L (3A16)	Next Master	The Bus Controller sends OKO to search for the highest priority of the Master requesting the Bus.
OKIO/OO	CP7R/L (1A35	CP7R/L (1B35)	Derived from the OKO signal OKIO is the input to IOPO, and OKOO is the output of IOPO.
OKI1/O1	CP7R/L (1A36)	CP7R/L (1B36)	Derived from the OKO signal OK11 is the input to IOP1 and OKO1 is the output of of IOP1.
OSC	CP7R/A (5A17)	FPP	Derived from the CPU basic clock frequency of 45nSec.
OPSON-3N	Remote Device	CP7R/J (5B26-29)	Four address lines, the code of which is used to address the last sixteen words of the Bootstrap.
PAFN	CP7R/G (5B20)		Page Fault
PWFN	Power Supply	CP7R/K (3A17)	Indicates to the CPU that a Power Failure has occurred. The CPU only enters the Power Fail Routine if the failure is for 10mS or more. If less than 10mS the Power Failure is ignored.
RESETN	CP7R/D (5B34)	Control Panel	Derived from the Power Supply signal RSLN signal RESETN is the Master Reset for the Control Panel
RSLN	Power Supply	CP7R/A (3B17)	To ensure an orderly start procedure this signal stays low until power has stabilised.
RTCE		CP7R/G (5A35)	Real Time Clock Enable
SDMP	CP7R/D (5A34)	Control Panel	Serial Data Master to Panel
SDPM	Control Panel	CP7R/D (5A31)	Serial Data Panel to Master
SPYC	CP7R/K (3A35)	Masters	Scan Priority Chain (Low active)
TMEN	CP7R/K (3A30)	Ext. Reg.	Timing Master to External Register, active low to validate the addresses and data; this signal also resets the Timeout Circuit.
TMFN	CP7R/G (5B12)	FPP	Timing Master to Floating Point Processor, active low to validate the addresses and data.

Table 13.2a INTERFACE SIGNALS (CONNECTORS 1,3, 5)-CONT'D

Signal Name	Source (Pin No)	Destination (Pin No)	Description
TMRN	CP7R/K	Memory	Timing Master to Memory, active low to validate addresses and data. This signal also resets the Timeout Circuit.
TMPN	CP7R/K (3A31)	C.U.	Timing Master to Peripheral (C.U.) active low to validate addresses and data. This signal also resets Timeout Circuit.
TPMN	CP7R/K (3A32)	Master	Timing Peripheral to Master, active low to validate data. Reply to TMPN.
TRMN	CP7R/K (3A28)	Master	Timing Memory to Master, active low to validate data. Reply to TMRN or TMEN.
SCEIN	CP7R/E (3A05)		Scan External Interrupts
RTCZ1N	Power Supply	CP7R/G (5B25)	
WRITE	CP7R/I (3A26)	GP Bus	Indicates to the GPB Slaves the direction of Bus Transfer; WRITE = 1 means Transfer Master to Slave, WRITE = 0 means Transfer Slave to Master.

Table 13.2a INTERFACE SIGNALS (CONNECTORS 1,3, 5)-CONT'D

Pin	Sig. Name	Description
6B01	ROMAD08	)
02	07	)
03	06	)
04	05	) Micro-program ROM Address Lines, note
05	04	)- that only 9 of the 11 lines are available
06	03	) here, for ROMAD 09 and 10 see pins 6A17 and 6A18.
07	02	) (CP7R/B)
08	01	)
09	ROMAD00	)
10	BSYIOP	(CP7R/L)
11	BSYCPUB	Indicates CPU busy with Bus (CP7R/K)
12	TMP	Indicates Transfer Master to Peripheral (CP7R/K)
13	TMR	Indicates Transfer Master to Memory (CP7R/K)
14	OSCENB	Enables the internal clock (CP7R/A)
15		)- Not used
16		)
17	RSLFN	Simulates RSLN from the Power Supply (CP7R/A)
18	APA	Enables an external test of the CPU Sequencer signal
19	5V	AP (CP7R/A)
20	5V	
6A01	D00	)
02	01	)
03	02	)
04	03	)
05	04	)
06	05	)
07	06	)
08	07	)
09	08	)- 3 - state internal CPU Bus (CP7R/D)
10	19	)
11	10	)
12	11	)
13	12	)
14	13	)
15	14	)
16	D15	)
17	ROMAD10	)
18	ROMAD09	)- See pin nos 6B01-6B09
19	0V	)
20	0V	

Table 13.3 TEST CONNECTOR NO. 6 (DEVELOPMENT ONLY)

13.4 V24 CONTROL UNIT

13.4.1 GENERAL

An USART 8251 is used as interface between Console Typewriter and CU.
The type 8251 is also used for the interface Control Panel - CPU.

USART : Universal Synchronous Asynchronous Receiver Transmitter.

CTW : Selectable baudrate : 50 - 19.200 baud.
Panel : Fixed baudrate : 4800 baud.

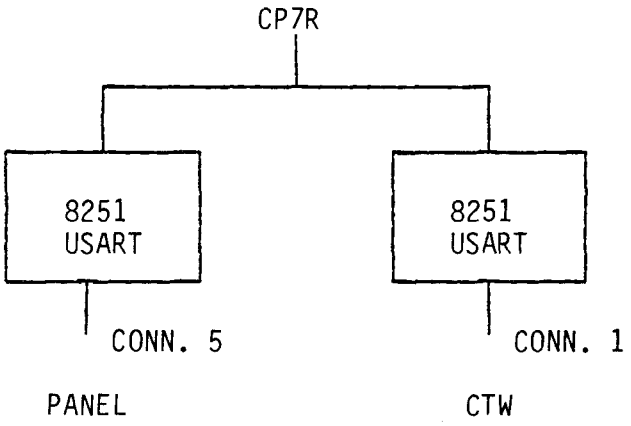


Figure 13.3 V24 AND PANEL INTERFACE

STRAPS : 5 straps total (baudrate and CT133)
CU Address : /10 (fixed)
Int. level : 7
HSI : see page 13-13

13.4.2 FACILITIES

I/O DEVICE INTERFACE

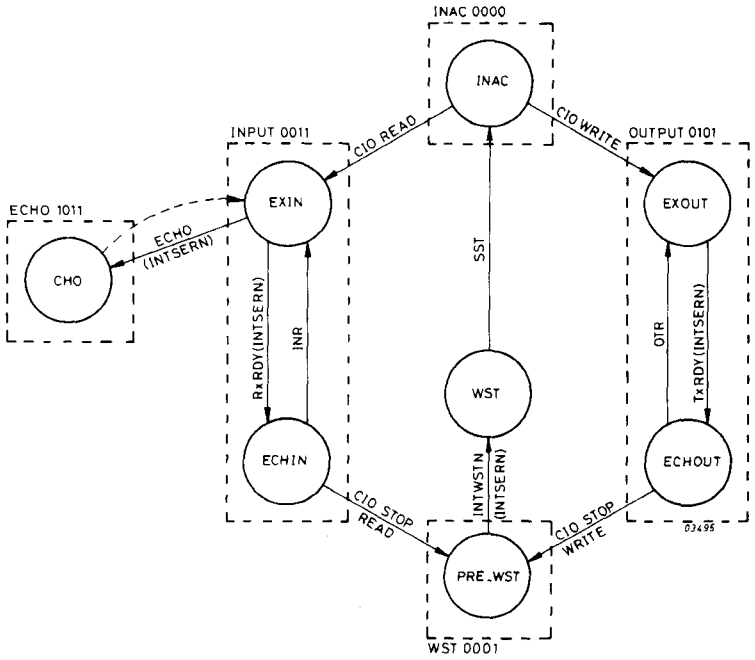
* Connection to an I/O device having V24/28 interface according CCITT.
* Programmed channel with or without using interrupt handling.
* The CU is working in half duplex mode. However, the line to an I/O device may be a so called 4 wire connection. 4 Wire line connection allows echo mode (software selection).
* The V24 line 'Ready For Receiving' CT133/CT119 may control the throughput during the output mode. (Used by PER3100). To be selected by a strap.
* Used V24 lines: CT101, 102, 103, 104, 107, 108, 109, 133. CT 107/108 must be controlled by CU/CTW.
* Break detection in order to set control panel interrupt.
* Transfer rate 50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 19.200 bits/sec.
* Character of line composed of:
  - 1 Start bit, rec. 1 or 2 Stop bits, trx. 2 Stop bits (normally).
  - 8 Data bits
  - Software selectable (parity bit) (number of stop bits).
  - Device address /10 (non selectable)

PANEL INTERFACE

* A-synchronous interface according CCITT V28 for serial transmission and reception.
* Transfer rate 4800 bits/sec.
* Character on line composed of:
  - 1 Start bit, (at least) 2 Stop bits.
  - 8 Data bits
  - (no parity)

Note: For interface connections see chapter 4 - figure 36, 37.

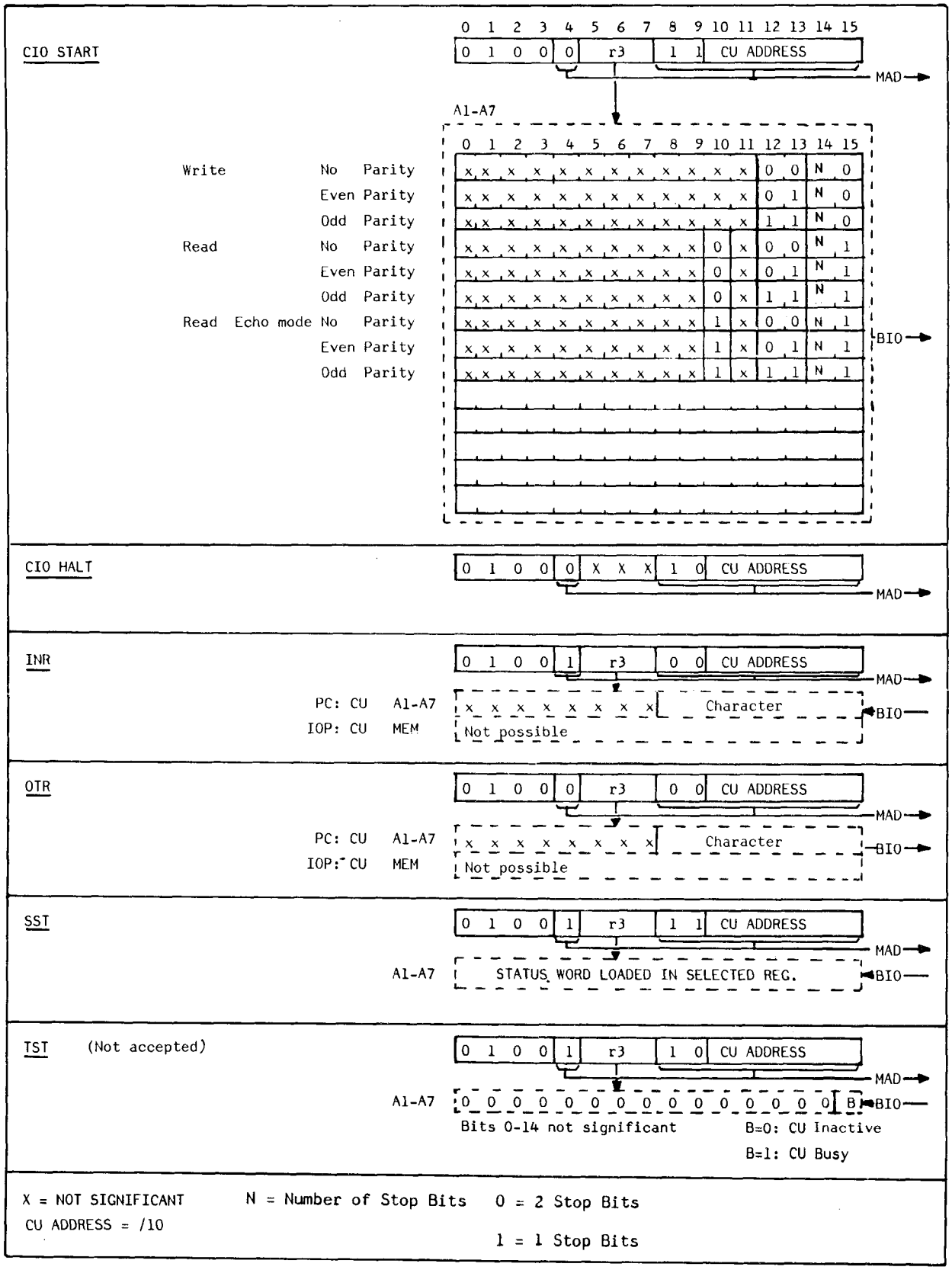
13.4.3 CONTROL UNIT STATES



Note: The states of the V24 Interface have a different significance at CPU level. Only ECHO, OUTPUT, INPUT are read by the V24 Status Indicators. When these bits are all zero, the CU is in the Inactive State.

Figure 13.4 V24 INTERFACE STATES

13.4.4 HARDWARE-SOFTWARE INTERFACE DETAILS V24

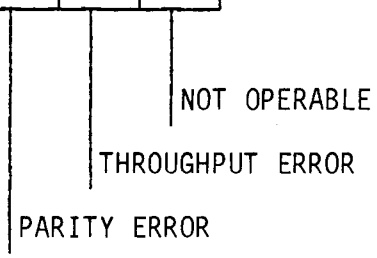


Note: * Bit 14 = 1: only one stop bit (necessary it terminal operates with one stop bit

Figure 13.5 INSTRUCTION-/COMMAND-WORD FORMATS

13.4.4.1 STATUS WORD

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0	0	0	0			



NOT OPERABLE

Bit 15 is set if the device is not connected or not operable.

THROUGHPUT ERROR

Bit 14 is set during input mode, if the interrupt is not yet answered by the CPU (INR) and the next input character arrives.

PARITY ERROR

Bit 13 is set when during input mode the received character has incorrect parity.

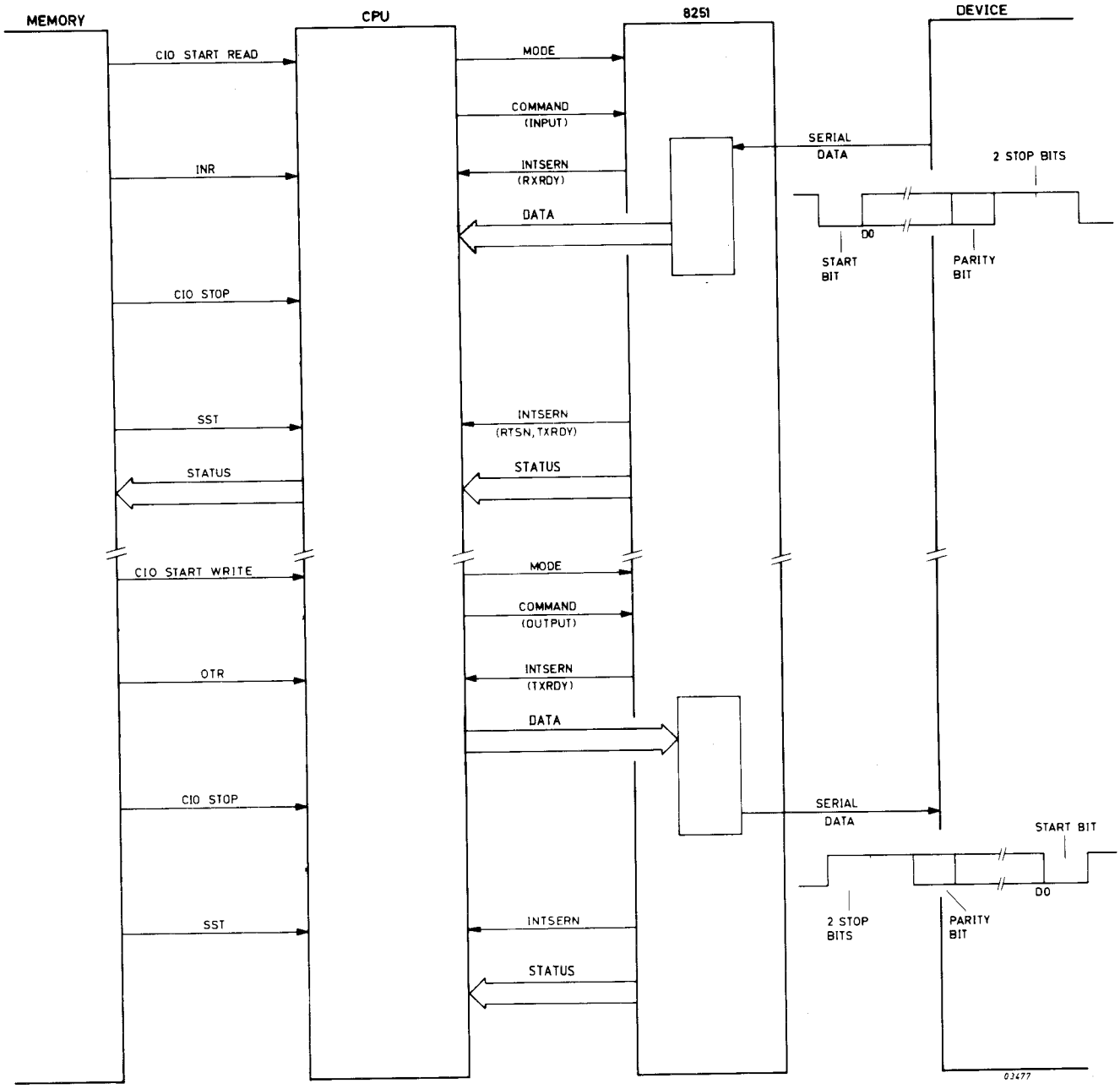


Figure 13.6 V24 PERIPHERAL INTERFACE DIALOGUES

13.5 HARDWARE SOFTWARE INTERFACE DETAILS CPU

In case the CPU detects either an unknown instruction code or a priviledged instruction in USER mode, the CPU will jump to the TRAP routine.
Actions executed by the CPU are slightly different from an interrupt:

- store Program Counter (here: address of the 'wrong' instruction
- store PSW (save condition register)
- update A15 (for possible interrupt)

] STACK

- INHibit for interrupts
- USER to SYSTEM mode
- ABI to address /7E

(/7E contains the startaddress of the TRAP routine)

Memory Layout of Interrupt and Trap Table:

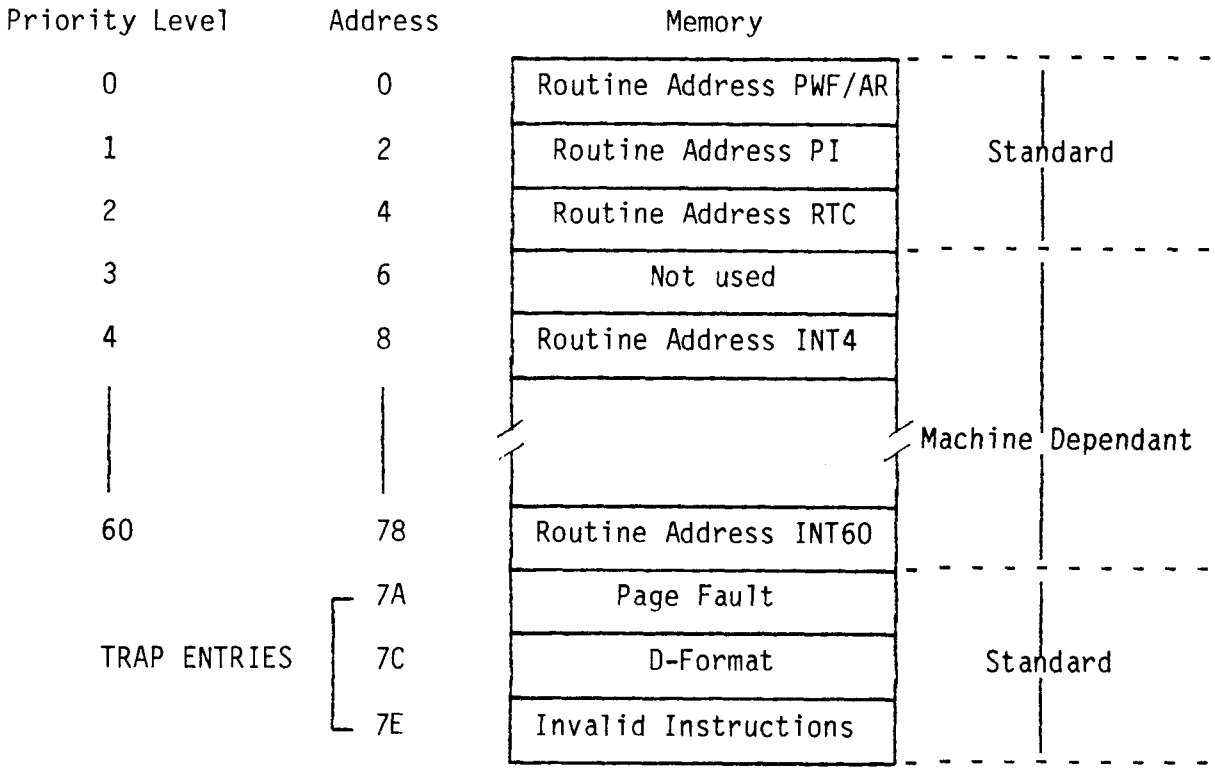


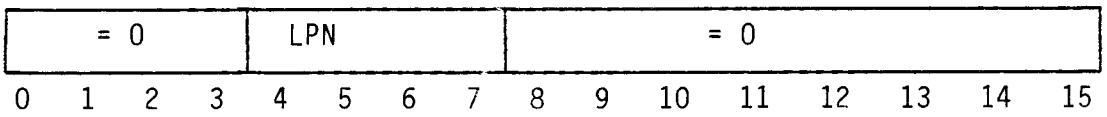
Table 13.4 INTERRUPT/TRAP LEVELS

Three kinds of traps can occur:

Memory Access Fault

Trap entry: /7A
This trap is activated whenever the CPU (User Mode) is informed of a "Page Fault" detection in the Memory Management Unit. For the particular trap, in addition to the P and PSW registers, a third parameter is pushed up into the stack: the 3rd word contains the Logical Page Number (LPN) on which the page fault was detected:

FORMAT:



Not Wired Instruction in D-Format

Trap entry: /7C
This trap can be used for software simulation of not wired instructions of the D-format type (OPC = 1101, T8 mode).

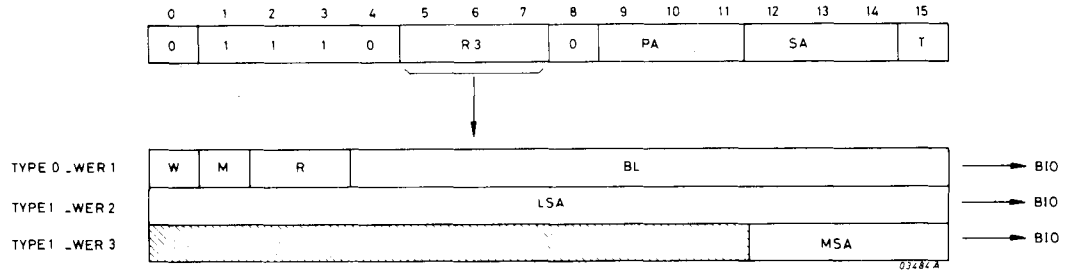
Invalid Instructions

Trap entry: /7E
This trap is dedicated for "abort" action if any of the following are detected:

. non-existing instructions
. privileged instructions detected in User Mode
. system stack access in User Mode

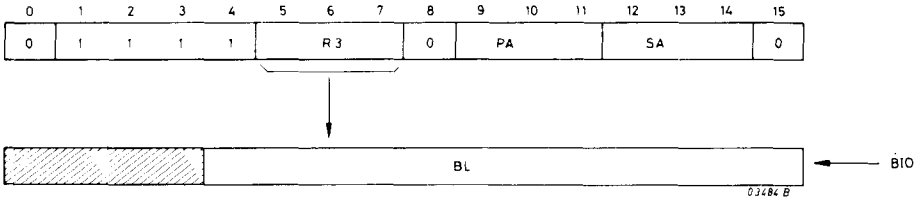
13.6 HARDWARE SOFTWARE INTERFACE DETAILS MIOP

13.6.1 IOP WRITE EXTERNAL REGISTER INSTRUCTIONS (WER)



PA IOP Address; for MIOP always 000 or 001 (IOPØ or IOP1).
SA Sub-channel address linked to PA to give the 6-bit C.U. address.
T Type of WER = 0 (WER 1), = 1 (WER 2 and 3).
W Word Transfer Indicator: = 0 transfer is an 8-bit character
M Output Mode: = 1 direction of exchange is memory to C.U.
R Address Bits (MAD128 and MAD64). If WER 3 is used these bits are overwritten by the MSA Field.
BL 12-bit block length: depending on W the block length is eiher a number of words or characters. When BL = 0 the length is 2^{12} words or bytes.
LSA Least significant bits of the memory start address of the block to be read or written.
MSA Most significant bits of the memory start address.

READ EXTERNAL REGISTER INSTRUCTION (RER)



PA IOP Address: for MIOP always 000 or 001 (IOPØ or IOP1).
SA Sub-channel address: linked to PA to give the 6-bit C.U. address.
BL Indicates the remaining length to be transferred.

Figure 13.7 IOP COMMAND FORMATS

13.6.2 MEMORY MANAGEMENT UNIT - FUNCTIONS

The Memory Management Unit (MMU) is a hardware facility which provides extended memory addressing and memory protection facilities for the P857R system.

EXTENDED MEMORY ADDRESSING (TRANSLATION)

The principal function of the MMU is to extend the memory addressing up to 512K physical words (20 address bits). (See Figure 13.8).
The basic rules for the operation of this facility are as follows:

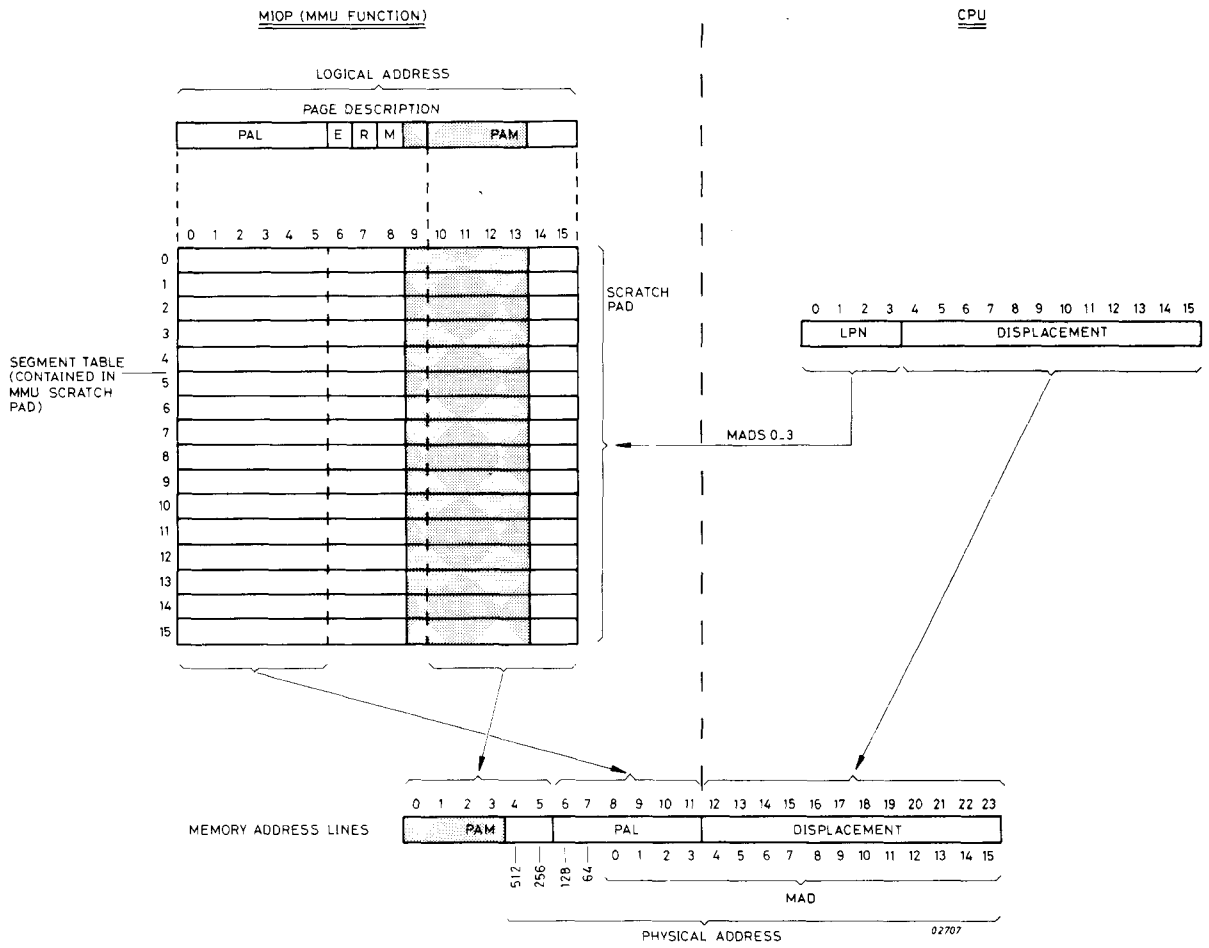
- A 16 segment table is pre-loaded with page addresses by one Table Load Instruction.
- All CPU/Memory transfers via the MMU use the four most significant address lines (MAD0-3) to select the table segment (page 0-15). The content of each page gives the 8 most significant MAD address bits plus 3 control bits.
- The Table Store instruction is used by software to read the 16 word segment table for test purposes or for dynamic relocation.

MEMORY PROTECTION

For memory protection purposes 2 information bits are loaded into the segment table at the same time that the TL instruction loads the page addresses; these information bits are:

- Bit 6 (E) Page Error if 1 page restricted to system mode only.
- Bit 7 (R) Read Only Indicator = 1 to protect the page against Write operations If a program in User Mode attempts to Write on this page then the translation is blocked.

In both of these cases the MMU indicates to the CPU that a Page Fault (PAF) has occured.



ABBREVIATIONS

PAL	— PAGE ADDRESS LEAST SIGNIFICANT
PAM	— PAGE ADDRESS MOST SIGNIFICANT
E	— PAGE ERROR; = 1 EXCEPT FOR MEMORY RESIDENT PAGES OF USER PROGRAM
R	— READ ONLY INDICATOR; = 1 TO PROTECT THE PAGE AGAINST WRITE OPERATIONS
M	— MODIFIED INDICATOR; = 1 WHEN A WRITE OPERATION IS PERFORMED FOR THAT PAGE
LPN	— LOGICAL PAGE NUMBER
DISPLACEMENT	— GIVES THE ADDRESS RELATIVE TO THE BEGINNING OF THE LOGICAL PAGE NUMBER
MAD	— MEMORY ADDRESS LINES

Figure 13.8 MEMORY MANAGEMENT

MODIFIED PAGE

This feature indicates to the operating system if a page needs to be "swapped out" or not. If it does not need to be "swapped out" then the new page can be overwritten so saving time. This possibility is indicated by bit 8 (M) which is set to "1" by the MMU whenever a Write operation (Store Instruction) is performed on a specific page.

PAGE FAULT

When an attempt is made to write into a protected page or access is made in user mode to a page that is restricted to system mode only, the MMU signal "Page Fault" initiates an interrupt TRAP Routine at the CPU. The sequence of events is indicated in the following Flow Chart:

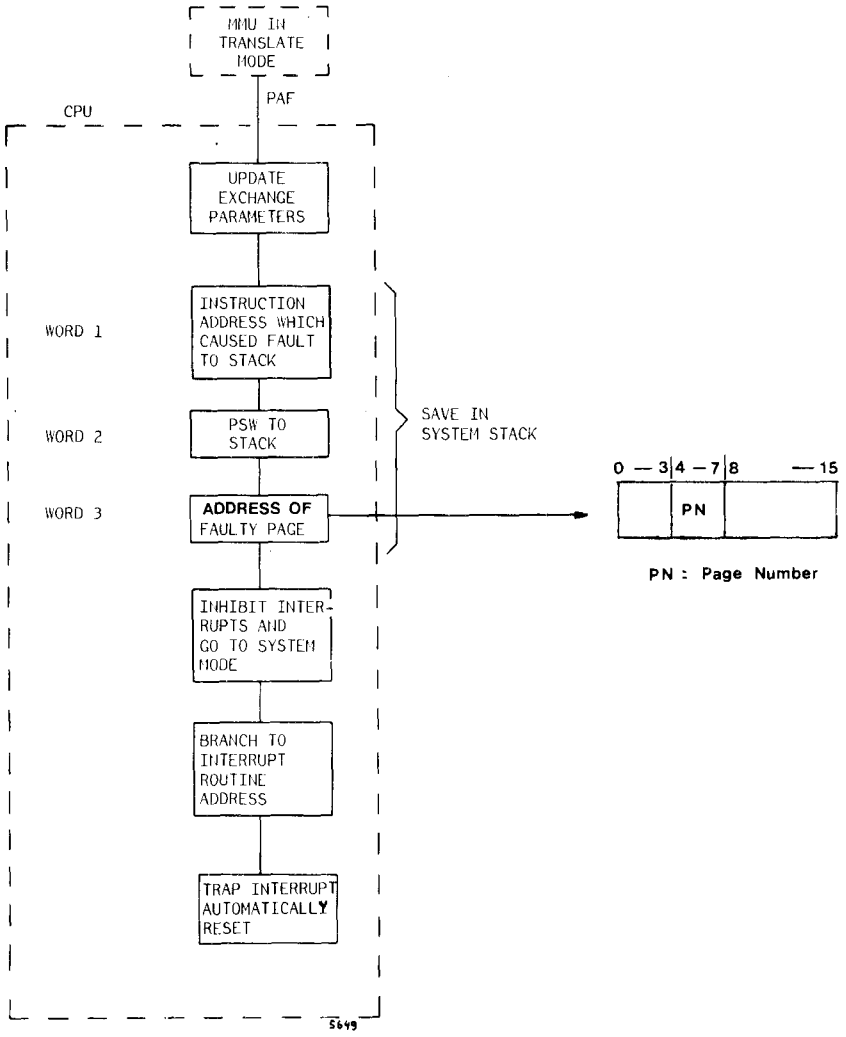


Figure 13.9 PAGE FAULT SEQUENCE

13.7 POWER SWITCH ON AND TEST

At switch-on a sequence of events takes place before the system is ready to go. This sequence of events may be considered as three separate phases.

. Phase 1 Automatic Test
. Phase 2 Microdiagnostic Test (only necessary if problems are expected)
. Phase 3 Load IPL (Initial Program Loader)

The hexadecimal codes of the HHCP and FRCP that are displayed after an event are indicated in the following flowcharts.

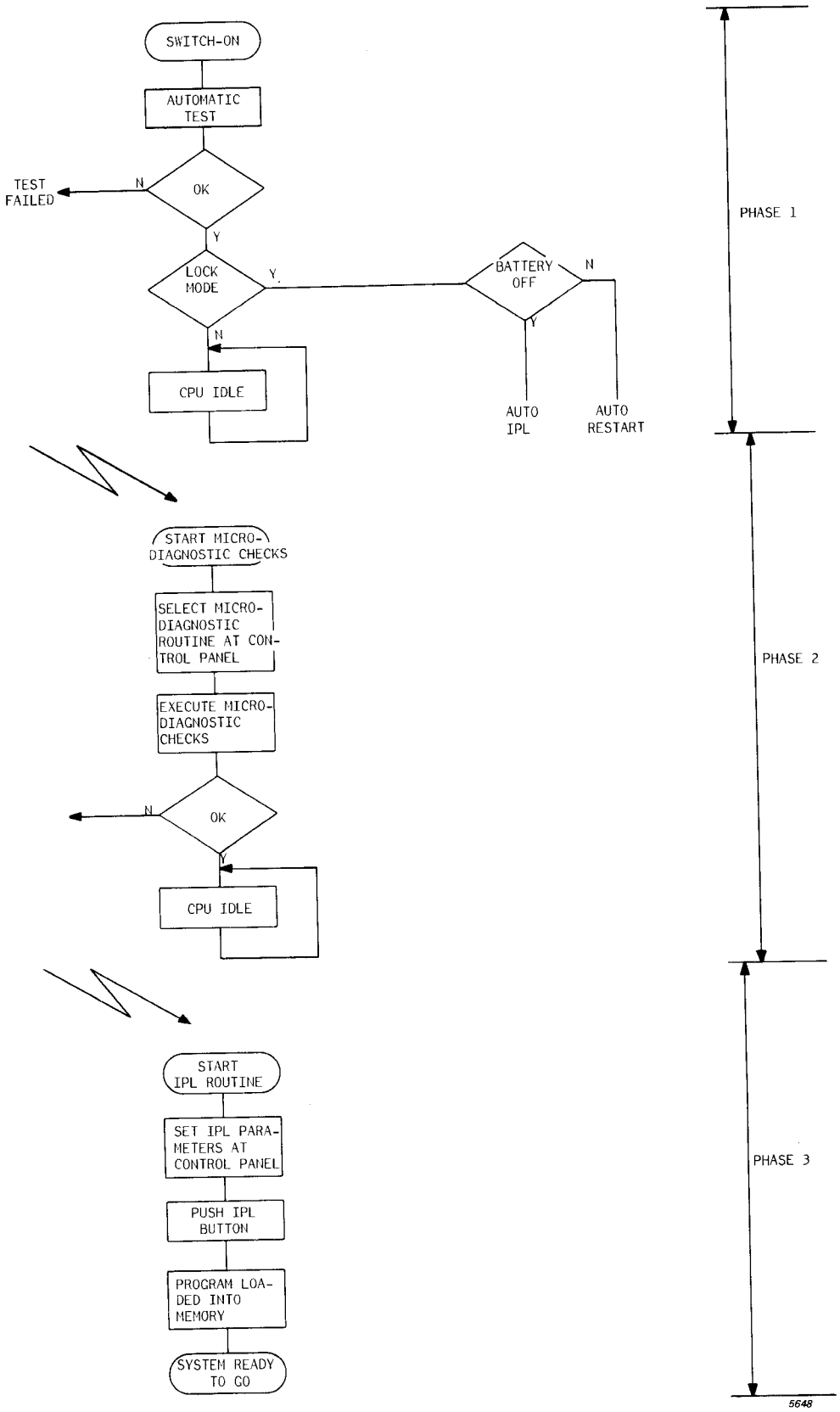


Figure 13.10 START PROCEDURE

13.7.1 AUTOMATIC TEST

An automatic test is executed at the power-on time. It tests the major part of the C.P.U., the Control Panel Interface, a part of the Control Panel itself and its cable. This test is terminated by displaying a code (FFFC) if the panel was not in LOCK state and if the test was O.K.

This automatic part of the test is of "go-no go" type. If the expected code is not displayed it is not possible to distinguish if the problem is due to the C.P.U., to the Control Panel or its cable and it is not possible to run further tests.

But if this first phase runs well and if displaying is possible and correct, in the second phase the C.P.U., C.U. and Memory failures could be distinguished from one another.

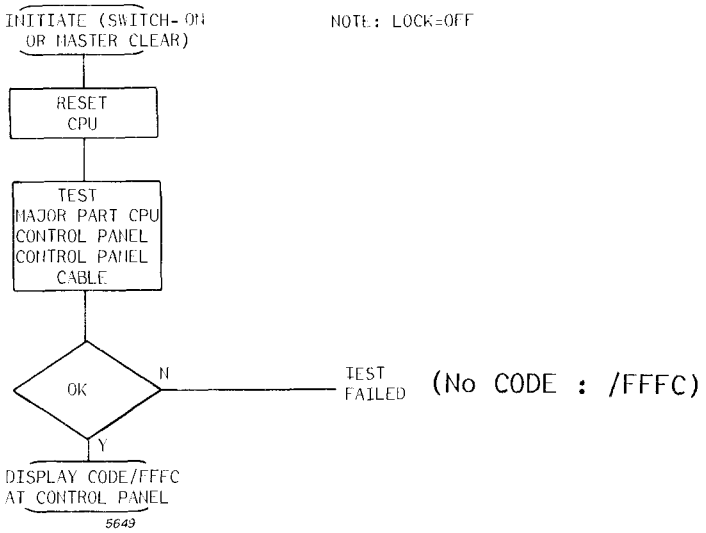


Figure 13.11 AUTOMATIC TEST

13.7.2 MICRODIAGNOSTIC TEST

The second phase is initialized by pressing the 0 and TEST push buttons on the Control Panel and it consists of the end of the C.P.U. test, RAM test (up to 32K), CPU-CU V24 (Address /10) dialogue test and MMU/IOP (MIOP) test.

At the end of this second phase, another code is displayed meaning either the correct end of test or an error.

These codes are:

C.P.U. error : Code 0001
BUS or CU error : Code 0002 or YY02
BUS or RAM error : Code XX03
O.K. : Code YY04
MIOP error : Code YY10

XX = Most significant 8 bits of the memory address causing the error.
YY = Most significant 8 bits of the last memory address.

The operator can read the address causing the error in A1, and the contents of this address read by the CPU in A2.

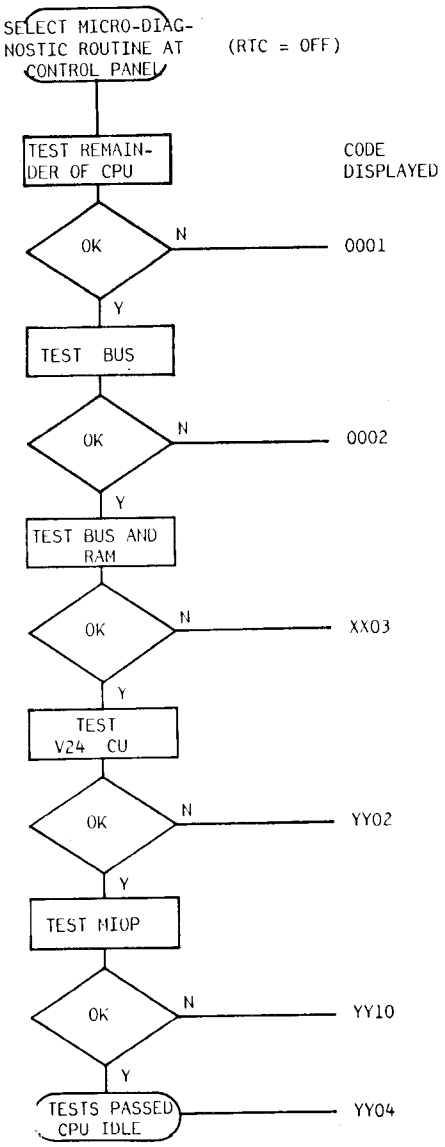


Figure 13.12 MICRODIAGNOSTIC TEST

13.8 SHORT DESCRIPTION OF TESTPROGRAMS

TESTPROGRAM TP 57 RE (PTS-108)

Mem. size 8Kw.
No output on CTW.
No power failure allowed.

Procedure:

. IPL

For this program the number of runs is output in hexadecimal format on sop panel. If an error occurs the count is stopped but no information on the error is done. It is only a GO/NO GO test.
If a parasitic interrupt occurs, its level is output on the sop panel with flashing lamps.

One complete CPU test lasts 1 - 2 seconds.

Tested: all CPU instructions are tested one by one.
I/O instructions and bus controller are not tested.

Procedure 5111 991 11291 = procedure CP57RE 5111 991 10353
with addendum PTS6000 5111 991 11381

Listing 5111 991 11201
Program 5111 991 62531

PROGRAM TEPAF (PTS-110) 32kw mem. min.
test for page fault, RTC also allowed.
test of auto restart

.IPL

- switch on the RTC (LOCK for PF/AR)
- The program loops continuosly.
(one loop lasts about 0.1 sec.)

For this program the number of runs is output in hexadecimal format on sop panel. If an error occurs the count is stopped but no information on the error is done. It is only a GO/NO GO test.
If a parasitic interrupt occurs, its level is output on the sop panel with flashing lamps.

--- for more info: see official description of testprograms ----

- Tested: correct processing of a page fault trap
correct resuming of the instruction, which caused the page fault
correct handling of RTC and Power Failure.

Procedure 5111 991 11311 = Procedure REPAF 5111 991 10371
with PTS6000 addendum 5122 991 11381

Listing 5111 991 11221

Program 5111 199 62511

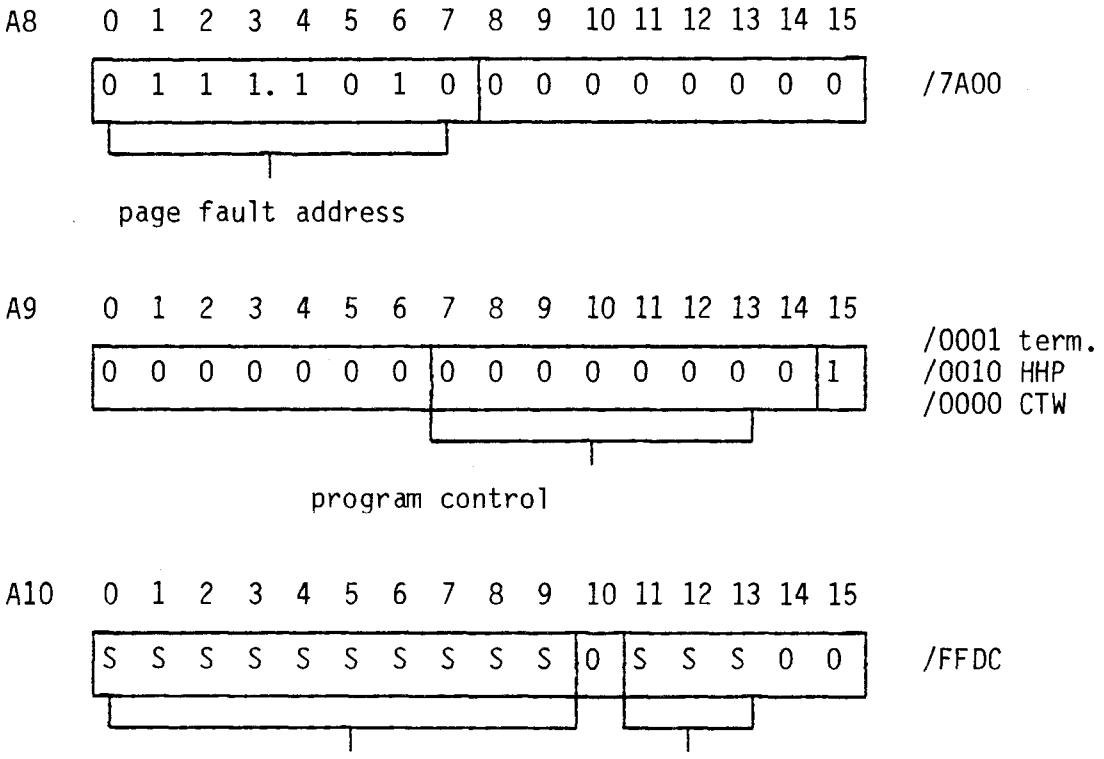
PROGRAM TEMMU1 (PTS-109)

mem. size 32 kw min.
test of MMU in memory size 0 - 32kw.
RTC, PF/AR allowed.

. IPL

. display /700 = restart point = after reception of unexpected interrupt.

- change registers:



- switch on RTC

The check which is executed, is displayed on the terminal.

. /700 normal end

. /5E0 info stop

- /5F0 error stop A1 contains error code.
(see also official description of testprogram).

Note: some checks are in inhibit mode. In such a case the power fail interrupt may be handled too late and auto restart fails.

13.9 SHORT ROUTINES

For CTW see chapter 9.6

13.9.1 SHORT ROUTINE MMU

```
00000                                   IDENT    MMU2
00001                           *
00002                           *
00003                           *PROGRAM TO TEST MMU FUNCTIONS
00004                           *
00005                           *THE USER PART OF THIS PROGRAM WILL BE TRAPPED ON A NOT ALLOWED
00006                           *STORE OPERATION IN PAGE 2.
00007                           *EACH TIME THE CP-INT BUTTON IS PRESSED, THE PROGRAM WILL BE
00008                           *MODIFIED, GIVING TRAPS ON ACCESS PAGE 1 OR WRITE ACCESS PAGE 2
00009                           *WHEN THE PROGRAM IS STOPPED BY A HLT INSTRUCTION IT IS POSSIBLE
00010                           *TO CHECK THE SYSTEM STACK (A15) AND THE SEGMENT TABLE (/300).
00011                           *
00012          0006     CPLEV   EQU      6                    FOR P854: /E IF P858/P859; C IF PTS 6814/24
00013                           AORG     /100
00014  0100    8841     PROGINT TS       /300                 SEGMENT TABLE TO MEMORY
       0102    0300
00015  0104    20F8             RIT      /1D
00016  0106    207F             HLT                           CHECKPOINT:TABLE + STACK
00017  0108    8840             TL       /200                 LOAD SEGMENT TABLE INTO MIOP
       010A    0200
00018  010C    87A0             LDKL     A15,/150             LOAD STACK POINTER
       010E    0150
00019  0110    8120             LDKL     A1,/FFE              PROGRAM COUNTER OF USER
       0112    0FFE
00020  0114    813F             STR      A1,A15               TO THE STACK
00021  0116    8120             LDKL     A1,/4041             PSW OF USER
       0118    4041
00022  011A    813F             STR      A1,A15               TO THE STACK
00023  011C    8120             LDKL     A1,/160              START ADDRESS TRAP ROUT.
       011E    0160
00024  0120    8141             ST       A1,/7A               PAGE FAULT TRAP ENTRY
       0122    007A
00025  0124    8120             LDKL     A1,/100              START ADDRESS PROG.INT ROUT.
       0126    0100
00026  0128    8141             ST       A1,2                 LEVEL 1
       012A    0002
00027  012C    8120             LDKL     A1,/400              START ADDRESS CPINT ROUTINE
       012E    0400
00028  0130    8141             ST       A1,CPLEV             LEVEL:P854=3,P858/9=7
       0132    0006
00029  0134    F03E             RTN      A15                  START USER PROGRAM (LEVEL=/10)
00030                           AORG     /160
00031  0160    8841     TRAP    TS       /300                 SEGMENT TABLE TO MEMORY
       0162    0300
00032  0164    207F             HLT                           CHECKPOINT:TABLE + STACK
00033  0166    8120             LDKL     A1,/200C             RESTART USER
       0168    200C
00034  016A    8141             ST       A1,/150              PROGRAM AT ADDRESS /200C (=/300C)
       016C    0150
00035  016E    813E             LDR*     A1,A15               A15 ADJUSTED +2 AFTER PAGE FAULT TRAP
00036  0170    F03E             RTN      A15
00037                           AORG     /200
00038  0200    0000     SEGTAB  DATA     /0000                SEGMENT TABLE PAGE 0
00039  0202    0400             DATA     /0400                PAGE 1
00040  0204    0D00             DATA     /0D00                PAGE 2
00041                           AORG     /400
00042  0400    8120     CPINT   LDKL     A1,/200              ROUTINE TO CHANGE TABLE :PAGE 1
       0402    0200
00043  0404    8141             XRS      A1,/202              BIT 6 (E) SET OR RESET
       0406    0202
00044  0408    200F             RIT      /0F                  RESET CONTROL PANEL INT.
00045  040A    F03E             RTN      A15                  GO BACK TO USER PROGRAM
00046                           AORG     /FFE
00047  0FFE    013F     USER    LDK      A1,/3F               PAGE 0 IS ACCESSED
00048  1000    1102     PAGE1   ADK      A1,2                 PAGE 1 IS ACCESSED
00049  1002    8F20             ABL      /2000                BRANCH TO PAGE 2 (/3000)
       1004    2000
00050                           AORG     /3000
00051  3000    8141     PAGE2   ST       A1,/500              STORE INTO PAGE 0
       3002    0500
00052  3004    8140             LD       A1,/2200             LOAD FROM PAGE 2
       3006    2200
00053  3008    8141             ST       A1,/2200             STORE INTO PAGE 2 (TRAPPED)
       300A    2200
00054  300C    2804             LKM                           CALL SYSTEM MODE VIA PROG. INT
00055  300E    0000             DATA     0
00056                           END
```

LIST OF ILLUSTRATIONS

14.1 MEMORY MODULES IDENTIFICATIONS

Type Number	Description	6810/12	6813/14	Mounting Code	Power requirements
				6881/6824	
PTS6822 P843-108	Memory module 8k 16-bit words of read/write core, cycle time 1.2 u sec.	X	X	1 slot	+ 5V.2.6A
PTS6823 P843-116 P843-216	Memory module 16k 16-bit words of read/write core, cycle time 1.2 usec.	X	X		
	Memory module 16k words of read/write core, cycle time 0.7 usec.	X	X		
PTS6825 P843-232	Memory module 32k words of read/write core, cycle time 0.7 u sec.		X		
PTS 6781 P843-528	Random access memory 128kW 21 bits			X 1 slot	

Testprograms: core memory 0-32K - ⟩ MEMTSC
core memory above 32K - ⟩

Power consumption for different core sizes in Ampères

Module size	+5V	-5V	16V
8K (1.2 µsec.) O.	2.5A	0.12A	3.6A
N.O.	2.4A	0.12A	0.4A
16K (1.2 µsec.) O.	2.8A	0.18A	4.6A
N.O.	2.6A	0.18A	0.5A
16K (0.7 µsec.) O.	3.2A	0.18A	5.7A
N.O.	2.7A	0.18A	0.7A
32K (0.7 µsec.) O.	4.5A	0.3A	4.7A
N.O.	4.0A	0.3A	0.7A

To derive power consumption at system-level, one module is assumed operating (O). The other modules are considered not-operating (N.O.)

Example: 2 x 16K (1,2 µsec) modules: +5V, 5.4A, -5V, 0.36A, 16V, 5.1A.

14.2 INSTALLATION DETAILS

Total capacity	Module(s) used	Addressing
8K.....	...One 8K-module.....	.....0-8K
16K.....	...One 16K-module....	.....0-16K
16K.....	...One 8K-module.....	.....0-8K
	One 8K-module.....	.....8-16K
24K.....	...One 16K-module....	.....0-16K
	One 8K-module.....	.....16-24K
32K.....	...One 16K-module....	.....0-16K
	One 16K-module ...	....16-32K

Before locating a memory module in the computer rack its address field must be strapped to enable correct addressing of the module. The Figures 2-22, 2-23, 2-24 and 2-25 show the existing versions of CMM straps.

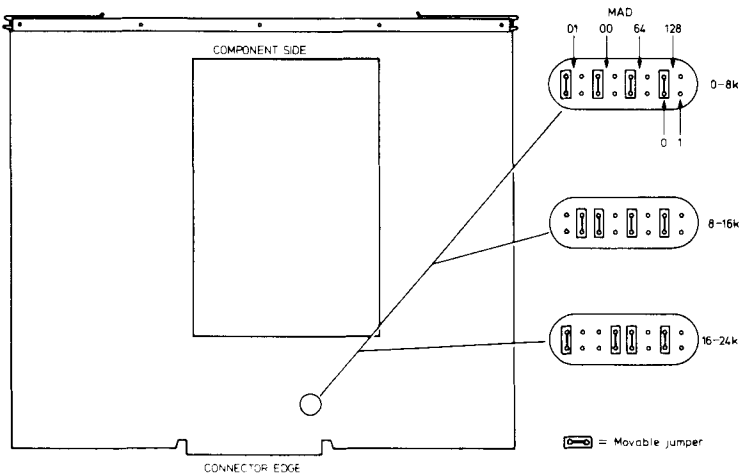


Figure 14.1 JUMPERS ON THE ELCOMA 8K CMM

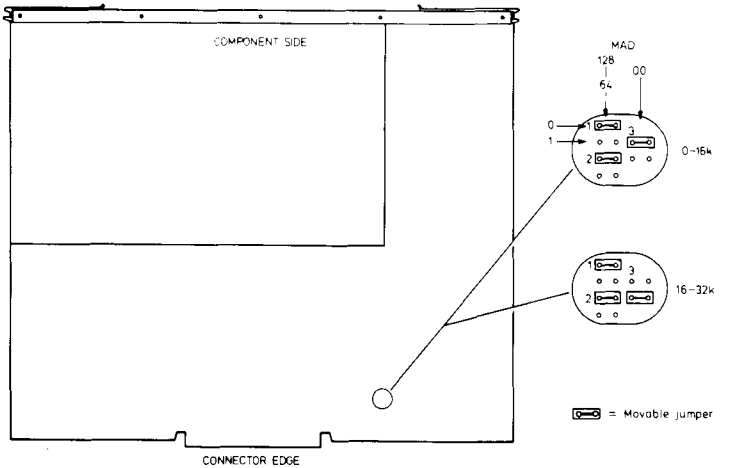


Figure 14.2 JUMPERS ON THE ELCOMA 16K CMM (EARLY VERSION)

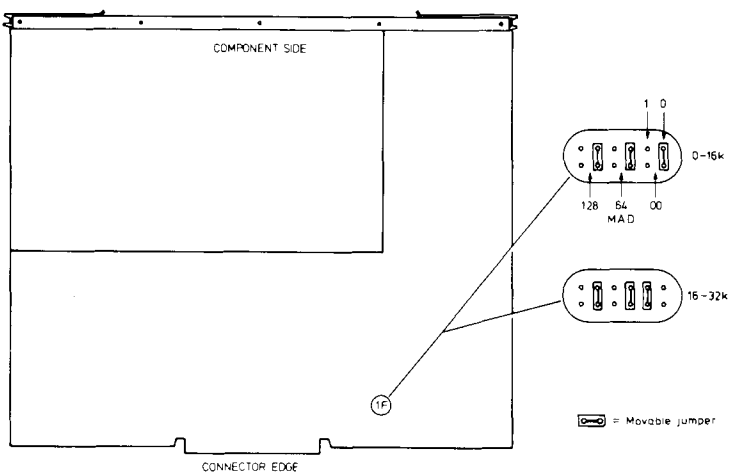


Figure 14.3 JUMPERS ON THE ELCOMA 16K CMM (LATER VERSION)

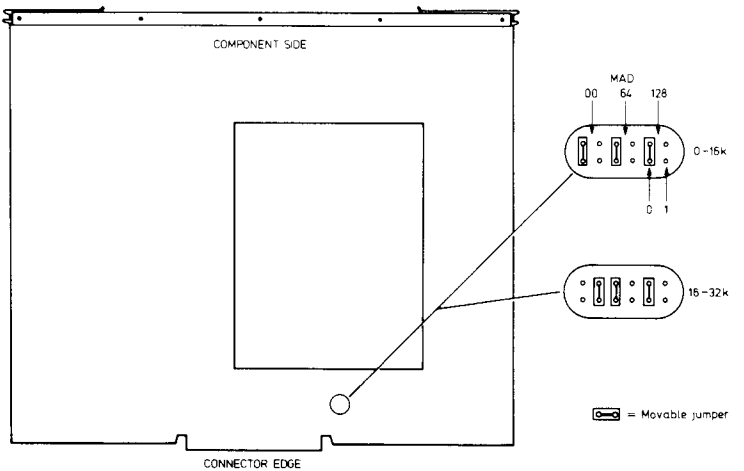
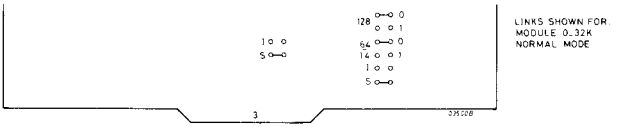


Figure 14.4 JUMPERS ON THE ELCOMA 16K CMM (EARLY VERSION)

The memory module or modules which comprises a complete memory are located as standard in slots 2 and 3 in the computer rack. Where both slots 2 and 3 are used for memory it is common practice to locate the first memory module (from address zero) in slot 2. However, as no physical differences exist between the slots, no fast ruling is necessary for the positioning of the two modules in specific slots.

STRAP ON S/N	AD 00/14	MAD 64	MAD 128	STRAP ON I
0 -16K	0	0	0	0 -32K even (bit 14)
16 -32K	1	0	0	0 -32K odd
32 -48K	0	1	0	32-64K even
48 -64K	1	1	0	32-64K odd
64 -80K	0	0	1	64-96K even
80 -96K	1	0	1	64-96K odd
96 -112K	0	1	1	96-128K even
112-128K	1	1	1	96-128K odd

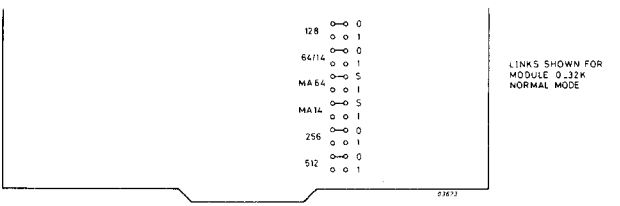
S = Standard addressing
I = Interleaving mode odd addressing



STRAPS ON S STANDARD	MAD 64/14	MAD 128	STRAPS ON I INTERLEAVING
0 -32K	0	0	0 - 64K even
32-64K	1	0	0 - 64K odd
64-96K	0	1	64-128K even
96-128K	1	1	64-128K odd

Figure 14.5a: 32K AMPEX

PTS6825 MEMORY MODULE



STRAPS ON S STANDARD	MAD 64/14	MAD 128	MAD 256	MAD 512	STRAPS ON I INTERLEAVING
0-32K	0	0	0	0	0-64K even
32-64K	1	0	0	0	0-64K odd
64-96K	0	1	0	0	64-128K even
96-128K	1	1	0	0	64-128K odd
128-160K	0	0	1	0	128-192K even
160-192K	1	0	1	0	128-192K odd
192-224K	0	1	1	0	192-256K even
224-256K	1	1	1	0	192-256K odd

448-480K	0	1	1	1	448-512K even
480-512K	1	1	1	1	448-512K odd

Figure 14.5b: 32 K FABRIEK MEMORY MODULE

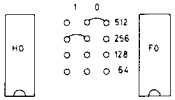
STRAPSETTING M128E/32/64 MODULES

STRAP 1
(Clear Register)

: Normally fitted for applications in which the CLEARN bus line is used.

STRAPS 2 and 3
(Memory Module No.)

STRAPS 4 and 5
(Memory Module Size)

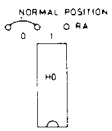


: EXAMPLE ONLY

Memory Module No. 1
Memory Size 128K

Note: For 64K variant fit strap '128'
For 32K variant fit strap '64'.

STRAP 6

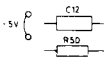


: Normally fitted to interconnect MI-1 and N04. Can be refitted to interconnect MI-1 and H0-10 so that a test program resides in memory block 16-32K. This allows memory block 0-16K to be tested.

STRAP 7

: Normally fitted. Open during initial production-test to protect memory stack.

STRAP 8



: Normally fitted. Open during initial production-test to protect memory stack.

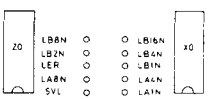
STRAP 9

: Not normally fitted: When fitted cancels the first 32K of stack addresses of Memory Module 0, only to accomodate another type of memory e.g. a 32K core memory.

STRAP 10

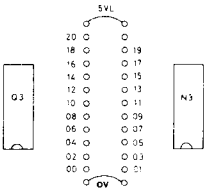
: Normally fitted, open during production test.

TEST CONNECTOR 1

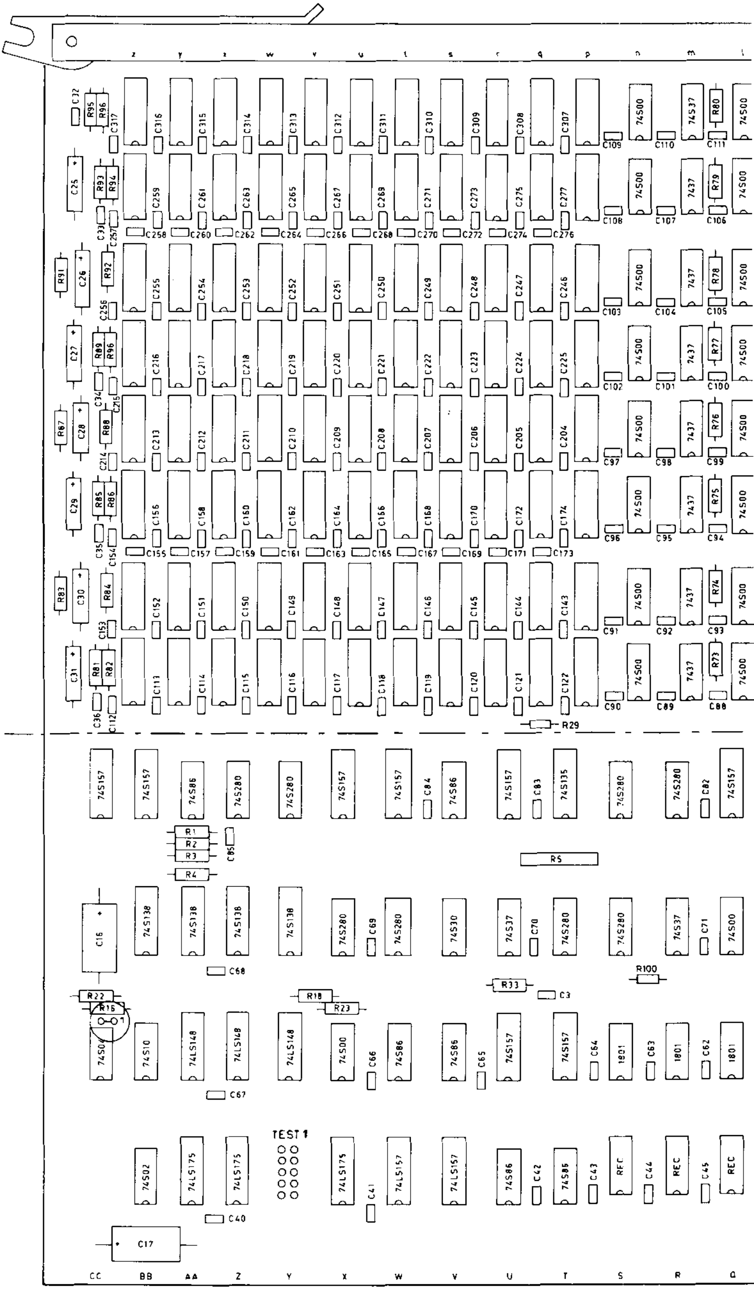


: During production-test it drives an LED display. Sometimes it is used to drive an application display.

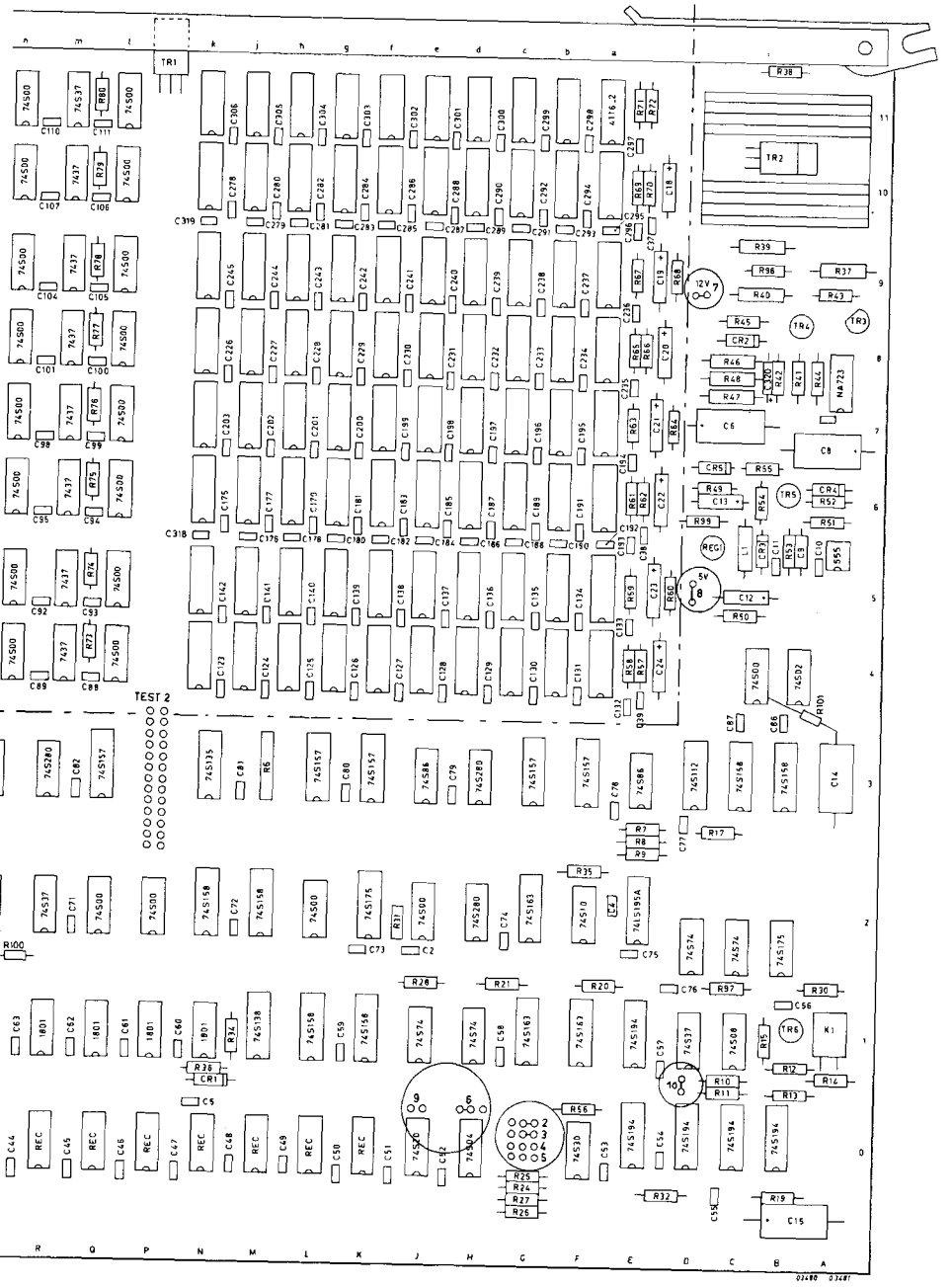
TEST CONNECTOR 2



: During production-test it is connected to a test box which simulates single-bit errors. Not normally used in the field.



LAYOUT


TR1
TR2
TR3
TR4
TR5
TR6
K1
TEST 2
12V
5V
C6
C8
C12
C14
C15
R38
R39
R96
R37
R40
R43
R45
CR2
R46
R48
R47
R42
R41
R44
NA723
CR5
R55
R49
C13
R54
R99
R51
CR4
R52
C11
C10
555
R50
R101
C87
C86
R17
R35
C4
C75
R97
C76
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C46
C45
C44
R36
CR1
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C63
C62
C61
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C58
C57
R26
R21
R20
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C2
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C74
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C71
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14.5 SHORT DESCRIPTION TESTPROGRAM

TESTABLE CONFIGURATIONS

The test program MEMTSC Release 2 can be used for testing core - and semiconductor memories of 32-256 Kbytes in the terminal computers 6805 and 6810-6813. Basic testing requires no extra equipment, a cassette or a diskette drive and the SOP provide the necessary man-to-machine interfaces.

WATCHED & TESTED FUNCTIONS

The program basically:

- Watches the power on/off handling in PSU and CPU (note: for test of this function; use instead the test program CPUTSC Release 2).
- Watches the occurence of invalid instruction codes.
- Watches the occurence of unwanted interrupts (all interrupts that are not expected by the program).
- Tests the memory function. Program move enables a test of the complete memory.

BAISC TEST - 'GO/NO GO'

PROGRAM LOAD & INITIATION

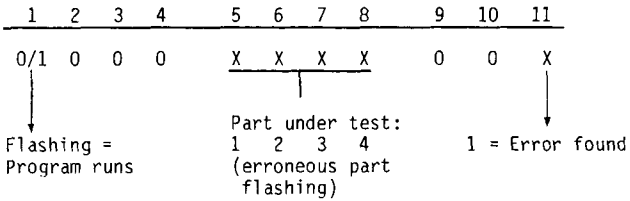
When the program has been loaded from a cassette or a diskette drive, it will automatically start a short sequence for initiating timers and identifying the memory system. Then it stops and lights the following SOP indicator (marked with 1):

1	2	3	4	5	6	7	8	9	10	11
1	0	0	X	X	X	X	X	0	0	0
			MMU	Memory Part: 1	2	3	4			

Note: Lit X-indicator = fitted unit. When MMU is fitted; each memory part represents 64 Kbytes in a physical memory module of its own. If no MMU is fitted; each part represents 16 Kbytes without any fixed relation to physical memory modules (a module may contain 16, 32 or 64 Kbytes).

PROGRAM RUN & ERROR INDICATIONS

Select NO STOP on error by operating SOP switch 3 (the indicator will be lit), and start the program by operating SOP switch 1. The program will now run through a single-shot test cycle, provide that no stop is caused by another operation of SOP switch 1, or a watched function (power failure, invalid instruction or unwanted interrupt). If no errors are found, a complete test cycle takes about 35 seconds/64 Kbytes. During run time the SOP indicators will display:



Should SOP switch 1 be operated during run time, or if no errors have been found at the end of the test, the program returns to the initial state described in section 2.1.

Should the program stop on a watched function, or find one or more memory errors, it will switch to an error display state. The three rightmost SOP indicators will then display the main function that has failed.

9	10	11	
0	0	1	= Power On/Off Error
0	1	1	= Invalid Instruction Code
1	0	1	= Unwanted Interrupt
1	1	1	= Memory Error

Further error investigations are described in detailed description

Program MEM

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	818E	Write	LDR	A9,A11
0088	85A7	Load	STR	A13,A9
008A	91A0		ADKL	A9,2
008C	0002			
008E	E992		CWR	A9,A12
0090	5C0A		RB(4)	Load
0092	5700		RF	* +2
0094	818E		LDR	A9,A11
0096	80A6	RDC	LDR*	A8,A9
0098	E896		CWR	A8,A13
009A	5002		RF(0)	Suit3
009C	207F		HLT	Fault
009E	91A0	Suit3	ADKL	A9,2
00A0	0002			
00A2	E992		CWR	A9,A12
00A4	5C10		RB(4)	RDC
00A6	5F22		RB	Write

Start the program:
- Load the starting address in register A11
- Load the ending address in register A12
- Load the test-pattern in register A13
- Load the start-address of the program (/0086) into register A0
- Push the RUN button

After Start:
   If no fault the program runs in loop

   Fault: program stops at /009E

- A9 contains address of erronous memory location
- A8 ,, read pattern
- A13 ,, expected pattern

DUMP FACILITY

This program enables an area of memory to be printed out on either the ASR or PTS3100, or to be Displayed. It can be loaded either with the IPL routine or by hand using the control panel switches. Once loaded the following routine should be used:

- Load the starting address to be printed into register A7. *)
- Load the ending address of the area into register A8.
- Load the starting address of the program into register A0.
- Push the RUN button.

The program will stop when the last memory address has been either printed or displayed.

*) Bit 15 must be zero.

Program DUMP

Memory Address	Data	Program Instructions		
0080	FFFF		DATA	-/FFFF
0082	0000		DATA	0
0084	207F	START	HLT	
0086	20BF		INH	
0088	47D0		CIO	A7,1,/10
008A	813C	WORD	LDR *	A1,A7
008C	0204		LDK	A2,4
008E	060F	CONT	LDK	A6,/F
0090	A604		ANR	A6,A1
0092	E558		LC	A5, TABLE, A6
0094	00BE			
0096	E549		SC	A5,BUFF + 1.A2
0098	00CF			
009A	39E4		SRC	A1,4

Memory Address	Data	Program Instructions		
009C	1A01		SUK	A2,1
009E	5C12		RB(NZ)	CONT
00A0	E348	OUT1	LC	A3,BUFF,A2
00A2	00CE			
00A4	4310		OTR	A3,0,/10
00A6	5C04		RB(NA)	* -2
00A8	1201		ADK	A2,1
00AA	EA20		CWK	A2,6
00AC	0006			
00AE	5C10		RB(NE)	OUT1
0080	1702		ADK	A7,2
00B2	EF02		CWR	A7,A8
00B4	5D2C		RB(NG)	WORD
00B6	4790		CIO	A7,0,/10
00B8	4FD0		SST	A7,/10
00BA	5C04		RB(NA)	* -2
00BC	5F3A		RB	START
00BE	3031	TABLE	DATA	'0123456789'
00C0	3233			
00C2	3435			
00C4	3637			
00C6	3839			
00C8	4142		DATA	'ABCDEF'
00CA	4344			
00CC	4546			
00CE	0D0A	BUFF	DATA	/0D0A

Notes:

LIST OF ILLUSTRATIONS

15.1 CHCR-IDENTIFICATIONS

Type-number: PTS 6833

Test-program: CASTST (only PTS 6810/12) AND PERTST

Channel: Programmed (PC) (Hardware (MX) Channel never used)

Devices DCR1 - PTS 6861 - 001
DCR3 - PTS 6865

Power-consumption +5V 3.8A

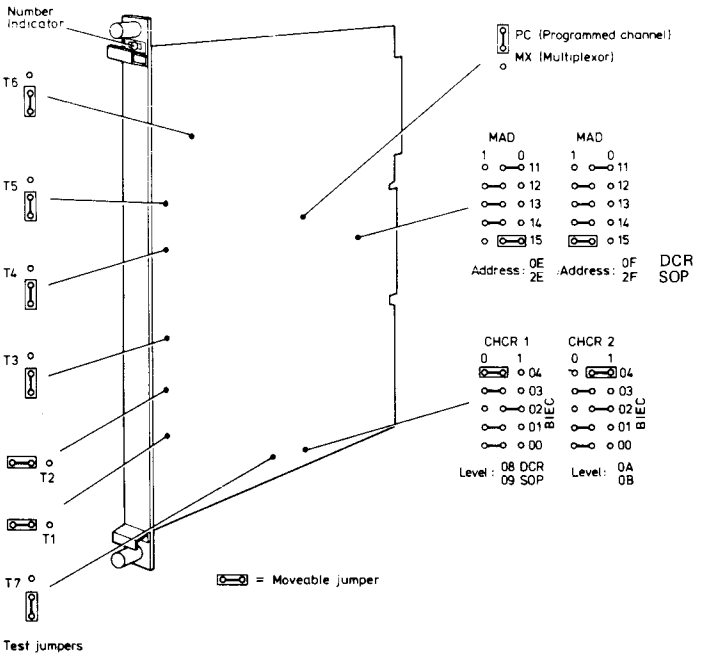


Figure 15.1 ADDRESS AND INTERRUPT STRAPS

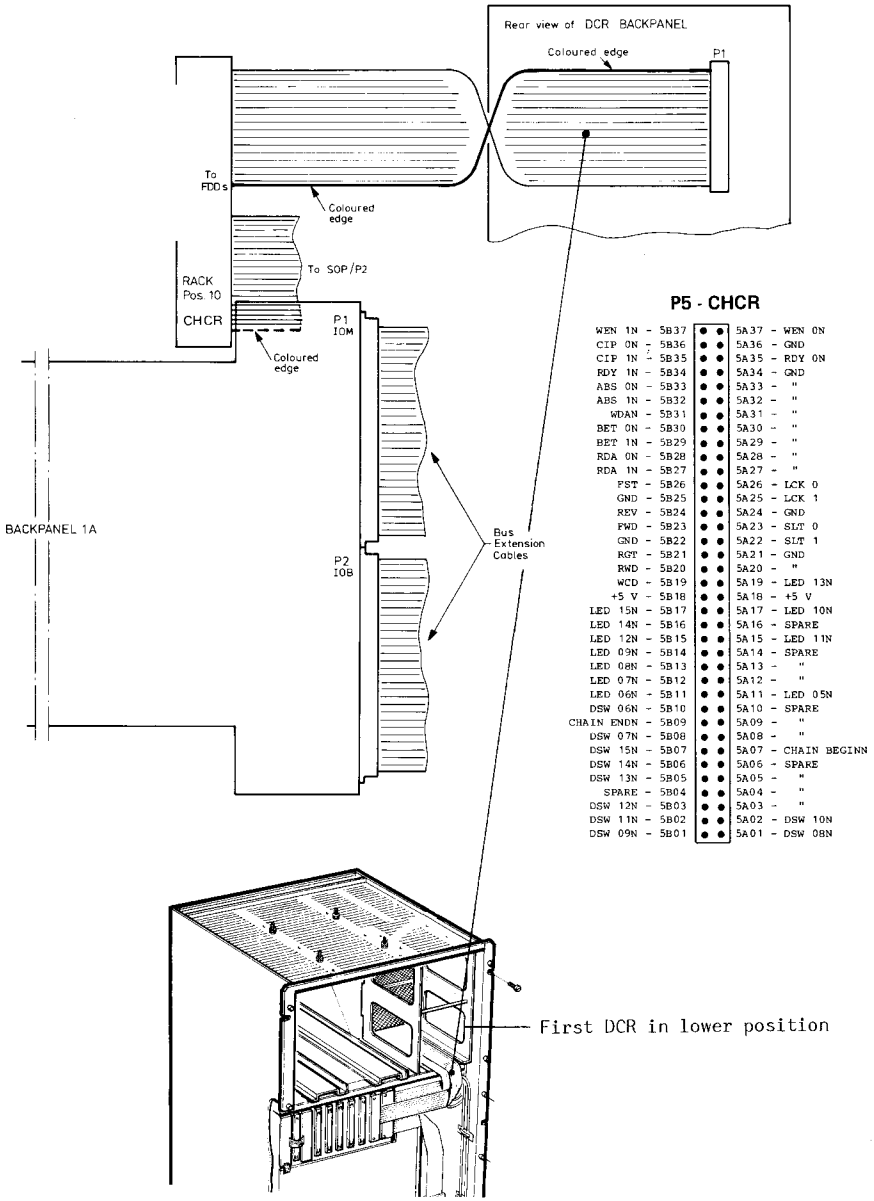


Figure 15.2 DCR INTERFACE 6812/13

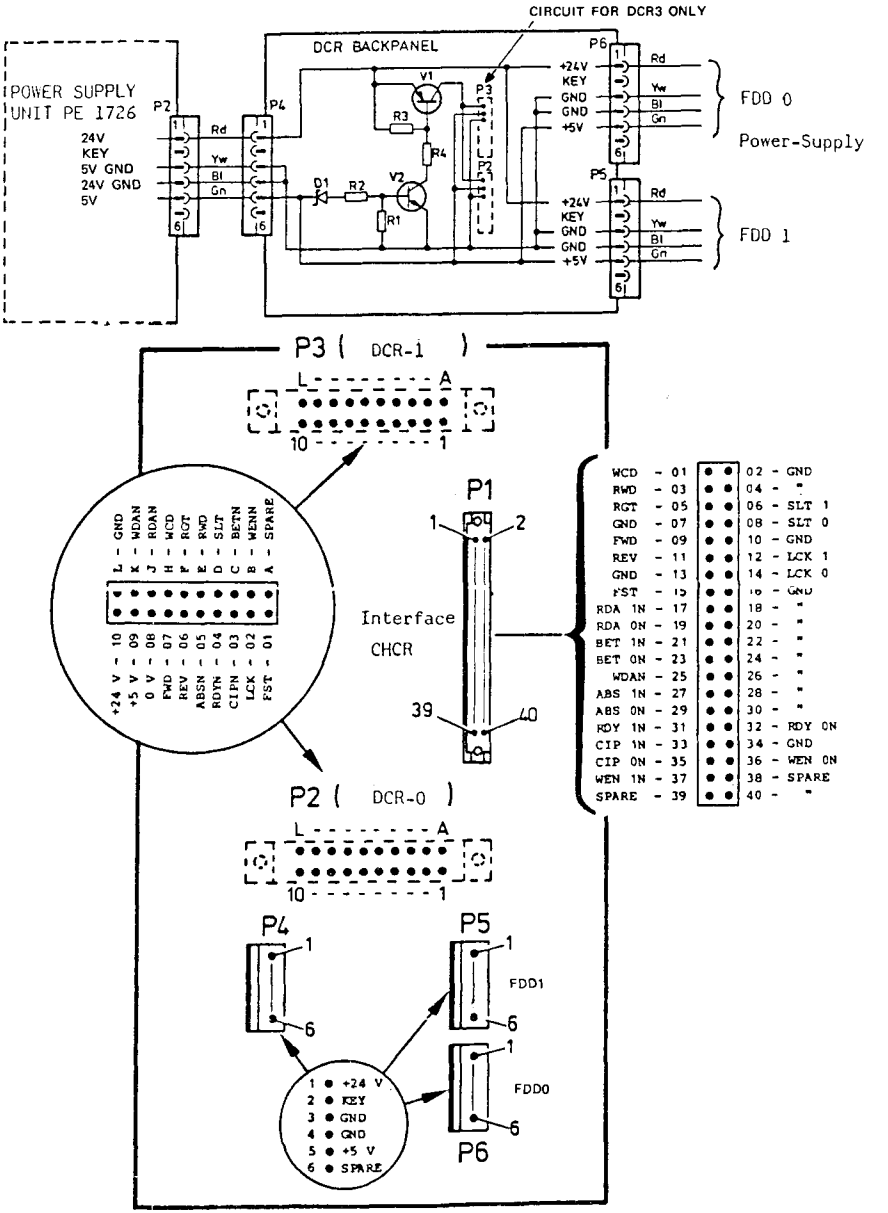


Figure 15.2a DCR INTERFACE PTS6812/13

CONNECTING DCR1 to 6810TC

Remove the panel in front of the recorder compartment by unscrewing four screws. Insert the DCR with precaution so the plug at the rear fits into the socket, flexibly mounted to a printed circuit board which is connected to the CPU rack via a flat cable. When only one DCR is fitted the DCR 2 socket must be equipped with a dummy board.

CAUTION: The dummy board has to be inserted with the text and the resistor, R1, upwards.

When a second DCR is not mounted a plastic cover must be mounted over its slot in the DCR-panel. The cover is fastened by means of double-adhesive tape.

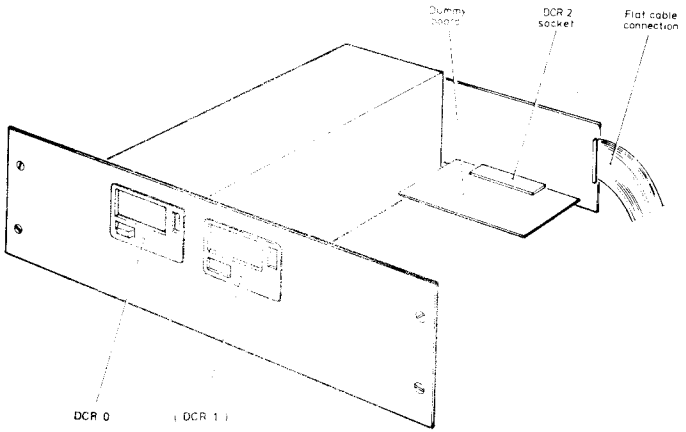


Figure 15.3 FITTING DCR (s) AND DUMMY BOARD (6810)

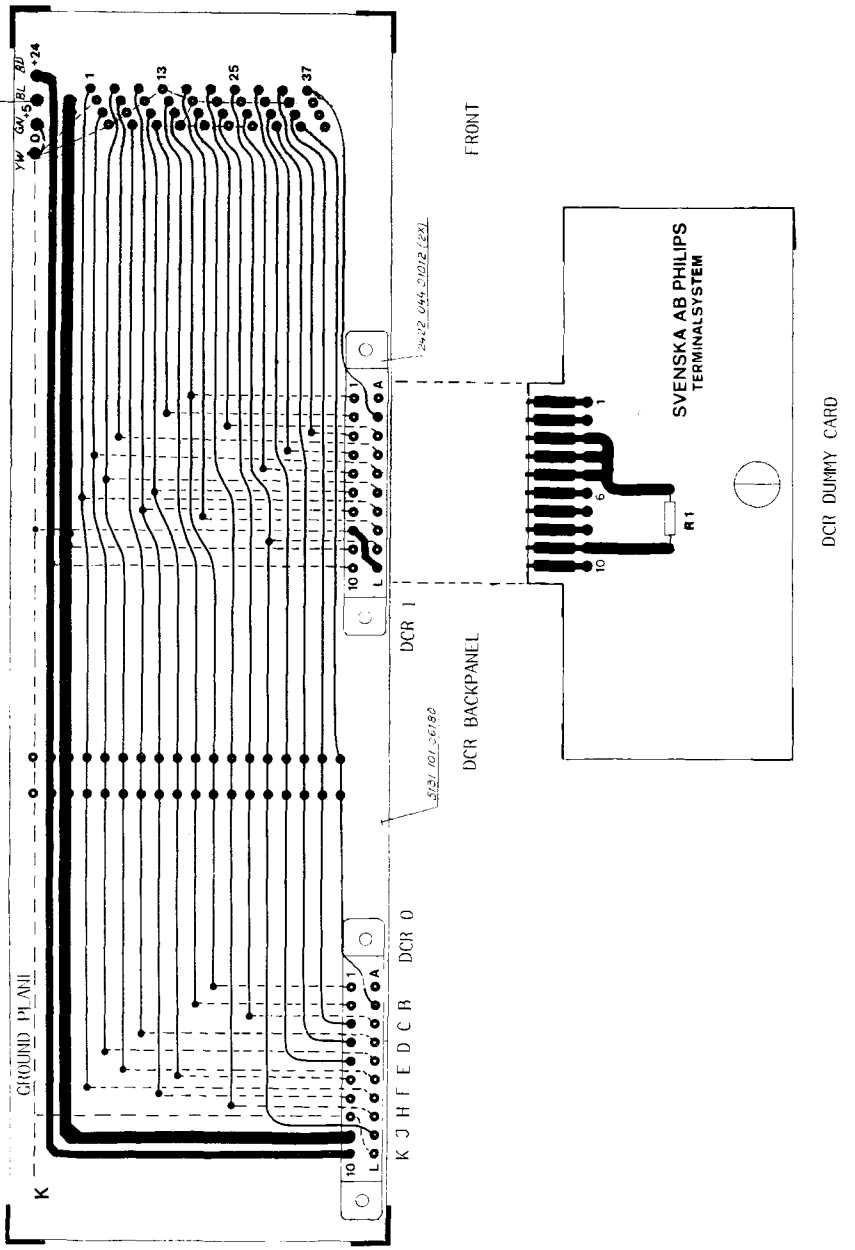


Figure 15.4 DCR BACKPANEL 6810

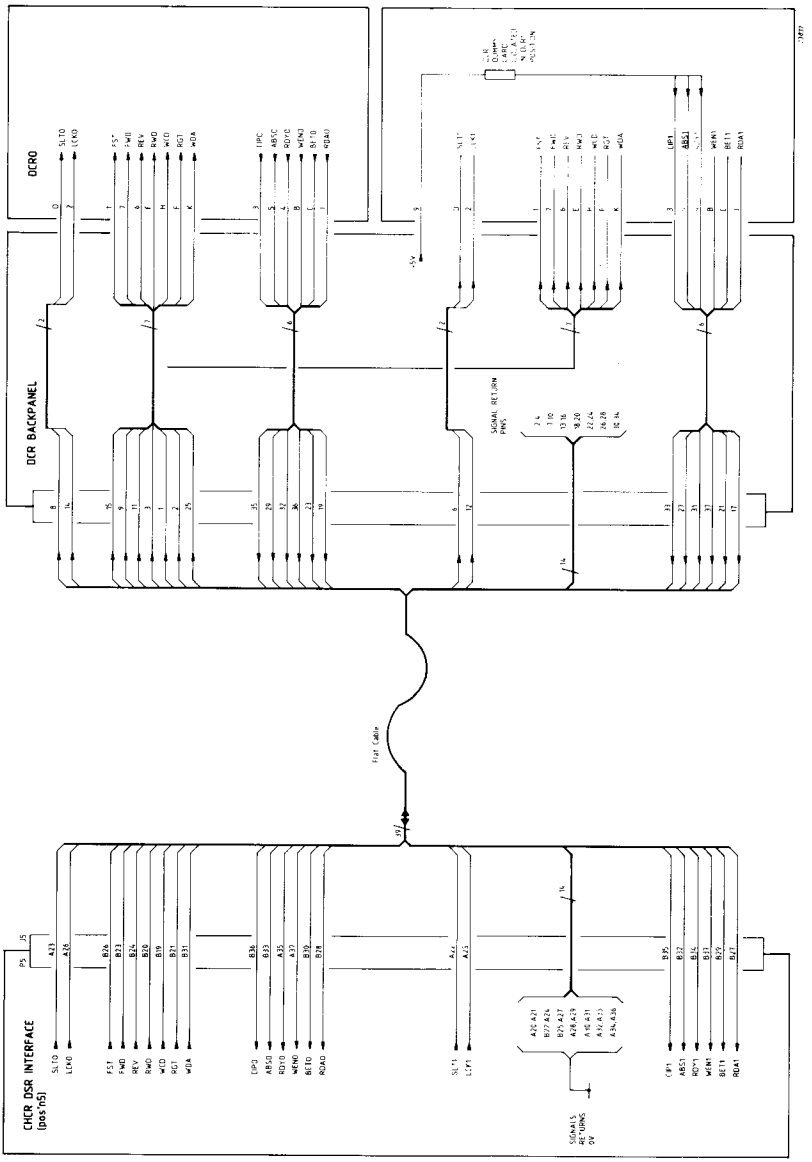
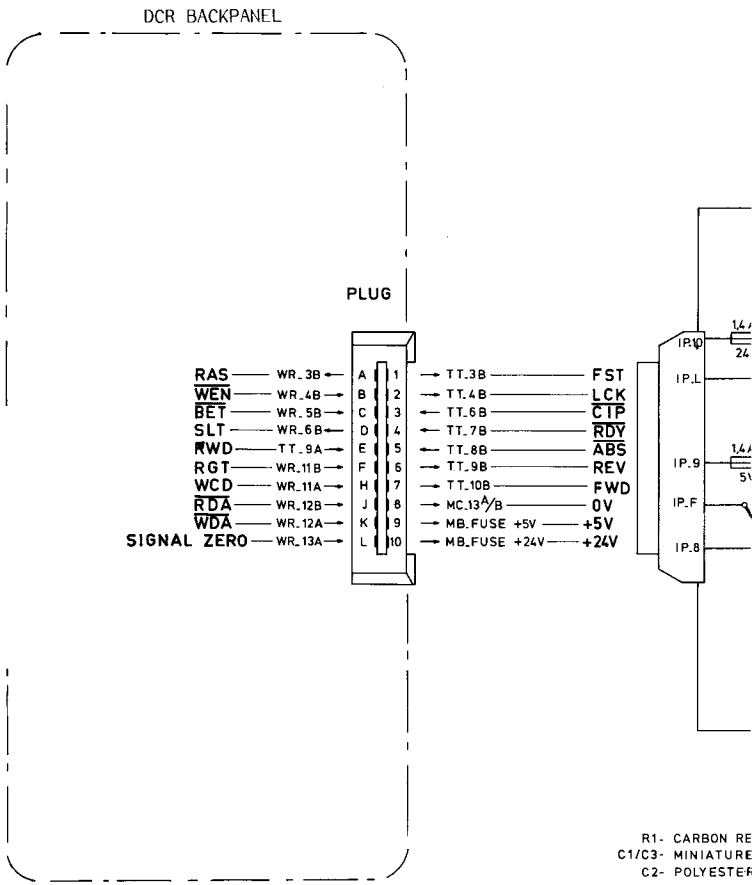


Figure 15.5 DCR DUMMY CARD (LOCATED IN DCR1 POSITION) (P6810)


DCR BACKPANEL
PLUG
RAS
WEN
BET
SLT
FWD
RGT
WCD
RDA
WDA
SIGNAL ZERO
WR_3B
WR_4B
WR_5B
WR_6B
TT_9A
WR_11B
WR_11A
WR_12B
WR_12A
WR_13A
A 1
B 2
C 3
D 4
E 5
F 6
H 7
J 8
K 9
L 10
TT_3B
TT_4B
TT_6B
TT_7B
TT_8B
TT_9B
TT_10B
MC_13A/B
MB_FUSE +5V
MB_FUSE +24V
FST
LCK
CTP
RDV
ABS
REV
FWD
0V
+5V
+24V
IP.10
IP.L
IP.9
IP.F
IP.8
R1- CARBON RE
C1/C3- MINIATURE
C2- POLYESTER

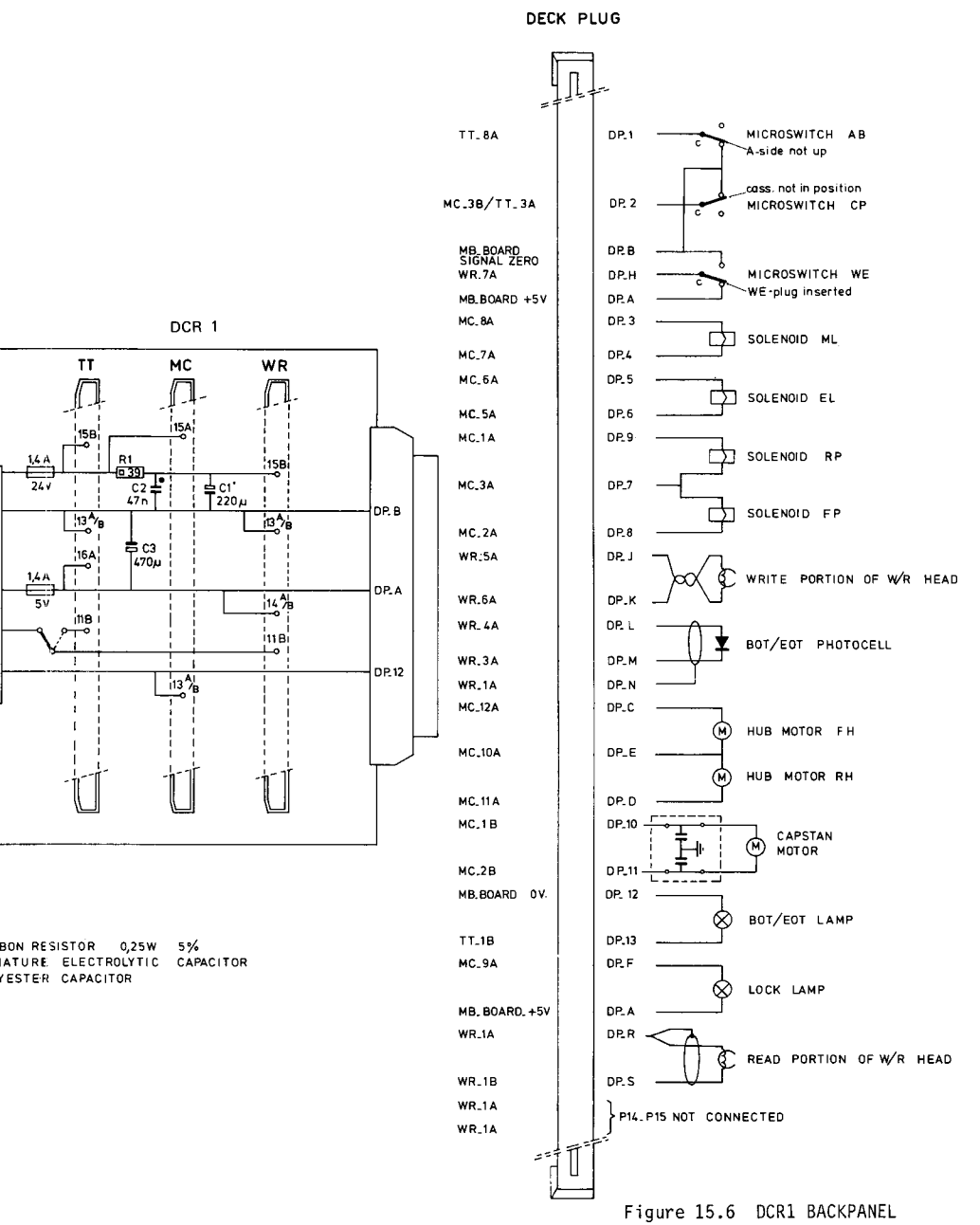


Figure 15.6 DCR1 BACKPANEL

15.4.1 STATUS WORD

Bit	Function	Meaning
15	Not Operable	Set if cassette not locked or at Rewind error.
14	Through-put error	Set if OTR, INR, CIO Halt or EOR is delayed more than 1.2 ms after each data interrupt.
13	CRC error	Set if CRC fails when reading data from the tape. (Applicable both at writing and reading).
12	Incorrect length	Set if numbers of INR's are less than numbers of characters in a read block (because of CIO Halt or EOR).
11	0	-
10	0	-
09	Rewind	Set if leader is not detected within 45 s during an "Sbot" command.
08	0	-
07	B-side	Set if B-side of the cassette is up.
06	Write protected	Set if chosen side (A/B) is write protected.
05	Bot or EOT	Set if BOT or EOT hole is passed.
04	No Data or Erased	Set if no data is detected within 2 s from Read Command (= 400mm) or if the tape is properly erased during an Erase command.
03	Tape Mark	Set if the last read, written or reversed block was a Tape Mark.
02	BOT missing	Set if the BOT hole is not found within 8 s after detection of leader during an "Sbot" command.
01	Leader	Set if the tape leader or BOT/EOT hole is positioned in front of the BOT detector.
00	0	-

For 6813: and 6810
Codes 10 -19 see PERTST

CASTST - Test of Cassette Recorder (PTS 6810)

CASTST is power failure proof. In the event of a power failure the program is stored and restarts from the stopping point when power is resumed, so long as the Key switch is set to LOCK.

The SOP is dedicated in the following way:

Switch	Function	Indicator	Function
0	IPL	0	Power On
1	Select drive 0 (left or lower)	1	Test step
2	Select drive 1 (right or upper)	2	
3	Start preliminary test	3	
4	Start infinity test	4	
5	Start cassette status test	5	Status (Error Type)
		6	
		7	
		8	
		9	Error code
10	Unload	10	
		11	Ready

- Load the program as directed in the SOP description.
- Select left or right recorder and depress appropriate switch (1 or 2).
- Press the appropriate switch to start the required test (3, 4 or 5).

Preliminary test (switch 3) tests all basic functions of the cassette drive in 12 steps:

1. Lock cassette drive	2. Search BOT	3. Erase
4. Write tape mark	5. Write one block	6. Write tape mark
7. Backspace	8. Search tape mark backwards	9. Read tape mark
A. Read one block	B. Search tape mark forwards	C. Search BOT

Infinity test: (switch 4) the preliminary test is run repeatedly until stopped by pressing Unload (switch 10) twice.

Status test: (switch 5) determines the status of the cassette (i.e. side A or side B) and whether write-protected

Normal indication

After a successful programrun, lamp 11 lights and the program waits for another command.

Error indication

The error indication is in two parts, the Error code, which is a 2 digit hexadecimal code, and the Status, which is a 4 digit hexadecimal code, using these two, the error can be deduced as follows:

Error Code BITS 9, 10	Status Code 5 - 8	Error
0	5	Side B, not write protected
	6	Side A, not write protected
	9	Side B, write protected
	A	Side A, write protected
1	3	Tape mark not found/written
	4	Not erased
	5	BOT not found
	6	Not write protected
	7	A-side
	F	Unlock unsuccessful
2	2	BOT missing
	3	Illegal tape mark
	4	No data
	6	Write protected
	9	Rewind time-out
	C	Incorrect length
	D	CRC error
	E	Throughput error
	F	Lock unsuccessful
3	0	Time too short
	1	Time too long

```
         DATE  82-05-05        IDENT    TESTK7    FOR PTS


0000                           IDENT    TESTK7                FOR PTS
0001                  *DATE: 820505 FOR PTS
0002                  *
0003                  *============PUT STRAP TO PROGRAMMED CHANNEL==============
0004                  *
0005                  *THIS PROGRAM TESTS THE MOST IMPORTANT CASSETTE COMMANDS
0006                  *PER BLOCK
0007                  *
0008                  * A1 COMMAND
0009                  * A7 DATA WRITE
0010                  * A3 STATUS
0011                  * A4 LENGTH (4-256 CHAR)
0012                  * A5 GEN USE
0013                  * A2 DATA READ
0014                  *
0015                  *HLT CAN BE REPLACED BY RB FOR LOOP ON COMMAND
0016                  *
0017      000E        DA        EQU      /0E
0018                            AORG     /80
0019 0080 FFFF                  DATA     /FFFF
0020 0082 0000                  DATA     0
0021 0084 207F        START     HLT
0022 0086 20BF                  INH
0023 0088 04FF                  LDK      A4,/FF               PRESET LENGTH (MAX)
0024 008A 0755                  LDK      A7,/55               PRESET DATA ('U')
0025 008C 207F                  HLT
0026                  *
0027 008E 0100                  LDK      A1,0                 SELECT DRIVE
0028 0090 41CE                  CIO      A1,1,DA
0029 0092 4BCE                  SST      A3,DA
0030 0094 5C04                  RB(4)    *-2
0031 0096 207F                  HLT
0032                  *
0033 0098 0102                  LDK      A1,2                 LOCK CASSETTE
0034 009A 41CE                  CIO      A1,1,DA
0035 009C 4BCE                  SST      A3,DA
0036 009E 5C04                  RB(4)    *-2
0037 00A0 207F                  HLT
0038                  *
0039 00A2 010B                  LDK      A1,8                 SEARCH BEGIN OF TAPE
0040 00A4 41CE                  CIO      A1,1,DA
0041 00A6 4BCE                  SST      A3,DA
0042 00A8 5C04                  RB(NZ)   *-2
0043 00AA 207F                  HLT
0044                  *
0045 00AC 010B                  LDK      A1,/B
0046 00AE 41CE                  CIO      A1,1,DA
0047 00B0 41BE                  CIO      A1,0,DA              WRITE TAPE MARK
0048 00B2 4BCE                  SST      A3,DA
0049 00B4 5C04                  RB(4)    *-2
0050 00B6 207F                  HLT
0051                  *
0052 00B8 0109                  LDK      A1,9                 ERASE FWD
0053 00BA 41CE                  CIO      A1,1,DA
0054 00BC 4BCE                  SST      A3,DA
0055 00BE 5C04                  RB(4)    *-2
0056 00C0 207F                  HLT
0057                  *
0058 00C2 8510                  LDR      A5,A4
0059 00C4 010B                  LDK      A1,/B                WRITE ONE BLOCK FWD
0060 00C6 41CE                  CIO      A1,1,DA
0061 00C8 470E                  OTR      A7,0,DA
0062 00CA 5C04                  RB(4)    *-2
0063 00CC 1D01                  SUK      A5,1
0064 00CE 5C08                  RB(4)    *-6
0065 00D0 41BE                  CIO      A1,0,DA
0066 00D2 4BCE                  SST      A3,DA
0067 00D4 5C04                  RB(4)    *-2
0068 00D6 207F                  HLT
0069                  *
0070 00D8 010E                  LDK      A1,/E                BACKSPACE
0071 00DA 41CE                  CIO      A1,1,DA
0072 00DC 4BCE                  SST      A3,DA
0073 00DE 5C04                  RB(4)    *-2
0074 00E0 207F                  HLT
0075                  *
0076 00E2 8510                  LDR      A5,A4
0077 00E4 010A                  LDK      A1,/A                READ BLOCK FWD
0078 00E6 41CE                  CIO      A1,1,DA
0079 00E8 4A0E                  INR      A2,0,DA
0080 00EA 5C04                  RB(4)    *-2
0081 00EC A220 00FF             ANKL     A2,/FF
0082 00F0 EA1C                  CWR      A2,A7
0083 00F2 5002                  RF(0)    *+4
0084 00F4 207F                  HLT                           DATA FAULT
0085 00F6 1D01                  SUK      A5,1
```

```
0086 00F8 5C12                  RB(4)     #-/10
0087 00FA 418E                  CIO       A1,0,DA
0088 00FC 4BCE                  SST       A3,DA
0089 00FE 5C04                  RB(4)     #-2
0090 0100 207F                  HLT
0091                    *
0092 0102 010D                  LDK       A1,/D                 SEARCH TAPE MARK BWD
0093 0104 41CE                  CIO       A1,1,DA
0094 0106 4BCE                  SST       A3,DA
0095 0108 5C04                  RB(4)     #-2
0096 010A 207F                  HLT
0097                    *
0098 010C 010F                  LDK       A1,/F
0099 010E 41CE                  CIO       A1,1,DA               REWIND AND UNLOCK CASSETTE
0100 0110 4BCE                  SST       A3,DA
0101 0112 5C04                  RB(4)     #-2
0102 0114 207F                  HLT
0103 0116 5F8A                  RB        START+10
0104                            END       START


          SYMBOL TABLE

   DA      000E  A   START   0084  A

          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-24S-720MS-
```

The Memcas program is for making a cassette with more short routines. The program SELPROG must be the first one on the cassette (see tape layout on next page).

When a CFP/EFP is fitted, and you IPL from this cassette the prog stops at /0086; then load A5 with the program number and push the RUN button, now the selected program will be loaded and started.

```
        DATE  82-05-05        IDENT    SELPROG   FOR PTS


0000                          IDENT    SELPROG               FOR PTS
0001                    #DATE 820505 FOR PTS
0002                    #PROG TO BE ABLE TO LOAD OTHER BLOCKS FROM CASSETTE THAN ONLY THE FIRST
0003                    *       WHEN THE PROGR STOPS PUT PROG NUMBER IN A5
0004
0005                            AORG      /80
0006 0080 FFFF 0000             DATA      /FFFF,0
0007 0084 207F          START   HLT
0008 0086 8440 0000             LD        A6,0
0009 008A EE20 44EE             CWK       A6,/44EE              IS IT THE NEW BOOTSTRAP
0010 008E 500C                  RF(0)     NBOOT
0011 0090 010C          STMK    LDK       A1,/C                 SEARCH TAPE MARK
0012 0092 F409                  CFR       A4,A2
0013 0094 1D01                  SUK       A5,1
0014 0096 5C08                  RB(4)     STMK
0015 0098 0680                  LDK       A6,/80                LOAD ADDR
0016 009A 0F42                  AB        /42                   READ BLOCK
0017 009C 8420 0500     NBOOT   LDKL      A4,/500
0018 00A0 B441 0090             XRS       A4,/90                CHANGE TO /040C
0019 00A4 B441 0092             XRS       A4,/92                CHANGE TO /F109
0020 00A8 5F1A                  RB        STMK
0021                            END       START


          SYMBOL TABLE

   NBOOT   009C  A   START   0084  A   STMK    0090  A

          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-07S-480MS-
```

```
        DATE  82-05-05        IDENT    MEMCAS    FOR PTS


0000                          IDENT    MEMCAS                FOR PTS
0001                    *DATE: 820505 FOR PTS
0002                    *PROGRAM TO PUT SMAL ROUTINES ON CASSETTE
0003                    *       A1       START ADDR OF PROG IN MEM
0004                    *       A2       LAST ADDR OF PROG IN MEM
0005                    *       A3       FIRST PROG ON CASSETTE SIDE YES PUT 0001 IN
0006
0007                          AORG     /80
0008 0080 FFFF 0000           DATA     /FFFF,0
0009 0084 207F          START HLT
0010 0086 20BF                INH
0011 0088 8604                LDR      A6,A1
0012 008A 8708                LDR      A7,A2
0013 008C 820C                LDR      A2,A3
0014 008E 80A0 00BA           LDKL     A8,SUBR
0015 0092 86A0 00DC           LDKL     A14,EOS
0016 0096 0400                LDK      A4,0                  SELECT DRIVE 0
0017 0098 F683                CFR      A14,A8                EXECUTE COMMAND
0018 009A 2301                ANK      A3,1
0019 009C 5402                RF(4)    *+4
0020 009E 207F                HLT                            NO CASSETTE IN
0021 00A0 0402                LDK      A4,2                  LOCK
0022 00A2 F683                CFR      A14,A8                EXECUTE COMMAND
0023 00A4 1A01                SUK      A2,1                  FIRST PROG ON SIDE?
0024 00A6 5408                RF(4)    NOFIR
0025 00A8 0408                LDK      A4,8                  SBOT
0026 00AA F683                CFR      A14,A8                EXECUTE COMMAND
0027 00AC 0409                LDK      A4,9                  ERASE
0028 00AE F683                CFR      A14,A8                EXECUTE COMMAND
0029 00B0 041B          NOFIR LDK      A4,/1B                WRITE TAPE MARK
0030 00B2 F683                CFR      A14,A8                EXECUTE COMMAND
0031 00B4 040B                LDK      A4,/B                 WRITE BLOCK
0032 00B6 F683                CFR      A14,A8                EXECUTE COMMAND
0033 00B8 5F36                RB       START
0034
0035 00BA 44CE          SUBR  CIO      A4,1,/0E              START
0036 00BC EC20 001B           CWK      A4,/1B                IS IT WRITE TAPEMARK?
0037 00C0 500C                RF(0)    STOP
0038 00C2 E538          OUT   LCR      A5,A6
0039 00C4 450E                QTR      A5,0,/0E              WRITE CHARACTER
0040 00C6 500A                RF(0)    UPD
0041 00C8 4BCE                SST      A3,/0E
0042 00CA 5C08                RB(4)    OUT+2
0043 00CC F03A                RTN      A14
0044 00CE 418E          STOP  CIO      A1,0,/0E
0045 00D0 5F10                RB       OUT
0046 00D2 1601          UPD   ADK      A6,1                  NEXT CHARACTER
0047 00D4 EE1C                CWR      A6,A7
0048 00D6 5C16                RB(4)    OUT
0049 00D8 5F0C                RB       STOP
0050 00DA                     RES      1
0051 00DC               EOS   RES      1
0052                          END      START


          SYMBOL TABLE

   EOS     00DC  A   NOFIR   00B0  A   OUT     00C2  A   START   0084  A
   STOP    00CE  A   SUBR    00BA  A   UPD     00D2  A

          ASS.ERR.     0000
:EOF
PROG ELAPSED TIME:  00H-00M-14S-600MS-
```

Tape layout

	TM	SELPROG	TM	Memcas	TM	Test K7	TM	etc

prog. nr. 1 prog. nr. 2 etc

16 CHANNEL UNIT FLEXIBLE DISC-0,25M

LIST OF ILLUSTRATIONS

LIST OF TABLES

16.1 CHFD-IDENTIFICATIONS

Type-Number: PTS6848

Test-Program: PERTST

Channel: PC or MX
Break-connection: 3A43

Devices: Flexible Disc-Drive CDC9404, with doorlock-PTS6867.
Stand alone Unit 2 drives FDU-PTS 6879

Power-consumption: +5 Volt, 4.7 Amp.

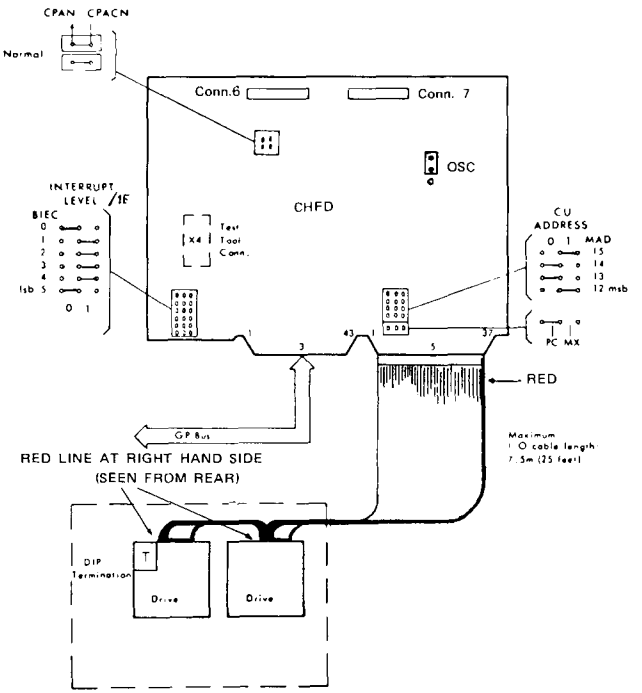


Figure 16.1a CONNECTORS, CABLES, U-LINKS (TC 6812/13)

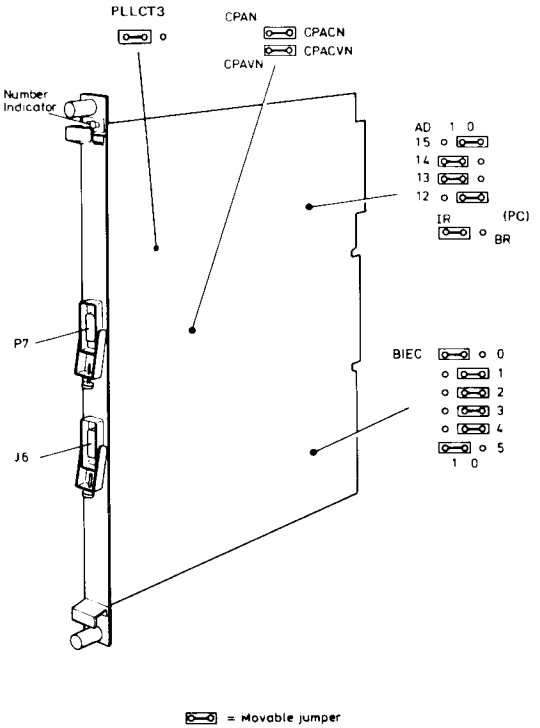
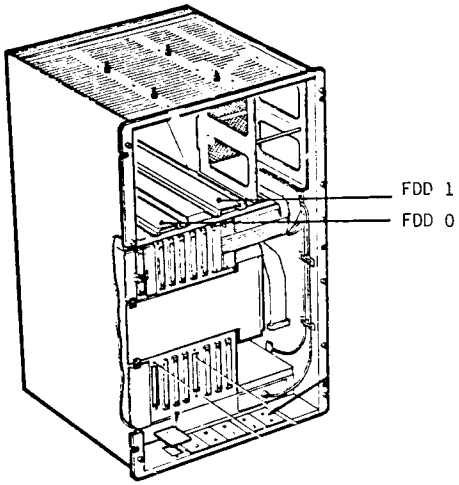
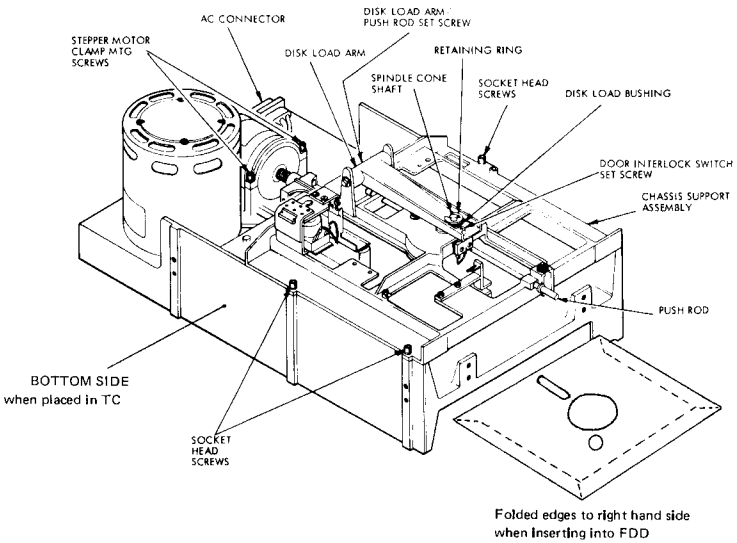
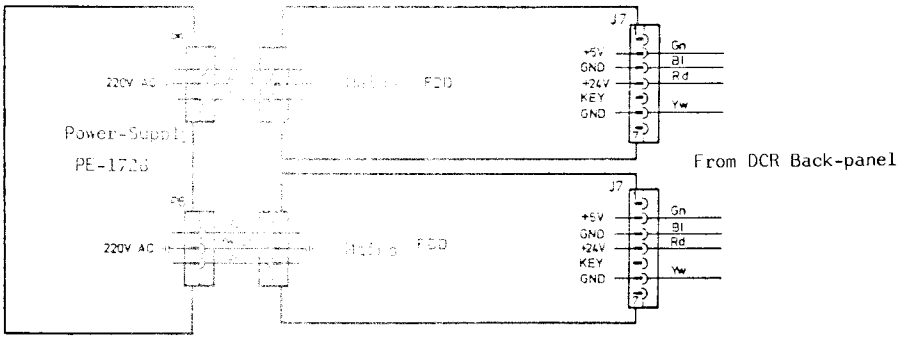


Figure 16.1b JUMPERS ON THE CHFD TC (6810)


FDD 1
FDD 0


AC CONNECTOR
DISK LOAD ARM PUSH ROD SET SCREW
STEPPER MOTOR CLAMP MTG SCREWS
DISK LOAD ARM
RETAINING RING
SPINDLE CONE SHAFT
SOCKET HEAD SCREWS
DISK LOAD BUSHING
DOOR INTERLOCK SWITCH SET SCREW
CHASSIS SUPPORT ASSEMBLY
PUSH ROD
BOTTOM SIDE when placed in TC
SOCKET HEAD SCREWS
Folded edges to right hand side when inserting into FDD



FDD

FDDs slid into their positions are fixed with the screws on top of the rack (if just one FDD is fitted it must be placed to the left). Ensure that:

- The mains cables of the FDDs are connected to P5 and P6 on the PSU (P7 is a mains outlet for the 5.25 unit).
- The flat cable is connected to the FDDs with the end socket fitted to the left unit (seen from front).

Preparing FDDs

Before FDDs are installed the following preparations must be carried out:

- Ensure that the FDDs are converted into the mains frequency being at hand, 50Hz or 60Hz.
- The 12-gang address switches (1 - 8 on each FDD) must be set as follows:

FDD No.	Location (seen from front)	Switch pos. to be 'ON'
1	Lefthand in Computer Cabinet (1st)	1-5-09
2	Righthand in Computer Cabinet (2nd)	2-6-10
3	Lefthand in Flexible Disc Unit (3rd)	3-7-11
4	Righthand in Flexible Disc Unit (4th)	4-8-12

- FDDs to be placed in lefthand positions (1st and 3rd according to the table above), must be equipped with terminating resistors. The resistors, contained in an IC package (CDC 96 454 500-8), are fitted into a holder below the address switches.

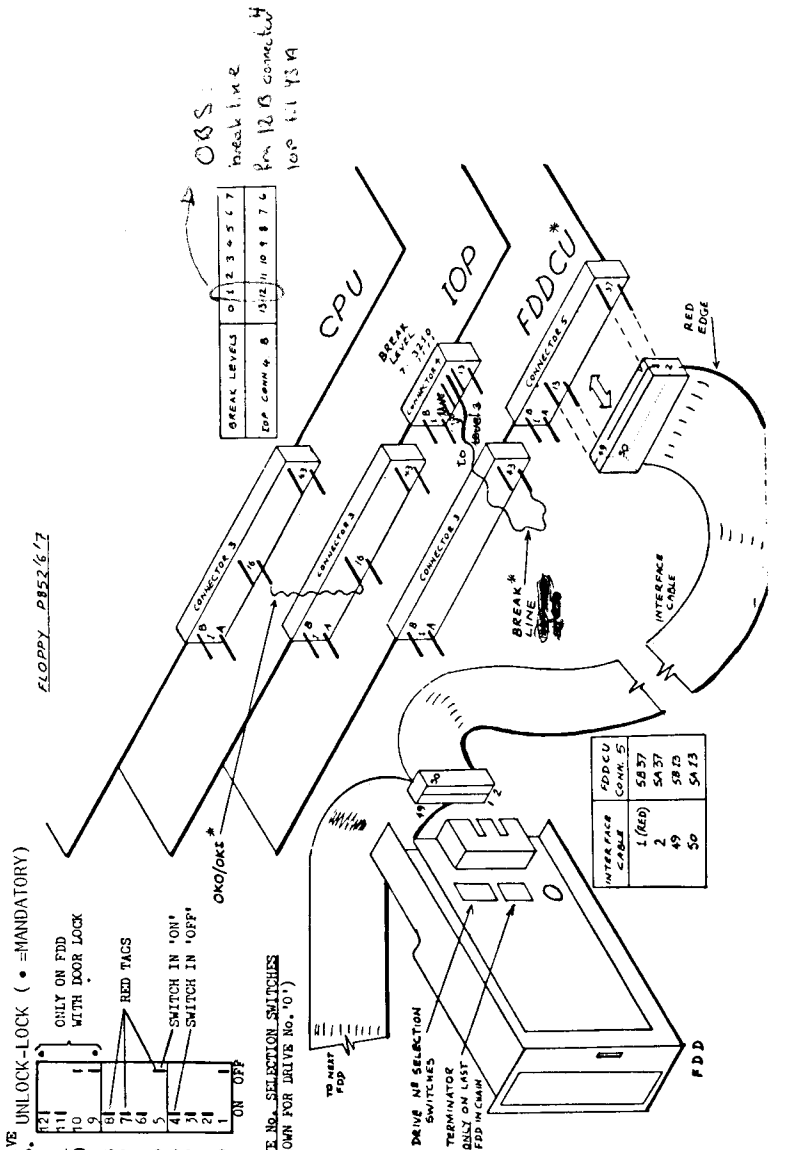


Figure 16.2 INSTALLATION DETAILS

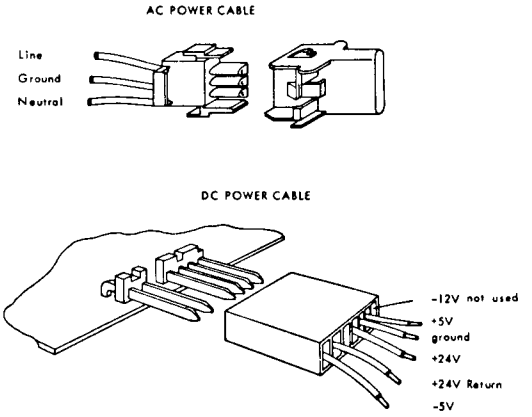


Figure 16.3 FLOPPY DISC DRIVE POWER CONNECTORS

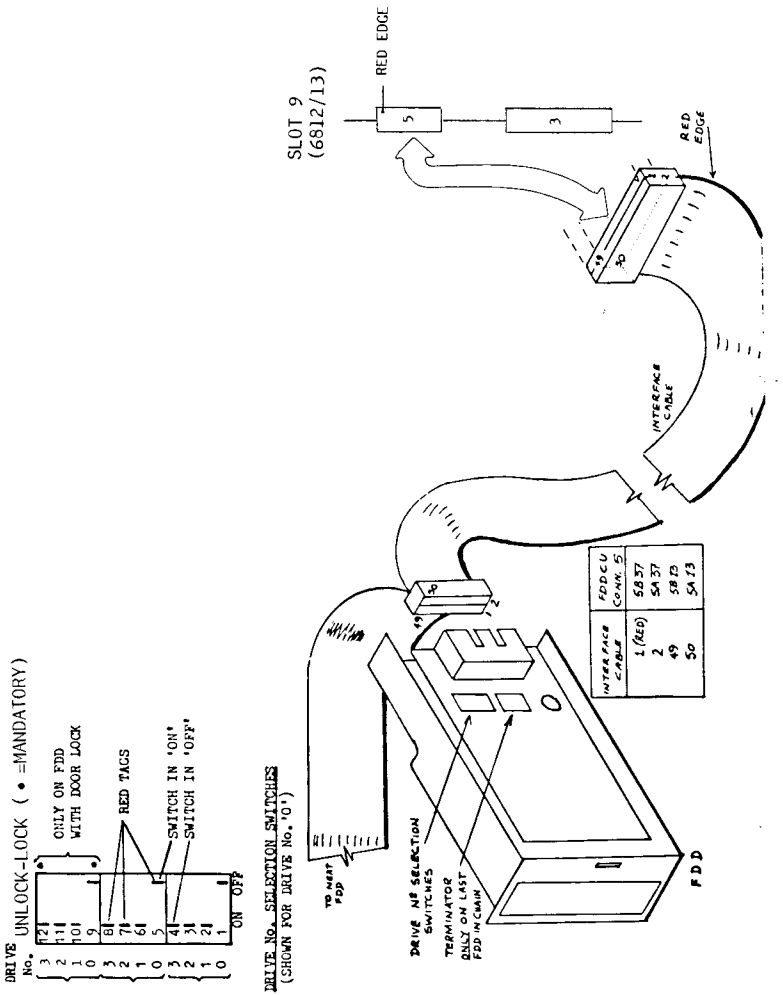


Figure 16.2 INSTALLATION DETAILS

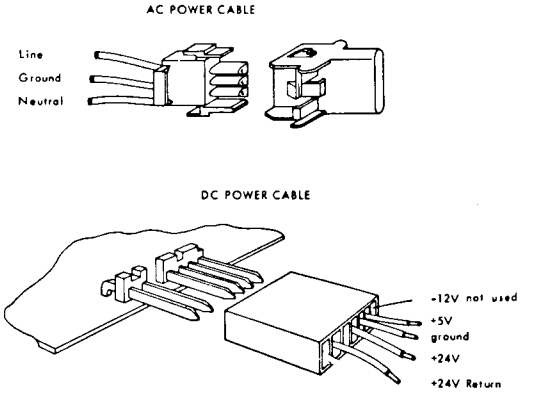


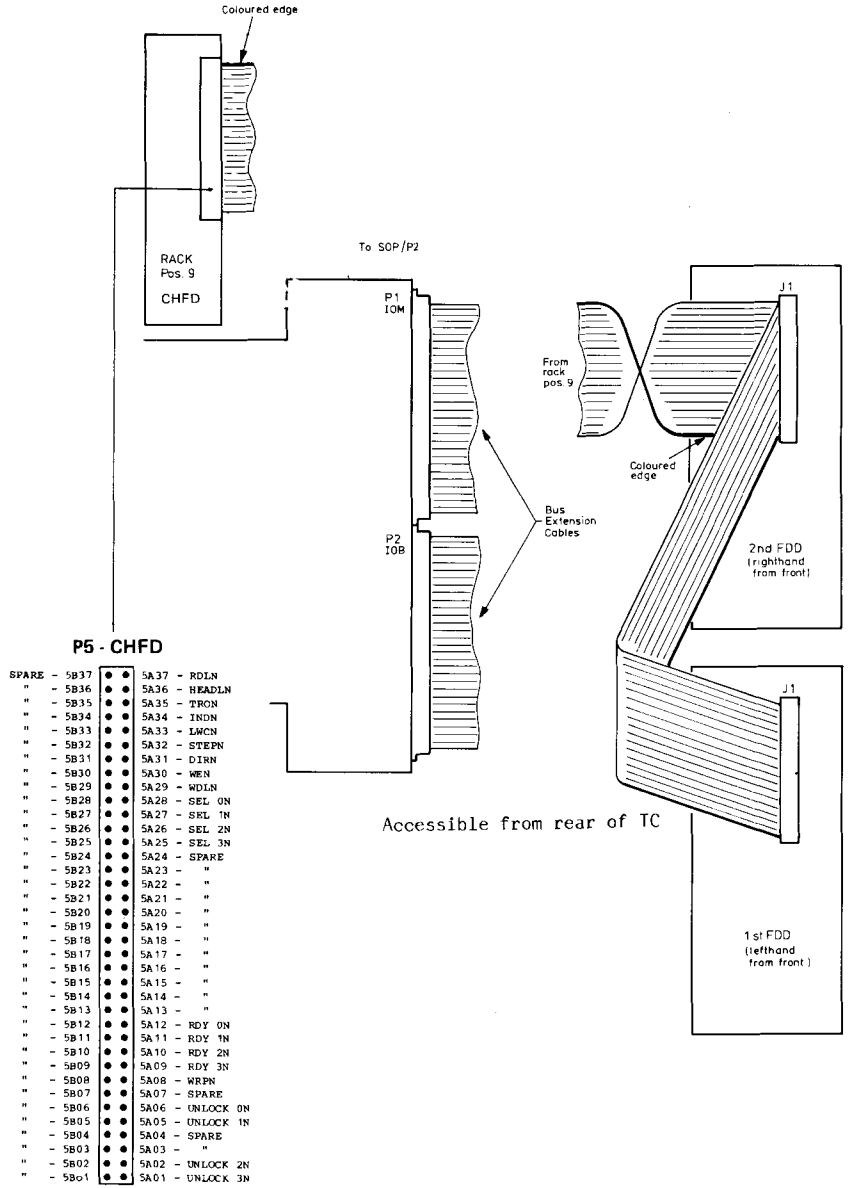
Figure 16.3 FLOPPY DISC DRIVE POWER CONNECTORS

EXTENTION (FDU 6879 DRIVE 2,3) or P6810 (FDU 6879 DRIVE 0,1)

NORMAL (DRIVE 0,1)

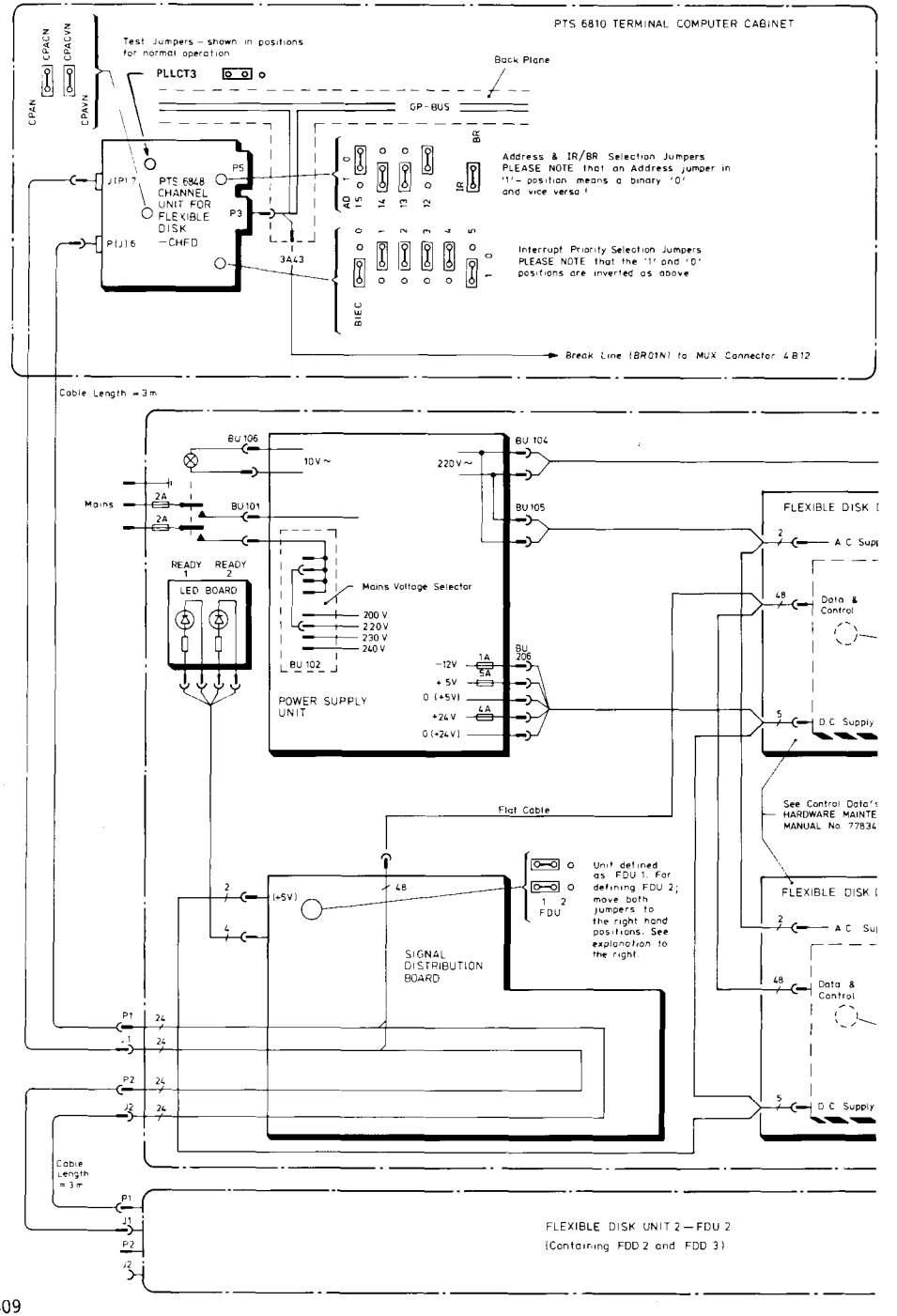
Control Unit				Disc Drive		
Logic Sheet	I/O Conn	I/O Conn	Signal Name		Drive Conn 3M	Drive Conn AMP
				ground	1	A
	7A02	5A37	←RDLN	READ DATA/CLOCK COMPOSITE	2	B
				ground	3	C
	7A03	5A36	HEADLN	HEAD LOAD →	4	D
				ground	5	E
	7A04	5A35	←TR0N	TRACK 00	6	F
				ground	7	H
	7A05	5A34	←INDN	INDEX	8	J
				ground	9	K
	7A06	5A33	LWCN	LOW WRITE CURRENT →	10	L
				ground	11	M
	7A07	5A32	STEPN	STEP →	12	N
				ground	13	P
	7A08	5A31	DIRN	DIRECTION →	14	R
				ground	15	S
	7A09	5A30	WEN	WRITE ENABLE →	16	T
				ground	17	U
	7A10	5A29	WDLN	WRITE DATA →	18	V
				ground	19	W
e	7A11	5A28	SEL0N	UNIT SELECT 1 →	20	X
				ground	21	Y
	7A12	5A27	SEL1N	UNIT SELECT 2 →	22	Z
				ground	23	AA
	7A13	5A26	SEL2N	UNIT SELECT 3 →	24	BB
				ground	25	CC
	6A02	5A25	SEL3N	UNIT SELECT 4 →	26	DD
				ground	27	EE
	6A03	5A12	←RDY0N	UNIT READY INTERRUPT 1	28	FF
				ground	29	HH
	6A04	5A11	←RDY1N	UNIT READY INTERRUPT 2	30	JJ
				ground	31	KK
	6A05	5A10	←RDY2N	UNIT READY INTERRUPT 3	32	LL
				ground	33	MM
	6A06	5A09	←RDY3N	UNIT READY INTERRUPT 4	34	NN
				ground	35	PP
	6A07	5A08	←WRPN	WRITE PROTECT	36	RR
				ground	37	SS
			NOT USED	READ DATA SEPARATED	38	TT
				ground	39	UU
	6A09	5A06	UNLOCK0N	DOOR UNLOCK 1 →	40	VV
				ground	41	WW
	6A10	5A05	UNLOCK1N	DOOR UNLOCK 2 →	42	XX
				ground	43	YY
d				WRITE FAULT	44	ZZ
			NOT USED	ground	45	AB
				WRITE FAULT RESET	46	AC
				ground	47	AD
	6A12	5A02	UNLOCK2N	DOOR UNLOCK 3 →	48	AE
				ground	49	AF
	6A13	5A01	UNLOCK3N	DOOR UNLOCK 4 →	50	AH

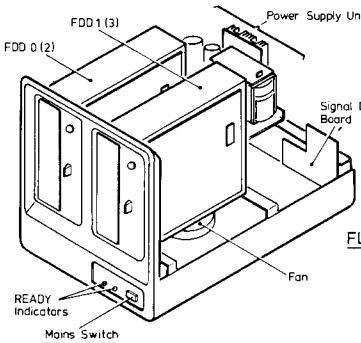
Table 16.1 CU DEVICE INTERFACE



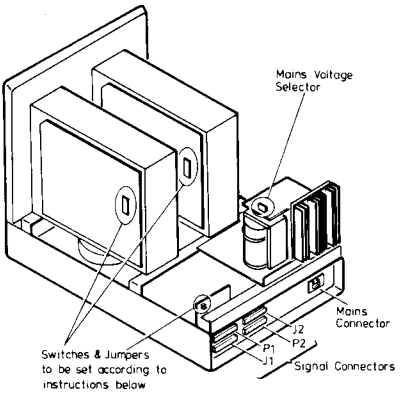
P5 - CHFD

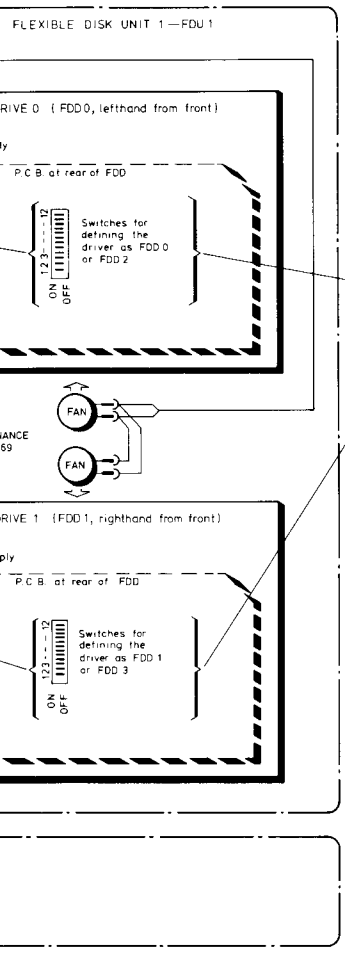
SPARE - 5B37	● ●	5A37 - RDLN
" - 5B36	● ●	5A36 - HEADLN
" - 5B35	● ●	5A35 - TRON
" - 5B34	● ●	5A34 - INDN
" - 5B33	● ●	5A33 - LWCN
" - 5B32	● ●	5A32 - STEPN
" - 5B31	● ●	5A31 - DIRN
" - 5B30	● ●	5A30 - WEN
" - 5B29	● ●	5A29 - WDLN
" - 5B28	● ●	5A28 - SEL 0N
" - 5B27	● ●	5A27 - SEL 1N
" - 5B26	● ●	5A26 - SEL 2N
" - 5B25	● ●	5A25 - SEL 3N
" - 5B24	● ●	5A24 - SPARE
" - 5B23	● ●	5A23 - "
" - 5B22	● ●	5A22 - "
" - 5B21	● ●	5A21 - "
" - 5B20	● ●	5A20 - "
" - 5B19	● ●	5A19 - "
" - 5B18	● ●	5A18 - "
" - 5B17	● ●	5A17 - "
" - 5B16	● ●	5A16 - "
" - 5B15	● ●	5A15 - "
" - 5B14	● ●	5A14 - "
" - 5B13	● ●	5A13 - "
" - 5B12	● ●	5A12 - RDY 0N
" - 5B11	● ●	5A11 - RDY 1N
" - 5B10	● ●	5A10 - RDY 2N
" - 5B09	● ●	5A09 - RDY 3N
" - 5B08	● ●	5A08 - WRPN
" - 5B07	● ●	5A07 - SPARE
" - 5B06	● ●	5A06 - UNLOCK 0N
" - 5B05	● ●	5A05 - UNLOCK 1N
" - 5B04	● ●	5A04 - SPARE
" - 5B03	● ●	5A03 - "
" - 5B02	● ●	5A02 - UNLOCK 2N
" - 5B01	● ●	5A01 - UNLOCK 3N


PTS 6810 TERMINAL COMPUTER CABINET
CPAN
CPACN
CPACVN
CPAVN
Test Jumpers – shown in positions for normal operation
PLLCT3
Back Plane
GP-BUS
J1P17
PTS 6848 CHANNEL UNIT FOR FLEXIBLE DISK – CHFD
P5
P3
P1J16
3A43
AD
BR
IR
BIEC
Address & IR/BR Selection Jumpers PLEASE NOTE that an Address jumper in '1' – position means a binary '0' and vice versa !
Interrupt Priority Selection Jumpers PLEASE NOTE that the '1' and '0' positions are inverted as above
Break Line (BR01N) to MUX Connector 4B12
Cable Length = 3m
BU 106
10V~
Mains
2A
2A
BU101
READY 1
READY 2
LED BOARD
Mains Voltage Selector
200 V
220 V
230 V
240 V
BU 102
POWER SUPPLY UNIT
BU 104
220V~
BU 105
BU 206
–12V
1A
+5V
5A
0 (+5V)
+24V
4A
0 (+24V)
FLEXIBLE DISK
A C Supp
Data & Control
D.C Supply
See Control Data's HARDWARE MAINTE MANUAL No. 77834
Flat Cable
(+5V)
SIGNAL DISTRIBUTION BOARD
Unit defined as FDU 1. For defining FDU 2; move both jumpers to the right hand positions. See explanation to the right.
1 2
FDU
P1
J1
P2
J2
24
48
Cable Length = 3m
FLEXIBLE DISK UNIT 2 – FDU 2
(Containing FDD 2 and FDD 3)



FLEXIBLE DISC UNIT





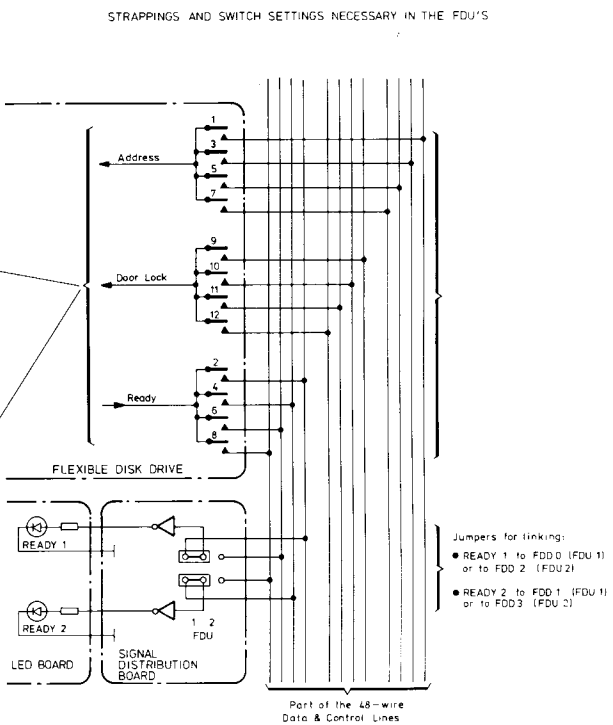


Figure 16.4 FDU 6879 INTERFACES

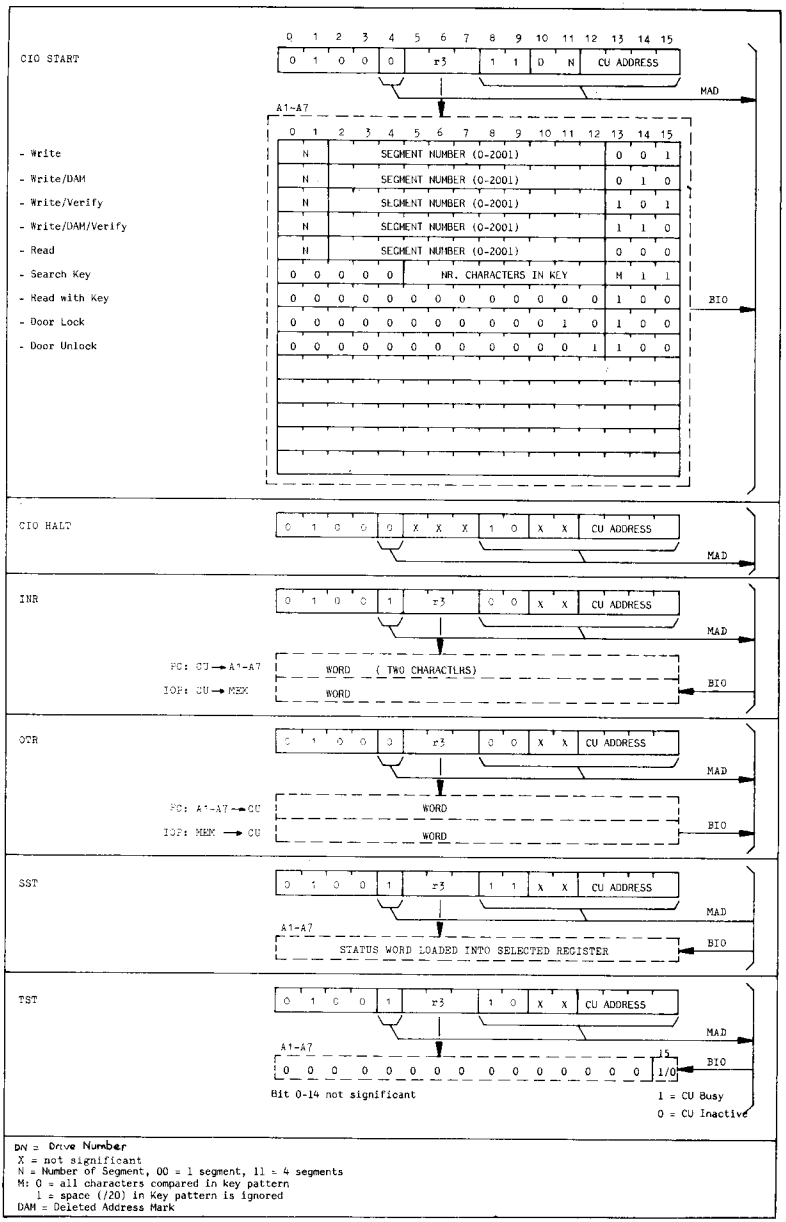


Figure 16.5 INSTRUCTION-/COMMAND-WORD FORMATS

16.4.1 STATUS-WORD

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	Possible Configurations:
	0			0				0							0		
	0	Drive Ready after Not Ready	Key Not Found	0	Deleted Data Adr. Mark	Record Not Found	Write Protect	0	Drive (msb)	(lsb)	Retry	Program Error	Incorrect Length	Data Fault	0	Drive Not Operable	
	0	0	0	0	0	0	0	0	Drive Number		Y	0	0	0	0	0	Write, Write/DAM performed correctly
	0	0	0	0	Y	0	0	0			Y	0	0	0	0	0	Read, Search Key performed correctly
	0	0	0	0	0	0	0	0			0	0	Y	0	0	0	Read Key Segment performed correctly
	0	0	0	0	0	0	0	0			0	0	0	0	0	0	Door command performed correctly
	0	0	0	0	0	x	x	0			Y	x	x	0	0	x	Write, Write/DAM incorrect
	0	0	0	0	0	x	x	0			Y	x	x	x	0	x	Write/Ver, Write/DAM/Verify incorrect
	0	0	0	0	Y	x	0	0			Y	x	x	x	0	x	Read incorrect
	0	0	x	0	Y	x	0	0			Y	x	x	x	0	x	Search Key incorrect
	0	0	0	0	0	0	0	0			0	x	x	0	0	x	Read Key Segment incorrect
	0	1	0	0	0	0	0	0			0	0	0	0	0	0	Device just became operable
	0	0	0	0	0	0	0	0			0	0	0	0	0	1	Door command not performed

Y = bit can be 1 or 0

x = at least one of these bits must be set to 1.

The status bits have the following meanings:

- 15 means command attempted on a Non-Operable Drive or the selected drive goes non-operable. (A non-selected drive going inoperable does not set CU status.) Note: a diskette inserted upside-down will cause the non-operable condition.
- 13 means Data Fault: In the Write/Verify or Write/DAM/Verify mode a CRC error has been detected during the verify reading. In the Read mode there is data-field CRC error non-recoverable with read retries (bit 10 also set). In the Search Key mode there is a non-recoverable data-field CRC error in any segment and the key is not found in any other segment (bits 2, 10 also set).
- 12 means Incorrect Length: Block length specified by channel does not correspond to number of segments to be transferred or required block length. Allowed lengths are:

  Any Write command $\leq (N+1) \times 64$ words

  Read $(N+1) \times 64$ words

  Search Key $\frac{n}{2} + 2$ words, or $\frac{n+1}{2} + 2$ words

  (n = even or odd number of characters)

  Read Key Segment 65 words
- 11 means Program Error:
  - Channel sends INR instead or OTR during any Write or Search Key, or Key command.
  - Segment number command is greater than 2001 or converts to a track number greater than 76.
  - The first segment number is greater than the second segment number for Search Key.
  - Unknown command.

Track	Sector	Segment		Hexadecimal
00	1-26	0- 25	↑	/000-/019
01	1-26	26- 51	Software	/01A-/033
02	1-26	52- 77	Limit	/034-/04D
73	1-26	1898-1923	↓	/76A-/783
74	1-26	1924-1949		/784-/79D
75	1-26	1950-1975		/79E-/7B7
76	1-26	1976-2001		/7B8-/7D1

- 10 means Retry: ID-field or data-field CRC error caused a read-retry procedure, whether or not the error was recovered.
- 9,8 mean Drive Number:

8	9	Drive
0	0	0
0	1	1
1	0	2
1	1	3

- 6 means Write Protect: Set if any Write command is attempted on a drive with a write-protected diskette loaded.
- 5 means Record Not Found:
  - Unrecoverable ID-Field CRC error during any Write command or Read command.
  - Unrecoverable ID- or data-field error and key is not found, during Search Key.
- 4 means Deleted Data Address Mark: Detected in a segment read during Read command or in the located key segment during a Search Key command.
- 2 means Key Not Found: The key segment not found within the search area of a Search Key command. There may also be a Record Not Found error.
- 1 means Drive Ready After Not Ready: Detected when the CU is in nactive state — the CU sends an interrupt request and goes to Wait Status state.

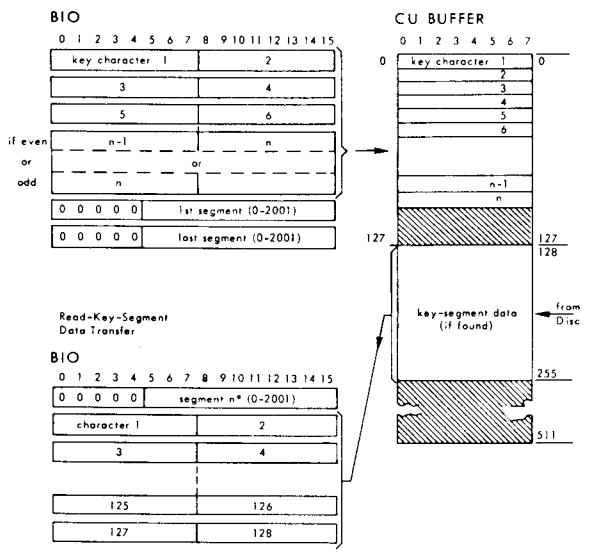


Figure 16.6 SEARCH-KEY, READ-KEY PATTERN/DATA LOADING

16.5 SHORT DESCRIPTIOON TESTPROGRAM

Pertst

Codes: 70-79

see detailed description

```
        DATE  82-05-05        IDENT    FDDWRT    ON PROGRAMMED CHANNEL


0000                          IDENT    FDDWRT              ON PROGRAMMED CHANNEL
0001                    *DATE: 820505 FOR PTS
0002                    *PROGRAM FOR WRITE OR WRITE KEY COMMANDS
0003                    *       REG. A3  COMMAND                      ***
0004                    *       REG. A1  NUMBER OF WORDS TO EXCHANGE  ***  -SEE NOTE
0005                    *       REG. A2  BUFFER ADDRESS IN MEMORY     ***
0006
0007                    *AFTER EXECUTION THE PROGRAM STOPS AT ADDR. /86
0008                    *       REG. A7  STATUS WORD
0009
0010                          AORG     /80
0011 0080 FFFF                DATA     /FFFF
0012 0082 0000                DATA     0
0013 0084 207F          START HLT                         STATUS IN A7
0014 0086 20BF                INH
0015 0088 850B                LDR      A5,A2              SAVE A2
0016 008A 8604                LDR      A6,A1              SAVE A1
0017 008C 43C9                CIO      A3,1,9             START CONTROLLER
0018 008E 5C04                RB(4)    *-2
0019 0090 8434          OUT   LDR*     A4,A5              LOAD WORD
0020 0092 4409          OTR   OTR      A4,0,9             OUTPUT WORD
0021 0094 5408                RF(4)    SST
0022 0096 1502                ADK      A5,2               UPDATE BUFFER ADDRESS
0023 0098 1E01                SUK      A6,1               DECREMENT NO OF EXCHANGES
0024 009A 5C0C                RB(4)    OUT
0025 009C 4489                CIO      A4,0,9             STOP CONTROLLER
0026 009E 4FC9          SST   SST      A7,9               GET STATUS
0027 00A0 5C10                RB(4)    OTR
0028 00A2 5F20                RB       START
0029                          END      START


          SYMBOL TABLE

  OTR     0092  A   OUT     0090  A   SST     009E  A   START   0084  A


          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-08S-920MS-
```

```
        DATE  82-05-05        IDENT    FDDRD     ON PROGRAMMED CHANNEL


0000                          IDENT    FDDRD               ON PROGRAMMED CHANNEL
0001                    *DATE: 820505 FOR PTS
0002                    *PROGRAM FOR READ OR READ KEY COMMANDS
0003                    *       REG. A3  COMMAND                      ***
0004                    *       REG. A1  NUMBER OF WORDS TO EXCHANGE  ***  - SEE NOTE
0005                    *       REG. A2  BUFFER ADDRESS IN MEMORY     ***
0006
0007                    *AFTER EXECUTION THE PROGRAM STOPS AT ADDR. /86
0008                    *       REG. A7  STATUS WORD
0009
0010                          AORG     /80
0011 0080 FFFF                DATA     /FFFF
0012 0082 0000                DATA     0
0013 0084 207F          START HLT                         STATUS IN A7
0014 0086 20BF                INH
0015 0088 850B                LDR      A5,A2              SAVE A2
0016 008A 8604                LDR      A6,A1              SAVE A1
0017 008C 43C9                CIO      A3,1,9             START CONTROLLER
0018 008E 5C04                RB(4)    *-2
0019 0090 4C09          INR   INR      A4,0,9             READ WORD
0020 0092 540A                RF(4)    SST
0021 0094 8435                STR      A4,A5              WORD TO BUFFER
0022 0096 1502                ADK      A5,2               UPDATE BUFFER ADDRESS
0023 0098 1E01                SUK      A6,1               DECREMENT NO OF EXCHANGES
0024 009A 5C0C                RB(4)    INR
0025 009C 4489                CIO      A4,0,9             STOP CONTROLLER
0026 009E 4FC9          SST   SST      A7,9               GET STATUS
0027 00A0 5C12                RB(4)    INR
0028 00A2 5F20                RB       START
0029                          END      START


          SYMBOL TABLE

   INR     0090  A   SST     009E  A   START   0084  A


          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-08S-760MS-
```

NOTE: *** See page 18. Take care that bit 0,1 in A1 are now zero.

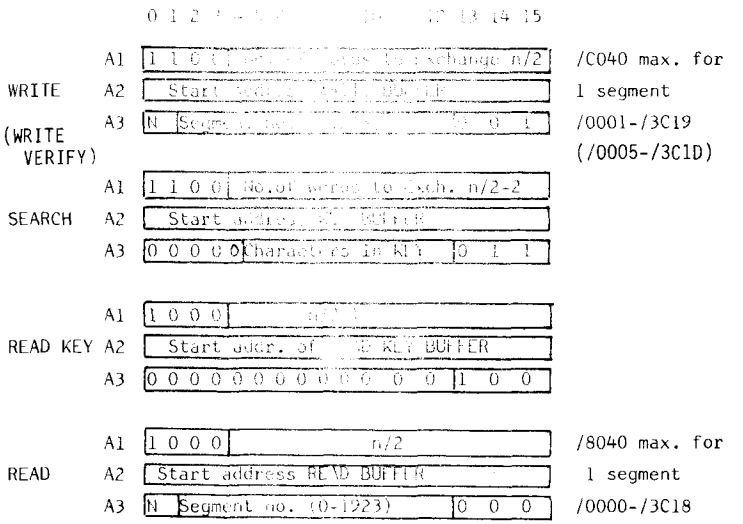
```
DATE  82-05-05        IDENT    PTSRWD          ON IOP CHANNEL

0000                    IDENT    PTSRWD                    ON IOP CHANNEL
0001                  *DATE: 820505 FOR PTS
0002                  *PROGRAM FOR WRITE AND READ COMMANDS
0003                  *        REG. A1  FIRST CONTROL WORD
0004                  *        REG. A2  SECOND CONTROL WORD (BUFFER ADDRESS)
0005                  *        REG. A3  COMMAND
0006
0007                  *AFTER EXECUTION PROGRAM STOPS AT ADDRESS /86
0008                  *        REG. A7  STATUS WORD
0009
0010                           ORG      /80
0011 0080 FFFF                 DATA     /FFFF
0012 0082 0000                 DATA     0
0013 0084 207F        START    MCI                        STATUS IN A7
0014 0086 20BF                 INH
0015                  *        PREPARE  IOP
0016 0088 7112                 MER      A1,/12            FIRST CONTROL WORD
0017 008A 7213                          A2,/13            SECOND CONTROL WORD
0018 008C 43C9                          A3,/19            START CONTROLLER
0019 008E 5C04                 RKUP     1,1
0020 0090 4FC9                 SSF      A7,9              GET STATUS
0021 0092 5C04                 REGA     1,1
0022 0094 5F12                 RB       START
0023                           END      START

          SYMBOL TABLE

  START   0084  A

          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-07S-450MS
```



Number of Segments:	Number of Characters:
N = 00	n = 128
01	256
10	384
11	512

```
0000                            IDENT   FLTST                   ON PTS
0001                    *DATE: 820505 FOR PTS
0002                    *        READ-WRITE TEST OF DISCETTE
0003                    *       PROGRAM PRESET:
0004                    *               FOR DRIVE 0 , DA /09
0005                    *               START SEGMENT NUMBER 0
0006                    *               WRITTEN DATA /30 (ASCII FOR '0')
0007                    *
0008                    *       PROGRAM STOP AT /BC:
0009                    *               WRITTEN DATA CAN BE CHANGED IN A2
0010                    *               START SEGMENT NUMBER CAN BE CHANGED IN A5
0011                    *               AFTER EXECUTION DISCETTE IS CORRECT
0012                    *
0013                    *       ERROR STOP ON /E2:
0014                    *               STATUS IN A6
0015                    *               SEGMENT NUMBER IN A5
0016                    *
0017                    *
0018                    *               A5 BIT CONFIGURATION
0019                                                    0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
0020                                                    * *(     SEGMENT NUMBER     )*  *  *
0021                            ADRG    /80
0022 0080 FFFF                  DATA    /FFFF
0023 0082 0000                  DATA    0
0024 0084 8220 3030     START   LDKL    A2,/3030                PRESET CHARACTER 0
0025 0088 0500                  LDK     A5,0                    PRESET SEGMENT 0
0026 008A 207F          BEGIN   HLT
0027 008C 20BF                  INH
0028 008E 0100                  LDK     A1,0                    RESET INDEX FOR BUFFER
0029 0090 8245 00EC             ST      A2,BUF,A1               FILL THE WRITE BUFFER
0030 0094 1102                  ADK     A1,2
0031 0096 E920 0200             CWK     A1,/200
0032 009A 5D0C                  RB(5)   *-/A
0033 009C 0100                  LDK     A1,0                    RESET EXECUTE POINTER
0034 009E 8720 FC1D             LDKL    A7,/FC1D                END SEGMENT
0035 00A2 9520 C005             ADKL    A5,/C005                SELECT WRITE VERIFY WITH 4 SEGMENTS
0036                    *       PREPARE THE IOP
0037 00A6 8320 C100     RET     LDKL    A3,/C100
0038 00AA 8420 C040             LDKL    A4,/C040                FOR 1 SEGMENT MODE
0039 00AE F045 00E4             EX      WER,A1                  EXECUTE WER A3 OR WER A4.
0040 00B2 8420 00EC             LDKL    A4,BUF
0041 00B6 7413                  WER     A4,/13
0042 00B8 45C9                  CIO     A5,1,9                  START CONTROLLER
0043 00BA 5C04                  RB(4)   *-2
0044 00BC 4EC9                  SST     A6,9                    GET STATUS
0045 00BE 5C04                  RB(4)   *-2
0046                    *       CHECK STATUS
0047 00C0 A620 641D             ANKL    A6,/641D
0048 00C4 5010                  RF(0)   CONT                    STATUS OKE
0049 00C6 8104                  LDR     A1,A1                   CHECK  4 SEGMENT OR 1 SEGMENT
0050 00C8 5116                  RF(1)   STOP
0051                    *       STATUS IS WRONG CHANGE TO WRITE VERIFY SEGMENT BY SEGMENT
0052 00CA 9D20 C000             SUKL    A5,/C000
0053 00CE 1102                  ADK     A1,2                    UPDATE EXECUTE POINTER FOR 1 SEGMENT MOD
0054 00D0 B720 C000             XRKL    A7,/C000                CHANGE    TO 1 SEGMENT MODE
0055 00D4 5F30                  RB      RET                     DO THE LAST SEGM. AGAIN IN 1 SEGMENTMODE
0056 00D6 F045 00E8     CONT    EX      UPDSEG,A1               NEXT SEGMENTS TO DO
0057 00DA ED1C                  CWR     A5,A7                   IS IT THE LAST ONE
0058 00DC 5D38                  RB(5)   RET                     NO
0059 00DE 5F58                  RB      BEGIN-2                 YES
0060 00E0 207F          STOP    HLT                             STATUS ERROR
0061 00E2 5F5C                  RB      BEGIN-2                 RESTART
0062 00E4 7312          WER     WER     A3,/12
0063 00E6 7412                  WER     A4,/12
0064 00E8 1520          UPDSEG  ADK     A5,/20
0065 00EA 1508                  ADK     A5,8
0066 00EC               BUF     RES     /100
0067                            END     START


          SYMBOL TABLE

  BEGIN   008A  A   BUF     00EC  A   CONT    00D6  A   RET     00A6  A
  START   0084  A   STOP    00E0  A   UPDSEG  00E8  A   WER     00E4  A


          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-16S-760MS-
```

```
0000                            IDENT    FLIPLS
0001                    *DATE: 820505 FOR PTS
0002                    * FLIPLS IS A PROGRAM THAT ENABLES TO LOAD 99
0003                    *PROGRAMS FROM 0.25M FLEXIBLE DISC
0004                    *WITHOUT EXTENDED OR FULL CONTROLPANEL (EFP/CFP)
0005
0006                    *THE PROGRAMS AS WELL FLIPLS CAN BE WRITTEN ON FLOPPY BY
0007                    *THE PROGRAMS :FDDWRT OR FDDRWD
0008
0009                    *IN THE PROGRAMS TO BELOADED WITHOUT EFP/CFP HLT INSTR IS NOT ALLOWED
0010                    *THE PROG FLIPLS SHOULD BE WRITTEN ON FLOPPY IN SEGMENT 4
0011                    *OTHER PROGRAMS MAY NOT BE LONGER THEN 4 SEGMENTS(=512 BYTES)
0012                    * PROG 1 WRITTEN IN SEGMENT 8 TO 11
0013                    *PROG 2                    12 TO 15
0014                    *PROG 3                    16 TO 19 AND SO ON
0015                    *WRITE ON THE LABEL WHAT PROGRAMS ARE ON AND WHAT IS
0016                    *THE FIRST FREE SEGMENT IN CASE YOU WANT TO ADD PROGRAMS
0017
0018                    *NOW THE PROGRAM FLIPLS :
0019                            AORG    /80
0020 0080 FFFF 0000             DATA    /FFFF,0
0021 0084 20BF                  INH                             NO INTERRUPTS
0022 0086 8720 0780             LDKL    A7,/0780                FOR LIGHTING THE SOP LAMPS
0023 008A 472E                  OTR     A7,0,/2E
0024 008C 41EE                  CIO     A1,1,/2E                START SOP
0025 008E 4B2E                  INR     A3,0,/2E                READ 1E SOP SWITCH
0026 0090 5C04                  RB(NA)  *-2                             ,
0027 0092 4D2E                  INR     A5,0,/2E                READ SECOND SOP SWITCH
0028 0094 5C04                  RB(NA)  *-2
0029                    *TRANSLATE FIRST SOP SWITCH VALUE RESULT IN A4
0030 0096 3B46                  SLL     A3,6
0031 0098 3B62                  SRL     A3,2
0032 009A 3B90                  SLN     A3,A4
0033                    *IF A4 IS /A THEN SOP SW 10 IS DEPRESSED AND A4 IS MADE 0
0034 009C EC20 000A             CWK     A4,/A
0035 00A0 5402                  RF(NE)  *+4
0036 00A2 0400                  LDK     A4,0
0037                    *TRANSLATE SECOND SOP SWITCH RESULT IN A6
0038 00A4 3D46                  SLL     A5,6
0039 00A6 3D62                  SRL     A5,2
0040 00A8 3D98                  SLN     A5,A6
0041                    *IF NOW A6 IS /A THEN ALSO MAKE A6 0
0042 00AA EE20 000A             CWK     A6,/A
0043 00AE 5402                  RF(NE)  *+4
0044 00B0 0600                  LDK     A6,0
0045                    *TRANSLATE THE DECIMAL NUMBER INTO HEXADECIMAL
0046 00B2 B410                  LDR     A4,A4                   CHECK IF FIRST WAS 0
0047 00B4 500C                  RF(0)   CONT
0048                    *CONVERT THE FIRST VALUE
0049 00B6 030A                  LDK     A3,/A
0050 00B8 0700                  LDK     A7,0
0051 00BA 970C                  ADR     A7,A3
0052 00BC 1C01                  SUK     A4,1
0053 00BE 5C06                  RB(4)   *-4
0054 00C0 841C                  LDR     A4,A7                   LOAD RESULT IN A4
0055 00C2 9418          CONT    ADR     A4,A6                   ADD THE FIRST AND THE SECOND VALUE
0056                    *CALCULATE THE SEGMENT NUMBER AND PREPARE FOR READING
0057 00C4 1401                  ADK     A4,1
0058 00C6 3C45                  SLL     A4,5
0059 00C8 9420 C000             ADKL    A4,/C000                4 SEGMENTS
0060 00CC 0680                  LDK     A6,/80                  BASE ADDRESS
0061 00CE 0F50                  AB      /50                     GOTO BOOTSTRAP TO LOAD PROGRAM
0062
0063
0064
0065                    *OPERATING:
0066                    *IPL FROM FLOPPY NORMALLY
0067                    * IF YOU WANT PROGRAM NUMBER 3 TO BE LOADED THEN DEPRESS
0068                    *AFTER LAMPS 1 UNTIL 4 ARE LIT*
0069                    *FIRST SW 10 (=0)AND THEN SOP SW3(=3)
0070                    *NOW THE SELECTED PROGRAM WIL BE LOADED
0071
0072                            END

          SYMBOL TABLE

   CONT    00C2  A

          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-00S-000MS-
```

PROGRAMS LOADED WITH FLIPLS
ARE STORED AT ADDRESS /80 AND ONWARDS
BUT STARTED FROM ADDRESS /84

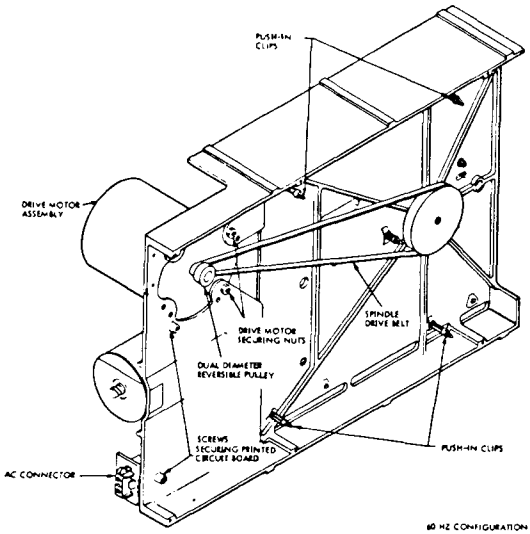


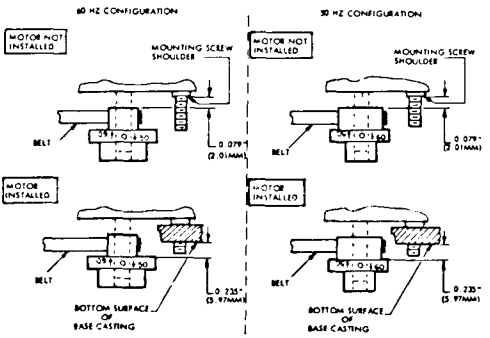
Figure A

Figure B

OPERATING FREQUENCIES CONVERSION PROCEDURE

This procedure should be used to convert the FDD unit from 50Hz operation to 60Hz operation or vice versa. This is accomplished by reversing the dual diameter reversible pulley on the spindle motor shaft using the following steps:

- Remove AC power
- Disconnect I/O cable from J1 on the printed circuit board
- Disconnect harnesses from J2, J3, J4, J5 and J6 on the board
- Remove two screws from board adjacent to connector J1 (Figure A)
- Remove board by detaching it from the four push-in clips shown in Figure A
- Remove the belt from the spindle motor pulley (accessible from the under side of unit)
- Loosen set-screw and remove pulley
- Reverse pulley and replace on motor shaft
- Position pulley allowing tolerance of 0.079" (2.01 mm) ± 0.010" (0.254 mm) between shoulder of motor mounting screws and pulley (Figure B)
- Tighten down set-screw
- Replace belt and printed circuit board



NOTE

IT IS IMPORTANT THAT THE NEW OPERATING FREQUENCY IS MARKED ON THE UNITS RATING NAMEPLATE!

Figure 16.7 FDD FREQUENCY CONVERSION INSTRUCTIONS

LIST OF ILLUSTRATIONS

LIST OF TABLES

17.1 FLEXIBLE DISC CONTROL UNIT (F1MB) - IDENTIFICATIONS

Type Number : P6849 -001, -002, -501 (F1MB)
Testprogram : TF1MZ (Floppy/CU test)
Channel : IOP/MIOP only. Break connection :3A43
Devices : Flexible Disc Drive CDC 9404 with or without doorlock option.
CDC 9406 with doorlock option (max. 2).
CDC 9406 without doorlock option (max. 4)
Philips X-3114 (max. 2) in FDU 6532

Board Identifications:

P-6849-001: F1MB with added PCB: 12NC: 5131 194 25700
F1MB without added PCB, 12NC: 5111 199 67420
P-6849-002: F1MBY, 12NC: 5111 199 58740
P-6849-501: F1MBØ6, without added PCB, 12NC: 5111 199 53720
F1MBØ6, with added PCB, 12NC: 5131 194 90600

Power Consumption: +5 Volt, 3 Amp.

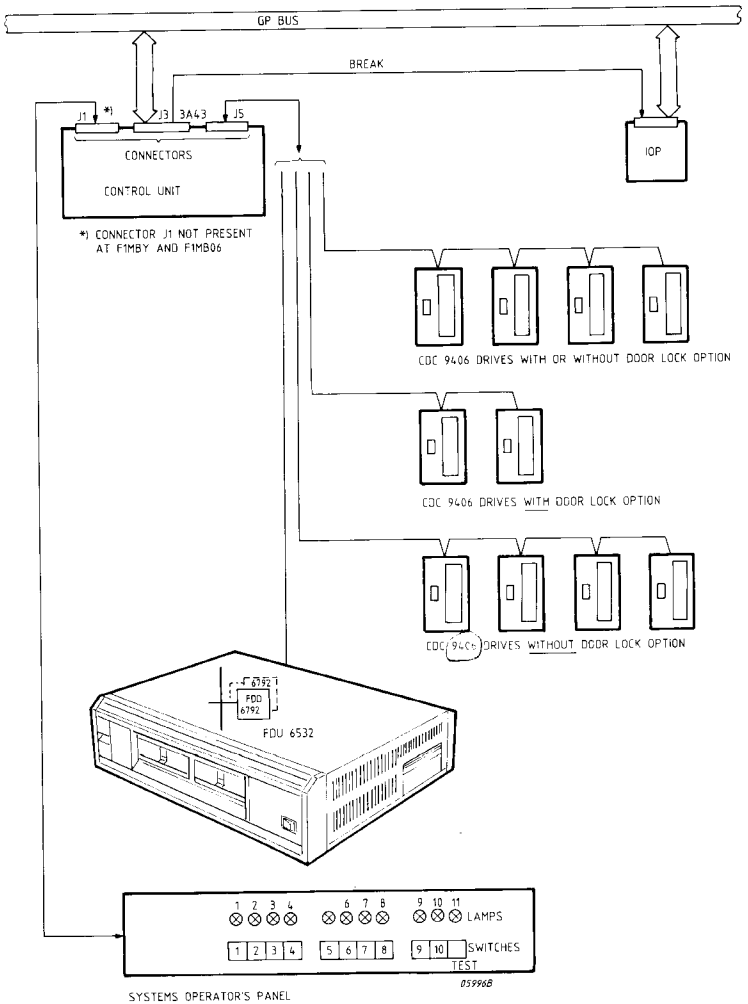


Figure 17.1 POSITION OF F1MB IN SYSTEM

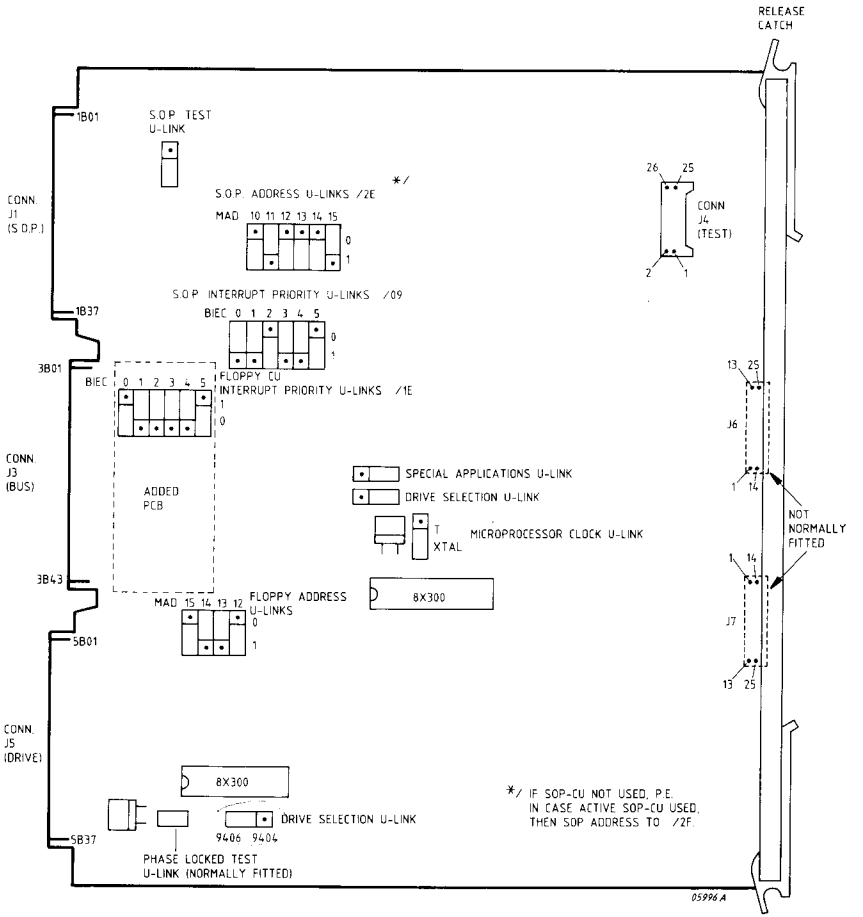


Figure 17.2 LAYOUT OF F1MB CARD WITH ADDED PCB

Note: SOP Test U-link: In position for normal operation.
SOP address U-links: Strapped for SOP address /2E. If SOP CU at this PCB is not used, the SOP address must be strapped to /2F.
SOP Interrupt Priority U-links: Strapped for interrupt level /09.
Floppy CU Interrupt Priority U-links (At added pcb): Strapped to interrupt level /1E.

Floppy Address U-links: Strapped to CU address /09.
Special Applications U-link:In position for normal operation.
Drive Selection U-links (2 links): Strapped for use with type 9406 (1M) drive (s).
Micro Processor Clock U-link: Strapped for normal operation.
Phase Locked Loop Test U-link: Must be fitted.

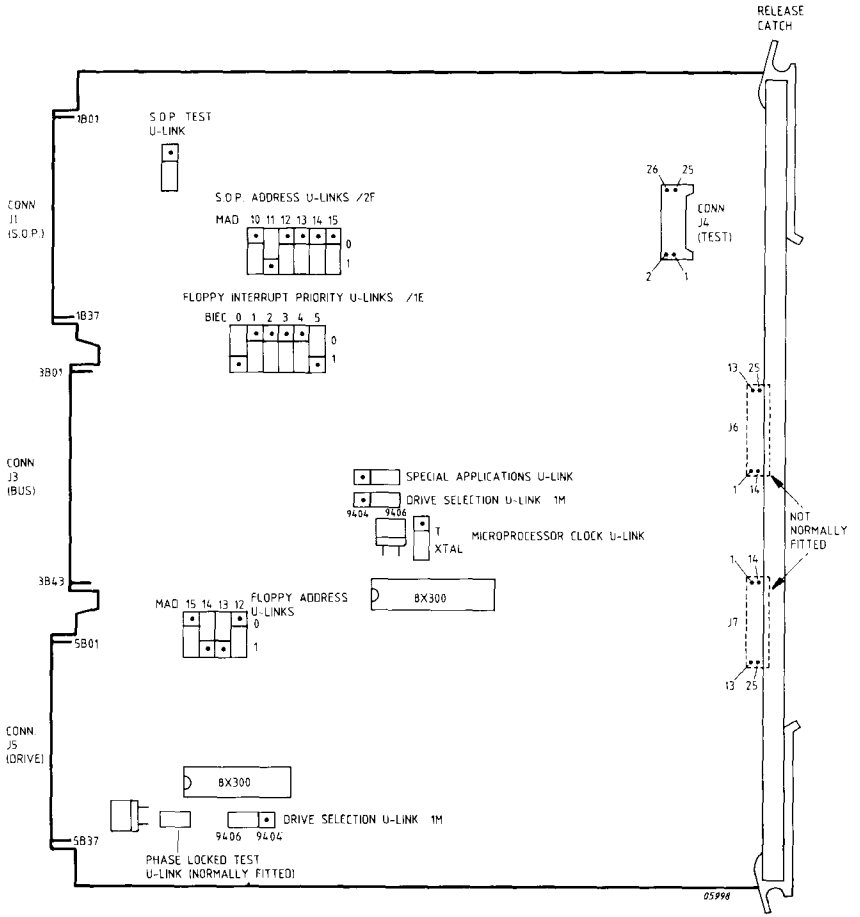


Figure 17.3 LAYOUT OF F1MB CARD WITHOUT ADDED PCB

Note: SOP Test U-link: Shown in position for normal use.
SOP address U-links: SOP CU at this PCB not used: SOP address to /2F (not used CU address).
Floppy Interrupt Priority U-links: Strapped for interrupt level /1E.
Floppy Address U-links: Strapped for address /09.
Special Applications U-link: Strapped for normal operation.
Drive Selection U-links (2 links): Strapped for operation with type 9406 (1M) drives(s).
Micro Processor Clock U-link: Strapped for normal operation.
Phase Locked Loop Test U-link: Must be fitted.

17.2.1 CONNECTION OF FDU 6532 TO P-6824.

INTRODUCTION:

The Flexible Disc Unit FDU 6532 is unintelligent and contains one or two 5.25 inch flexible disc drives. The FDU 6532 is designed primarly as an aid to copy programs used in PTS-6000 systems from 8 inch to the 5.25 inch discs used by WSC 6910 controllers.
The flexible disk drives used in the FDU are of the type FDD 6792 (X-3114) with a maximum capacity of 1MByte each.
See for detailed description of FDU 6532 Field Support Manual Flexible Disc Unit PTS-6532, 12NC: 5122 991 33921, d.d. May 1984.

CONNECTION TO TC 6824.

- Disconnect the TC Mains cable.
- Install Channel Unit 6849-501. Slot 9 is recommended.
- Install the connector adaptor to the J5 connector of the channel unit and secure it with the two screws included in the installation kit.

- Remove one of the cover plates from the cable entries at the lower front end of the TC and pass the FDU cable through the opening until the cable fastener is through.
- Remove the nut from the cable fastener. Place provided cover plate on the fastener as shown in the figure and secure it with the nut.
- Fasten the cover plate of the FDU cable at the cable entry.
- Connect the FDU cable to the connector adaptor.
- Install a break wire as indicated in the figure.
- Connect the TC mains cable and test the installation.
- Replace all covers and close the front door.

The Connector Adaptor (12NC: 5131 194 79900) and other mounting parts are in the TC Installation Kit (12NC: 5131 195 17200).

INITIAL PROGRAM LOADING

The IPL can be loaded from floppy disc using the standard P800 bootstrap (P843-053) sequential and disc bootstrap. The control panel data switches must be positioned as follows:

0	1	2	3	4 5 6 7	8	9	10 11	12 13 14 15
0	1	1	0	Sector No. (0-15)	1	1	Drive No.	CU Address

With this bootstrap the IPL is loaded from cylinder 0, head 0. This track is always formatted with format 0 (single density, 26 sectors/track and 128 bytes/sector).

Note: This IPL procedure is not applicable to the SOP. Via SOP, IPL is possible from drive 0 (switch 7) or drive 1 (switch 8).

POWER FAILURE AUTOMATIC RESTART

The CU and disc drive will be restarted after a power failure without operator action. Information on the disc will not be destroyed but a sector of the disc being written when a power failure occurs must be completely rewritten after the CU is restarted.

DRIVE CONTROL

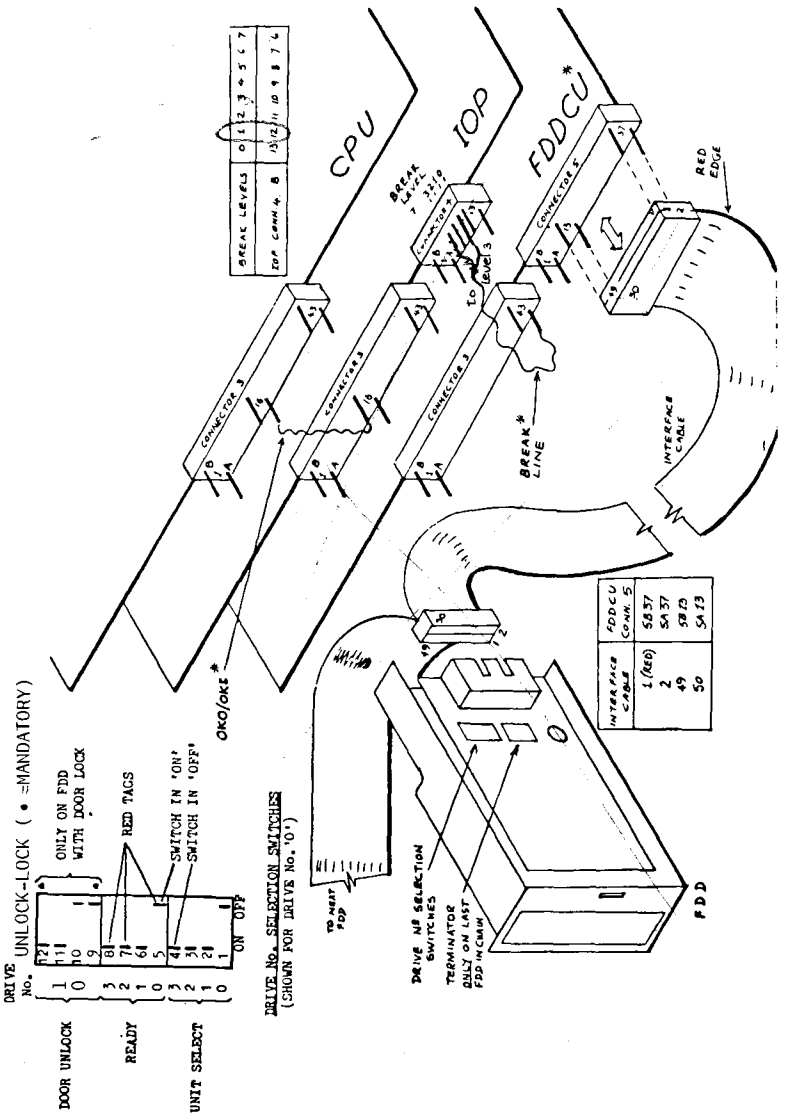
Up to four drives may be controlled from a single CU but the drives must all be of the same type. The drives cannot operate simultaneously, a command for one drive must be finished before the CU will accept a command for another drive.

STRAP SETTINGS (refer to figure 17.2)

U-Links on the card are used to select

- Floppy CU address
- SOP interface address
- Interrupt Priority for both Floppy CU and SOP interface.(see note)
- Drive type selection
- Special Applications
  These U-links are set at system installation time. Three other U-links are provided for test purposes.
- Phase locked loop test link for testing the floppy disc controller chip fitted during normal operation of the card, removed for test.
- Microprocessor clock input selection, set at position XAL for normal operation of the card, set at 'T' for test.
- SOP test U-link, shown in figure 17.3 in its position for normal operation, set at the lower position for test.

Note: Floppy disc interrupt priority U-links are on a separate small printed-circuit board. (near connector J3).
When this board is not mounted, the U-links of the SOP-interrupt priority are used for selection of Floppy interrupt priority.



Note: P6814/24: OKO/OKI and BREAK connected to MIOP (channel 1).

Figure 17.3 INSTALLATION DETAILS

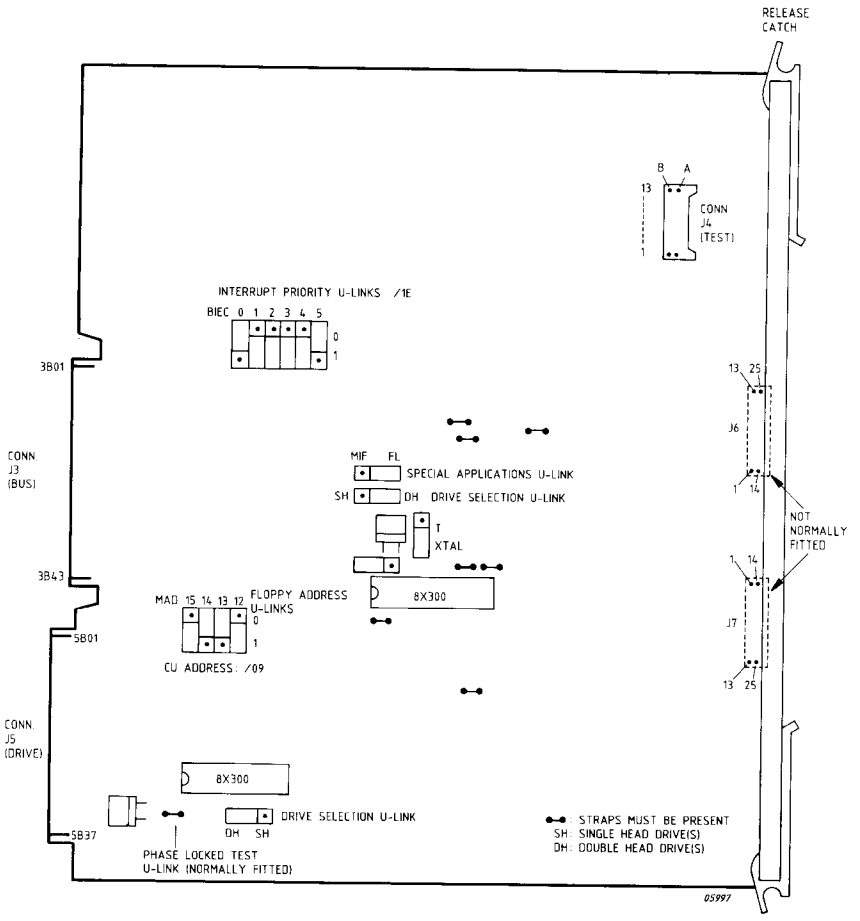


Figure 17.4 LAYOUT OF F1MBY CARD

Note: Interrupt priority U-links: Interrupt level /1E.
Control Unit Address U-links: Address /09.
Special Applications U-link: Normal operation: FL.
Drive Selection U-links (2 links): Shown for use with type 9406 drive(s).
Micro Processor Clock U-links (2 links): In position normal operation.
Seven small U-links must be present.

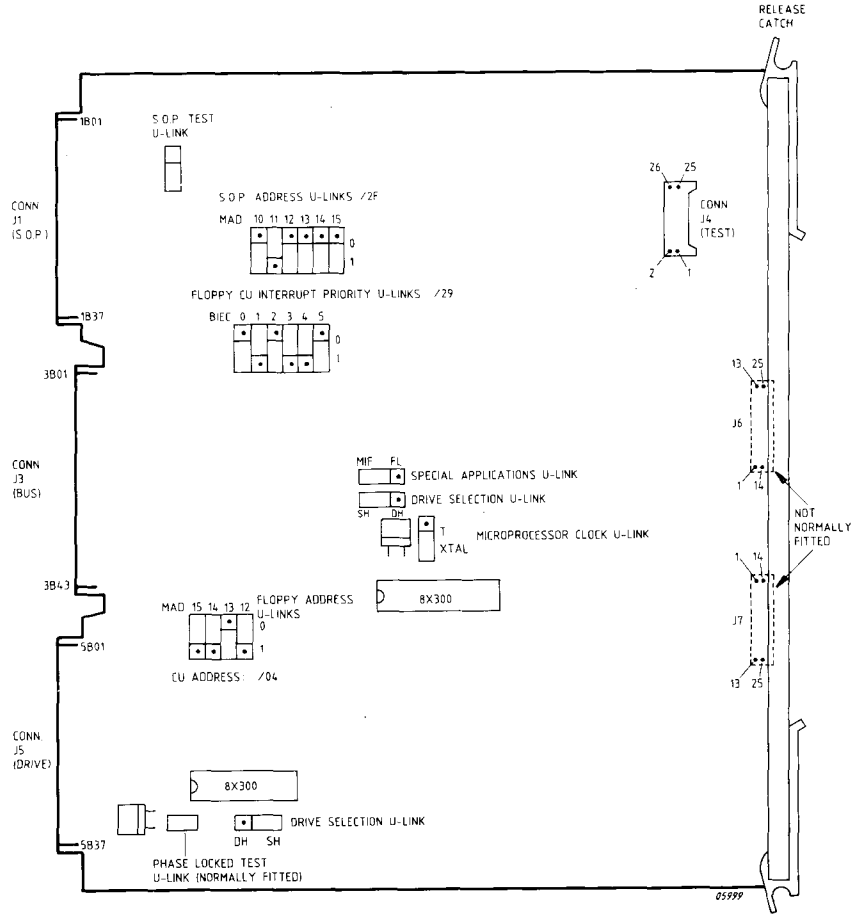
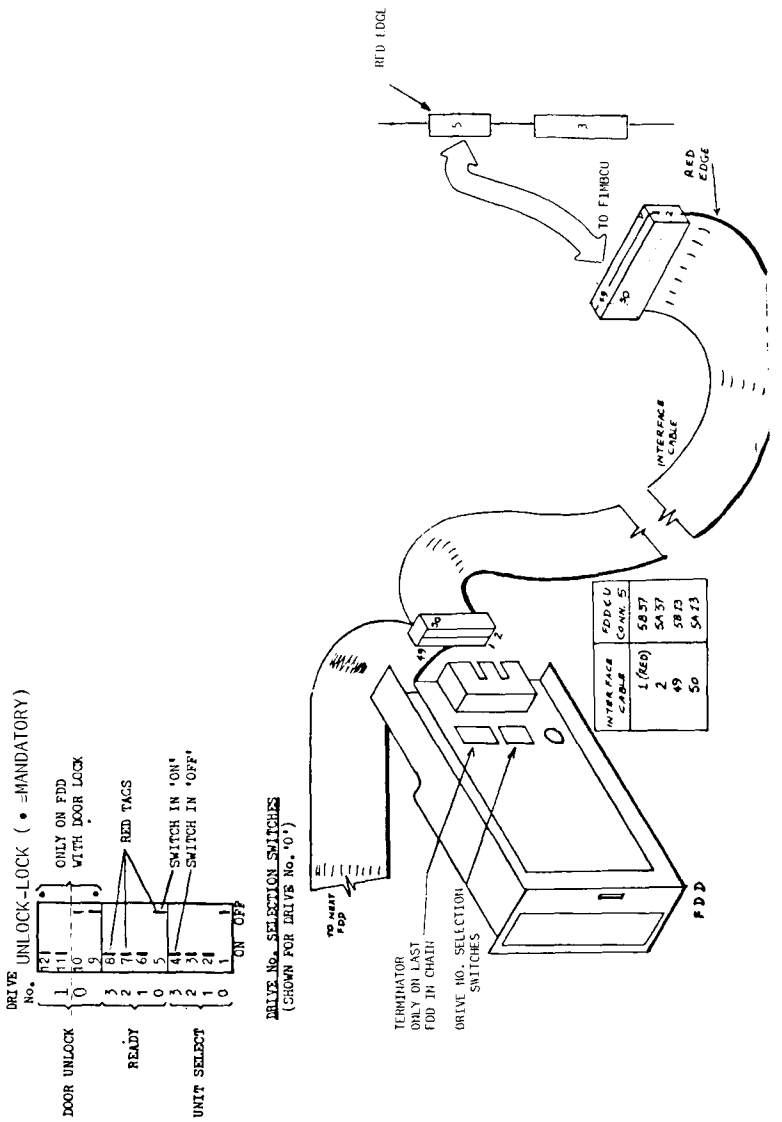


Figure 17.5 LAYOUT OF F1MBØ6 CARD

Note: This board is used with FDU 6532 (X-3114 drives) to 'translate' files at 0.25M and/or 1M, 8 inch discettes to 5.25 inch, P-6911 format discettes.
See next pages for connection FDU 6532.
SOP Test U-link : Strapped for normal operation.
SOP address U-links: Strapped to /2F: Not used CU address.
Floppy CU Interrupt Priority U-links: Strapped to level /29 (dec. 41)
Special Application U-link: Strap position not important.
Drive Selection U-links (2 times): Strapped for use with FDU 6532.
Micro Processor Clock U-link: Strapped for normal operation. (XAL)
Floppy CU Address U-links: Strapped for address /04.
Phase Locked Loop U-link: Must be fitted for normal operation.



Note: P6814/24: OKO/OKI and BREAK connected to MIOP (channel 1).

Figure 17.6 INSTALLATION DETAILS

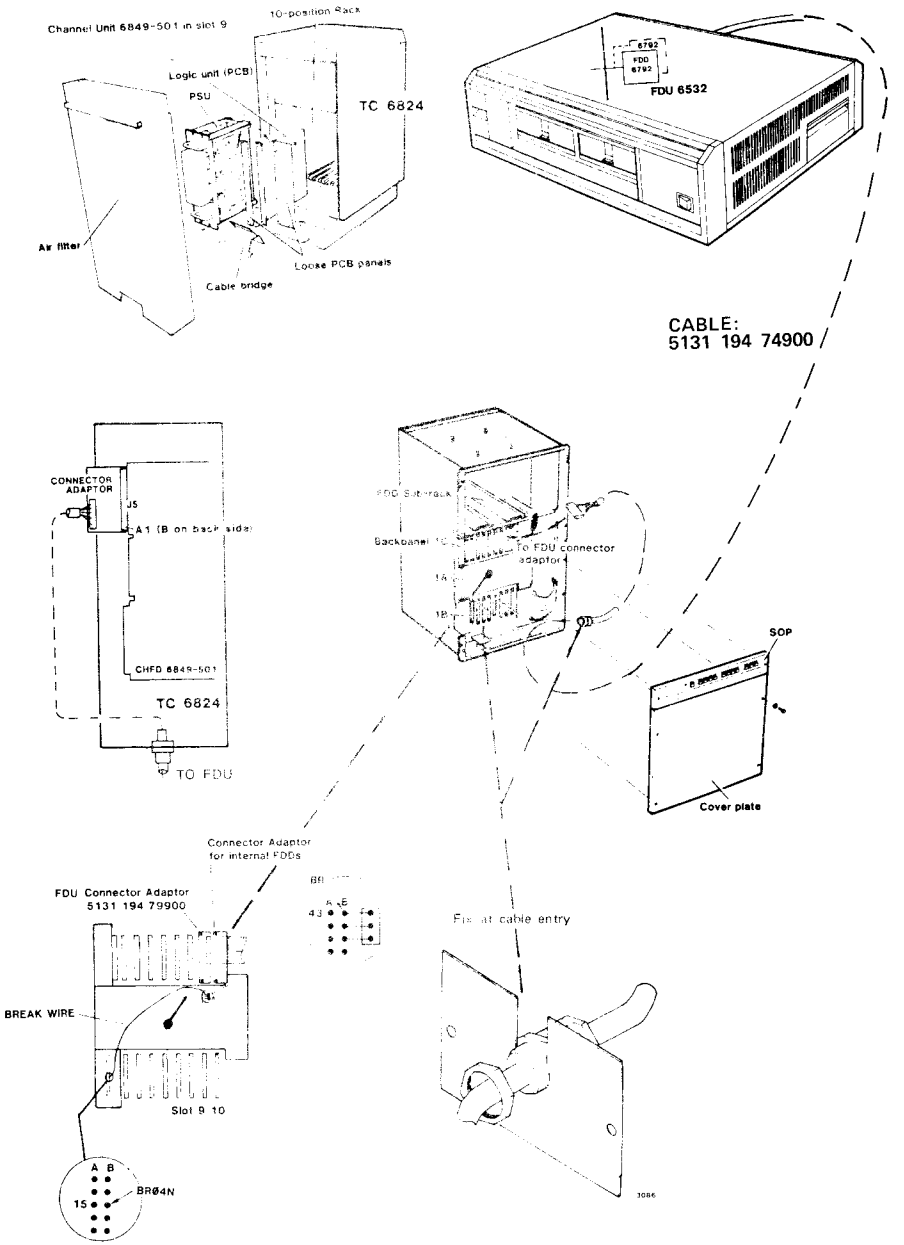


Figure 17.7 CONNECTION FDU 6532/6849-501

Pin No.	Signal Mnemonic	Signal Function	
5A01	DC5ØN	Disc Type (9406)	Unit 4 door lock (9404)
5A02	DC48N	Unit 2 door lock (9406)	Unit 3 door lock 9404)
5A03,4	--	Not used	
5A05	DC42N	Unit 1 door lock (9406)	Unit 2 door lock (9404)
5A06	DC4ØN	Head Select (9406)	Unit 1 door lock (9404)
5A07	RDYØN	Drive unit 1 ready signal	
5A08	WRPN	Write protected disc	
5A09	RDY3N	Drive unit 4 ready signal	
5A10	RDY2N	Drive unit 3 ready signal	
5A11	RDY1N	Drive unit 2 ready signal	
5A12-24	--	Not used	
5A25	SEL3N	Drive unit 4 selection signal	
5A26	SEL2N	Drive unit 3 selection signal	
5A27	SEL1N	Drive unit 2 selection signal	
5A28	SELØN	Drive unit 1 selection signal	
5A29	WDN	Write data signal	
5A30	WEN	Write enable signal	
5A31	DIRN	Each pulse of STEPN moves the head one track	
5A32	STEPN	in the direction specified by DIRN	
5A33	LWCN	Low write current select	
5A34	INDN	Index pulse	
5A35	TRØN	Track zero detect	
5A36	HLN	Head load signal	
5A37	RDLN	Read data/clock composite signal	
5B01	OV	Ground	
5B02	DC47N	Special applications (9406)	Not used (9404)
5B03	DC45N	(see table 17.2)	Not used (9404)
5B04-11	OV	Ground	
5B12-24	--	Not used	
5B25-37	OV	Ground	

Table 17.1 CONNECTIONS TO FLOPPY DISC DRIVES (connector J5)

CU signal name	Pin No.	CU function with 9404	9404 drive signal name	CU function with 9406	9406 drive signal name
DC40N	5A06	Lock unit 0	Lock unit 1	Head select	Head select
DC42N	5A05	Lock unit 1	Lock unit 2	Lock unit 0	Lock unit 1
DC45N	5B03	--	Ground	Lock unit 2	Ground
DC47N	5B02	--	Ground	Lock unit 3	Ground
DC48N	5A02	Lock unit 2	Lock unit 3	Lock unit 1	Lock unit 2
DC50N	5A01	Lock unit 3	Lock unit 4	Disc type	Disc type

Table 17.2 FUNCTIONS OF DCXXN SIGNALS

Pin No.	Signal Mnemonic	Signal Function
1A10	DS06N	Panel switch 1 operated
1A08	DS07N	2
1B01	DS08N	3
1A01	DS09N	4
1B02	DS10N	5 — DSW
1A02	DS11N	6
1A03	DS12N	7
1A05	DS13N	8
1A06	DS14N	9
1A07	DS15N	10
1B11	DL05N	Illuminate panel lamp 1
1A11	DL06N	2
1A12	DL07N	3
1A13	DL08N	4
1A14	DL09N	5 — LED
1A18,1B18	DL10N	6
1A15,1B15	DL11N	7
1A16	DL12N	8
1B20	DL13N	9
1A17,1B17	DL14N	10
1A19	DL15N	11
1A04	0V	Power supply return
1A09	CHAEND	Switch operated detect
1A20	+5V	Power supply
1A21-37	--	Not used
1B03-6,8-10,12-14,16	0V	Power supply return
1B07	CHABEGN	Activate switch chain on panel
1B19	+5V	Power supply
1B21-37	--	Not used

Table 17.3 SYSTEM'S OPERATOR PANEL CONNECTIONS (connector J1)

Pin No.	Signal Mnemonic	Signal Function
4J01,3	+5V	Power supply
4J02-16 (even nos.)	IVB7N-ON	CU internal bus lines
4J25,23, 5-21 (odd nos.)	RAD02-12	PROM address lines
4J18	CX1TEST	Test input for microprocessor clock
4J20	CX2TEST	
4J22,24	0V	Power supply

Table 17.4 TEST CONNECTIONS (connector J4)

SIGNAL	FUNCTION	PIN NO ADAPT. CHFD	WIRE COLOUR IN CABLE	PIN NO CONN. FDU
HLN	Head Load	36A	Yw/Pk	04
DUN1N	Door 1 Unlock	03B	Yw/Gy	8
RDYN	Ready	13A	Yw/Bu	28
INDN	Index Pulse	34A	Yw	08
USØN	Unit Select Ø	05A	Bu/Rd	20
US1N	Unit Select 1	02A	Vt	22
MTRØN	(Conn. to ground)	--	--	--
MTR1N	(Conn. to ground)	--	--	--
DIRN	Head Direction In	31A	Gy/Bn	14
STEPN	Head Movement 1 track	32A	Wt	12
WDN	Write Data	29A	Bn/Gn	18
WEN	Write Enable	30A	Yw/Bn	16
TRØN	Track Ø detected	35A	Pk	06
WRPN	Write Protected Disc	08A	Bn/Bu	36
RDN	Read Data/Clock	37A	Rd	02
HDSN	Head 1 Select	06A	Br/Bk	40
DUNØN	Door Ø Unlock	01A	Yw/Rd	42
GROUND		01B,/4-11B, 25-37B	--	ODD NO'S

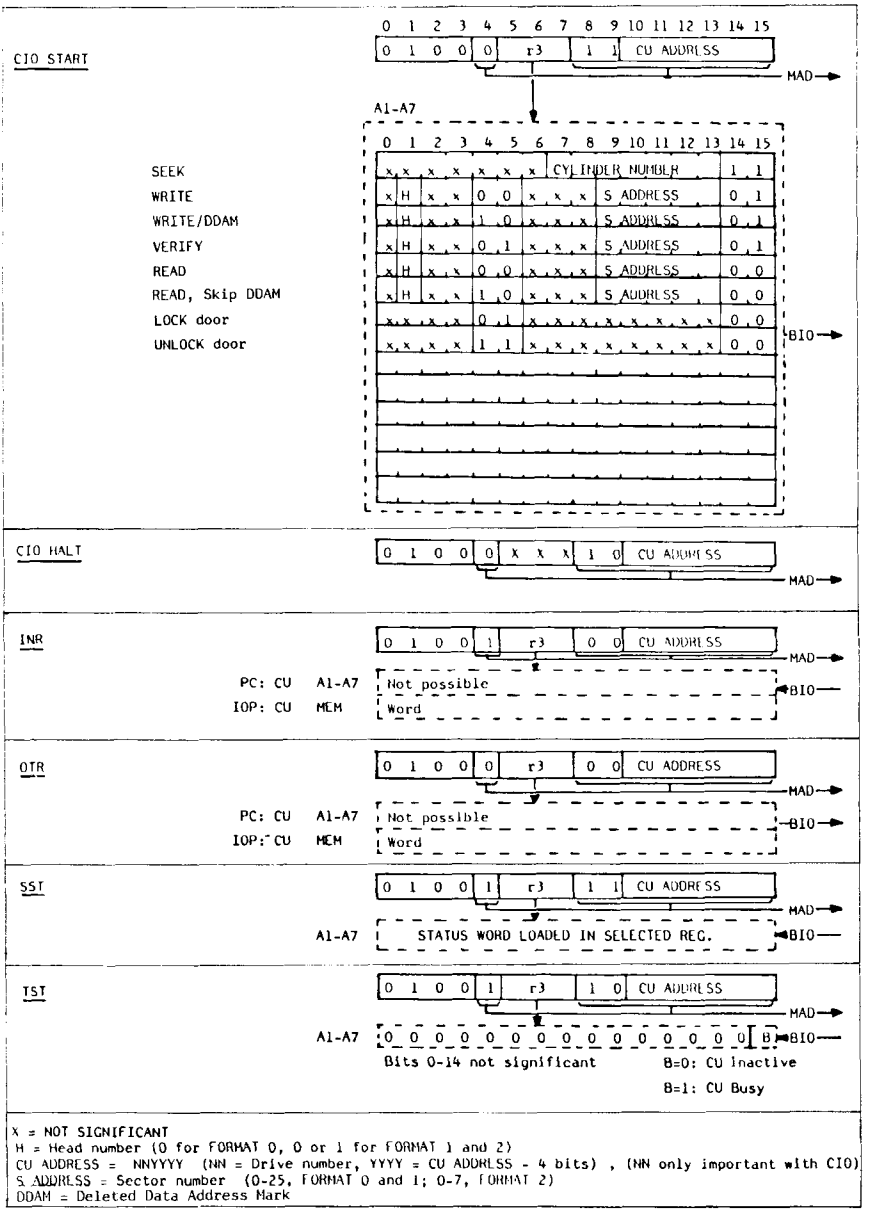
Identification cable: 5131 194 74900

Table 17.5 SIGNAL/PIN RELATION F1MBØ6/FDU 6532

Format 0	Format 1	Format 2
1 sided discette single density 1 head	2 sided discette double density 2 heads	2 sided discette double density 2 heads
77 tracks total (0 - 76) track 0 - Index 1 - 73 or 74 - Data tracks 75,76 - Spare	77 cylinders total (0 - 76) cylinder 0 - Index 1 - 74 - Data cyl 75,76 - Spare	77 cylinders total (0 - 76) cylinder 0 - Index 1 - 74 - Data cyl 75,76 - Spare
26 sectors/track 128 bytes/sector	26 sectors/track * 256 bytes/sector	8 sectors/track * 1024 bytes/sector
total 'data' capacity 246,272 bytes	total 'data' capacity 985,088 bytes	total 'data' capacity 1,212,416 bytes
drive types CDC 9404 or CDC 9406	drive type CDC 9406	drive type CDC 9406
discette type - 8" IBM, 1-sided, PARTN 2305830 (or equiv.)	discette type - 8" IBM, 2-sided, PARTN 1766872 (or equiv.)	discette type - 8" IBM, 2-sided, PARTN 1669045 (or equiv.)
IBM systems using this format - IBM 3740, IBM 5320, IBM 1, all systems using IBM "Standard Data Interchange"	IBM systems using this format - IBM 34-2	IBM systems using this format - IBM 34-2

Table 17.6 FORMATS AND DISCETTES

* Note: Format 1 - Cyl. 0, head 0 is formatted as for format 0
(i.e. 26 sectors/track, 128 bytes/sector)
Format 2 - Cyl. 0, head 0 as for format 0
Cyl. 0, head 1 as for format 1



X = NOT SIGNIFICANT
H = Head number (0 for FORMAT 0, 0 or 1 for FORMAT 1 and 2)
CU ADDRESS = NNYYYY (NN = Drive number, YYYY = CU ADDRESS - 4 bits) , (NN only important with CIO)
S ADDRESS = Sector number (0-25, FORMAT 0 and 1; 0-7, FORMAT 2)
DDAM = Deleted Data Address Mark

Figure 17.8 INSTRUCTION / COMMAND-WORD FORMATS

17.4.1 INITIAL PROGRAM LOADING

The High/Low Core Loader can be loaded from floppy disc using the standard IPL ROM.
With the bootstrap the High/Low Core Loader is loaded from cylinder 0, head 0. This TRACK is always formatted with Format 0 (single density, 26 sectors/track and 128 bytes/sector).

From SOP loading is possible with SOP switch 7 from drive 0 and with SOP switch 8 from drive 1.

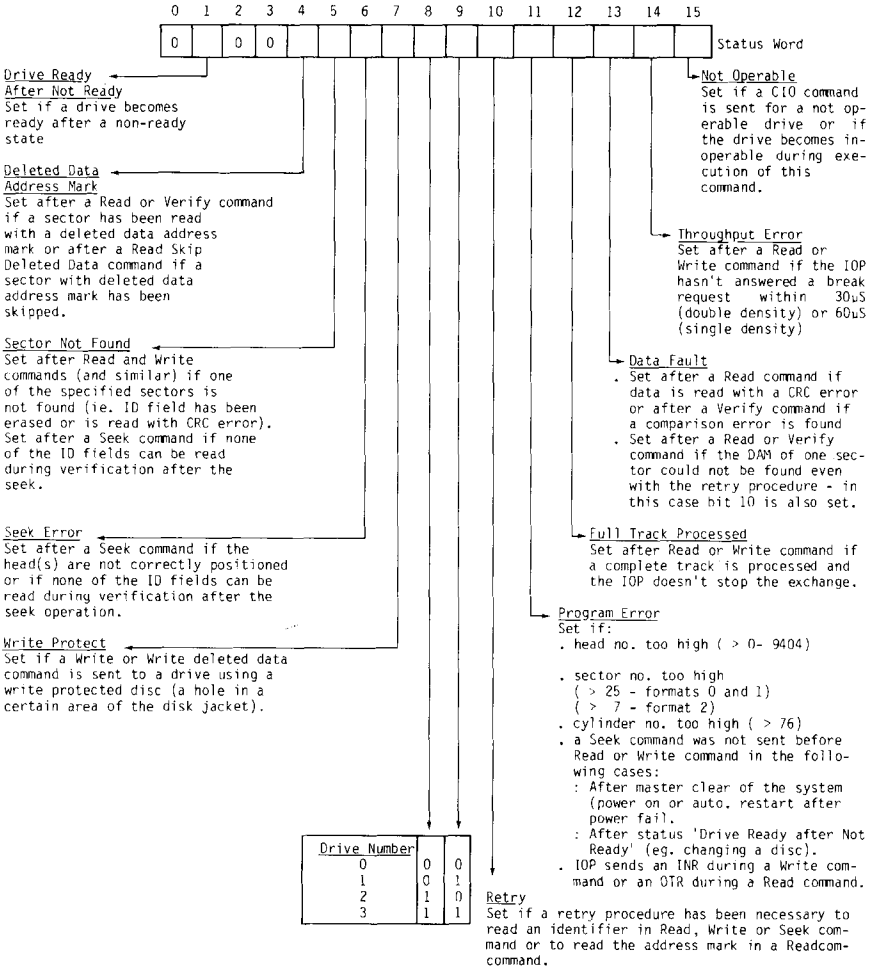


Figure 17.9 EXPLANATION OF STATUS WORD

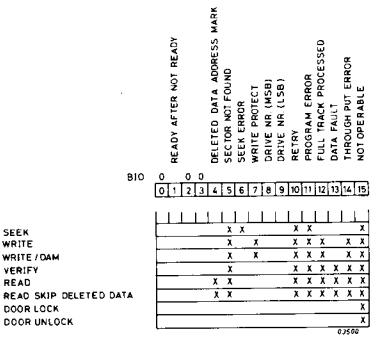


Figure 17.10 STATUS WORD - POSSIBLE CONFIGURATIONS

17.5 SHORT DESCRIPTION OF TESTPROGRAMS

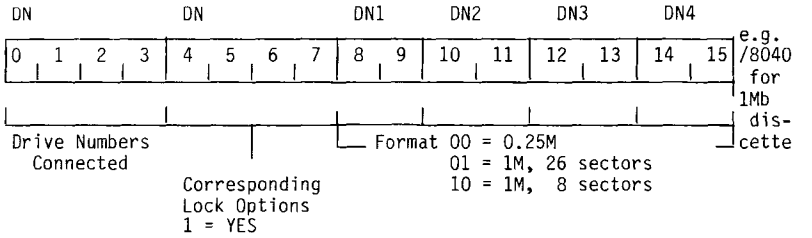
TESTPROGRAM TF1MZ (SEE LOAD PROCEDURE TF TESTPROGRAMS)
MINIMAL REQUIRED: HAND HOLD PANEL OR TERMINAL

1) IPL
Program simulates stops at /700 = (SOP indicators 2,3,4 on).

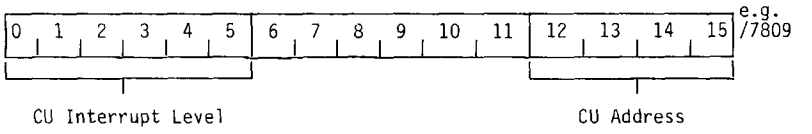
2) SWITCH ON RTC
Load scratch discette

3) Press SOP switch 10 if the registers A7, 8, 9, 10 have to be modified.

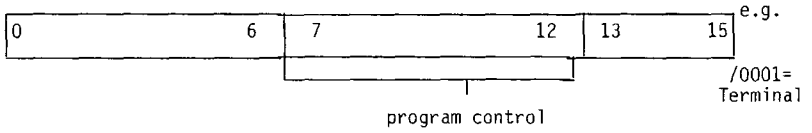
A7



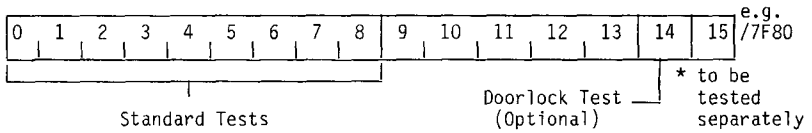
A8



A9



A10



4) Program starts after modification of the registers or after depressing SOP switch 9.
Error stop: /5F0 is simulated on SOP.

Interrupts return: /700 is simulated on SOP.
Information stop: /5E0 is simulated on SOP.

For more information, see detailed description of test-program.

```
                        IDENT    F1SEEK
                      * SEEK TEST FOR F1M-Z (FLOPPY CU 1MB)
                      * SEEKS BETWEEN CYL 00 AND 32
                      * DRIVE 0 ONLY. STATUS IN A5
                      * IF SEEKING, YOU HEAR THE REGULAR MOVEMENT
                      *
                      * REG A4 IS PRESET BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
                      *              /0003    0 0 0 0 0 0 0 0 0 0  0  0  0  0  1  1
                      *                                            ----------------
                      *                                            SEEK CYLINDER NUMBER
          0009        DA        EQU      9
0000                            RES      /40
0080      FFFF        DATA      DATA     /FFFF
0082      0000                  DATA     0
0084      0403        START     LDK      A4,3
0086      207F                  HLT
0088      20BF                  INH
008A      44C9        RET       CIO      A4,1,DA              SEEK
008C      5C04                  RB(4)    *-2
008E      40C9                  SST      A5,DA                STATUS
0090      5C04                  RB(4)    *-2
0092      8514                  LDR      A5,A5                SET CR ACCORDING STATUS
0094      5104                  RF(1)    ST
0096      3480                  XRK      A4,/80               CHANGE CYL 00 - 32, ETC
0098      5F10                  RB       RET
009A      207F        ST        HLT
                                END      START
```

```
                        IDENT    F1LOOP
                *
                * PROGRAM TO WRITE AND READ A SECTOR CONTINUOUSLY (CU 1MB)
                * WRITE BUFFER /200 UP UNTIL /27E
                * READ BUFFER /300 UP UNTIL /37E
                * DRIVE 0 ONLY.  REG A5 CONTAINS STATUS
                *
                *    PRESET A1: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
                *               /0001  0 0 0 0 0 0 0 0 0 0  0  0  0  0  1
                *                =CIO    -                  I-----------I     -
                *                       HEAD                SECTORNO.         WRITE
                *
                *              A2: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
                *               /C040  1 1 0 0 0 0 0 0 0 1  0  0  0  0  0  0
                *                =WER1   -                  I--------------------1
                *                       WRITE                  BLOCK LENGTH
                *
                *              A3: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
                *               /0200  0 0 0 0 0 0 1 0 0 0  0  0  0  0  0  0
                *                =WER2 I-----------------------------------I
                *                                BUFFER  ADDRESS
                *
                *              A4: BIT 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
                *               /0003  0 0 0 0 0 0 0 0 0 0  0  0  0  0  1  1
                *               =SEEK                    I---------------I
                *                                         CYL NUMBER
                *
                * CHECK CORRECT RUNNING:STOP PROGRAM , COMPARE IF /200 AND ON
                * EQUALS /300 AND ON.
                *    NOTE: DISCETTE FORMAT 0,SS,SD  26 SECTORS,64 WORDS/SECTOR
                * ERROR: STATUS STOP AT /BC (/00BE AT HHP);A5 CONTAINS STATUS WORD
                *
     0009       DA       EQU      9
0000            DA       RES      /4D
0080  FFFF      DATA     DATA     /FFFF
0082  0000      DATA     DATA     0
0084  0101      START    LDK      A1,1                    PRESET REG
0086  8220               LDKL     A2,/C040
0088  C040
008A  8320               LDKL     A3,/200
008C  0200
008E  0403               LDK      A4,3
0090  207F               HLT
0092  20BF               INH
0094  44C9               CIO      A4,1,9                  SEEK
0096  5C04               RB(4)    *-2
0098  4DC9               SST      A5,9                    STATUS
009A  5C04               RB(4)    *-2
009C  8514               LDR      A5,A5
009E  511C               RF(1)    ST                      STATUS FAULT
00A0  7212       RET     WER      A2,/12
00A2  7313               WER      A3,/13
00A4  41C9               CIO      A1,1,9                  PREPARE WRITE (OR READ)
00A6  5C04               RB(4)    *-2
00A8  4DC9               SST      A5,9                    STATUS
00AA  5C04               RB(4)    *-2
00AC  8514               LDR      A5,A5
00AE  510C               RF(1)    ST                      STATUS FAULT
00B0  3101               XRK      A1,1
00B2  8220               XRKL     A2,/4000                CHANGE WRITE TO READ,VICE VERSA
00B4  4000
00B6  8320               XRKL     A3,/0100
00B8  0100
00BA  5F1C               RB       RET
00BC  207F       ST      HLT
                         END      START
```

```
00000                          IDENT    ADJF1M
00001                 *PROGRAM TO ADJUST 1M FLOPPY PTS SYSTEMS
00002                 *
00003                 * AFTER IPL ALL SOP INDICATORS ARE ON
00004                 *
00005                 * LOAD ALIGNMENT FLOPPY IN DRIVE 0
00006                 *
00007                 * PROGRAM SELECTION:
00008                 *   SOP SWITCH 1: ALIGNMENT HEAD 0 (CYLINDER 38)
00009                 *                 2:                HEAD 1
00010                 *                 3: INDEX TO BURST ADJUSTM. HEAD 0 (CYL. 1)
00011                 *                 4:                HEAD 1
00012                 *              BEFORE NEXT STEP, LOAD A SCRATCH FLOPPY
00013                 *                 5: CYLINDER ZERO ADJUSTMENT (CONT. SEEK BETWEEN CYL 0 AND 1)
00014                 *              BEFORE NEXT STEP, LOAD ALIGNMENT FLOPPY AGAIN
00015                 *                 6: CHECK ALIGNMENT HEAD 0
00016                 *                 7:                HEAD 1
00017                 *
00018                 *    8, 9 AND 10: STOP, UNLOAD THE HEADS
00019                 *
00020                 * FLASHING SOP INDICATOR WHEN TEST RUNS
00021                 *
00022                 ************************************************************
00023  0000                    RES      /40
00024  0080  FFFF              DATA     /FFFF,0
       0082  0000
00025        0009       ADR     EQU      9
00026  0084  208F       START   INH
00027  0086  41EE               CIO      A1,1,/2E              START SOP CU
00028  0088  8320               LDKL     A3,/7FF
       008A  07FF
00029  008C  432E               OTR      A3,0,/2E              ALL SOP INDIC. ON
00030  008E  492E       INPUT   INR      A1,0,/2E              INPUT SWITCH FROM SOP
00031  0090  5C04               RB(NA)   *-2
00032  0092  4FC9               SST      A7,ADR                RESET READY INT JUST IN CASE
00033  0094  3962               SRL      A1,2
00034  0096  21FE               ANK      A1,/FE                MASK SOP SW 1-7
00035  0098  580C               RB(Z)    INPUT                 WRONG SWITCH
00036  009A  217E               ANK      A1,/7E                SW1 ?
00037  009C  5018               RF(Z)    PROG1
00038  009E  21BE               ANK      A1,/BE                SW2 ?
00039  00A0  5026               RF(Z)    PROG2
00040  00A2  21DE               ANK      A1,/DE                SW3 ?
00041  00A4  502C               RF(Z)    PROG3
00042  00A6  21EE               ANK      A1,/EE                SW4 ?
00043  00A8  503A               RF(Z)    PROG4
00044  00AA  21F6               ANK      A1,/F6                SW5 ?
00045  00AC  503E               RF(Z)    PROG5
00046  00AE  21FA               ANK      A1,/FA                SW6 ?
00047  00B0  5050               RF(Z)    PROG6
00048                 *
00049                 *****HEAD 1 ALIGNMENT CHECK*****
00050                 *
00051  00B2  0110       PROG7   LDK      A1,/10                SOP INDIC. 7
00052  00B4  5716               RF       PROG2+4
00053                 *
00054                 *****HEAD 0 ALIGNMENT*****
00055                 *
00056  00B6  8120       PROG1   LDKL     A1,/400               SOP INDIC. 1
       00B8  0400
00057  00BA  0200               LDK      A2,0                  READ HEAD 0
00058  00BC  049B               LDK      A4,/9B                SEEK CYL 38
00059  00BE  44C9               CIO      A4,1,ADR              EXEC SEEK COMM
00060  00C0  4FC9               SST      A7,ADR
00061  00C2  5C04               RB(NA)   *-2
00062  00C4  42C9               CIO      A2,1,ADR              EXEC READ COMM
00063  00C6  573E               RF       SOP
00064                 *
00065                 *****HEAD 1 ALIGNMENT*****
00066                 *
00067  00C8  8120       PROG2   LDKL     A1,/200               SOP INDIC 2
       00CA  0200
00068  00CC  8220               LDKL     A2,/4000              READ HEAD 1
       00CE  4000
00069  00D0  5F16               RB       PROG1+6
00070                 *
00071                 *****INDEX TO BURST HEAD 0 ADJUST*****
00072                 *
00073  00D2  8120       PROG3   LDKL     A1,/100               SOP INDIC 3
       00D4  0100
00074  00D6  0200               LDK      A2,0                  READ HEAD 0
00075  00D8  0407               LDK      A4,7                  SEEK CYL 1
00076  00DA  44C9               CIO      A4,1,ADR
00077  00DC  4FC9               SST      A7,ADR
00078  00DE  5C04               RB(NA)   *-2
00079  00E0  42C9               CIO      A2,1,ADR              READ
00080  00E2  5722               RF       SOP
00081
```

```
00082                    *****INDEX TO BURST CHECK HEAD 1*****
00083                    *
00084  00E4  0180       PR064    LDK      A1,/80              SOP INDIC 4
00085  00E6  8220                LDKL     A2,/4000            READ HEAD 1
       00E8  4000
00086  00EA  5F14                RB       PR063+6
00087                    *
00088                    *****CYLINDER 0 ADJUSTMENT*****
00089                    *
00090  00EC  0240       PR065    LDK      A2,/40              SOP INDIC 5
00091  00EE  0403                LDK      A4,3                SEEK CYL 0
00092  00F0  44C9                CIO      A4,1,ADR
00093  00F2  4FC9                SST      A7,ADR
00094  00F4  5C04                RB(NA)   *-2
00095  00F6  340C                XRK      A4,/C               SEEK CYL 3, 0, 3, ETC.
00096  00F8  422E                OTR      A2,0,/2E
00097  00FA  3240                XRK      A2,/40              FLASHING SOP INDIC 5
00098  00FC  492E                INR      A1,0,/2E            SOP SW PRESSED?
00099  00FE  5C10                RB(NA)   PR065+4             IF NOT DO NEXT SEEK
00100  0100  5F70                RB       INPUT+4             NEXT STEP
00101                    *
00102                    *****HEAD 0 ALIGNMENT CHECK*****
00103                    *
00104  0102  0120       PR066    LDK      A1,/20              SOP INDIC 6
00105  0104  5F4C                RB       PR061+4
00106                    *
00107                    *****SOP CONTROL SUBROUTINE*****
00108                    *
00109  0106  0680       SOP      LDK      A6,/80              DELAY
00110  0108  8304                LDR      A3,A1
00111  010A  B20C                XRR      A2,A3               INVERT PROG. NO INDICATION
00112  010C  422E                OTR      A2,0,/2E
00113  010E  E718                ECR      A7,A6               PREPAIR DELAY
00114  0110  1F01                SUK      A7,1
00115  0112  5E04                RB(6)    *-2                 DELAY LOOP
00116  0114  492E                INR      A1,0,/2E            ANY SOP SW PRESSED?
00117  0116  5C0E                RB(NA)   SOP+4               IF NOT CHANGE INDICATOR AND WAIT
00118  0118  5F88                RB       INPUT+4
00119                            END      START
```

```
00000                                IDENT    COPYF1                 (PTS  10-10-85)
00001                          *
00002                          *  COPY PROGR FROM DRIVE  0 TO 1 ON 1M-CU
00003                          *   0.25 DISCETTES ONLY
00004                          *
00005          0003            DA       EQU      3
00006  0000                             RES      /40
00007  0040    FFFF                     DATA     /FFFF,0
       0042    0000
00008  0044    20BF            START    INH
00009  0046    207F                     HLT
00010  0048    87A0                     LDKL     A15,/180               STACK
       004A    0180
00011  004C    0700                     LDK      A7,0                   RESET DDAM FLAG
00012  004E    0100                     LDK      A1,0                   SELECT HEAD 0
00013                          *********SEEK**********
00014  0050    0403            HEAD     LDK      A4,3                   CYL 0
00015  0052    44C3            NXTCY    CIO      A4,1,DA                SEEK
00016  0054    F7A1                     CF       A15,STATUS
       0056    00E4  R
00017  0058    4403                     CIO      A4,1,DA+/10
00018  005A    F7A1            CF       CF       A15,STATUS
       005C    00E4  R
00019                          **********READ**********
00020  005E    8220                     LDKL     A2,/8340
       0060    8340
00021  0062    7206                     WER      A2,DA+DA
00022  0064    8320                     LDKL     A3,/200                DATA BUF ADDR
       0066    0200
00023  0068    7307                     WER      A3,DA+DA+1
00024  006A    41C3                     CIO      A1,1,DA                READ FROM DRIVE 0
00025  006C    F7A1                     CF       A15,STATUS
       006E    00E4  R
00026                          **********WRITE*********
00027  0070    8220                     LDKL     A2,/C340
       0072    C340
00028  0074    7206                     WER      A2,DA+DA
00029  0076    7307                     WER      A3,DA+DA+1
00030  0078    1101                     ADK      A1,1                   CHANGE READ TO WRITE
00031  007A    4103                     CIO      A1,1,DA+/10
00032  007C    F7A1                     CF       A15,STATUS
       007E    00E4  R
00033                          *********VERIFY**********
00034  0080    7206                     WER      A2,DA+DA
00035  0082    7307                     WER      A3,DA+DA+1
00036  0084    B120                     XRKL     A1,/400
       0086    0400
00037  0088    4103                     CIO      A1,1,DA+/10
00038  008A    F7A1                     CF       A15,STATUS
       008C    00E4  R
00039                          *******
00040  008E    B120                     XRKL     A1,/401                RESET FOR READ
       0090    0401
00041  0092    1401                     ADK      A4,1
00042  0094    EC20                     CWK      A4,/133                CYL 76?
       0096    0133
00043  0098    5A48                     RB(2)    NXTCY
00044  009A    9120                     ADKL     A1,/4000               HEAD 1
       009C    4000
00045  009E    5950                     RB(1)    HEAD
00046  00E0    207F                     HLT
00047  00E2    5F5E                     RB       START+2
00048                          *
00049                          *
00050  00E4    4DC3            STATUS   SST      A5,DA
00051  00E6    5C04                     RB(4)    *-2
00052  00E8    A520                     ANKL     A5,/0F07
       00EA    0F07
00053  00EC    5002                     RF(0)    RTN
00054  00EE    207F                     HLT                             BIT 4=DDAM OTHER BITS MEAN ERROR
00055                          *     IN CASA OF DDAM CONTINUE IS POSSIBLE, BUT DDAM SIGN IS NOT COPIED
00056  00F0    F03E            RTN      RTN      A15
00057                          END      END
```

```
00000                                   IDENT    READF1                 (PTS  10-10-85)
00001                          *
00002                          *  READ CHECK ON IDENTIFIERS AND DATA
00003                          *   0.25 DISCETTES AND 1M (26 SECTORS)
00004                          *
00005          0009            DA       EQU      9
00006                          *
00007                          *  START BY SOP SWITCH
00008                          *  STATUS BITS DISPLAYED ON SOP:
00009                          *
00010                          *   SOP IND.NO      MEANING
00011                          *          1        SECTOR NOT FOUND
00012                          *          2        SEEK ERROR
00013                          *          3        -
00014                          *          4        -
00015                          *          5        -
00016                          *          6        RETRY
00017                          *          7        -
00018                          *          8        -
00019                          *          9        DATA ERROR
00020                          *         10        THROUGHPUT ERROR
00021                          *         11        NOT OPERABLE
00022                          *  NO INDICATOR MEANS DDAM FOUND: CONTINUE
00023                          *
00024                          *
00025  0000                             RES      /40
00026  0080  FFFF                       DATA     /FFFF,0
       0082  0000
00027  0084  20BF            CIOS       INH
00028  0086  47EE                       CIO      A7.1,/2E                START SOP
00029  0088  4F2E                       INR      A7,0,/2E                WAIT FOR SOP INTERRUPT
00030  008A  5C04                       RB(4)    *-2
00031  008C  87A0                       LDKL     A15,/180                STACK
       008E  0180
00032  0090  4DC9                       SST      A5,DA
00033  0092  0100                       LDK      A1,0                    SELECT HEAD 0
00034                          *********SEEK**********
00035  0094  0403            HEAD       LDK      A4,3                    CYL 0
00036  0096  44C9            NXTCY      CIO      A4.1,DA                 SEEK
00037  0098  F7A1                       CF       A15,STATUS
       009A  008E  R
00038                          **********READ**********
00039  009C  8220                       LDKL     A2,/8DDD
       009E  8DDD
00040  00A0  7212                       WER      A2,DA+0A
00041  00A2  8320                       LDKL     A3,/200                 DATA BUF ADDR
       00A4  0200
00042  00A6  7313                       WER      A3,DA+0A+1
00043  00A8  41C9                       CIO      A1.1.DA                 READ FROM DRIVE 0
00044  00AA  F7A1                       CF       A15,STATUS
       00AC  008E  R
00045  00AE  1404            ON         ADK      A4,4                    NEXT CYL
00046  00B0  EC20                       CWK      A4,/133                 CYL 767
       00B2  0133
00047  00B4  5A20                       RB(2)    NXTCY
00048  00B6  9120                       ADKL     A1,/4000                HEAD 1
       00B8  4000
00049  00BA  5928                       RB(1)    HEAD
00050  00BC  5F38                       RB       CIOS+2                  READ FINISHED
00051                          *
00052  00BE  4DC9            STATUS     SST      A5,DA
00053  00C0  5C04                       RB(4)    *-2
00054  00C2  A520                       ANKL     A5,/0E27
       00C4  0E27
00055  00C6  500C                       RF(0)    RTN
00056  00C8  452E                       OTR      A5,0,/2E                STATUS TO SOP (/000=DDAM,CONTINUE!)
00057  00CA  4F2E                       INR      A7,0,/2E                WAIT FOR SOP INTERRUPT
00058  00CC  5C04                       RB(4)    *-2
00059  00CE  8720                       LDKL     A7,/780                 CLEAR SOP OUTPUT TO/FDD
       00D0  0780
00060  00D2  472E                       OTR      A7,0,/2E
00061                          * CONTINUE AFTER DDAM (A5=/800) MEANS DDAM IS NOT COPIED
00062  00D4  F03E            RTN        RTN      A15
00063                                   END      CIOS
```

LIST OF ILLUSTRATIONS

LIST OF TABLES

18.1 CHLT-IDENTIFICATIONS

Type-number:	PTS-6831-001
Test-Program:	TERTST
Channel:	Programmed Channel
Devices:	Selector Unit Local Terminals: PTS-6314-OXX (XX=configuration number) TP71: PTS-6371-OXX (equipped with COML) FT80: PTS6281/83

Power-Consumption: +5 Volt, 2.2 Amp.

Transmission mode: A-synchronous, PTS local procedure, with acknowledgement of each transmitted character, via Local Cable. Character length: 16 bits. Full Duplex.

Line Speed: fixed by strap: 38.4 kHz or 76.8 kHz

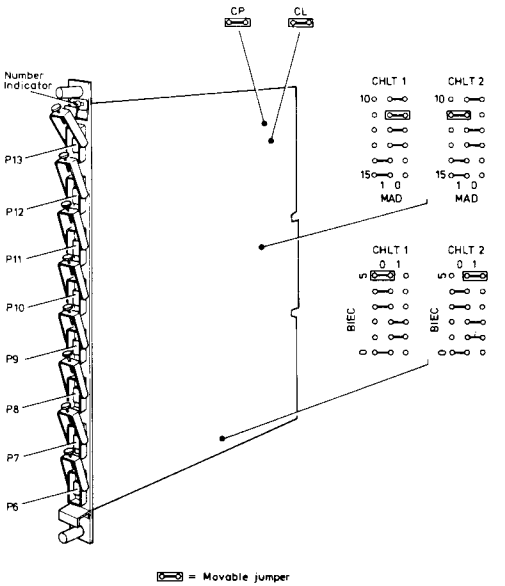


Figure 18.1 STRAP-SETTINGS

Strap CL can be put in two positions: L = 38.4 kHz|— Transfer rate
H = 76.8 kHz| bits/second

Number Indicator: CHLT1 : slide to show 1 (Terminals 1 - 8)
CHLT2 : slide to show 2 (Terminals 9 - 16)

Signal name	Pin no.'s CU Connector
DATA IN	1 & 2
DATA OUT	3 & 4
CLOCK	5 & 9

Table 18.1 CU TO TERMINAL CONNECTIONS

At the rear of the Channel Unit are 8 connectors, each 9 sockets Cinch Connector.
One to eight terminals may be connected.
A terminal connected to the bottom connector is called Terminal 1 (logical 0).
The terminal connected to the top connector is called Terminal 8 (logical 7).

The Channel Unit may be connected to a Terminal by means of a e.g. Local Cable; the length of which may not exceed 150 meters.

LOCAL CABLE

For cabling see chapter 2 "Installation"

The "local" cables have a "Cinch" connector at one end. (CU connection). These are 9-socket connectors consisting of:

. Cinch Shell R43 81960 00 000
. Cannon Connector DEC 9S-F0
. Cannon Sockets 030-1953 00 000

These connectors are available in kits containing all parts required to mount 50 connectors (excluding cable markers).

A kit contains:

- 50 Connectors
- 50 Shells
- Relevant number of sockets
- Shrink tubing
- Roll of Copper Tape
- Roll of Electro Tape

Such kits can be ordered under the code number 5131 191 44500.

At the other end there is either a "CINCH", a "PHILIPS" or a "BERG" connector, depending on the type of terminal.

Bit configuration input/output register CPU:

Bit no:	0	1 2 3	4 5 6	7 8	9 10 11 12 13 14 15
	0	D_2 D_1 D_0	T_2 T_1 T_0	0 0	C_6 C_5 C_4 C_3 C_2 C_1 C_0

T= Terminal Address

D= Device Address

C= Character Code (/00-/7F) (ASCII or Device dependent commands or status-messages)

The following table defines the different types of messages and bit configuration measured at the Local Cable.

Transfer rate can be 38.4 Kbits/second or 76.8 Kbits per second.

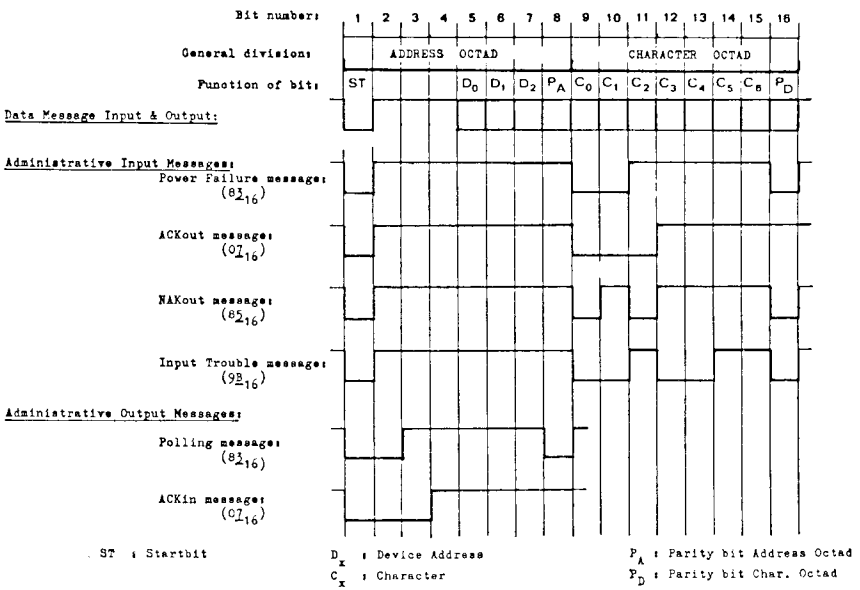


Figure 18.2 MESSAGES AND BIT CONFIGURATION ON THE LOCAL LINE

All Terminal connections (connectors) are "Polled" by the Channel Unit. The POLLING MESSAGE is the sign to a connected Terminal that it can start to do input if any. Output from the Channel Unit is send to the Terminal after the POLLING MESSAGE.

The following figure shows the relation between polling, input and output to one Terminal.

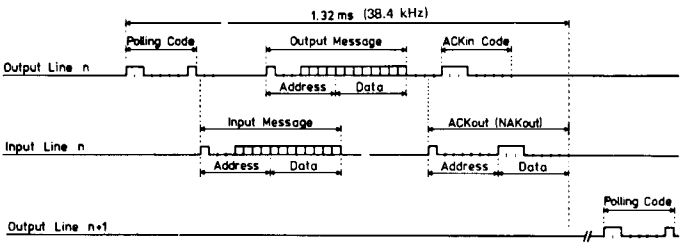


Figure 18.3 SIMULTANEOUS INPUT AND OUTPUT AFTER A POLLING

All input or output messages (except the POLLING MESSAGE) must be acknowledged by the receiver.

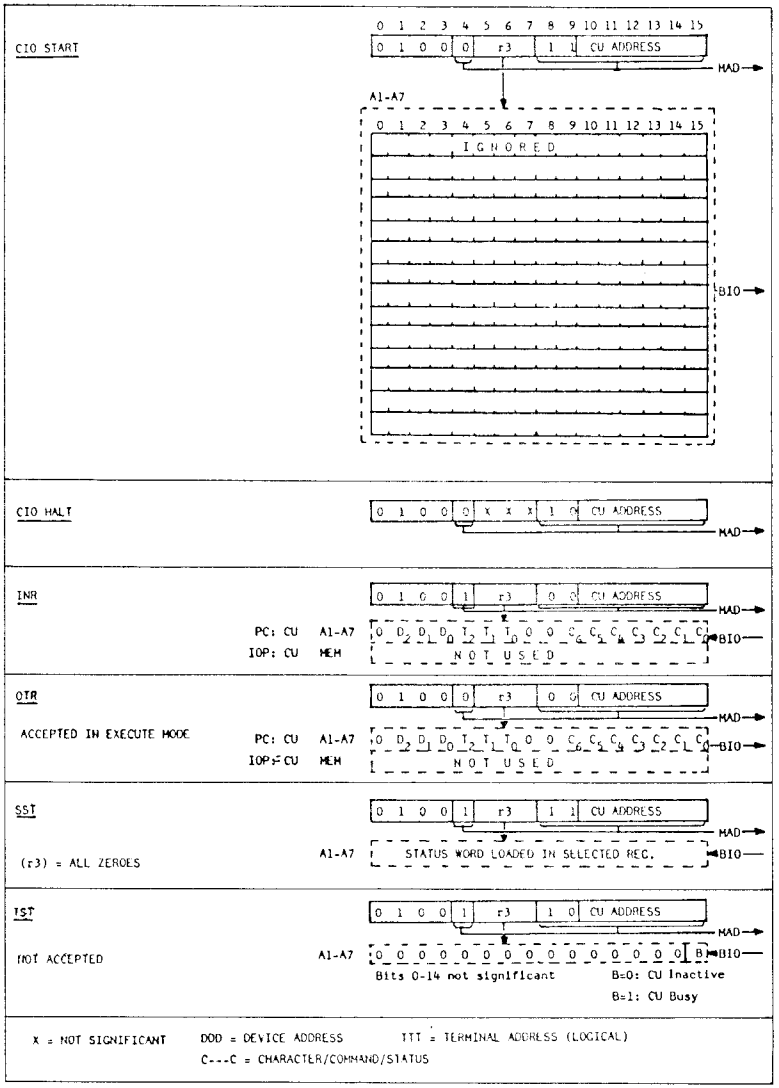
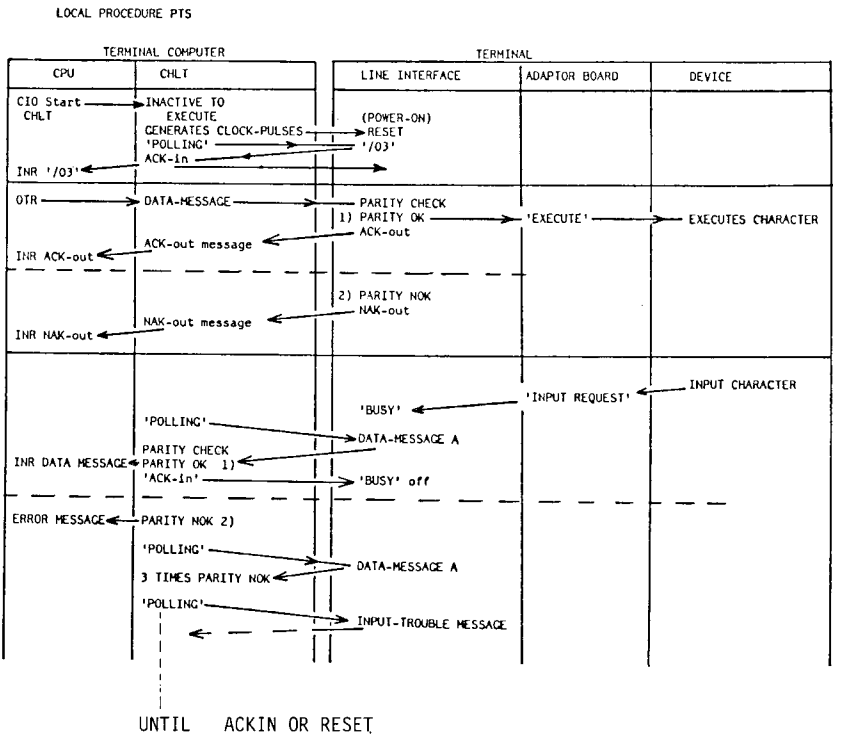


Figure 18.4 INSTRUCTION/COMMAND-WORD FORMAT CHLT



18.5 SHORT DESCRIPTION OF TEST PROGRAMS

The CHLT can be tested only in combination with a Terminal by means of the test-program TERTST. (See detailed description)

```
         DATE  82-05-05        IDENT    KBINPL    FOR PTS


0000                           IDENT    KBINPL                FOR PTS
0001                    *DATE: 820505
0002                    *PROGRAM FOR INPUT FROM KEYBOARD (ADDR 1) ON CHLT1
0003                    *INPUT CHARACTER IS DISPLAYED ON SOP
0004
0005                           AORG     /80
0006
0007 0080 FFFF 0000            DATA     /FFFF,0
0008 0084 20BF          START  INH                           WAITMODE
0009 0086 41C3                 CIO      A1,1,3               START CHLT
0010 0088 4A03          NEXT   INR      A2,0,3               READ POWERFAIL(3) OR CHARACTER
0011 008A 5C04                 RB(4)    NEXT
0012 008C 422E                 OTR      A2,0,/2E             OUTPUT ON SOP
0013 008E 5F08                 RB       NEXT
0014                           END      START
```

```
         DATE  82-05-10        IDENT    KBVDUL


0000                           IDENT    KBVDUL
0001                    *DATE: 82 05 07 FOR PTS
0002                    *PROGRAM FOR INPUT FROM KEYBOARD(DA=1) AND OUTPUT ON
0003                    *VDU(DA=4)ON CHLT1
0004                           AORG     /80
0005
0006 0080 FFFF 0000            DATA     /FFFF,0
0007 0084 20BF          START  INH                           NO INTERRUPTS
0008 0086 41C3                 CIO      A1,1,3               START CHLT
0009 0088 4A03          IN     INR      A2,0,3               WAIT FOR INPUT
0010 008A 5C04                 RB(NA)   IN
0011 008C 8308                 LDR      A3,A2                FOR ANSWER TO KEYBOARD
0012 008E A320 F0FF            ANKL     A3,/F0FF             TAKE OUT LINE
0013 0092 EB20 0007            CWK      A3,7                 IS IT ACK?
0014 0096 5010                 RF(E)    NEXT                 NOT TO KEYBOARD
0015 0098 8308                 LDR      A3,A2                REPAIR LINE
0016 009A A320 0FFF            ANKL     A3,/FFF              TAKE OUT DA
0017 009E 9320 1000            ADKL     A3,/1000             PUT IN KEYB AD
0018 00A2 4303                 OTR      A3,0,3               SEND TO KEYBOARD LAMPS
0019 00A4 4C03                 INR      A4,0,3               GET ANSWER
0020 00A6 5C04                 RB(4)    *-2
0021                    00AB   EQU      *
0022 00AB 422E                 OTR      A2,0,/2E             DISPLAY REC.MES ON SOP
0023 00AA 3AC3                 SLC      A2,3                 CHECK IF KEYBOARD INPUT
0024 00AC 5E26                 RB(NN)   IN
0025 00AE 3AE3                 SRC      A2,3                 REPAIR A2
0026 00B0 9220 3000            ADKL     A2,/3000             ADD DA FOR VDU
0027                                                        WHEN /3000 IS CHANGED TO OTHER VALUE
0028                                                        OUTPUT IS DONE ON OTHER DEVICE
0029 00B4 4203                 OTR      A2,0,3
0030 00B6 5F30                 RB       IN
0031
0032
0033                    *      BY CHANGING /3000 TO OTHER VALUE:
0034                    *      OUTPUT CAN BE DONE ON AN OTHER DEVICE
0035                    *EG:   FOR TEP 71
0036                    *      CHANGE TO /1000
0037                    *      TYPE FROM KEYBOARD: /0D,/11,'IT WORKS',/06
0038                    *      AND IT WORKS IS WRITEN ON THE YOURNAL.
0039                    *      TYPE /0F AND THE PRINTERTEST STARTS
0040                    *      TYPE /0C AND THE TEST STOPS
0041
0042
0043                           END      START


            SYMBOL TABLE

    IN      0088  A   NEXT    00AB  A   START   0084  A

            ASS.ERR.    0000
 :EOF
 PROG ELAPSED TIME:  00H-00M-00S-000MS-
```

```
          DATE  82-08-12        IDENT    TEPLOC


0000                            IDENT    TEPLOC
0001                      *DATE: 820812 FOR PTS
0002                      *TEPLOC IS A PROGRAM THAT PRINTS LINES OF
0003                      *CHARACTERS ABCDEFG ON JOURNAL
0004                      *
0005                      *OF TEP 71
0006 0000                       RES      /40
0007
0008 0080 FFFF                  DATA     /FFFF
0009 0082 0000                  DATA     0
0010 0084 20BF                  INH                          NO INTERRUPTS
0011 0086 8220 00EA R           LDKL     A2,DATBUF           ADDR OF DATABUFFER
0012 008A 41C3                  CID      A1,1,3              START CHLT
0013 008C 4B03            INR   INR      A3,0,3              MESSAGES
0014 008E 5C04                  RB(4)    INR
0015                      *FIND OUT WHAT MESSAGE IS GIVEN
0016 0090 EB21 0707             CCK      A3,/0707            IS IT ACK?
0017 0094 5028                  RF(E)    NEXT                THEN PRINT NEXT CHARACTER
0018 0096 EB21 0505             CCK      A3,/0505            IS IT NACK?
0019 009A 502C                  RF(E)    PREV                PRINT LAST CHAR AGAIN
0020 009C EB21 0303             CCK      A3,/0303            IS IT POWER FAIL?
0021 00A0 5010                  RF(E)    LDR                 THEN LOAD LINENUMBER
0022 00A2 EB21 0000             CCK      A3,0                WAS IT OUTPUT ERROR
0023 00A6 5020                  RF(E)    PREV
0024                                                         AND START PRINTING ON THIS LINE
0025 00A8 432E                  OTR      A3,0,/2E            DISPLAY ANY OTHER MESSAGE ON SUP
0026 00AA 3BC2                  SLC      A3,2                IS IT PRINTER STATUS?
0027 00AC 5602                  RF(NN)   *+4                 YES THEN STOP
0028 00AE 5700                  RF       *+2                 REPLACE BY /207F FOR STOP ON
0029                                                         STATUS MESSAGE FROM TEP
0030 00B0 5F26                  RB       INR
0031                      *LOAD LINENUMBER FROM POWERFAIL MESSAGE
0032                      *AND PUT IN DEVICE ADDRESS
0033 00B2 840C            LDR   LDR      A4,A3
0034 00B4 9420 2000             ADKL     A4,/2000
0035 00B8 8220 00EA R           LDKL     A2,DATBUF
0036 00BC 5706                  RF       LCR
0037      00BE            NEXT  EQU      *
0038 00BE EA20 00F6 R           CWK      A2,BUFEND           IS IT FINISHED?
0039 00C2 560E                  RF(NL)   AGAIN               YES,THEN NEXTLINE ON JOURNAL
0040 00C4 E428            LCR   LCR      A4,A2               LOAD CHARACTER
0041 00C6 5702                  RF       *+4
0042 00C8 1A01            PREV  SUK      A2,1
0043 00CA 4403                  OTR      A4,0,3              WRITE CHARACTER
0044 00CC 5C42                  RB(4)    INR
0045 00CE 1201                  ADK      A2,1
0046 00D0 5F46                  RB       INR                 GET ANSWER
0047 00D2 8520 0500       AGAIN LDKL     A5,/500             TIME DELAY AFTER 1 LINE
0048 00D6 8620 0100       TIMDEL LDKL    A6,/100
0049 00DA 1E01                  SUK      A6,1
0050 00DC 5C04                  RB(NZ)   *-2
0051 00DE 1D01                  SUK      A5,1
0052 00E0 5C0C                  RB(NZ)   TIMDEL
0053 00E2 5700                  RF       *+2                 CAN BE CHANGED TO HLT /207F TO
0054                                                         STOP AFTER EVERY LINE
0055 00E4 8220 00EA R           LDKL     A2,DATBUF           LOAD ADDR DATA BUF
0056 00E8 5F26                  RB       LCR                 GOT PRINT NEXT LINE
0057
0058                      *DATA BUFFER
0059 00EA 0D11            DATBUF DATA    /0D11               CARIAGE RETURN,LINE FEED
0060 00EC 4142 4344             DATA     'ABCDEFGH'
     00F0 4546 4748
0061 00F4 4906                  DATA     /4906               I AND END OF TEXT
0062                      BUFEND END     INR-8


          SYMBOL TABLE

  AGAIN   00D2  R   BUFEND  00F6  R   DATBUF  00EA  R   INR     00BC  R
  LCR     00C4  R   LDR     00B2  R   NEXT    00BE  R   PREV    00C8  R
  TIMDEL  00D6  R

          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-18S-700MS-
```

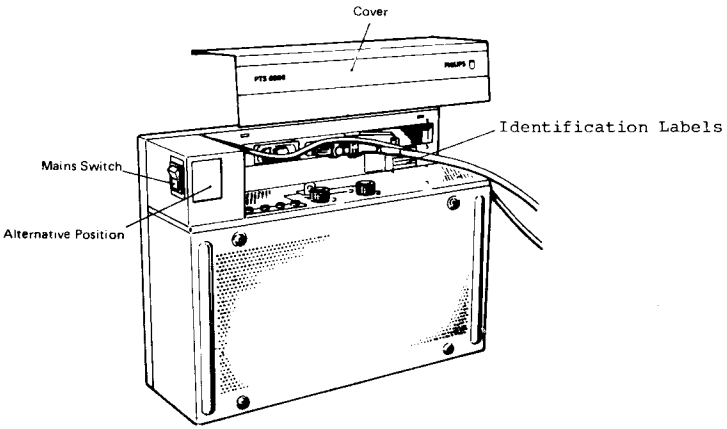


Figure 18.5 TYPICAL SELECTOR UNIT

```
6X1X - XXX
  |  |   |└──────Configuration, see Table 18.2
  |  |   0 = Local Connection, 1 = Remote Connection
  |  |
  |  1 = Non-modular 80W unit
  |  2 = Non-modular 100W unit
  |  3 = Reserved for future use
  |  4 = Modular 100W unit (SUM)
  |
  2 = Teller Terminal Environment
  3 = General Terminal Environment or modular unit
  5 = Special Terminal Environment
```

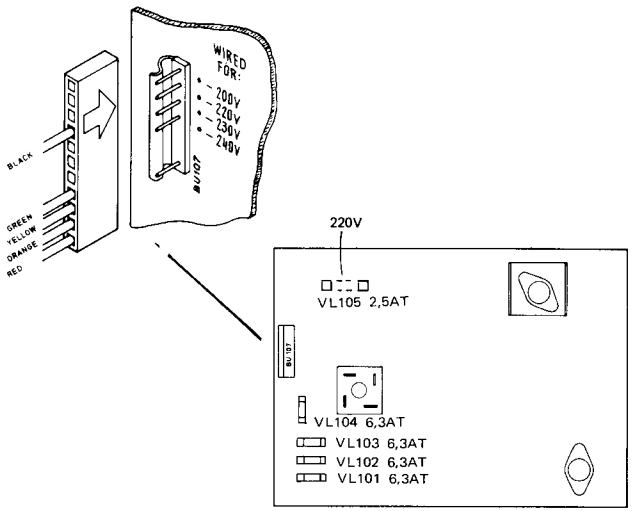


Figure 18.6 MAINS VOLTAGE SELECTOR

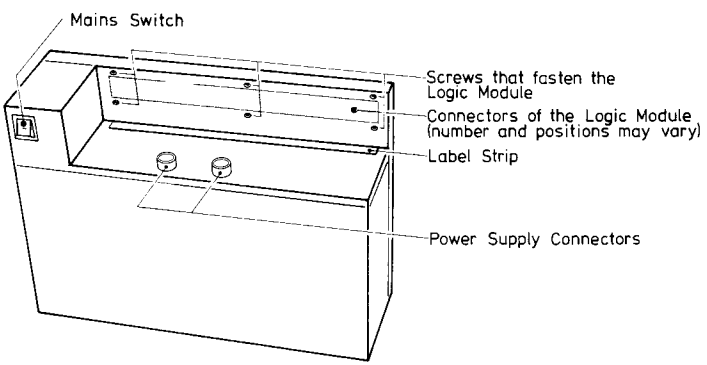
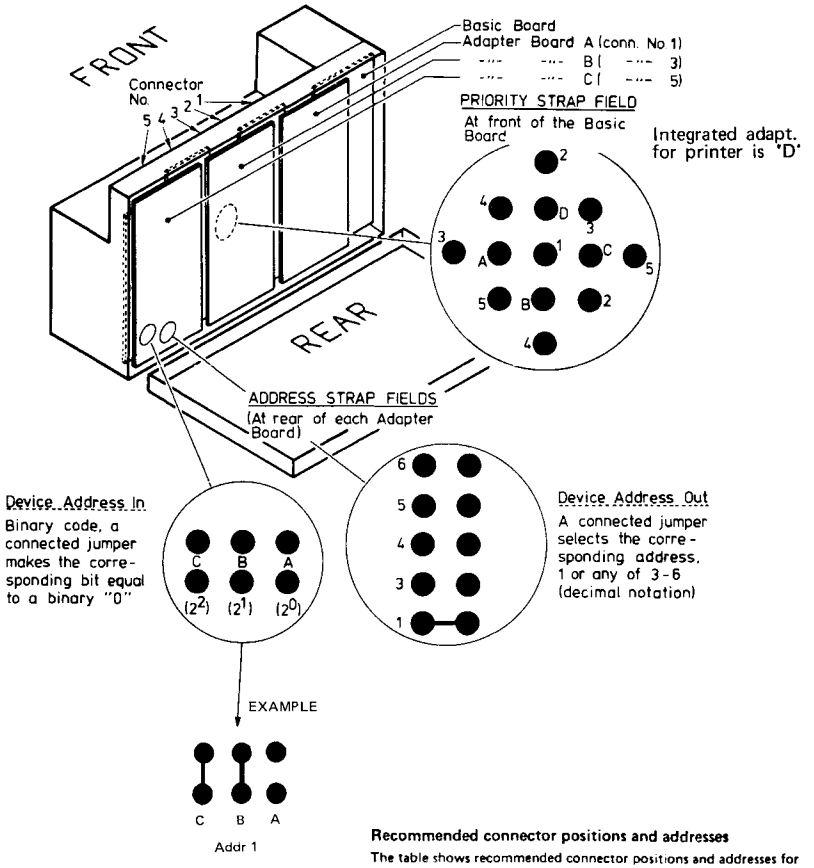


Figure 18.7 CONNECTORS, SCREWS AND LABEL STRIP ON SELECTOR UNITS



Recommended connector positions and addresses

The table shows recommended connector positions and addresses for each group device. If two devices of the same kind or another collision occur a second hand alternative of recommended positions/ addresses is also given. Each device shall have unique connector position and address.

Device	Connector position	Address In	Address Out
Printer	4	2	2
Keyboard			
1 st alt.	1	1	1
2nd alt.	5	5	5
Display			
1st alt.	3		4
2nd alt.	5		3
Reader/Writer	5	5	5

Figure 18.8 JUMPERS IN MODULAR SELECTOR UNITS

The basic unit of the PTS 6314 Selector Unit Modular includes the printer interface. 3 additional adapter boards can be inserted and connected. (1 printer connectable to each SUM). Some subnumbers may show the same configuration of device interfaces (adapter boards) but they differ on the adjustment side. Therefore regarding connector positions, addresses and priorities please see next page.

SUML = Selector Unit Modular Local SUMR = Selector Unit Modular Remote

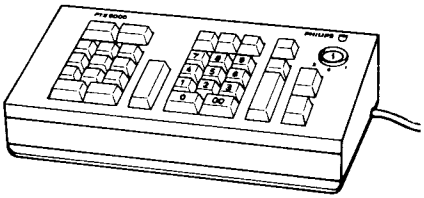
	Subnumbers				Device Interface (adapter boards) 12 NC 5131 192 . . .									Extra PROM
	SUML 50 Hz	SUMR 50 Hz	SUML 60 Hz	SUMR 60 Hz	19600 for SDT 6242	28800 for NSD 6241	29900 for VDU all	35900 for POU 6351	50900 for KBA 6331	51100 for KBN 6231	51300 for KBNS 6233	52500 for KBAN 6232/4	75200 for 1)	
	001	101				1				1				
	002	102			1					1				
	003	103								1				
	004	104										1		
	005	105							1	1				
	006	106			1		1			1				
	007	107					1							
	008	108				1						1		
	009	109	209	309										
	010	110				1						1		
	011	111			1							1		
	012	112						1				1		
	013	–				1			1	1				
	014	114						1		1		1		
	015	115							1					
	016	116										1		
	017	117			1				1	1				
	018	118	218	318			1					1		
N	019	119									1			PTT-S
	020	120			1			1		1				
	022	122	222	322				1		1				
	025	125						1	1	1				
N	026	126						1			1			
N	027	127			1						1			
	028	128					1		1					
	029	129						1				1		
	030	130					1					1		
N	031	131						1				2		ASLK
	032	132			1					2				
	033	133											1	
	034	134	234	334			1						1	
	035	135						1				2		
	036	136											2	
	037	137					1			1				
	038	138	238	338				1					1	
	039	139			1					1		1		
	040	140						1	1					
	041	141										2		
	042	142						1					2	
	043	143	243	343									2	
	044	144	244	344									3	
	045	145								1			1	
	046	146										2	1	
	047	147					1						2	
	048	148					1						2	

1) 5131 192 75200 = PTS 6000 Standard Device Interface, PTS 6317 SDI, for the keyboards 6236/6271/6272, the displays 6385/6386 and the reader/writer units 6261/6266.

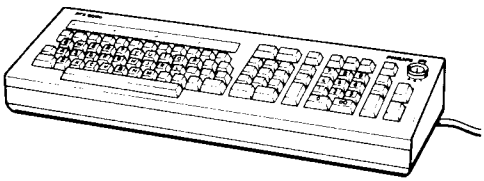
05.04.3.
Oct. 197.

Table 18.2a CONFIGURATION LIST SUML, SUMR-VERSION 1

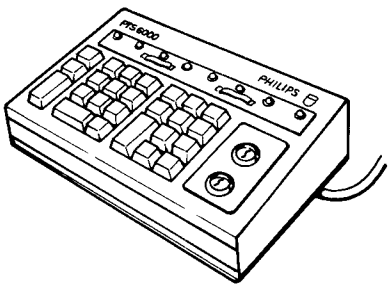
PTS 6231 Keyboard Numeric



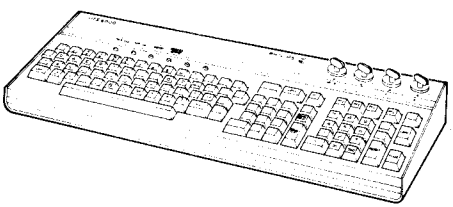
PTS 6232
PTS 6234 Keyboard Alpha Numeric



PTS 6233 Keyboard Numeric



PTS 6236 Keyboard Alpha Numeric



PTS 6331 Keyboard Alpha Numeric

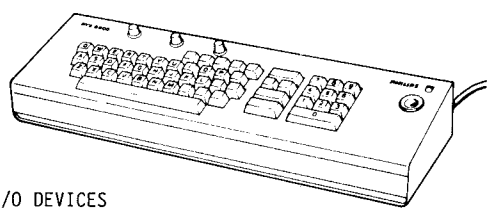
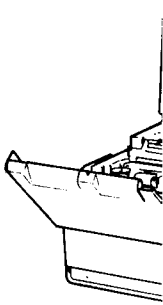
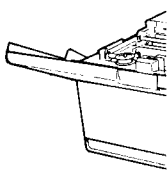


Figure 18.8 TERMINAL I/O DEVICES

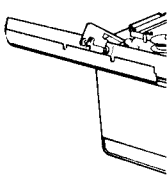
PTS 6221 Teller Te



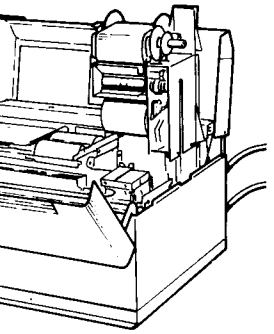
PTS 6222
PTS 6224 Teller Te



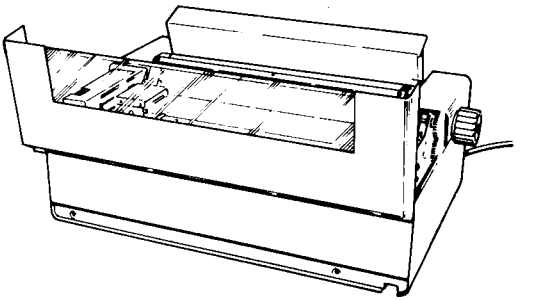
PTS 6223 Teller Te



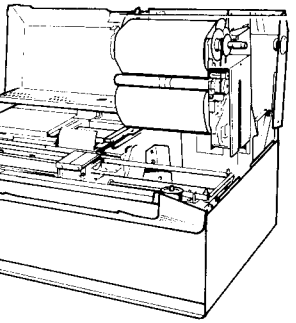
rminal Printer



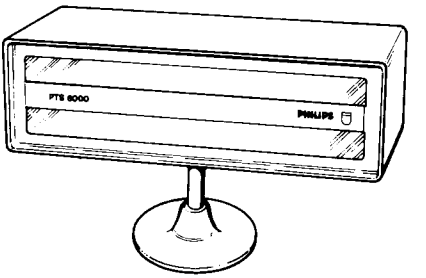
PTS 6321 General Terminal Printer



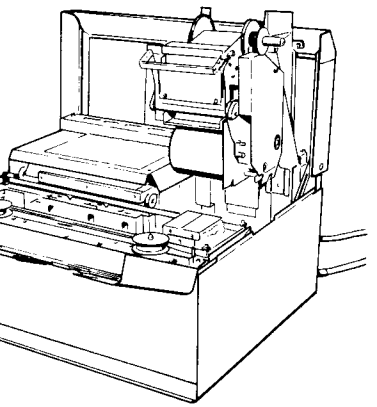
rminal Printer



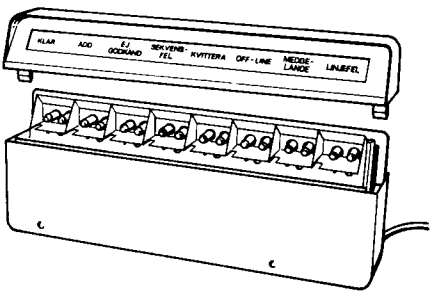
PTS 6241 Numeric and Signal Display



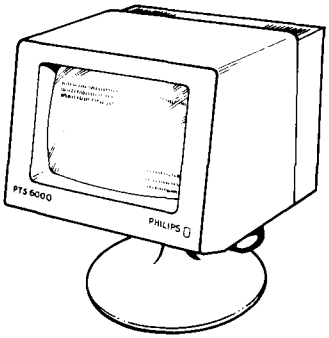
rminal Printer



PTS 6242 Signal Display



PTS 6344 Video Display Unit



PTS 6351 Plasma Display Unit

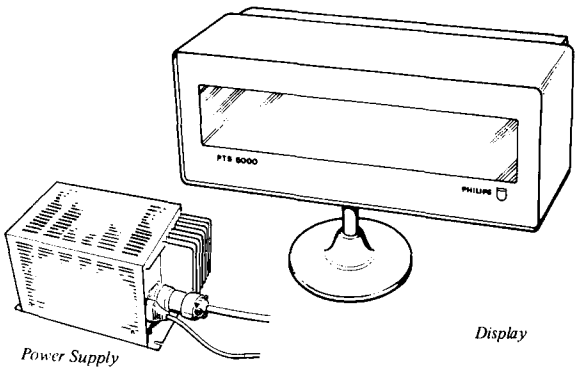


Figure 18.9 TERMINAL I/O DEVICES (CONT'D)

LIST OF ILLUSTRATIONS

LIST OF TABLES

19.1 CHRT-IDENTIFICATIONS

Type-number: PTS-6832-001
Test-Program: TERTST
Channel: Programmed Channel
Devices: Selector Unit Remote Terminals: PTS-6314-1XX
(XX = configuration Number)
TP71: PTS-6371-1XX (equipped with COMR)
FT80: PTS6282/84
TFU: (Transfer Unit): PTS-6471

Transmission mode: A-synchronous, V24, Modem and telephone lines. Character and/or Block mode, depending on software, with acknowledgement. Full duplex.

Line Speed: Up to 9600 bits per second.

Power-Consumption: +5 Volt, 3,4 Amp.

Note: For short distance it is possible to connect the CHRT direct to the Terminal by means of an extended Modem cable.
Some signals have to be forced to a certain voltage level.

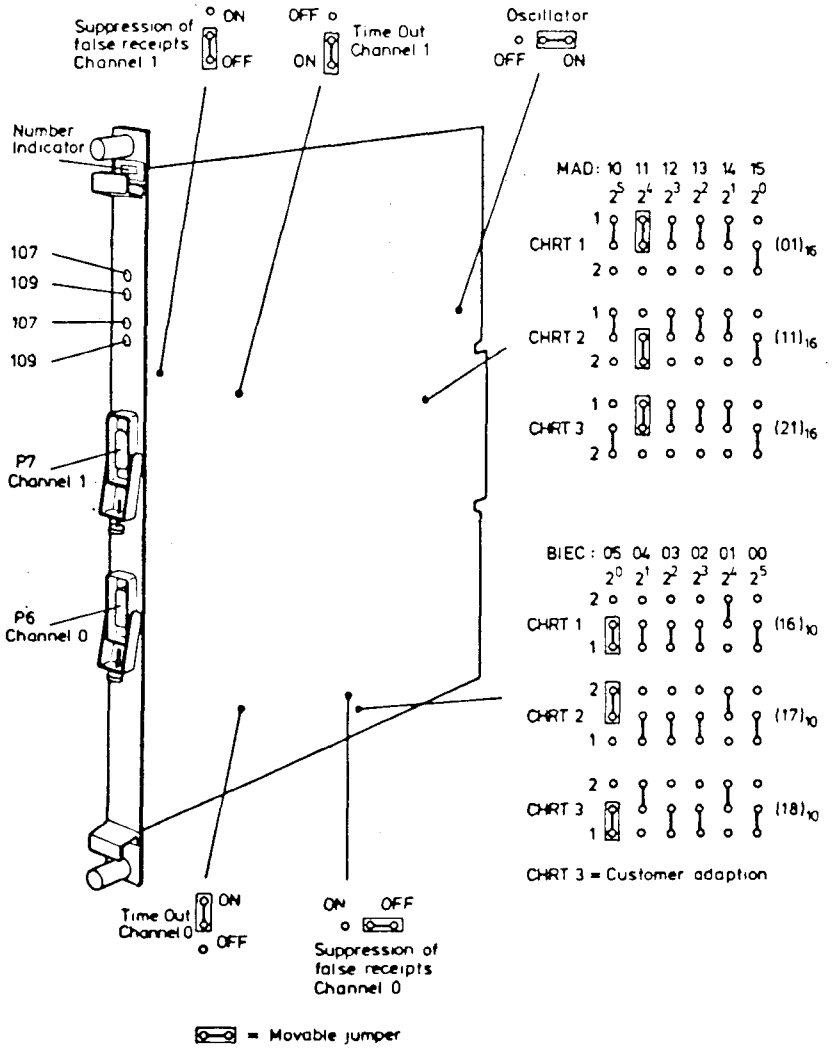
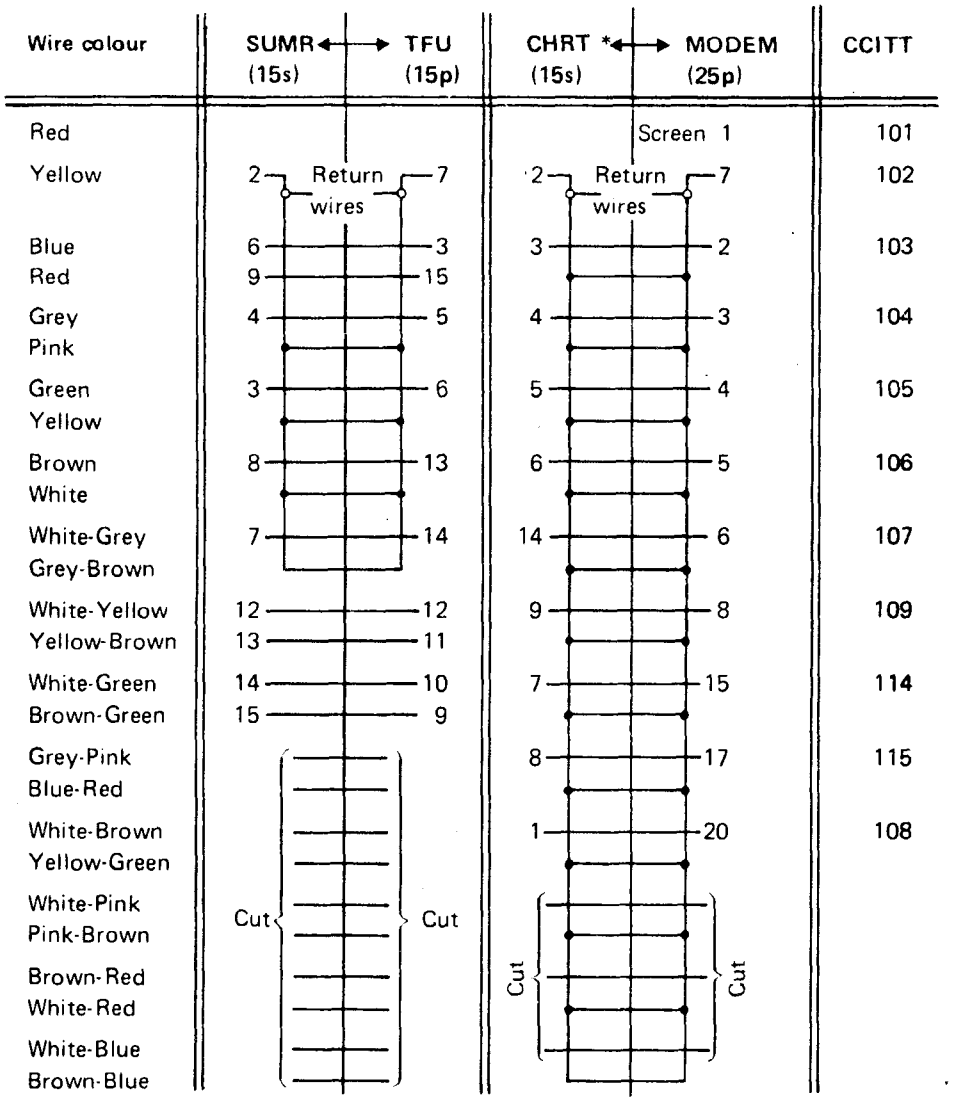


Figure 19.1 STRAP SETTINGS

Number indicator: CHRT1: Slide to show '1': Line numbers 1 and 2
CHRT2: Slide to show '2': Line numbers 3 and 4
CHRT3: Use sticker to indicate CHRT3: Line numbers 5 and 6



PLEASE NOTE!
The pin numbers given for »Modem» are applicable for ITT GH 2054. If other modem is used, the relation between pin numbers and »CCITT» numbers must be checked (connect against »CCITT» numbers)!

Table 19.1 WIRE CONNECTIONS IN CABLE (5131 191 33712) CHRT/MODEM, SUMR/MODEM, TFU/MODEM, SUMR/TFU

V24 signal lines / name / description. (For PTS use)

101 Safety Earth (terminated)
102 Signal Ground (terminated)
103 TDAT: Transmit Data (source)
104 RDAT: Receive Data (receiver)
105 RTS : Request to Send (Not used between TFU and SUMR)
106 RFS : Ready for Sending(Not used between TFU and SUMR) Used for E-bit
107 DSR : Data Set Ready (from modem to lamp) (Modem is ready to operate)
108 Connect Data Set to Line (CHRT is ready to operate)(Not TFU-SUMR)
109 CAD : Carrier detected (from modem to led. Carrierwave 300 - 3000 Hz)
111 Rate Select (Not used)
114 TET : Transmitter Element Timing (from modem to clock/control CHRT)
115 RET : Receiver Element Timing (from modem to clock/control CHRT)

Note: 108 is in SUMR connected to +5 volts

Table 19.2 DESCRIPTION V24 INTERFACE SIGNALS

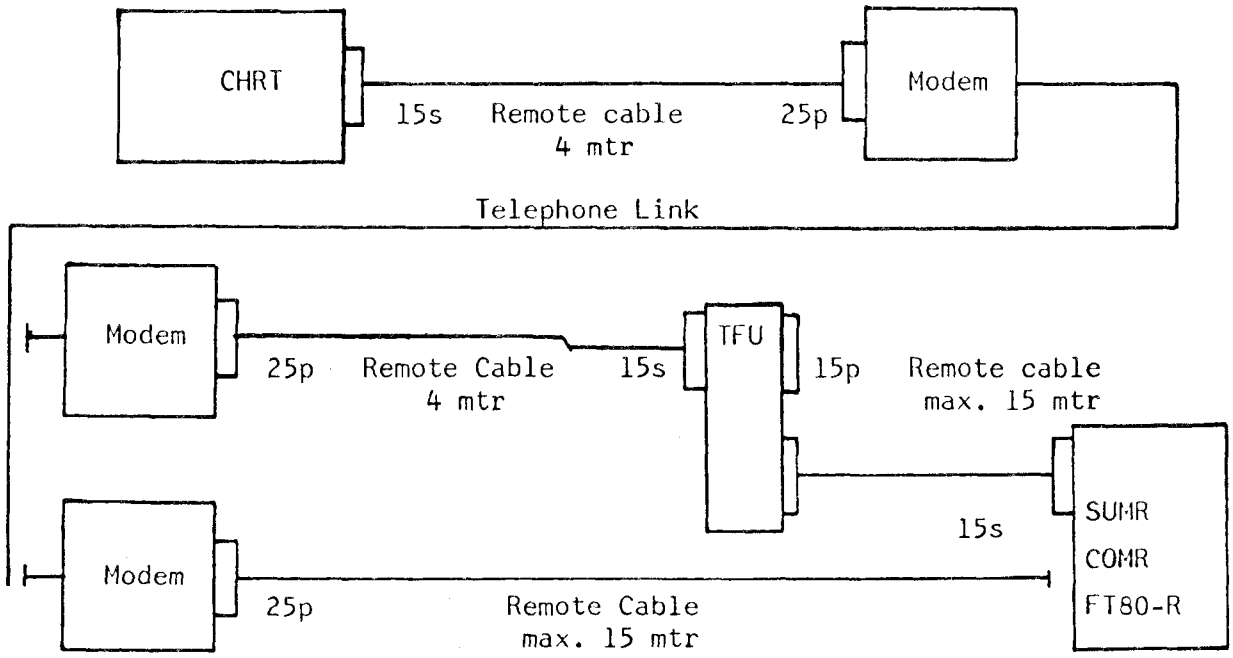


Figure 19.2 CABLE CONNECTIONS PTS REMOTE CONFIGURATION

REMOTE CABLE

For cabling see Chapter 2 " Installation"

If, for some reason, a "remote" 4-m cable must be made up on site, this is easiest made from a prefabricated cable kit. Two kits are available, both giving a 4-m cable with a "modem" connector at one end, but one type has a "15s" connector at the other end while the second has a "25s" connector. These kits are prefabricated up to the point where superfluous wires are to be cut, and where pins and sockets are to be fitted into the connector blocks.

As far as cables TFU-Modem and CRT/CHRT-Modem are concerned, the wiring shown in Table 19.1 is applicable. However, the note on the modem connection is still to be taken into consideration!

The cable kits can be ordered under the following code numbers:

- Kit for a "Modem/15s" cable 5131 191 41700
- Kit for a "Modem/25s" cable 5131 191 41800

The applied connectors are available in kits containing all parts required to mount connectors of one type (excluding cable markers). A kit contains:

- 50 shells (modified)
- 50 connectors
- Relevant number of pins or sockets
- Shrink tubing
- Roll of Copper tape
- Roll of Electro tape
- PVC tubing
- Earthing wire (where applicable).

These kits can be ordered under the following code numbers:

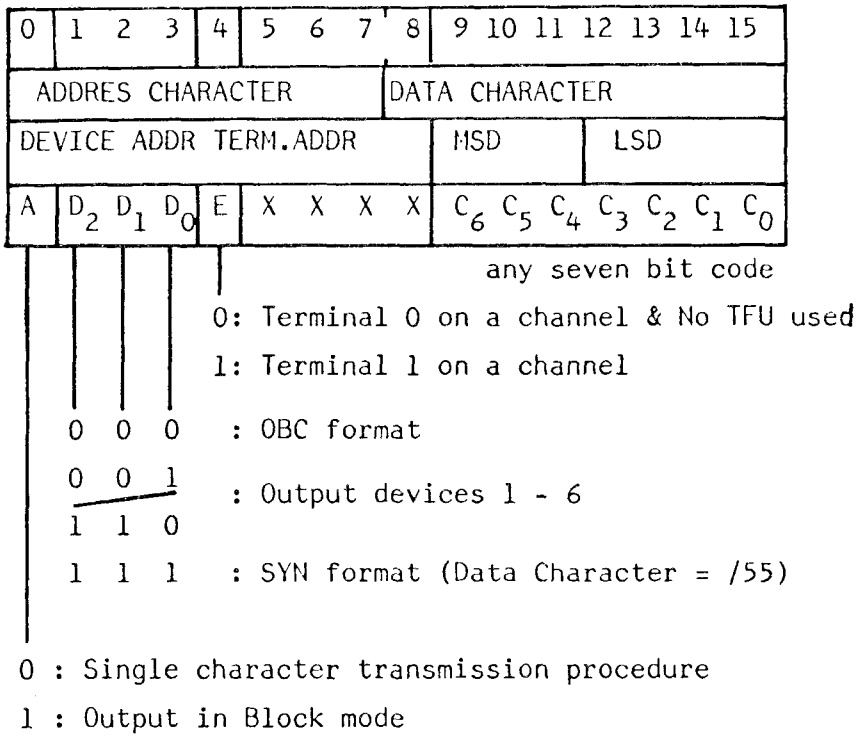
- Kit for 50 connectors "Modem" 5131 191 44200
- Kit for 50 connectors "15s" 5131 191 44300
- Kit for 50 connectors "15p" 5131 191 44400

Note: If the "Cinch" shells are bought from other supplier than Philips, the cable entry hole must be bored out to 12 mm -0 +1 mm.

19.4 HARDWARE/SOFTWARE INTERFACE DETAILS

Output message: (Data & Commands)

BIO-lines:



X : Irrelevant.

—Output message measured on the 103 line:

	ST	d	D_0 D_1 D_2	E	C_0 C_1 C_2 C_3 C_4 C_5 C_6	P	SP SP
OBC	0	0	0 0 0	E	DATA	P	1 1
DOS	0	0	1 -- 6	E	DATA/COMMAND	P	1 1
DOB	0	0	1 -- 6	E	DATA/COMMAND	P	1 1
SYN	0	0	1 1 1	E	1 0 1 0 1 0 1	P	1 1

—Output Receipt message measured on the 103 line:

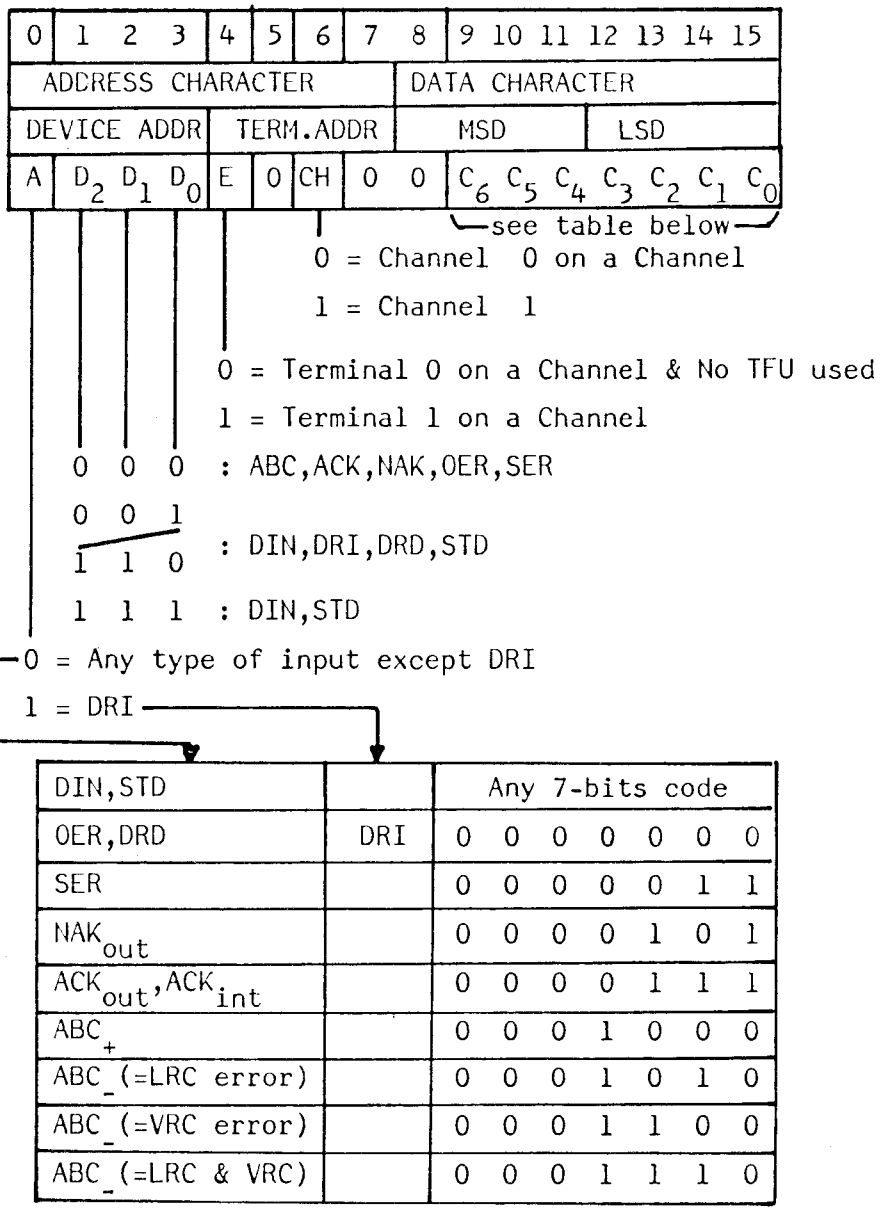
	ST	d	D_0 D_1 D_2	E	P	SP SP
ACK_{in}	0	1	1 1 1	E	P	1 1
NAK_{in}	0	1	0 0 0	E	P	1 1

A = Character or Block mode
d = Message type determinant
DDD = Device Address
E = Terminal Address

ST = Startbit
C--C = Any 7-bits character
P = Parity bit (Odd in Data- and Even in Receipt message)
SP = Stop-bit

Input message: (Data & Status)

BIO-lines:



DIN,STD		Any 7-bits code
OER,DRD	DRI	0 0 0 0 0 0 0
SER		0 0 0 0 0 1 1
NAK_{out}		0 0 0 0 1 0 1
ACK_{out},ACK_{int}		0 0 0 0 1 1 1
ABC_{+}		0 0 0 1 0 0 0
ABC_{-} (=LRC error)		0 0 0 1 0 1 0
ABC_{-} (=VRC error)		0 0 0 1 1 0 0
ABC_{-} (=LRC & VRC)		0 0 0 1 1 1 0

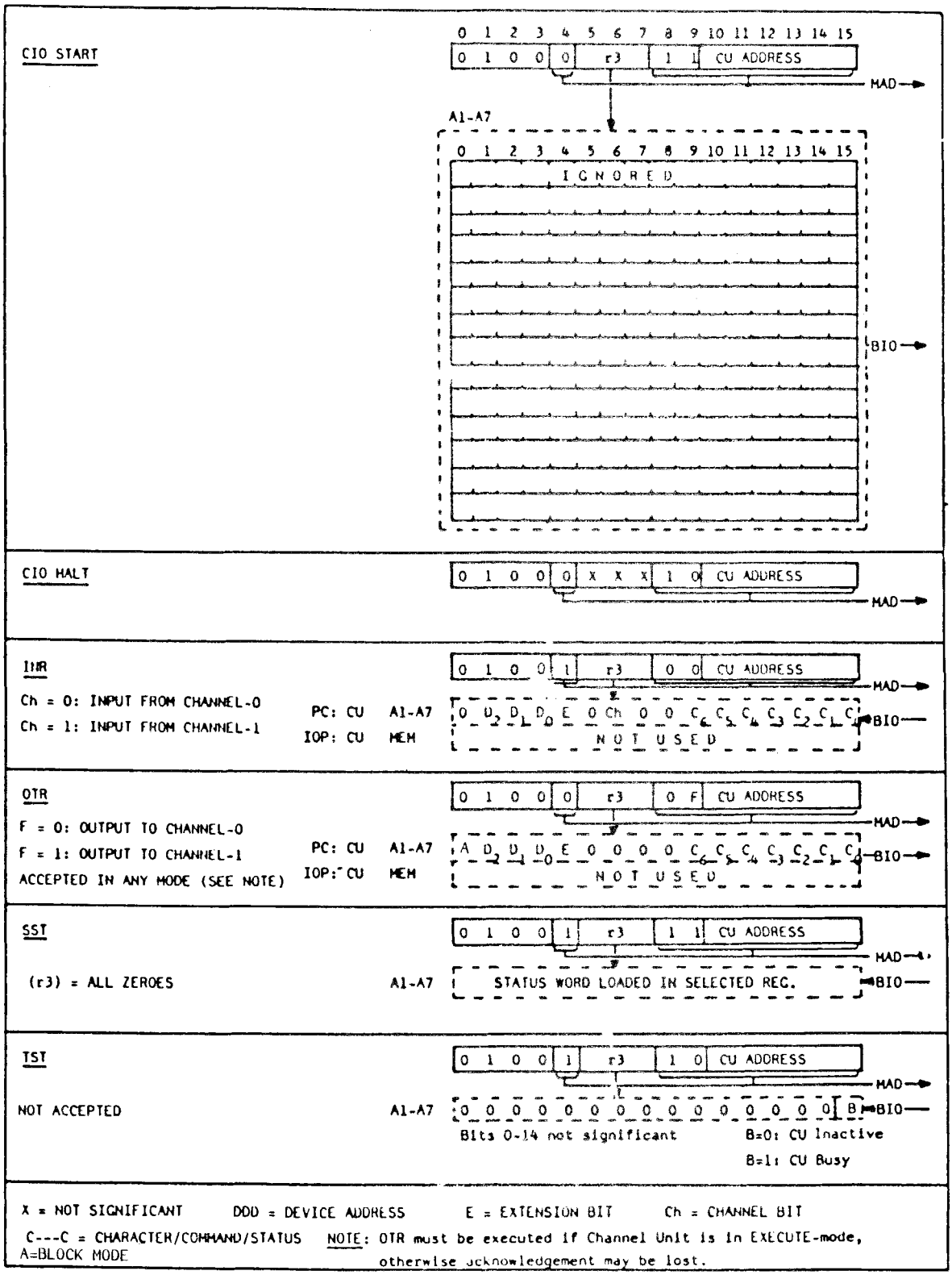
——Input message measured on the 104 line:

	ST	d	D_0 D_1 D_2	E	C_0 C_1 C_2 C_3 C_4 C_5 C_6	P	SP	SP
DIN	0	0	1--7	E	DATA	P	1	1
STD	0	0	1--7	E	STATUS	P	1	1
DRD	0	0	1--6	E	0 0 0 0 0 0 0	P	1	1
ABC *)	0	0	0 0 0	E	/08,/0A,/0C,/0E	P	1	1
SER	0	0	0 0 0	E	1 1 0 0 0 0 0	P	1	1
OER is generated by Channel Unit								

*) Value of the C--C field must be read reversed

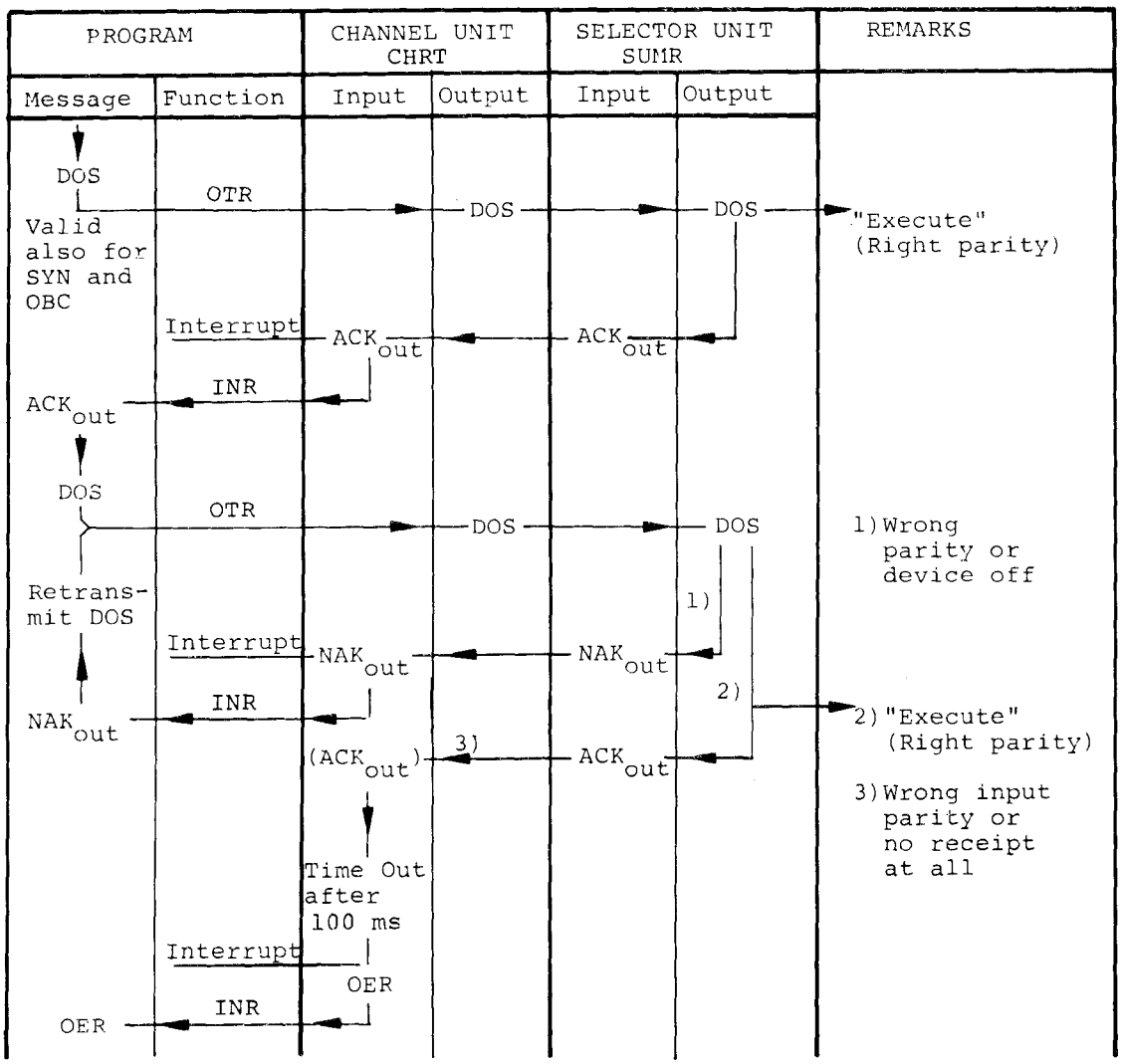
——Input Receipt message measured on the 104 line:

	ST	d	D_0 D_1 D_2	E	P	SP SP
ACK_{out}	0	1	1 1 1	E	P	1 1
NAK_{out}	0	1	0 0 0	E	P	1 1
DRI	0	1	1---6	E	P	1 1
ACK_{int}	Generated by Channel Unit					

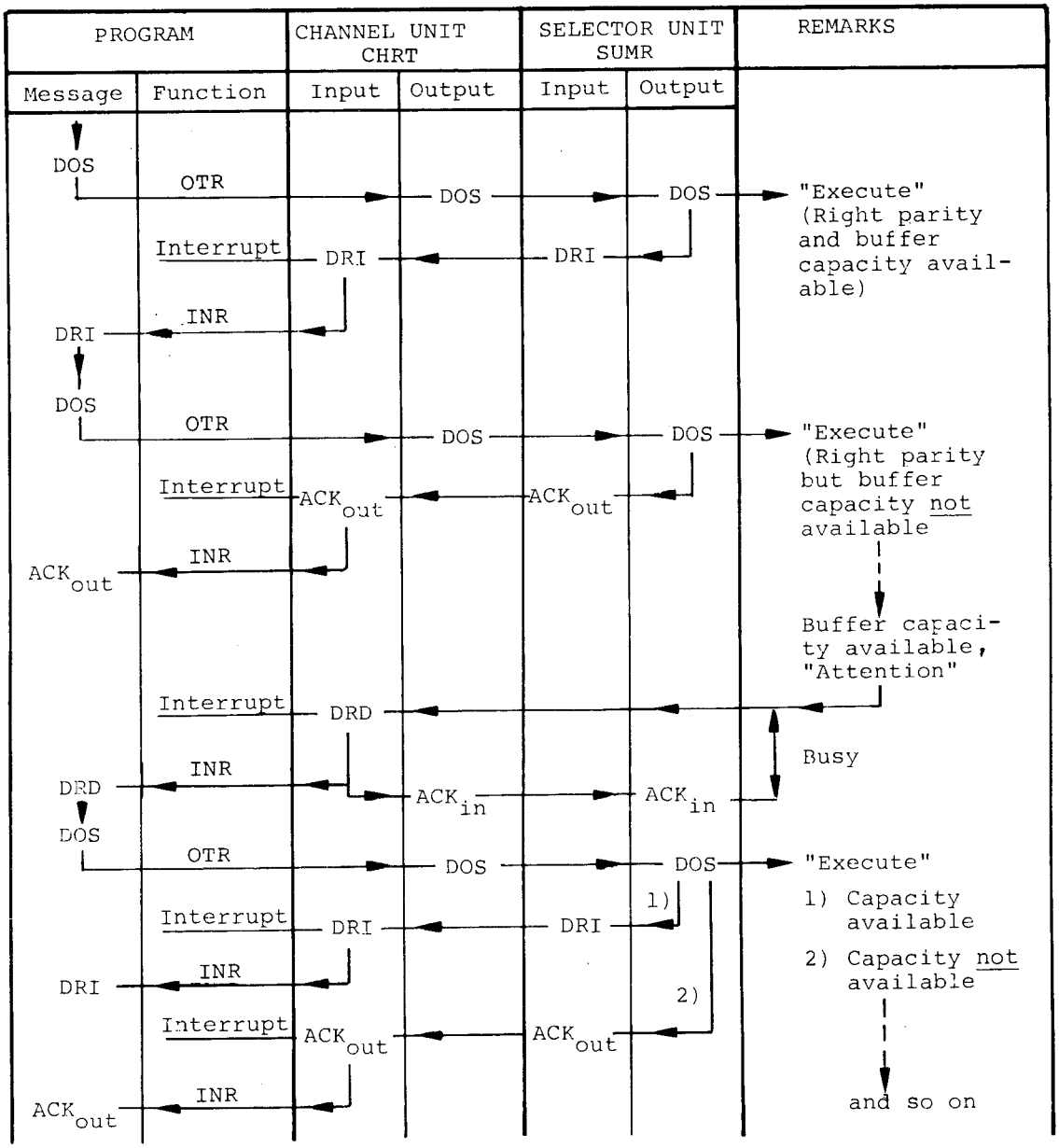


INSTRUCTION-/COMMAND-WORD FORMATS CHRT

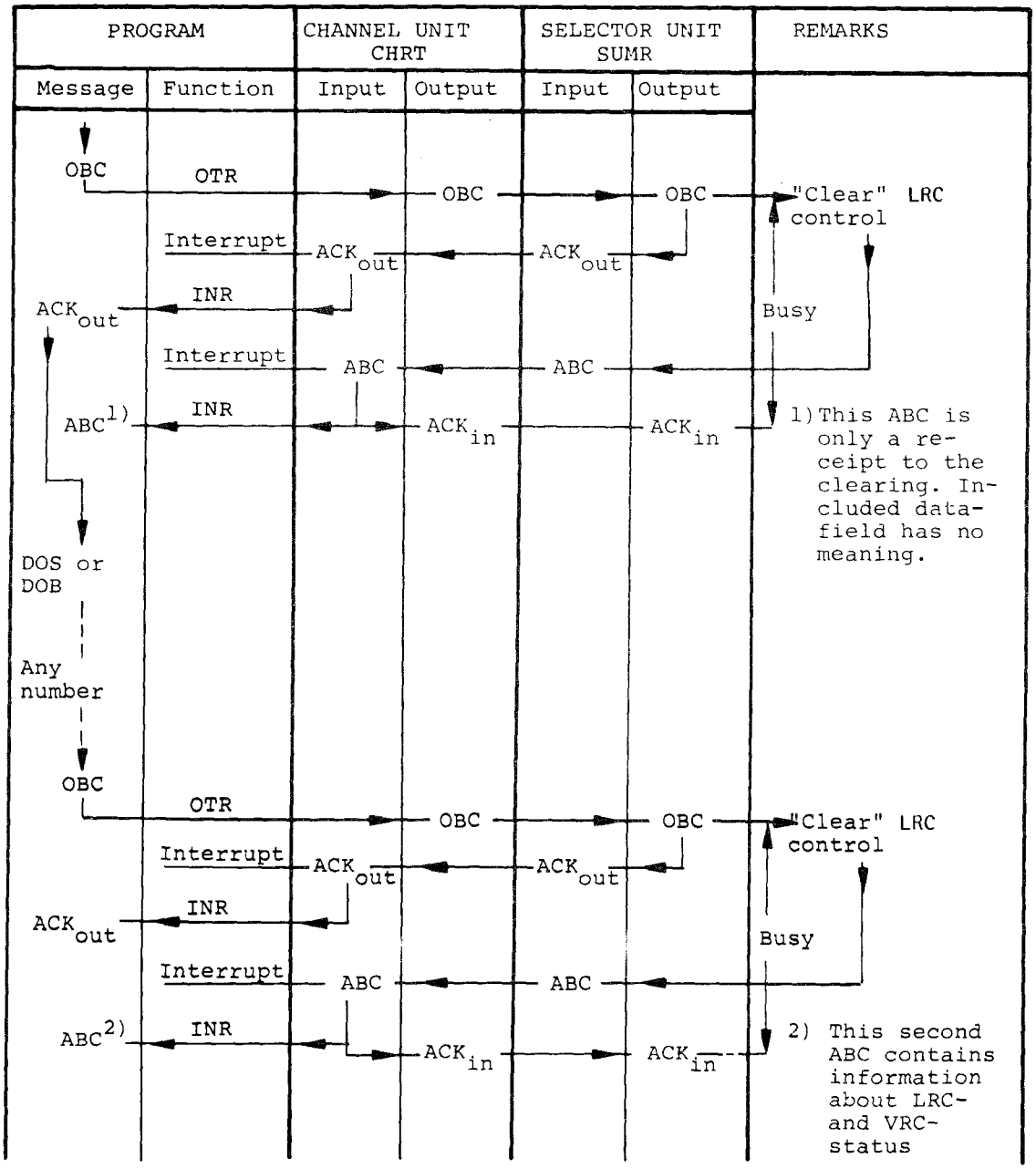
Characterwise output procedure, without data request



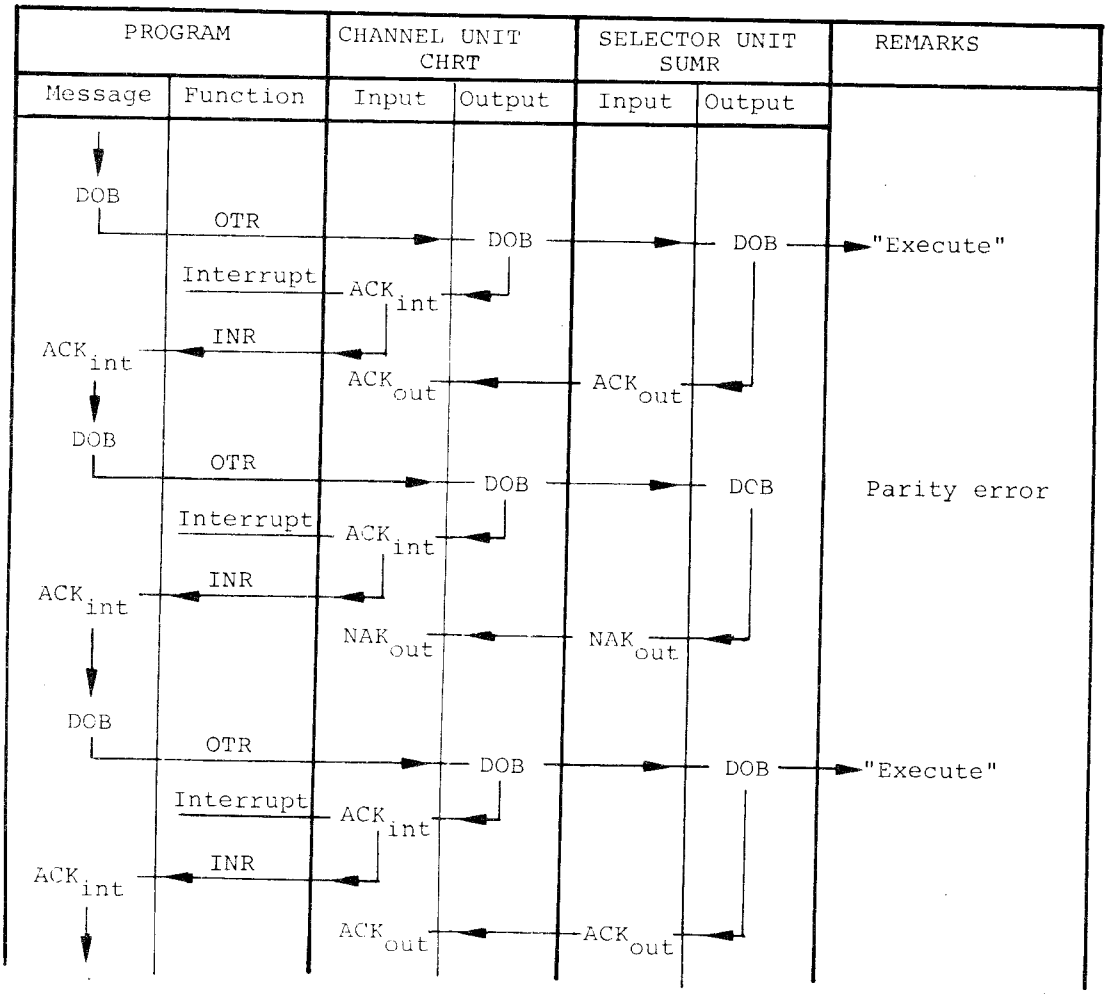
Characterwise output procedure, controlled by data request



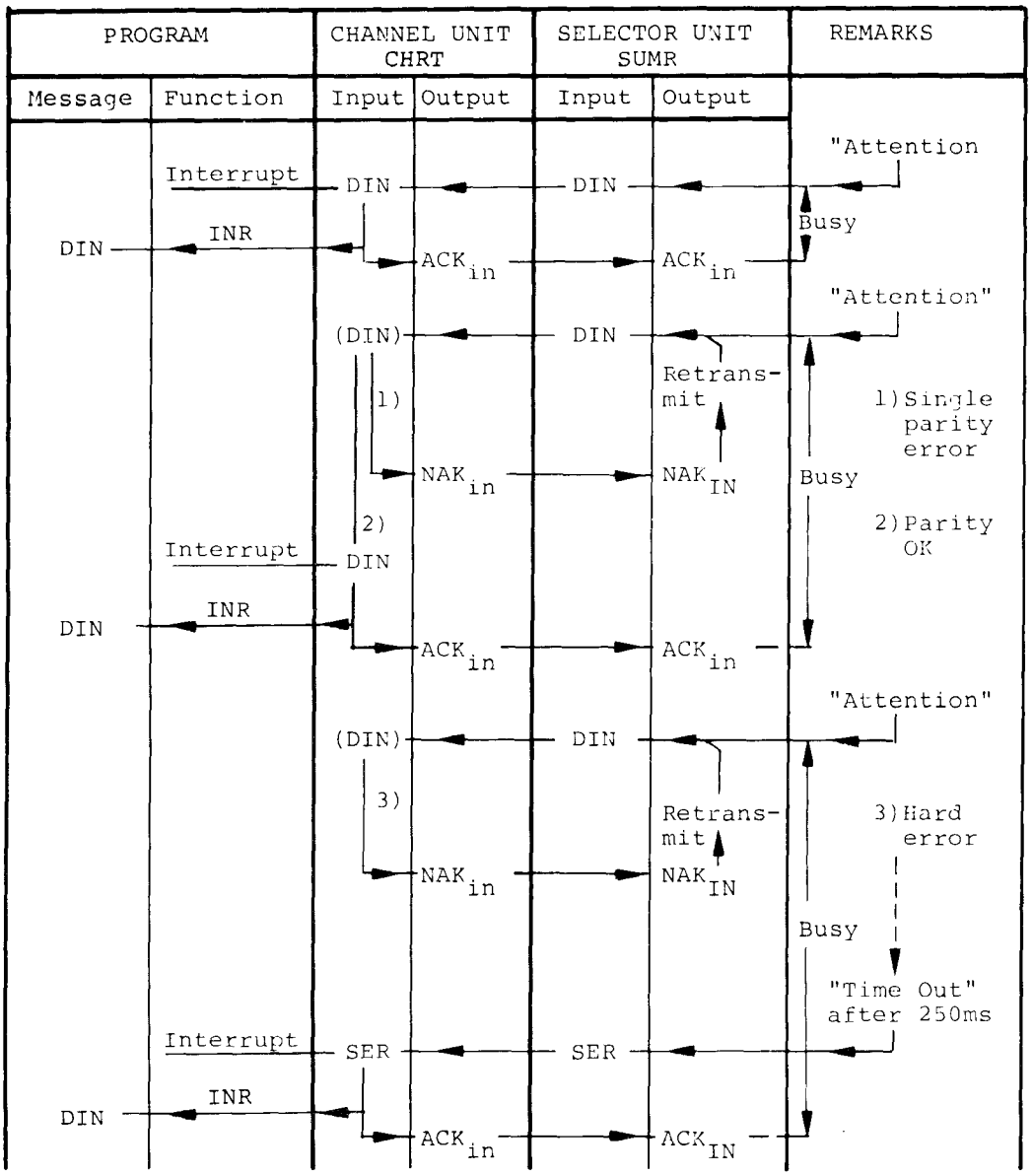
Output procedure, with OBC–ABC



Block output procedure



Characterwise input procedure



MESSAGE TERMS

The procedures are described by use of flow charts and the functions are named as follows:

. SYNC	Synchronization character	Output format used for maintenance of bit synchronization at a channel requiring that (modem V23)
. DOS	Data output, single character	Data to output device, characterwise acknowledge
. DOB	Data output, blockwise	Data to output device, blockwise acknowledged
. DIN	Data input, single char.	Data from input device,
. STD	Device status	Status information from input or output device
. OER	Output error	A message generated in CHRT and sent to CPU if a characterwise output is not received by ACK_{out} NAK_{out} or DRI within 100 ms
. SER	Selector unit error	Status information sent from SUMR when it is in normal function again after power failure or time-out (250 mS)

• DRD	Data request delayed	Data request from output device.
• DRI	Data request immediate	Means ACK_{out} of an output data format and request for a new character to addressed device.
• ACK_{in}	Acknowledge input	Positive acknowledgement of a data input to CHRT
• NAK_{in}	Not acknowledge input	Negative acknowledgement of a data input to CHRT
• ACK_{out}	Acknowledge output	Positive acknowledgement of a data output to SUMR
• NAK_{out}	Not acknowledge output	Negative acknowledgement of a data output to SUMR
• $ACK_{int.}$	Internal acknowledge output	At block output transmission this ACK is generated by the CHRT itself for each transmitted data character in block-mode (A=1). ACk_{int} is equal to ACk_{out}
• OBC	Output block control	This message reads and clears the LRC-logic in SUMR. OBC is used both as start and stop message in as well characterwise as in block transmission. The LRC-SUM calculated by the software must be included in the stop OBC to be compared in SUMR with hardware calculated LRC-SUM.
• ABC	Acknowledge block control	The answer to an OBC-message. ABC contains information about the VRC- and LRC-status in SUMR

19.5 SHORT DESCRIPTION OF TEST-PROGRAM

The CHRT can be tested only in combination with a Terminal, connected either direct or via a Transfer Unit, by means of test-program TERTST. In case a Transfer Unit is used, and activating the Test-switch in this unit, output data can be transferred directly back to the Channel Unit. In this case, the E-bit in the output message must be 0. To execute the test-program, see detailed description.

19.6 SHORT ROUTINES

```
         DATE  82-05-12        IDENT    KBINPR


0000                           IDENT    KBINPR
0001                    *DATE: 820507 FOR PTS
0002                    *PROGRAM FOR INPUT FROM EG A KEYBOARD
0003                    *ON REMOTE AND KEY-CODE DISPLAY ON SOP
0004                           AORG     /80
0005
0006 0080 FFFF 0000            DATA     /FFFF,0
0007 0084 20BF          START  INH                          NO INTERRUPTS
0008 0086 41C1                 CIO      A1,1,1             START CHRT
0009 0088 4A01          INR    INR      A2,0,1             READ KEY
0010 008A 5C04                 RB(NA)   *-2
0011 008C 422E                 OTR      A2,0,/2E           DISPLAY ON SOP
0012 008E 5F08                 RB       INR
0013                           END      START


            SYMBOL TABLE

   INR     0088  A   START   0084  A

            ASS.ERR.    0000
 :EOF
 PROG ELAPSED TIME:  00H-00M-00S-000MS-
```

```
         DATE  82-05-11          IDENT    KBVDUR


0000                             IDENT    KBVDUR
0001                    *DATE: 82 05 07 FOR PTS
0002                    *PROGRAM FOR INPUT FROM KEYBOARD(DA=1) AND OUTPUT ON
0003                    *VDU(DA=4)ON CHRT1
0004                             AORG     /80
0005
0006 0080 FFFF 0000              DATA     /FFFF,0
0007 0084 20BF          START    INH                          NO INTERRUPTS
0008 0086 41C1                   CIO      A1,1,1              START CHRT
0009 0088 0500          ACC      LDK      A5,0                SET OTR ACCEPTED
0010 008A 4A01          IN       INR      A2,0,1              WAIT FOR INPUT
0011 008C 5C04                   RB(NA)   IN
0012 008E 8514                   LDR      A5,A5               IS OTR ACCEPTED?
0013 0090 5002                   RF(Z)    *+4                 YES
0014 0092 820C                   LDR      A2,A3               NO SEND PREVIOUS CHAR
0015 0094 8308                   LDR      A3,A2               FOR ANSWER TO KEYBOARD
0016 0096 A320 FOFF              ANKL     A3,/FOFF            TAKE OUT E AND CH
0017 009A EB20 0007              CWK      A3,7                IS IT ACK?
0018 009E 501C                   RF(E)    NEXT                NOT TO KEYBOARD
0019 00A0 8308                   LDR      A3,A2               REPAIR E AND CH
0020 00A2 0102                   LDK      A1,2                SET CH 1
0021 00A4 3BC6                   SLC      A3,6                IS IT CH0
0022 00A6 5202                   RF(N)    *+4
0023 00A8 0100                   LDK      A1,0                SET CH0
0024 00AA 3BE6                   SRC      A3,6                REPAIR A3
0025 00AC A320 0FFF              ANKL     A3,/FFF             TAKE OUT DA
0026 00B0 9320 1000              ADKL     A3,/1000            PUT IN KEYB AD
0027 00B4 F045 00D4              EX       OTRK,A1             SEND TO KEYBOARD LAMPS
0028 00B8 4C01                   INR      A4,0,1              GET ANSWER
0029 00BA 5C04                   RB(4)    *-2
0030      00BC          NEXT     EQU      *
0031 00BC 422E                   OTR      A2,0,/2E            DISPLAY REC.MES ON SOP
0032 00BE 3AC3                   SLC      A2,3                CHECK IF KEYBOARD INPUT
0033 00C0 5E38                   RB(NN)   IN
0034 00C2 3AE3                   SRC      A2,3                REPAIR A2
0035 00C4 9220 3000              ADKL     A2,/3000            ADD DA FOR VDU
0036                                                         WHEN /3000 IS CHANGED TO OTHER VALUE
0037                                                         OUTPUT IS DONE ON OTHER DEVICE
0038 00C8 F045 00D8              EX       OTR,A1              OUTPUT
0039 00CC 5402                   RF(4)    *+4                 OTR NOT ACC
0040 00CE 5F48                   RB       ACC                 OTR ACCEPTED
0041 00D0 0501                   LDK      A5,1                SET NOT ACCEPTED
0042 00D2 5F4A                   RB       IN
0043 00D4 4301          OTRK     OTR      A3,0,1              OUTP KB CH 0
0044 00D6 4341                   OTR      A3,1,1              OUTP KB CH 1
0045 00D8 4201          OTR      OTR      A2,0,1              OUTP DEV CH 0
0046 00DA 4241                   OTR      A2,1,1              OUTP DEV CH 1
0047
0048
0049                    *        BY CHANGING /3000 TO OTHER VALUE:
0050                    *        OUTPUT CAN BE DONE ON AN OTHER DEVICE
0051                    *EG:     FOR TEP 71
0052                    *        CHANGE TO /1000
0053                    *        TYPE FROM KEYBOARD: /0D,/11,'IT WORKS',/06
0054                    *        AND IT WORKS IS WRITEN ON THE YOURNAL.
0055                    *        TYPE /0F AND THE PRINTERTEST STARTS
0056                    *        TYPE /0C AND THE TEST STOPS
0057
0058
0059                             END      START


          SYMBOL TABLE

  ACC     0088  A   IN      008A  A   NEXT    00BC  A   OTR     00D8  A
  OTRK    00D4  A   START   0084  A

          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-15S-500MS-
```

```
          DATE  82-08-12        IDENT    TEPREM


0000                              IDENT    TEPREM
0001                     *DATE: 820812 FOR PTS
0002                     *TEPREM IS A PROGRAM THAT PRINTS LINES OF
0003                     *CHARACTERS ABCDEFG ON JOURNAL
0004                     *
0005                     *OF TEP 71
0006 0000                         RES      /40
0007
0008 0080 FFFF                    DATA     /FFFF
0009 0082 0000                    DATA     0
0010 0084 20BF                    INH                          NO INTERRUPTS
0011 0086 8220 00F4 R             LDKL     A2,DATBUF           ADDR OF DATABUFFER
0012 008A 41C1                    CIO      A1,1,1              START CHRT
0013 008C 4B01           INR      INR      A3,0,1              MESSAGES
0014 008E 5C04                    RB(4)    INR
0015                     *FIND OUT WHAT MESSAGE IS GIVEN
0016 0090 EB21 0707               CCK      A3,/0707            IS IT ACK?
0017 0094 5030                    RF(E)    NEXT                THEN PRINT NEXT CHARACTER
0018 0096 EB21 0505               CCK      A3,/0505            IS IT NACK?
0019 009A 5034                    RF(E)    PREV                PRINT LAST CHAR AGAIN
0020 009C EB21 0303               CCK      A3,/0303            IS IT POWER FAIL?
0021 00A0 5010                    RF(E)    LDR                 THEN LOAD LINENUMBER
0022 00A2 EB21 0000               CCK      A3,0                WAS IT OUTPUT ERROR
0023 00A6 5028                    RF(E)    PREV
0024                                                           AND START PRINTING ON THIS LINE
0025 00A8 432E                    OTR      A3,0,/2E            DISPLAY ANY OTHER MESSAGE ON SOP
0026 00AA 3BC2                    SLC      A3,2                IS IT PRINTER STATUS?
0027 00AC 5602                    RF(NN)   *+4                 YES THEN STOP
0028 00AE 5700                    RF       *+2                 REPLACE BY /207F FOR STOP ON
0029                                                           STATUS MESSAGE FROM TEP
0030 00B0 5F26                    RB       INR
0031                     *LOAD LINENUMBER FROM FOWERFAIL MESSAGE
0032                     *AND PUT IN DEVICE ADDRESS AND FIND OUT CHANNEL
0033 00B2 840C           LDR      LDR      A4,A3
0034 00B4 9420 2000               ADKL     A4,/2000
0035 00B8 0102                    LDK      A1,2                SET CH1
0036 00BA 3BC6                    SLC      A3,6                IS IT CH 1
0037 00BC 5202                    RF(N)    *+4
0038 00BE 0100                    LDK      A1,0                NO SET CH0
0039 00C0 8220 00F4 R             LDKL     A2,DATBUF
0040 00C4 5706                    RF       LCR
0041      00C6           NEXT     EQU      *
0042 00C6 EA20 0100 R             CWK      A2,BUFEND           IS IT FINISHED?
0043 00CA 5610                    RF(NL)   AGAIN              YES,THEN NEXTLINE ON JOURNAL
0044 00CC E428           LCR      LCR      A4,A2               LOAD CHARACTER
0045 00CE 5702                    RF       *+4
0046 00D0 1A01           PREV     SUK      A2,1
0047 00D2 F045 0100 R             EX       OTR,A1              WRITE CHARACTER
0048 00D6 5C4C                    RB(4)    INR
0049 00D8 1201                    ADK      A2,1
0050 00DA 5F50                    RB       INR                 GET ANSWER
0051 00DC 8520 0500      AGAIN    LDKL     A5,/500             TIME DELAY AFTER 1 LINE
0052 00E0 8620 0100      TIMDEL   LDKL     A6,/100
0053 00E4 1E01                    SUK      A6,1
0054 00E6 5C04                    RB(NZ)   *-2
0055 00E8 1D01                    SUK      A5,1
0056 00EA 5C0C                    RB(NZ)   TIMDEL
0057 00EC 5700                    RF       *+2                 CAN BE CHANGED TO HLT /207F TO
0058                                                           STOP AFTER EVERY LINE
0059                                                           STOP AFTER EVERY LINE
0060 00EE 8220 00F4 R             LDKL     A2,DATBUF           LOAD ADDR DATA BUF
0061 00F2 5F28                    RB       LCR                 GOT PRINT NEXT LINE
0062
0063                     *DATA BUFFER
0064 00F4 0D11           DATBUF   DATA     /0D11               CARIAGE RETURN,LINE FEED
0065 00F6 4142 4344               DATA     'ABCDEFGH'
     00FA 4546 4748
0066 00FE 4906                    DATA     /4906               I AND END OF TEXT
0067      0100           BUFEND   EQU      *
0068 0100 4401           OTR      OTR      A4,0,1              OTR FOR CH 0
0069 0102 4441                    OTR      A4,1,1              OTR FOR CH 1
0070                              END      INR-8


          SYMBOL TABLE

  AGAIN   00DC  R   BUFEND  0100  R   DATBUF  00F4  R   INR     008C  R
  LCR     00CC  R   LDR     00B2  R   NEXT    00C6  R   OTR     0100  R
  PREV    00D0  R   TIMDEL  00E0  R

          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-20S-120MS-
```

20.1 CHDU-IDENTIFICATIONS

Type-number: PTS6844, P824-040
Test-programs:

X1215: PERTST, CDDTSC
X1216:

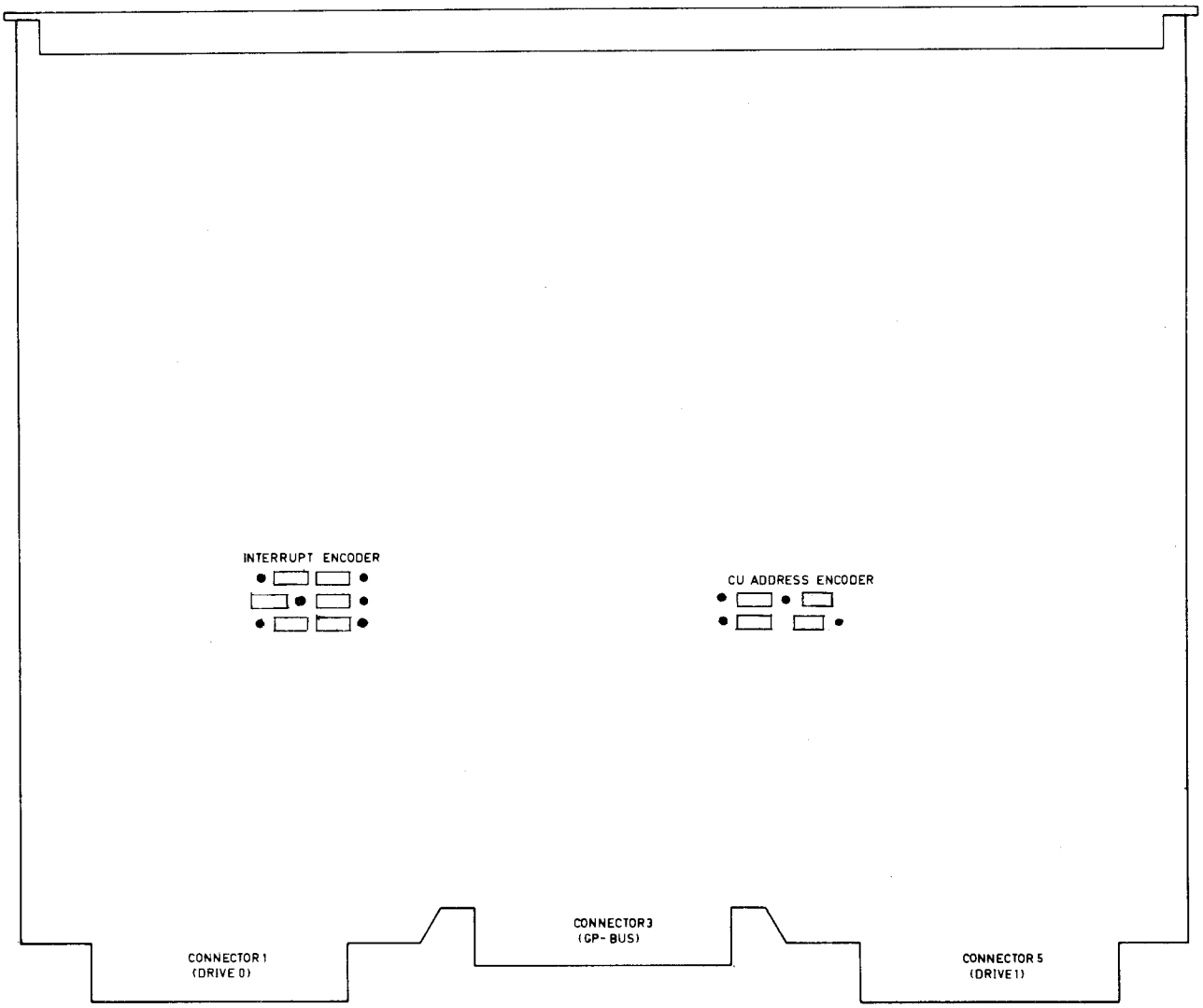
Channel: Hardware channel MX

Break-connection: 3A43

Devices:

2 x X1215 (2.7 Mb) - PTS6875
2 x X1216 (5.4 mb) - PTS6876

Power-consumption: 5 Volt, 4 Amp.



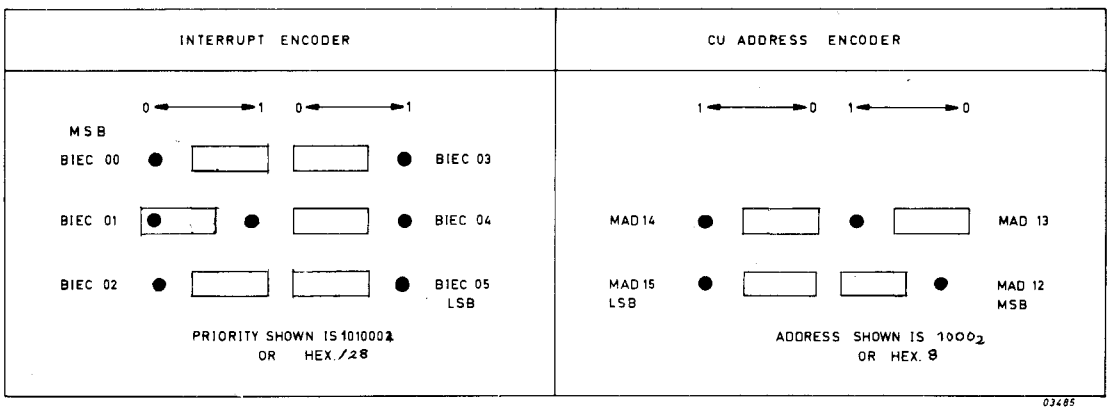


Figure 20.1 ADDRESS AND INTERRUPT ENCODERS

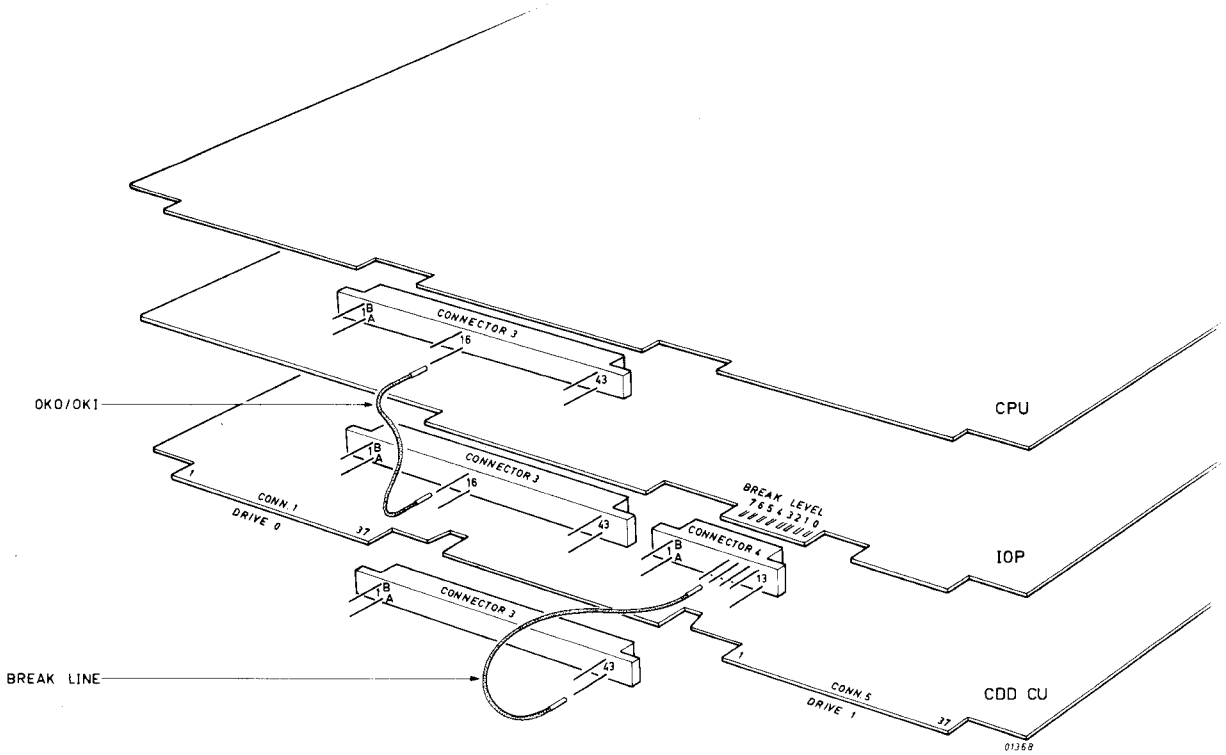
20.3 INTERFACE CONNECTIONS

CONTROL UNIT		DISK DRIVE		
SIGNAL NAME	CONNECTOR PIN	SIGNAL NAME	CONNECTOR PIN	
BUS # 0N	A 25	$\overline{A\ B\ 0}$	48	Lines for cylinder number, CS head selection, HS commands, CTS
SIGNAL GROUND	B 25		51	
BUS # 1N	A 26	$\overline{A\ B\ 1}$	47	
SIGNAL GROUND	B 26		50	
BUS # 2N	A 27	$\overline{A\ B\ 2}$	46	
SIGNAL GROUND	B 27		49	
BUS # 3N	A 13	$\overline{A\ B\ 3}$	54	
SIGNAL GROUND	B 13		57	
BUS # 4N	A 12	$\overline{A\ B\ 4}$	53	
SIGNAL GROUND	B 12		56	
BUS # 5N	A 11	$\overline{A\ B\ 5}$	52	
SIGNAL GROUND	B 11		55	
BUS # 6N	A 35	$\overline{A\ B\ 6}$	60	
SIGNAL GROUND	B 35		64	
BUS # 7N	A 34	$\overline{A\ B\ 7}$	59	
SIGNAL GROUND	B 34		63	
BUS # 8N	A 10	$\overline{A\ B\ 8}$	40	
SIGNAL GROUND	B 10		43	
SEL # N	A 07	$\overline{USL}$	36	unit select
SIGNAL GROUND	B 07		39	
FTCYL # N	A 04	$\overline{C\ S}$	10	cylinder select
SIGNAL GROUND	B 04		13	
FTH # N	A 05	$\overline{H\ S}$	11	head select
SIGNAL GROUND	B 05		14	
FCONT # N	A 33	$\overline{CTS}$	17	control select
SIGNAL GROUND	B 33		21	
WDL # N	A 37	$\overline{WRDA}$	08	write data line
SIGNAL GROUND	B 37		12	
UNSAFE # N	A 03	$\overline{U\ S\ A\ 2}$	34	unit unsafe 2
SIGNAL GROUND	B 03		37	
RER # N	A 02	$\overline{U\ S\ A\ 1}$	03	unit unsafe 1 (rer)
SIGNAL GROUND	B 02		07	
SEC # 0N	A 06	$\overline{S\ P\ C}$	23	sector puls cartr.
SIGNAL GROUND	B 06		26	
SEC # 1N	A 29	$\overline{S\ P\ F}$	30	sector puls fixed
SIGNAL GROUND	B 29		33	
IND # 0N	A 08	$\overline{I\ P\ C}$	24	index puls cartr.
SIGNAL GROUND	B 08		27	
IND # 1N	A 30	$\overline{I\ P\ F}$	35	index puls fixed
SIGNAL GROUND	B 30		38	
RDY # N	A 31	$\overline{U\ R}$	02	unit ready
SIGNAL GROUND	B 31		05	
ONCIL # N	A 32	$\overline{C\ O\ N}$	29	on cylinder
SIGNAL GROUND	B 32		32	
RDL # N	A 36	$\overline{RDDA}$	01	read data line
SIGNAL GROUND	B 36		04	
SEL # N	A 07	$\overline{CUAS}$	58	controller absent
SIGNAL GROUND	B 07		62	
		DRIVE 0	DRIVE 1	
KEY TO SIGNAL NAME: #		0	1	
CONTROL UNIT CONNECTOR		1	5	

CONTROL UNIT to DISK DRIVE INTERFACE CONNECTIONS

Table 20.1 CONTROL UNIT TO DISK DRIVE INTERFACE CONNECTIONS

Example showing the CPU, IOP and Disk CU installed in the CPU cabinet. OKO/OKI connection shown in correct for IOP with address 0. Break line shown is correct for Disk CU with address 8.



BREAK LEVELS	0	1	2	3	4	5	6	7
IOP CONN. 4 B	13	12	11	10	9	8	7	6

Figure 20.1a CONNECTION ON HARDWARE CHANNEL (6810,12,13)

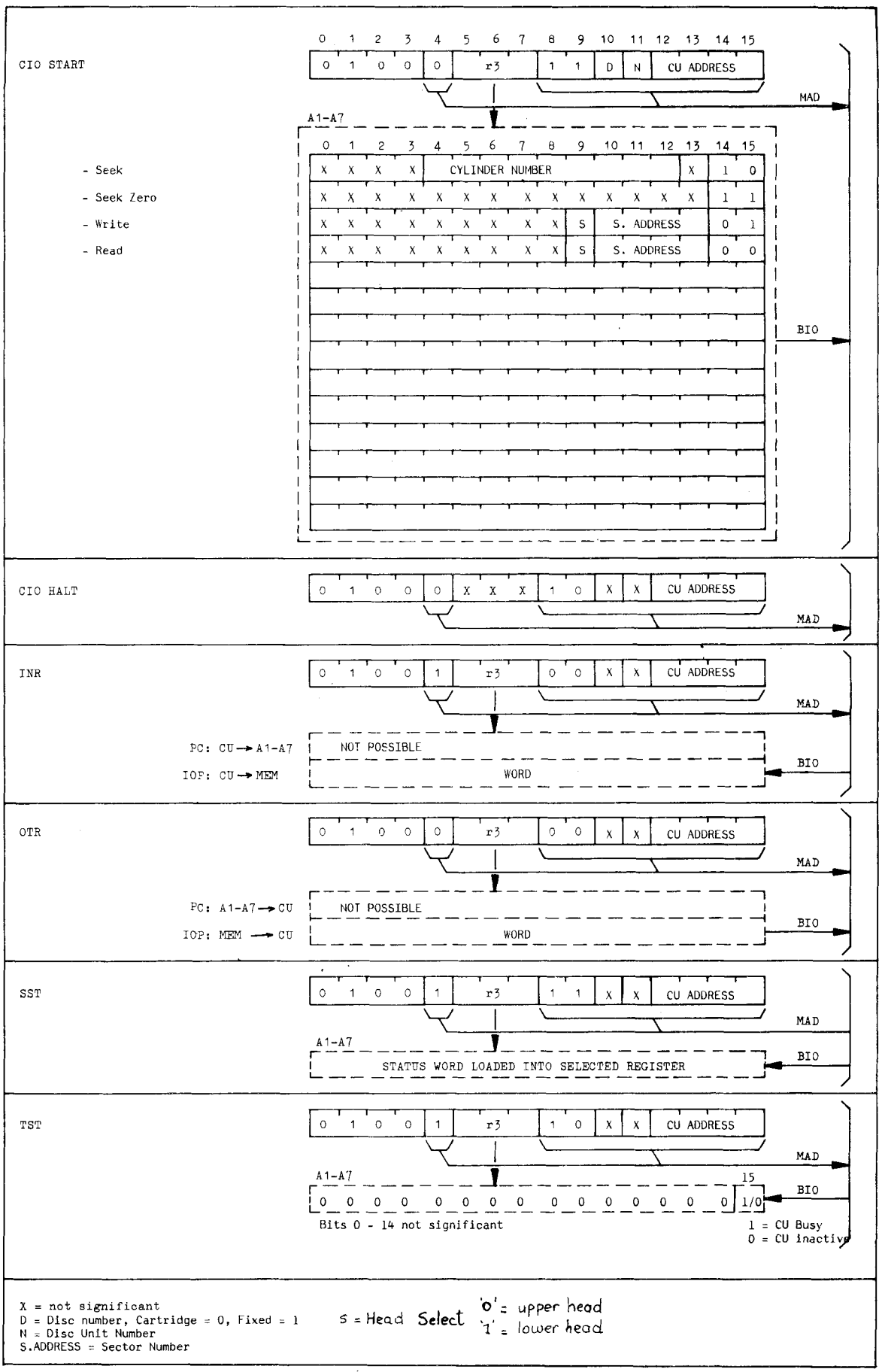
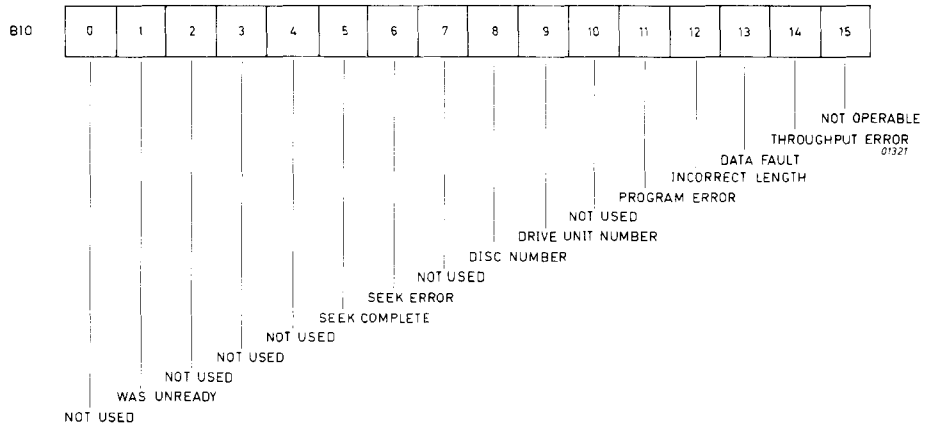


Figure 20.2 INSTRUCTION-/COMMAND-WORD FORMATS

20.4.1 STATUS-WORD



Bit 15 Not operable - is set if the drive (indicated in bit 9) is not operable.

Bit 14 Throughput Error - is set during a write operation if both words in the Input Data Buffer have been written to disc and serialization of the current word is completed before the IOP has answered the exchange data request with an OTR. It is set during a read operation if neither word in the Read Data Buffer have been transferred to memory and deserialization of the current word has ended before the IOP has answered the exchange data request with an INR.

Bit 13 Data Fault - is set when the LRC check fails at the end of a read operation.

Bit 12 Incorrect Length - is set if a read or write operation is incomplete when the start of the next physical sector is detected, by means of the sector pulse.

Bit 11 Program Error - is set if the CU receives an OTR command during a read operation or an INR during a write operation.

Bit 9 Drive Unit Number - is set for drive number 1.

Bit 8 Disc Number - is set for the fixed disc. The disc number is valid only after a read or write operation, after a seek or ready interrupt bit 8 will always be zero.

Bit 6 Seek Error - is set if an error has been detected or the drive becomes inoperable during a seek operation.

Bit 5 Seek Complete - is set if the seek operation is complete whether or not errors were detected.

Bit 1 Was Unready - is set if during scanning a change of status has occured from not operable to operable.

20.5 SHORT DESCRIPTION TESTPROGRAM

Codes: 50 - 59 PERTEST for disc drive 1
60 - 69 for disc drive 2

User instruction

General

Cartridge disc drive test program, CDDTSC, performs a complete test of

- CDD 6875 2 x 2.5 Mbyte
- CDD 6876 2 x 5 Mbyte

The test program can be run on all PTS 6000 computers (except TC6110).

The pre-released version of the CDDTSC is only intended to be a GO/NOGO test of the cartridge or the fix disc. All control and communication facilities are located to the SOP panel to exclude the need of special test system configurations (e g CTW).

The test is power failure proof.

Warning! Use of fix disc test might easily destroy the contents on the disc.

Program loading

The program is available as a stand-alone program on cassette and the loading procedure is as normal, see appendix 1 "PTS 6000 - Program loading". After correct loading the SOP indicator 1 is lit up.

Program initiation

1) Use the SOP panel (see appendix 2) to select if any of the cartridge discs, drive 0 or 1, should be tested.

2) If no test of cartridge disc is selected, it is possible to select test of any of the fix discs, drive 0 or 1.

   Warning! Data on fix disc can easily be destroyed using this test.

3) The program is initiated with the following default values that are normally used:

   Interrupt level = 40 (101000)
   CU address = 8 (not changeable)

   If change of interrupt level is required, input the disc unit interrupt level used in the present system (see appendix 2).

Program execution

4) Start the test (SOP indicator 1 is turned off)

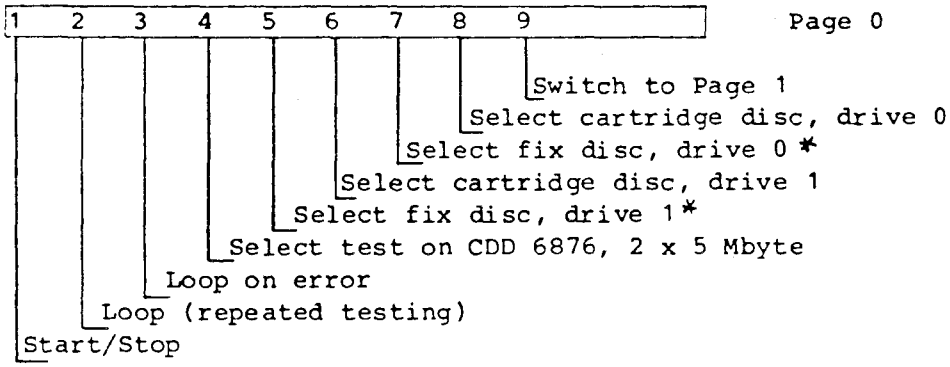
5) If no error is detected, the test will stop after about 10 minutes and SOP indicator 1 will light up again.

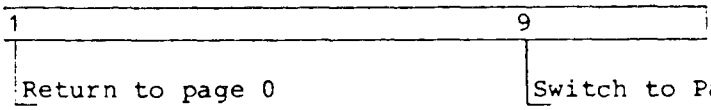
   If an error is detected the testing will stop and the SOP indicators 9-11 will light up. For error description or restart of testprogram see appendix 3 "SOP handling - error condition".

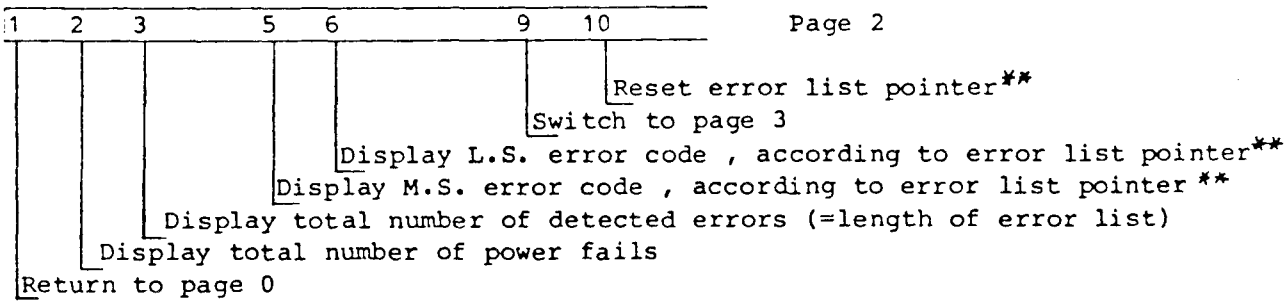
SOP-handling - program execution

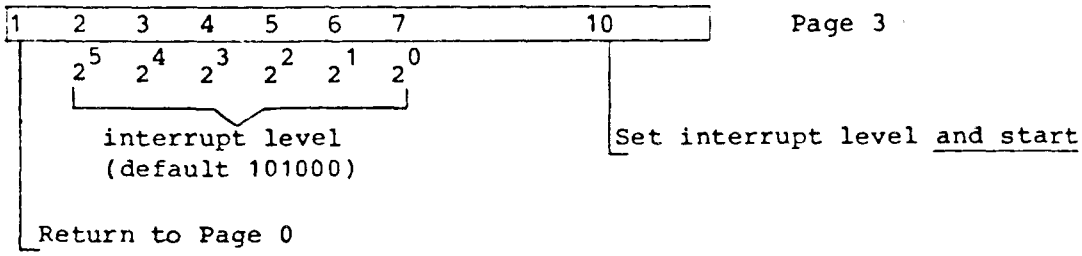
Page 0 is initiated in the following cases:

- after program loading
- after a complete test
- after return command from other pages







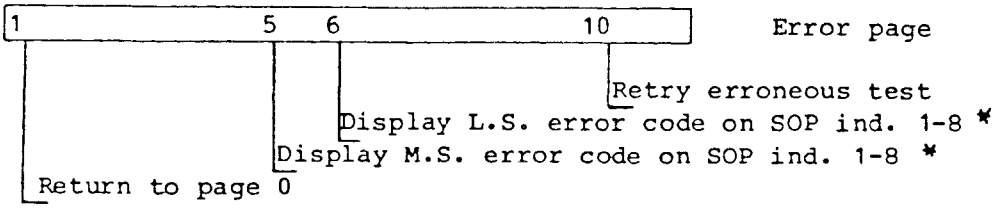


*) Warning! Data on fix disc might be destroyd using fix disc test.

**) All detected errors during the test are logged in an error list. The error codes are the same as used in the old version of CDDTST that includes CTW and CFP.

SOP handling - error condition

When the test program detects an error the SOP indicators 9, 10 and 11 light up. The SOP switches will then have the following function.



*) The error codes are the same as used in the old version of CDDTST that includes CTW and CFP.

20.6 SHORT ROUTINES

```
         DATE  82-05-05        IDENT    SEEK      FOR PTS


0000                           IDENT    SEEK                  FOR PTS
0001                    *DATE: 820505 FOR PTS
0002                    * PROGRAM USABLE INSTEAD OF AN EXERSISER
0003
0004                    *       LOAD START CYLINDER IN REG A1
0005                    *       LOAD LAST CYLINDER IN REG A2
0006                    *       LOAD STEPPING INCREMENT IN REG A3
0007                    *       LOAD TIME DELAY IN REG A6
0008                    *       DISC DRIVE 0 IS ADDRESSED  OTHERWISE CHAGE DEVICE ADDRESSES
0009
0010                           AORG     /80
0011 0080 FFFF                 DATA     /FFFF
0012 0082 0000                 DATA     0
0013 0084 207F          START  HLT
0014 0086 20BF                 INH
0015 0088 8404          CIO    LDR      A4,A1
0016 008A 3C43          CIO1   SLL      A4,3
0017 008C 1402                 ADK      A4,2
0018 008E 44C8                 CIO      A4,1,8
0019 0090 4DC8                 SST      A5,8
0020 0092 5C04                 RB(4)    *-2
0021 0094 E718                 ECR      A7,A6
0022 0096 1F01                 SUK      A7,1
0023 0098 5E04                 RB(6)    *-2
0024 009A ED20 0400            CWK      A5,/400
0025 009E 5002                 RF(0)    CONT
0026 00A0 207F                 HLT                            STATUS ERROR SEE A5
0027 00A2 3C63          CONT   SRL      A4,3
0028 00A4 940C                 ADR      A4,A3
0029 00A6 EC08                 CWR      A4,A2
0030 00A8 5922                 RB(1)    CIO
0031 00AA 5F22                 RB       CIO1
0032
0033                           EJECT
0034                    *EXAMPLE
0035                    *FOR CERTAIN ADJUSTMENTS SEEK FROM 0 TO 64 IN LOOP
0036                    *LOAD THE REGISTERS AS FOLLOWS:
0037                    *       LOAD A1 WITH 0
0038                    *       LOAD A2 WITH 64 DEC = /40
0039                    *       LOAD A3 WITH 64 DEC = /40
0040                    *       LOAD A6 WITH  /40 ( MAX VALUE IN A6 = /80)
0041                    *               (/40= 64 DEC IS ABOUT A DELAY OF 64 MSEC)
0042
0043                    *       LOAD START ADDRESS IN A0
0044                    *       PUSH  MC AND RUN
0045
0046                    *NOTE   WITH INST YOU CAN STOP THE PROGRAM AND IT IS
0047                    *       POSSIBLE TO CHANGE THE PARAMETERS, PUSH RUN AND
0048                    *       THE PRORAM WILL RUN FOR THE CANGED PARAMETERS
0049
0050                           END      START


          SYMBOL TABLE

   CIO     0088  A   CIO1    008A  A   CONT    00A2  A   START   0084  A


          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-13S-340MS-
```

```
         DATE  82-05-05        IDENT    DISKTS


0000                           IDENT    DISKTS
0001                    *DATE: 820505 FOR PTS
0002                    *PROGRAM FOR READING AND WRITING ON DISC
0003                    *PUT THE PATTERN YOU WANT READ AND WRITE IN A5, BEFORE RUNNING THE PROGRAM
0004                    *IF THE PROGRAM STOPS YOU FIND THE WRITTEN WORD IN A3 AND THE READ WORD IN A4
0005                    *IN A2 IS THE POSITION OF THE WORDS IN THE DATA BUFFERS
0006                    *AFTERWARDS YOU FIND THE STATUS IN A6.
0007                    *
0008                    *
0009                           AORG     /80
0010       0008        DA      EQU      /08                  DEVICE ADDR. DISC
0011       0010        ER1     EQU      /10                  FIRST EXTERNAL REGISTER
0012       0011        ER2     EQU      /11                  SECOND EXTERNAL REGISTER
0013                    *
0014                    *MAIN PROGRAM
0015 0080 FFFF                 DATA     /FFFF
0016 0082 0000                 DATA     0
0017 0084 207F          START  HLT
0018 0086 87A0 0780            LDKL     A15,EOS              LOAD STACKPOINTER
0019 008A 8120 00F4            LDKL     A1,INTROU            ADDR. INTERRUPTROUTINE
0020 008E 8141 0050            ST       A1,/50
0021 0092 0200          LOAD   LDK      A2,0
0022 0094 8549 00FA     STORE  ST       A5,DATAIN,A2         WRITE BUFFER
0023 0098 1202                 ADK      A2,2
0024 009A EA20 019A            CWK      A2,/19A
0025 009E 5C0C                 RB(4)    STORE
0026 00A0 8120 C0CD            LDKL     A1,/C0CD             WER CONTROL WORD 1
0027 00A4 7110                 WER      A1,ER1
0028 00A6 8120 00FA            LDKL     A1,DATAIN            WER CONTROL WORD 2
0029 00AA 7111                 WER      A1,ER2
0030 00AC 0101                 LDK      A1,1
0031 00AE 41C8                 CIO      A1,1,DA              START WRITE
0032 00B0 5C04                 RB(4)    *-2
0033 00B2 4F88          WAIT   TST      A7,DA
0034 00B4 EF20 0000            CWK      A7,0
0035 00B8 5C08                 RB(4)    WAIT
0036 00BA 8120 80CD            LDKL     A1,/80CD             WER CONTROL WORD 1
0037 00BE 7110                 WER      A1,ER1
0038 00C0 8120 043A            LDKL     A1,DATAOT            WER CONTROL WORD 2
0039 00C4 7111                 WER      A1,ER2
0040 00C6 0100                 LDK      A1,0
0041 00C8 41C8                 CIO      A1,1,DA              START READ
0042 00CA 5C04                 RB(4)    *-2
0043 00CC 4F88          WAITAG TST      A7,DA
0044 00CE EF20 0000            CWK      A7,0
0045 00D2 5C08                 RB(4)    WAITAG
0046 00D4 0200                 LDK      A2,0
0047 00D6 8348 00FA     TEST   LD       A3,DATAIN,A2         COMPARE WRITE AND
0048 00DA 8448 043A            LD       A4,DATAOT,A2         READ BUFFER
0049 00DE EB10                 CWR      A3,A4                OK?
0050 00E0 540C                 RF(4)    HALT                 NO STOP
0051 00E2 1202                 ADK      A2,2                 YES GO ON
0052 00E4 EA20 019A            CWK      A2,/19A
0053 00E8 5C14                 RB(4)    TEST
0054 00EA 8F20 0092            ABL(7)   LOAD
0055 00EE 207F          HALT   HLT                           DATA ERROR
0056 00F0 8F20 0092            ABL(7)   LOAD
0057                    *
0058                    *INTERRUPT ROUTINE
0059 00F4 4EC8          INTROU SST      A6,DA                AFTERWARDS STATUS IN A6
0060 00F6 5C04                 RB(4)    *-2
0061 00F8 F03E                 RTN      A15
0062
0063
0064 00FA               DATAIN RES      /1A0
0065 043A               DATAOT RES      /1A0
0066 077A               STACK  RES      3
0067 0780               EOS    RES      1
0068                           END      START


          SYMBOL TABLE

   DA       0008  A   DATAIN  00FA  A   DATAOT  043A  A   EOS     0780  A
   ER1      0010  A   ER2     0011  A   HALT    00EE  A   INTROU  00F4  A
   LOAD     0092  A   STACK   077A  A   START   0084  A   STORE   0094  A
   TEST     00D6  A   WAIT    00B2  A   WAITAG  00CC  A

          ASS.ERR.     0000
:EOF
PROG ELAPSED TIME:  00H-00M-17S-860MS-
```

```
         DATE  82-05-05        IDENT    DKPROG

0000                           IDENT    DKPROG
0001                    *DATA: 820505 FOR PTS
0002
0003                    *      THIS PROGRAM TESTS READING AND WRITING ON DISC IN
0004                    *      PROGRAMMED CHANNEL
0005
0006                    ****************TAKE OFF BREAKLINE*****************
0007
0008
0009                    *      LOAD WORD TO WRITE IN REGISTER A2
0010                    *      LOAD START ADDRESS (/0086) IN A0 AND PUSH RUN
0011
0012                           AORG     /80
0013
0014 0080 FFFF                 DATA     /FFFF
0015 0082 0000                 DATA     0
0016                    *      WRITE ROUTINE
0017
0018 0084 207F          START  HLT
0019 0086 20BF                 INH
0020 0088 0101                 LDK      A1,1                 WRITE COMMAND ON SECTOR ZERO
0021 008A 41C8                 CIO      A1,1,8               START CONTROLLER
0022 008C 4208                 OTR      A2,0,8               WRITE A2 CONTENTS ON DISC
0023 008E 5C04                 RB(4)    *-2
0024 0090 4188                 CIO      A1,0,8               STOP CONTROLLER
0025 0092 4CC8                 SST      A4,8                 GET STATUS
0026 0094 5C04                 RB(4)    *-2
0027 0096 207F                 HLT                           CHECK STATUS IN A4
0028                    *                                    SOMETIMES THROUGHPUT ERROR IS GIVEN
0029                    *                                    BECAUSE CIO HALT WAS JUST TO LATE
0030
0031
0032                    *      READ ROUTINE
0033 0098 20BF                 INH
0034 009A 0100                 LDK      A1,0                 READ COMMAND ON SECTOR ZERO
0035 009C 41C8                 CIO      A1,1,8               START CONTROLLER
0036 009E 4B48                 INR      A3,1,8               READ WORD
0037 00A0 5C04                 RB(4)    *-2
0038 00A2 4188                 CIO      A1,0,8               STOP CONTROLLER
0039 00A4 4CC8                 SST      A4,8                 GET STATUS
0040 00A6 5C04                 RB(4)    *-2
0041 00A8 207F                 HLT                           STATUS IN A4
0042                                                         READ WORD IN A3
0043 00AA 5F28                 RB       START
0044
0045
0046                           END      START

            SYMBOL TABLE

    START   0084  A

            ASS.ERR.    0000
  :EOF
  PROG ELAPSED TIME:  00H-00M-11S-540MS-
```

21 CHANNEL UNIT LINE PRINTER/CARD READER

LIST OF ILLUSTRATIONS

LIST OF TABLES

21.1 CHCD-IDENTIFICATIONS

Type-number: PTS6847, P840-003
PTS6843*, P810-040

Test-programs:		
	Line-Printer	PERTST, MLPTSC
	Card-Reader	CRDTST

Channel: Normally MX (Hardware Channel)
PC is possible

Break-connections: LP: 3A43
CR: 3A41

Devices:

LP-CU:	Data Products interface:	
	X-1415, 200 lpm, matrix-line-printer -	PTS6881
	X-1425, 400 lpm, matrix-line-printer -	PTS6882
CR-CU:	Documation M300, 300 cards/min. -	PTS6885

Power-consumption: + 5 Volt, 1,7 Amp.

* 6843 only LP CU on the board

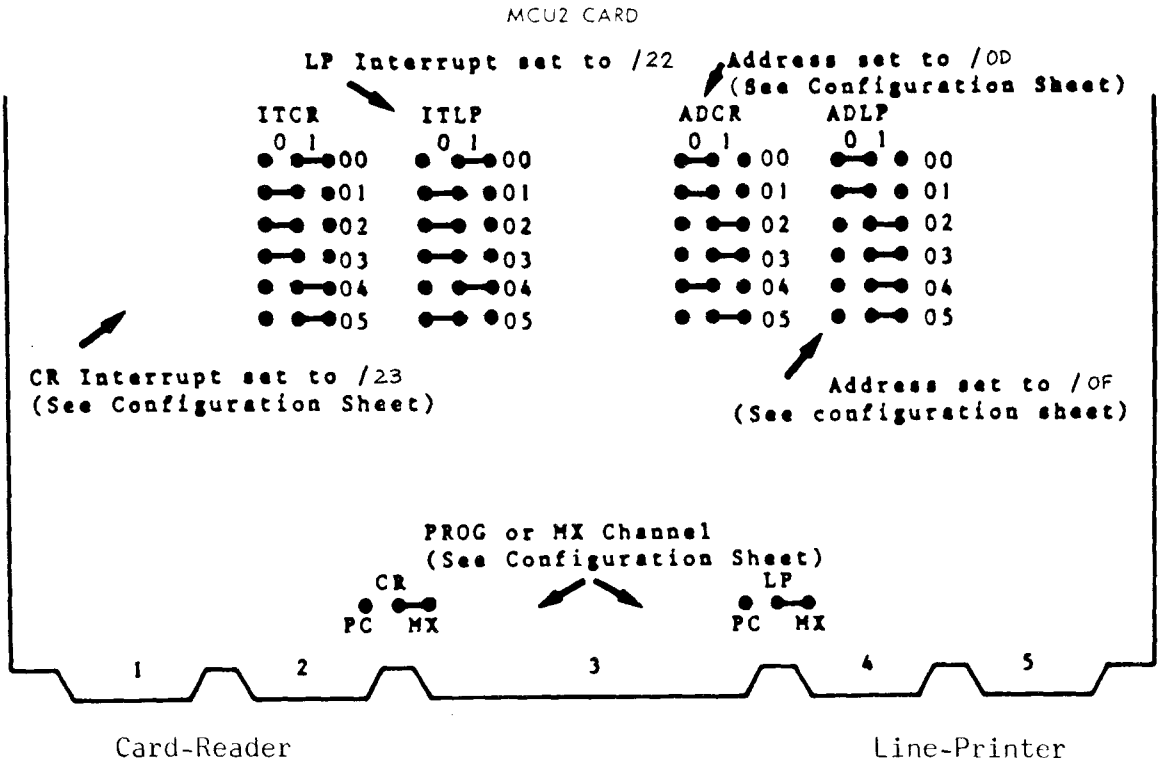


Figure 21.1 STRAP-SETTING

Signal Name	CU Connector	Line Printer Connector
DATA 1	4A06	B
Signal Ground	4B06	D
DATA 2	4A07	F
Signal Ground	4B07	J
DATA 3	4A08	L
Signal Ground	4B08	N
DATA 4	4A09	R
Signal Ground	4B09	T
DATA 5	4A10	V
Signal Ground	4B10	X
DATA 6	4A11	Z
Signal Ground	4B11	b
DATA 7	4A12	n
Signal Ground	4B12	k
PI	4A13	p
Signal Ground	4B13	s
STROBE	5A01	j
Signal Ground	5B01	m
DEMAND	5A11	E
Signal Ground	5B11	C
ONLINE	5A13	y
Signal Ground	5B13	AA

Table 21.1 CU TO LINE-PRINTER CONNECTION

Signal Name	CU Connector	Device Connector
ICL01N	1A10	D
Signal Ground	1B10	J
ICL02N	1A11	K
Signal Ground	1B11	P
ICL03N	1A12	L
Signal Ground	1B12	R
ICL04N	1A13	M
Signal Ground	1B13	S
ICL05N	2A01	N
Signal Ground	2B01	T
ICL06N	2A02	U
Signal Ground	2B02	W
ICL07N	2A03	V
Signal Ground	2B03	X
ICL08N	2A04	Y
Signal Ground	2B04	CC
ICL09N	2A05	Z
Signal Ground	2B05	DD
ICL00N	2A06	C
Signal Ground	2B06	H
ICL11N	2A07	B
Signal Ground	2B07	F
ICL12N	2A08	A
Signal Ground	2B08	E
IDSN	1A04	AA
Signal Ground	1B04	EE
ITRN	1A05	HH
Signal Ground	1B05	NN
IHESFN	1A03	JJ
Signal Ground	1B03	PP
IPFN	1A02	KK
Signal Ground	1B02	RR
IRCN	2A11	LL
Signal Ground	2B11	SS
ICIRN	1A01	MM
Signal Ground	1B01	TT

Table 21.2 CU TO CARD-READER CONNECTIONS

21.4 HARDWARE/SOFTWARE INTERFACE DETAILS

CONTROL UNIT (CU) DATA

MCU2 - LINE PRINTER CU.

DATA and PRINT CONTROL CHARACTER CODE

BIO Lines	08	09	10	11	12	13	14	15
Code Bit Number	P1	7	6	5	4	3	2	1

When the value of P1 is 0 the other seven bits represent either a printable character or a format control character.

VERTICAL FORMAT CONTROL CODE

BIO Lines	08	09	10	11	12	13	14	15
Code Bit Number	P1	7	6	5	4	3	2	1
Logic Value	1	1	X	0	0	Channel Number		

where --

- X is not significant.
- Channel Number indicates the channel number in the paper tape control loop.

BIO Lines	08	09	10	11	12	13	14	15
Code Bit Number	P1	7	6	5	4	3	2	1
Logic Value	1	1	X	1	Number of Lines			

where --

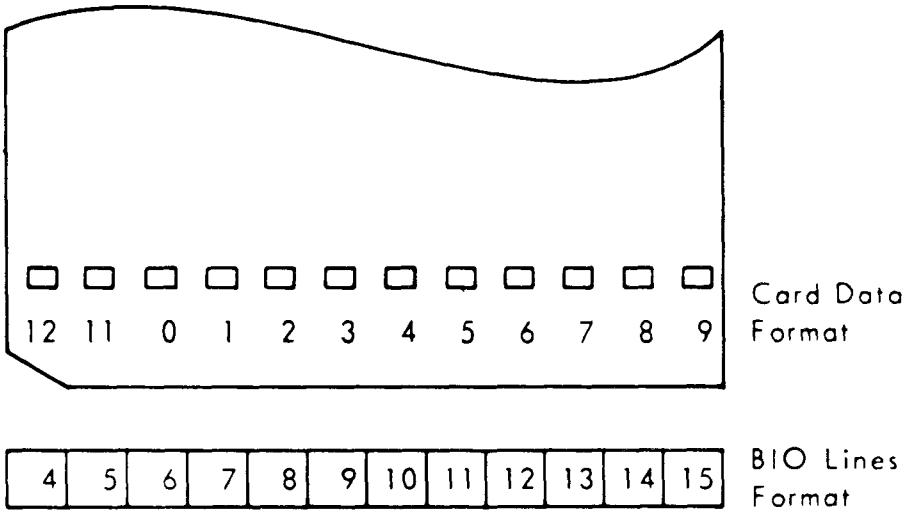
- X is not significant.
- Number of Lines indicates the number of lines to be skipped from 0 to 15.

CHARACTER CODE

			b7	0	0	0	1	1
			b6	0	1	1	0	0
b4	b3	b2	b5 b1	0	0	1	0	1
0	0	0	0		Space	Ø		P
0	0	0	1		!	1	A	Q
0	0	1	0		"	2	B	R
0	0	1	1		#	3	C	S
0	1	0	0		$	4	D	T
0	1	0	1		%	5	E	U
0	1	1	0		&	6	F	V
0	1	1	1		'	7	G	W
1	0	0	0		(	8	H	X
1	0	0	1		)	9	I	Y
1	0	1	0	PF	*	:	J	Z
1	0	1	1		+	;	K	[
1	1	0	0	FF	,	<	L	◇
1	1	0	1	CR	-	=	M	]
1	1	1	0		.	>	N	-
1	1	1	1		/	?	O	♡

- PF Paper Feed: advances the paper one line and prints buffer-contents
- FF Form Feed : advances the paper to the top of the next sheet of paper and prints the buffer-contents
- CR Carriage Return: prints buffer-contents

DATA FORMAT



Note: A hole is a "1".

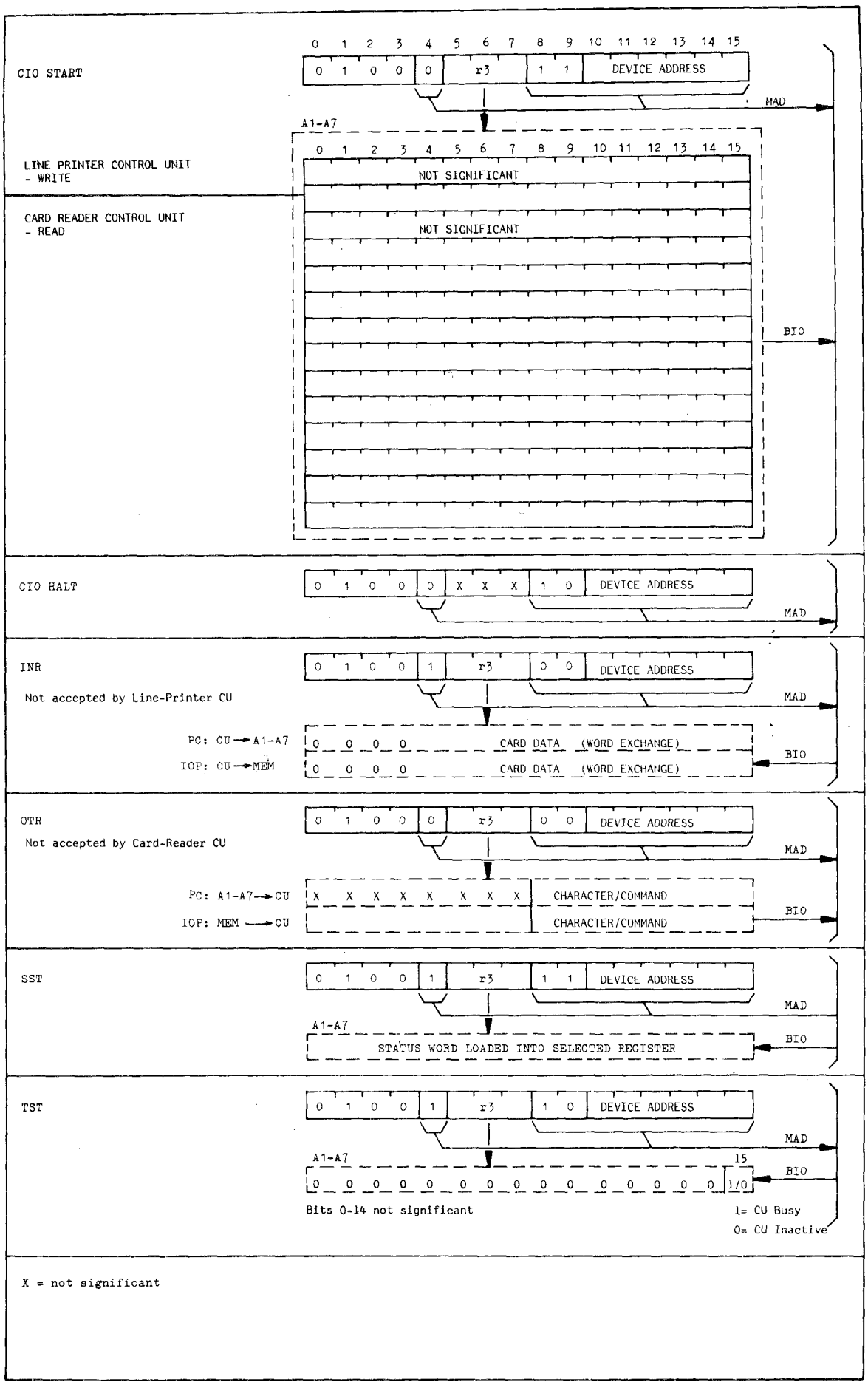


Figure 21.2 INSTRUCTION-/COMMAND-WORD FORMATS

21.4.1 STATUS WORD

LPC-CU

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Not Operable

CR-CU

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	0	0	0		0		0		

Not Operable
Throughput Error
Incorrect Length
Hopper Empty/ Stacker Full

NOT OPERABLE

Bit 15 is set:
- If the Line Printer is inoperable, due to Switched-off/ not On-Line or Paper-Fault.
- If Card Reader is inoperable, due to Switched-off/ not On-Line or Pick-error / Stacker Full / Hopper-Empty.

THROUGHPUT ERROR

Bit 14 is set:
- If a new character is read and the CPU/IOP did not yet answer the data-request Interrupt/Break.

INCORRECT LENGTH

Bit 12 is set:
- If the number of data exchanges by CPU or IOP differs from the number of characters on the card.

HOPPER EMPTY / STACKER FULL

Bit 10 is set:
- If either of these conditions is true.

21.5 SHORT DESCRIPTION TESTPROGRAM

Codes: 90 - 99 PERTST

see detailed description

USER INSTRUCTION

General

Matrix line printer test program MLPTSC performs a complete test of

- PTS 6881 200 l/min
- PTS 6882 400 l/min

The test program can be run on all PTS 6000 computers (except TC 6110).

All control and communication facilities are located to the SOP panel to exclude the need of special test system configuration (CTW, CFP etc).

The test is power failure proof.

Program loading

The program is available as a stand-alone program on cassette and the loading procedure is as normal, see appendix 1 "PTS 6000 - Program loading".

After correct loading the SOP indicator 1 is lit up.

Program initiation

1. Use the SOP panel (see app. 2) to select if the test object is a PTS 6882 line printer. As default a PTS 6881 is assumed.

2. If the printer is connected at programmed channel this must be selected on the SOP. As default MUX channel is assumed.

3. The program is initiated with the following default values that are normally used:

   Interrupt level = 34 (100010)
   CU address = / F (00 1111, not changeable)

   If change of interrupt level is required, input the line printer interrupt level used in the present system (see app. 2).

Program execution

4. Start the test (SOP indicator 1 is turned off)

5. A correct test is as follows:

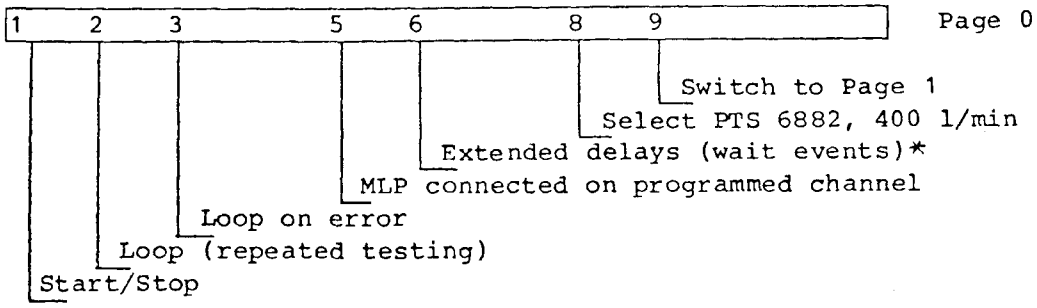
   The printer will print six test patterns preceded by "CHECK 1" to "CHECK 6", see appendix 3 "Printer action". Then SOP indicator 1 is lit up.
   A complete test of the MLP has now been performed except for the status "not operable". For test of this function, see detailed description.

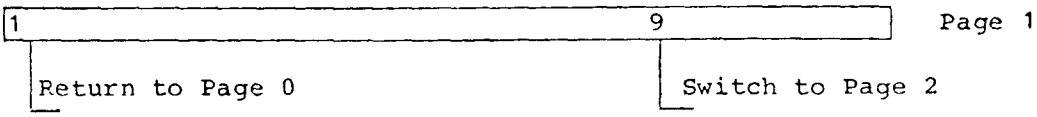
6. If an error is detected by the program this will be displayed on the SOP (see app. 4).
   There is a special service test available for selected testing and measurements. (see detailed description)

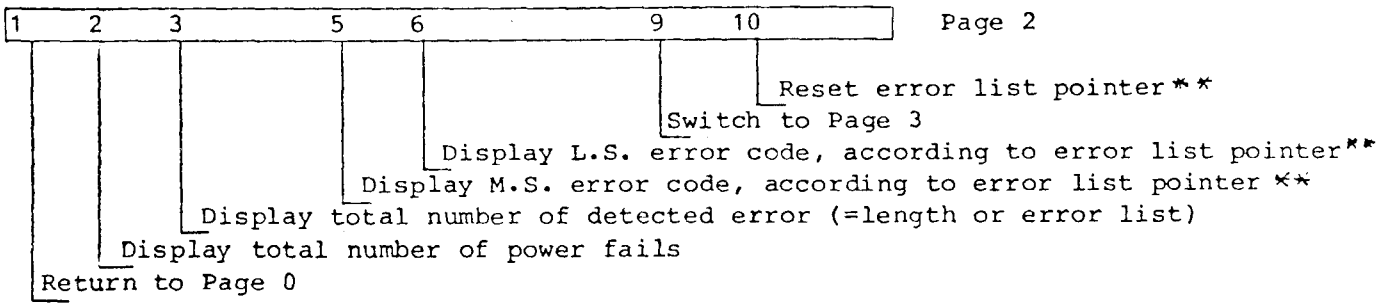
SOP handling - program execution

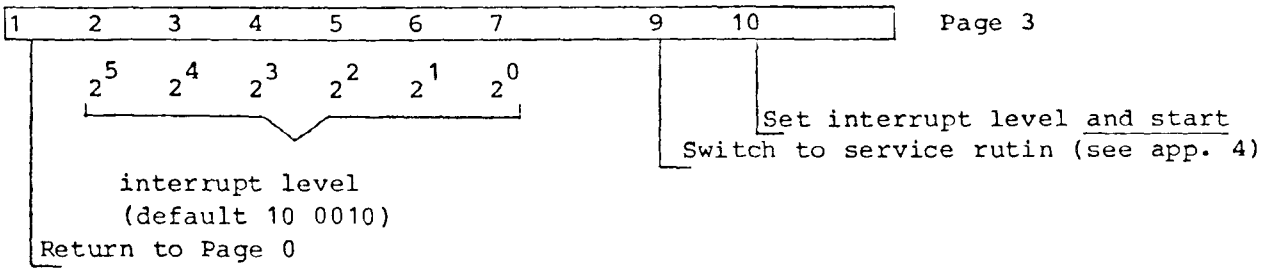
Page 0 is initiated in the following cases:

- after program loading
- after a complete test
- after a return command from other pages







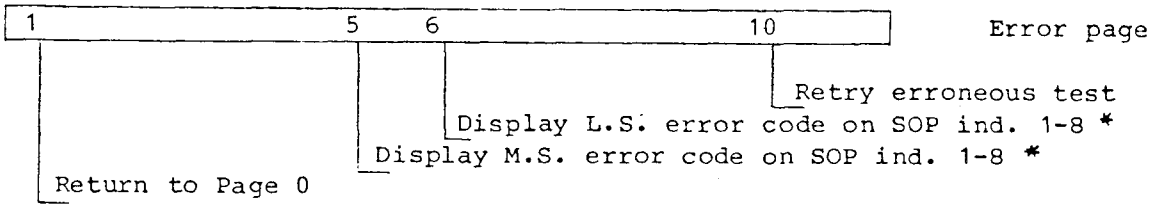


*/ Used to determine if a problem is due to critical timing.

**/ All detected errors during the test are logged in an error list. The error codes are the same as used in the old version of MLPTST that requires CTW and CFP.

SOP handling - error condition

When the test program detects an error the SOP indicators 9, 10 and 11 light up. The SOP switches will then have the following function.



*/ The error codes are the same as used in the old version of MLPTST that requires CTW and CFP.

TESTABLE CONFIGURATION

- PTS 6810 Terminal Computer
- Cassette Drive, or Flexible Disk Drive (FDD) (to load program)
- 4K Memory
- CFP – Customer Full Panel
- Multiplexer PTS 6827
- Card Reader PTS 6885 or Documation M200, M300 or M600
- One Control Peripheral (Console Typewriter)

Program Loading and Normal Running

Set 3 position switch on SOP panel in position 'NO RTC'. – Press IPL
(Run lamp on CFP then lights.)
Load program cassette in recorder (or diskette in FDD).
Depress either:
SW1 (left hand cassette unit or disk drive)
SW2 (right hand cassette unit or disk drive)
Lamp over SW1 or SW2 lights indicating program loading
After loading PGM stops in /700
Set the 3 position switch to 'ON RTC'.
Set:
SHUTDOWN SWITCH POSITION ..... AUTO
MODE SWITCH POSITION ..... REMOTE
POWER SWITCH POSITION ..... ON
Load reference card deck in the Card Reader hopper.
Press RESET on Card Reader.
Press RUN button on CFP (Standard Initialisation)
The program then runs checks 0–6.

Information and error messages are printed out on the Console Typewriter.

When all checks have been completed the program stops in /700 and the card reader hopper is empty.

If the program stops earlier at / 5F0 an error has been detected. (see detailed information)

The operator may at any time stop the program and restart at /700.

Program Modification

A8 Register (standard /8C0D)

Interrupt Level								MUX=0 PC =1	Controller Address						
1	0	0	0	1	1	0	0	0	0	0	0	1	1	0	1

A9 Register (standard /800)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Device Select							X4	OS	CSE	CSP	CED	CSI			
0	0	0	0												

Bit 0 Bit 1 Bit 2 Bit 3	Set to '0' for Card Reader
Bits 4–6	Not used
Bit 7 (X4)	'1' all delays (wait events) multiplied by 4. (This enables us to determine if problem is due to critical timing.)
Bit 8 (One Shot (OS))	'1' program prints out the message 0016 on CTW and stops at /5E0 after each check (selected in reg A10) is executed. Run button must be pressed to execute the next check.
Bit 9 (Clear Stop on Error (CSE))	'1' stop is suppressed at 5E0 in case of error. (An error counter may be read out at address /F2. This counter is reset to zero in case of a restart at /700.)
Bit 10 (Clear Stop on Program (CSP))	'1' stop is suppressed at /700 after one pass of checks selected in A10. Program continues to pass through the checks until the operator stops it by depressing the INST or INT on the control panel. A pass counter may be read at address /F0. This counter is reset to zero in the case of a restart at /700.
Bit 11 (Clear Edition (CED))	'1' error and information messages suppressed on CTW.
Bit 12 (Clear Stop on Information (CSI))	'1' stop at /5E0 before execution of each check is suppressed.
Bits 13–15	Not used

A10 Register (standard FE00)

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
← Check Numbers →										Not Used					
1	1	1	1	1	1	0	0	0	0						

Standard initialized contents /FC00 = bits 0–5 set to '1'

For more information see detailed description

Notes:

LINE PRINTER

This program is written for Programmed Channel operation so if the printer is normally used on the IOP Channel the CU must be connected to operate on the Programmed Channel. The program can be loaded either with the IPL routine or by hand using the switches on the control panel. Once loaded the following routine should be used:

- Load register A6 with the ASCII character to be printed.
- Load register A7 with number of times you want the character printed on each line.
- Load register A0 with the Start address.
- Push the RUN button.

To stop the program push the INST button.

Program LINELP

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	20BF		INH	
0088	0200		LDK	A2,0
008A	4BCF		SST	A3,/0F
008C	42CF		CIO	A2,1,/0F
008E	5C04		RB(NA)	* -2
0090	050A	OUTLF	LDK	A5,/0A
0092	450F		OTR	A5,0,/0F
0094	5C04		RB(NA)	* -2
0096	460F	OUTCH	OTR	A6,0,/0F
0098	5C04		RB(NA)	* -2
009A	1201		ADK	A2,1
009C	EA1C		CWR	A2,A
009E	5C0A		RB(NE)	OUTCH
00A0	0200		LDK	A2,0
00A2	5F14		RB	OUTLF

```
         DATE  82-05-05        IDENT    LPIOP


0000                           IDENT    LPIOP
0001                    *DATE: 820505 FOR PTS
0002                    *
0003                    *
0004                    *        THIS PROGRAM STORES TWO SELECTED CHARACTERS INTO A BUFFER
0005                    *        THEN PRINTS THEM AND STOPS WAITING NEW CHARACTERS TO BE SELECTED
0006                    *
0007                    *
0008      0000          BEGIN    EQU      *
0009                           RORG     BEGIN+/80
0010                    *
0011                    *
0012                    *        LOAD THE TWO CHARACTERS TO BE PRINTED IN REGISTER A3
0013                    *
0014                    *        PUSH THE RUN BUTTON
0015                    *
0016 0080 FFFF                 DATA     /FFFF
0017 0082 0000                 DATA     0
0018 0084 207F          START  HLT
0019 0086 20BF                 INH
0020 0088 850C                 LDR      A5,A3                 LOAD DATA INTO A5
0021 008A 0100                 LDK      A1,0                  CLEAR CHAR COUNTER
0022 008C 8545 00B8 R  REPT    ST       A5,LPBUF,A1           STORE THE CONTENTS OF A5 INTO LPBUF
0023 0090 1102                 ADK      A1,2                  UPDATE LPBUF ADDRESS
0024 0092 E920 00F8            CWK      A1,/F8                AND CHECK IF LINE FULL
0025 0096 5C0C                 RB(NE)   REPT
0026 0098 8520 0D0A            LDKL     A5,/0D0A              LOAD CARRIAGE RETURN LINE FEED CHARS
0027 009C 8545 00B8 R          ST       A5,LPBUF,A1           AND STORE IN LPBUF
0028 00A0 8120 4050            LDKL     A1,/4050              LOAD PARAMS FOR FIRST WER
0029 00A4 711E                 WER      A1,/1E                AND SEND TO IOP
0030 00A6 8120 00B8 R          LDKL     A1,LPBUF              LOAD FIRST ADDRESS OF LPBUF
0031 00AA 711F                 WER      A1,/1F                AND SEND TO IOP
0032 00AC 0600                 LDK      A6,0
0033 00AE 46DF                 CIO      A6,1,/1F              SEND START COMMAND TO PRINTER
0034 00B0 5C04                 RB(NA)   *-2                   TRY AGAIN IF NOT ACCEPTED
0035 00B2 4CDF                 SST      A4,/1F                GET STATUS
0036 00B4 5C04                 RB(NA)   *-2
0037 00B6 5F34                 RB       START                 GO AND WAIT FOR NEW DATA
0038                    *
0039 00B8               LPBUF  RES      80                    OUTPUT BUFFER
0040                           END      START


          SYMBOL TABLE

  BEGIN   0000  R   LPBUF   00B8  R   REPT    008C  R   START   0084  R


          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-10S-640MS-
```

```
        DATE  82-05-05          IDENT    CRPROG


0000                            IDENT    CRPROG
0001                    *DATE: 820505 FOR PTS
0002                    *
0003                    *
0004                    *       THIS PROGRAM READS A CARD VIA THE PROGRAMMED CHANNEL AND STOPS SO THAT
0005                    *       CONTENTS OF THE BUFFER CAN BE CHECKED AGAINST THE PUNCHED HOLES IN THE
0006                    *       CARD
0007                    *
0008      0000          BEGIN   EQU      *
0009                            RORG     BEGIN+/80
0010                    *
0011                    *
0012                    *       LOAD THE CARD(S) TO BE READ INTO THE CARDREADER
0013                    *       AND START THE CARD READER
0014                    *
0015                    *       LOAD START ADDRESS(/0086) IN A0 AND PUSH THE RUN BUTTON
0016                    *
0017 0080 FFFF                  DATA     /FFFF
0018 0082 0000                  DATA     0
0019 0084 207F          START   HLT
0020 0086 20BF                  INH
0021 0088 0200                  LDK      A2,0                   LOAD ZERO IN A2
0022 008A 0100                  LDK      A1,0                   CLEAR WORD COUNTER
0023 008C 8245 00B8 R   STORE   ST       A2,BUFF,A1             STORE ZERO INTO BUFF ADDRESS
0024 0090 1102                  ADK      A1,2                   UPDATE WORD COUNT OF BUFF ADDRESS
0025 0092 E920 002A             CWK      A1,42                  CHECK IF LAST WORD IS REACHED
0026 0096 5C0C                  RB(NE)   STORE                  NO? GO AND STORE THE NEXT WORD
0027 0098 0100                  LDK      A1,0                   CLEAR CHARACTER COUNTER
0028 009A 0601                  LDK      A6,1
0029 009C 46CD                  CIO      A6,1,/D                SEND CIO START COMMAND TO THE CARDREADER
0030 009E 5C04                  RB(NA)   *-2
0031 00A0 4D0D          READ    INR      A5,0,/D                GET CHARACTER FROM CU
0032 00A2 5C04                  RB(NA)   *-2
0033 00A4 8545 00B8 R           ST       A5,BUFF,A1             AND STORE IN BUFFER
0034 00A8 1102                  ADK      A1,2                   UPDATE BUFFER ADDRESS
0035 00AA E920 00A0             CWK      A1,/A0                 CHECK IF LAST COLUMN READ
0036 00AE 5C10                  RB(NE)   READ                   NO? GO AND READ NEXT COLUMN
0037 00B0 468D                  CIO      A6,0,/D                SEND STOP COMMAND TO CU
0038 00B2 4CCD                  SST      A4,/D                  GET STATUS FROM CU
0039 00B4 5C04                  RB(NA)   *-2
0040 00B6 5F34                  RB       START                  GO AND WAIT FOR NEXT RUN
0041                    *
0042 00B8               BUFF    RES      42                     READ BUFFER
0043                            END      START


            SYMBOL TABLE

   BEGIN    0000  R    BUFF     00B8  R    READ     00A0  R    START    0084  R
   STORE    008C  R

            ASS.ERR.     0000
  :EOF
  PROG ELAPSED TIME:  00H-00M-11S-360MS-
```

CARD READER

This program is written to use the IOP channel. If the Card Reader normally operates on the Programmed Channel it will be necessary to connect the Break Request line on the CU. The program will read one card and stop; the data on the card can be checked by displaying the contents of the program buffer, BUFF. Once the program has been loaded either by the IPL routine or by hand using the control panel switches, it is only necessary to load the start address into register A0 and push the RUN button.

Program CRTEST

Memory Address	Data	Program Instructions		
0080	FFFF		Data	/FFFF
0082	0000		Data	0
0084	207F	Start	HLT	
0086	20BF		INH	
0088	8120		LDKL	A1,/8050
008A	8050			
008C	710C		WER	A1,/1A
008E	8220		LDKI	A2,BUFF
0090	009E			
0092	720D		WER	A2,/1B
0094	43C6		CIO	A3,1,/0D
0096	5C04		RB(NA	* -2
0098	4CC6		SST	A4,/0D
009A	5C04		RB(NA)	* -2
009C	5F1A		RB	Start
009E		BUFF		

LIST OF ILLUSTRATIONS

LIST OF TABLES

22.1 CHDU-IDENTIFICATIONS

Type-Number:	PTS6845, P825-040
Testprogram:	BCDC2 for both disc-drives 0,7 usec memory obliged
Channel:	DMA OKI 3B16, OKO 3A16
Devices	2x 80Mb drives, (CDC 9762) PTS 6877 Cartridge 80Mb, (CDC 9877) PTS
Power consumption:	+5V, 8.0 A -5V, 0.4 A

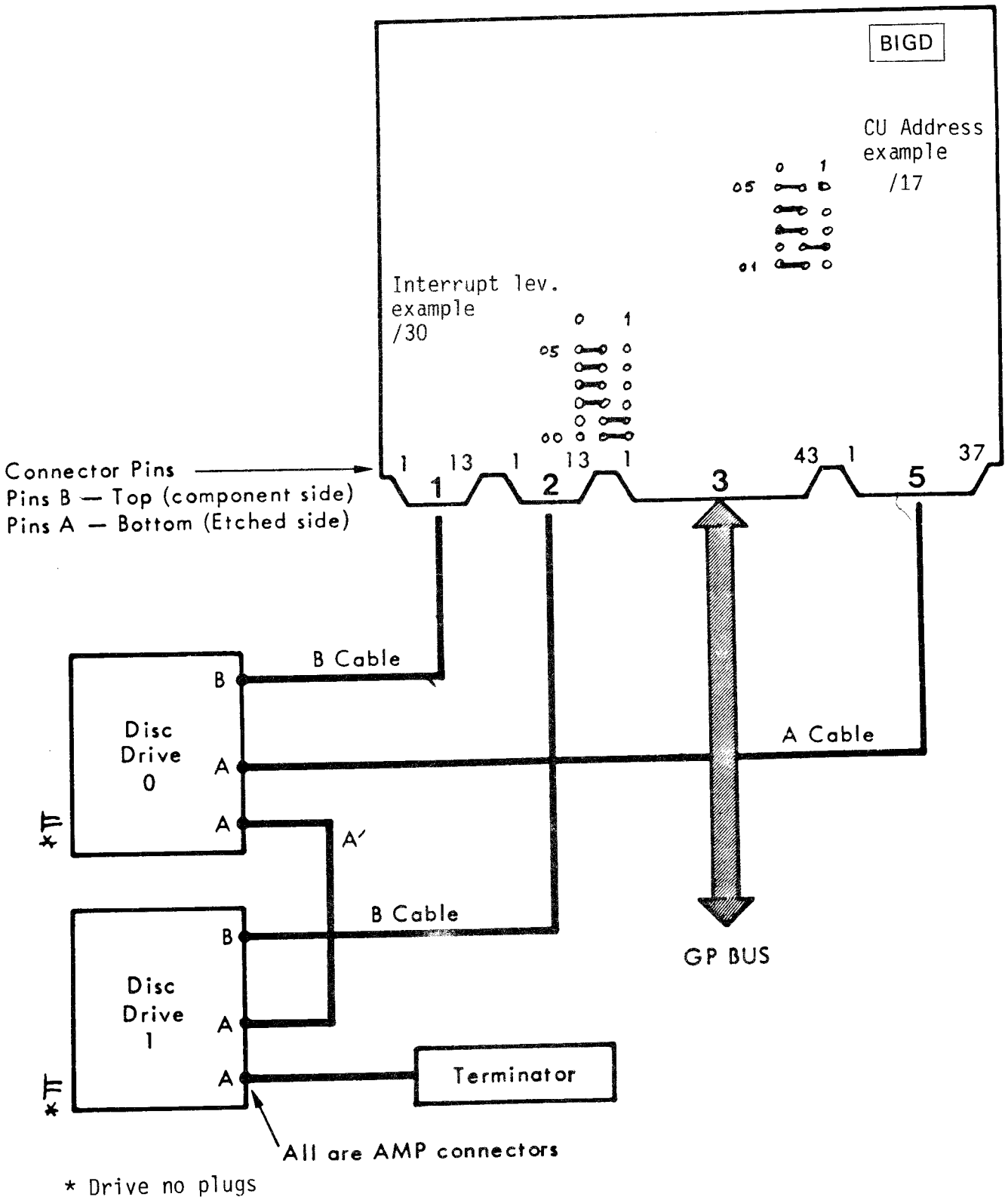


Figure 22.1 STRAPSETTING AND INTERFACE

Signal	Con. 5	AMP Con.	Device Name, Remarks
A Cable Output Signals			
SEL, N	A37, B37	25, 22	UNIT SELECT, Disc Selection
TAG1, N	A12, B12	49, 46	Cylinder Selection
TAG2, N	A13, B13	51, 48	Head Selection
TAG3, N	A25, B25	55, 52	Control Selection
BUS0, N	A8, B8	26, 23	
BUS1, N	A9, B9	27, 24	
BUS2, N	A10, B10	31, 28	
BUS3, N	A11, B11	32, 29	
BUS4, N	A31, B31	33, 30	Bit 0-9, Data Lines
BUS5, N	A32, B32	37, 34	
BUS6, N	A33, B33	38, 35	
BUS7, N	A34, B34	39, 36	
BUS8, N	A35, B35	43, 40	
BUS9, N	A36, B36	44, 41	
AD0, N	A7, B7	4, 1	
AD1, N	A28, B28	5, 2	UNIT SELECT 0-3, Disc Address
AD2, N	A29, B29	7, 3	
AD3, N	A30, B30	12, 8	
OCD, N	A6, B6	20, 16	Open Cable Detector
A Cable Input Signals			
IND, N	A3, B3	13, 10	INDEX Pulse
SEC, N	A27, B27	77, 74	Not Used (grounded)
SER, N	A5, B5	78, 75	SEEK ERROR
ONCIL, N	A1, B1	18, 15	ON CYLINDER
RDY, N	A4, B4	21, 17	UNIT READY
AMF, N	A2, B2	45, 42	ADDRESS MARK FOUND
FAULT, N	A26, B26	14, 11	Not Used (grounded)
INHA	A14 B14		Strap
B Cable Output Signals (1 set for each disc) disc0 = con.1 disc1 = con.2			
WDL, N	B1, B2	B, A	Write Data Line (bit serial)
Ground	B5	D	
WRC, N	A11, A12	J, H	Write Clock
Ground	B11	E	
B Cable Input Signals (1 set for each disc)			
RCP, N	A1, A2	X, W	Read Clock Pulse
Ground	B3	Y	
RD, N	A3, A4	V, U	Read Data (bit serial from disc)
Ground	B4	T	
WCP, N	A9, A10	N, M	SERVO CLOCK, Write Clock Pulse
Ground	B10	K	
SKEND,	A5, A6	CC, AA	Seek End
USL,	A7, A8	BB, DD	Unit Selected
INHB	B6 B7		Strap

Table 22.1 CU - DEVICE INTERFACE

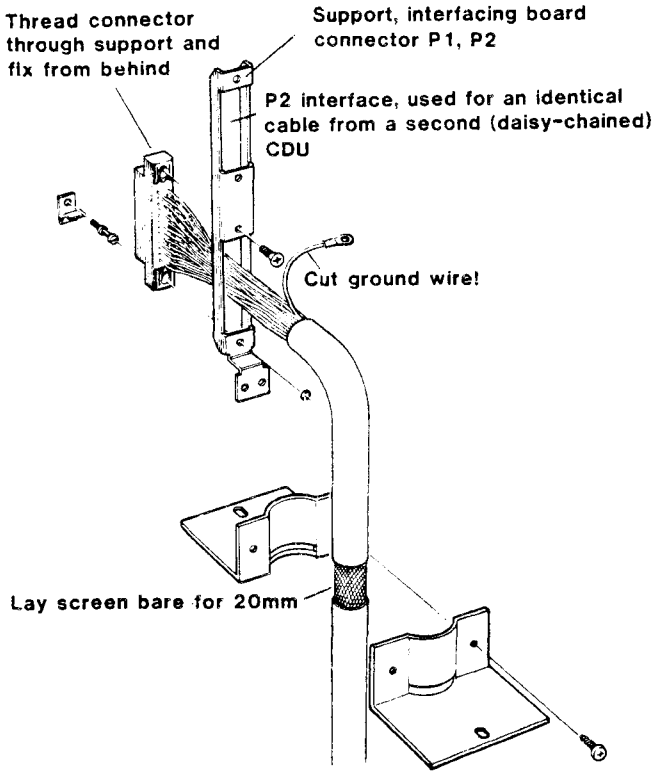


Figure 22.2 ENTRY KIT FOR B-CABLE FROM CDU 6877

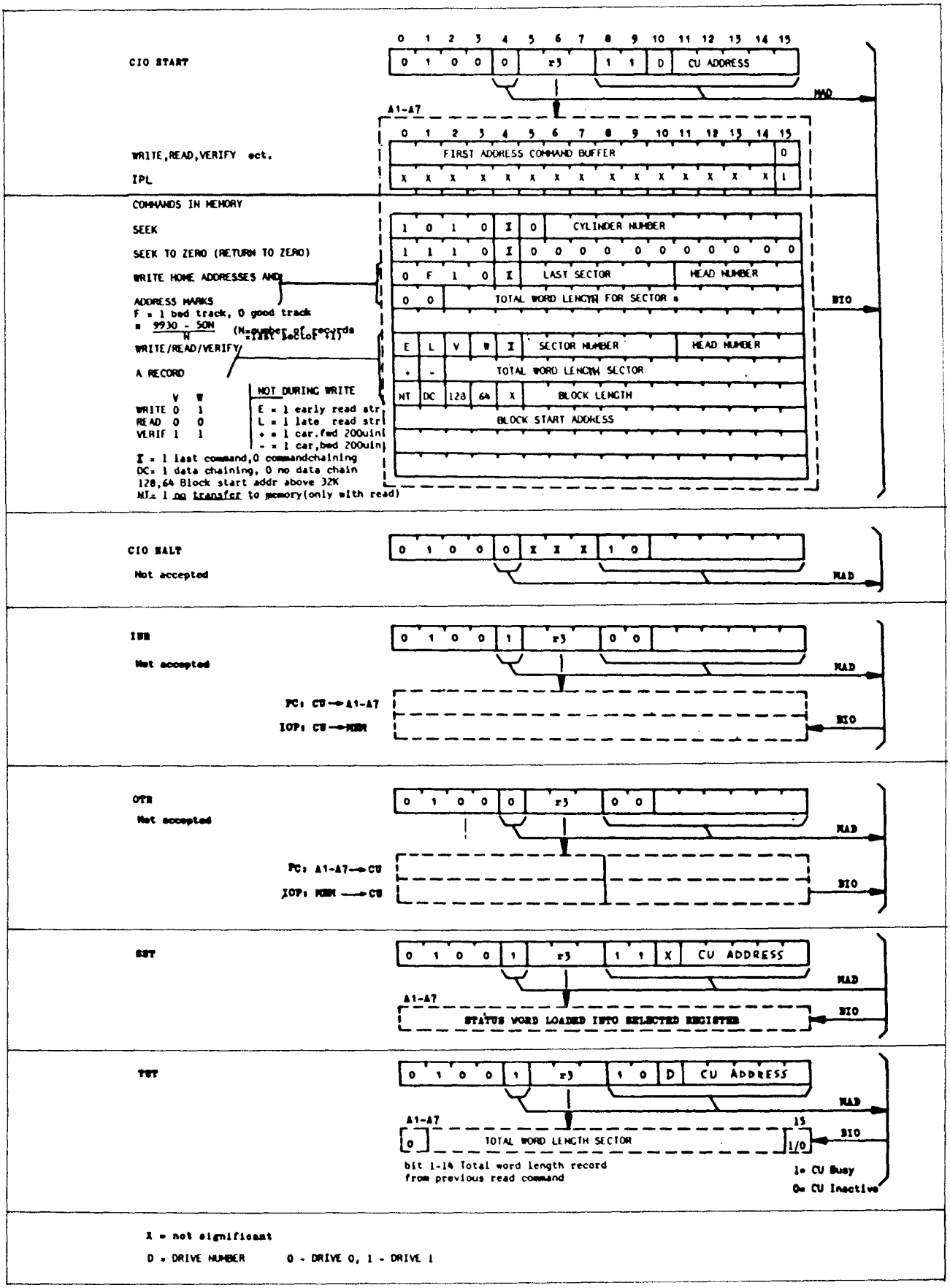
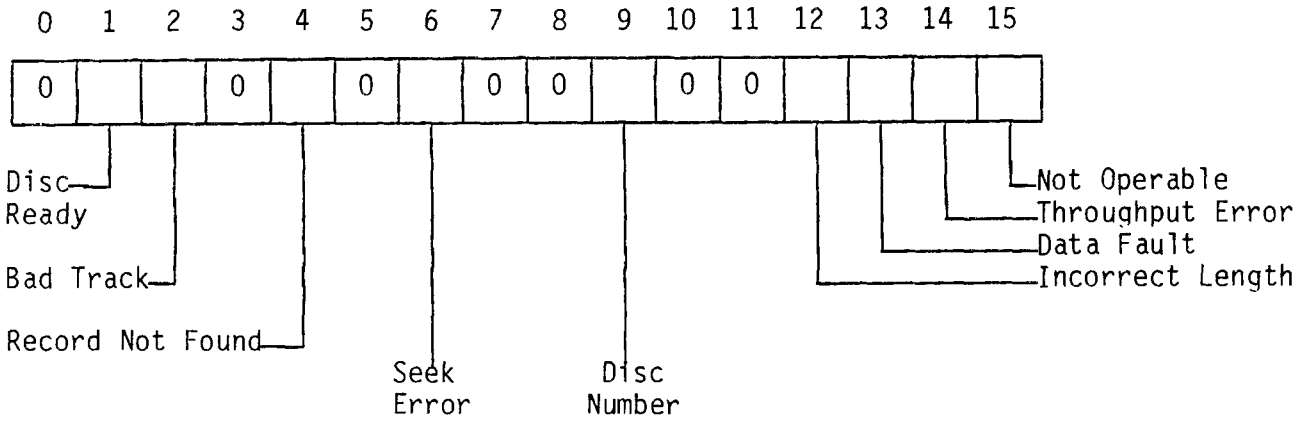


Figure 22.3 INSTRUCTION-/COMMAND-WORD FORMATS

22.4.1 STATUS WORD



Bit 15: Command attempted on a not operable disc drive.

Bit 14: Throughput error; the CU could not access the memory within 100 usec., during WRITE/READ or VERIFY Command.

Bit 13: Data fault; CRC check incorrect or during a VERIFY command a word does not compare.

Bit 12: Incorrect length; specified record length differs from the actual length or READ/WRITE not finished before end of track (next index-pulse).

Bit 9 : Disc drive number 0 = drive 0, 1 = drive 1.

Bit 6 : Seek error: The drive cannot reach the addressed cylinder or a cylinder number read from the Home Address does not compare at the end of the seek command.

Bit 4 : Record not found, during a WRITE/READ or VERIFY-command.

Bit 2 : Bad track; bad track bit is set in the home address of the accessed track.

Bit 1 : Drive became ready after being not operable (ready interrupt).

22.5 SHORT DESCRIPTION TEST-PROGRAM

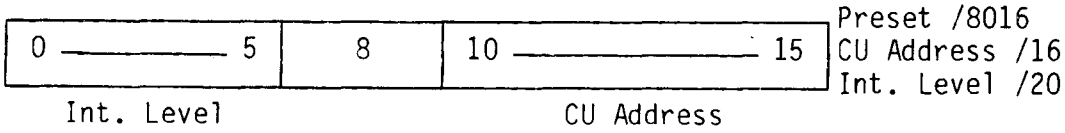
TESTPROGRAM BCDC2 32K 0.7 USEC.

1. IPL
   Program stops at /700 (= restart address and normal end).

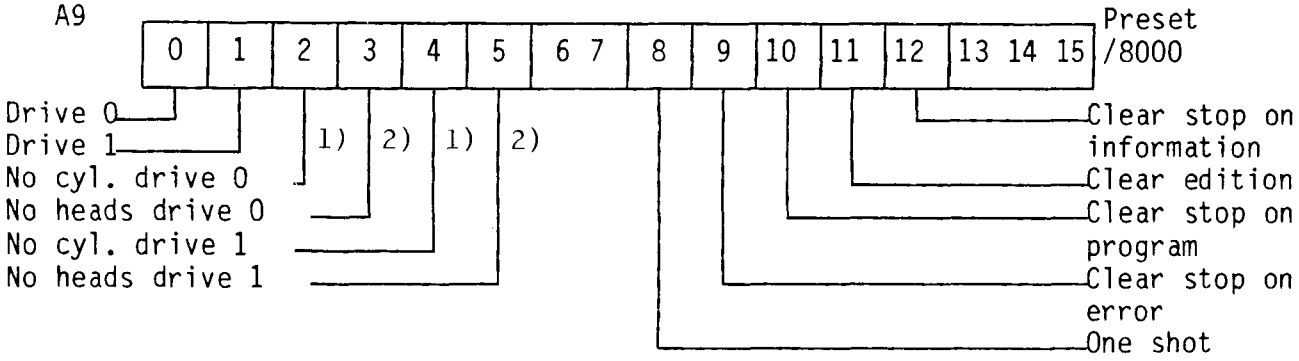
2. Switch on RTC (PF/AR also possible).
   Load a scratch dispack on the drive to be tested.

3.

A8



A9



Note 1): Bit 2,4: 0=411 cylinders, 40Mb/150Mb
1=823 cylinders, 80Mb/300Mb
Note 2): Bit 3,5: 0=5 heads, 40Mb/80Mb
1=19 heads, 150Mb/300Mb

A10

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
o	S	S	S	S	S	S	S	o	o	o	o	o	S	S	o	Preset /7F06 Checks to be executed

S = Standard setting
o = Optional

4. Depress MC, RUN

   Error stop at /5F0
   Restart after power/off :/6EE
   Interrupts return: /700
   Information stop: /5E0

For more information see detailed description of testprogram.

```
         DATE  82-05-05        IDENT    BIGD1


0000                           IDENT    BIGD1
0001                     *DATE: 820505 FOR PTS
0002
0003                     *        SMALL PROGRAM FOR WRITE,SEEK,WRITE HOME ADDR. AND VERIFY
0004
0005                     *        A1       START ADDRESS COMMAND BUFFER, PRESET FOR SEEK
0006                     *        DATA BUFFER START ADDRESS IS /0100
0007
0008                           AORG     /80
0009 0080 FFFF                 DATA     /FFFF
0010 0082 0000                 DATA     0
0011 0084 0194                 LDK      A1,/94                COMMAND BUFFER FOR SEEK
0012 0086 207F           START HLT                            AFTER RUN CHECK STATUS IN REG A4
0013 0088 20BF                 INH
0014 008A 41D7                 CIO      A1,1,/17              START CONTROLLER
0015 008C 5C04                 RB(4)    *-2
0016 008E 4CD7                 SST      A4,/17                GET STATUS
0017 0090 5C04                 RB(4)    *-2
0018 0092 5F0E                 RB       START
0019
0020                     * COMMAND BUFFER
0021
0022 0094 A000           SEEK  DATA      /A000                 SEEK TO CYLINDER 0
0023 0096 AB50                 DATA     /AB50                 SEEK TO CYLINDER 80
0024 0098 A000           WHAWVER DATA    /A000                 SEEK CYL. 0
0025 009A 27E0                 DATA     /27E0                 WRITE HOME ADDRESSES 64 SECTORS
0026 009C 0040                 DATA     /0040
0027 009E 1000                 DATA     /1000                 WRITE A SECTOR
0028 00A0 0040 0040            DATA     /0040,/0040
0029 00A4 0100                 DATA     /0100                 MEMORY BUFFER
0030 00A6 3800                 DATA     /3800                 VERIFY WRITTEN SECTOR
0031 00A8 0040 0040            DATA     /0040,/0040,/0100
     00AC 0100
0032
0033                           END      START


              SYMBOL TABLE

      SEEK    0094  A   START   0086  A   WHAWVE  0098  A

              ASS.ERR.    0000
    :EOF
    PROG ELAPSED TIME:  00H-00M-09S-240MS-



         DATE  82-05-05        IDENT    BIGD2


0000                           IDENT    BIGD2
0001                     *DATE: 820505 FOR PTS
0002
0003                     * SMALL PROGRAM TO PREMARK SURFACE 0
0004                     * WITH 64 SECTORS PER TRACK
0005                           AORG     /80
0006 0080 FFFF 0000            DATA     /FFFF,0
0007 0084 207F                 HLT
0008 0086 20BF           START INH
0009 0088 8120 00AC            LDKL     A1,COBUF              COMMAND BUFFER ADDRESS
0010 008C 41D7           CIO   CIO      A1,1,/17
0011 008E 4CD7                 SST      A4,/17                GET STATUS
0012 0090 5C04                 RB(4)    *-2
0013 0092 9041 00AC            IM       COBUF                 NEXT CYL.
0014 0096 8340 00AC            LD       A3,COBUF
0015 009A EB20 A336            CWK      A3,/A336              IS IT THE LAST CYL.
0016 009E 5D14                 RB(5)    CIO                   NO,THEN THE NEXT
0017 00A0 207F                 HLT                            YES,CHECK STATUS IN A4
0018 00A2 8320 A000      AGAIN LDKL     A3,/A000
0019 00A6 8341 00AC            ST       A3,COBUF              REPAIR COMMAND
0020 00AA 5F26                 RB       START
0021
0022                     * COMMAND BUFFER
0023
0024 00AC A000 2FE0      COBUF DATA     /A000,/2FE0,/0040     SEEK,WHA FOR 64 SECTORS
     00B0 0040
0025
0026                           END      START


             SYMBOL TABLE

    AGAIN   00A2  A   CIO     008C  A   COBUF   00AC  A   START   0086  A

             ASS.ERR.    0000
  :EOF
  PROG ELAPSED TIME:  00H-00M-08S-460MS-
```

```
         DATE  82-05-05        IDENT    BIGD3

0000                           IDENT    BIGD3
0001                  *DATE: 820505 FOR PTS
0002                  *PROGRAM FOR ADJUSTING THE HEADS
0003
0004
0005                           AORG     /80
0006 0080 FFFF                 DATA     /FFFF
0007 0082 0000                 DATA     0
0008 0084 207F         START   HLT
0009 0086 20BF                 INH
0010 0088 01AC                 LDK      A1,SK230
0011 008A 41D7                 CIO      A1,1,/17              SEEK TO CYL 230
0012 008C 4CD7                 SST      A4,/17
0013 008E 5C04                 RB(4)    *-2
0014 0090 01AE                 LDK      A1,HSEL
0015 0092 41D7                 CIO      A1,1,/17
0016 0094 4CD7                 SST      A4,/17
0017 0096 5C04                 RB(4)    *-2
0018 0098 01B6                 LDK      A1,SK245
0019 009A 41D7                 CIO      A1,1,/17              SEEK TO CYL 245
0020 009C 4CD7                 SST      A4,/17
0021 009E 5C04                 RB(4)    *-2
0022 00A0 207F                 HLT                            PUSH RUN FOR RTN TO ZERO
0023 00A2 01B8                 LDK      A1,SK0
0024 00A4 41D7                 CIO      A1,1,/17              RETURN TO CYL 000
0025 00A6 4CD7                 SST      A4,/17
0026 00A8 5C04                 RB(4)    *-2
0027 00AA 5F28                 RB       START
0028                  *        COMMAND BUFFERS
0029 00AC A8E6         SK230   DATA     /A8E6                 SEEK TO CYL 230
0030 00AE 0800         HSEL    DATA     /0800                 READ WITH HEAD 0
0031 00B0 0040 0040            DATA     /0040,/0040,/0100
     00B4 0100
0032 00B6 A8F5         SK245   DATA     /A8F5                 SEEK TO CYL. 245
0033 00B8 E800         SK0     DATA     /E800                 RETURN TO CYL 000
0034
0035
0036                  *AFTER THE PROGRAM HAVE RUNNED ONCE
0037                  *AND YOU WANT TO SELECT AN OTHER HEAD;
0038                  *OPERATE SW 2 ON A05(REMOTE/LOCAL) TO LOCAL
0039                  *AND BACK TO REMOTE. THE PROGRAM THEN STOPS IN
0040                  *ADDRESS /00A0, PUSH THE RUN BUTTON TO PERFORM
0041                  *A RETURN TO CYL 0, AND THE PROGRAM STOPS AT
0042                  *ADDRESS /0086
0043                  *CHANGE THE CONTENS OF ADDR. /00A4:
0044                  *        /0800    HEAD 0
0045                  *        /0801    HEAD 1
0046                  *        /0802    HEAD 2
0047                  *        /0803    HEAD 3
0048                  *        /0804    HEAD 4
0049                           END      START

            SYMBOL TABLE

    HSEL    00AE  A   SK0     00B8  A   SK230   00AC  A   SK245   00B6  A
    START   0084  A

            ASS.ERR.    0000
  :EOF
  PROG ELAPSED TIME:  00H-00M-13S-440MS-
```

```
        DATE  82-06-23        IDENT    BIGD4N


0000                          IDENT    BIGD4N
0001                    *DATE: 820618 FOR PTS
0002                    *       PROGRAM FOR HEAD ADJUSTMENT FOR 80M DISC
0003                    *       CONNECTED TO BIGD1 CU OR BIGD2 CU
0004
0005
0006                                    - OPERATING BIGD4N ADJUSTMENT PROGRAM
0007                                    - LOAD PROGRAM FROM CASSETTE,DISC OR FLEXIBLE DISC
0008                                    OR WITH EFP OR CFP
0009
0010                    *       A       AFTER LOADING SOP DISPLAY /7FF (ALL LAMPS LIT
0011                    *               -DEPRESS A SOP-SWITCH
0012                    *                DISPLAY ON SOP /FF AND SEEKING FROM CYL 230-
0013                    *                235 FOR ABOUT 30 SEC.
0014                    *               -SOP DISPLAYS /004
0015                    *                HEADS AT CYL 4 FOR SERVO MEASUREMENT
0016                    *               -AFTER MEASURING OPERATE LOCAL/REMOTE
0017                    *                SWITCH ON CARD A05 IN DISC DRIVE(SW2)
0018                    *               -SOP DISPLAYS /005
0019                    *                HEADS ON CYL 5 FOR SERVO MEASURING
0020                    *               -AFTER MEASURING OPERATE SW2 ON A05
0021                    *       B       -SOP DISPLAYS /03E
0022                    *               -BY DEPRESSING OF A SOP SWITCH WITH LED LIT ABOVE
0023                    *                A HEAD IS SELECTED FOR ADJUSTMENT OR CHECKING
0024                    *                SOP SW 6,7,8,9,0 IS HEAD 4,3,2,1,0
0025                    *                DEPRESSING AN OTHER SOP SWITCH RESULTS IN A STEP
0026                    *                TO PROGRAM PART C
0027                    *                EXAMPLE:
0028                    *               -DEPRESS SOP SW 8
0029                    *                SOP DISPLAYS /A2 (ADJUST,CHECK AND FIX HEAD 2)HEADS ARE AT
0030                    *                CYL 4
0031                    *               -OPERATE SW2 ON A05
0032                    *               - SOP DISPLAYS /03E GO BACK TO A FOR SELECTING
0033                    *                OTHER HEAD OR PART C
0034
0035                    *       C       -SOP DISPLAYS /2FF
0036                    *                CONTINUES SEEK IS DONE AS IN A
0037                    *               -SOP DISPLAYS /3E
0038                    *                HEAD SELECTION IS DONE AS IN B BUT ONLY
0039                    *                FOR CHECKING ADJUSTMENT
0040                    *                EXAMPLE:
0041                    *               -DEPRESS SOP SW 8 FOR HEAD 2
0042                    *               - SOP DISPLAYS /2C2
0043                    *                HEAD AT CYL 245 AND HEAD 2 CAN BE CHECKED
0044                    *               -OPERATE SW2 ON A05
0045                    *               -SOP DISPLAYS /03E FOR SELECTION OF AN OTHER
0046                    *                HEAD
0047                    *               -IF AN OTHER SOP SWITCH(WITH NO LED LIT ABOVE)
0048                    *                IS DEPRESSED PROGRAM RESTARTS AND
0049                    *                SOP DISPLAYS /7FF GOTO A
0050
0051
0052 0000                               RES      /40
0053                                    EJECT
0054 0080 FFFF 0000                     DATA     /FFFF,0
0055 0084 208F                  START   INH                              NO INTERRUPTS
0056 0086 86A0 A804                     LDKL     A14,/A804               SEEK TO CYL 4
0057 008A 86C1 0168 R                   ST       A14,SEK245              CHANGE TO SEEK CYL 4
0058 008E 0500                          LDK      A5,0                    CLEAR RETRY FLAG
0059 0090 41EE                          CIO      A1,1,/2E                START SOP
0060 0092 8320 07FF                     LDKL     A3,/7FF                 /7FF ON SOP
0061 0096 432E                          OTR      A3,0,/2E
0062 0098 4A2E                          INR      A2,0,/2E                READ SOP SW
0063 009A 5C04                          RB(NA)   *-2
0064 009C 03FF                          LDK      A3,/FF                  DISP FIRST SEEKING
0065 009E 86A0 0154 R                   LDKL     A14,EOS                 STACKPOINTER
0066 00A2 0700                          LDK      A7,0                    FLAG FIRST TIME
0067      00A4                  SECOND  EQU      *
0068 00A4 80A0 03FF                     LDKL     A8,/3FF                 FOR 30 SECONDS SEEK
0069 00A8 85A0 0130 R                   LDKL     A13,CIOSST              SUBROUTINE ADDRESS
0070                            *       CONTINUOUS SEEK FROM 230 TO 235
0071
0072
0073 00AC 8120 0156 R           SEEK    LDKL     A1,CSEEK                COMMAND BUFFER ADDRESS
0074 00B0 F697                  CONT    CFR      A14,A13                 SEEK FROM 230 TO 235
0075 00B2 1102                          ADK      A1,2                    COMMAND BUFFER ADDRESS
0076 00B4 F697                          CFR      A14,A13                 SEEK TO 235
0077 00B6 98A0 0001                     SUKL     A8,1                    TIME OVER?
0078 00BA 5910                          RB(P)    SEEK
0079 00BC 871C                          LDR      A7,A7                   IS IT THE FIRST TIME?
0080 00BE 5120                          RF(P)    SK245
0081                            *       SEEK TO CYLINDER 4
0082 00C0 8120 015A R                   LDKL     A1,SEEK4                COMMAND BUFFER ADDRESS
0083 00C4 0304                          LDK      A3,4                    DISPLAY CIL 4
0084 00C6 F697                          CFR      A14,A13                 SEEK TO CYL 4
0085 00C8 0300                          LDK      A3,0                    SOP DISPL
```

```
0086 00CA 8120 016A R           LDKL    A1,SEEK0
0087 00CE F697                  CFR     A14,A13                 PERFORM SEEK TO ZERO
0088                                                            STOP FOR MEASURING TO CONTINUE PUSH RUN
0089                    *       SEEK TO CYLINDER 5
0090 00D0 0305                  LDK     A3,5                    CYL 5
0091 00D2 8120 015C R           LDKL    A1,SEEK5                COMMAND BUFFER ADDRESS
0092 00D6 F697                  CFR     A14,A13                 SEEK TO CYL 5
0093 00D8 0300                  LDK     A3,0                    SOP DISPL
0094 00DA 8120 016A R           LDKL    A1,SEEK0
0095 00DE F697                  CFR     A14,A13                 PERFORM SEEK TO ZERO
0096                                                            STOP FOR MEASURING TO CONTINUE PUSH SW A
0097                    *       SEEK TO CYLINDER 4 OR 245 FOR THE SEVERAL HEADS
0098
0099 00E0 033E          SK245   LDK     A3,/3E
0100 00E2 432E                  OTR     A3,0,/2E                DISPLAY HEAD SEL
0101 00E4 4A2E                  INR     A2,0,/2E                READ HEAD NUMBER
0102 00E6 5C04                  RB(NA)  *-2
0103 00E8 3AAC                  SRN     A2,A3                   FIND HEAD NUMBER
0104 00EA EB20 0004             CWK     A3,4                    MUST  IT GO TO CHECK
0105 00EE 512A                  RF(G)   CHECK
0106 00F0 E341 015F R           SC      A3,HSEL+1               TO START WITH SELECTED HEAD
0107 00F4 B320 02C0             XRKL    A3,/2C0                 FOR DISPLAY 2CX IN 2ND CHECK
0108 00F8 871C          NEXTH   LDR     A7,A7                   IS IT THE FIRST TIME
0109 00FA 5404                  RF(NZ)  NEXT                    NO
0110 00FC B320 0260             XRKL    A3,/260                 FOR DISPLAY AX ADJUST HEAD
0111 0100 8120 016A R   NEXT    LDKL    A1,SEEK0                COMMAND BUFFER ADDRESS
0112 0104 860C                  LDR     A6,A3                   SAVE SOP DISPLAY
0113 0106 0300                  LDK     A3,0                    FOR DISPLAY 0
0114 0108 F697                  CFR     A14,A13                 SEEK TO 0
0115 010A 8120 015E R           LDKL    A1,HSEL                 SEL HEAD
0116 010E F697                  CFR     A14,A13                 DO HEAD SEL
0117 0110 8318                  LDR     A3,A6                   LOAD SOP DISPLAY
0118 0112 8120 0168 R           LDKL    A1,SEK245               COMMAND BUFFER ADDRESS
0119 0116 F697                  CFR     A14,A13                 SEEK 4 OR 245
0120                    *       AFTER ADJUSTING THE HEAD
0121
0122 0118 5F3A                  RB      SK245                   ASK NEXT HEAD
0123      011A          CHECK   EQU     *
0124 011A 1701                  ADK     A7,1                    SET FLAG 2 ND TIME
0125 011C EF20 0002             CWK     A7,2                    IS TI THE SECOND TIME?
0126 0120 589E                  RB(E)   START
0127 0122 84A0 A8F5             LDKL    A12,/A8F5               SEEK TO 245
0128 0126 84C1 0168 R           ST      A12,SEK245              CHANGE TO SEEK 245
0129 012A 8320 02FF             LDKL    A3,/2FF                 DISPLAY SEEK
0130 012E 5F8C                  RB      SECOND
0131                    *                                       FOR CONTUNUOUS SEEK AGAIN
0132                    *       SUBROUTINE
0133
0134 0130 41D7          CIOSST  CIO     A1,1,/17                START OPERATION
0135 0132 432E                  OTR     A3,0,/2E                DISPLAY FUNCT ON SOP
0136 0134 4CD7                  SST     A4,/17                  ASK FOR STATUS
0137 0136 5C04                  RB(NA)  *-2
0138 0138 2401                  ANK     A4,1                    CHECK IF NOT OPERABLE
0139 013A 5104                  RF(P)   CHRETRY                 CHECK IF RETRY
0140 013C 0500                  LDK     A5,0                    CLEAR RETRY FLAG
0141 013E F03A                  RTN     A14
0142 0140 8514          CHRETRY LDR     A5,A5                   RETRY OR NOT
0143 0142 5C14                  RB(NZ)  CIOSST                  DO RETRY
0144 0144 0501          NORETRY LDK     A5,1                    SET RETRY FLAG FOR NEXT COMMAND
0145                    *       STACK AREA
0146
0147 0146                       RES     7
0148 0154               EOS     RES     1
0149                    *       COMMAND BUFFERS
0150
0151 0156 A8E6          CSEEK   DATA    /A8E6                   SEEK TO 230
0152 0158 A8EB                  DATA    /A8EB                   SEEK TO 235
0153
0154 015A A804          SEEK4   DATA    /A804                   SEEK TO 4
0155
0156 015C A805          SEEK5   DATA    /A805                   SEEK TO 5
0157
0158      015E          HSEL    EQU     *
0159 015E 0800                  DATA    /0800                   READ WITH HEAD X
0160 0160 0040 0040             DATA    /0040,/0040
0161 0164 0000 0000     BUFL    DATA    0,0
0162 0168 A8F5          SEK245  DATA    /A8F5                   SEEK TO CYL 245
0163
0164 016A E800          SEEK0   DATA    /E800                   RETURN TO CYL 0
0165
0166                            END     START
```

SYMBOL TABLE

BUFL	0164	R	CHECK	011A	R	CHRETR	0140	R	CIOSST	0130	R
CONT	00B0	R	CSEEK	0156	R	EOS	0154	R	HSEL	015E	R
NEXT	0100	R	NEXTH	00F8	R	NORETR	0144	R	SECOND	00A4	R
SEEK	00AC	R	SEEK0	016A	R	SEEK4	015A	R	SEEK5	015C	R
SEK245	0168	R	SK245	00E0	R	START	0084	R			

ASS.ERR. 0000

:EOF

PROG ELAPSED TIME: 00H-00M-00S-000MS-

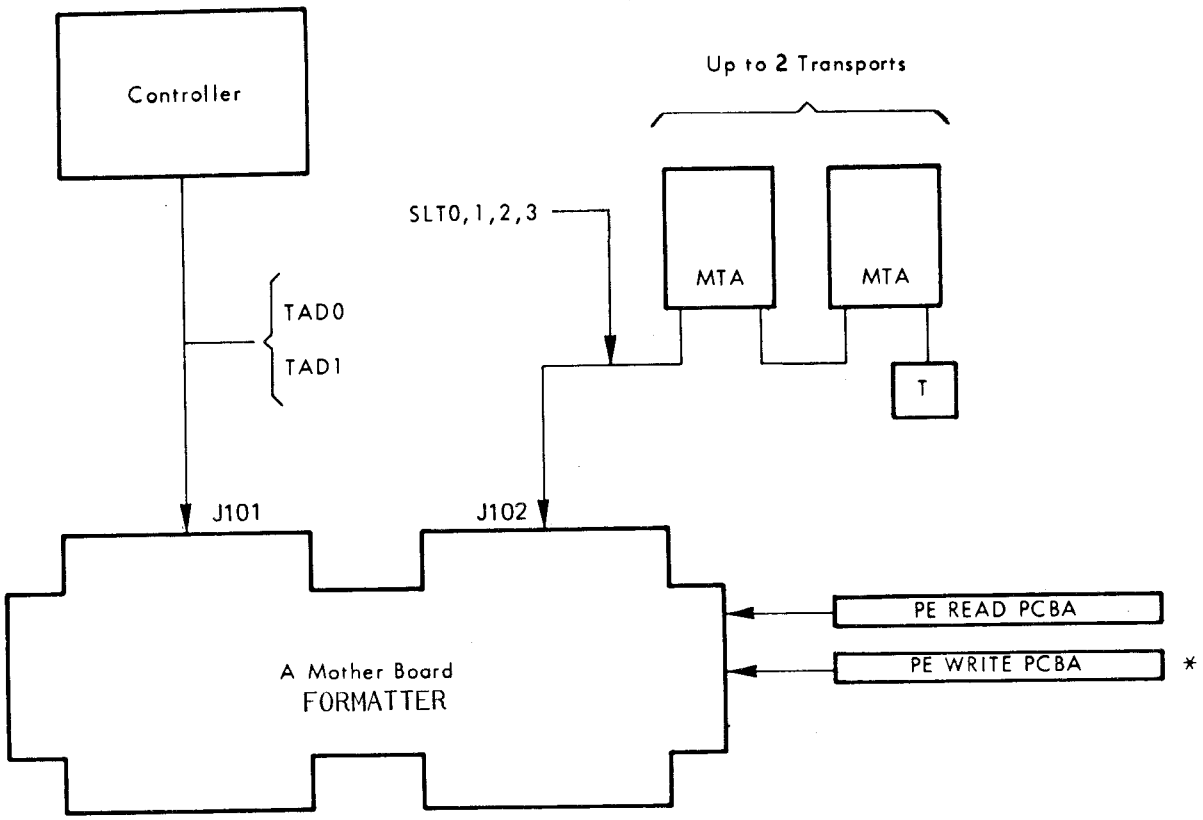
23 CHANNEL UNIT MAGNETIC TAPE UNIT

LIST OF ILLUSTRATIONS

LIST OF TABLES

23.1 CHMT-IDENTIFICATIONS

Type-number:	: PTS-6842
Test-Program:	: MTUTSC
Channel:	: Hardware Channel (IOP)
CU address	: CHMT1: /OC, CHMT2: /OD.
Break Connections	: CHMT1: 3A43 - IOP1: 4B09 (BR04N). : CHMT2: 3A43 - IOP1: 4B08 (BR05N).
Magnetic Tape Units	: MTU 0: PTS 6168, 1600bpi, PE (including formatter F849). or MTU 0: PTS 6872-001, 1600bpi, PE (incl. formatter F849). MTU 1: PTS 6872-002, 1600bpi, PE.
Power-Consumption	: 5 VOLT, 2.5 AMP



* Note: Switch on PCB always to "0".

Figure 23.1 FORMATTER/TRANSPORT SYSTEM CONFIGURATION

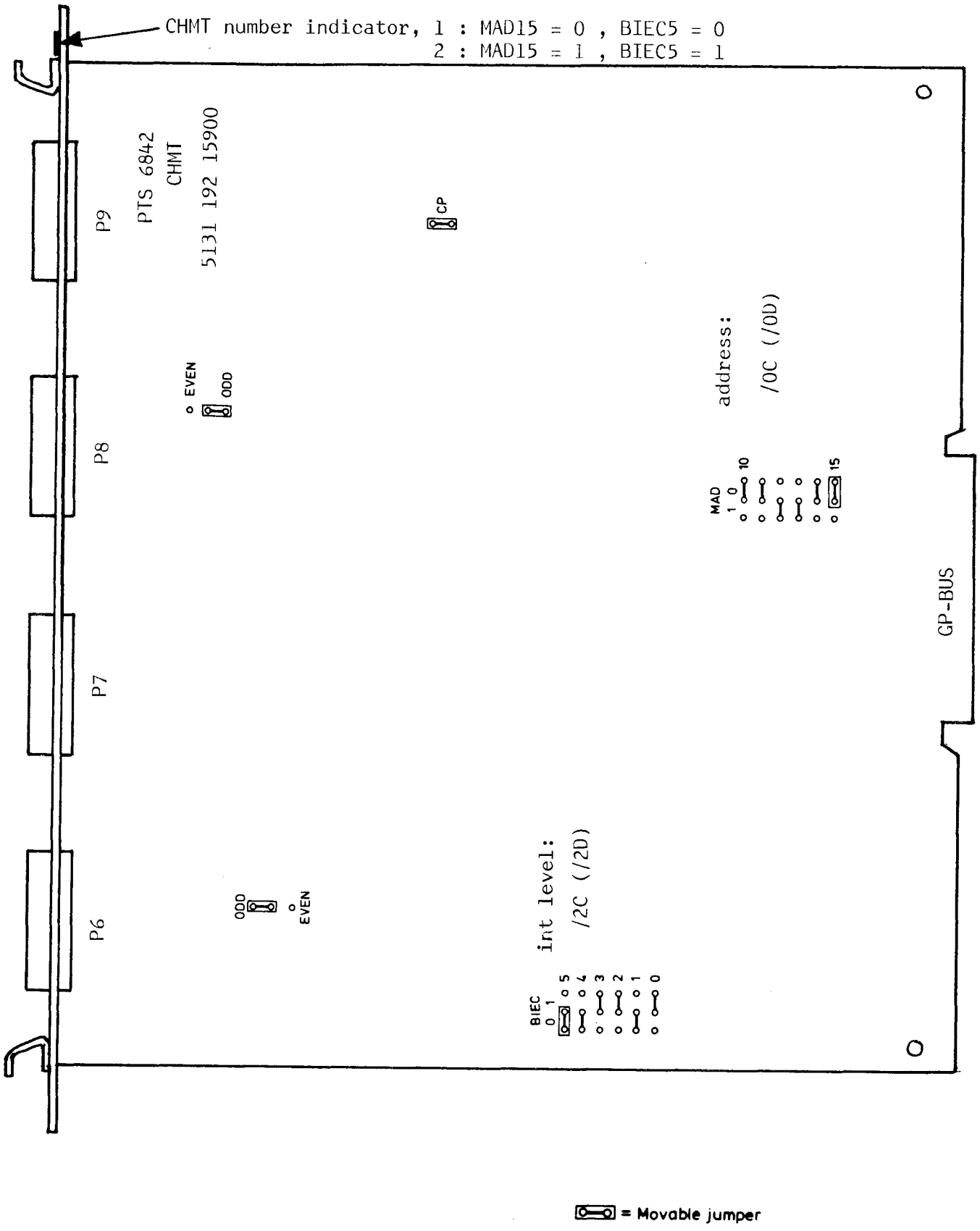


Figure 23.2 CHMT STRAP SETTING

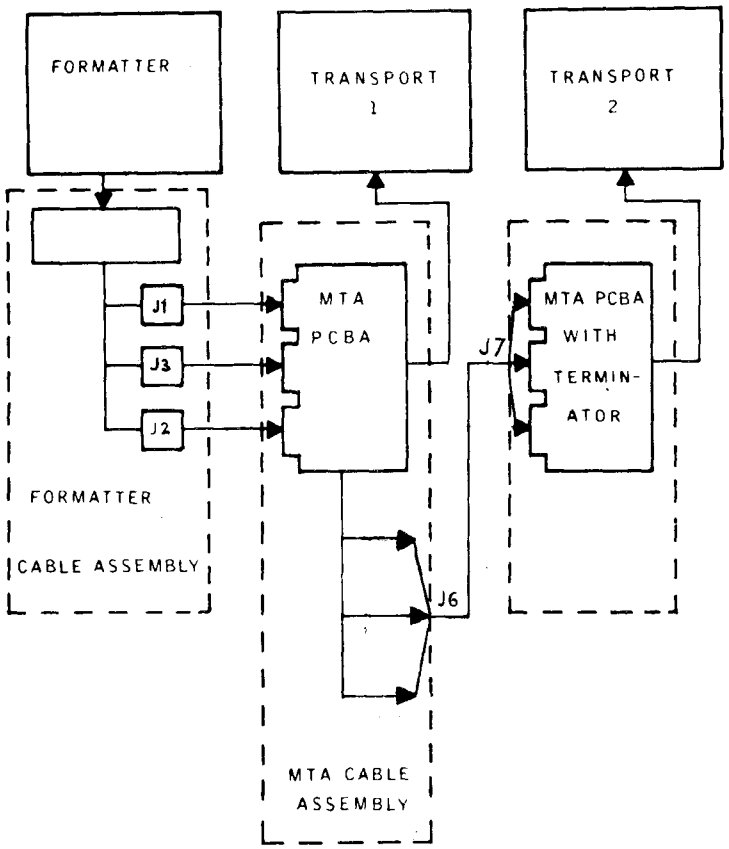


Figure 23.3 MTA SYSTEM DIAGRAM

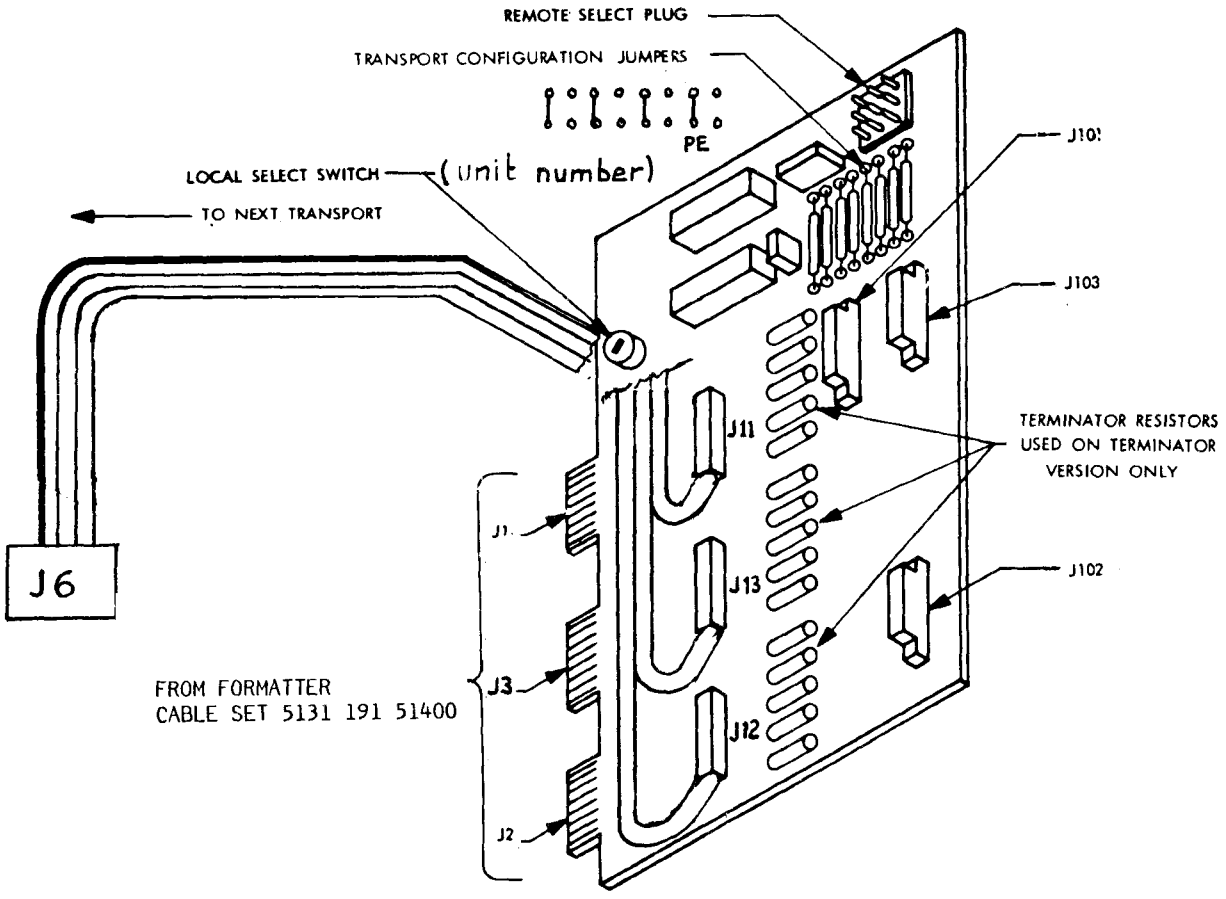
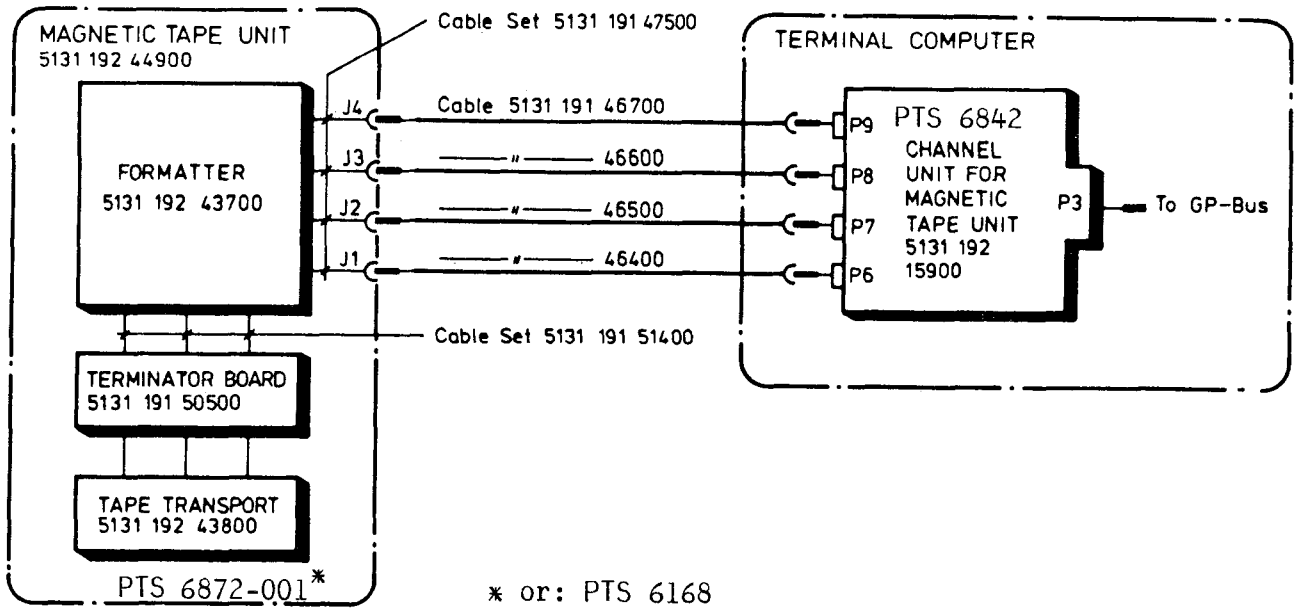
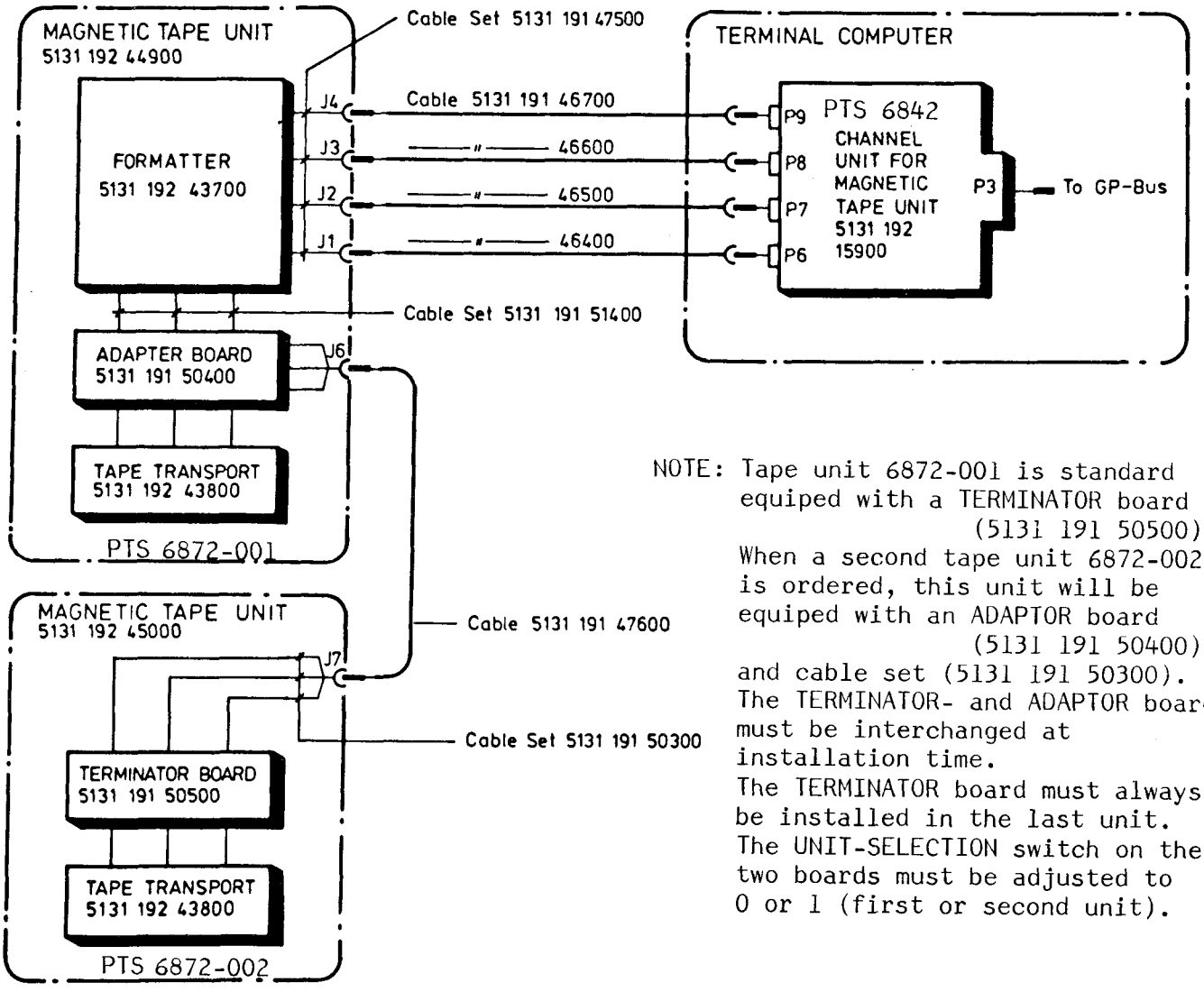


Figure 23.4 MTA CABLE ASSEMBLY 5131 191 50400



* or: PTS 6168



NOTE: Tape unit 6872-001 is standard equiped with a TERMINATOR board (5131 191 50500).
When a second tape unit 6872-002 is ordered, this unit will be equiped with an ADAPTOR board (5131 191 50400) and cable set (5131 191 50300).
The TERMINATOR- and ADAPTOR board must be interchanged at installation time.
The TERMINATOR board must always be installed in the last unit.
The UNIT-SELECTION switch on the two boards must be adjusted to 0 or 1 (first or second unit).

Figure 23.5 CABLING

CU Connector P6 6872-001 J1		INPUT Signal	Formatter Card Connector J101		
Live Pin	Ground Pin	Name	Live Pin	Ground Pin	
02	14	RPN	A36	*	
03	15	RON	B37		
04	16	R1N	A37		
05	17	R2N	B39		
06	18	R3N	A39		READ DATA Lines
07	19	R4N	B40		
08	20	R5N	A40		
09	21	R6N	B42		
10	22	R7N	A42		
11	23	CCGN	B24		IDENTIFICATION BURST
12	24	DBYN	A22		DATA BUSY
13	25				

* Note: Nearest ground pin is used.

Table 23.1a FORMATTER TO CU INTERFACE

CU Connector P7 6872-001 J2		INPUT Signal	Formatter Card Connector J101		
Live Pin	Ground Pin	Name	Live Pin	Ground Pin	
02	14	WSTRN	A34	*	WRITE STROBE
03	15	RSTRN	B36		READ STROBE
04	16	FMKN	A25		FILE MARK READ
05	17	EOTN	A30		END OF TAPE
06	18	HERN	A24		HARD ERROR
07	19	CERN	B25		CORRECTED ERROR
08	20	LDPN	B30		LOAD POINT
09	21	FPTN	A28		FILE PROTECTED
10	22	RDYN	B27		READY
11	23	FBYN	B22		FORMATTER BUSY
12	24	ONLN	A27		ONLINE
13	25				

* Note: Nearest ground pin is used.

Table 23.1b FORMATTER TO CU INTERFACE

CU Connector P8 6872-001 J3		OUTPUT Signal	Formatter Card Connector J101		
Live Pin	Ground Pin	Name	Live Pin	Ground Pin	
02	14	WPN	A15	*	
03	15	W0N	B16		
04	16	W1N	A16		
05	17	W2N	B18		
06	18	W3N	A18		WRITE DATA Lines
07	19	W4N	B19		
08	20	W5N	A19		
09	21	W6N	B21		
10	22	W7N	A21		
11	23	LWDN	B13		LAST WORD
12	24	FENN	A13		FORMATTER ENABLE
13	25				

* Note: Nearest ground pin is used.

Table 23.2a CU TO FORMATTER INTERFACE

CU Connector P9 6872-001 J4		OUTPUT Signal	Formatter Card Connector J101		
Live Pin	Ground Pin	Name	Live Pin	Ground Pin	
02	14	GON	A03	*	INITIATE Command
03	15	REVN	B04		REVERSE/FORWARD
04	16	WRTN	A04		WRITE/READ
05	17	WFMN	B06		WRITE FILE MARK
06	18	EDITN	A06		EDIT Command
07	19	ERASEN	B07		ERASE Command
08	20	REWN	B12		REWIND Command
09	21	LOLN	A10**	B15**	LOAD ON LINE Command
10	22	FADN	B01		FORMATTER ADDRESS
11	23	TADON	A01		TRANSPORT ADDRESS
12	24	TAD1N	B03		TRANSPORT ADDRESS
13	25	OFLN	A12		OFF-LINE Command

* Note: Nearest groundpin is used.

** Note: J101 pin A10 is interconnected with J102 pin A04 (in the formatter)
J101 pin B15 is interconnected with J102 pin B04.

Table 23.2b CU TO FORMATTER INTERFACE

Transport J103 Live	Ret		MTA II J3* Live	Ret		Formatter J102 Live	Ret	Signal
1	A	→	1	A	→	B1	B2	READ DATA PARITY (IRDP)
2	B	→	2	B	→	A1	A2	
3	C	→	3	C	→	B3	B2	READ DATA 0 (IRD0)
4	D	→	4	D	→	A3	A2	READ DATA 1 (IRD1)
8	J	→	8	J	→	A6	A5	READ DATA 2 (IRD2)
9	K	→	9	K	→	B7	A8	READ DATA 3 (IRD3)
10	L	→	10	L	→	A7	A8	
11	M	→	11	M		B9	B8	
12	N	→	12	N		A9	A8	
13	P	→	13	P		B10	B11	
14	R	→	14	R	→	A10	A11	READ DATA 4 (IRD4)
15	S	→	15	S	→	B12	B11	READ DATA 5 (IRD5)
17	U	→	17	U	→	B13	B14	READ DATA 6 (IRD6)
18	V	→	18	V	→	A13	A14	READ DATA 7 (IRD7)

Note: The following pins provide +5v and ground from the Formatter to the MTA assemblies.

5	E	←	A48	B48	
6	F	←	A49	B49	
7	H	←	A50	B50	

*Read signals applied to J3 are also applied in parallel to J10 for application to other MTA II PCBAs in the daisy-chain. Refer to Schematic No. 103914.

Table 23.3 READ SIGNALS, TRANSPORT TO FORMATTER VIA MTA II

Formatter J102 Live	Ret		MTA II J2* Live	Ret		Transport J102 Live	Ret	Signal
B15	B14	→	A	1	→	A	1	WRITE DATA STROBE (IWDS)
B16	B17	→	C	3	→	C	3	WRITE AMPLIFIER RESET (IWARS)
B18	B17		E	5	→	E	5	
A18	A17		F	6	→	F	6	
A21	A20	→	L	10	→	L	10	WRITE DATA PARITY (IWDP)
B22	B23	→	M	11	→	M	11	WRITE DATA 0 (IWD0)
A22	A23	→	N	12	→	N	12	WRITE DATA 1 (IWD1)
B24	B23	→	P	13	→	P	13	WRITE DATA 2 (IWD2)
A24	A23	→	R	14	→	R	14	WRITE DATA 3 (IWD3)
B25	B26	→	S	15	→	S	15	WRITE DATA 4 (IWD4)
A25	A26	→	T	16	→	T	16	WRITE DATA 5 (IWD5)
B26	B26	→	U	17	→	U	17	WRITE DATA 6 (IWD6)
A27	A26	→	V	18	→	V	18	WRITE DATA 7 (IWD7)
						J101		
A42	A41	→	B	2	→	J	2	SELECT 1 (ISLT1)**
B43	B44	→	D	4	→	J	16	SELECT 2 (ISLT2)**
A43	A44	→	H	7	→	J	17	SELECT 3 (ISLT3)**

*Write signals applied to J2 are also applied in parallel to J12 for application to other MTA II PCBAs in the daisy-chain. Refer to Schematic No. 103914.

**Provided through Select Switch

Table 23.4 WRITE SIGNALS, FORMATTER TO TRANSPORT VIA MTA II

Formatter J102 Live	Ret		MTA II J1* Live	Ret		Transport J101 Live	Ret	Signal
A28	A29	→	B	2	→	B	2	OVER WRITE (IOVW)
B30	B29	→	C	3	→	C	3	SYNCHRONOUS FORWARD Command (ISFC)
A30	A29		D	4	→	D	4	
B31	B32	→	E	5	→	E	5	SYNCHRONOUS REVERSE Command (ISRC)
A31	A32	←	F	6	←	F	6	DATA DENSITY INDICATOR (IDDI)*
B33	B32	→	H	7	→	H	7	REWIND Command (IRWC)
B34	B35	→	K	9	→	K	9	SET WRITE STATUS (ISWS)
A34	A35	→	L	10	→	L	10	OFF-LINE Command (IOFC)/REWIND UNLOAD (IRWU)***
B36	B35	←	M	11	←	M	11	ON-LINE (IONL)
A36	A35		N	12	←	N	12	
B37	B38	←	P	13	←	P	13	FILE PROTECT (IFPT)
A37	A38	←	R	14	←	R	14	LOAD POINT (ILDP)
A39	A38	←	T	16	←	T	16	READY (IRDY)
B40	B41	←	U	17	←	U	17	END OF TAPE (IEOT)
B42	B41	→	J	8	→	J	8	SELECT 0 (ISLT0)****
A4	B4	→	1	2	→	1	2	LOAD ON-LINE (ILOL)

*Control signals applied to J1 are also applied in parallel to J11 for application to other MTA II PCBAs in the daisy-chain. Refer to Schematic No. 103914.

***REWIND UNLOAD operation applies to T9000 series transports only.

****Provided through Select Switch.

Table 23.5 CONTROL SIGNALS, TRANSPORT/MTA II/FORMATTER

ADAPTOR BOARD		J6 - J7		TERMINATOR BOARD		SIGNAL NAME
Live	Ground	Live	Ground	Live	Ground	
J11-1	J11-2	1	15	J1-1	J1-2	LOAD ON-LINE (LOL)
B	2	2	16	B	2	OVERWRITE (OVW)
C	3	3	17	C	3	SYNCHRONOUS FORWARD (SFC)
D	4			D	4	
E	5	4	18	E	5	SYNCHRONOUS REVERSE (SRC)
F	6	5	19	F	6	DATA DENSITY INDICATOR (DDI)
H	7	6	20	H	7	REWIND Command (RWC)
J	8	7	21	J	8	SELECT (SLT)
K	9	8	22	K	9	SET WRITE STATUS (SWS)
L	10	9	23	L	10	OFF-LINE Command (OFC)
M	11	10	24	M	11	ON-LINE (ONL)
N	12			N	12	
P	13	11	25	P	13	FILE PROTECT (FPT)
R	14	12	26	R	14	LOAD POINT (LDP)
S	15			S	15	
T	16	13	27	T	16	READY (RDY)
U	17	28	41	U	17	END OF TAPE (EOT)
J11-V	J11-18			J1-V	J1-18	
J12-A	J12-1	29	42	J2-A	J2-1	WRITE DATA STROBE (WDS)
B	2	30	43	B	2	
C	3	31	44	C	3	WRITE AMPLIFIER RESET (WARS)
D	4	36	48	D	4	
E	5			E	5	
F	6			F	6	
H	7	37	49	H	7	
J	8			J	8	
K	9			K	9	
L	10	32	45	L	10	(WDP)
M	11	34	46	M	11	(WD0)
N	12	35	47	N	12	(WD1)
P	13	56	68	P	13	(WD2)
R	14	57	69	R	14	WRITE DATA (WD3)
S	15	58	70	S	15	(WD4)
T	16	59	71	T	16	(WD5)
U	17	60	72	U	17	(WD6)
J12-V	J12-18	61	74	J2-V	J2-18	(WD7)
J13-1	J13-A	62	75	J3-1	J3-A	(RDP)
2	B	63	76	2	B	
3	C	64	77	3	C	READ DATA (RD0)
4	D	78	92	4	D	(RD1)
5	E	79	93	5	E	5 VOLT
6	F	80	94	6	F	5 VOLT
7	H	81	95	7	H	5 VOLT
8	J	82	96	8	J	(RD2)
9	K	83	97	9	K	READ DATA (RD3)
10	L	84	98	10	L	
11	M			11	M	
12	N			12	N	
13	P			13	P	
14	R	85	99	14	R	(RD4)
15	S	86	100	15	S	(RD5)
16	T			16	T	READ DATA
17	U	87	101	17	U	(RD6)
J13-18	J13-V	88	102	J3-18	J3-V	(RD7)

Table 23.6 INTERCONNECTION BETWEEN TWO TAPE UNITS

23.4 HARDWARE SOFTWARE INTERFACE DETAILS

23.4.1 COMMANDS

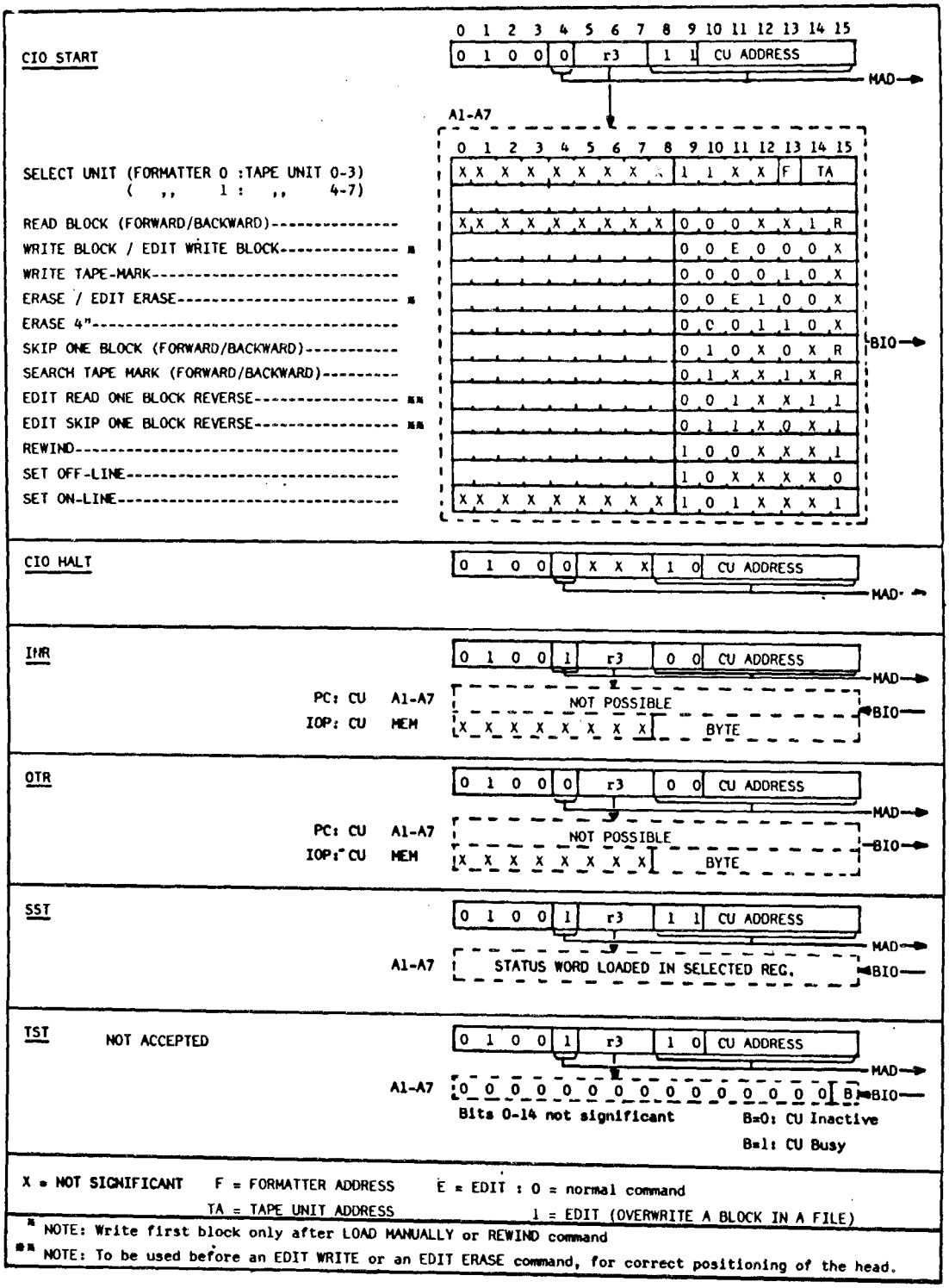
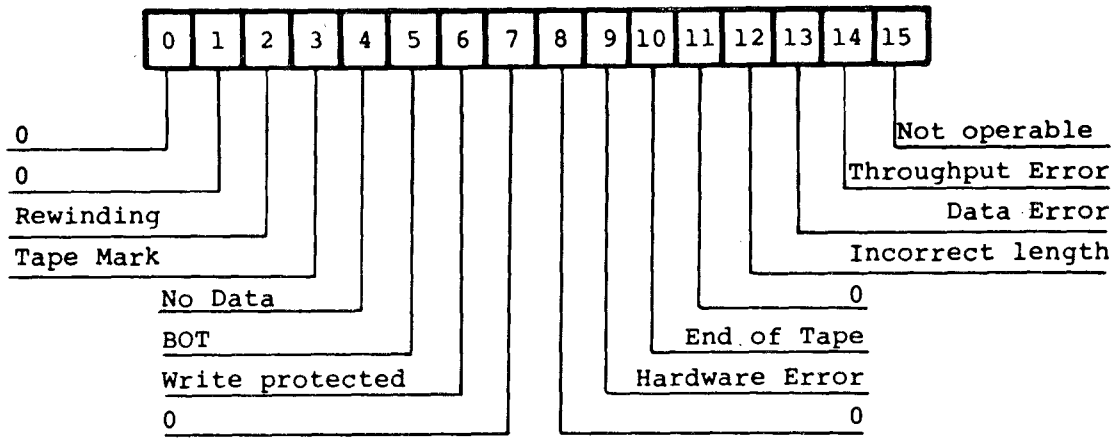


Figure 23.6 INSTRUCTION -/COMMAND-WORD FORMATS

23.4.2 STATUS WORD



Bit	Function	Meaning
0	-	
1	-	
2	Rewinding	Set if the selected transport is rewinding.
3	Tape Mark	Set if the last read/written block was a Tape Mark. It suppresses bit 13 "Data Error".
4	No Data	Set if no data is found within 2 seconds during a read/write command. Also set after a successful erase command.
5	BOT	Set when BOT is reached and the transport is at rest.
6	Write protected	Set if a tape or reel, without a Write Enable ring installed, is mounted on the transport. Set to zero if the selected transport is OFF line.
9	Hardware Error	Set if the transport does not begin the execution of the given command within 2 seconds.
10	End of tape	Set when the EOT is reached or passed on the tape.
11	-	
12	Incorrect length	Set if the number of characters transferred during reading is less than the number of characters in the block.
13	Data Error	Set when a read error has been detected by the formatter (CER or HER) or by the CHMT as parity error. This status bit is not set when a Tape Mark is detected.
14	Throughput Error	Set if an OTR, INR or CIO halt instruction is delayed more than 20 µs after a Break is emitted during a read, write or erase command. This status bit is not set if bit 12, Incorrect length, is set.
15	Not Operable	Set if the selected transport is not On-line.

23.5 DESCRIPTION TESTPROGRAM

MAGNETIC TAPE UNIT TESTPROGRAM

MTUTST

Applicable to Philips Magnetic Tape Unit PTS 6872-001(2) or PTS 6186
Procedure 12NC: 8701-740-41000

MTUTST package includes:
Procedure
Listing
Cassette

GENERAL DESCRIPTION

MTUTST is a test program for the Magnetic Tape Unit (MTU) PTS 6872–001 (2) or PTS 6186.

It tests the tape recorder, formatter plus other units which make up the MTU.

The program is run from the TC 6810 SOP panel. Results of the tests are displayed on the SOP panel lamps.

The program tests all commands given by the channel card CHMT together with control of all the status bits which CHMT can raise after execution of a command.

The program contains 24 short tests for control of individual commands, a longer test (TEST 1) which executes all commands and checks the equivalent status bits raised, and a read/write test (TEST 2) which writes, reads and compares data using the whole tape length until it is interrupted:

For normal testing, tests 1 and 2 are run plus write protect and end of tape test (see General Verification Procedure).

TESTABLE CONFIGURATION

- TC 6810 computer + CPU
- Minimum Memory 4K
- Cassette Drive or Flexible Disk to load the program
- A Multiplexor or I/O Processor for operation in multiplex mode
- MTU PTS 6872-001 (2) or MTU PTS 6168 and associated controller card CHMT PTS 6842–00

NOTE! Original pre-series versions of CHMT card (5131 101 0784) will not accept the test program. Cards with modification AO1867 will accept the program.

The SOP is dedicated as follows:

Switch	Function	Lamp	Function
0 —	IPL	0 —	Power on
1	Select tests	1	Test code
2		2	
3		3	
4		4	
5		5	
6		6	
7		7	
8		8	
9		9	
10		10 —	Error
11 —	Lamp test	11 —	Test completed

Program loading and normal running

On Computer:

- Set 3 position switch on SOP panel to 'NO RTC'.
- Press IPL switch.
- Load program casette in recorder (or diskette in FDD) and depress either:
  SW1 (left hand cassette unit or disk drive)
  or SW2 (right hand cassette unit or disk drive).

Lamp 1 lights indicating program loading. Lamp goes out when loading is complete.
Set 3 position switch to 'RTC'.

On MTU:

- Load a scratch (empty) tape on MTU

For PTS 6872 press switches 5 and 8
For PTS 6168 press switches 5 and 9
For PTS 6872-001 plus PTS 6872-002 press switches 5 and 7.

The program consists of 2 parts:

- 24 short tests which can be run individually by selecting the appropriate switches, or all together by selecting 'TEST 1'
- 'TEST 2', which is a read/write test.

The test to be run is selected by pressing two switches in sequence as follows:
Test–Codes (Two switches on SOP must be pressed)

Switch Code	Test Description	Switch Code	Test Description
4 & 9	TEST 1	3 & 5	ERASE 4 INCHES
5 & 6	TEST 2	3 & 6	SKIP ONE BLOCK FWD
1 & 2	SELECT 0	3 & 7	SKIP ONE BLOCK REV.
1 & 3	SELECT 1	3 & 8	SEARCH TAPE MARK FWD
1 & 4	SELECT 2	3 & 9	SEARCH TAPE MARK REV.

Switch Code	Test Description	Switch Code	Test Description
1 & 5	SELECT 3	4 & 5	EDIT WRITE BLOCK
1 & 6	SELECT 4		(40 characters)
1 & 7	SELECT 5	4 & 6	EDIT ERASE
1 & 8	SELECT 6		(40 characters)
1 & 9	SELECT 7	4 & 7	EDIT READ BLOCK REV.
2 & 3	SET 'OFF LINE'		(20 characters)
2 & 4	SET 'ON LINE'	4 & 8	EDIT SKIP BLOCK REV.
	(6872 only)	9 & 9	STATUS
2 & 5	SEARCH BOT	10 & 10	CLEAR LAMPS
2 & 6	READ BLOCK		(All SOP lamps extinguished)
	(40 characters)		
2 & 7	READ BLOCK REVERSE		
	(40 characters)		
2 & 8	WRITE BLOCK		
	(40 characters)		
2 & 9	WRITE TAPE MARK		
3 & 4	ERASE		
	(40 characters)		

TEST 1

Before running test 1 move the tape past BOT, e.g. by code 26 (6168 and 6872). Then (6872 only) switch off and on the tape drive to make the tension arms go to retracted position. This should be done to check that the SET 'ON LINE' command will be correctly executed by the drive.

The sequence of the short tests in TEST 1 is as follows:

Test	Status	Remarks
12	11	K59 Status–
24	–	
13	11	
24	–	K58 and K59: Status 6 plus 11
14	11	
15	11	
16	11	
17	11	
18	11	
19	11	
12	–	
*23	11	K57: Test-start on MTU 2
24	–	
25	1 }	Command 25 repeated until status 4 comes
25	4 }	Time out = 3 minutes
29	2	
27	2	
27	3+4	
36	2	
28	– }	Repeated 25 times. 40 characters in every block
28	– }	
29	2	
27	2	
27	–	Read data compared with Write Data

Test	Status	Remarks
38	2	
28	–	Repeated 10 times
28	–	
29	2	
47	2	
47	8	Repeated 5 times. Status 7 achieved intentionally
47	8	Only 20 characters read
45	–	Data different to that for test 28
36	–	
36	–	
48	–	
46	3	
39	2	
26	2	
26	–	Repeated 9 times. Blocks nos 1–5 with ordinary data
26	–	Block 6 with special data. Block 7 with ordinary data
		Block 8 missing. Blocks 8 and 10 with ordinary data
26	2	
35	3	K57 and K58: repeated 20 times
35	3	K59: repeated 10 times
39	3	
39	2	
26	2	
26	3	
39	3	If status = 2 next test not carried out
39	2	
37	–	
26	10	Status intentionally received through
28	10	disconnection of MUX
28	–	
29	2	
28	–	Block with 2000 characters
28	–	
37	–	
37	–	
34	3	A half length block erased
37	2	
26	2	
26	3+9	Status 3 means no data to memory
		Status 9 means formatter has found a half block but has not transferred it
26	–	Next block correct
25	1	
23	11	
14	11	
24	6+11	
13	–	K57 first time (MTU1): status–
		K57 second time (MTU2) * K58 and K59 status 11
*		K57 first time (MTU1): Program jumps back to test marked * for test of MTU2.
		K57 second time (MTU2), K58 and K59: Test complete

When test 1 has run successfully, indicator lamps 2, 4 and 11 light.

Status indication should then be 6 + 11. (Press switches 9 & 9 for status)

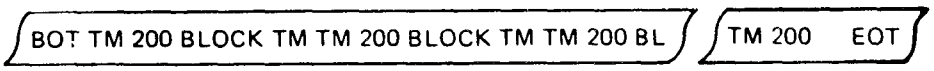
Sequence of test 2

Select type of MTU by pressing switches 5 & 7, 5 & 8 or 5 & 9. With 5 & 9 'ON LINE' switch on tep drive must be pressed. Unit number must then be selected (normally unit 0—test code 1 & 2).

Press switches 5 & 6.

Tape Unit seeks BOT first. Then a Tape mark is written followed by 200 blocks, whos length and contents come from a random number generator, then a new tape mark after the block. The tape unit then seeks reverse to the first tape mark at the beginning of the block and compares the read data with the written data. The unit continues to write blocks of data, read and compare them in this way until EOT mark is reached. The tape is then rewound to BOT and the test repeated. To STOP the test put the MTU 'OFF-LINE' by pressing the 'ON-LINE' switch.

The tape format after test 2 is shown in figure below.



Normal Indication

While a test is running the lamps corresponding to the switch code for that test are lit. On successful completion of a test, lamp 11 lights as well.

Error Indication

If a test fails, the error lamp 10 lights and the program stops. The failing test is indicated by the two lamps corresponding to the switch code of the short test.

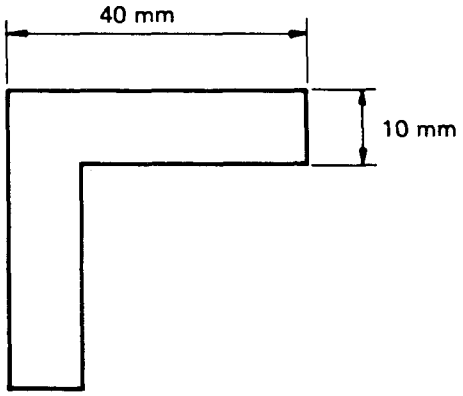
Pressing switch 9 twice gives the status as follows:

Lamp	Status	Lamp	Status
0		6	HARD WARE ERROR
1	REWIND	7	EOT
2	TAPE MARK	8	INCORRECT LENGHT
3	NO DATA	9	DATA ERROR
4	BOT	10	THROUGHPUT ERROR
5	WRITE PROTECT	11	NOT OPERABLE

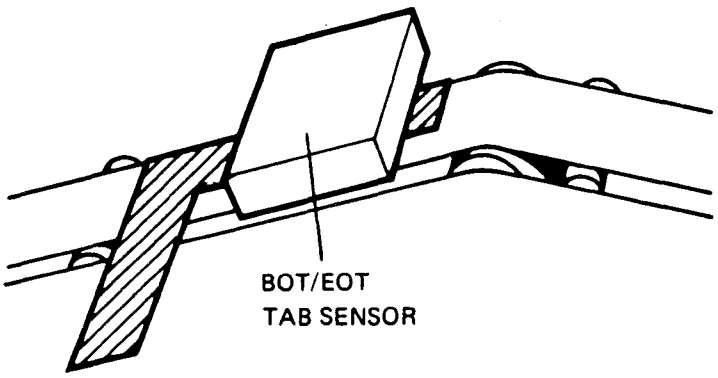
GENERAL VERIFICATION PROCEDURE

To check that MTU is functioning correctly the following 4 verification tests should be performed:

1. Test 1 (code 49)
2. Test 2 (code 56)
3. Write Protect Test.
   Remove rubber ring from the magnetic tape thus write protecting the tape.
   Replace the tape on the MTU and run the tape forward past BOT.
   Press 'ON LINE' switch.
   Choose SELCT 0 (code 12).
   When lamp 11 lights press switch 9 twice to read status.
   Lamp 5 should light indicating write protect status.
   Replace rubber ring.
4. EOT test
   Cut out a pice of white paper as shown



Press switches 5 and 6 (test 2).
Stop the tape drive by pressing the 'ON LINE' switch. Put the tape drive 'ON LINE' again.
Don't stop at BOT!
Place the paper between the tape and the BOT/EOT sensor as shown below.



Check status (test code 9 & 9).
Lamp 7 – EOT should be lit.

To avoid damage to the tape, don't use the L-shaped paper when running the tape.

If a Computer Full Panel is fitted, more elaborate checks, such as looping on a faulty test, can be performed – for more information see 'De-bugger use' document TSB 30/75.

```
00000                          IDENT    CHMTGS                  10-09-1982  G SMIT
00001                     *ALL CHMT (PTS 6842) COMMANDS CAN BE TESTED.
00002                     *ALL SOP INDICATORS ARE ON AFTER PROGRAM IS LOADED
00003                     *THE COMMANDS MUST BE SPECIFIED, ONE BY ONE VIA SOP PANEL:
00004                     *
00005                     *  SELECT UNIT                  :SOP SWITCH 4,5 (8,9,10=UNIT NR)
00006                     *  READ BLOCK FORWARD           :           9
00007                     *  READ BLOCK REVERSE           :           9,10
00008                     *  WRITE BLOCK                  :           --
00009                     *  WRITE TAPE MARK              :           8
00010                     *  ERASE                        :           7
00011                     *  ERASE 4 INCH                 :           7,8
00012                     *  SKIP ONE BLOCK FORWARD       :           5
00013                     *  ,,  ,,  ,,  REVERSE          :           5,10
00014                     *  SEARCH TAPE MARK FORWARD     :           5,8
00015                     *  ,,  ,,  ,, REVERSE           :           5,8,10
00016                     *  EDIT WRITE BLOCK             :           6
00017                     *  EDIT ERASE                   :           6,7
00018                     *  EDIT READ BLOCK REVERSE      :           6,9,10
00019                     *  EDIT SKIP ONE BLOCK REVERSE  :           5,6,10
00020                     *  REWIND                       :           4,10
00021                     *  SET OFF-LINE                 :           4
00022                     *  SET ON-LINE                  :           4,6,10
00023                     *
00024                     *FOR REPEAT COMMAND FUNCTION, PRESS SOP SW.  3
00025                     *TO START COMMAND EXECUTION,PRESS   SOP SW.  1
00026                     *TO STOP REPEAT COMMAND EXECUTION, PRESS SOP SW. 1 AGAIN
00027                     *STATUS BITS 5-15 ARE DISPLAYED ON SOP INDICATORS
00028                     *PRESS A SOP SWITCH (NOT SW 1) TO DISPLAY STATUS AND INPUT CHARS
00029                     *PRESS SOP SWITCH 1 TO CONTINUE
00030                     *ENTER NEXT COMMAND WHEN ALL SOP INDICATORS ARE ON
00031                     *
00032  0000                             RES      /40
00033  0080  FFFF                       DATA     /FFFF,0
       0082  0000
00034        000C        ADR          EQU      /0C
00035  0084  208F        START        INH
00036                    *FETCH COMMAND BITS FROM SOP
00037  0086  41EE                       CIO      A1,1,/2E                START SOP
00038  0088  8320        NEWCOM       LDKL     A3,/7FF                 PROGRAM LOADED INDICATION
       008A  07FF
00039  008C  432E                       OTR      A3,0,/2E                DISPLAY ON SOP
00040  008E  8220                       LDKL     A2,/400                 MASK SOP SWITCH 1
       0090  0400
00041  0092  0300                       LDK      A3,0                    CLEAR COMMAND REG
00042  0094  4C2E        NEXBIT       INR      A1,0,/2E                COMMAND BIT FROM SOP
00043  0096  5C04                       RB(NA)   *-2                     WAIT TIL SOP SWITCH IS PRESSED
00044  0098  9104                       ADR      A1,A1                   SHIFT 1 BIT POS LEFT FOR SOP DISPLAY
00045  009A  B304                       XRR      A3,A1                   LOAD COMMAND INTO A3
00046  009C  432E                       OTR      A3,0,/2E                DISPLAY ENTERED COMMAND BITS
00047  009E  A109                       TM       A1,A2                   INITIATE? (SOP SWITCH 1)
00048  00A0  580E                       RB(Z)    NEXBIT                  NEXT COMMAND BIT FROM SOP
00049  00A2  3BE1                       SRC      A3,1                    (A3) BACK TO CORRECT POS.
00050                    *PREPARE IOP DEPENDING ON COMMAND
00051  00A4  0402                       LDK      A4,2
00052  00A6  A40C                       ANR      A4,A3                   COULD IT BE A DATA OUTPUT COMMAND?
00053  00A8  500A                       RF(Z)    OTR                     IF YES, GO TO OTR
00054  00AA  8520                       LDKL     A5,/100                 256 BYTES INPUT MODE
       00AC  0100
00055  00AE  7518                       WER      A5,ADR+ADR
00056  00B0  7519                       WER      A5,ADR+ADR+1            INPUT BUFFER ADDRESS : /100
00057  00B2  570C                       RF       INIT
00058  00B4  8520        OTR          LDKL     A5,/4100                256 BYTES OUTPUT MODE
       00B6  4100
00059  00B8  7518                       WER      A5,ADR+ADR
00060  00BA  8520                       LDKL     A5,BUF                  BUFFER ADDRESS TO IOP
       00BC  00EC  R
00061  00BE  7519                       WER      A5,ADR+ADR+1
00062                    *INITIATE THE COMMAND
00063  00C0  43CC        INIT         CIO      A3,1,ADR                START COMMAND
00064  00C2  4ECC                       SST      A6,ADR
00065  00C4  5C04                       RB(NA)   *-2
00066  00C6  8641                       ST       A6,/FE                  STATUS WORD IN FRONT OF INPUT BUF
       00C8  00FE
00067  00CA  462E                       OTR      A6,0,/2E                STATUS BITS 5-15 TO SOP
00068  00CC  0480                       LDK      A4,/80                  REPEAT FUNCTION MASK
00069  00CE  A40C                       ANR      A4,A3                   WAS IT REPEAT MODE?
00070  00D0  5004                       RF(Z)    NEXTC                   NEXT COMMAND
00071  00D2  492E                       INR      A1,0,/2E                REPEAT IF NO SOP SWITCH WAS PRESSED
00072  00D4  5C16                       RB(NA)   INIT
00073                    *RESTART AFTER STATUS IS DISPLAYED
00074  00D6  8720        NEXTC        LDKL     A7,/FE                  INPUT BUFFER START ADDRESS
       00D8  00FE
00075  00DA  492E        NEXT         INR      A1,0,/2E                (FIRST 2 BYTES = STATUS WORD)
00076  00DC  5C04                       RB(NA)   *-2                     WAIT FOR SOP SWITCH PRESSED
00077  00DE  9104                       ADR      A1,A1                   SHIFT TO CORRECT LAMP POS
00078  00E0  A109                       TM       A1,A2                   SOP SWITCH ONE?
00079  00E2  5C5C                       RB(NZ)   NEWCOM                  IF YES, TO NEW COMMAND
00080  00E4  E43C                       LCR      A4,A7                   FETCH CHARACTER FROM INPUT BUFFER
00081  00E6  442E                       OTR      A4,0,/2E                DISPLAY STATUS + INPUT DATA
00082  00E8  1701                       ADK      A7,1                    NEXT CHAR ADDRESS
00083  00EA  5F12                       RB       NEXT
00084  00EC  0000        BUF          DATA     0
00085  00EE  FFFF                       DATA     /FFFF,0,/FFFF,0
       00F0  0000
       00F2  FFFF
       00F4  0000
00086  00F6  FFFF                       DATA     /FFFF,0,/FFFF,0
       00F8  0000
       00FA  FFFF
       00FC  0000
00087  00FE  FFFF                       DATA     /FFFF,0,/FFFF,0
       0100  0000
       0102  FFFF
       0104  0000
00088                                   END      START
```

LIST OF ILLUSTRATIONS

LIST OF TABLES

24.1 CHHD-IDENTIFICATIONS

Type- Number:	PTS 6886, P825-041 (BIGD2)
Testprogram:	TIGD2C (for HDU) TIGD2S (for CDU)
Channel:	DMA OKI 3B16, OKO 3A16
Devices:	PTS 6961 HDU, 16 + 16M (CDC 9448/32M) PTS 6962 HDU, 16 + 80M (CDC 9448/96M) PTS 6877 CDU, 80M (CDC 9762) Cartridge HDU: CDC 91204 Disk pack CDU: CDC 9877
Power consumption	+5V 4.5A -5V 0.8A

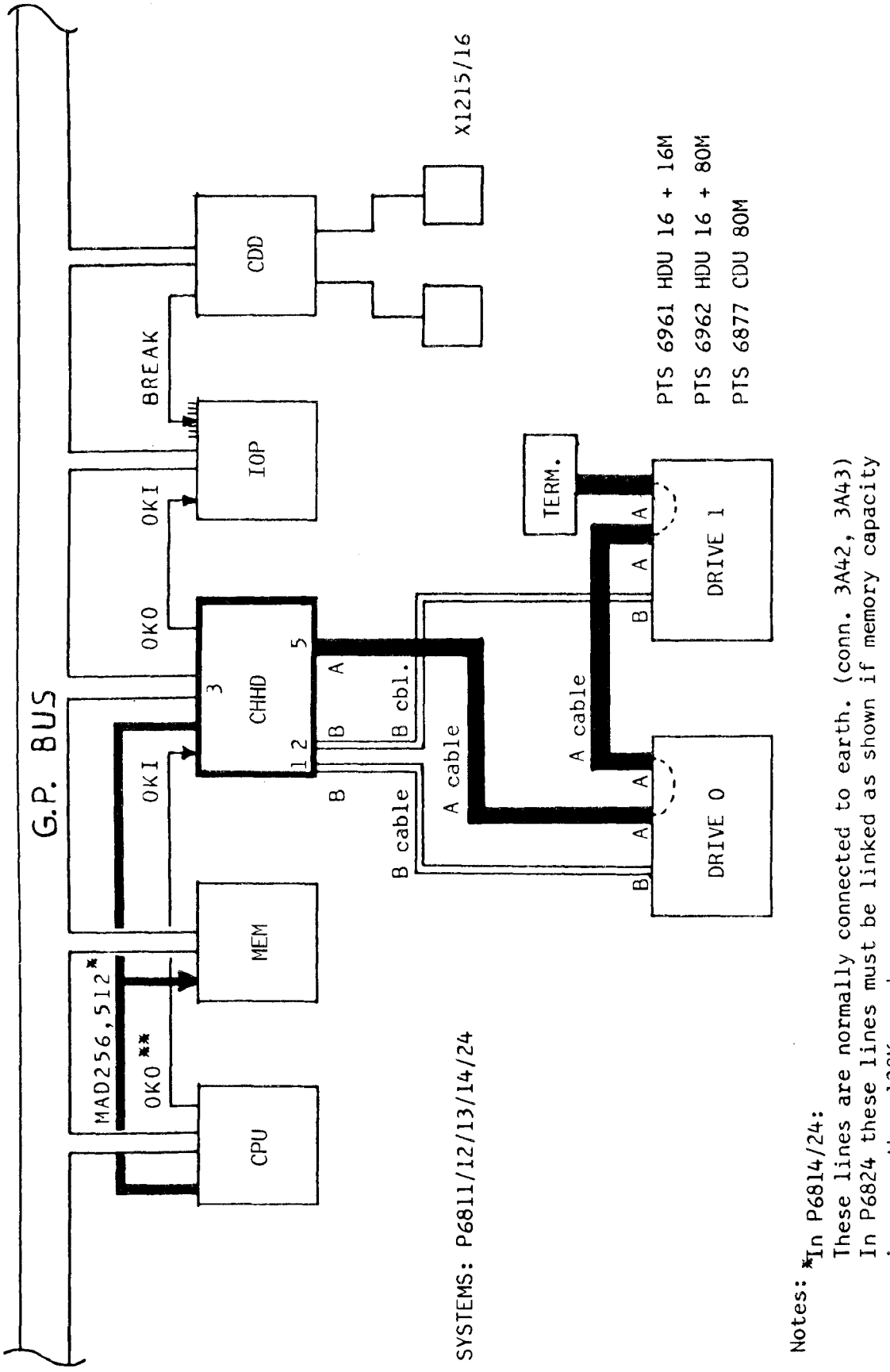


Figure 24.1 SYSTEM OVERVIEW WITH CHHD

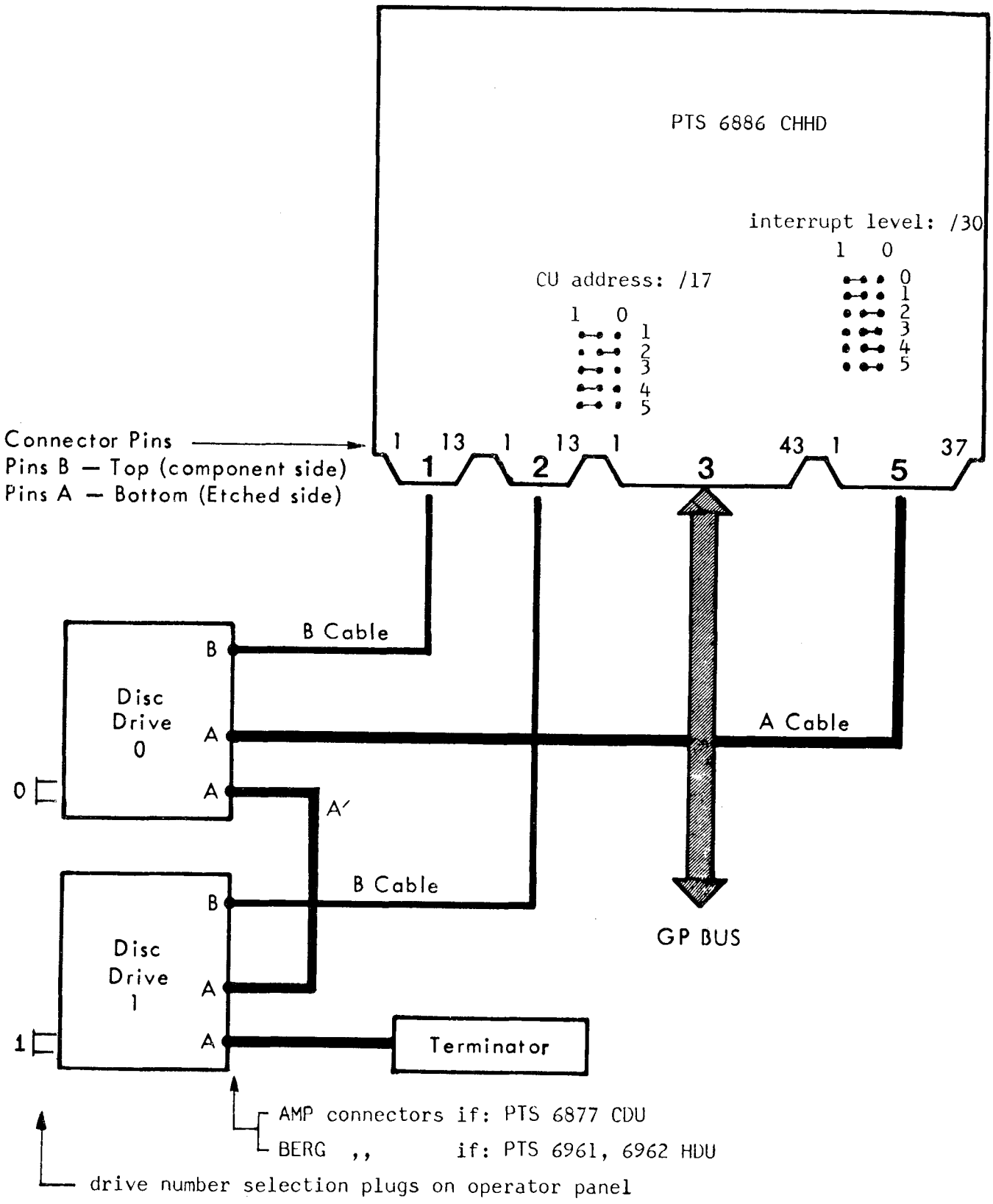


Figure 24.2 STRAPSETTING AND INTERFACE CONNECTORS

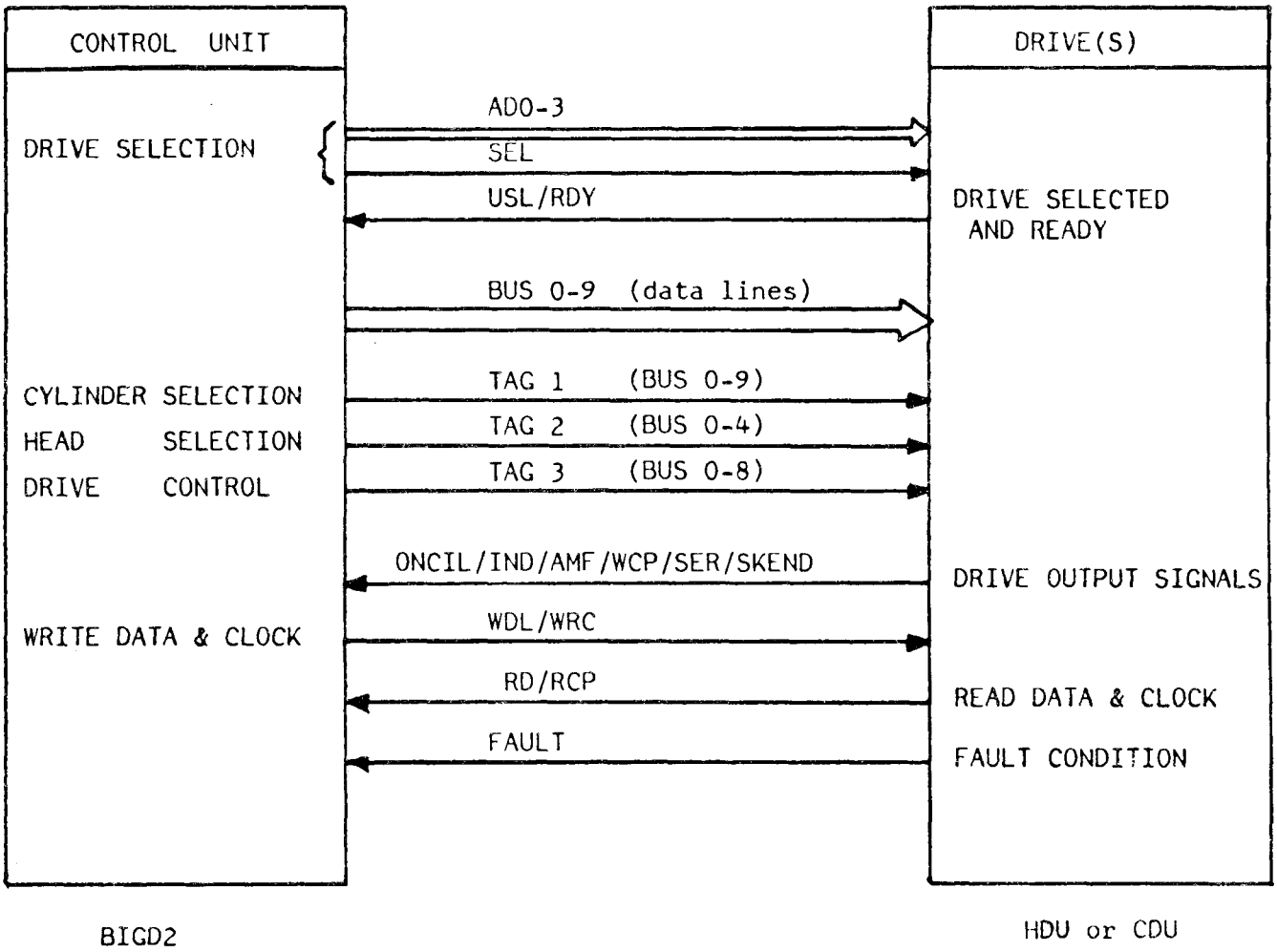


Figure 24.3 INTERFACE SIGNALS CU - DRIVES

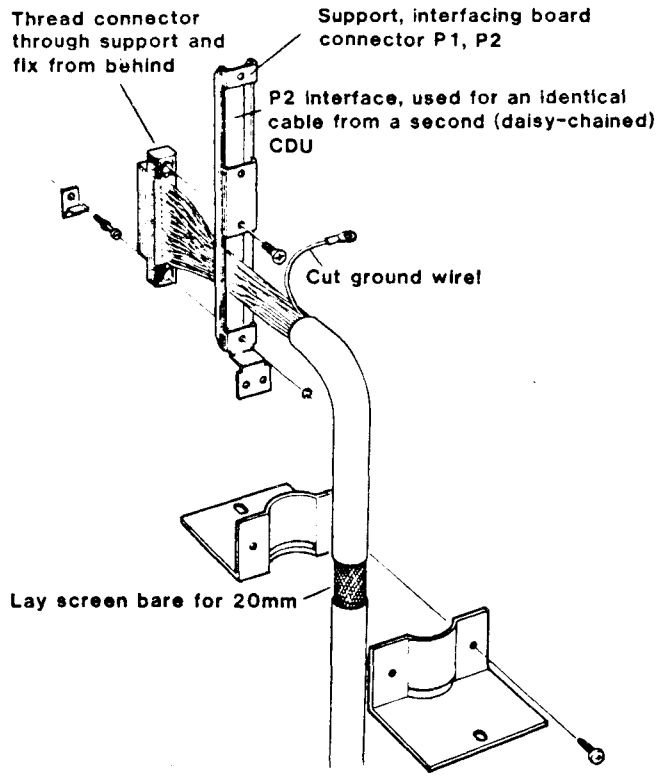


Figure 24.4 ENTRY KIT FOR B-CABLE FROM CDU 6877

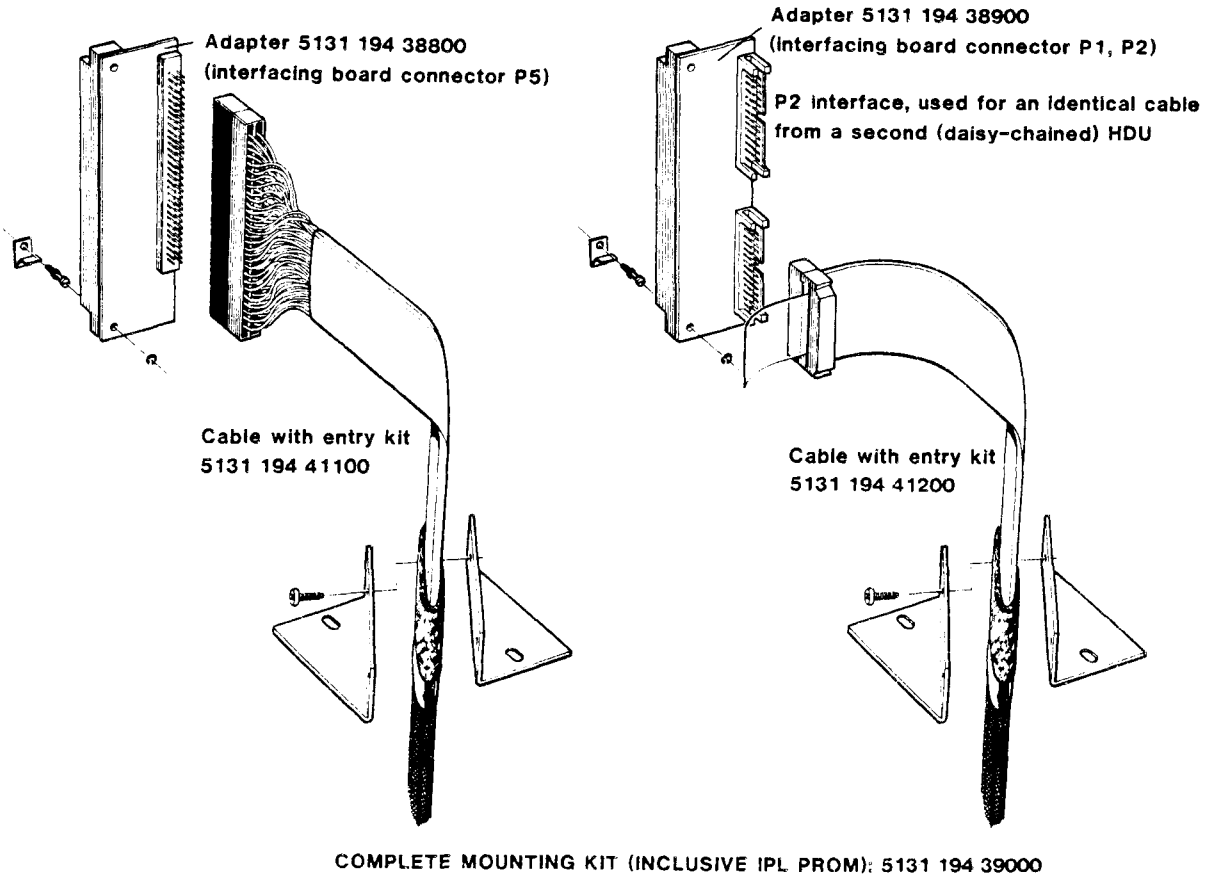


Figure 24.5 ENTRY KITS FOR CABLES FROM HDU 6981/62

Signal	Con. 5	AMP Con.	Device Name, Remarks	BERG
A Cable Output Signals				
SEL, N	A37, B37	25, 22	UNIT SELECT, Disc Selection	52, 22
TAG1, N	A12, B12	49, 46	Cylinder Selection	31, 1
TAG2, N	A13, B13	51, 48	Head Selection	32, 2
TAG3, N	A25, B25	55, 52	Control Selection	33, 3
BUS0, N	A8, B8	26, 23		34, 4
BUS1, N	A9, B9	27, 24		35, 5
BUS2, N	A10, B10	31, 28		36, 6
BUS3, N	A11, B11	32, 29		37, 7
BUS4, N	A31, B31	33, 30	Bit 0-9, Data Lines	38, 8
BUS5, N	A32, B32	37, 34		39, 9
BUS6, N	A33, B33	38, 35		40, 10
BUS7, N	A34, B34	39, 36		41, 11
BUS8, N	A35, B35	43, 40		42, 12
BUS9, N	A36, B36	44, 41		43, 13
AD0, N	A7, B7	4, 1		53, 23
AD1, N	A28, B28	5, 2		54, 24
AD2, N	A29, B29	7, 3	UNIT SELECT 0-3, Disc Address	56, 26
AD3, N	A30, B30	12, 8		57, 27
OCD, N	A6, B6	20, 16	Open Cable Detector	44, 14
A Cable Input Signals				
IND, N	A3, B3	13, 10	INDEX Pulse	48, 18
SEC, N	A27, B27	77, 74	Not Used (grounded)	55, 25
SER, N	A5, B5	78, 75	SEEK ERROR	46, 16
ONCIL, N	A1, B1	18, 15	ON CYLINDER	47, 17
RDY, N	A4, B4	21, 17	UNIT READY	49, 19
AMF, N	A2, B2	45, 42	ADDRESS MARK FOUND	50, 20
FAULT, N	A26, B26	14, 11	Not Used (grounded)	45, 15
INHA	A14 B14		Strap	
B Cable Output Signals (1 set for each disc) disc0 = con.1 disc1 = con.2				
WDL, N	B1, B2	B, A	Write Data Line (bit serial)	20, 8
Ground	B5	D		7
WRC, N	A11, A12	J, H	Write Clock	19, 6
Ground	B11	E		18
B Cable Input Signals (1 set for each disc)				
RCP, N	A1, A2	X, W	Read Clock Pulse	17, 5
Ground	B3	Y		4
RD, N	A3, A4	V, U	Read Data (bit serial from disc)	16, 3
Ground	B4	T		15
WCP, N	A9, A10	N, M	SERVO CLOCK, Write Clock Pulse	14, 2
Ground	B10	K		1
SKEND,	A5, A6	CC, AA	Seek End	23, 10
USL,	A7, A8	BB, DD	Unit Selected	9, 22
				21
INHB	B6 B7		Strap	

Conversion cable A 51111996149.
,, ,, B ,, 6148.

Table 24.1 CU - DEVICE INTERFACE

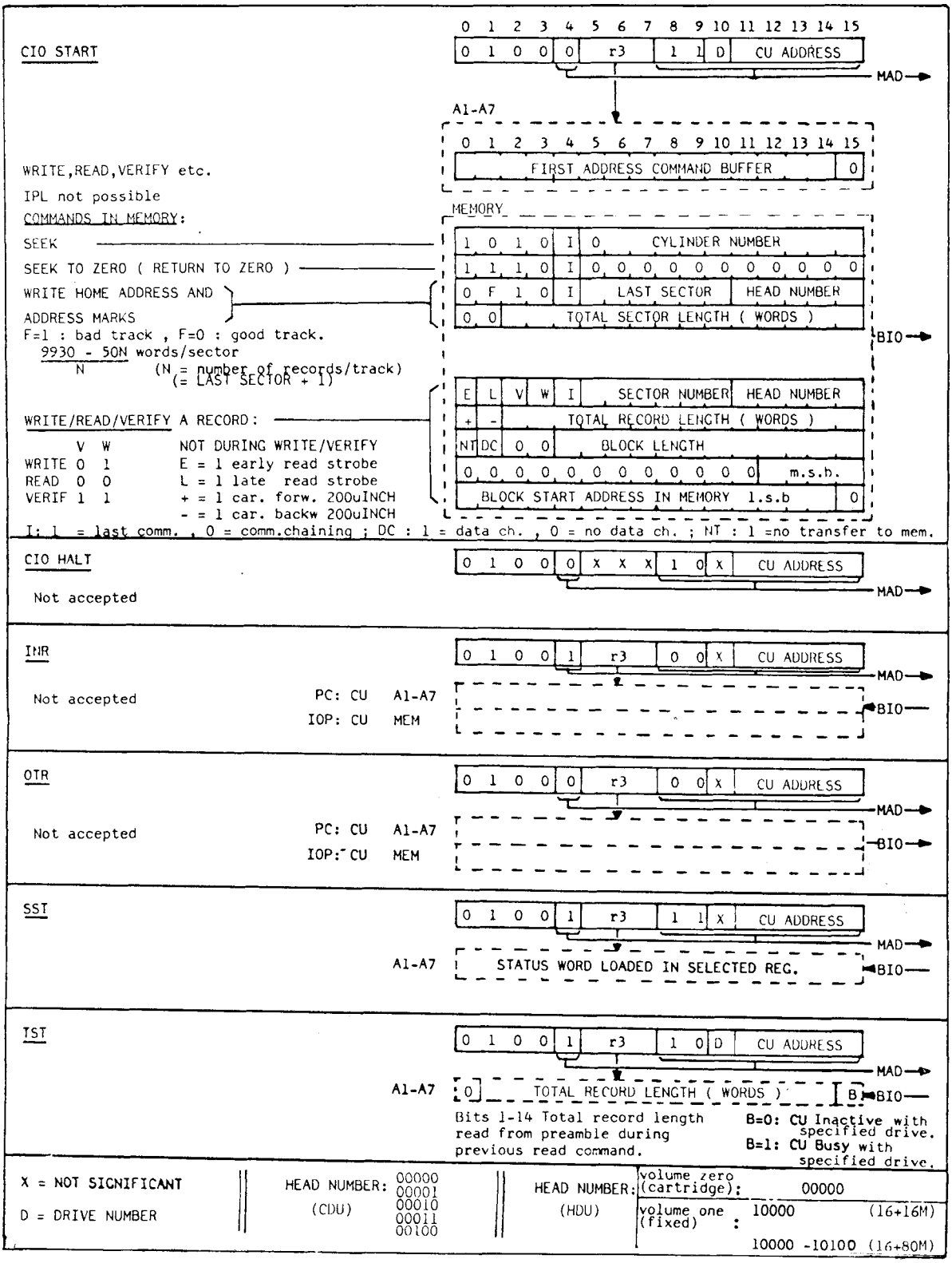
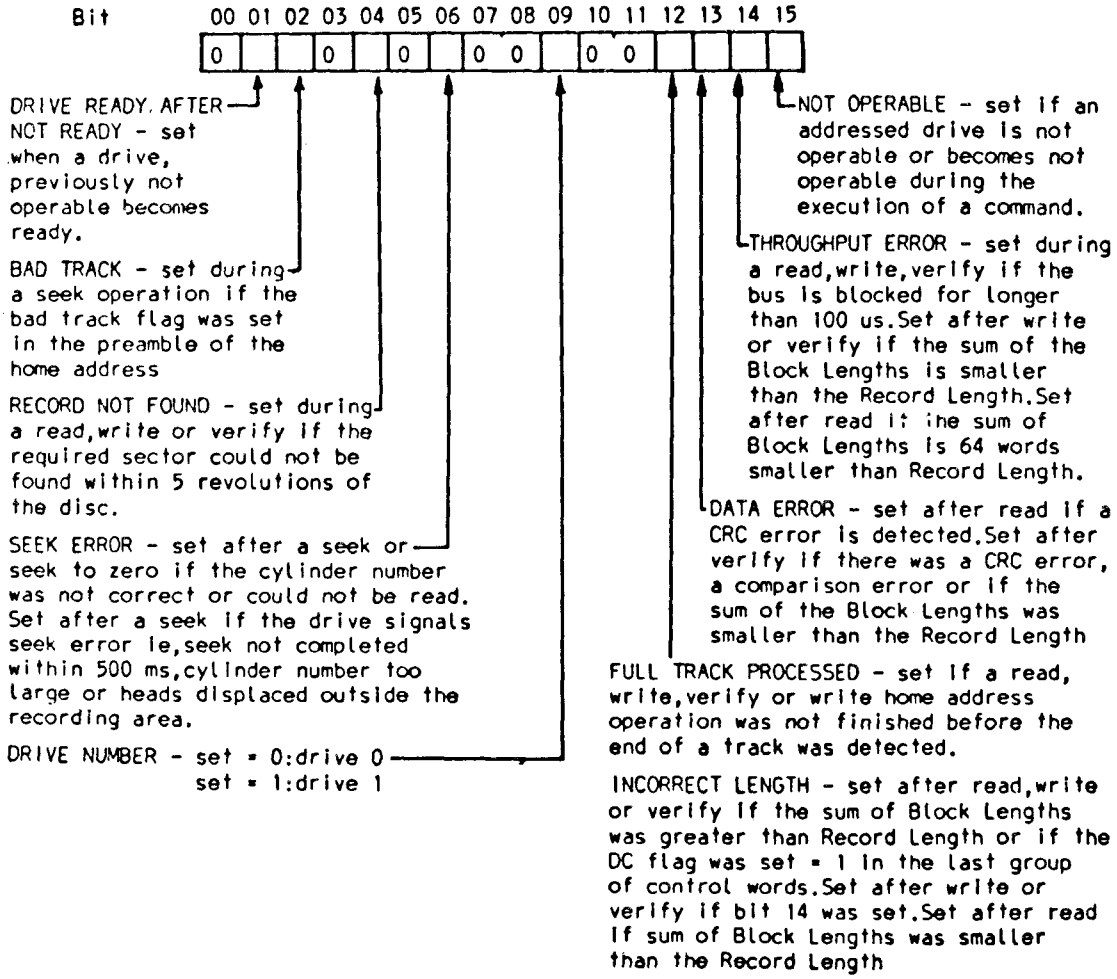


Figure 24.6 INSTRUCTION-/COMMAND-WORD FORMATS

24.4.1 STATUS WORD



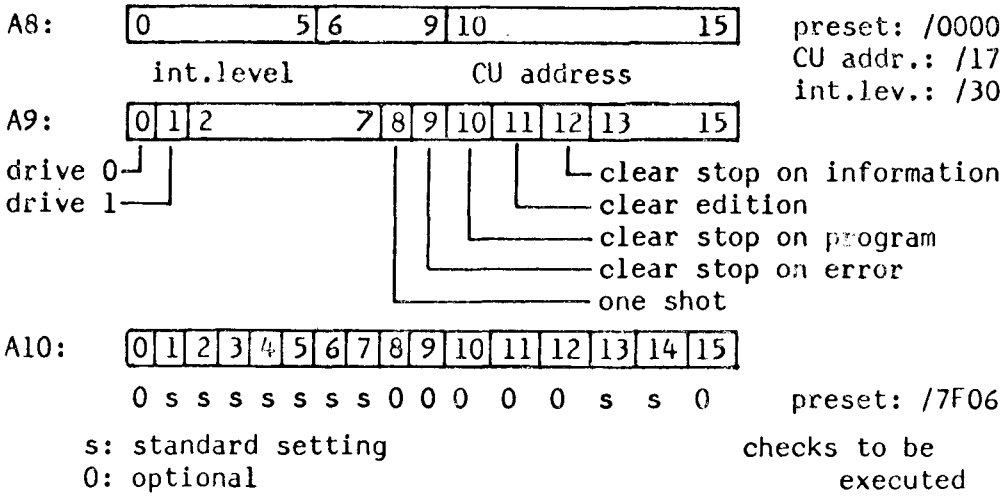
24.5 SHORT DESCRIPTION TEST-PROGRAM

TEST-PROGRAM TIGD2C 32K

1) disk drive loaded with a scratch cartridge must be ready.
IPL
program simulates stop at /700 (SOP indicators 2,3,4 on)

2) switch on RTC

3) Press SOP switch 10 if register A9 (bits 8-12) and
register A10 have to be modified



4) program will ask for the following parameters after modification
of the registers or after depressing SOP switch 9:

-CU address?

-interrupt level?

-unit selected (unit 0, or unit 1, or both) ?

-for each unit: -Do you want to test the fixed disk? (Y or N)
- ,, removable ,, (Y or N)
-If fixed disk, what type ? 16M (0)
48M (1)
80M (2)

program starts running

error stop: /5F0 is simulated on SOP

interrupts return: /700 is simulated on SOP
information stop: /5E0 is simulated on SOP

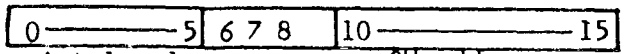
for more information, see detailed description of test-program

1) disk drive loaded with a scratch pack must be ready.
IPL
program simulates stop at /700 (SOP indicators 2,3,4 on).

2) switch on RTC

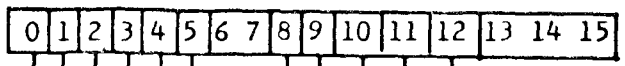
3) press SOP switch 10 if the registers A8,9,10 have to be modified.

A8:

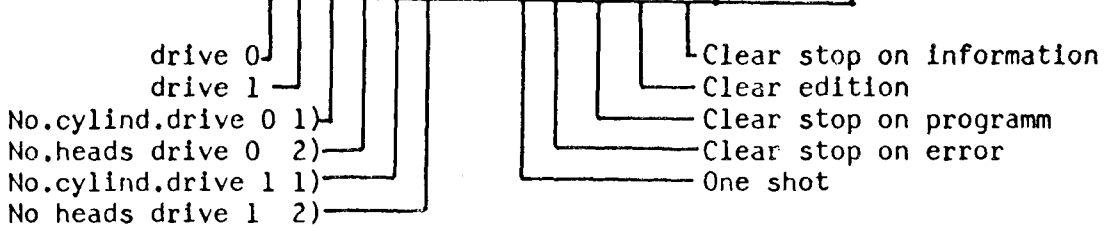


Preset /8016
CU addr. :/16
int-level: /20

A9:

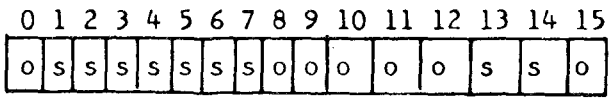


Preset: /8000



Note 1): Bit 2,4: 0= 411 cylinders, 40Mb/150Mb
1= 823 cylinders, 80Mb/300Mb
Note 2): Bit 3,5: 0= 5 heads, 40Mb/80Mb
1= 19 heads, 150Mb/300Mb

A10:



Preset: /7F06

Checks to be executed

s: standard setting
o: optional

4) program starts after modification of the registers
or after depressing SOP switch 9.
Error stop: /5F0 is simulated on SOP.

Interrupts return: /700 is simulated on SOP.
Information stop: /5E0 is simulated on SOP.

For more information, see detailed description of test-program.

24.6 SHORT ROUTINES

```
         DATE  82-08-03        IDENT    BIGD1S


0000                           IDENT    BIGD1S
0001                    *DATE: 820803 FOR PTS
0002
0003                    *      SMALL PROGRAM FOR WRITE,SEEK,WRITE HOME ADDR. AND VERIFY
0004
0005                    *      A1       START ADDRESS COMMAND BUFFER, PRESET FOR SEEK
0006                    *      DATA BUFFER START ADDRESS IS /0100
0007
0008                           AORG     /80
0009 0080 FFFF                 DATA     /FFFF
0010 0082 0000                 DATA     0
0011 0084 0194                 LDK      A1,/94                COMMAND BUFFER FOR SEEK
0012 0086 207F          START  HLT                            AFTER RUN CHECK STATUS IN REG A4
0013 0088 20BF                 INH
0014 008A 41D7                 CIO      A1,1,/17              START CONTROLLER
0015 008C 5C04                 RB(4)    *-2
0016 008E 4CD7                 SST      A4,/17                GET STATUS
0017 0090 5C04                 RB(4)    *-2
0018 0092 5F0E                 RB       START
0019
0020                    * COMMAND BUFFER
0021
0022 0094 A000          SEEK   DATA     /A000                 SEEK TO CYLINDER 0
0023 0096 A850                 DATA     /A850                 SEEK TO CYLINDER 80
0024 0098 A000          WHAWVER DATA    /A000                 SEEK CYL. 0
0025 009A 27E0                 DATA     /27E0                 WRITE HOME ADDRESSES 64 SECTORS
0026 009C 0040                 DATA     /0040
0027 009E 1000                 DATA     /1000                 WRITE A SECTOR
0028 00A0 0040 0040            DATA     /0040,/0040
0029 00A4 0000 0100            DATA     /0000,/0100           MEMORY BUFFER
0030 00A8 3800                 DATA     /3800                 VERIFY WRITTEN SECTOR
0031 00AA 0040 0040            DATA     /0040,/0040,/0000,/0100
     00AE 0000 0100
0032
0033                           END      START

            SYMBOL TABLE

    SEEK    0094  A   START   0086  A   WHAWVE  0098  A

            ASS.ERR.    0000
  :EOF
  PROG ELAPSED TIME:  00H-00M-00S-000MS-



         DATE  82-08-03        IDENT    BIGD2


0000                           IDENT    BIGD2
0001                    *DATE: 820505 FOR PTS
0002
0003                    * SMALL PROGRAM TO PREMARK SURFACE 0
0004                    * WITH 64 SECTORS PER TRACK
0005                           AORG     /80
0006 0080 FFFF 0000            DATA     /FFFF,0
0007 0084 207F                 HLT
0008 0086 20BF          START  INH
0009 0088 8120 00AC            LDKL     A1,COBUF              COMMAND BUFFER ADDRESS
0010 008C 41D7          CIO    CIO      A1,1,/17
0011 008E 4CD7                 SST      A4,/17                GET STATUS
0012 0090 5C04                 RB(4)    *-2
0013 0092 9041 00AC            IM       COBUF                 NEXT CYL.
0014 0096 8340 00AC            LD       A3,COBUF
0015 009A EB20 A336            CWK      A3,/A336              IS IT THE LAST CYL.
0016 009E 5D14                 RB(5)    CIO                   NO,THEN THE NEXT
0017 00A0 207F                 HLT                            YES,CHECK STATUS IN A4
0018 00A2 8320 A000     AGAIN  LDKL     A3,/A000
0019 00A6 8341 00AC            ST       A3,COBUF              REPAIR COMMAND
0020 00AA 5F26                 RB       START
0021
0022                    * COMMAND BUFFER
0023
0024 00AC A000 2FE0     COBUF  DATA     /A000,/2FE0,/0040     SEEK,WHA FOR 64 SECTORS
     00B0 0040
0025
0026                           END      START

            SYMBOL TABLE

   AGAIN   00A2  A   CIO     008C  A   COBUF   00AC  A   START   0086  A

            ASS.ERR.    0000
  :EOF
  PROG ELAPSED TIME:  00H-00M-00S-000MS-
```

```
         DATE  82-08-03        IDENT    BIGD4N


0000                           IDENT    BIGD4N
0001                    *DATE: 820803 FOR PTS
0002                    *      PROGRAM FOR HEAD ADJUSTMENT FOR 80M DISC
0003                    *      CONNECTED TO BIGD1 CU OR BIGD2 CU
0004
0005
0006                                   - OPERATING BIGD4N ADJUSTMENT PROGRAM
0007                                   - LOAD PROGRAM FROM CASSETTE,DISC OR FLEXIBLE DISC
0008                                   OR WITH EFP OR CFP
0009
0010                    *      A       AFTER LOADING SOP DISPLAY /7FF (ALL LAMPS LIT
0011                    *              -DEPRESS A SOP-SWITCH
0012                    *               DISPLAY ON SOP /FF AND SEEKING FROM CYL 230-
0013                    *               235 FOR ABOUT 30 SEC.
0014                    *              -SOP DISPLAYS /004
0015                    *               HEADS AT CYL 4 FOR SERVO MEASUREMENT
0016                    *              -AFTER MEASURING OPERATE LOCAL/REMOTE
0017                    *               SWITCH ON CARD A05 IN DISC DRIVE(SW2)
0018                    *              -SOP DISPLAYS /005
0019                    *               HEADS ON CYL 5 FOR SERVO MEASURING
0020                    *              -AFTER MEASURING OPERATE SW2 ON A05
0021                    *      B       -SOP DISPLAYS /03E
0022                    *              -BY DEPRESSING OF A SOP SWITCH WITH LED LIT ABOVE
0023                    *               A HEAD IS SELECTED FOR ADJUSTMENT OR CHECKING
0024                    *               SOP SW 6,7,8,9,0 IS HEAD 4,3,2,1,0
0025                    *               DEPRESSING AN OTHER SOP SWITCH RESULTS IN A STEP
0026                    *               TO PROGRAM PART C
0027                    *               EXAMPLE:
0028                    *              -DEPRESS SOP SW 8
0029                    *               SOP DISPLAYS /A2 (ADJUST,CHECK AND FIX HEAD 2)HEADS ARE AT
0030                    *               CYL 4
0031                    *              -OPERATE SW2 ON A05
0032                    *              - SOP DISPLAYS /03E GO BACK TO A FOR SELECTING
0033                    *               OTHER HEAD OR PART C
0034
0035                    *      C       -SOP DISPLAYS /2FF
0036                    *               CONTINUES SEEK IS DONE AS IN A
0037                    *              -SOP DISPLAYS /3E
0038                    *               HEAD SELECTION IS DONE AS IN B BUT ONLY
0039                    *               FOR CHECKING ADJUSTMENT
0040                    *               EXAMPLE:
0041                    *              -DEPRESS SOP SW 8 FOR HEAD 2
0042                    *              - SOP DISPLAYS /2C2
0043                    *               HEAD AT CYL 245 AND HEAD 2 CAN BE CHECKED
0044                    *              -OPERATE SW2 ON A05
0045                    *              -SOP DISPLAYS /03E FOR SELECTION OF AN OTHER
0046                    *               HEAD
0047                    *              -IF AN OTHER SOP SWITCH(WITH NO LED LIT ABOVE)
0048                    *               IS DEPRESSED PROGRAM RESTARTS AND
0049                    *               SOP DISPLAYS /7FF GOTO A
0050
0051
0052 0000                      RES      /40
0053                           EJECT
0054 0080 FFFF 0000            DATA     /FFFF,0
0055 0084 20BF          START  INH                        NO INTERRUPTS
0056 0086 86A0 A804            LDKL     A14,/A804         SEEK TO CYL 4
0057 008A 86C1 0170 R          ST       A14,SEK245        CHANGE TO SEEK CYL 4
0058 008E 0500                 LDK      A5,0              CLEAR RETRY FLAG
0059 0090 41EE                 CIO      A1,1,/2E          START SOP
0060 0092 8320 07FF            LDKL     A3,/7FF           /7FF ON SOP
0061 0096 432E                 OTR      A3,0,/2E
0062 0098 4A2E                 INR      A2,0,/2E          READ SOP SW
0063 009A 5C04                 RB(NA)   *-2
0064 009C 03FF                 LDK      A3,/FF            DISP FIRST SEEKING
0065 009E 86A0 015C R          LDKL     A14,EOS           STACKPOINTER
0066 00A2 0700                 LDK      A7,0              FLAG FIRST TIME
0067      00A4          SECOND EQU      *
0068 00A4 80A0 03FF            LDKL     A8,/3FF           FOR 30 SECONDS SEEK
0069 00A8 85A0 0130 R          LDKL     A13,CIOSST        SUBROUTINE ADDRESS
0070                    *      CONTINUOUS SEEK FROM 230 TO 235
0071
0072
0073 00AC 8120 015E R  SEEK    LDKL     A1,CSEEK          COMMAND BUFFER ADDRESS
0074 00B0 F697         CONT    CFR      A14,A13           SEEK FROM 230 TO 235
0075 00B2 1102                 ADK      A1,2              COMMAND BUFFER ADDRESS
0076 00B4 F697                 CFR      A14,A13           SEEK TO 235
0077 00B6 98A0 0001            SUKL     A8,1              TIME OVER?
0078 00BA 5910                 RB(P)    SEEK
0079 00BC 871C                 LDR      A7,A7             IS IT THE FIRST TIME?
0080 00BE 5120                 RF(P)    SK245
0081                    *      SEEK TO CYLINDER 4
0082 00C0 8120 0162 R          LDKL     A1,SEEK4          COMMAND BUFFER ADDRESS
0083 00C4 0304                 LDK      A3,4              DISPLAY CIL 4
0084 00C6 F697                 CFR      A14,A13           SEEK TO CYL 4
0085 00C8 0300                 LDK      A3,0              SOP DISPL
0086 00CA 8120 0172 R          LDKL     A1,SEEK0
0087 00CE F697                 CFR      A14,A13           PERFORM SEEK TO ZERO
0088                                                     AFTER MEASURING TO CONTINUE OPERATE SW2
0089                    *      SEEK TO CYLINDER 5
0090 00D0 0305                 LDK      A3,5              CYL 5
```

```
0091 00D2 8120 0164 R          LDKL    A1,SEEK5              COMMAND BUFFER ADDRESS
0092 00D6 F697                 CFR     A14,A13               SEEK TO CYL 5
0093 00D8 0300                 LDK     A3,0                  SOP DISPL
0094 00DA 8120 0172 R          LDKL    A1,SEEK0
0095 00DE F697                 CFR     A14,A13               PERFORM SEEK TO ZERO
0096                                                         AFTER MEASURING TO CONTINUE OPERATE SW2
0097                   *        SEEK TO CYLINDER 4 OR 245 FOR THE SEVERAL HEADS
0098
0099 00E0 033E         SK245   LDK     A3,/3E
0100 00E2 432E                 OTR     A3,0,/2E              DISPLAY HEAD SEL
0101 00E4 4A2E                 INR     A2,0,/2E              READ HEAD NUMBER
0102 00E6 5C04                 RB(NA)  *-2
0103 00E8 3AAC                 SRN     A2,A3                 FIND HEAD NUMBER
0104 00EA EB20 0004            CWK     A3,4                  MUST  IT GO TO CHECK
0105 00EE 512A                 RF(G)   CHECK
0106 00F0 E341 0167 R          SC      A3,HSEL+1             TO START WITH SELECTED HEAD
0107 00F4 B320 02C0            XRKL    A3,/2C0               FOR DISPLAY 2CX IN 2ND CHECK
0108 00F8 871C         NEXTH   LDR     A7,A7                 IS IT THE FIRST TIME
0109 00FA 5404                 RF(NZ)  NEXT                  NO
0110 00FC B320 0260            XRKL    A3,/260               FOR DISPLAY AX ADJUST HEAD
0111 0100 8120 0172 R  NEXT    LDKL    A1,SEEK0              COMMAND BUFFER ADDRESS
0112 0104 860C                 LDR     A6,A3                 SAVE SOP DISPLAY
0113 0106 0300                 LDK     A3,0                  FOR DISPLAY 0
0114 0108 F697                 CFR     A14,A13               SEEK TO 0
0115 010A 8120 0166 R          LDKL    A1,HSEL               SEL HEAD
0116 010E F697                 CFR     A14,A13               DO HEAD SEL
0117 0110 8318                 LDR     A3,A6                 LOAD SOP DISPLAY
0118 0112 8120 0170 R          LDKL    A1,SEK245             COMMAND BUFFER ADDRESS
0119 0116 F697                 CFR     A14,A13               SEEK 4 OR 245
0120                   *        AFTER ADJUSTING THE HEAD
0121
0122 0118 5F3A                 RB      SK245                 ASK NEXT HEAD
0123      011A         CHECK   EQU     *
0124 011A 1701                 ADK     A7,1                  SET FLAG 2 ND TIME
0125 011C EF20 0002            CWK     A7,2                  IS IT THE SECOND TIME?
0126 0120 589E                 RB(E)   START
0127 0122 84A0 A8F5            LDKL    A12,/A8F5             SEEK TO 245
0128 0126 84C1 0170 R          ST      A12,SEK245            CHANGE TO SEEK 245
0129 012A 8320 02FF            LDKL    A3,/2FF               DISPLAY SEEK
0130 012E 5F8C                 RB      SECOND
0131                   *                                    FOR CONTUNUOUS SEEK AGAIN
0132                   *        SUBROUTINE
0133
0134 0130 41D7         CIOSST  CIO     A1,1,/17              START OPERATION
0135 0132 432E                 OTR     A3,0,/2E              DISPLAY FUNCT ON SOP
0136 0134 4CD7                 SST     A4,/17                ASK FOR STATUS
0137 0136 5C04                 RB(NA)  *-2
0138 0138 2401                 ANK     A4,1                  CHECK IF NOT OPERABLE
0139 013A 5104                 RF(P)   CHRETRY               CHECK IF RETRY
0140 013C 0500                 LDK     A5,0                  CLEAR RETRY FLAG
0141 013E F03A                 RTN     A14
0142 0140 8514         CHRETRY LDR     A5,A5                 RETRY OR NOT
0143 0142 5C14                 RB(NZ)  CIOSST                DO RETRY
0144 0144 0501         NORETRY LDK     A5,1                  SET RETRY FLAG FOR NEXT COMMAND
0145 0146 02FF                 LDK     A2,/FF                TIME DELAY
0146 0148 1A01                 SUK     A2,1
0147 014A 5C04                 RB(NZ)  *-2
0148 014C F03A                 RTN     A14
0149                   *        STACK AREA
0150
0151 014E                      RES     7
0152 015C              EOS     RES     1
0153                   *        COMMAND BUFFERS
0154
0155 015E A8E6         CSEEK   DATA    /A8E6                 SEEK TO 230
0156 0160 A8EB                 DATA    /A8EB                 SEEK TO 235
0157
0158 0162 A804         SEEK4   DATA    /A804                 SEEK TO 4
0159
0160 0164 A805         SEEK5   DATA    /A805                 SEEK TO 5
0161
0162      0166         HSEL    EQU     *
0163 0166 0800                 DATA    /0800                 READ WITH HEAD X
0164 0168 0040 0040            DATA    /0040,/0040
0165 016C 0000 0000    BUFL    DATA    0,0
0166 0170 A8F5         SEK245  DATA    /A8F5                 SEEK TO CYL 245
0167
0168 0172 E800         SEEK0   DATA    /E800                 RETURN TO CYL 0
0169
0170                           END     START
```

SYMBOL TABLE

BUFL	016C	R	CHECK	011A	R	CHRETR	0140	R	CIOSST	0130	R
CONT	00B0	R	CSEEK	015E	R	EOS	015C	R	HSEL	0166	R
NEXT	0100	R	NEXTH	00F8	R	NORETR	0144	R	SECOND	00A4	R
SEEK	00AC	R	SEEK0	0172	R	SEEK4	0162	R	SEEK5	0164	R
SEK245	0170	R	SK245	00E0	R	START	0084	R			

```
          ASS.ERR.    0000
:EOF
PROG ELAPSED TIME:  00H-00M-00S-000MS-
```

```
00000                           IDENT    HDUSER
00001                  *DATE 820727 FOR PTS HDU  TO CHECK SERVO HEADS
00002
00003                  *AFTER IPL ALL SOP INDICATORS ON
00004                  *DEPRESS A SOP SWITCH
00005                  *PROGRAM IS STARTED
00006                  *SEEK ON VOLUME ZERO TO CYL. ZERO
00007                  *READ ON VOLUME ONE (VOLUME CHANGE IS MADE)
00008                  *SEEK ON VOLUME ONE TO NEXT CYL
00009                  *READ ON VOLUME ZERO (VOLUME CHANGE IS MADE)
00010                  *AND SO ON TILL CYL /336 IS REACHED.  THEN START AGAIN
00011                  *CYLINDER NUMBERS ARE DISPLAYED ON SOP
00012                  *IF DRIVE NOT OPERABLE OR SEEKERROR (SER,NOP)  STATUS TO SOP
00013                  *PROGRAM IS STOPPED OR RESTARTED BY PRESSING A SOP SWITCH
00014  0000                             RES      /40
00015                            EJECT
00016  0080  FFFF                       DATA     /FFFF,0
       0082  0000
00017  0084  20BF        START          INH
00018  0086  41EE                       CIO      A1,1,/2E              START SOP
00019  0088  8320                       LDKL     A3,/7FF
       008A  07FF
00020  008C  432E                       OTR      A3,0,/2E              /7FF ON SOP
00021  008E  85A0                       LDKL     A13,CIOSST            START ADDRESS SUBROUTINE
       0090  00CE  R
00022  0092  0610                       LDK      A6,16                 VOLUME 0/1
00023  0094  80A0                       LDKL     A8,/AB36              SEEK TO LAST CYL (822)
       0096  AB36
00024  0098  4A2E        RESTART        INR      A2,0,/2E
00025  009A  5C04                       RB(NA)   *-2                   WAIT TILL SOP SWITCH IS PRESSED
00026                          *
00027                          *    RETURN TO VOLUME 0, CYLINDER 0
00028  009C  8120                       LDKL     A1,SEEKZ              RETURN TO CYL/VOL ZERO
       009E  0102  R
00029  00A0  86A0                       LDKL     A14,EOS               STACK POINTER
       00A2  00F6  R
00030  00A4  F697                       CFR      A14,A13               EXECUTE RTZ SEEK
00031                          *
00032                          *    SEEK OPERATION
00033  00A6  8420        AGAIN          LDKL     A4,/A800              SEEK TO CYLINDER 0
       00A8  A800
00034  00AA  8441                       ST       A4,SEEK
       00AC  0104  R
00035  00AE  8120        NEXT           LDKL     A1,SEEK
       00B0  0104  R
00036  00B2  F697                       CFR      A14,A13               EXECUTE SEEK
00037                          *
00038                          *    VOLUME CHANGE
00039  00B4  8120                       LDKL     A1,READ
       00B6  00F8  R
00040  00B8  8641                       XRS      A6,READ               READ ON OTHER VOLUME
       00BA  00F8  R
00041  00BC  F697                       CFR      A14,A13               EXECUTE READ (VOLUME CHANGE)
00042  00BE  E8C0                       CW       A8,SEEK               LAST CYL?
       00C0  0104  R
00043  00C2  581E                       RB(E)    AGAIN                 RESTART OF PROGRAM
00044  00C4  9041                       IM       SEEK                  NEXT CYL
       00C6  0104  R
00045  00C8  8340                       LD       A3,SEEK               NEW CYL TO DISPLAY ON SOP
       00CA  0104  R
00046  00CC  5F20                       RB       NEXT                  SEEK ON OTHER VOLUME TO NEXT CYL
00047                          *
00048                          *    SUBROUTINE CIO, OTR (SOP), SST
00049  00CE  41D7        CIOSST         CIO      A1,1,/17              EXECUTE SEEK/READ OPERATION
00050  00D0  432E                       OTR      A3,0,/2E              DISPLAY CYL ON SOP
00051  00D2  4DD7                       SST      A5,/17
00052  00D4  5C04                       RB(NA)   *-2
00053  00D6  A520                       ANKL     A5,/201               SER, NOP
       00D8  0201
00054  00DA  5106                       RF(P)    HALT
00055  00DC  4A2E                       INR      A2,0,/2E              STOP WHEN A SOP SW IS DEPRESSED
00056  00DE  5848                       RB(A)    RESTART
00057  00E0  F03A                       RTN      A14
00058                          *
00059                          *    DRIVE ERROR
00060  00E2  452E        HALT           OTR      A5,0,/2E              STATUS BITS 6, 15 TO SOP
00061  00E4  5F4E                       RB       RESTART
00062  00E6                             RES      8
00063  00F6              EOS            RES      1
00064                          *
00065                          *    DRIVE OPERATIONS
00066  00F8  0800        READ           DATA     /0800
00067  00FA  0040                       DATA     /0040,/0040
       00FC  0040
00068  00FE  0000                       DATA     /0000,BUF
       0100  0106  R
00069  0102  E800        SEEKZ          DATA     /E800
00070  0104  A800        SEEK           DATA     /A800
00071  0106              BUF            RES      1
00072                                    END      START
```

25 CHANNEL UNIT LOCAL WORKSTATIONS

LIST OF ILLUSTRATIONS

25.1 CHLW-IDENTIFICATIONS

Type-number:	PTS-6895
Test-Program:	TERTST4.1 and higher releases
Channel:	Hardware Channel (DMA is implemented in channel unit)
Devices:	Those devices with a Local Workstation interface. viz.
also Secondary-,	Modular Device Adaptor, MDA 6411
Work-stations)	Terminal Printer, TP 6371
	Visual Display Unit, VDU 6347, VDU 6381
	General Printer, GP 6374
	Compact Financial Terminal, CFT 6280

Power-consumption :	+5 Volt	: 2.9 A +/- 0.1A
	-5 Volt	: 10 mA +/- 1 mA (made from -18 Volt)
	+16 Volt	: 55 mA +/- 3 mA (made from +18 VOlt)

Transmission information:

Line configuration:	Multidrop, 1 line
Number of workstations:	Max. 32, typical 6-8
Cable:	3 twinned pairs, max. length 750 metres
Type of transmission:	A-synchronous, self clocked serial data, NRZI, full duplex
Line procedure:	HDLC/X27, with polling
Character format:	8 bits, without parity
Max. Packet length	259 bytes (3 bytes in Packet Header plus 256 characters)
Speed of transmission:	96k bits per second

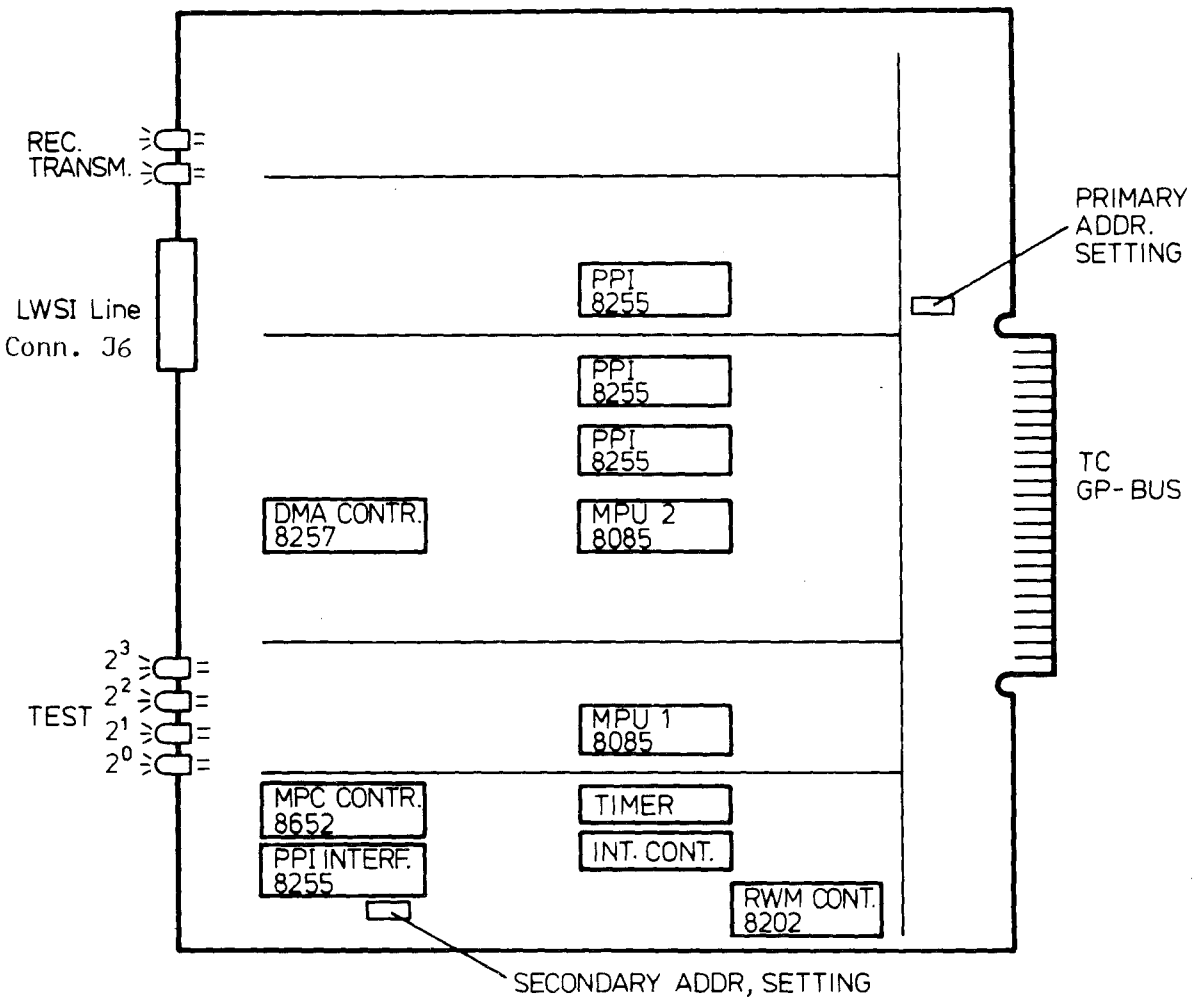


Figure 25.1 LAYOUT OF CHLW

STRAP-SETTING CONTROL UNIT ADDRESS

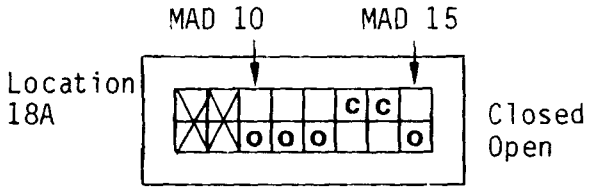
CHLW used as Primary: Prim. Addr. switches: CHLW1 /06
CHLW2 /07
CHLW3 /26
CHLW4 /27
Second. Addr. switches: Don't care

CHLW used as Secondary: Prim. Addr. switches: Don't care
Second. Addr. switches: 0 - 31, (switches at '0' = WS NR. 32) depending on Software

INTERRUPT LEVEL:
No straps available; is software set.

The Interrupt level can be: (decimal)

CHWL1: 26
CHWL2: 27
CHWL3: 24
CHWL4: 25

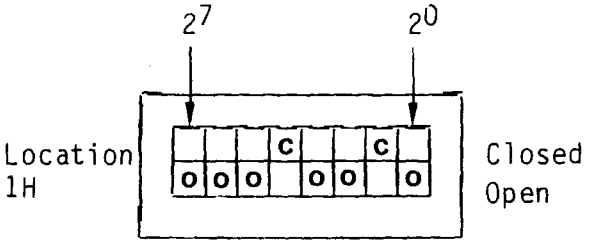


Primary Address: 06 CHLW1
07 CHLW2

Decimal Interrupt Level: 26 CHLW1
(Software Set) 27 CHLW2

MAD	Closed	Open	
10		X	2^5
11		X	2^4
12		X	2^3
13	X		2^2
14	X		2^1
15		X	2^0

Example:
Primary
Address 06

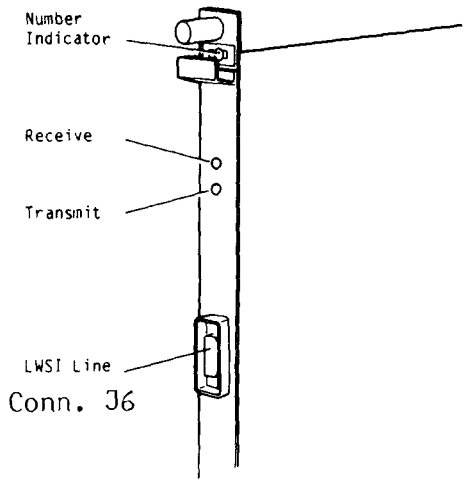


Secondary Address: 00 - 1F

	Closed	Open
2^7		X
2^6		X
2^5		X
2^4	X	
2^3		X
2^2		X
2^1	X	
2^0		X

Example:
Work station
address 18 (/12)

Figure 25.2 EXAMPLES OF PRIMARY & SECONDARY ADDRESS SETTING



Number Indicator:
CHLW1: slide to show 1
CHLW2: slide to show 2

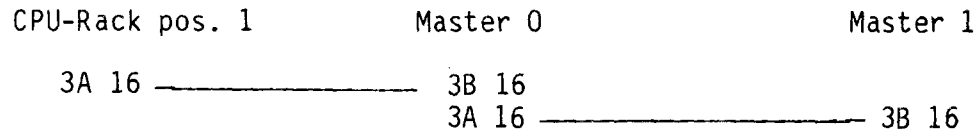
Figure 25.3 NUMBER INDICATOR

As a Direct Memory Access function is implemented in CHLW, the control unit is a master during transfers of information between the TC's main memory and the memory of the CHLW.
For this reason this control unit must be connected in the Master priority chain, the OKO-OKI line.

The priority level must be according the following table:

Priority level	Master	Remark
0	DMA (CURD 80 MDisc.)	Highest priority
1	IOP 1 (Dev. Addr. 08-0F)	
2	CHLW	
3	CHRW	
4	CPU	Not wired.

The bus priority line OKO/OKI originates from the Bus Controller, located on the CPU board, and the line is wired in the following way:



In case a master with higher priority is not used the others are advanced one level.

CAUTION

If a CHLW is removed from the rack the OKO/OKI on that rack position must be linked in order not to break the line for masters with lower priority.

25.3 INTERFACE CONNECTIONS

Connector J6:

Signal Name	Pin No.	Type	Remark
Data In	2	Input	To CHLW from WSs
Data In N	4	Input	" " " "
Data Out	3	Output	From CHLW to WSs
Data Out N	5	Output	" " " "
Signal Ground	7		

Figure 25.4 RELATION PIN NUMBER /SIGNAL

The input-line wires are clamped to signal ground by two resistors, each 560 Ohm at the CHLW.
Signal levels are according to CCITT X27 specification.

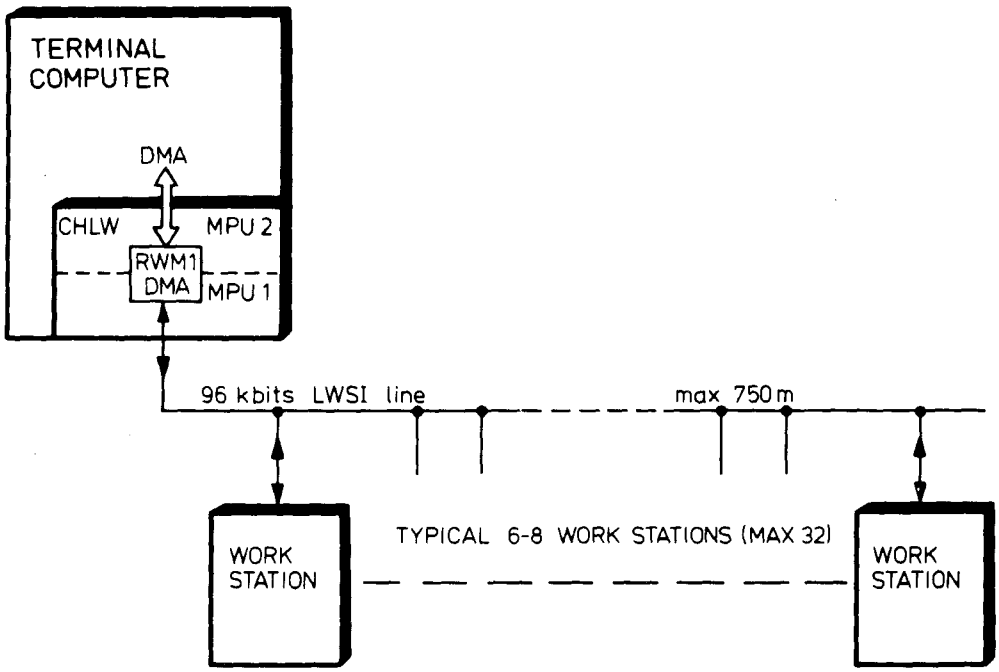


Figure 25.5 LWSI CONFIGURATION

For cabling See Chapter 2 "Installation"

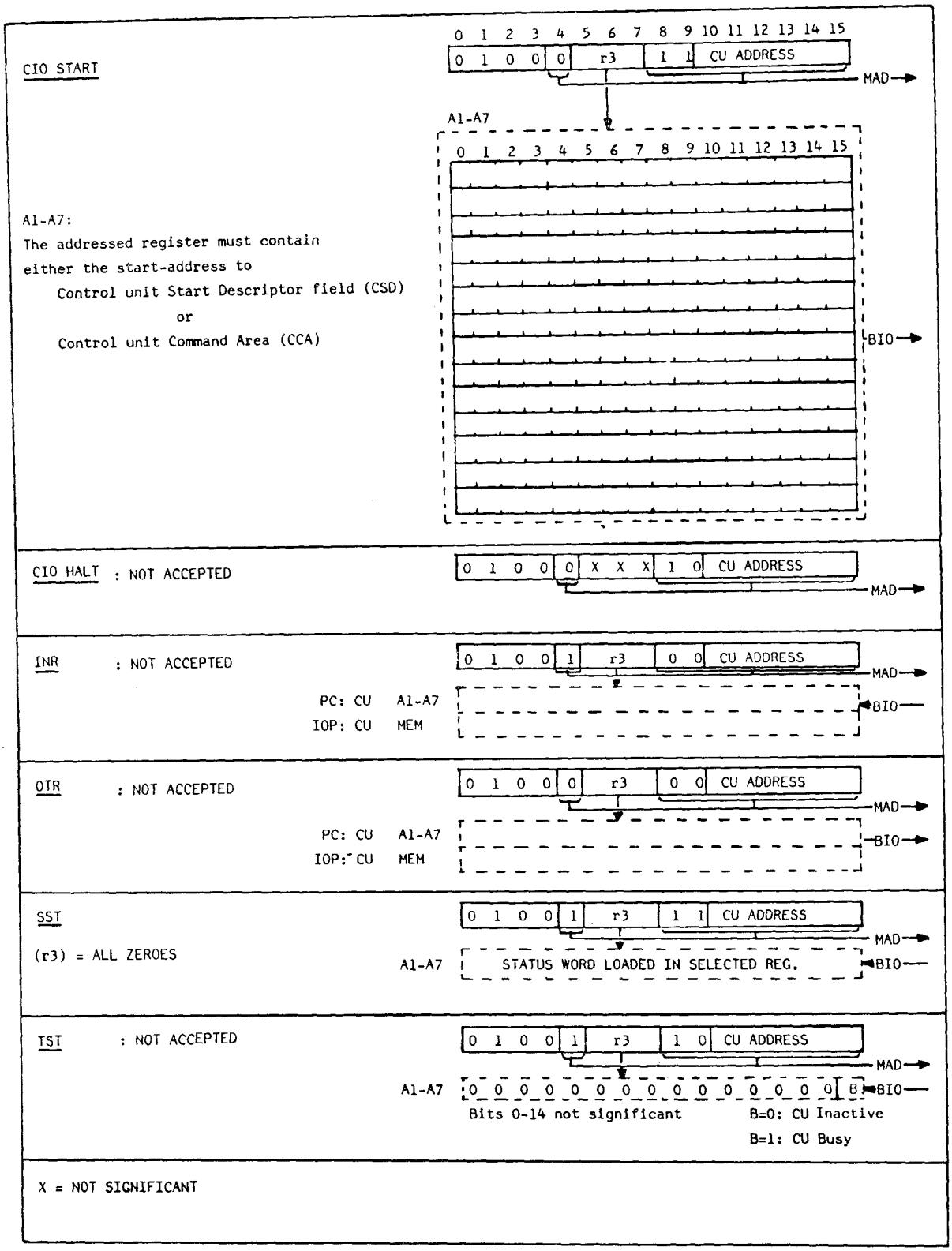


Figure 25.6 INSTRUCTION-/COMMAND-WORD FORMATS

COMMAND/RESPONSE INTERFACE BLOCKS

INITIALIZATION OF CHLW:

After power-on the CHLW is in Reset state and has to be initialised. During initialisation three control blocks are transferred from main memory to CHLW memory, viz. Control unit Start Descriptor (CSD), Control unit Interface Descriptor (CID) and Control unit Command Area (CCA).
Before the CCA is transferred to CHLW the control unit tests itself. (See diagnostic tests).

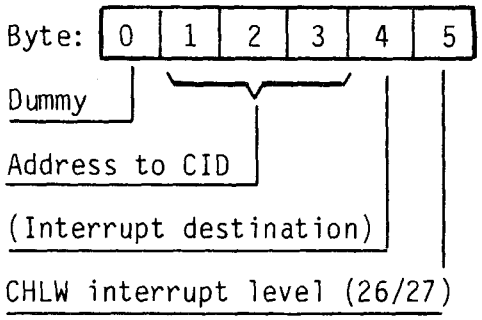


Figure 25.7 LAYOUT OF CSD

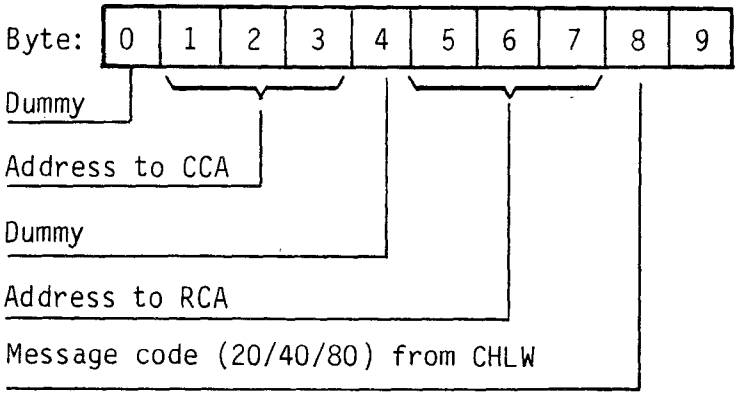
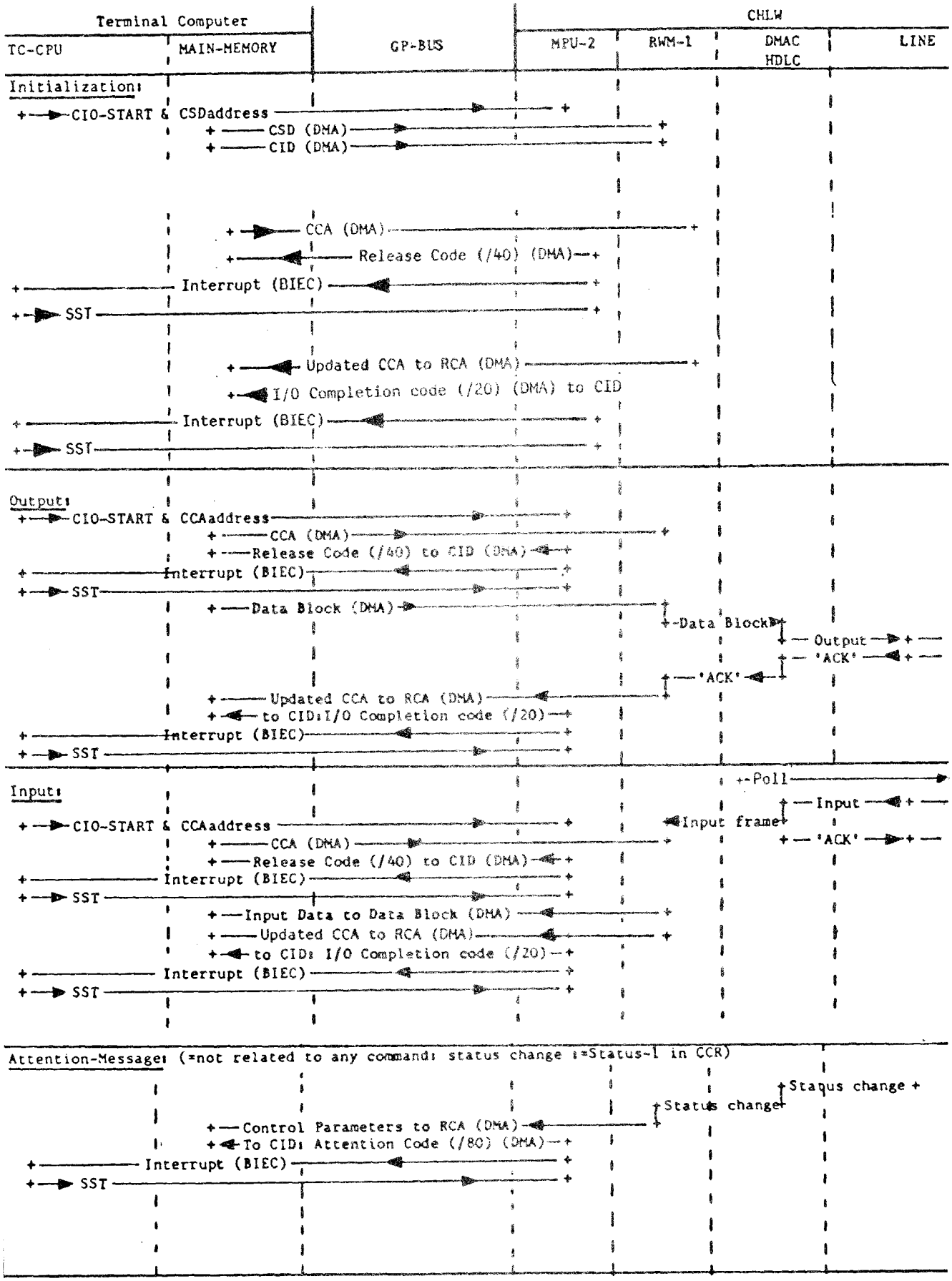


Figure 25.8 LAY-OUT OF CID

After the CHLW has completed a command it transfers a message code to byte 8 of CID in main memory, an updated CCA Response Communication Area (RCA) in main memory, and interrupts the CPU at level as stated in byte 5 of CSD. (Software set Interrupt level of CHLW).
The start address of RCA is stated in CID.

For transfer of the blocks see figure 26.9 Data Flow Initialisation, Output, Input, Attention Message.



Following messages can be given:
If the WS is disconnected: No Connection
If the CHLW has reset the Link: Link Reset
If the CHLW has re-established the data link: Communication Re-established
The information is put in Status-1 of RCA.

Figure 25.9 DATA-FLOW INITIALISATION, OUTPUT, INPUT, ATTENTION MESSAGE

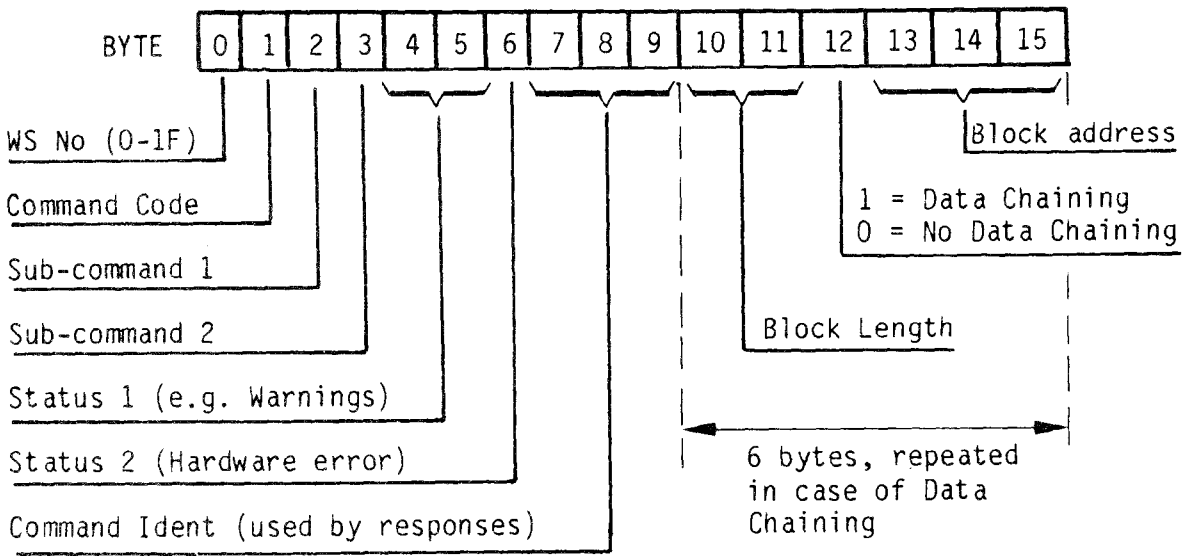


Figure 25.10 LAYOUT OF CCA/RCA

Three different message codes can be received from CHLW:

- Release code: /40
- I/O Completion Code: /20
- Attention Code : /80

CHLW sends the Release Code if CSD and CID or if CCA is transferred to the memory of the CHLW. Customer software now can fill these blocks with new information.

CHLW sends I/O Completion Code after a command is completely executed. The Attention Code is send by CHLW if there has been a change in the hardware somewhere in the network or at the CHLW. This code has no relation to any command.

Directly after transfer of one of these codes the CHLW interrupts the CPU via the BIEC lines. These interrupts must be reset by means of an SST instruction.

All transfers between TC's main memory and the CHLW are controlled by the Direct Memory Access part of the CHLW. (Hardware Channel). As the CHLW is acting as a Master, the control unit must be taken into the Master priority chain by means of OKO-OKI signal. The priority order is set by the Customer's application.

COMMAND CODES FOR CHLW

The CHLW recognizes the following command codes set in byte 1 of CCA. There are three types of command codes, with some commands additional information has to be sent in special formatted information blocks.

Command Code Hex	Command	Command Type	Remark
20	General Read	Input	From any WS
21	Specific Read	"	From addressed WS
40	Standard Write	Output	To addressed WS
41	Fast Write	"	To addressed WS with high priority
80	Test CU	Supervisory	Starts CHLW internal tests
81	Terminate (Not used)	"	Software Reset of CHLW
82	Close Line	"	Resets line parameters
83	Get DLS Statistics	"	Statistics for an addressed WS are transferred to TC.
84	Get Line Statistics	"	Statistics for the line counters are fetched to TC.
85	Open Data Link	"	Establishes a connection to a specified WS.
86	Open Line	"	Defines the type of line and sets the line parameters.
87	Read Local Memory	"	Read from RWM1 on CHLW to specified memory area in TC.
88	Cancel	"	Cancels a previously sent Read command.
89	Close Data Link		Closes the data link for a specific WS.

Figure 25.11 COMMAND CODES FOR CHLW

WS- Work Station

25.5 DIAGNOSTIC TESTS

In the software of the CHLW are implemented 4 diagnostic test types:

- Start-up test
- In-line test
- On-line test
- Off-line test (=Start-up test)

The outcome of the test is displayed in hex. format on four leds at the front of the CHLW.
Line-activity is indicated by 2 yellow leds: one for transmit data and one for received data.

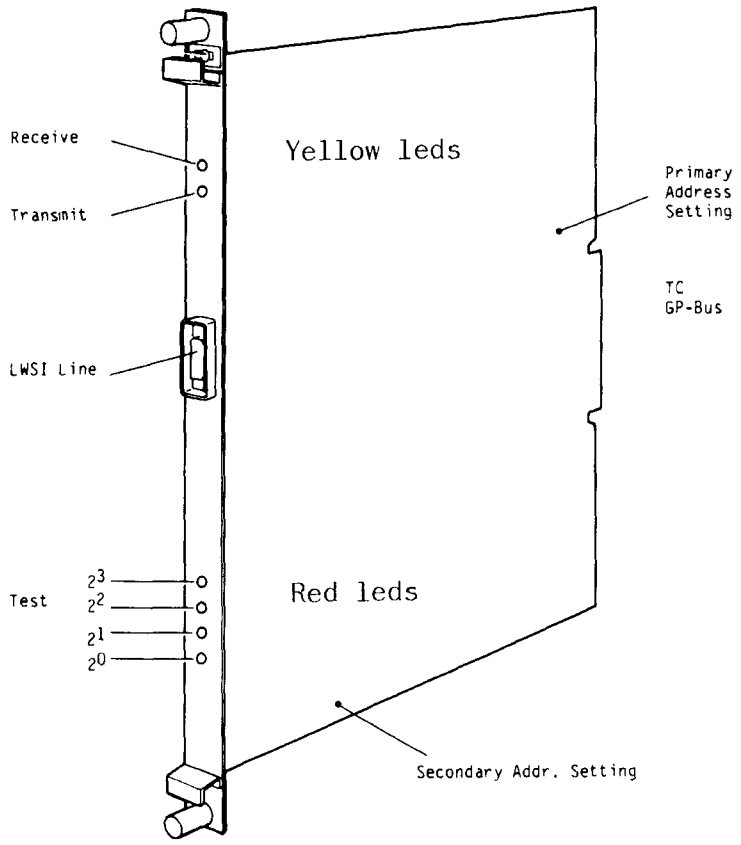


Figure 25.12 POSITION OF LEDs

START-UP TEST AND OFF-LINE TEST

The Start-up test and the Off-line test are exactly the same but initiated in different ways. Start-up test is started by "power-up".
The Off-line test is started when the IPL button or the Master-Clear button are pressed. The test-codes are shown in the figure below.

In case of an error the leds for the corresponding code are flashing.

If led(s) are flashing the CHLW has put itself into NOT OPERABLE mode and will not respond to any command from the host program.
The test can be started again by means of power-off/on, IPL- or MCL-button.

The following internal logic are tested during the test:

- MPU1
- ROM1 (all data is LRC checked)
- RWM1 (all locations are written into, read and reset)
- MPU2
- ROM2 (all data is LRC checked)
- RWM2 (all locations are written into, read and reset)

TEST CODE Hex	2^3 2^2 2^1 2^0	Meaning
0	0 0 0 0	No error, and "TEST CU"-command received
1	0 0 0 ⊛	ROM 1 error, MPU 1
2	0 0 ⊛ 0	ROM 2 error, MPU 2
3	0 0 ⊛ ⊛	Not used
4	0 ⊛ 0 0	RWM 1 error, bit 0/1, MPU 1
5	0 ⊛ 0 ⊛	RWM 1 error, bit 2/3, MPU 1
6	0 ⊛ ⊛ 0	RWM 1 error, bit 4/5, MPU 1
7	0 ⊛ ⊛ ⊛	RWM 1 error, bit 6/7, MPU 1
8	⊛ 0 0 0	RWM 2 error, MPU 2
9	----	Not used
A	⊛ 0 ⊛ 0	HDLC error/Data loop error
B	----	Not used
C	----	Not used
D	----	Not used
E	⊛ ⊛ ⊛ 0	Test OK, but no "Test CU" yet, not flashing.
F	⊛ ⊛ ⊛ ⊛	Hardware reset received, not flashing.

Figure 25.13 TEST CODES START-UP/OFF-LINE TEST

To switch the CHLW from RESET to NORMAL OPERATION mode from the host program the TEST CU command must be given.
This command is only accepted if no error was detected in the Start-up test. The TEST CU command starts the Start-up test all over again.
It takes about 10 seconds between a reset and accepting the TEST-CU command.

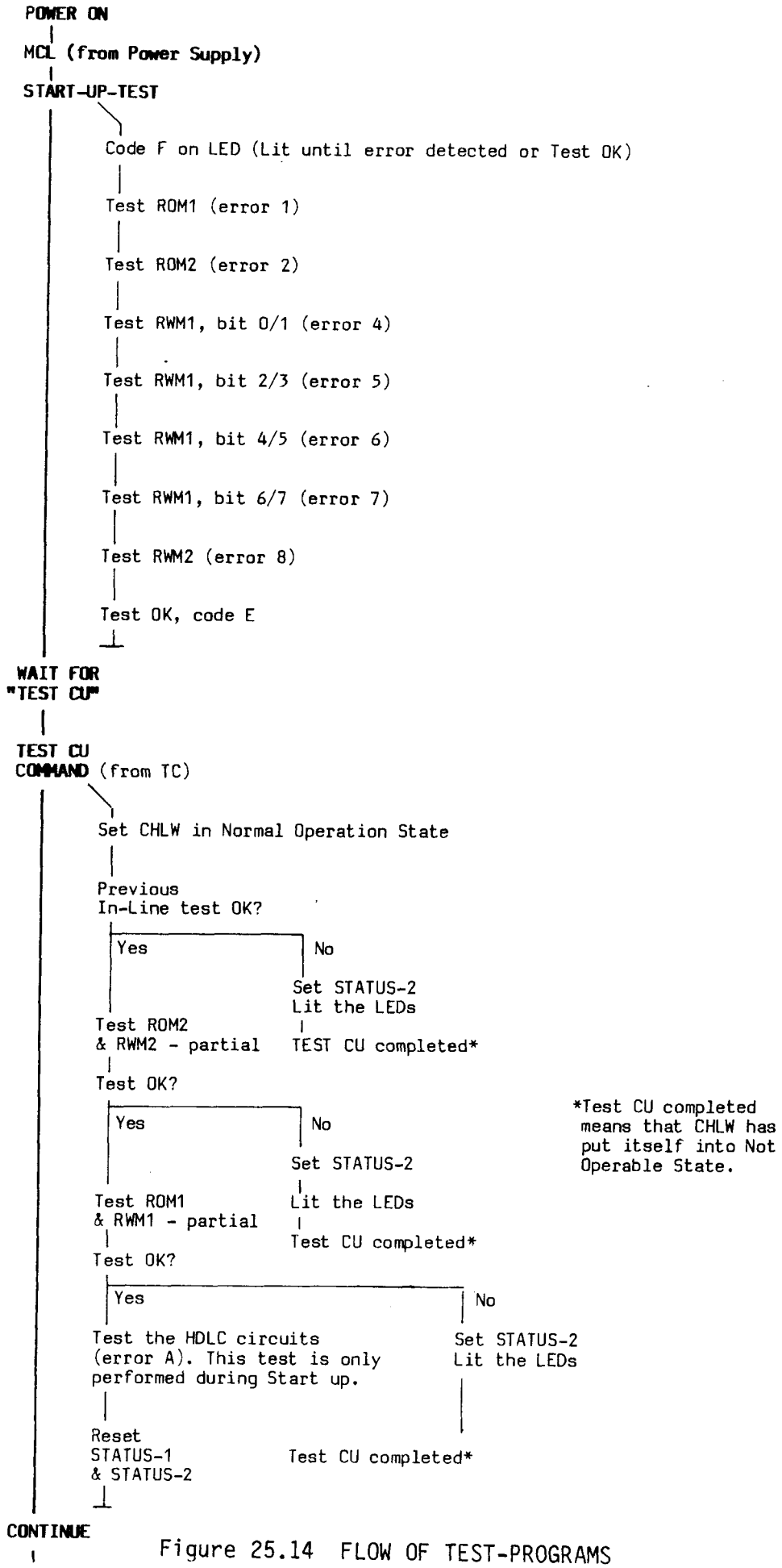


Figure 25.14 FLOW OF TEST-PROGRAMS

IN-LINE TEST

The In-line test is activated several times by CHLW during run-time without affecting the user's application.
The codes B and C in the figure below indicate that an error has been detected. The CHLW, however, will continue its normal execution in order to allow the host program to detect the error by means of a TEST-CU command

TEST CODE Hex	2^3 2^2 2^1 2^0	MEANING
B	Ø 0 Ø Ø	MPU1 error, not flashing
C	Ø Ø 0 0	MPU2 error, not flashing
D	Ø Ø 0 Ø	Not used

Figure 25.15 ERROR CODES IN-LINE TEST

ON LINE TEST

The On-line test if activated by means of a TEST CU command during the time the CHLW is in NORMAL OPERATION mode.

The following actions are taken:

- If the In-line test previous has detected an error the TEST CU command is immediately executed.
- A ROM2 and a simple RWM2 test is performed. If an error is detected the appropriate leds, as shown in the figure below, are lit.
- A ROM1 and a simple RWM1 test is performed. If an error is detected the appropriate leds, as shown in the figure below, are lit.
- If no error is detected the TEST CU command is completed with the fields STATUS-1 and STATUS-2 in the RCA set to zero.

In case of an error the Test Code is duplicated in the 4 least significant bits of the STATUS-2 field after the TEST CU command has been completed.

TEST CODE **Hex**	2^3 2^2 2^1 2^0	**Meaning**
1	0 0 0 Ø	ROM 1 error, MPU 1
2	0 0 Ø 0	ROM 2 error, MPU 2
3	0 0 Ø Ø	Not used
4	0 Ø 0 0	RWM 1, bit 0/1, MPU 1
5	0 Ø 0 Ø	RWM 1, " 2/3, MPU 1
6	0 Ø Ø 0	RWM 1, " 4/5, MPU 1
7	0 Ø Ø Ø	RWM 1, " 6/7, MPU 1
8	Ø 0 0 0	No error, and "TEST CU"-command received

Figure 25.16 TEST CODES ON-LINE TEST

FAULT FINDING AIDS

TEST- AND TRANSMIT/RECEIVE LEDS:

The fault symptoms that can be discovered during runtime are shown in the flow-chart below together with advised remedy.

Use the Test LEDs and the Transmit and Receive LEDs on the CHLW board to trace the faults. Besides, watch the operation of the devices during the OFF-LINE TEST when the Test-switch is set ON at respective main module of the work stations.

TEST PROGRAMS

To test the network and connected terminals the test-program TERTST4.1 and higher releases may be used.

See description of TERTST for details.

LWSI-DATASCOPE

The LWSI-Datascope is a VDU 6347 which is used for looking at data sent on the LWSI line in a running system. To make the VDU 6347 to a datascope, the program held in three PROMs 2716 and one 2732 must be exchanged and a keyboard must be connected to the display. The keyboard is to be used for communication between the operator and the datascope.

The VDU can be connected to any drop point and by using a standard VDU drop cable it is possible to look at data sent from the terminal computer to one or more secondary work stations.

Using a specially prepared VDU drop cable, where the receiving line wires are changed, it is possible to look at data sent from the secondary stations, e.g. MDA 6411, to the terminal computer.

The use of the LWSI-Datascope is described in a separate manual - **LWSI-Datascope, Operator's Guide.**

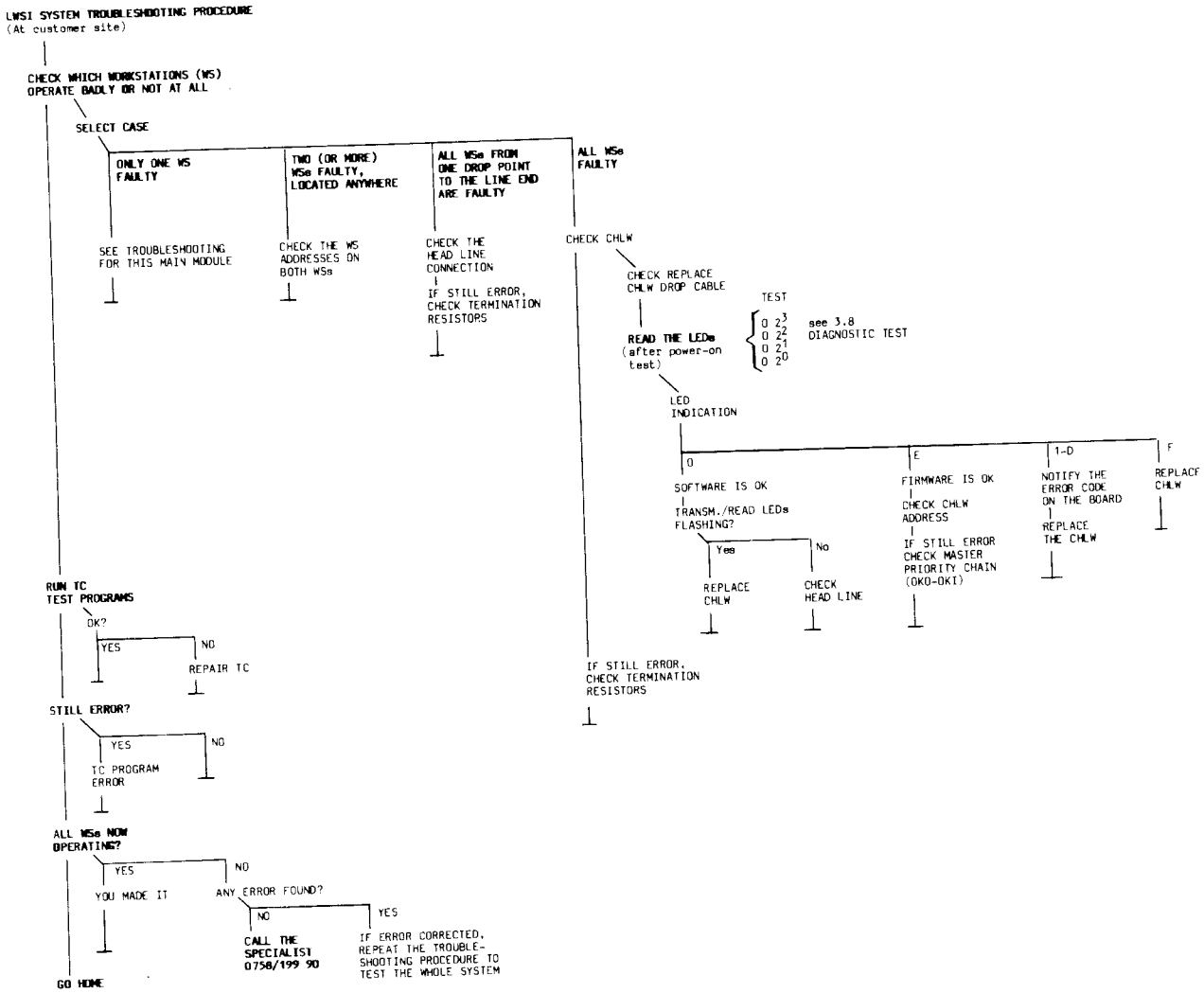


Figure 25.17 TROUBLE-SHOOTING PROCEDURE

26 CHANNEL UNIT REMOTE WORKSTATIONS

LIST OF ILLUSTRATIONS

26.1 CHRW IDENTIFICATIONS

Type-number:	PTS-6896
Test-Program:	TERTST4.2 and higher releases
Channel:	Hardware Channel (DMA is implemented in channel unit)
Devices:	Those devices with a Remote Workstation interface, viz.
(also Secondary-,	Work Station Controller, PTS-6911/12
Work-stations,	Terminal Printer, TP 6371
Main modules)	Modular Device Adaptor, MDA 6411

Power-Consumption	+5 Volt	: 3.8A +/-380mA
	-18 Volt	: 50 mA +/- 5mA
	+18 Volt	: 130 mA +/- 13mA

Transmission Information:

Line Configuration:	Multidrop, 4 lines
Number of Workstations:	8 on each line, typical 2-3 per line
Line:	2 or 4 wire leased lines
Type of transmission:	A-synchronous, modem-clocked serial data, half or full duplex
Line procedure:	HDLC/V24-V28, with polling
Max. Packet length:	259 bytes (3 bytes in Packet Header plus 256 characters
Character format:	8 bits, without parity
Speed of transmission	Up to 19.200 bits per second,typical 4800 bps.

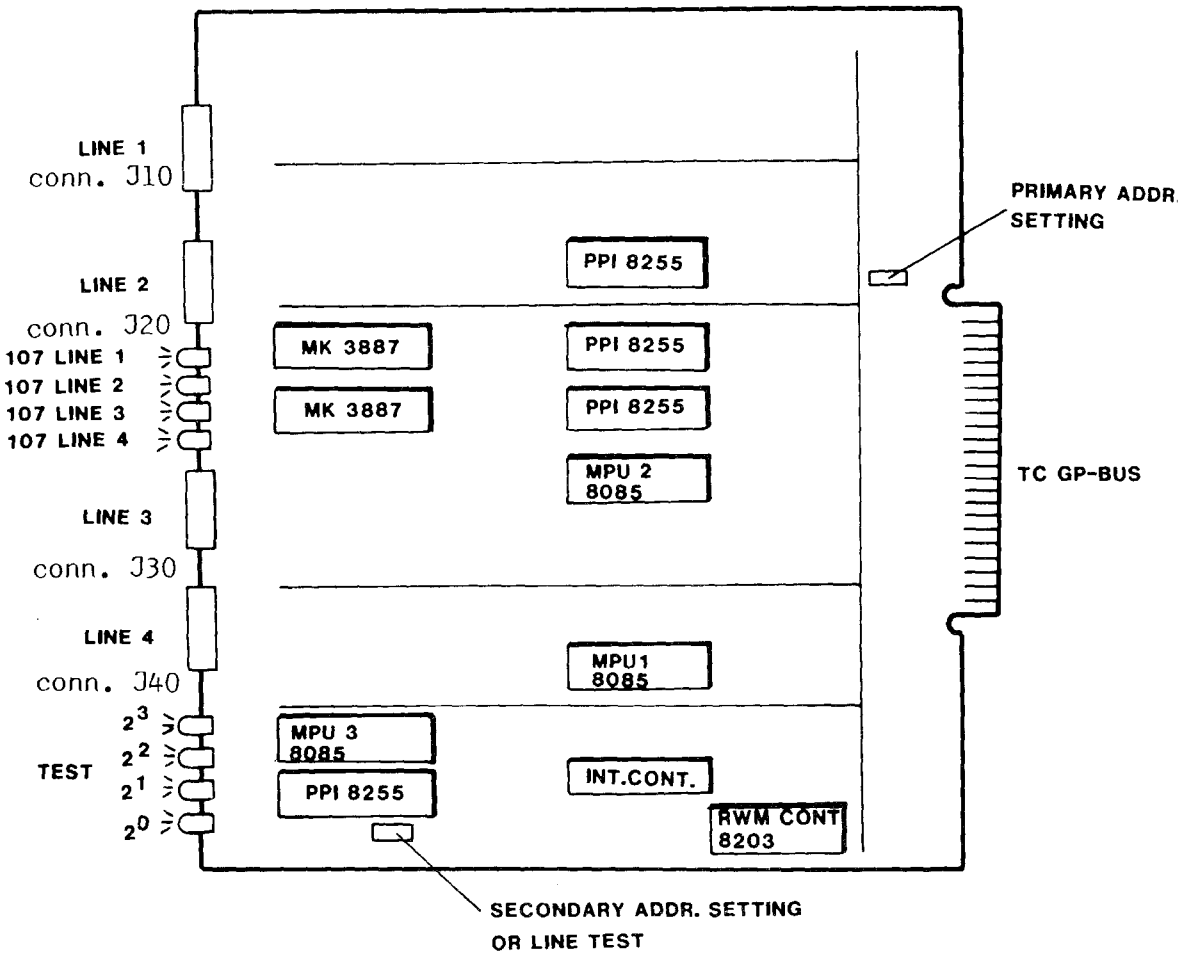


Figure 26.1 LAYOUT OF CHRW

STRAP-SETTING CONTROL UNIT ADDRESS

CHRW used as Primary:	Prim. Addr. switches:	CHRW1 /3A
		CHRW2 /3B
		CHRW3 /2A
		CHRW4 /2B
	Second Addr. switches:	Don't care
CHRW used as Secondary:	Prim. Addr. switches:	Don't care
	Second Addr. switches:	0-32, depending on software

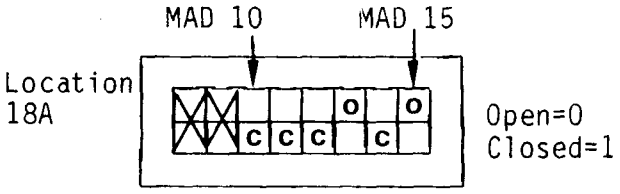
The Secondary address set on the switches may be overruled by a Secondary address setting from the software.
The Secondary address is only applicable for Line 1 (channel 0)

INTERRUPT LEVEL:

No straps are available for setting the interrupt level.
This level is software set.

The Interrupt level can be: (decimal)

CHRW1: 18
CHRW2: 19
CHRW3: 20
CHRW4: 21

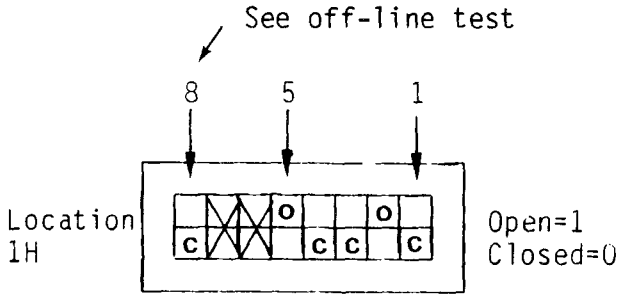


Primary Address: 3A CHRW1
3B CHRW2
2A CHRW3
2B CHRW4

Decimal Interrupt Level: 18 CHRW1
(Software Set) 19 CHRW2
20 CHRW3
21 CHRW4

MAD	Closed	Open	
10	X		2^5
11	X		2^4
12	X		2^3
13		X	2^2
14	X		2^1
15		X	2^0

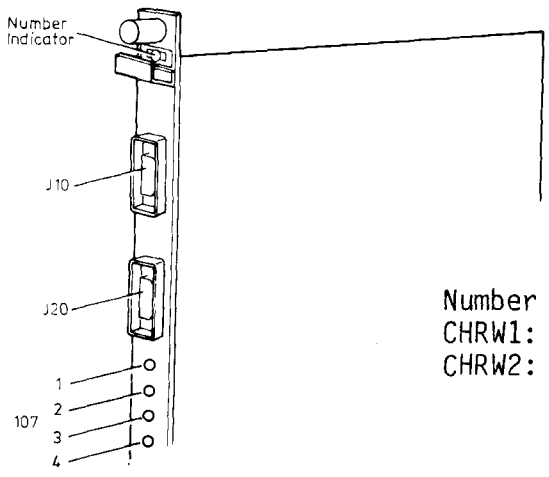
Example:
Primary
Address 3A



Secondary Address: 00 - 1F

	Closed	Open	
8	X		Off Line TEST
7			
6			
5		X	2^4
4	X		2^3 Example:
3	X		2^2 Work
2		X	2^1 station
1	X		2^0 address/12

Figure 26.2 EXAMPLES OF PRIMARY & SECONDARY ADDRESS SETTING



Number Indicator:
CHRW1: slide to show 1
CHRW2: slide to show 2

Figure 26.3 NUMBER INDICATOR

OKO-OKI SIGNALS

As a Direct Memory (DMA) function is implemented in CHRW, the control unit is a master during transfers of information between the TC's main memory and the memory of the CHRW.
For this reason this control unit must be connected in the Master priority chains, the OKO-OKI line-.

The priority level must be according the following table:

Priority level	Master	Remark
0	DMA (CUHD 80 Mb Disc.)	Highest priority
1	IOP 1 (Dev. Addr. 08-0F)	
2	CHRW	
3	CHRW	
4	CPU	Not wired

The bus priority line OKO/OKI originates from the Bus Controller, located on the board, and the line is wired in the following way:

CPU-Rack pos. 1 Master 0 Master 1

3A 16 ——————— 3B 16
3A 16 ——————— 3B 16

In case a master with higher priority is not used the others are advanced one level.

CAUTION

If a CHRW is removed from the rack the OKO/OKI on that rack position must be linked in order not to break the line for masters with lower priority.

26.3 INTERFACE CONNECTIONS

Connectors J10, J20, J30 & J40

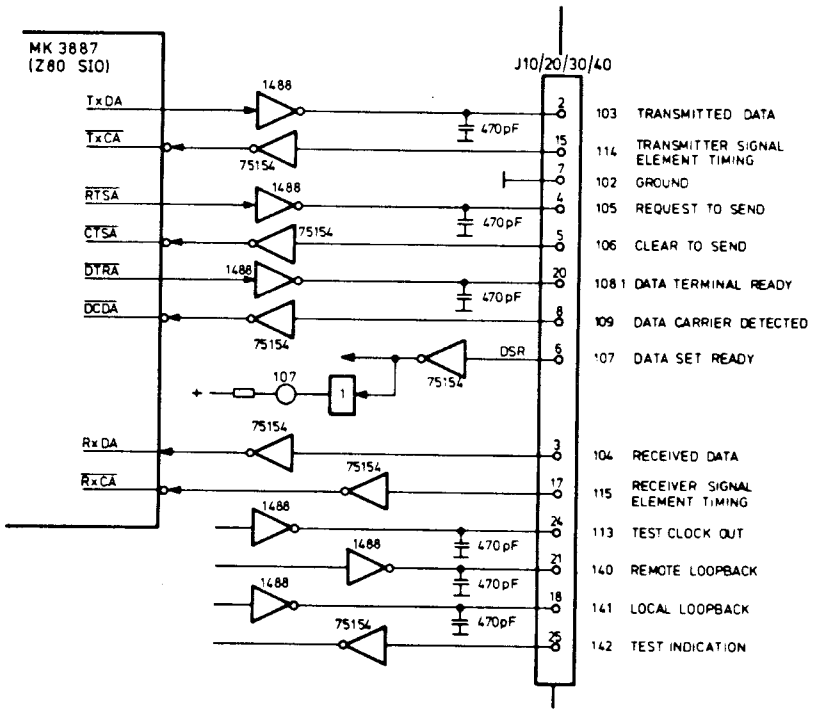


Figure 26.4 LINE INTERFACE

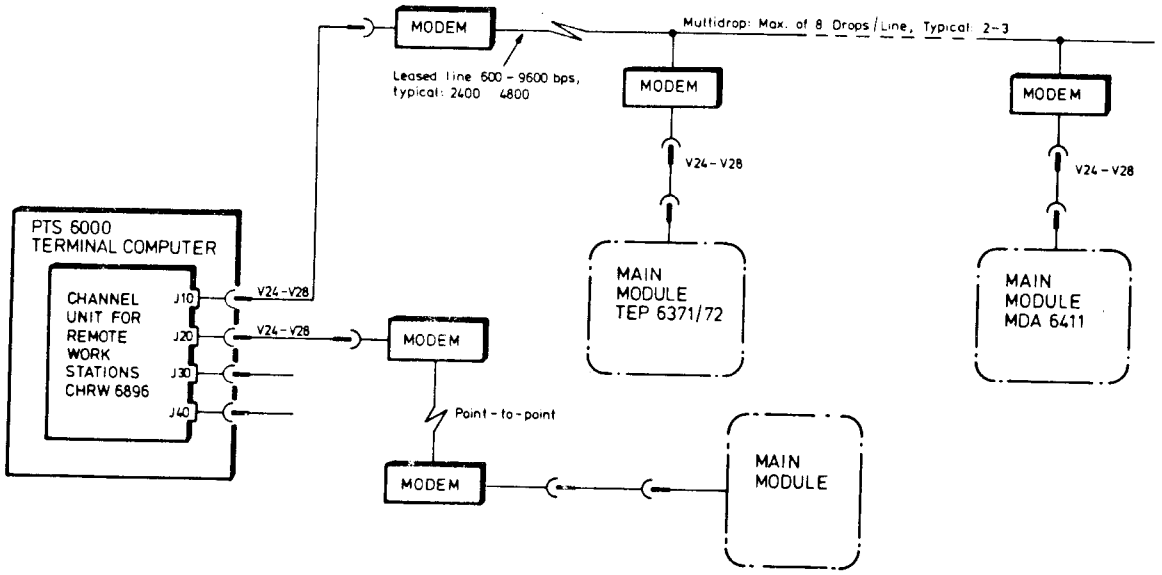


Figure 26.5 RWSI CONFIGURATION

LINE TRANSFER SPEED

The total sum of bits per second over the four lines may not exceed 30.000 bps. As the transfer speed may be different for the four channels the lines should be connected in the order shown below.

Example: If four lines with respective transfer speeds of 19.200 bps, 4.800 bps, 1.200 bps and 600 bps are to be connected, it should be done as follows:

Transfer speed:	Connect line to:
19.200 bps	Channel 2
4.800 bps	Channel 3
1.200 bps	Channel 0
600 bps	Channel 1

Total: 25.800 bps

The channels are scanned by the CHRW in a priority order.
Channel 2 has the highest priority and next is channel 3.
These channels should be used for high speed data transfer.
The lower speed lines should be connected to channel 1 or channel 0 which are treated with a low priority.

For cabling see chapter 2 " Installation"

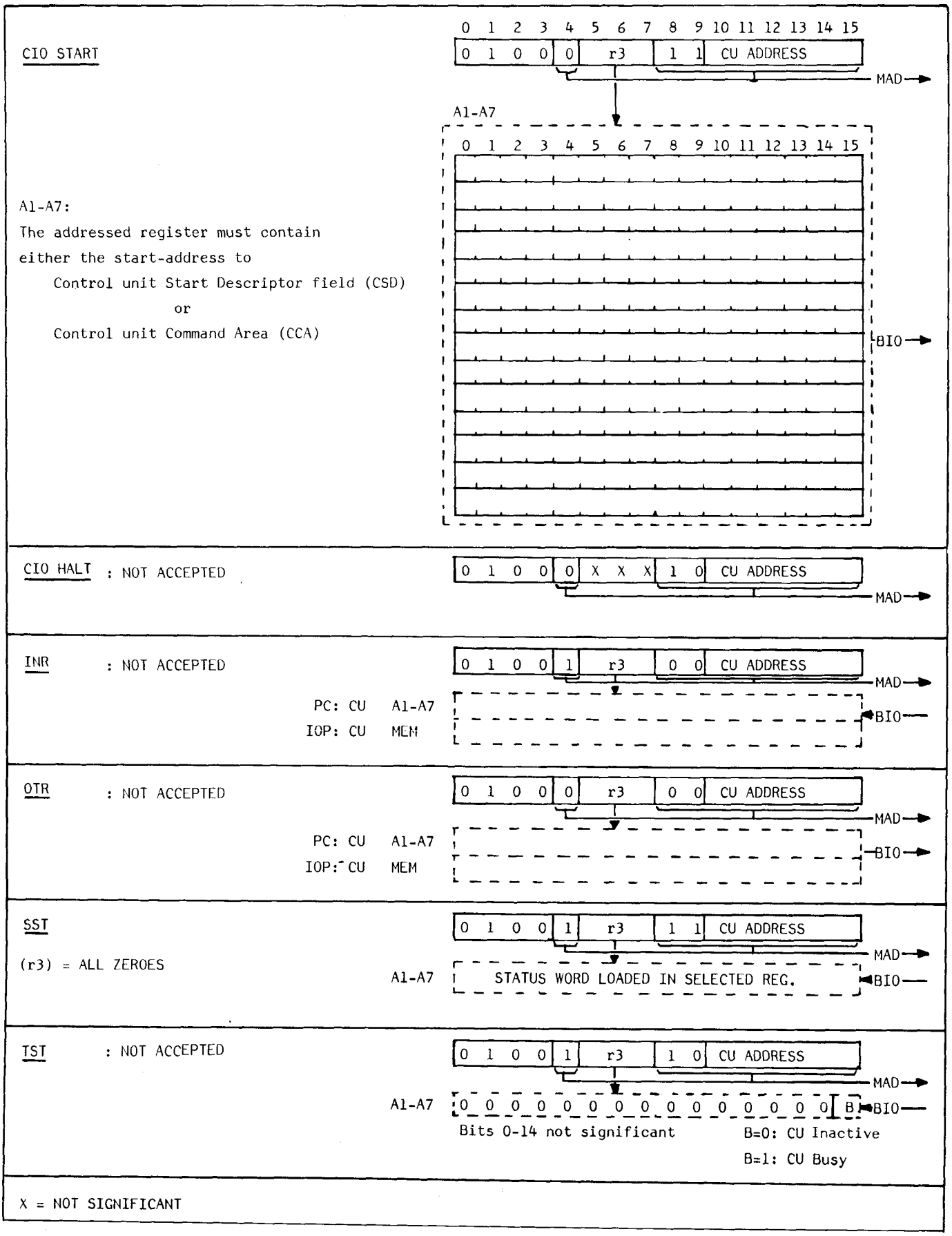


Figure 26.6 INSTRUCTION -/COMMAND-WORD FORMATS

COMMAND/RESPONSE INTERFACE BLOCKS

INITIALIZATION OF CHRW

After power-on the CHRW is in the RESET state and has to be initialized. During initialization three control blocks are transferred from main memory to CHRW, viz. Control unit Start Descriptor (CSD), Control unit Interface Descriptor (CID) and Control unit Command Area (CCA). Before the CCA is transferred to CHRW the control unit tests itself. (See Diagnostic tests)

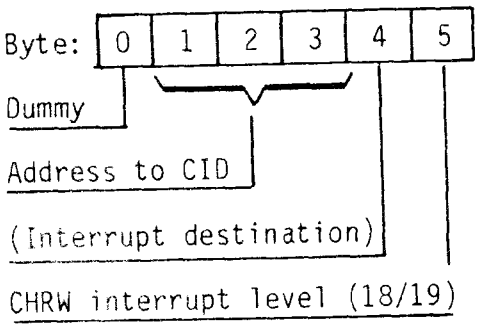


Figure 26.7 LAYOUT OF CSD

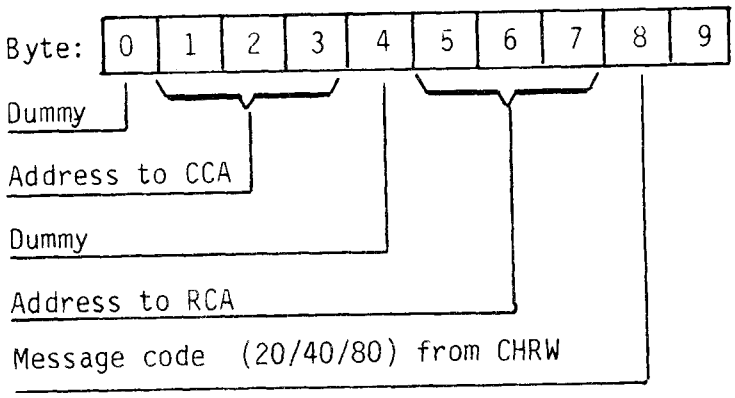


Figure 26.8 LAY-OUT OF CID

After the CHRW has completed a command it transfers a message code to byte 8 of CID in main memory, an updated CCA to Response Communication Area (RCA) in main memory and interrupts the CPU at a level as stated in byte 5 of CSD. (Software set Interrupt level of CHRW).
The start address of RCA is stated in CID.
For transfer of the blocks see figure 26.11, Data Flow Initialization, Output, Input, Attention Message.

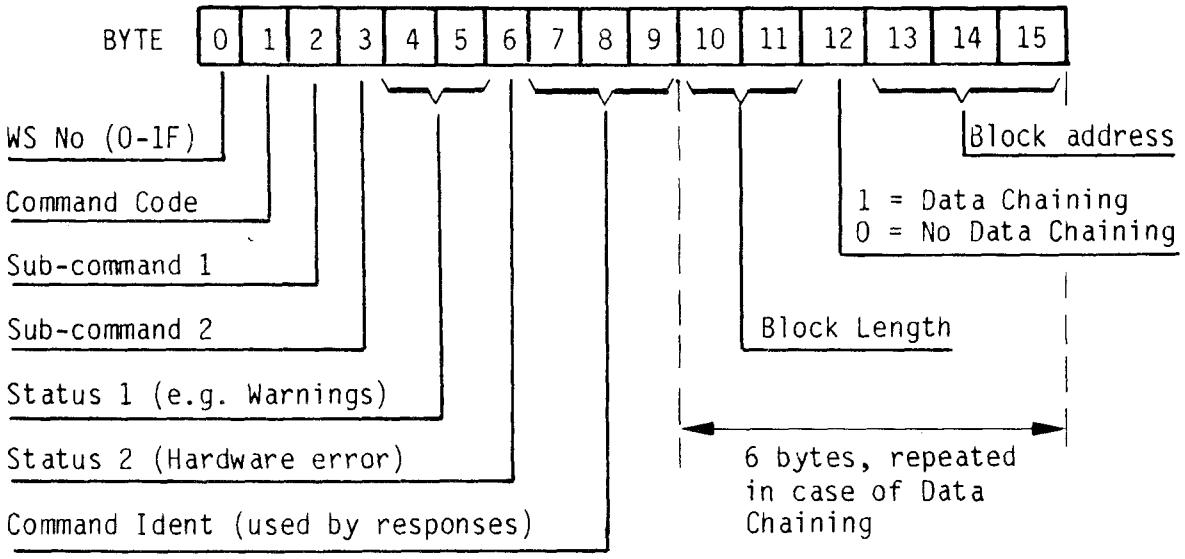


Figure 26.9 LAYOUT OF CCA/RCA

Three different message codes can be received from CHRW:

- Release: /40
- I/O Completion Code: /20
- Attention Code /80

CHRW sends the Release code if CSD or if CCA is transferred to the memory of the CHRW. Customer software now can fill these blocks with new information.
CHRW sends I/O Completion Code after a command is completely executed. The Attention Code is send by CHRW if there has been a change in the hardware, somewhere in the network or at the CHRW. This code has no relation to any command.
Directly after transfer of one of these codes the CHRW interrupts the CPU via the BIEC lines. These interrupts must be reset by means of an SST instruction.

All transfer between TC's main memory and the CHRW are controlled by the Direct Memory Access part of the CHRW. (Hardware Channel).
As the CHRW is acting as a Master, the control unit must be taken into the Master priority chain by means of the OKO-OKI signal. The priority order is set by the Customer's application.

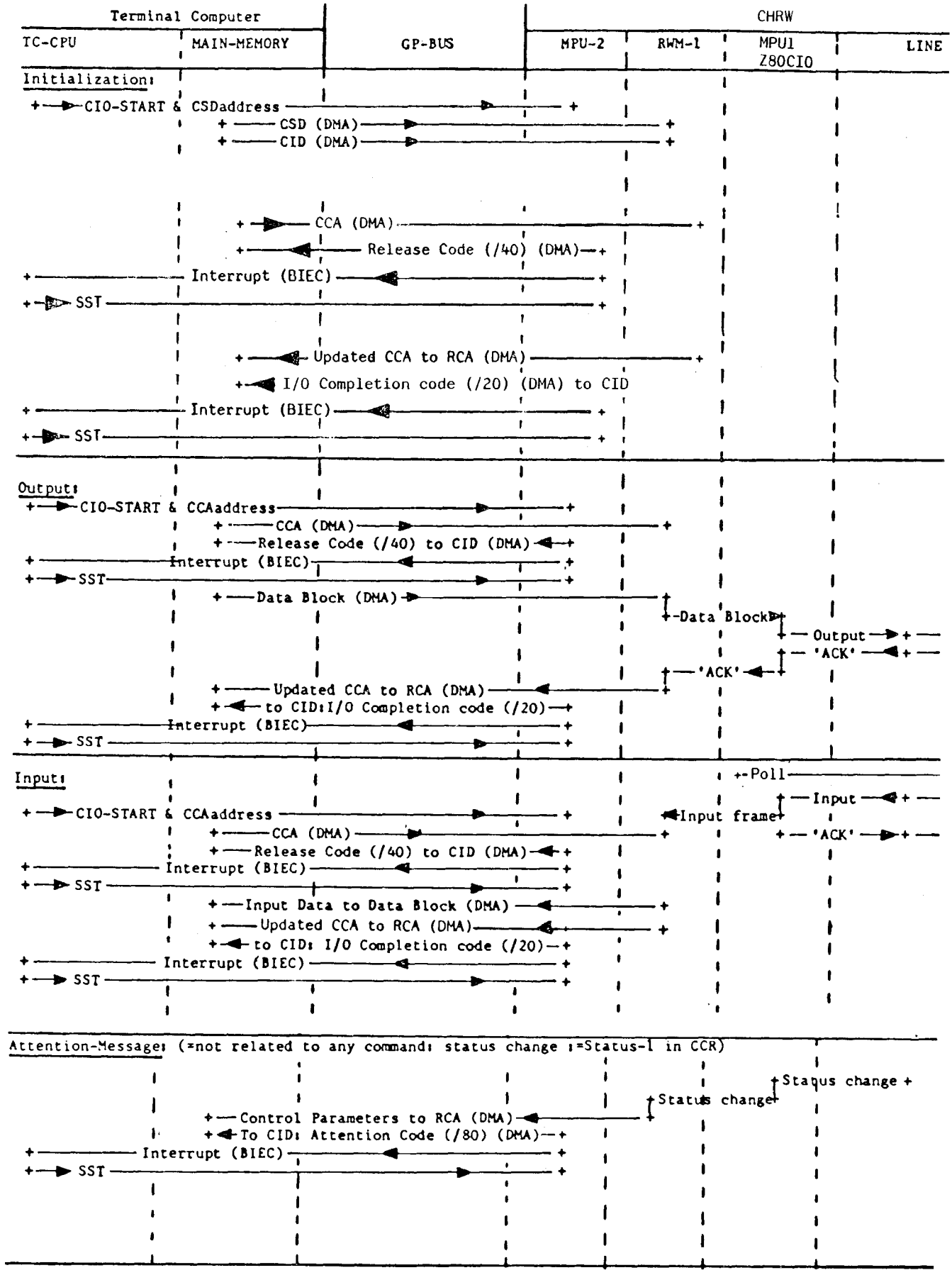
COMMAND CODES FOR CHRW

The CHRW recognizes the following command codes set in byte 1 of CCA. There are three types of command codes, with some commands additional information has to be sent in special formatted information blocks.

Command Code Hex	Command	Command Type	Remark
20	General Read	Input	From any WS
21	Specific Read	"	From addressed WS
40	Standard Write	Output	To addressed WS
41	Fast Write	"	To addressed WS with high priority
80	Test CU	Supervisory	Starts CHRW internal tests
81	Terminate (Not used)	"	Software Reset of CHRW
82	Close Line	"	Resets line parameters
83	Get DLS Statistics	"	Statistics for an addressed WS are transferred to TC.
84	Get Line Statistics	"	Statistics for the line counters are fetched to TC.
85	Open Data Link	"	Establishes a connection to a specified WS.
86	Open Line	"	Defines the type of line and sets the line parameters.
87	Read Local Memory	"	Read from RWM1 on CHRW to specified memory area in TC.
88	Cancel	"	Cancels a previously sent Read command.
89	Close Data Link		Closes the data link for a specific WS.

Figure 26.10 COMMAND CODES FOR CHRW

WS = Work Station



Following messages can be given:
If the WS is disconnected: No Connection
If the CHLW has reset the Link: Link Reset
If the CHLW has re-established the data link: Communication Re-established
The information is put in Status-1 of RCA.

Figure 26.11 DATA-FLOW INITIALIZATION, OUTPUT, INPUT, ATTENTION MESSAGE

26.5 DIAGNOSTIC TESTS

In the software of the CHRW are implemented 4 diagnostic test types:

- Start-up test
- In-line test
- On-line test
- Off-line test (= Start-up test)

The outcome of the test is displayed in hex. format on four leds at the front of the CHRW, at the bottom.
The modem-signal Data Set Ready (107), for each line separately, is displayed with a led positioned between the connectors J20 and J30.

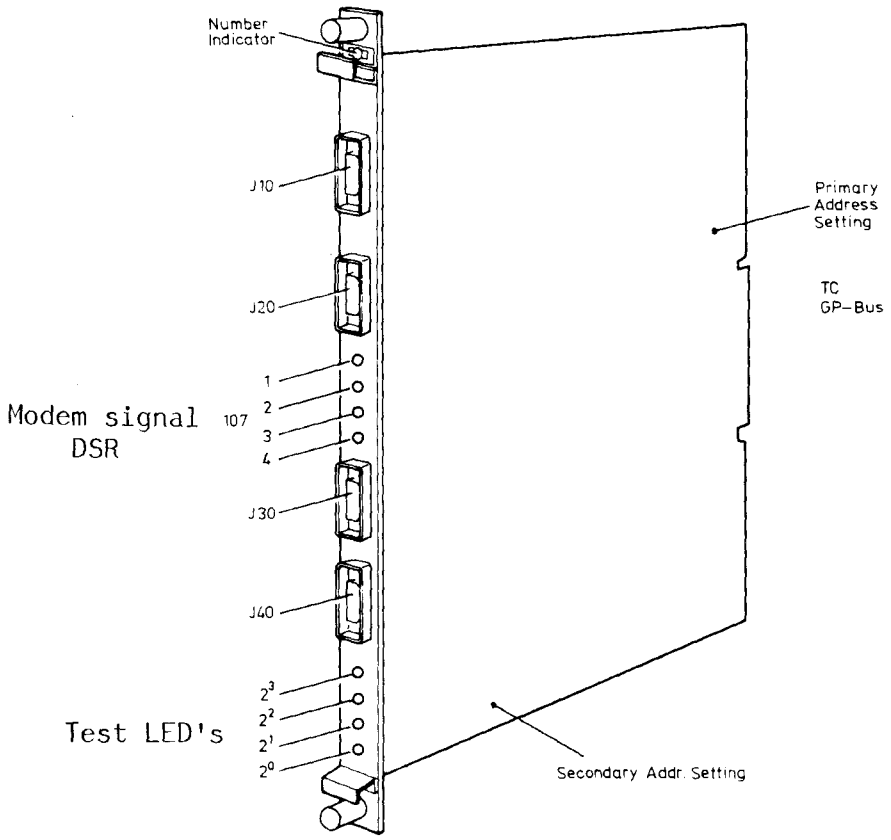


Figure 26.12 POSITION OF LEDS

START-UP TEST AND OFF-LINE TEST

The Start-up test and the Off-line test are exactly the same but intitiated in different ways.

The start-up test is started by "power-up".
The Off-line test is started when the IPL button or the Master-Clear button are pressed. The test-codes are shown in the figure below.

In case of an error the LEDs for the corresponding code are flashing.
If the LEDs are flashing the CHRW will not respond to any command from the host program because it put itself into NOT OPERABLE state.
The test can be started again by means of Power off/on, IPL- or MCL-button.
The following internal logic are tested in the test:

- MPU 1
- ROM1 (all data LRC checked)
- RWM1 (all location are written into, read and reset)
- MPU2
- ROM2 (all data is LRC checked)
- RWM2 (all locations are written into, read and reset)
- MPU3
- ROM3 (all data is LRC checked)
- RWM3 (all locations are written into, read and reset)

TEST CODE Hex	2^3	2^2	2^1	2^0	Meaning
0	0	0	0	0	No error, and "TEST CU"-command received
1	0	0	0	●	ROM 1 error, MPU 1
2	0	0	●	0	ROM 2 error, MPU 2
3	0	0	●	●	ROM 3 error, MPU 3
4	0	●	0	0	RWM 1 error, bit 0/1, MPU 1
5	0	●	0	●	RWM 1 error, bit 2/3, MPU 1
6	0	●	●	0	RWM 1 error, bit 4/5, MPU 1
7	0	●	●	●	RWM 1 error, bit 6/7, MPU 1
8	●	0	0	0	RWM 2 error, MPU 2
9	●	0	0	●	RWM 3 error, MPU 3
A	●	0	●	0	HDLC error/Data loop error, not flashing
B	●	0	●	●	RWM 1 error, MPU 2
C	●	●	0	0	RWM 1 error, MPU 3
D		----			Not used
E	●	●	●	0	Test OK, but no "Test CU" yet, not flashing.
F	●	●	●	●	Hardware reset received, not flashing.

Figure 26.13 TEST CODES START-UP OFF-LINE TEST

To switch the CHRW from the RESET to NORMAL OPERATION mode the TEST-CU command must be given by the host program.
This command is only accepted if no error was detected in the Start-up test.
The TEST-CU command starts the Start-up test all over again.
It takes about 10 seconds between a reset and accepting the TEST-CU command.

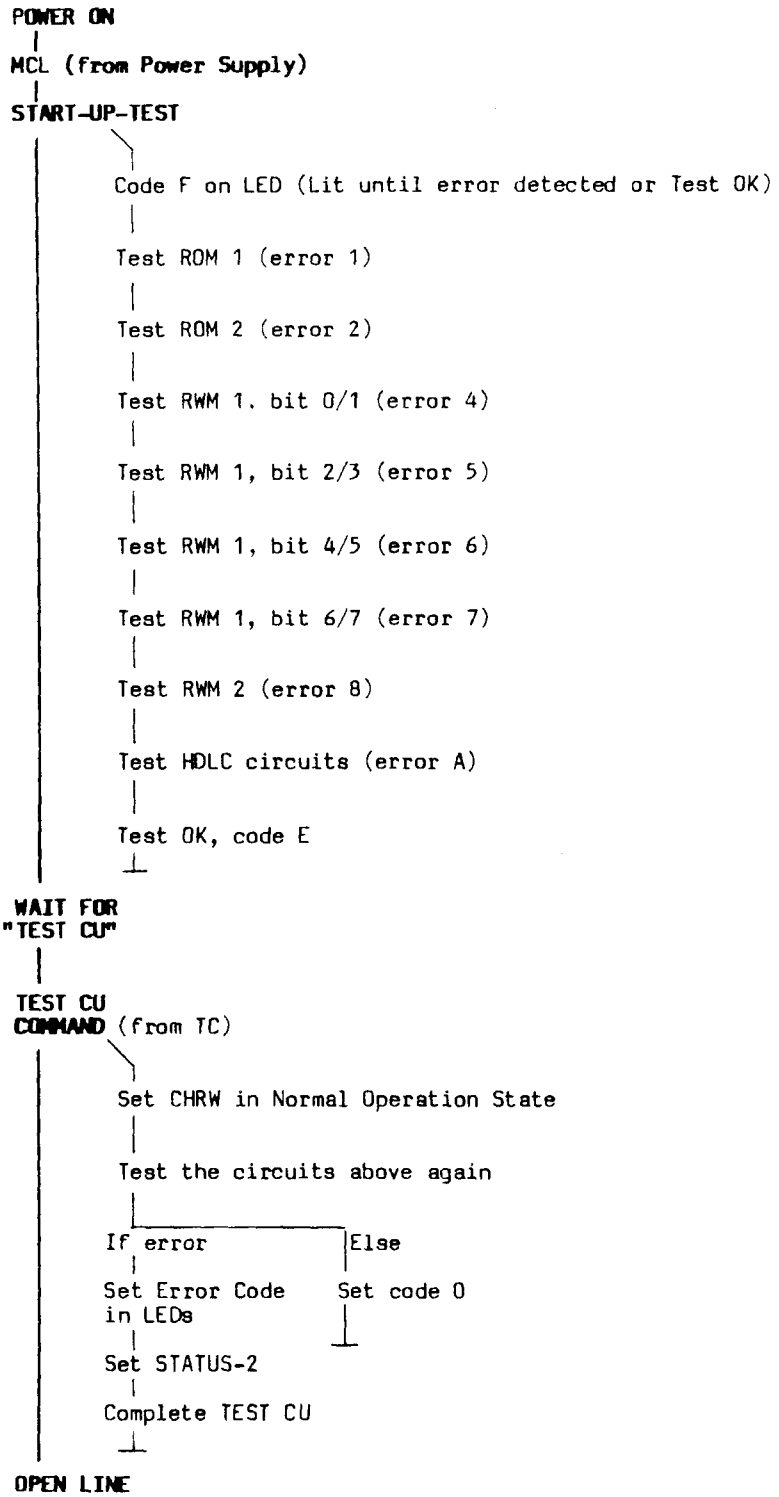


Figure 26.14 FLOW OF TEST-PROGRAM

IN-LINE TEST

The In-Line test is activated several times by CHRW during run-time without affecting the user's application.

The /B and /C in the figure below indicate that an error has been detected. The CHRW however, will continue its normal execution in order to allow the host program to detect the error by means of a TEST-CU command.

TEST CODE Hex	2^3 2^2 2^1 2^0	Meaning
B	ø 0 ø ø	MPU 1 error, not flashing
C	ø ø 0 0	MPU 2 error, not flashing
D	ø ø 0 ø	MPU 3 error, not flashing

Figure 26.15 ERROR CODES IN-LINE TEST

ON-LINE TEST

The On-Line test is activated by means of a TEST-CU command during the time the CHRW is in NORMAL OPERATION mode.

The following actions are taken:

- If the In-Line test previously has detected an error, the TEST-CU command is immediately executed.
- A ROM2 and a simple RWM1 test is performed.
  If an error is detected the appropriate LEDs, as shown in the figure below, are lit.
- A ROM1 and a simple RWM1 test is performed.
  If an error is detected the appropriate LEDs, as shown in the figure below, are lit.
- If no error is detected the TEST-CU command is completed with the fields STATUS-2 in the RCA set to zero.

In case of an error the Test code is duplicated in the 4 least significant bits of the STATUS-2 field after the TEST-CU command has been completed.

TEST CODE Hex	2^3 2^2 2^1 2^0	Meaning
1	0 0 0 ø	ROM 1 error, MPU 1
2	0 0 ø 0	ROM 2 error, MPU 2
3	0 0 ø ø	Not used
4	ø 0 0 0	RWM 1, bit 0/1, MPU 1
5	0 ø 0 ø	RWM 1, " 2/3, MPU 1
6	0 ø ø 0	RWM 1, " 4/5, MPU 1
7	0 ø ø ø	RWM 1, " 6/7, MPU 1
8	ø 0 0 0	RWM 2 error, MPU 2

Figure 26.16 TEST-CODES ON LINE TEST

OFF-LINE TEST:

To activate the Off-Line test the DIP-switch number 8 in the Primary Address Field must be opened (= set to '1'). (If this switch is set to '0' the Secondary address is enabled. Also a data loop must be set up before the test is started (on one or more channels).

This is possible in two different ways:

1. By looping the data with a specially prepared connector on the board. Also the interface circuits must be looped.
2. By setting the LOOP-3 button on the site modem or the LOOP-2 button on one or more of the remote modems.

The Off line test first verifies the internal logic in the CHRW (Start-up test) and then checks the data channel(s) with the Data-Channel test.

The DIP-switches for the Secondary Address are used to select the different test modes:

Dipswitch No.	Open (1)	Closed (0)
1	-	Test of channel 0
2	-	Test of channel 1
3	-	Test of channel 2
4	-	Test of channel 3
5		
6	Single Test	Loop test
7	Stop on error	No stop on error (without error detection and error code display, intended for signature testing) However, stop on start up test error.
8	Off-Line Test Selected	Second.Workstation Number

Figure 26.17 SECONDARY DIP-SWITCH SETTING/TEST MODE

The error codes displayed are the same as for the Start-up/Off-line test (see figure 26.13. Test codes Start-up/Off-line test)

If no error is detected during the Data-Channel test, code/E is displayed, code /A indicates a data loop error.

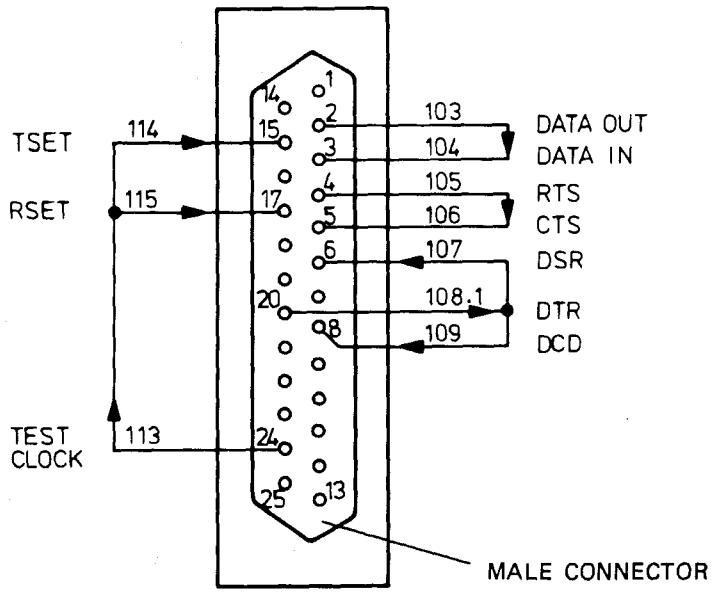


Figure 26.18 LINE LOOP TEST CONNECTOR

FAULT FINDING AIDS

TEST AND 107-LEDs

The fault symptoms that can be discovered during run time are shown in the flowchart together with the advised remedy.

Use the Test LEDs and the 107-LEDs (one for each channel) on the CHRW board to trace the faults. Besides, watch the operation of the devices during the Off-Line test when the Test-switch is set ON at respective Main Module of the workstations.

TEST PROGRAM

To test the network and the connected terminals the test-program TERTST4.2 and higher releases may be used.
See detailed description of TERST4.x.

MODEM TEST

The data modem is provided with extensive test facilities.
Line and interface loops can be set.
These loops are according to CCITT recommendation V54, controlled via certain CCITT interchange circuits or by TEST switches on the modem front.

With a remotely controlled test loop a rapid location of a faulty transmission element can performed by the operator at the local station in a 'point-to-point' link, without any assistance from the remote station.

However, control signals for the setting of this loop must be transmitted on the backward channel. (= not for data transfer used frequency band in the total frequency band of the line).

Test-procedure of Local modem:
To test the local modem, the loop test "LOOP-3" is used.
It is a full duplex test which can be set by:

Switch "LOOP-3" on the modem front panel.

When the loop is set, the test is started when the reset button on TC is pressed. The result of the test is displayed on the TEST LEDs of the CHRW board. (See figure 26.13. Test codes Start-up/Off-line test)

An /E is displayed when the internal test of the CHRW board is finished and no errors are detected.
Hereafter the loop test starts at the channel selected by the switch set in the Secondary Address field (see figure 26.17. Secondary DIP-switch setting/Test mode).
An /A is displayed if the channel is faulty, otherwise code /E remains displayed.

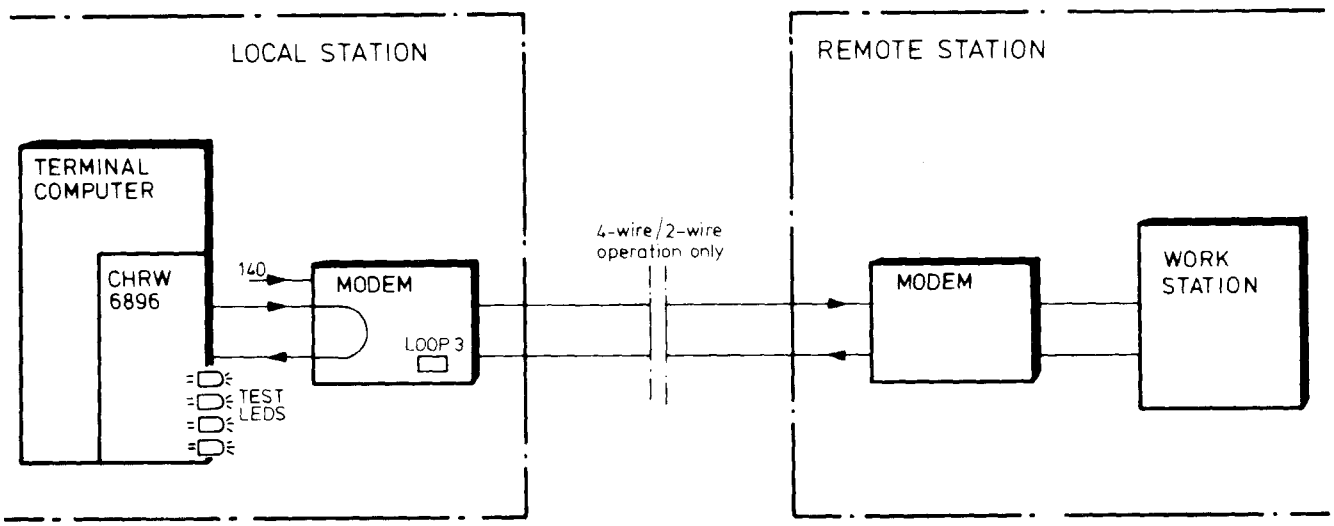


Figure 26.19 LOCAL MODEM TEST

TEST-PROCEDURE OF THE REMOTE MODEM

The remote modem at the other end of the telephone line, as well as the local modem, can be tested by setting the test "LOOP-2".

The test is set by either 1 or 2.

1. Switch "LOOP-2" on the front panel of the Remote modem. See figure 26.21. Remote modem test, LOOP-2, remote set.
2. Switch "REMOTE LOOP-2" on the front panel of the Local modem. With this test the backward channel, implemented in the modem is used. See figure 26.20 Remote modem test, LOOP-2, local set.

The result of the test is displayed by the LEDs at the front panel of the CHRW. See figure 26.13. Test codes Start-up/Off-line test.

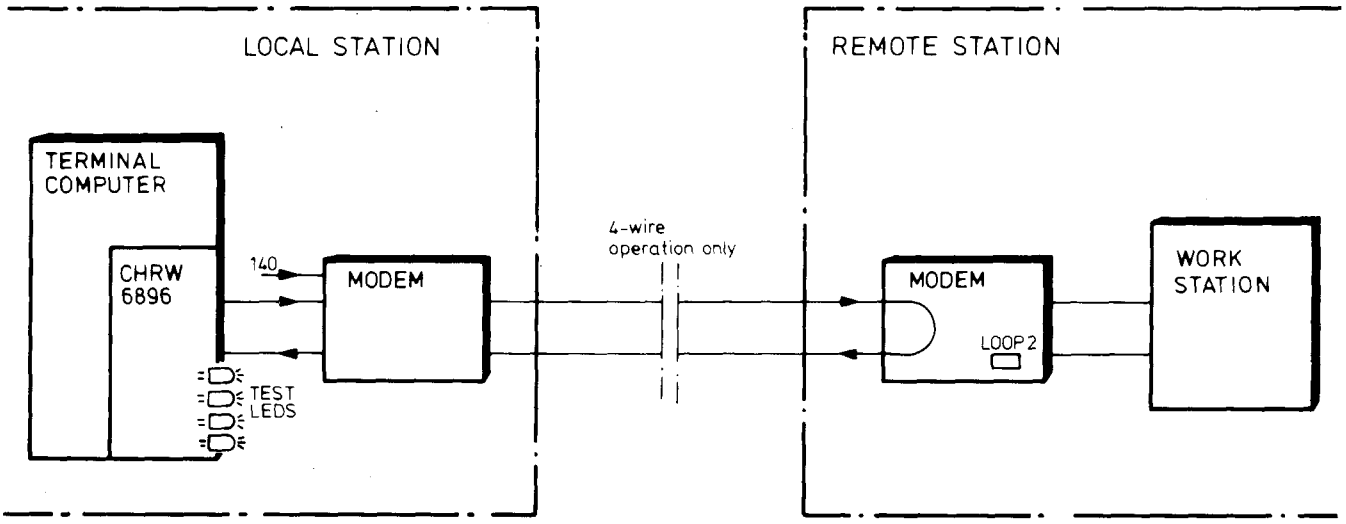


Figure 26.20 REMOTE MODEM TEST, LOOP-2, LOCAL SET

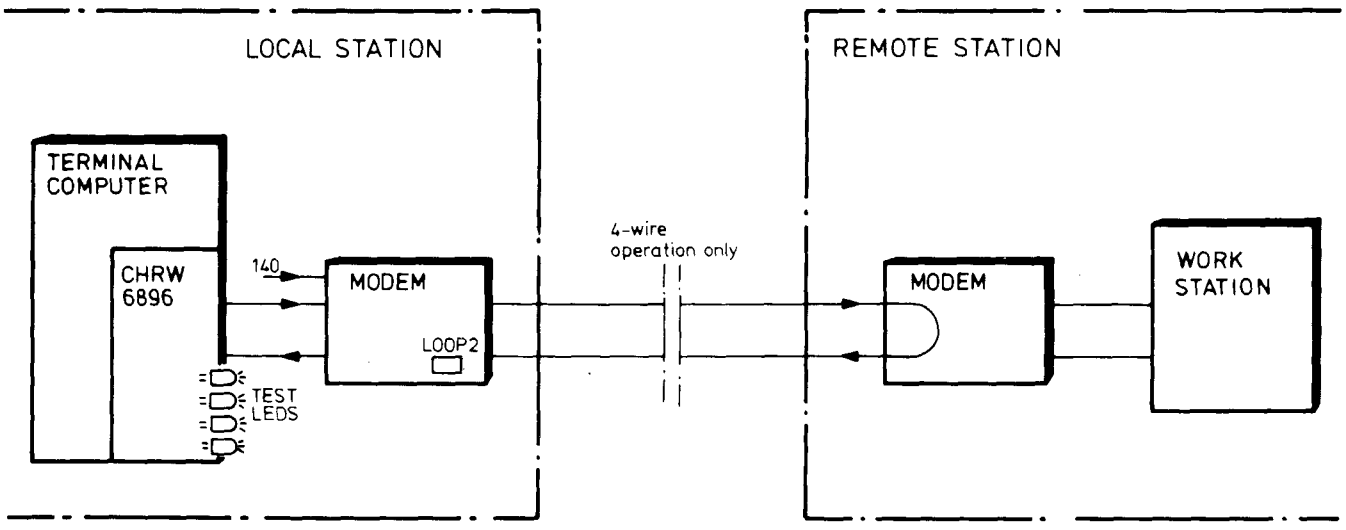


Figure 26.21 REMOTE MODEM TEST, LOOP-2 REMOTE SET

SIMULATED MODEM TEST

With a special wired connector, simulating the modem, each channel can be tested. The connector is shown in figure 26.18. Line-loop Test connector.

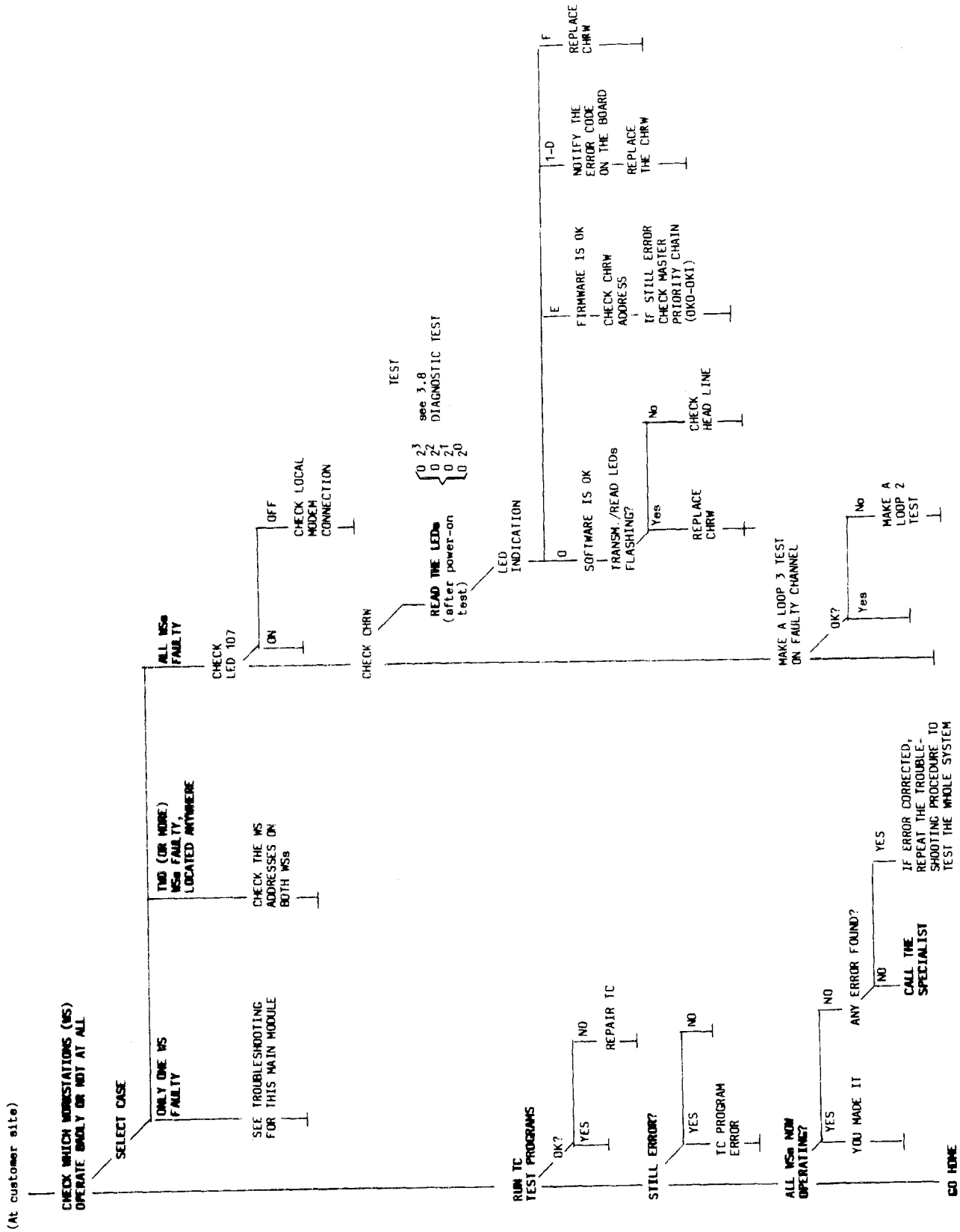


Figure 26.22 RWSI TROUBLE SHOOTING PROCEDURE

27 CHANNEL UNIT FOR DATA COMMUNICATION HDLC-X.21

LIST OF ILLUSTRATIONS

LIST OF TABLES

27.1 CHDX IDENTIFICATIONS (Line Controller for HDLC - X.21)

Type Number	: PTS-6891-002 This Channel Unit is a combination of : - GP Bus Adaptor Board, 5131 194 07900 - PTS-6858-003, CUDX, 5111 199 55670 - Panel, 5131 193 53000 The assembly is identified with 5131 194 90500
Control Unit Address	: Depending on application
Interrupt levels	: One for Receiver part and one for Transmitter part: Depending on application
Channel	: Programmed Channel
Power Consumption	: +5 Volt, 2.5 Amp. +18 Volt, 50 mAmp. -18 Volt, 50 mAmp.
Number of Lines	: 1 line
Line Interface	: CCITT X.24, X.27, CCITT X.21
Transmission Speed	: Less or equal to 4800 bits per second
Timing Control	: External clock
Transmission Type	: Full duplex, Bit oriented in data phase, Character oriented in connection phase
Data Length	: Data Phase: 16 bits Connection Phase, 8 bits
Parity Control	: Data Phase: FCS according to ECMA-40
Special features	: Forced data phase, NRZ or NRZI strap selectable
Procedures	: HDLC protocol for circuit switched networks (X.21) Byte timing not supported
Software	: TOSS driver DRDC23 (Release 11 and higher)
Test Program	: t.b.f.

CONNECTOR 1J:

Pin Number	Signal Name	Pin Number	Signal Name
1C01		1A01	
1C02		1A02	
1C03	BCI**	1A03	INCL**
1C04	IR1N*	1A04	BR1N*
1C05	IRØN*	1A05	BRØN*
1C06	0 Volt	1A06	0 Volt
1C07	PWFN	1A07	RSLN
1C08	CLEARN	1A08	ACN
1C09	0 Volt	1A09	0 Volt
1C10	TMPN	1A10	TSMN
1C11		1A11	
1C12	0 Volt	1A12	0 Volt
1C13	MADØØ	1A13	MADØ1
1C14	MADØ2	1A14	MADØ3
1C15	MADØ4	1A15	MADØ5
1C16	MADØ6	1A16	MADØ7
1C17	MADØ8	1A17	MADØ9
1C18	MAD10	1A18	MAD11
1C19	MAD12	1A19	MAD13
1C20	MAD14	1A20	MAD15
1C21		1A21	
1C22	0 Volt	1A22	0 Volt
1C23	BIØ8-N	1A23	BIØØ-N
1C24	BIØ9-N	1A24	BIØ1-N
1C25	BI010-N	1A25	BIØ2-N
1C26	BI011-N	1A26	BIØ3-N
1C27	BI012-N	1A27	BIØ4-N
1C28	BI013-N	1A28	BIØ5-N
1C29	BI014-N	1A29	BIØ6-N
1C30	BI015-N	1A30	BIØ7-N
1C31		1A31	
1C32	+5 Volt	1A32	+5 Volt

Note: ** Not used with PTS

* Are connected via Adaptor card.

Receiver interrupt: 1CØ4
Transmitter interrupt: 1CØ5

Receiver Break: 1AØ4
Transmitter Break: 1AØ5

Table 27.1 GP-SIMPLIFIED BUS INTERFACE CONNECTOR 1J

CONNECTOR 3J:

Pin Number	Signal Name	Function	Direction
3J02 3J09	T-N T-P	Transmission Line	From HLXCU3 to DCE
3J03 3J10	C-N C-P	Control Line	From HLXCU3 to DCE
3J06 3J13	S-N S-P	Signal Element Timing	From DCE to HLXCU3
3J07 3J14	B-N B-P	Byte Timing	From DCE to HLXCU3
3J04 3J11	R-N R-P	Receiver Line	From DCE to HLXCU3
3J05 3J12	I-N I-P	Indicator Line	From DCE to HLXCU3
3J08	G	Ground	

Table 27.2 X21 INTERFACE CONNECTOR 3J

CONNECTOR 4J:

Pin Number	Signal Name	Function	Direction
4B03	IVBØ-N	Internal Bus Signal	To Test tool
4B02	IVB1-N		
4B01	IVB2-N		
4A13	IVB3-N		
4A12	IVB4-N		
4A11	IVB5-N		
4A10	IVB6-N		
4A09	IVB7-N	Internal Bus Signal	To Test tool
4B13	APROGØØ	Internal Address line	To Test tool
4B12	APROGØ1		
4B11	APROGØ2		
4B10	APROGØ3		
4B09	APROGØ4		
4B08	APROGØ5		
4B07	APROGØ6		
4B06	APROGØ7		
4B05	APROGØ8		
4B04	APROGØ9		
4A03	APROG1Ø	Internal Address line	To Test tool
4A07	OSCTEST	Oscillator signal	From Test tool
4A08	0 Volt		
4A06	0 Volt		
4A04	+5 Volt		To Test tool

Table 27.3 INTERFACE TEST CONNECTOR 4J

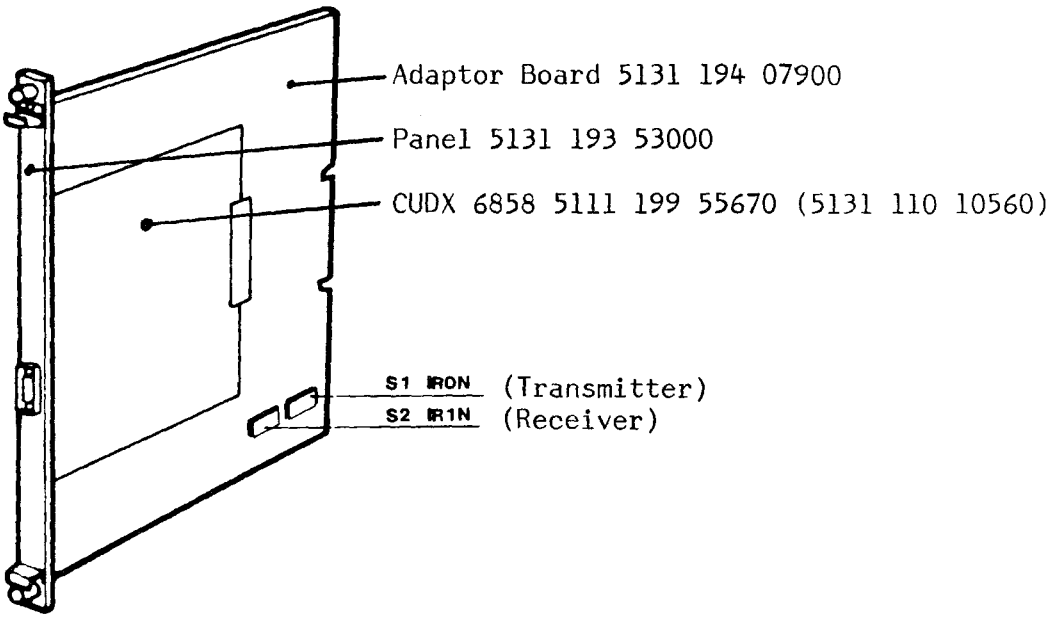


Figure 27.1 P-6891-002 (ASSEMBLY)

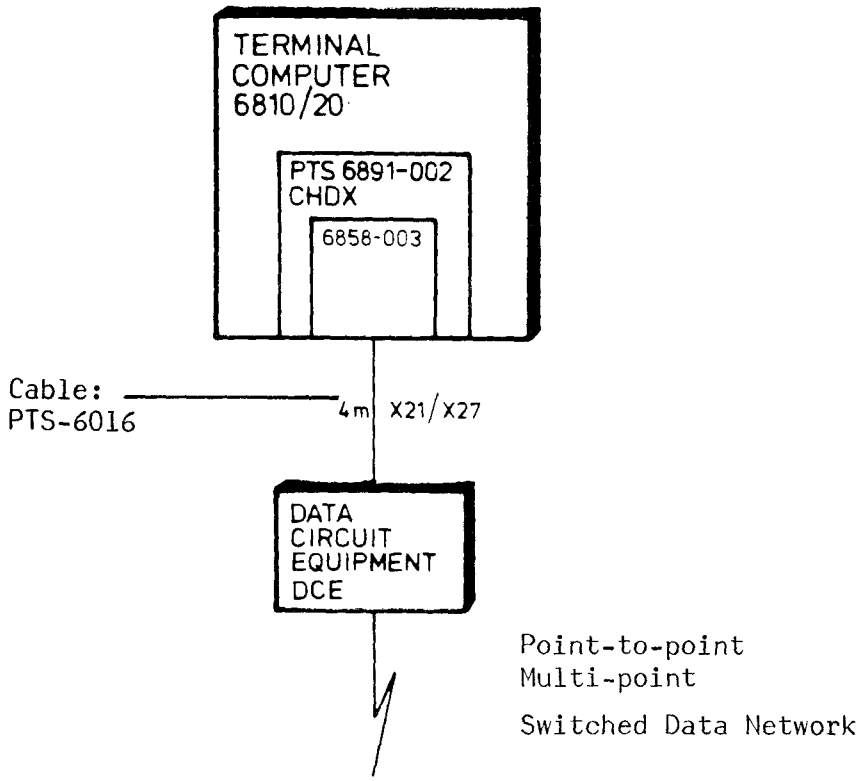
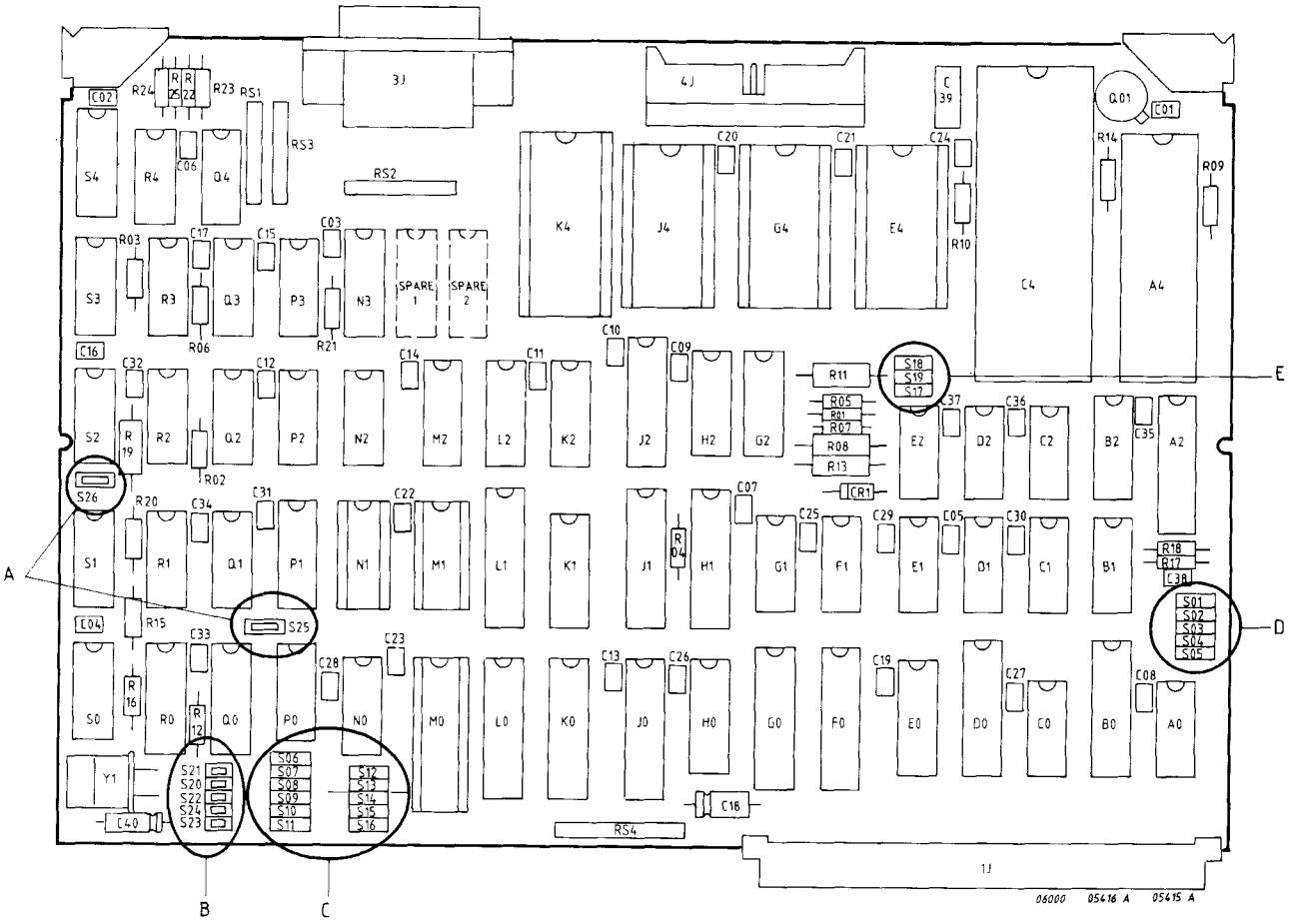
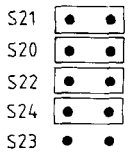


Figure 27.2 P-6891 IN A SYSTEM



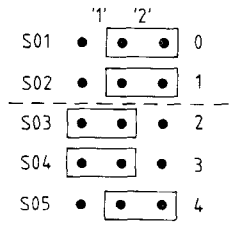
A- S26, S25: Must be fitted for normal operation.

B- Single Interrupt selected.
Receiver Interrupt Output pin: 1C04 (conn. 1J)
Transmitter Interrupt Output pin: 1C05 (conn. 1J)
See further General Purpose Bus Adaptor.



C- Interrupt Level Selection.
Not significant. The interrupt level is strapped at GP Bus Adaptor.

D- Control Unit Address Selection.
MAD10-MAD14 (S01-S05) are strapped for the Receiver part. The Transmitter part is then addressed by: (Receiver part + 1)



Example: /0C (Rec.)
/0D (Trx.)

E- S18 (Enable Oscillator) must be fitted.
S19 & S17 (NRZI or not) must be strapped according the mode selected.

Figure 27.3 STRAP SETTINGS

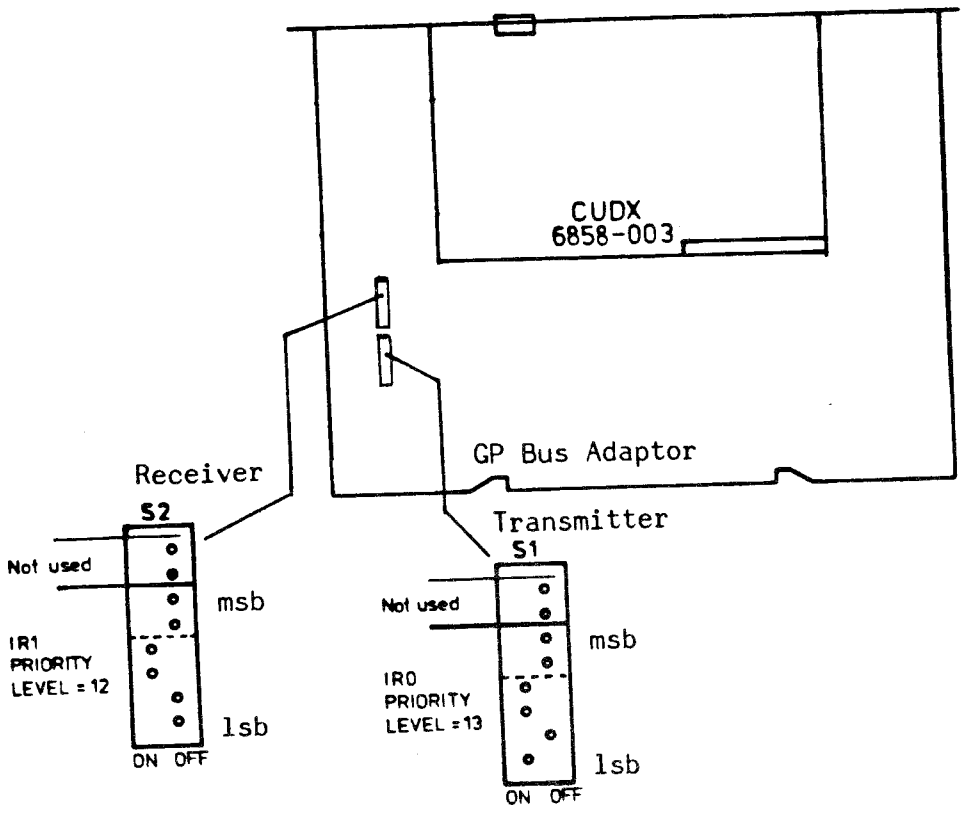


Figure 27.4 INTERRUPT SWITCHES ADAPTOR BOARD

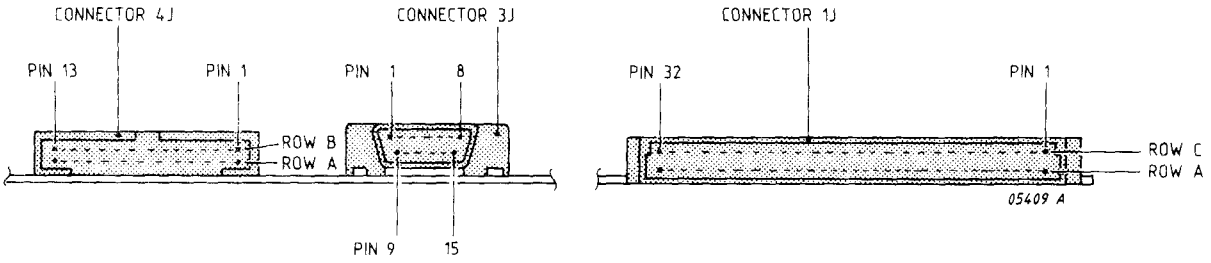


Figure 27.5 LAYOUT CONNECTORS 4J, 3J, 1J

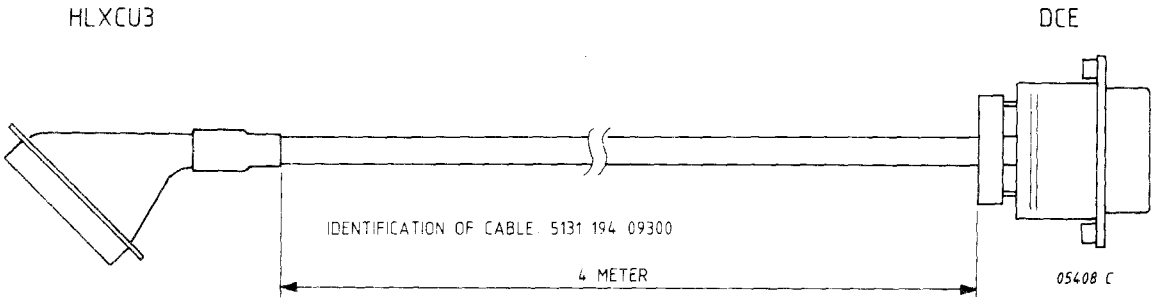


Figure 27.6 DCE CABLE PTS-6016

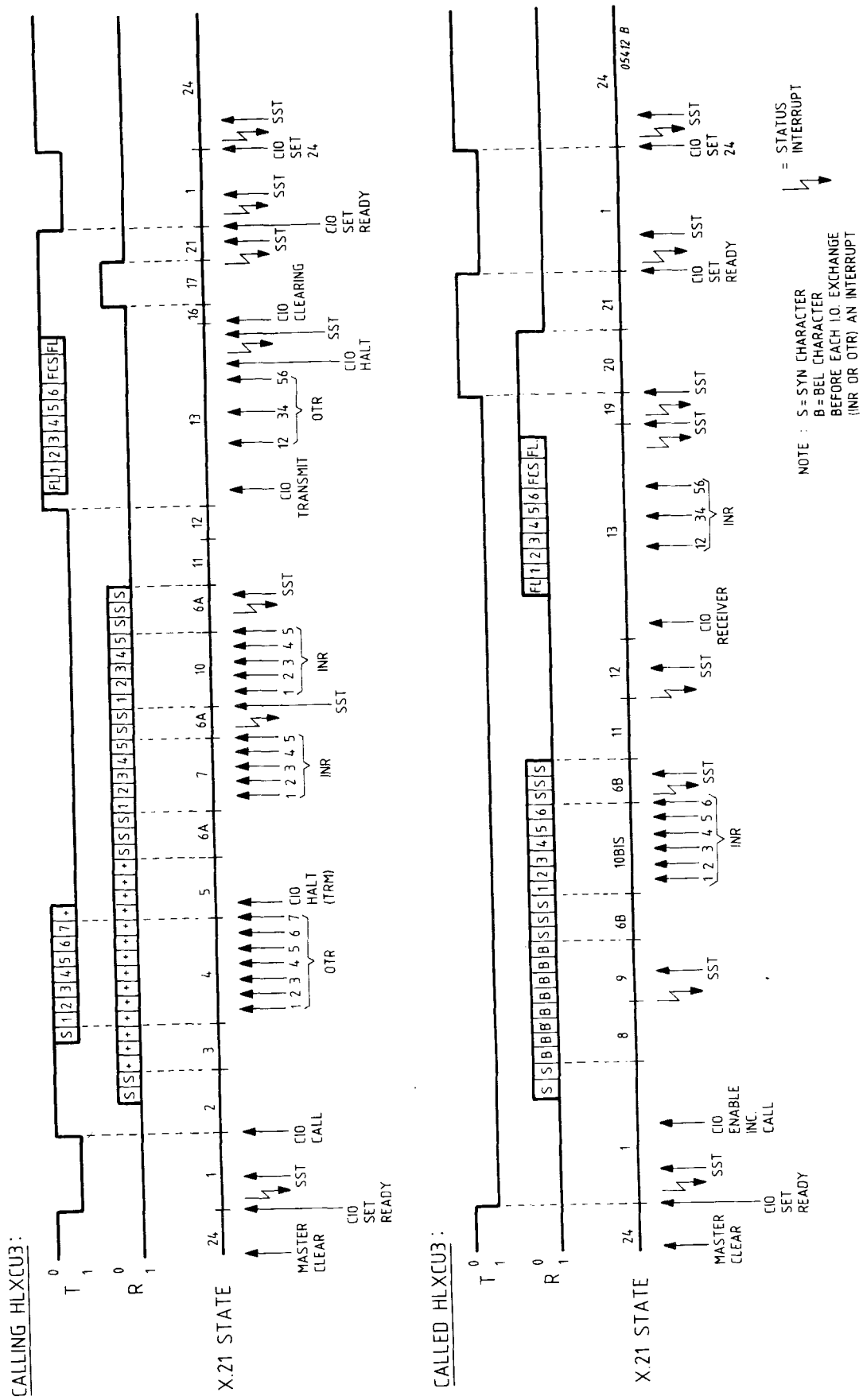


Figure 27.7 COMMAND TIMING

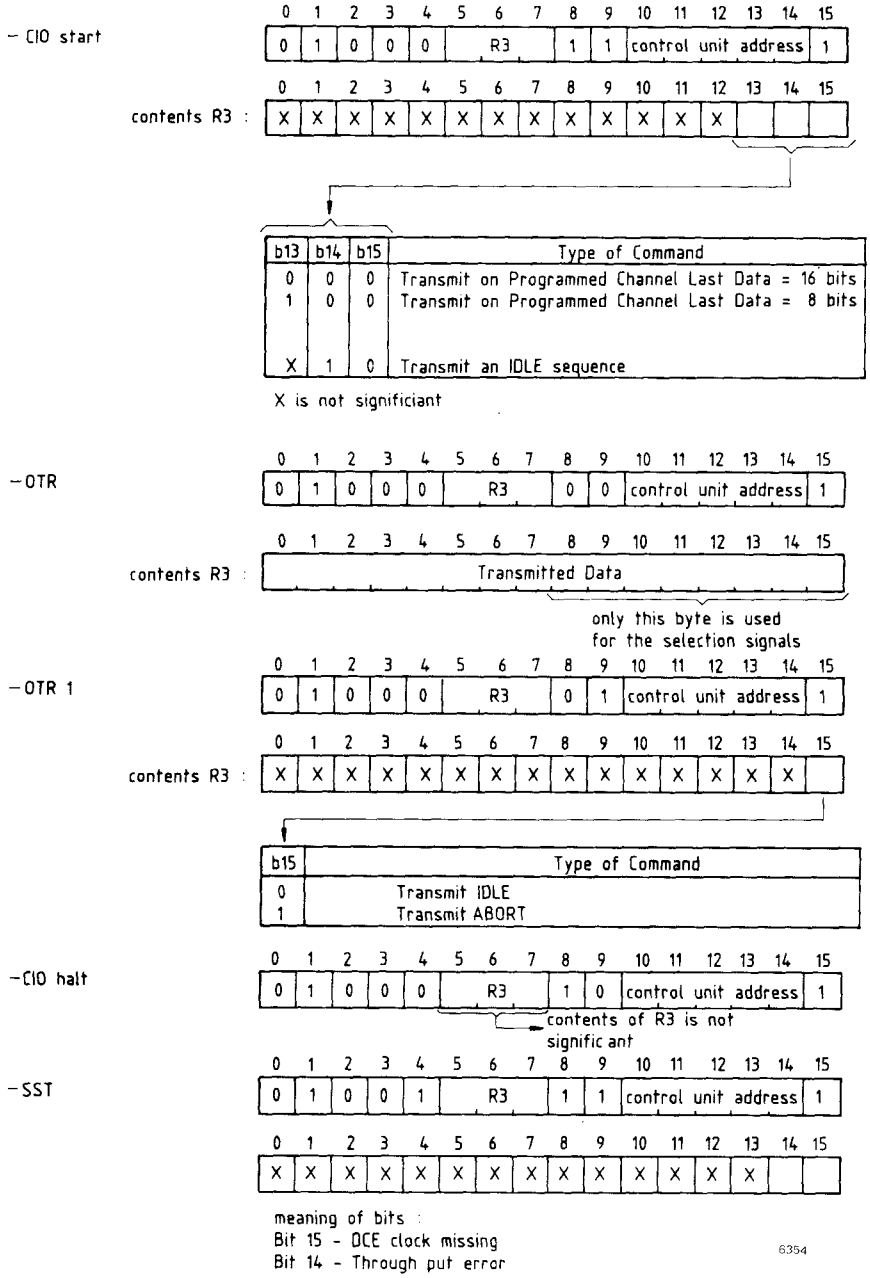


Figure 27.8 TRANSMITTER COMMANDS SUMMARIZED

Receiver Commands

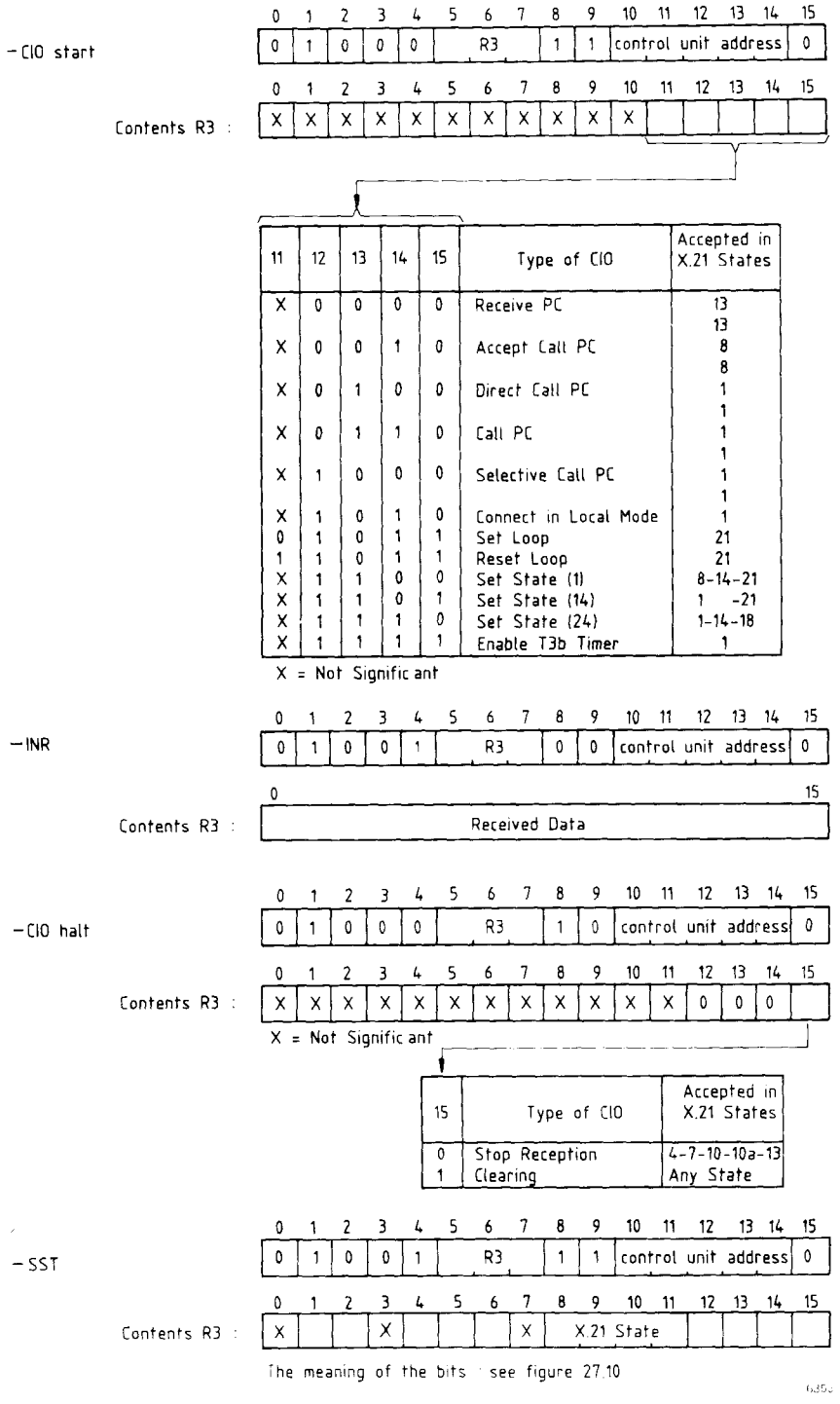
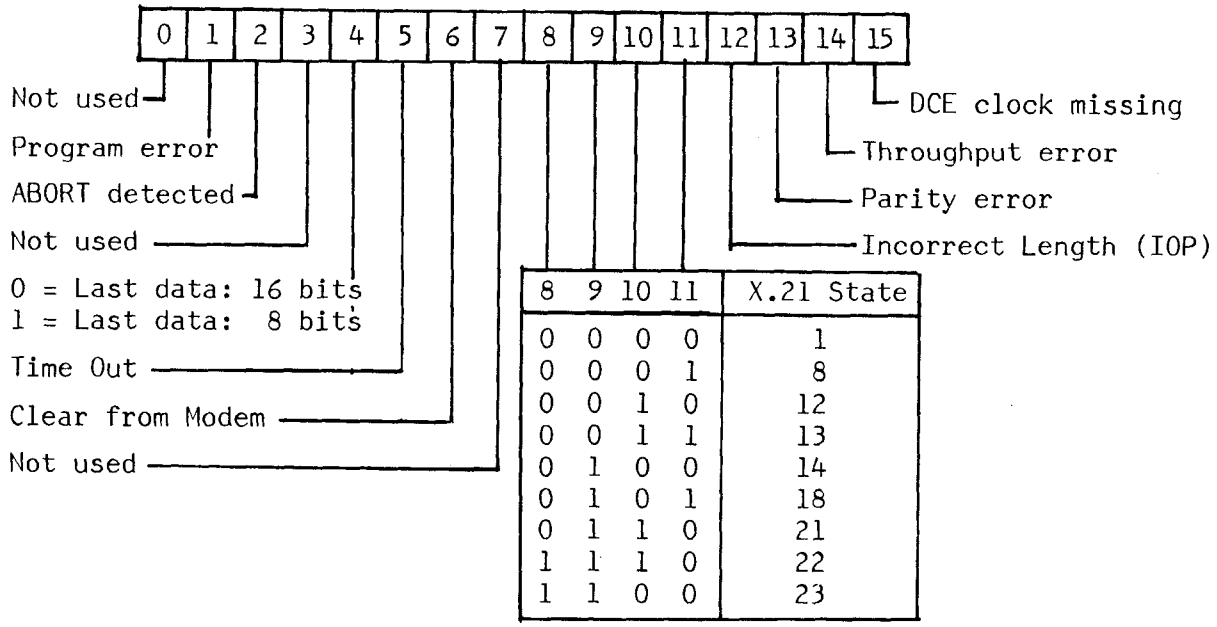


Figure 27.9 RECEIVER COMMANDS SUMMARIZED

Status word from Receiver part:



8	9	10	11	X.21 State
0	0	0	0	1
0	0	0	1	8
0	0	1	0	12
0	0	1	1	13
0	1	0	0	14
0	1	0	1	18
0	1	1	0	21
1	1	1	0	22
1	1	0	0	23

Status word from Transmitter part:

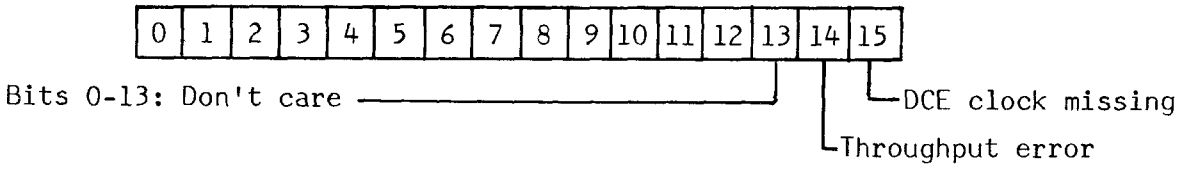


Figure 27.10 STATUS INFORMATION RECEIVER AND TRANSMITTER

27.5 TEST PROGRAMS

Not available (May 1985)