RC900

KAS451 Keyboard Assembly

Hardware reference manual

PN: 99110982

PN: 99200389

RC Computer

Keywords:
KAS451, KBU451, RC930, Keyboard

Abstract:
This paper contains a hardware description of the KAS451 used in the RC930 keyboard. The main electronic elements are discussed, and the diagram is provided. Datasheets of important components are provided.

Date:
October 1987

Author:
Troels H. Johansen

TABLE OF CONTENT PAGE

1. General overwiew..... 1

2. The hardware..... 1
2.1 The processor..... 1
2.2 The NVM (Non Volatile Memory)..... 1
2.3 Communication interface..... 1
2.4 The program store..... 1
2.5 Scanline selection..... 2
2.6 Auxillary output register..... 2
2.7 Key click generation..... 3
2.8 Monitor control..... 3

3. Logic diagrams..... 4

4. Intel 80c31 Datasheet..... 7

5. NMC9306 Datasheet..... 19

1. General overview

The technical name for the RC930 keyboard is KBU451 (KeyBoard Unit). One part of the KBU451 is the KAS451 (Keyboard ASsembly). The KAS is the printed circuit board with electronics and key-switches. The scope of this document is to provide a technical description of the KAS451.

In addition to the information provided in this document, the reader should be familiar with the keyboard description given in "Programmer's Technical Guide, RC900".

2. The hardware

In the following sections the hardware architecture will be discussed. Please refer to the diagram in the end of this document.

2.1 The processor

The KAS is build around a Intel 80C31 single chip CPU. The CPU contains 128byte RAM which is the only RAM in the system. The program is external to the CPU (pin 31 VPP/-EA is grounded). A ceramic resonator (X1) is used to generate the 6MHz +-0,5% CPU clock. Please note that the C5 and C6 capacitor only should be mounted if a crystal is used instead off the resonator.

2.2 The NVM (Non Volatile Memory)

A serial 16x16bits EEPROM (IC9 NMC9306) is used for storing of the following parameters: Contrast value
- Brightness value
- Brightness limitation function
- Key-click on/off
- Key-click volume
- Contrast timeout function
- 10 system accessible bytes

The NMC9306 data sheet is shown in appendix 1. The following NMC9306 commands are used: READ
- WRITE
- ERASE
- ENABLE ERASE/WRITE
- DISABLE ERASE/WRITE

In order to write a given NVM-cell, the following sequence must be performed:
ENABLE ERASE/WRITE
ERASE <address>
WRITE <address> <data>
DISABLE ERASE/WRITE

2.3 Communication interface

The CLOCK- and DATA-line is used for communication with the system. In order to implement the communication protocol described in ref.1, the two lines are both wired-and.
The CLOCK- and DATA-lines are driven by P3.0 and P3.1. The status of the lines are detected on P3.2 and P3.3.

2.4 The program store

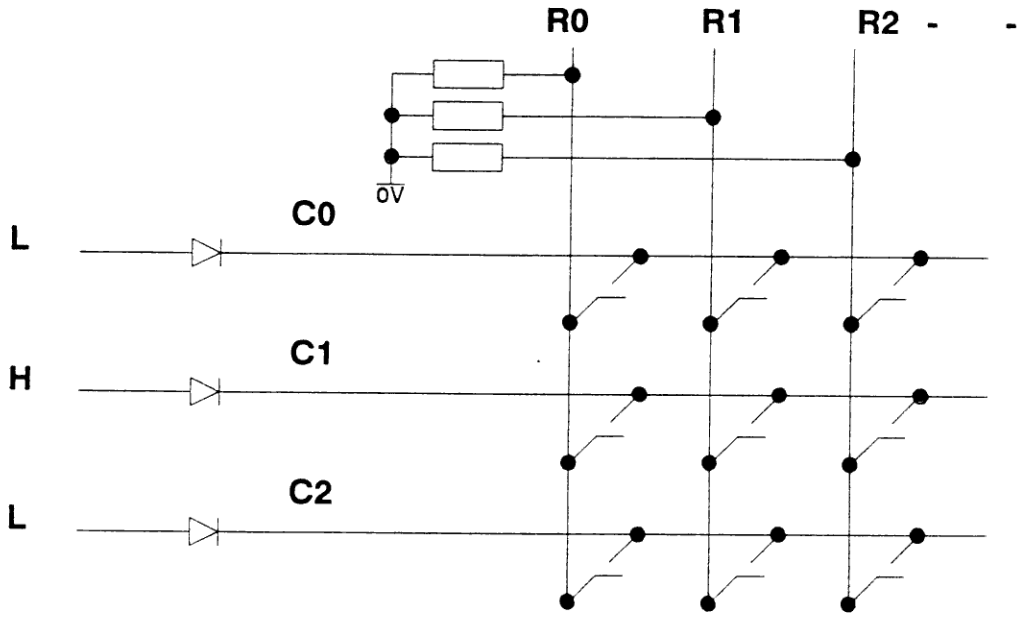
A Intel27C64 (8Kx8) PROM is used for program store. It should be noted that the A13 input (pin26) actually is a NC (No Connection). The A13 line from the CPU is connected to this pin in order to allow use of 27128 PROM`s.

2.5 Scan-line selection

A 74HCT4514 (U2) 4-to-16 line decoder is used to drive one - and only one - scan line high at a time. The following command sequence is used to read all key-switches connected to one scan-line:

```
MOVX @R0,A      (Move content of A to external RAM)
NOP             (No operation)
MOV  A,P1       (Move content of port 1 to A)
```

No address decoding is performed, so the content of R0 in the first instruction is don`t care. R1 could also have been used. The content of A specifies the the scan-line. A=00001001 selects a high level on Q9 (pin 17) and thereby enables scan-line 6 (C6). The 4 most significant bits of A are don`t care.
A NOP is inserted to ensure the correct setteling time. The status of the switches are read on P1. A high level indicates key activation. Diodes are provided at the output of the decoder in order to prevent short circuiting in case of multiple key activations. Figur 1 is illustrating the scanning system.



Figur 1

2.6 Auxillary output register

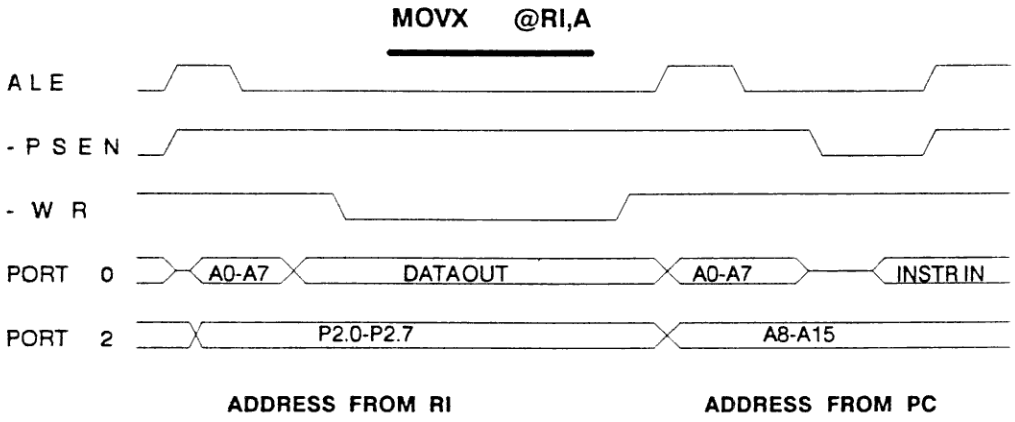
A 74HCT573 (U7) is used as a auxillary output register. Monitor contrast and brightness, key-click generation and indicator LED`s are controlled by this register. The content of P2 is loaded into the aux. register during a write to external RAM. Normally the P2 pins are used as address lines. During a write to external RAM (with 8 bit address) the P2 content is however available on the address lines.

Example: The following code sequence will turn on the LED in keyswitch no.38 (Num Lock).

```
CLR P2.1
MOVX @R0,A
```

The first instruction alters P2 content and the second loads P2 content into the aux. register. The content of R0 and A are don`t care.

Figur 2 illustrates the function of the register loading.



Figur 2

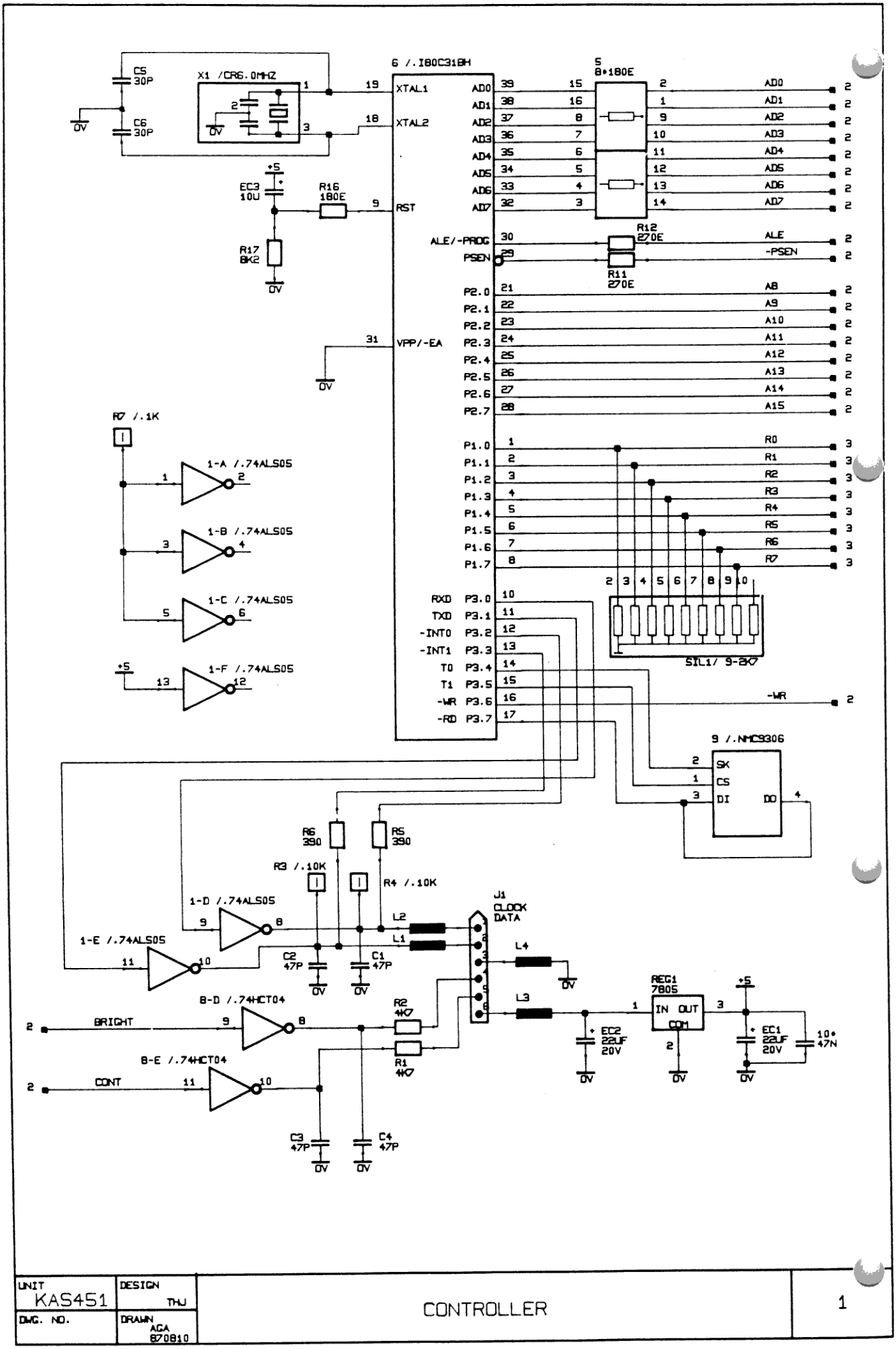
2.7 Key-click generation

The click-device (BEEP) is a piezo electric device. The component is electrically equvivalent with a capacitor. The configuration around the click device, allows for a 10V voltage swing in order to get an appropriate click-volume.

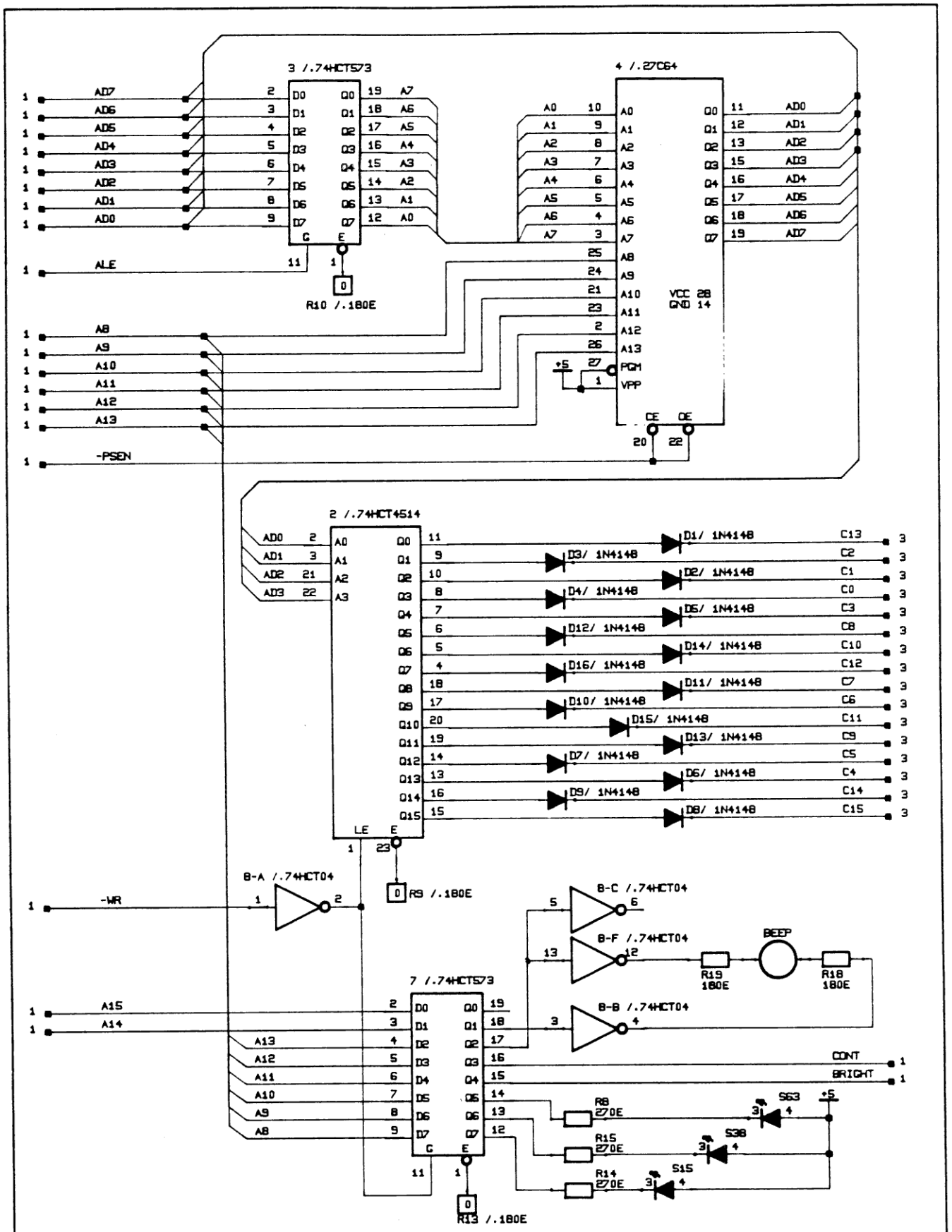
2.8 Monitor control

Two Pulse Width Modulated (PWM) signals controls the monitor contrast and brightness. The two signals are generated in the aux. register. A further description of the monitor control signals are given in reference 1.

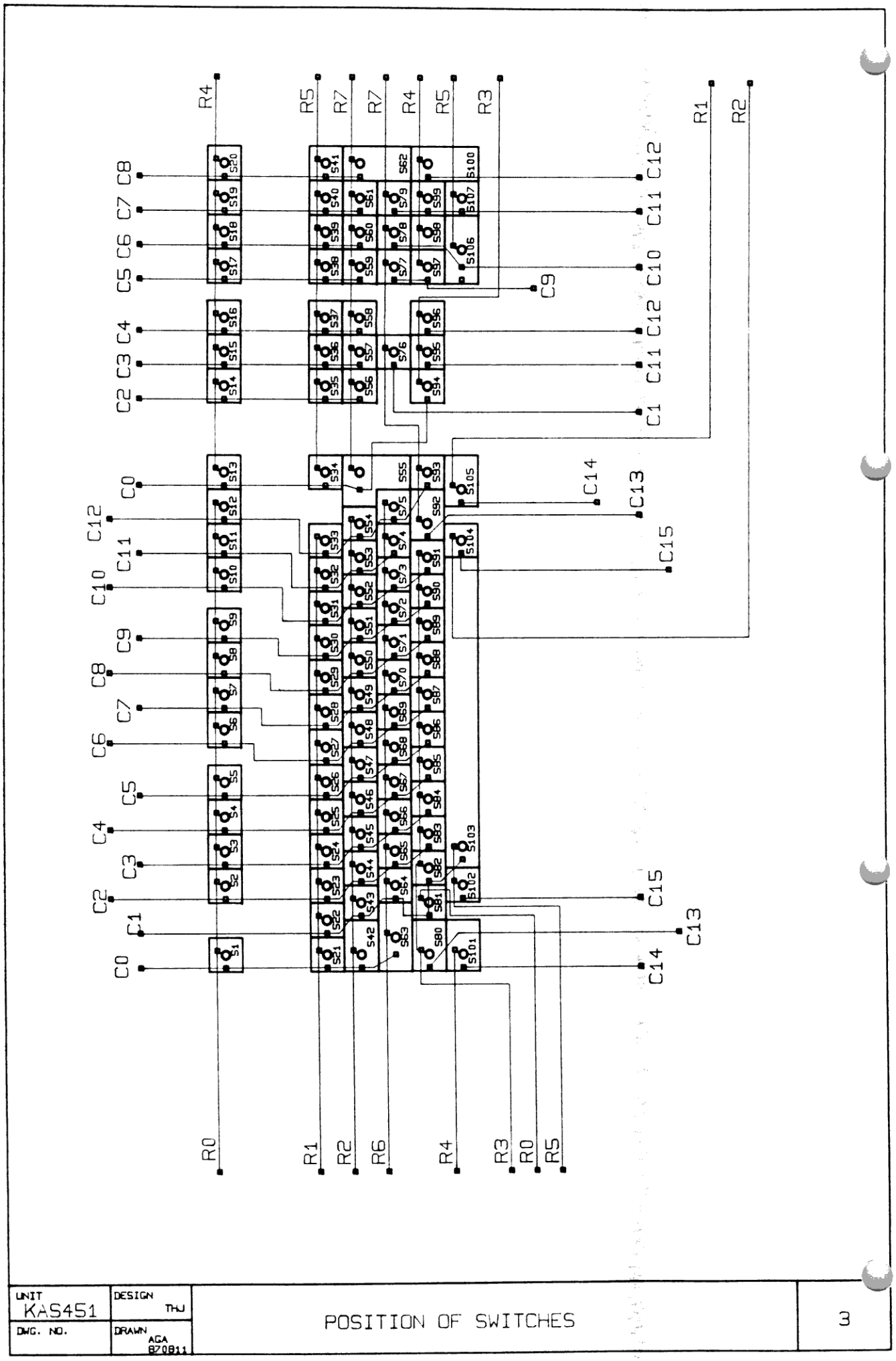
3. Logic diagram



UNIT	DESIGN		
KAS451	THJ	CONTROLLER	1
DWG. NO.	DRAWN AGA 870810		



UNIT KAS451	DESIGN THJ	DRIVER	2
DWG. NO.	DRAWN AGA 870810		



UNIT	DESIGN		
KAS451	THJ	POSITION OF SWITCHES	3
DWG. NO.	DRAWN AGA 870811		

4. Intel 80c31 Datasheet

PRELIMINARY

80C51BH/80C51BH-1/80C51BH-2 CHMOS SINGLE-CHIP 8-BIT MICROCOMPUTER WITH FACTORY MASK-PROGRAMMABLE ROM

80C31BH/80C31BH-1/80C31BH-2 CHMOS SINGLE-CHIP 8-BIT CONTROL-ORIENTED CPU WITH RAM AND I/O

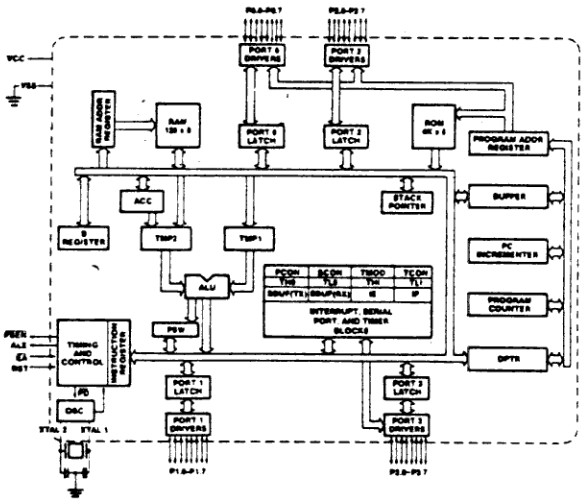
80C51BH/80C31BH—3.5 to 12 MHz, V_{CC} = 5V ±20%
80C51BH-1/80C31BH-1—3.5 to 16 MHz, V_{CC} = 5V ±20%
80C51BH-2/80C31BH-2—0.5 to 12 MHz, V_{CC} = 5V ±20%

- **Power Control Modes**
- **128 x 8-Bit RAM**
- **32 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **64K Program Memory Space**
- **High Performance CHMOS Process**
- **Boolean Processor**
- **5 Interrupt Sources**
- **Programmable Serial Port**
- **64K Data Memory Space**

The MCS®-51 CHMOS products are fabricated on Intel's CHMOS III process and are functionally compatible with the standard MCS-51 HMOS and EPROM products. CHMOS III is a technology which combines the high speed and density characteristics of HMOS with the low power attributes of CHMOS. This combination expands the effectiveness of the powerful MCS-51 architecture and instruction set.

Like the MCS-51 HMOS versions, the MCS-51 CHMOS products have the following features: 4K byte of ROM (80C51BH/80C51BH-1/80C51BH-2 only); 128 bytes of RAM; 32 I/O lines; two 16-bit timer/counters; a five-source two-level interrupt structure; a full duplex serial port; and on-chip oscillator and clock circuitry. In addition, the MCS-51 CHMOS products have two software selectable modes of reduced activity for further power reduction—Idle and Power Down.

The Idle mode freezes the CPU while allowing the RAM, timer/counters serial port and interrupt system to continue functioning. The Power Down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.



270064-1

Figure 1. Block Diagram

November 1986
Order Number: 270064-004

IDLE MODE

In the Idle mode, the CPU puts itself to sleep while all the on chip peripherals stay active. The instruction that invokes the Idle mode is the last instruction executed in the normal operating mode before Idle mode is activated. The content of CPU, the on chip RAM, and all the Special Function Registers remain intact during this mode. The Idle mode can be terminated either by any enabled interrupt, at which time the process is picked up at the interrupt service routine and continued, or by a hardware reset which starts the processor the same as a power on reset.

POWER DOWN MODE

In the Power Down mode the oscillator is stopped, and the instruction that invokes Power Down is the last instruction executed. Only the contents of the on chip RAM is preserved. A hardware reset is the only way to terminate Power Down.

The control bits for the reduced power modes are in the Special Function Register PCON.

NOTE:
For more detailed information on these reduced power modes refer to Application Note AP-252, "Designing with the 80C51BH".

PIN DESCRIPTIONS

V_{CC}

Supply voltage during normal, Idle, and Power Down operations.

V_{SS}

Circuit ground.

Port 0

Port 0 is an 8-bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 80C51BH. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. Port 1 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.

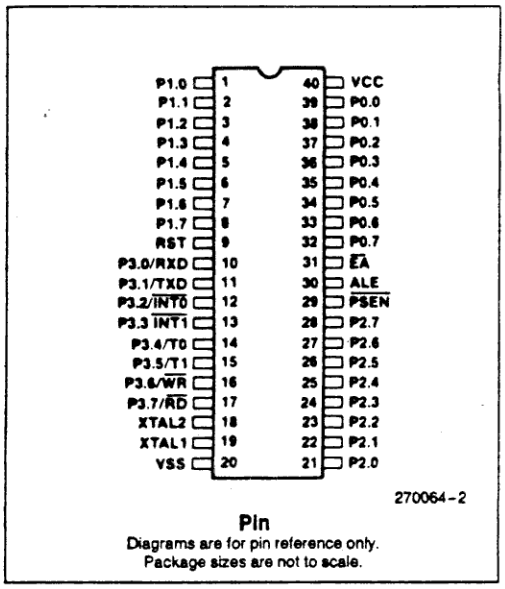
Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. Port 2 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external Program Memory and during

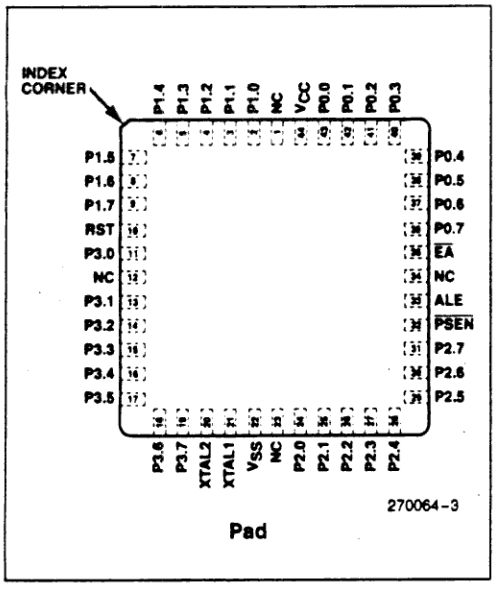
Table 1. Status of the external pins during Idle and Power Down modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data



Pin

Diagrams are for pin reference only.
Package sizes are not to scale.



Pad

Figure 2. Connection Diagrams

accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external Data Memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. Port 3 pins that have 1s written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the pullups.

Port 3 also serves the functions of varjous special features of the MCS-51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. An internal diffused resistor to V_{SS} permits Power-On reset using only an external capacitor to V_{CC}.

ALE

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$

Program Store Enable is the read strobe to external Program Memory.

When the 80C51BH is executing code from external Program Memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory. $\overline{PSEN}$ is not activated during fetches from internal program memory.

$\overline{EA}$

External Access enable. $\overline{EA}$ must be strapped to V_{SS} in order to enable the device to fetch code from external Program Memory locations 0000H to 0FFFH. If $\overline{EA}$ is strapped to V_{CC} the device executes from internal Program Memory unless the program counter contains an address greater than 0FFFH.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock generator circuits.

XTAL2

Output from the inverting oscillator amplifier.

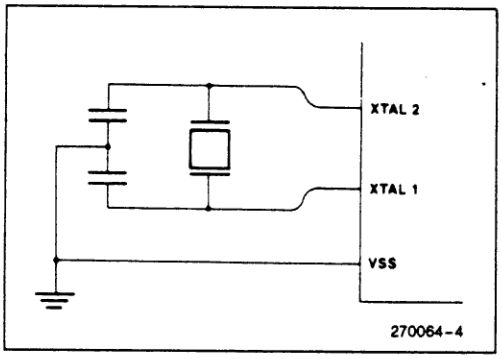


Figure 3. Crystal Oscillator

Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. More detailed information concerning the use of the on-chip oscillator is available in Application Note AP-155, "Oscillator for Microcontrollers".

To drive the device from an external clock source, XTAL1 should be driven, while XTAL2 is left unconnected, as shown in Figure 4. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

Design Considerations

- At power on, the voltage on V_{CC} and RST must come up at the same time for a proper start-up.
- Before entering the Power Down mode the contents of the Carry Bit and B.7 must be equal.
- When the Idle mode is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

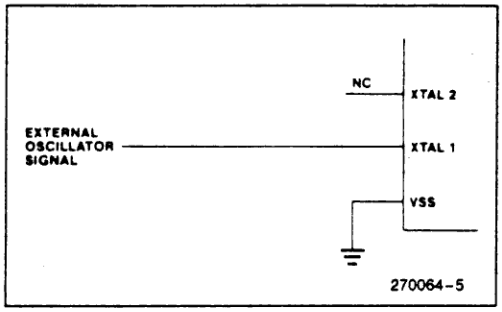


Figure 4. External Drive Configuration

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias .....0°C to 70°C
Storage Temperature .....−65°C to +150°C
Voltage on any Pin to V_{SS} .....−0.5V to V_{CC} +0.5V
Voltage on V_{CC} to V_{SS} .....−0.5V to 6.5V
Power Dissipation.....1.0W*

*This value is based on the maximum allowable die temperature and the thermal resistance of the package.

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ±20%; V_{SS} = 0V)

Symbol	Parameter	Min	Typ(3)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (Except $\overline{EA}$)	−0.5		0.2 V_{CC} −0.1	V	
V_{IL1}	Input Low Voltage ($\overline{EA}$)	−0.5		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)			0.45	V	I_{OL} = 1.6 mA (1)
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)			0.45	V	I_{OL} = 3.2 mA (1)
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	2.4			V	I_{OH} = −60 µA V_{CC} = 5V ±10%
		0.9 V_{CC}			V	I_{OH} = −10 µA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4			V	I_{OH} = −400 µA V_{CC} = 5V ±10%
		0.9 V_{CC}			V	I_{OH} = −40 µA (2)
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)			−50	µA	V_{IN} = 0.45V
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3)			−650	µA	V_{IN} = 2V
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)			±10	µA	0.45 < V_{IN} < V_{CC}
RRST	Reset Pulldown Resistor	50		150	KΩ	
CIO	Pin Capacitance			10	pF	Test Freq = 1 MHz, T_A = 25°C
I_{CC}	Power Supply Current:					
	Active Mode, 12 MHz (4)		11	20	mA	
	Idle Mode, 12 MHz (4)		1.7	5	mA	(5)
	Power Down Mode		5	50	µA	

NOTES:
1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OLS} of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing.
3. "Typicals" are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temperature, 5V.
4. ICCMAX at other frequencies is given by
   Active Mode: ICCMAX = 1.47 × FREQ + 2.35
   Idle Mode: ICCMAX = 0.33 × FREQ + 1.05
where FREQ is the external oscillator frequency in MHz. ICCMAX is given in mA. See Figure 5.
5. See Figures 6 through 9 for ICC test conditions.

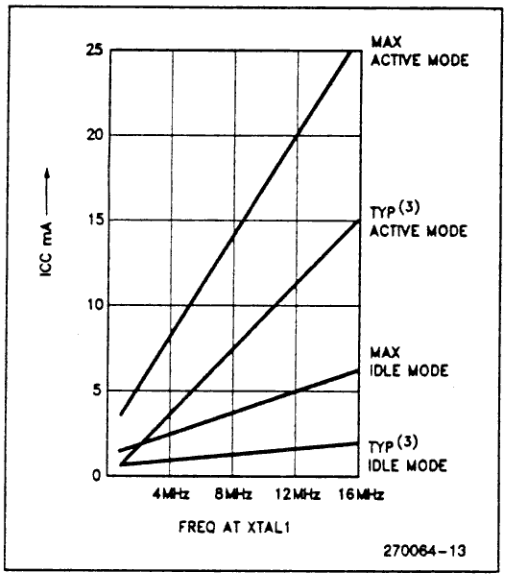


Figure 5. I_{CC} vs. Frequency. Valid only within frequency specifications of the device under test.

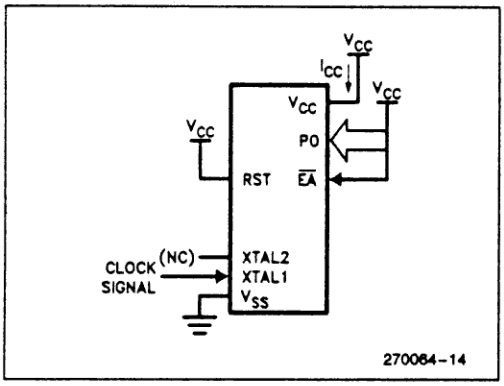


Figure 6. I_{CC} Test Condition, Active Mode. All other pins are disconnected.

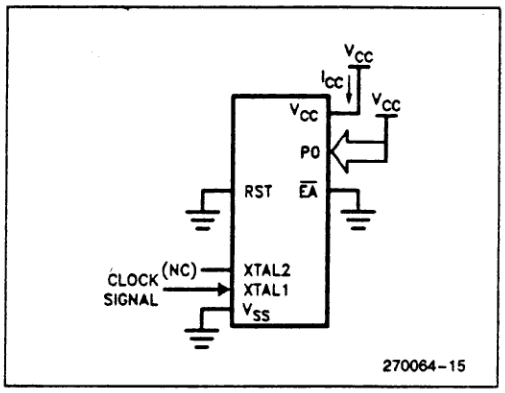


Figure 7. I_{CC} Test Condition, Idle Mode. All other pins are disconnected.

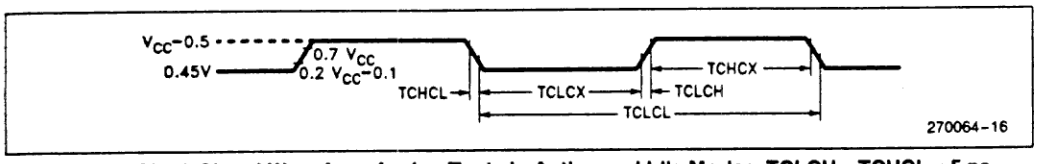


Figure 8. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes. TCLCH = TCHCL = 5 ns.

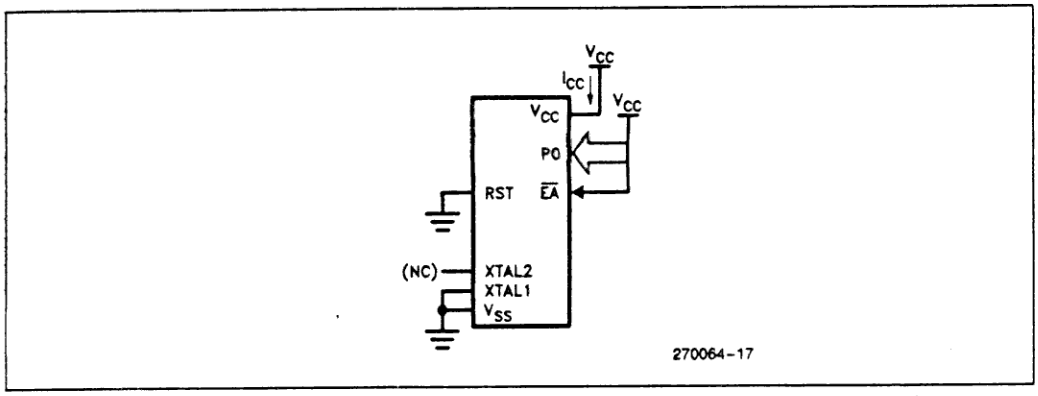


Figure 9. I_{CC} Test Condition, Power Down Mode. All other pins are disconnected.

EXPLANATION OF THE AC SYMBOLS

Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

A: Address.
C: Clock.
D: Input data.
H: Logic level HIGH.
I: Instruction (program memory contents).
L: Logic level LOW, or ALE.
P: $\overline{PSEN}$.
Q: Output data.
R: $\overline{RD}$ signal.
T: Time.
V: Valid.
W: $\overline{WR}$ signal.
X: No longer a valid logic level.
Z: Float.

EXAMPLE:

TAVLL = Time for Address Valid to ALE Low.
TLLPL = Time for ALE Low to $\overline{PSEN}$ Low.

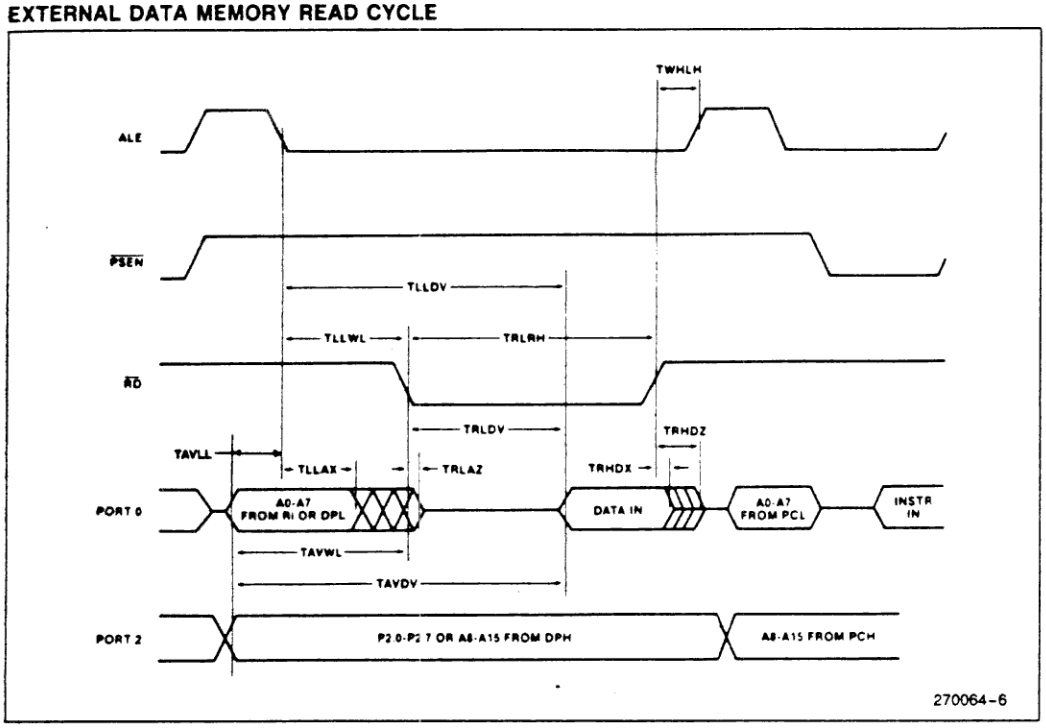
A.C. CHARACTERISTICS

(T_A = 0°C to 70°C, V_{CC} = 5V ±20%, V_{SS} = 0V, Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

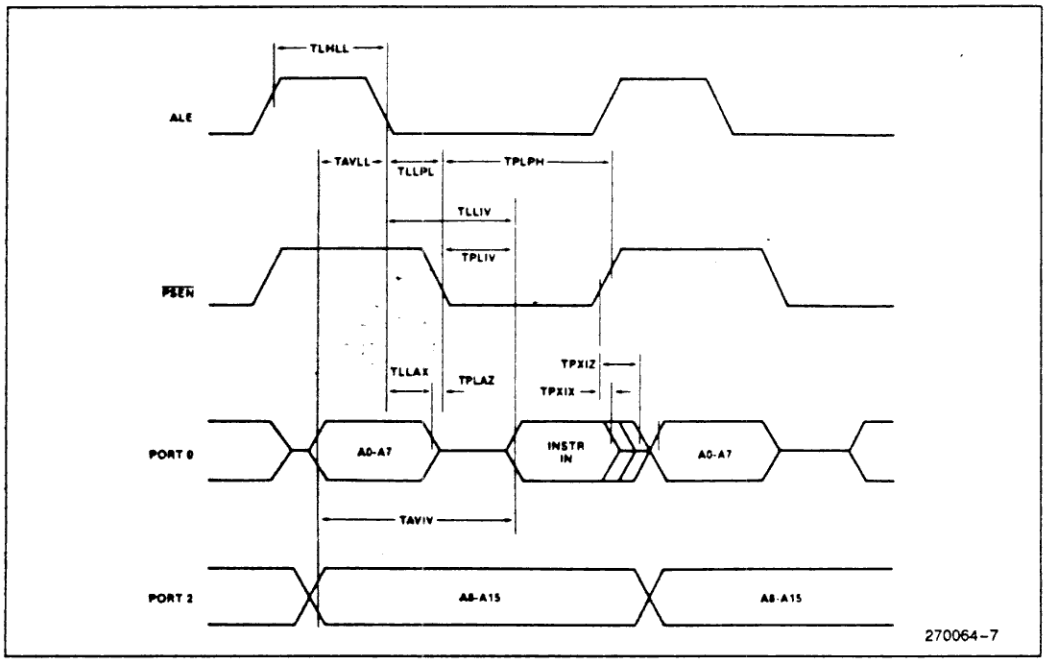
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency 80C51BH/80C31BH 80C51BH-1/80C31BH-1 80C51BH-2/80C31BH-2			 3.5 3.5 0.5	 12 16 12	MHz
TLHLL	ALE Pulse Width	127		2TCLCL − 40		ns
TAVLL	Address Valid to ALE Low	28		TCLCL − 55		ns
TLLAX	Address Hold After ALE Low	48		TCLCL − 35		ns
TLLIV	ALE Low to Valid Instr In		234		4TCLCL − 100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	43		TCLCL − 40		ns
TPLPH	$\overline{PSEN}$ Pulse Width	205		3TCLCL − 45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr In		145		3TCLCL − 105	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instr Float After $\overline{PSEN}$		59		TCLCL − 25	ns
TAVIV	Address to Valid Instr In		312		5TCLCL − 105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL − 100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL − 100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		252		5TCLCL − 165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		97		2TCLCL − 70	ns
TLLDV	ALE Low to Valid Data In		517		8TCLCL − 150	ns
TAVDV	Address to Valid Data In		585		9TCLCL − 165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	3TCLCL − 50	3TCLCL + 50	ns
TAVWL	Address Valid to $\overline{RD}$ or $\overline{WR}$ Low	203		4TCLCL − 130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	23		TCLCL − 60		ns
TWHQX	Data Hold After $\overline{WR}$	33		TCLCL − 50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	TCLCL − 40	TCLCL + 40	ns

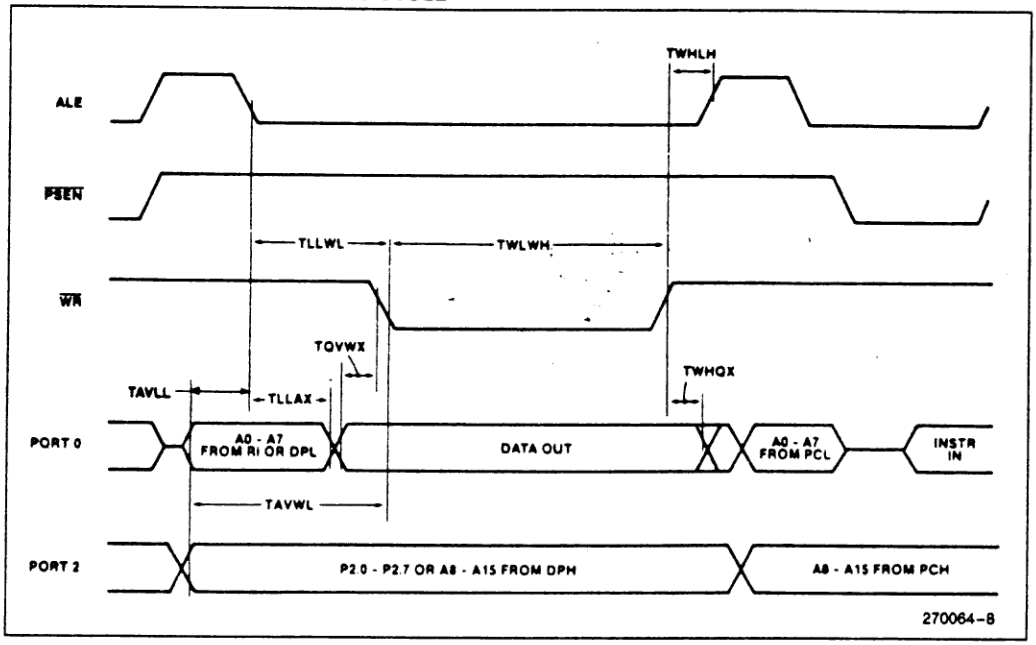
EXTERNAL DATA MEMORY READ CYCLE

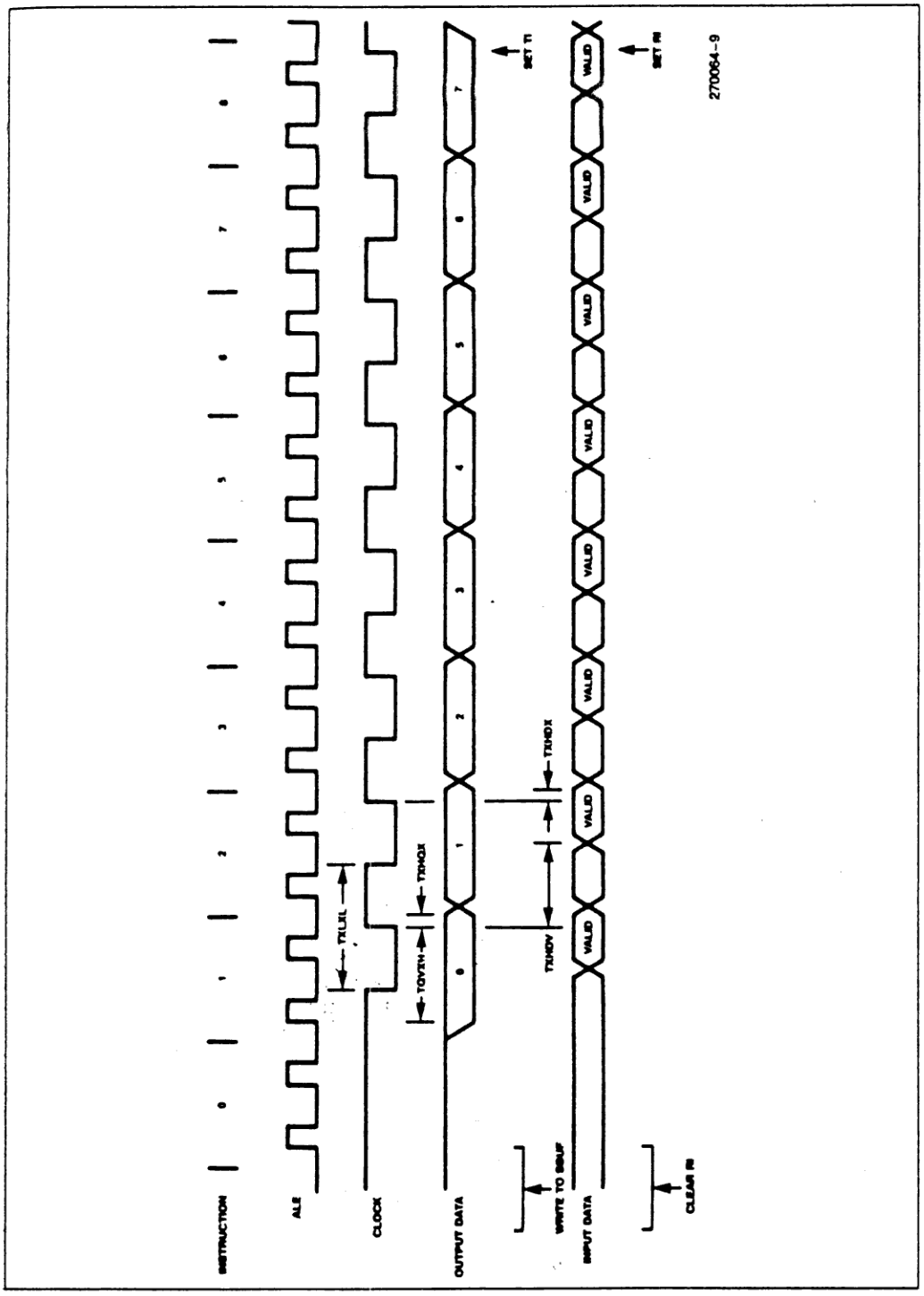


EXTERNAL PROGRAM MEMORY READ CYCLE



EXTERNAL DATA MEMORY WRITE CYCLE





Shift Register Mode Timing Waveforms

8-47

EXTERNAL CLOCK DRIVE

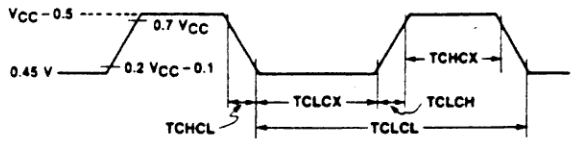
Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency 80C51BH/80C31BH 80C51BH-1/80C31BH-1 80C51BH-2/80C31BH-2	 3.5 3.5 0.5	 12 16 12	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

SERIAL TIMING—SHIFT REGISTER MODE

Test Conditions: T_A = 0°C to 70°C; V_{CC} = 5V ±20%; V_{SS} = 0V; Load Capacitance = 80 pF

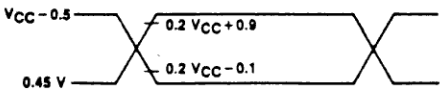
Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL − 133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL − 117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL − 133	ns

EXTERNAL CLOCK DRIVE WAVEFORM



270064-10

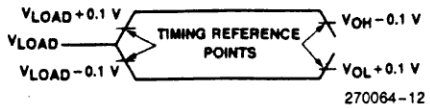
AC TESTING INPUT, OUTPUT WAVEFORMS



270064-11

AC Inputs during testing are driven at V_{CC} − 0.5 for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at V_{IH} min. for a logic "1" and V_{IL} max. for a logic "0".

FLOAT WAVEFORMS



270064-12

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

5. NMC9306 Datasheet

NMC9306

National Semiconductor Corporation

NMC9306 256-Bit Serial Electrically Erasable Programmable Memory (5V Only)

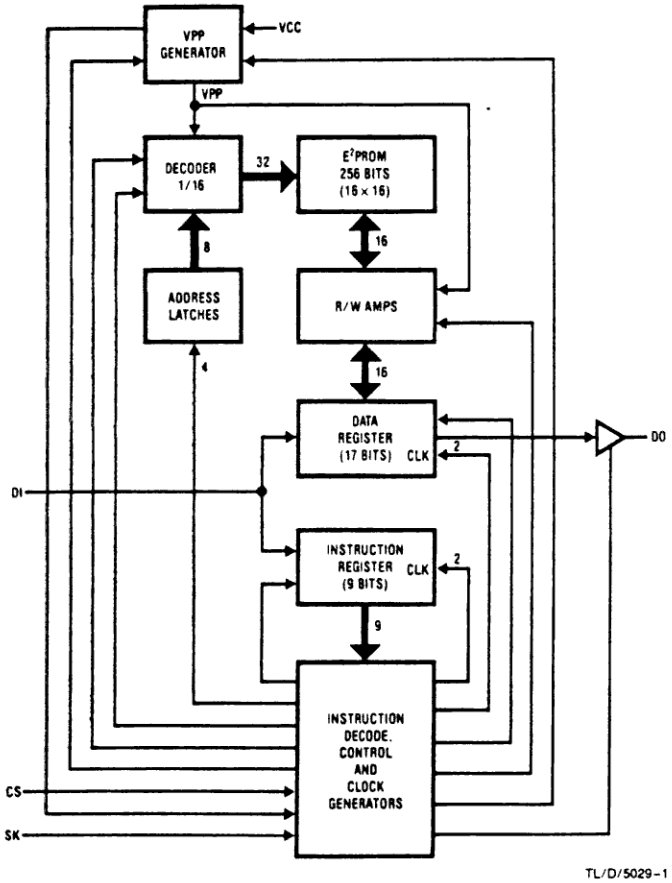
General Description

The NMC9306 is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E²PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306 has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

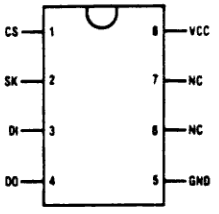
- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16×16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams



TL/D/5029–1

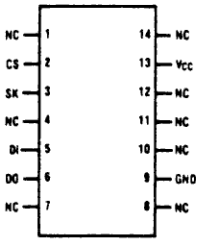
Dual-In-Line Package



TL/D/5029–10

Top View
Order Number NMC9306N
See NS Package Number N08E

SO Package



TL/D/5029–2

Top View
Order Number NMC9306M
See NS Package Number M14B

Note: Contact factory for S08 availability.

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground

Absolute Maximum Ratings

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature	
NMC9306/COP494	0°C to +70°C
Ambient Storage Temperature	
with Data Retention	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Electrical Characteristics 0°C ≤ TA ≤ 70°C, V_{CC} = 5V ± 10% unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage (V_{CC})		4.5		5.5	V
Operating Current (I_{CC1})	V_{CC} = 5.5V, CS = 1			10	mA
Standby Current (I_{CC2})	V_{CC} = 5.5V, CS = 0			3	mA
Input Voltage Levels					
V_{IL}		−0.1		0.8	V
V_{IH}		2.0		V_{CC} + 1	V
Output Voltage Levels					
V_{OL}	I_{OL} = 2.1 mA			0.4	V
V_{OH}	I_{OH} = −400 μA	2.4			V
Input Leakage Current	V_{IN} = 5.5V			10	μA
Output Leakage Current	V_{OUT} = 5.5V, CS = 0			10	μA
SK Frequency		0		250	kHz
SK HIGH TIME t_{SKH} (Note 2)		1			μs
SK LOW TIME t_{SKL} (Note 2)		1			μs
Input Set-Up and Hold Times					
CS t_{CSS}		0.2			μs
t_{CSH}		0			μs
DI t_{DIS}		0.4			μs
t_{DIH}		0.4			μs
Output Delay	CL = 100 pF				
DO t_{PD1}	V_{OL} = 0.8V, V_{OH} = 2.0V			2	μs
t_{PD0}	V_{IL} = 0.45V, V_{IH} = 2.40V			2	μs
Erase/Write Pulse Width ($t_{E/W}$) (Note 1)		10		30	ms
CS Low Time (t_{CS}) (Note 3)		1			μs

Note 1: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Note 2: The SK frequency spec. specifies a minimum SK clock period of 4 μs, therefore in an SK clock cycle, t_{SKH} + t_{SKL} must be greater than or equal to 4 μs. e.g. if t_{SKL} = 1μs then the minimum t_{SKH} = 3 μs in order to meet the SK frequency specification.

Note 3: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10xx	A3A2A1A0		Read register A3A2A1A0
WRITE	1	01xx	A3A2A1A0	D15−D0	Write register A3A2A1A0
ERASE	1	11xx	A3A2A1A0		Erase register A3A2A1A0
EWEN	1	0011	xxxx		Erase/write enable
EWDS	1	0000	xxxx		Erase/write disable
ERAL	1	0010	xxxx		Erase all registers
WRAL	1	0001	xxxx	D15−D0	Write all registers

NMC9306/COP494 has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

Functional Description

The NMC9306/COP494 is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Seven 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, four bits as an op code, and four bits of address. SK clock cycle is necessary after CS equals logical "1" before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (V_{CC}). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. after a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE (Note 4)

Like most E²PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE (Note 4)

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

CHIP ERASE (Note 4)

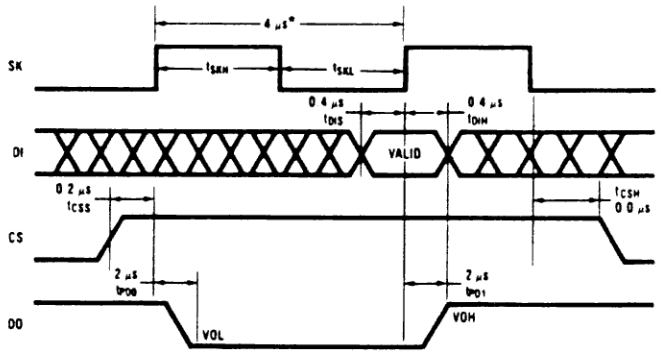
Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

CHIP WRITE (Note 4)

All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 4: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the Erase/Write pulse width ($t_{E/W}$).

Timing Diagrams

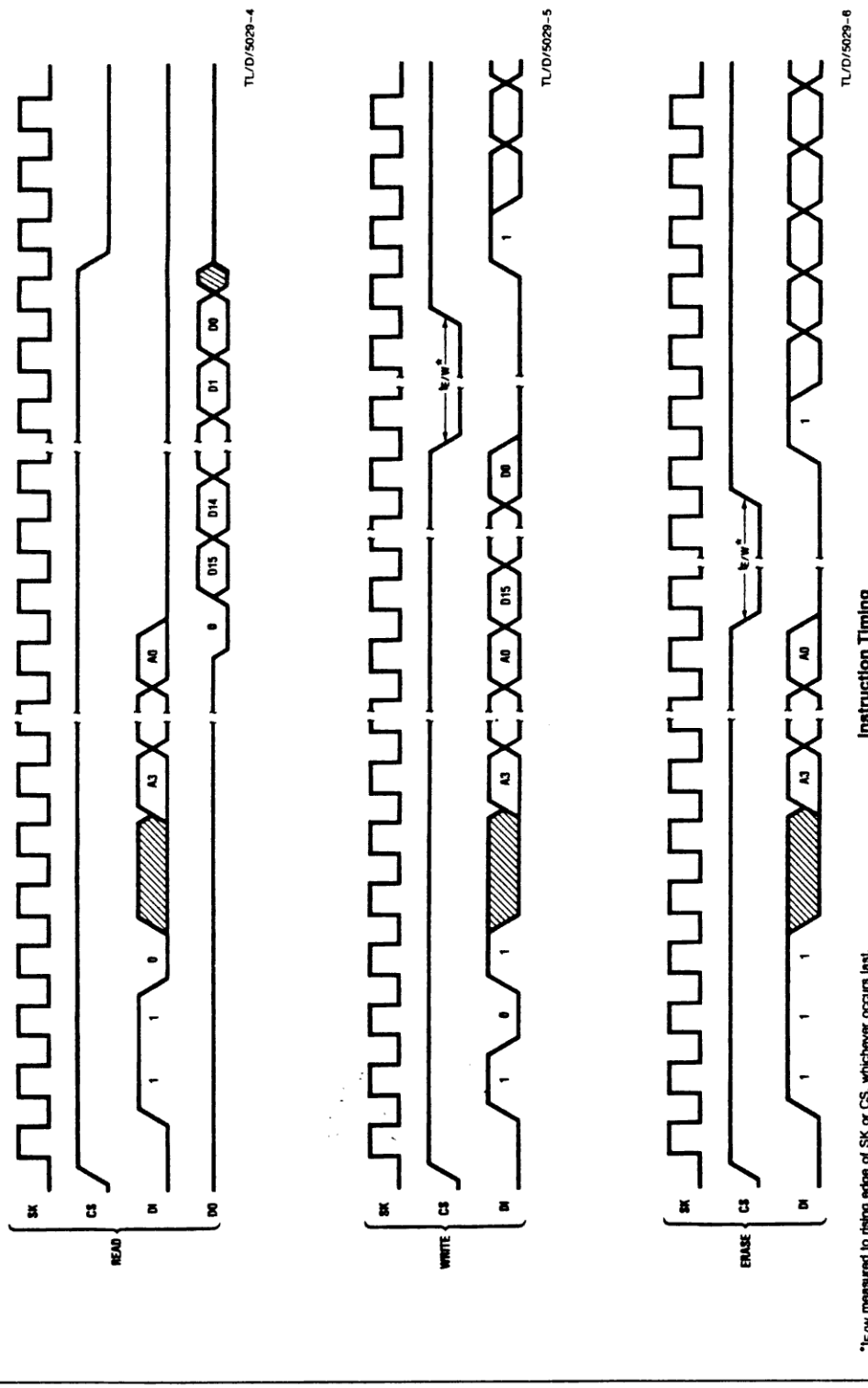


TL/D/5029-3

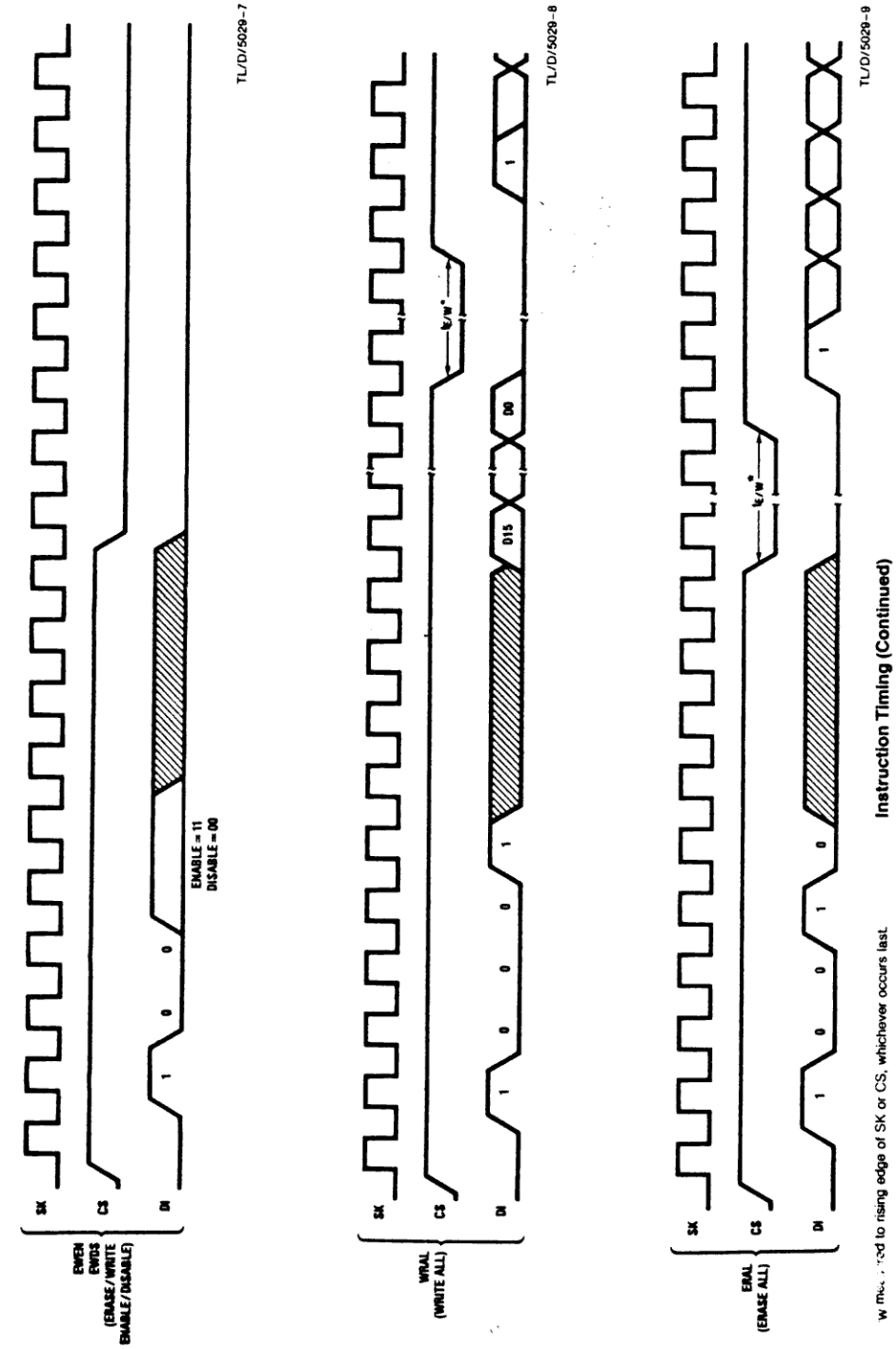
*This is the minimum SK period

Synchronous Data Timing

Timing Diagrams (Continued)



Timing Diagrams (Continued)



w ma[illegible]d to rising edge of SK or CS, whichever occurs last.

Instruction Timing (Continued)