RC900

MEM451 2M Memory module

Hardware reference manual

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RC Computer

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Abstract:
This paper contains a hardware description of the MEM451 memory module. The MEM451 provides 2 Megabytes of system memory for the RC900 series.

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1. GENERAL INFORMATION

1.1 Introduction

The MEM451 is a 2 Mega byte memory module intended for use in the RC900 series.

The memory is organized in two banks each containing 256 K words 32 bits wide plus 4 parity bits.

The two banks share data and address lines but have separate control lines (RAS, CAS and WE).

The address- and control- lines are buffered to groups of memory chips, whereas the databus connects the memory chips directly with the plug.

This manual describes the MEM451 board in three major sections. The first section gives a short description and specification of the board. The second section contains a functional description. The third section is devoted to the detailled hardware description with circuit- logic- and timing-diagrams.

1.2 Specifications

1.2.1 Performance specifications

capacity	: 2097152 bytes of 9 bit (8 + parity)		
organisation	: 2 banks of 262144 words		
word length	: 32 bits + 4 parity bits		
page size	: 2048 bytes		
access time	: read from idle bank	: 110 nsec.	
	: read from selected page		
	page hit	: 60 nsec.	
	page miss	: 205 nsec.	
cycle time	: page hit	: 120 nsec.	
	page miss	: 220 nsec.	
capacity	: 32 Kbytes.		
wordlength	: 16 bits.		
access time	: Depends on the programmed System bus speed.		

1.2.2 Environmental Specifications

Operating temperature	: 0 to 40 degrees C.
Relative Humidity	: 20% to 80% (non condensing).
Altitude	: 0 to 6,000 feet.

1.2.3 Physical Specification

Width	: 142 mm
Length	: 213 mm
Hight	: 14 mm
Weight	: 350 gram

The dimensions are excluding the mounting.

1.2.4 Power Specification

Power consumption

Dissipation	: 5 W max.
Vcc	: +5V +/- 5% (2.5A max.)

2 FUNCTIONAL DESCRIPTION

2.1 DRAM operation

The memory is equipped with 72 chips 256K by 1 bit Dynamic Random Access Memory.

The 262144 bits are stored in 262144 small capacitors each charged to a high or a low voltage representing the bit value. With each capacitor is attached a transistor being the gate to the charge. The transistor-capacitor pairs are organized in 512 rows with 512 pairs in each. All transistors in a row are turned on and off at the same time gating the charge of each capacitor to one of 512 bus lines transferring the charges to an array of 512 amplifier/latches constituting the row register. These bus lines with the associated amplifier/latch are called coloums. Access to one of the 512 coloums from the singlebit input and output on the chip is done via a 512/1 multiplexer.

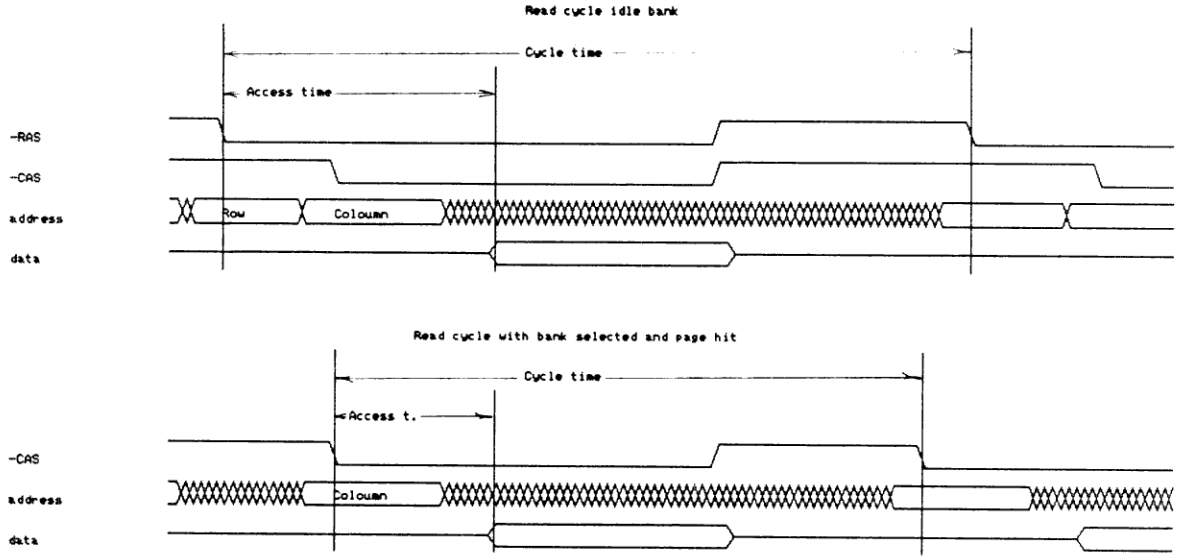


fig. 1 DRAM timing

The memoty chip is controlled with three signals: RAS (Row Address Select), CAS (Coloumn Address Select) and WE (Write Enable). The 18 bit address is multiplexed into the chip in two portions of 9 bits each. An access to a bit starts with applying the 9 most significant address bits to the address bus and activate RAS. This will latch the row address into a row address register and select the corresponding row and load it into the row register. Next step is to shift the remaining 9 address bits onto the address bus and activate CAS. This controls the coloumn multiplexer to select one bit in the row register to be gated to the output or to be modified according to the data input (if WE is active). As long time RAS is kept active it is possible to access bits in the row register only specifying the coloumn address, WE and reactivating CAS. When RAS is deactivated, the current contents of the row register (modified or unmodified) is stored back into the row capacitors (this is reffered to in the databooks as the precharge time), then the row is "closed", and when CAS is released as well the chip is deselected. The capacitors being not totally "tight" require refresh evry 4 millisecond. This is done for a row each time it is accessed. Row access without bit access (without CAS being activated) are cdalled refresh cycles.

3. TECHNICAL DESCRIPTION

3.1 Introduction

This section gives the detailled description of the CPU451 circuit board until the chip level. For the technical description of the used chips please refer to the manufacturer manuals in the appendices.

3.2 Block diagram

Figure 2 shows a detailled blockdiagram of the CPU451 intended to provide an overwiev of the board. The blocks correspond to physical and or logical entities and are labeled with numbers referring to the logic diagrams in section 3.3, where the exact electrical connections are drawn. Two or more numbers separated with commas indicates that the block is spread over more diagrams.

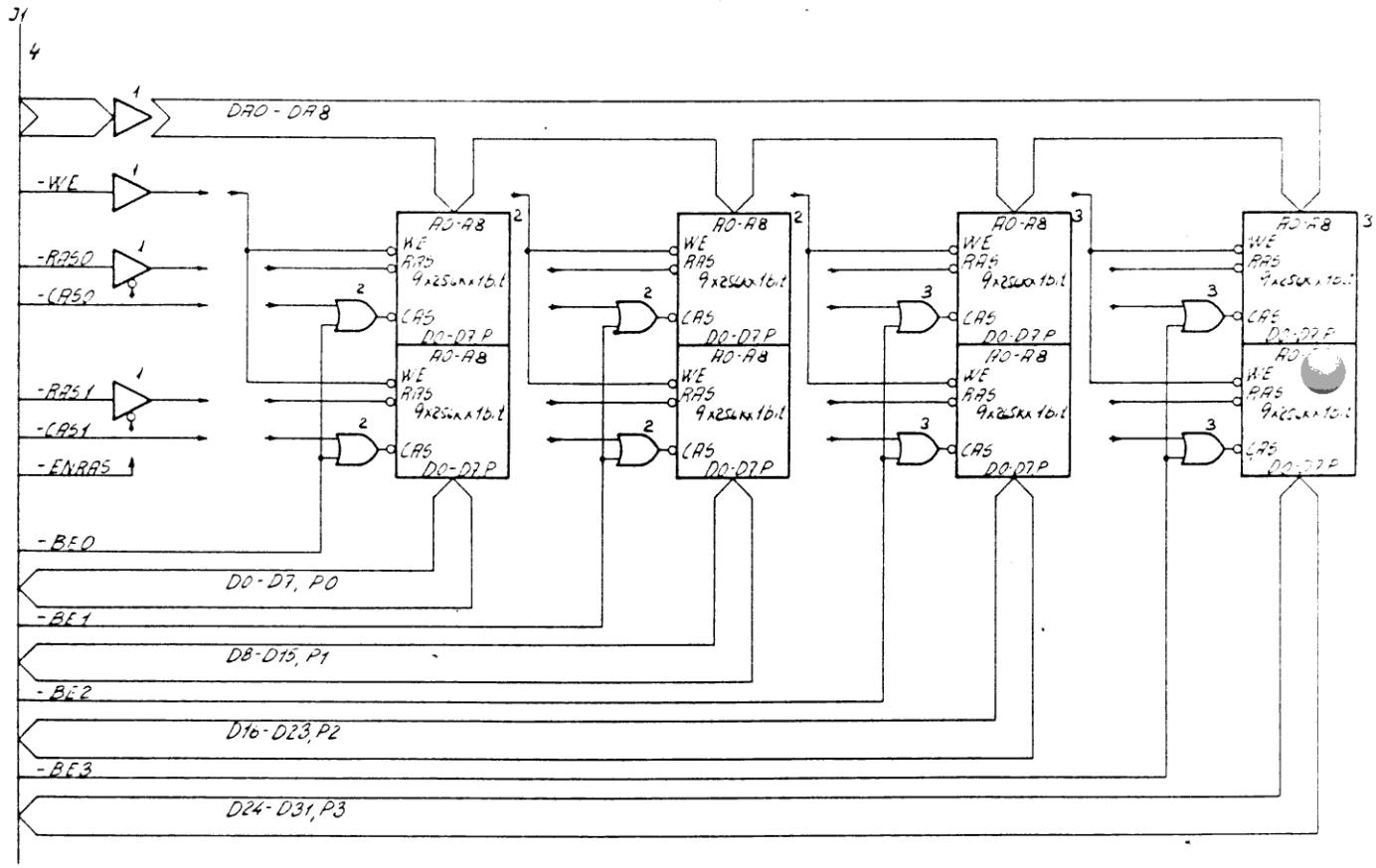


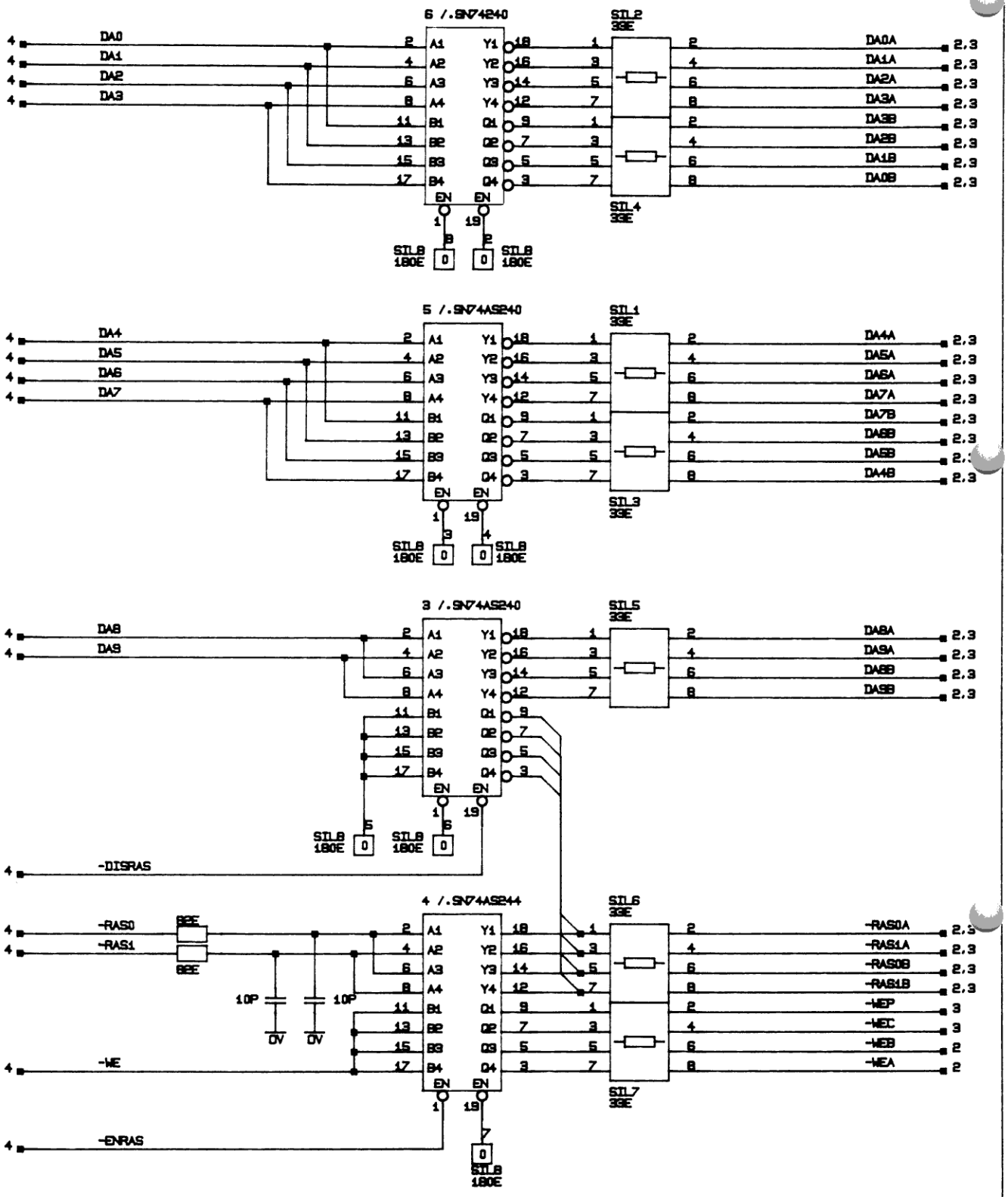
Fig. 2 detailled block diagram.

3.3 Logic diagrams

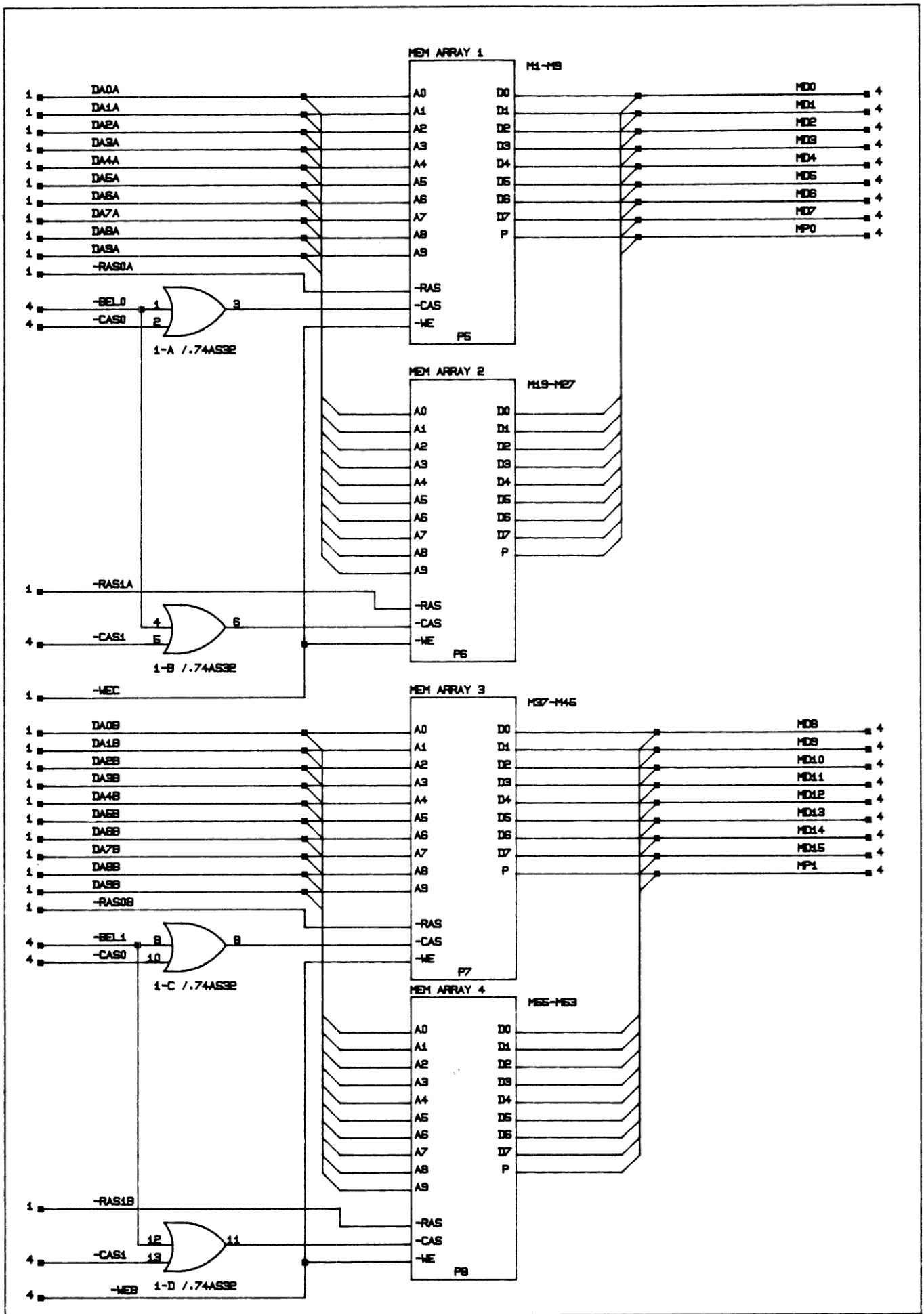
This section contains the logic diagrams of the MEM451.

The pages of the diagram are numbered separately from the pagination of the manual. These dragram numbers are used on the diagrams for source and destination references, where signals enter or leave a page.

The position code found above each component on the diagrams coresponds to the position number marked on the printed circuit board.



UNIT	DESIGN		
MEM451	PKA	BUFFERE	1
DWG. NO.	DRAWN LIJ 880202		



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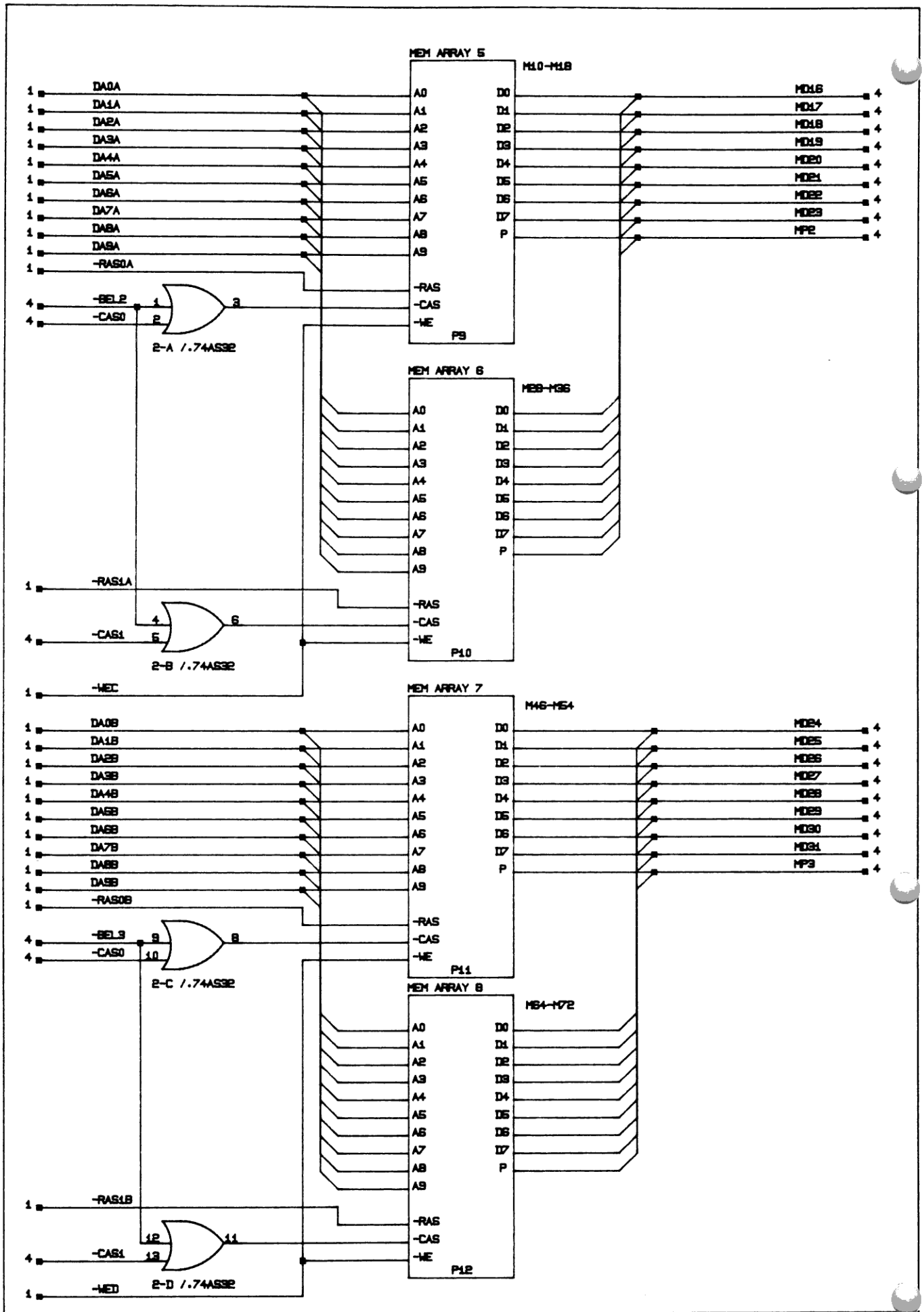
MEM451	PKA	MEMORY BYTE 0,1	2
DWG. NO.	DRAWN LTJ 880202		



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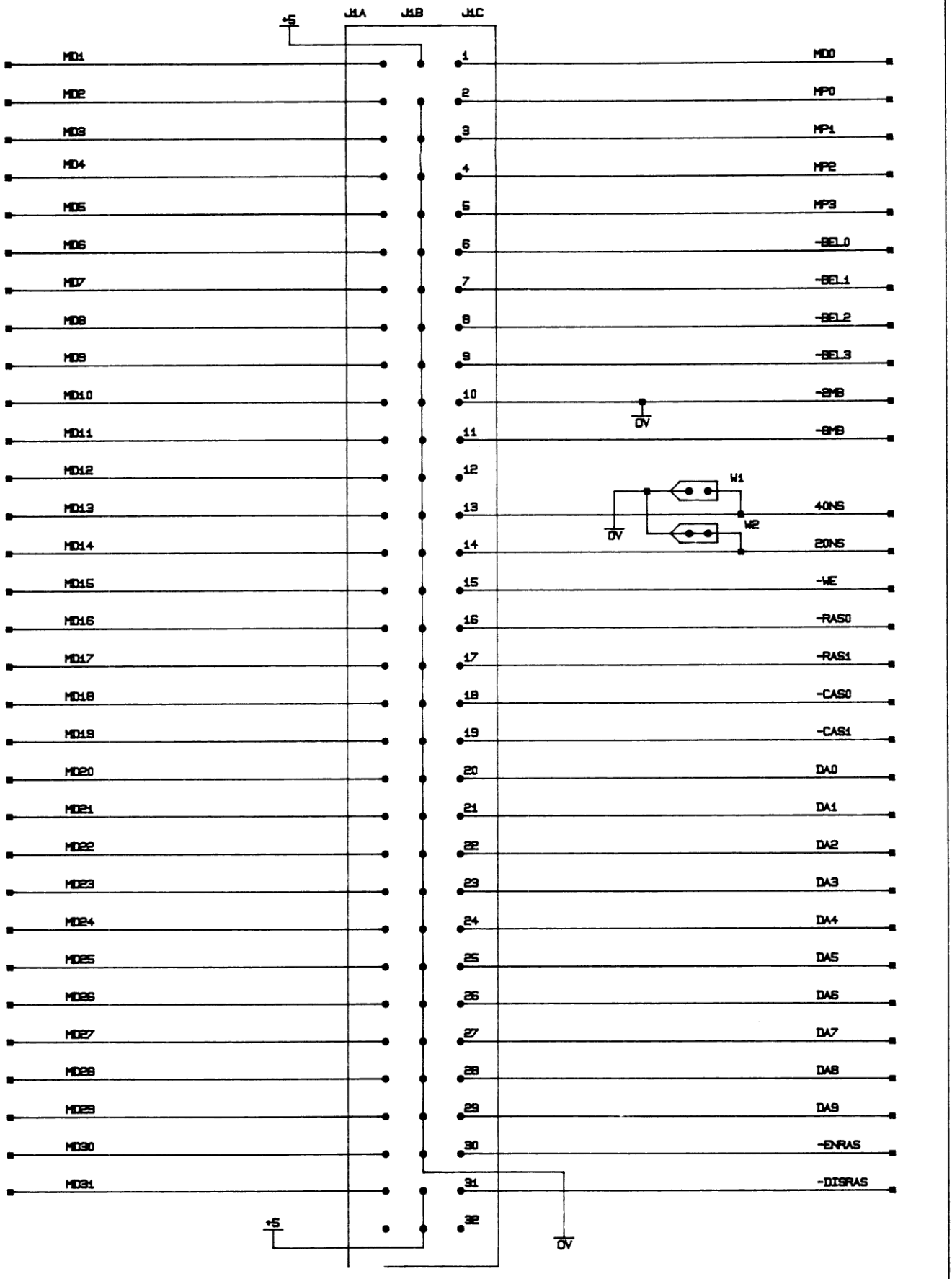
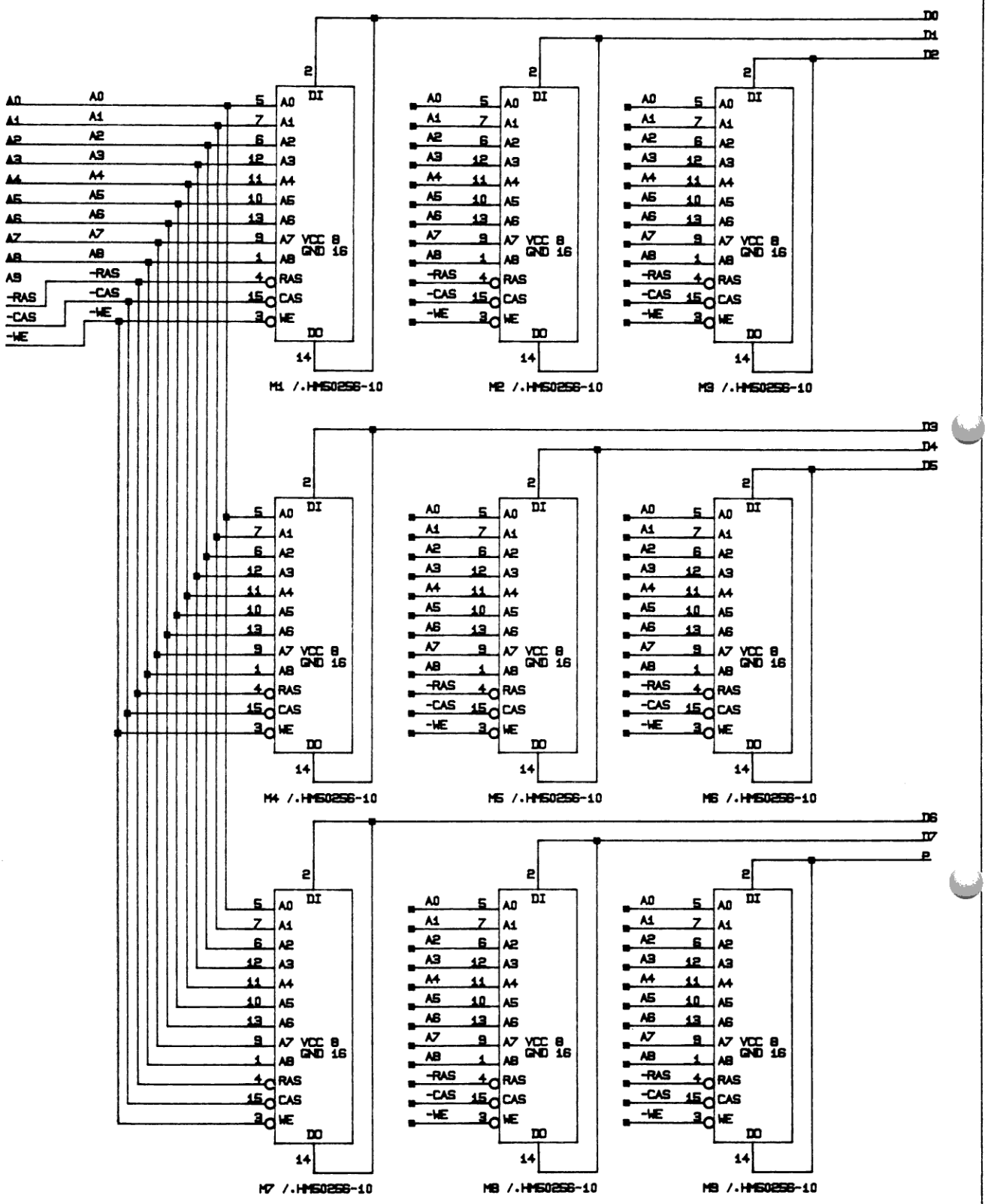


UNIT MEM451	DESIGN PKA	CONNECTOR	4
DWG. NO.	DRAWN AGA 870813		



UNIT MEM451	DESIGN PKA	256K*9 BIT MEM ARRAY	5
DWG. NO.	DRAWN AGA 870813		

3.4 Assembly drawing