RC900

LAN452 LAN Adapter 10Mbps

Hardware reference manual

PN: 99111112

PN: 99200389

RC Computer

Keywords:
LAN452 LAN adapter, Local Area Network, Ethernet, Cheapernet

Abstract:
This paper contains a hardware description of the LAN adapter LAN452. The LAN452 is provided with an IBM-AT bus interface and can be connected to an Ethernet Transceiver or a Cheapernet Transceiver.

Date:
July 1987

Author:
Jens K. Andreassen

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1. INTRODUCTION

This manual describes the LAN452 board. The LAN452 board is an intelligent Ethernet adapter with IBM-AT I/O bus interface.

The LAN452 is provided with a 80186 CPU and 512 k bytes of local RAM. The LAN452 can become a master on the AT I/O bus, thus providing the board with the facility to read from and write to the system board memory. The Intel 82586 LAN controller is used on the board.

The manual is divided into basically three sections. The first section contains a short description and a short specification of the board. The second section contains a description which is relevant for the programmer of the board. The last section contains a detailed hardware description of the board.

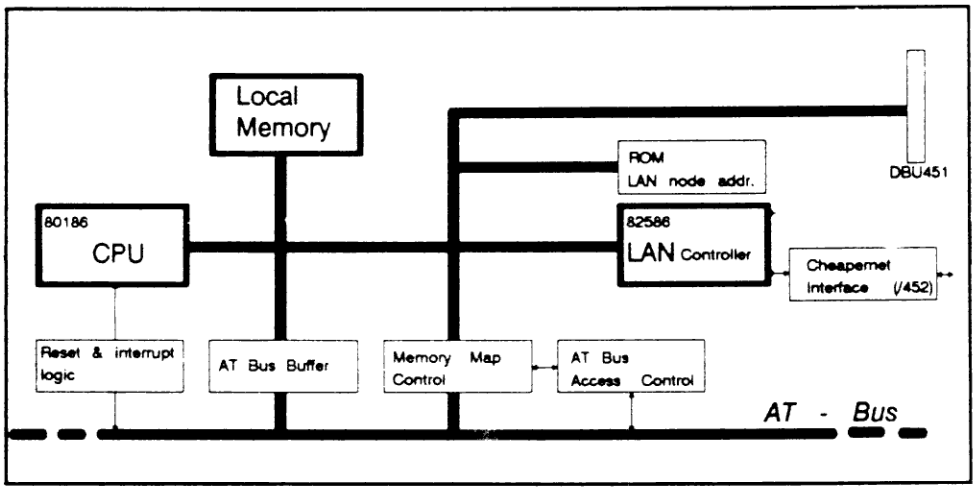


Fig. 1. Block diagram of LAN452

2. GENERAL INFORMATION

2.1 Short Description

Fig. 1 shows a block diagram of the LAN452 board.

The CPU is an 8MHz INTEL 80186 processor, see (1). The CPU is integrated with

- 3 programmable timer.
- 5 interrupt input lines and an interrupt controller.
- Programmable waitstate generator.
- 2 programmable DMA controllers.
- 7 programmable I/O chip select lines.

The INTEL 82586 LAN controller is a coprocessor operating parallel with the 80186 CPU, see (1). The 82586 can access the Local Memory and communicates with the 80186 through this memory. The 82586 interfaces the RcMikronet interface logic.

The Local Memory consists of 512 Kbyte DRAM. No PROM is available on the LAN452 board. The Local Memory can only be accessed by the 80186 CPU and the 82586 LAN controller.

The upper most 128K byte of the 80186 address space is mapped onto the system memory through the AT bus. The Boot Memory Map Register controlles the mapping of the upper most 64 Kbyte. The Buffer Memory Map Register controlles the mapping of the next 64 Kbyte.

After reset the 80186 starts executing code in the system memory in the Boot Memory address space.

Through a 15 pol D-connector the LAN452 board can be connected with a Ethernet transceiver or Cheapernet transceiver.

A 48 pol EURO connector on the LAN452 provides for testing the board with a Debug Board, DBU451, see (4). The DBU451 is provided with EPROMs. After reset, which may be generated by the DBU451 board, the 80186 may execute the code placed in these EPROMs.

Through the Reset and Interrupt Logic the LAN452 can generate an interrupt on the system board and the System Board can interrupt the LAN452 board. The system board can also generate a reset signal to the LAN452 board.

A maximum of two LAN boards (LAN451 and/or LAN452) can be mounted in the AT slots.

2.2 Specification

2.2.1 Performance Specifications

80186 CPU clock	: 8 MHz
Data Bus Size	: 16 bits
EPROM	: none
On board RAM capacity (Local Memory)	: 512 Kbyte expandable to 896 Kbyte by mounting extra DRAM devices.
Off board Memory	:
Boot Memory	: 64 Kbytes of the system memory.
Buffer Memory	: 64 Kbyte of the system memory.
Memory address range	:
Local Memory	: 00000H-7FFFFH
Boot Memory	: F0000H-FFFFFH
Buffer Memory	: E0000H-EFFFFH

2.2.2 Environmental Specifications

Operating Temperature	: $0^{o}C$ - $40^{o}C$.
Relative Humidity	: 20% - 80% (non condensing).

2.2.3 Physical Specification

Width	: 121.80 mm
Length	: 333.25 mm
Height	: 20 mm

2.2.4 Power Specification

Power Dissipation	: 7.5 W max.
Vcc	: +5V +/- 5% (1.5 A max.)
Vdd	: +12V +/- 10% (0.5 A max.)

2.3 Installation

The LAN452 board can be plugged into any of the AT-I/O slot. If a LAN452 or another LAN452 is allready plugged into one of the slots a jumper must be mounted on one of the LAN452 or LAN452 boards. The jumper must be mounted at the position named S1 on the board. A maximum of two LAN boards can be installed in the AT slots.

3. PROGRAMMING INFORMATION

This chapter contains the necessary programming information of the LAN452 board.

3.1 The 80186 CPU

The LAN board is based on an INTEL80186 single chip CPU. The reader should read (1) and (2) in conjunction with reading this chapter. Abbreviations from (1) and (2) are used in this chapter.

An 16 MHz x-tal is connected to the on-chip clock generator providing the board with an 8 MHz clock signal. This means that an local memory access takes 0.5 us, i.e. with no wait states. The R0-2 fields in the 80186 UMCS, LMCS and MMCS register should be programmed to 000B. This means external generated RDY signal and no internal generated wait states.

3.1.1 Interrupts to the 80186 CPU

The 80186 interrupt controller are connected to the following interrupt sources:

80186 interrupt pin	Interrupt source
INT0	82586 LAN controller interrupt
INT1	Interrupt from the system board
INT2	Transmit interrupt from Debug Board
INT3	not used
NMI	Receive interrupt from Debug Board

The interrupt vectors must be generated by the 80186 interrupt controller it self.

3.1.2 The 80186 DMA controller

The two integrated DMA controllers on the 80186 chip is not used on the LAN452 board.

3.1.3 The 80186 Timers

the 80186 has three integrated timers. Timer 0 is dedicated as a DRAM refresh request source. The timer must be programmed to generate a signal with a duty cycle of appr. 50% and a cycle time of max. 14 usec. The DRAM on the board then performs a CAS before RAS refresh cycle every 14 usec. An initial pause of 200 usec is required after power-up. After the pause a minimum of 8x256 refresh cycles are required. Timer 1 and timer 2 is not used.

3.1.4 The 80186 peripheral chip select

The 80186 has seven integrated peripheral chip select lines. On the LAN452 board these lines are used in the following way:

80186 chip select pin	I/O Address range	Desitnation
!PCS0	! PBA-PBA+7FH	! 82586 LAN Controller
!	!	! Channel attention
!PCS1	! PBA+80H -	! Chip select to Debug
!	! PBA+0FFH	! Board
!PCS2	! PBA+100H -	! Acknowledges an interrupt
!	! PBA+17FH	! from the system board
!PCS3	! PBA+180H -	! Generates an interrupt
!	! PBA+1FFH	! on the AT-bus (IRQ10)
!PCS4	! PBA+200H -	! Ethernet ROM or Memory
!	! PBA+27FH	! Map Register load
!PCS5	! PBA+280H -	! 82586 LAN Controller
!	! PBA+2FFH	! Hardware reset
!PCS6	! PBA+300H -	! Turns on the LAN Led
!	! PBA+37FH	! in appr. 0.5 sec.

PBA is the I/O offset address contained in the 80186 PACS register.

The MS bit in the 80186 MPCS register must be loaded with 0H, i.e. peripherals are mapped into I/O space.

the R2-R0 bits in the PACS register should be programmed with 101B, i.e. one wait state in I/O cycles for PCS0-PCS3 asserted.

The R2-R0 bits in the MPCS register should be programmed with 111B, i.e. three wait states for PCS4-PCS6 asserted.

The PCS0 signal generates a channel attention signal for the 82586 LAN Controller.

PCS1 is asserted when reading from or writing to the Debug Board.

An I/O cycle asserting the PCS3 signal will generate an interrupt on the AT-bus (IRQ10). This interrupt signal may be deasserted by the system board, see chapter 3.4.3.

The 80186 can deassert an interrupt from the AT-bus (INT1, see chapter 3.1.1) by executing an I/O write cycle with PCS2 asserted.

The Ethernet address is placed in a 256x4 bit PROM. the 80186 can read the contents of the PROM by executing I/O read instructions with PCS4 asserted. The contents of the PROM is loaded onto the lowermost four bits of the databus. The addressbits A1-A4 selects four bits word on the PROM. i.e. the address range is 00H to 1EH. Note that the address bit A0 is not used.

Writing to an I/O address with PCS4 asserted will load the Memory Map Register, see chapter 3.2.2. The Memory Map Register is loaded with the contents of the lowermost eight data bits.

When PCS6 is asserted a LED will light in appr. 0.5 sec. indicating that the LAN452 is receiving a frame from the coax or is transmitting one. The LED is placed in the front of the computer.

3.2 LAN452 Memory

The 80186 1 Mbyte address space on the LAN452 is divided into three parts:

1. Local Memory Address space: 00000H-7FFFFH
2. Buffer Memory Address space: E0000H-EFFFFH
3. BOOT Memory Address space: F0000H-FFFFFH.

Fig. 2 shows the organization of the 1 Mbyte memory space.

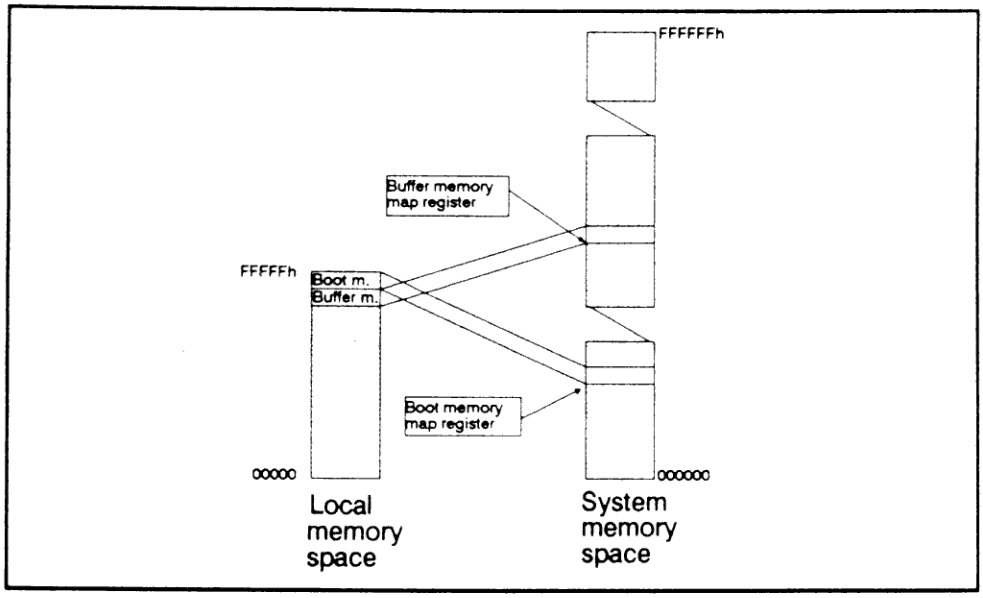


Fig. 2. LAN memory organization and system memory map.

3.2.1 Local Memory

The Local Memory consists of 512 Kbytes of on-board DRAM. 256Kx4bit DRAM chips are used. This memory can only be accessed by the 80186 CPU and the 82586 LAN Controller. By mounting extra four memory chips up to 896 Kbytes of Local Memory is available on the LAN452 board. The memory chips are fast enough to avoid insertion of wait states.

The Local Memory is automatically refreshed by the 80186 Timer 0 see chapter 3.1.3.

3.2.2 Buffer Memory

The Buffer Memory is a memory map of the 80186 CPU address space onto the system memory. When accessing this memory the LAN452 board becomes a master of the AT-bus. Due to the arbitration a number of wait states are inserted.

The memory mapping of the buffer memory is controlled by the 80186 CPU through the Buffer Memory Map register. This register is loaded by the 80186 CPU by writing to the I/O device with PCS4 asserted, see section 3.1.4. The Memory Map register contains the following bit:

7	6	5	4	3	2	1	0
LA23	LA22	LA21	LA20	LA19	LA18	LA17	SA16

The MSB of the register controlles the most significant address bit, LA23, on the AT-bus. The LSB of the register controlles the AT-address signal SA16, when accessing the Buffer Memory. the Buffer Memory Map register selects a 64 Kbyte boundary in the system memory.

By using the 80186 LOCK prefix it is possible to move or compare a block of data to or from the system memory. Normally a device on the AT-bus is not allowed to be a master on the AT-bus in more than 14 usec. The floppy must be serviced within 14 usec. on a DMA request. If the LAN452 is master, by using the REP/LOCK prefix in more than 14 usec. data to or from the floppy controller may be lost and data in the system memory may be lost due to lack of refresh. Though, the system memory will be refreshed by the LAN452 board if one of the following instructions are used:

REP LOCK MOVS or
REP LOCK CMPS.

3.2.3 Boot Memory

The upper 64 Kbytes of the 80186 memory space is normally of the Read Only Memory type. In this manual this is called the Boot Memory. This memory space is mapped into the system memory through the Boot Memory Map register. The Boot Memory Map register is loaded by the system board by an I/O write cycle, see section 3.4.1.

The least significant byte on the AT data bus is loaded into the Boot Memory Map register. The Boot Memory Map register contains the following bits.

7	6	5	4	3	2	1	0
LA23	LA22	LA21	LA20	LA19	LA18	LA17	SA16

The MSB of the register controlles the most significant address signal, LA23, on the AT-bus. The LSB of the register controlles the least significant address signal, SA16, on the AT-bus. The Boot Memory Map register selects a 64 Kbyte boundary in the 16 Mbyte system memory.

3.3 LAN interface

The LAN interface consists of the 82586 LAN Controller (see (2)) and IC logic providing the LAN452 board with serial interface to the Ethernet Transceiver.

3.3.1 The 82586 LAN Controller

The 82586 LAN Controller can only access the Local Memory. Any addresses generated by the 82586 will be mapped into the Local Memory. When the 82586 is started with a Channel Attention (CA) the 82586 will start reading the Initialization Root in the address FFFF6H, which is mapped into the Local Memory address 7FFF6H.

The 82586 operates in the maximum mode. The 82586 SRDY/ARDY pin must be programmed to act as ARDY input.

3.4 IBM-AT Bus Interface

Some of the AT-interface characteristica are mentioned in section 3.2. This section contains information on how to select AT-I/O addresses. DMA channels and AT interrupt signals. The reader should also consult (3).

3.4.1 AT I/O addresses

Through the jumper S1 the I/O addresses is slected:

S1	I/O address space	
On	304H-307H	(the jumper is mounted)
Off	300H-303H	(the jumper is not mounted)

If two LAN boards (either LAN452 or LAN452) are mounted in the AT slots, one and only one of them must be configured with S1 in the off position.

The LAN452 will recognize four AT I/O addresses:

S1=on	S4=off	
304H	300H	Deassert the reset signal on the LAN452 board and load the Boot Memory MAP register.
305H	301H	Activate the reset signal on the LAN452.
306H	302H	Acknowledge from the system board on an interrupt from the LAN452.
307H	303H	Interrupt to the LAN452 CPU 80186.

3.4.2 AT DMA Channel Select

The LAN452 board uses the DMA channel 0 on the AT bus to become a Master on the AT bus. If two LAN452 boards or one LAN452 and one LAN452 are installed arbitration logic on the boards will select one of the boards to become Master if they request the bus at the same time.

3.4.3 AT interrupt

The LAN452 board can activate the IRQ10 interrupt signal on the AT bus. If two LAN boards are mounted in the AT slots they will both activate IRQ10.

3.5 Debug Board Interface

A debug board, DBU451, can be plugged into a 36 pin connector on the LAN board, providing the technician with debug facilities. The reader should consult (4) for further information.

4. TECHNICAL DESCRIPTION

4.1 Introduction

This chapter contains a detailed technical description of the LAN452 hardware. Section 4.2 gives a survey of the LAN452 board. Section 4.3 contains the electrical diagrams of the LAN452 and should be readen together with section 4.2. Section 4.4 contains description of the LAN452 PAL's and Ethernet ROM. Section 4.5 contains some relevant timing diagrams.

A description of the LSI components used is not given in this chapter. It is recommended that the reader consults the relevant data sheets (see chapter 5).

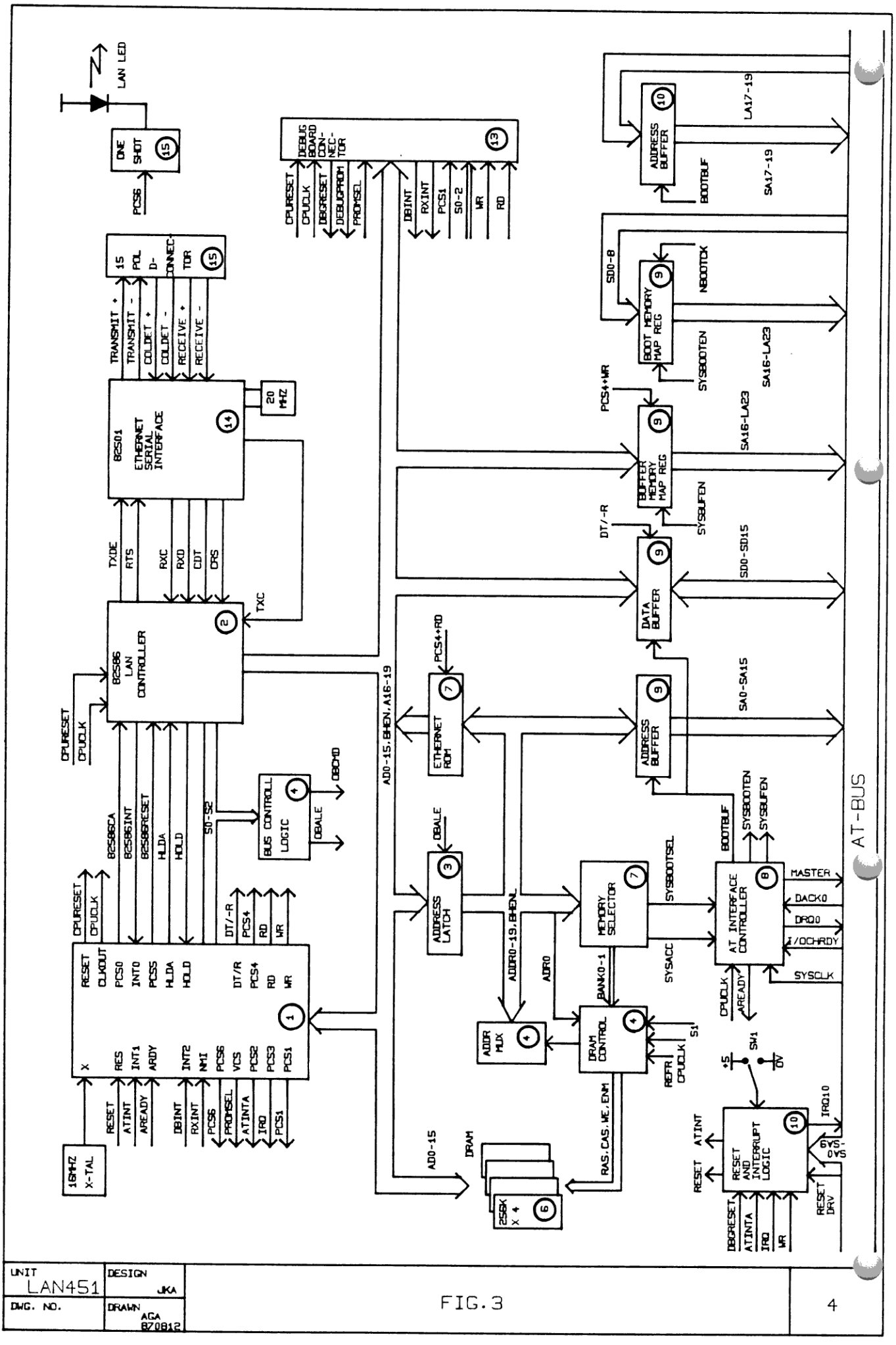
4.2 Short Technical description

Fig. 3 shows a more detailed block diagram of the LAN452 board. Some of the most important signal names are shown in fig. 3 and can be found in section 4.3. The numbers in circles refer to a diagram page number in section 4.3 where the group of logic can be found as electrical diagrams. In the rest of this section we refer to these diagram pages.

Diagram page 1 shows the 80186 CPU. The 80186 CPU are connected to provide ALE, WR and RD signals (no queue status data). A 16 MHz x-tal is connected to the 80186 providing the board with an 8 MHz CPU clock.

Diagram page 2 shows the 82586 LAN Controller. The 82586 is operating in the Maximum mode (MN/MX is low) providing the Bus Controll Logic (diagram page 4) with the S0 and S1 status signals when the 82586 access the Local Memory. A Ready input pin is also available in this mode.

The 82586 can be reset by the '82586RESET' signal or by the 'CPURESET' signal. The '82586RESET' signal is connected to the 80186 PCS5 output pin. The 'CPURESET' signal is a reset signal for the whole LAN452 board.



UNIT	DESIGN		
LAN451	JKA		
DWG. NO.	DRAWN AGA 870812	FIG.3	4

The 82586 is a co-processor and obtains the access to the Local Memory by activating the 'HOLD' signal from the 80186.

By the '82586CA' signal (channel attention) the 80186 CPU can initiate the 82586.

The 82586 may interrupt the 80186 by activating the '82586INT' signal.

Diagram page 3 shows the Address Latch.

Diagram page 4 contains three logic units:

- Bus Controll Logic
- DRAM Controller and
- DRAM Address Multiplexer.

The Bus Controll Logic generates the address latch enable signal 'OBALE' and an On Board Command signal for the Memory Selector and the DRAM Controller.

The DRAM Controller consists of a PAL16R6A device. the DRAM Controller generates controll signals to the DRAM devices:

- Row Address Strobe ('RAS0', 'RAS1')
- Column Address Strobe ('CAS')
- Write Enable ('WEHI', 'WELO')
- Enable Memory ('ENMEM0', 'ENMEM1')

Enable Memory is active when reading from the Local Memory.

On a request from the 80186 CPU timer0 ('REFR') the DRAM controller generates a 'CAS before RAS refresh' cycle to the DRAM devices. The DRAM devices contains an internal refresh counter. A refresh cycle can occur whenever the 80186 CPU or the 82586 are not accessing the Local Memory.

The DRAM Address Multiplexer generates the Row and Column addresses from the latched 16 addresses.

Diagram page 5 shows a Local Memory with 64Kx4bit DRAM devices. These devices is not mounted on the LAN452 board.

Diagram page 6 shows a Local Memory with 256Kx4bit DRAM devices. Only DRAM devices with even IC numbers are mounted providing the LAN452 board with 512 Kbyte Local Memory.

Diagram page 7 shows the Ethernet ROM and the Memory Selector. The Ethernet ROM contains 16 nibbles of which 12 of the nibbles constitutes the Ethernet address of this board. A nibble is 4 bit.

The PAL16L8A constitutes the Memory Selector and the function can be described with the following table:

HOLD*											
	-,DEBUG								-,SYS	-,SYSBOOT	
HLDA	-,OBCMD	PROM	A19	A18	A17	A16	-,BANK0	-,BANK1	ACC	SEL	
X	H	X	X	X	X	X	H	H	H	H	No access
L	L	X	0	X	X	X	L	H	H	H	80186 access
L	L	X	1	1	0	X	H	L	H	H	To Local Memory
L	L	X	1	1	1	0	H	H	L	H	80186 access to Buffer Memory
L	L	H	1	1	1	1	H	H	L	L	80186 access to Boot Memory
L	L	L	1	1	1	1	H	H	H	H	80186 access to Debug Board PROM
H	L	X	0	X	X	X	L	H	H	H	80286 access
H	L	X	1	X	X	X	L	H	H	H	to Local Memory

Notes: X indicates a dont care state
1 is equal to H (High) state
0 is equal to L (Low) state.

The 'SYSMENEN' enables two buffers, controlling the AT bus read and write signals, when the LAN452 board has gained access to the AT bus ('MASTEREN' is active). When the 80186 CPU has gained access to the AT bus ('MASTEREN' = L) and is reading from or writing to the Local Memory the PAL will activate the refresh signal on the AT bus ('-,REFRESH = L'). Refreshing the System Memory is done when the 80186 is activating the '-,LOCK' signal.

Diagram page 8 shows the AT Interface Controller. When the 80186 access the System Memory the following sequence will occure:

1. '-,SYSACC' becomes active (L).
2. '-,DRQ' is activated by the PAT113.
   The 'AREADY' becomes active.
3. If another LAN board has not activated the DRQ0 signal on the AT bus this LAN board will clock the '-,DRQ' signal through U18 and activate the DRQ0 signal on the AT bus.
4. The system board answer by activating the '-,DACK0' signal which is gated into the LAN452 board and the '-,OBDACK' signal becomes active.
5. 'OBDACK' is latched and the LAN452 board will activate the 'MASTER' signal on AT bus and the 'MASTEREN' signal on the LAN452 board.
6. The 80186 can now read from or write to the System Memory.
7. '-,SYSACC' is deactivated by the 80186 and the 'DRQ0' on the AT bus is also deactivated.

If the '-,LOCK' signal is activated by the 80186 the LAN452 will occupy the AT bus in more than one memory cycle.

Diagram page 9 contains address buffers and data buffers interfacing the AT address and data bus.

Diagram page 10 shows the Reset and Interrupt Logic that consist of a PAL1618 and a 74LS138. A number of latches are implemented in the PAT115 and these latches can be set and reset by writing to I/O addresses from the 80186 CPU and from the System board. The following table shows how:

Signal	Set by (Writing)	Reset by (Writing)
ATINT (Interrupt to 80186)	System board on I/O address 307H(S1=L) or 303H (S1=H)	80186 with PCS2 asserted (I/O address 100H-17FH)
IRQ10 (interrupt to system board)	80186 with PCS3 (I/O address 180H-1FFH)	System board on I/O address 306H (S1=L) or 302H (S1=H).
RESET	System board on I/O address 305H (S1=L) or 301H (S1=H) or by System board RESET DRV signal	System board on I/O address 304H (S1=L) or 300H (S1=H) or by Debug board.

When the system board is deactivating the 'RESET' signal a clock signal will be generated to the Boot Memory Map register and this register will thus be loaded by the system board.

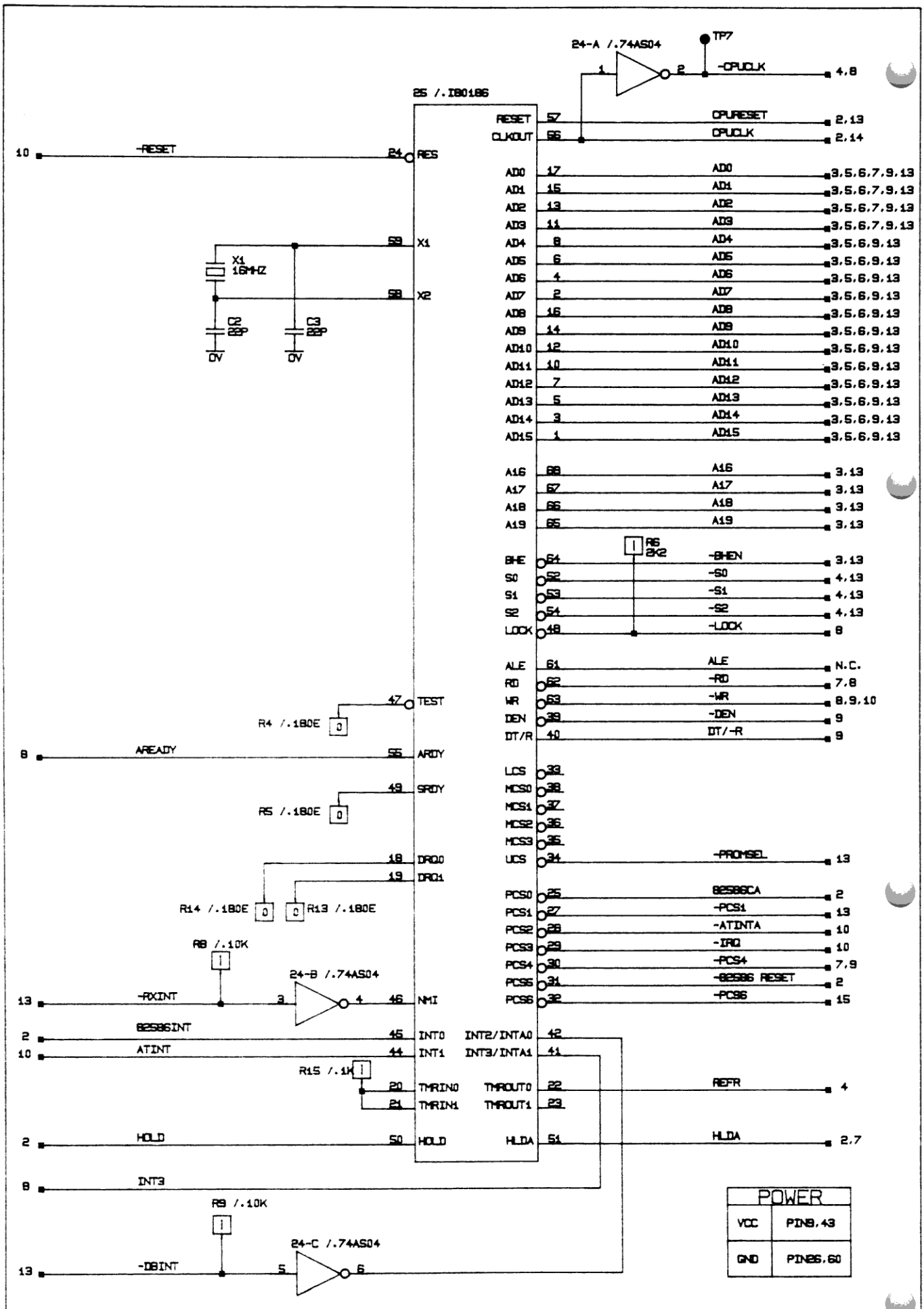
Diagram page 11 and 12 shows the AT bus connection.

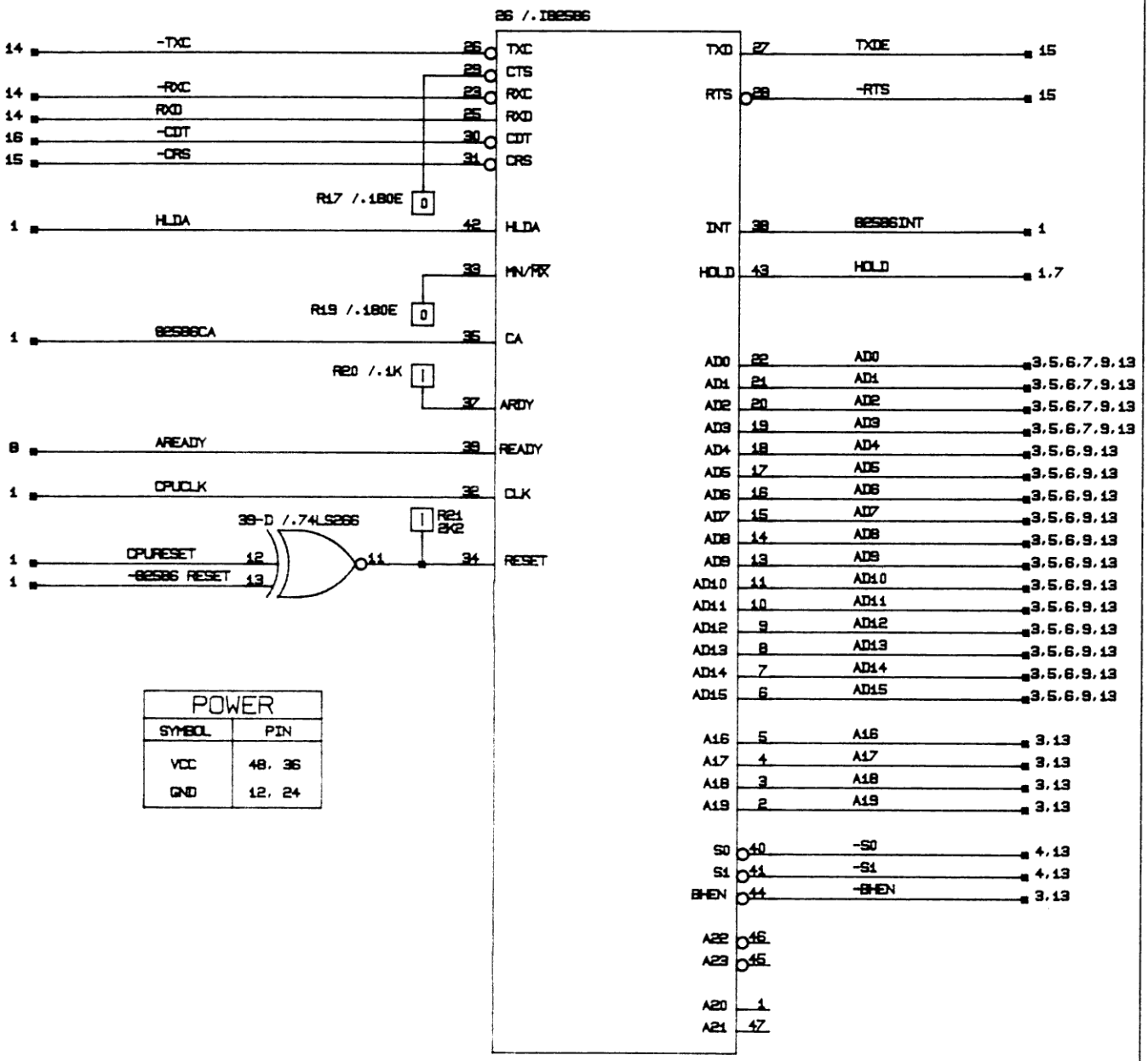
Diagram page 13 shows the Debug Board connection.

Diagram page 14 shows the Ethernet Serial Interface. This is either an Intel 80501 or a SEEQ 8023 chip. Transmit data from the 82586 is encoded into Manchester code and receive data from the transceiver is decoded. A receiver clock is extracted from the Manchester coded data from the transceiver.

Diagram page 15 shows the 15 pol connector to the transceive cable.

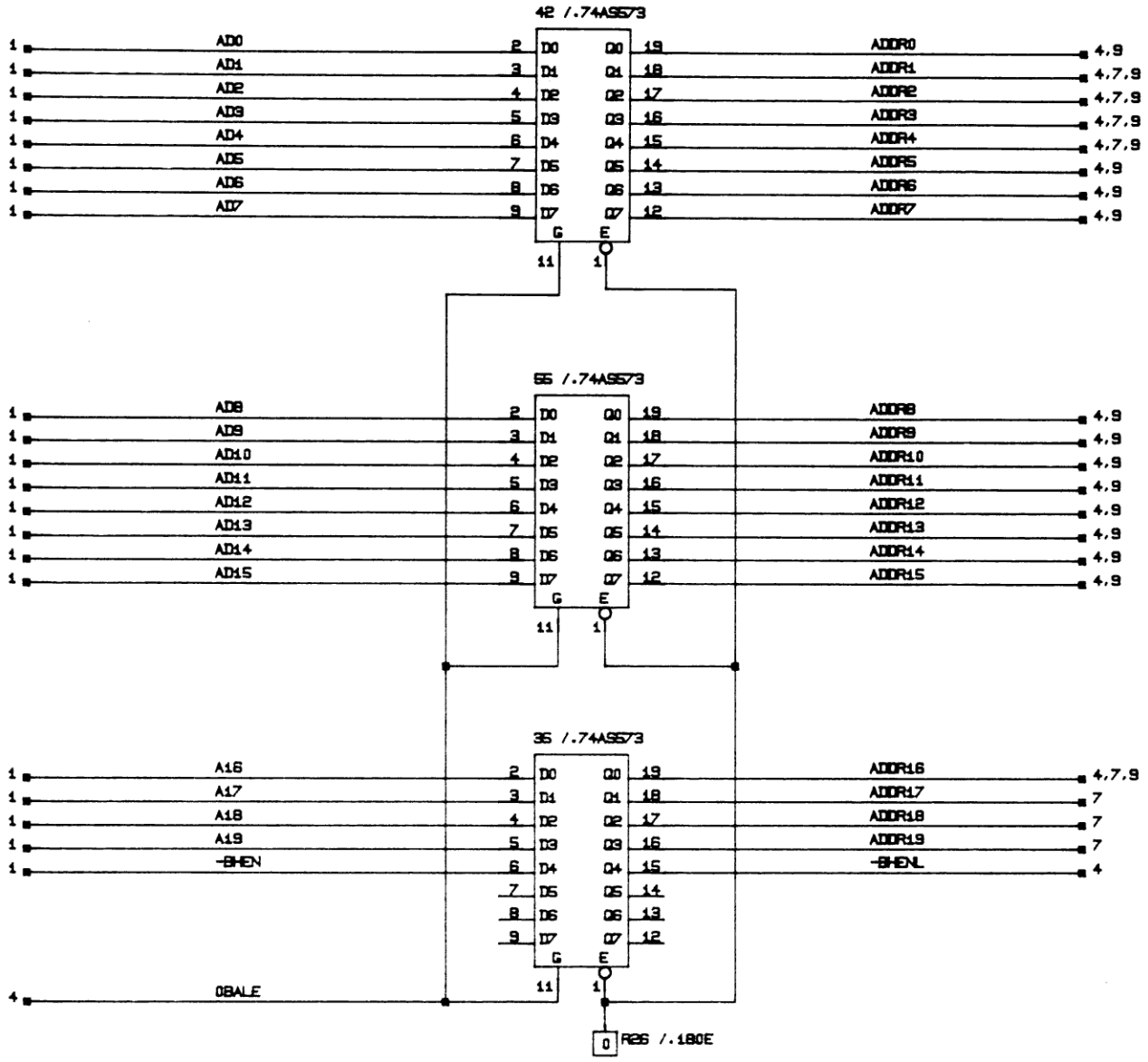
4.3 Logic Diagrams


24-A /.74AS04
TP7
-CPUCLK
4,8
25 /.I80186
RESET
CLKOUT
CPURESET
CPUCLK
2,13
2,14
10
-RESET
RES
X1
X2
X1
16MHZ
C2
22P
C3
22P
0V
0V
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
3,5,6,7,9,13
3,5,6,9,13
A16
A17
A18
A19
3,13
R6
2K2
BHE
S0
S1
S2
LOCK
-BHEN
-S0
-S1
-S2
-LOCK
4,13
8
ALE
RD
WR
DEN
DT/R
N.C.
7,8
8,9,10
9
R4 /.180E
TEST
8
AREADY
ARDY
SRDY
R5 /.180E
LCS
MCS0
MCS1
MCS2
MCS3
UCS
-PROMSEL
13
DRQ0
DRQ1
R14 /.180E
R13 /.180E
PCS0
PCS1
PCS2
PCS3
PCS4
PCS5
PCS6
82586CA
-PCS1
-ATINTA
-IRQ
-PCS4
-82586 RESET
-PCS6
2
13
10
10
7,9
2
15
R8 /.10K
24-B /.74AS04
13
-RXINT
NMI
2
82586INT
INT0
10
ATINT
INT1
INT2/INTA0
INT3/INTA1
R15 /.1K
TMRIN0
TMRIN1
TMROUT0
TMROUT1
REFR
4
2
HOLD
HOLD
HLDA
HLDA
2,7
8
INT3
R9 /.10K
24-C /.74AS04
13
-DBINT
POWER
VCC
PIN8,43
GND
PIN26,60
UNIT LAN452
DESIGN JKA
DWG. NO.
DRAWN LIJ 880408
S1

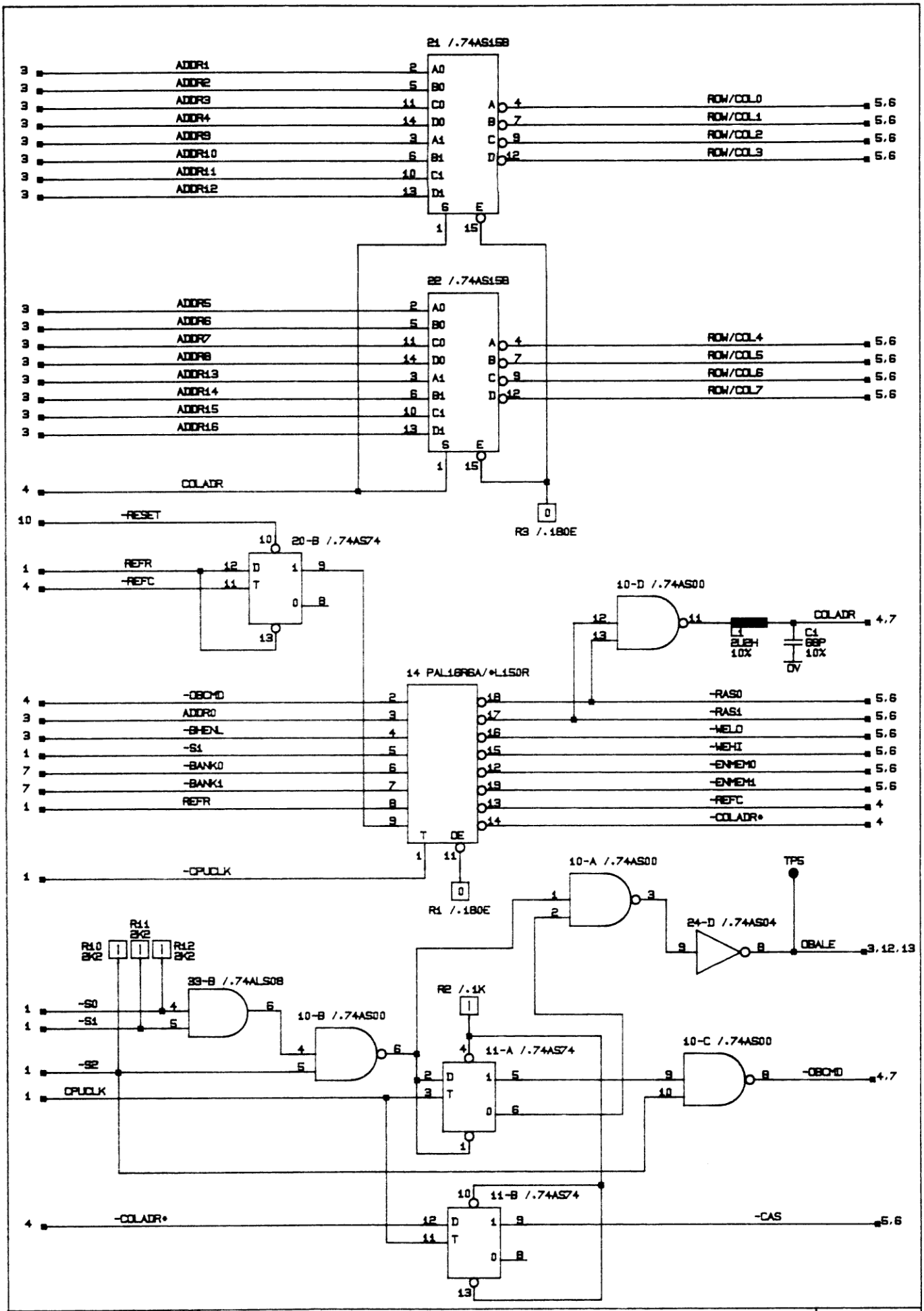


POWER	
SYMBOL	PIN
VCC	48, 36
GND	12, 24

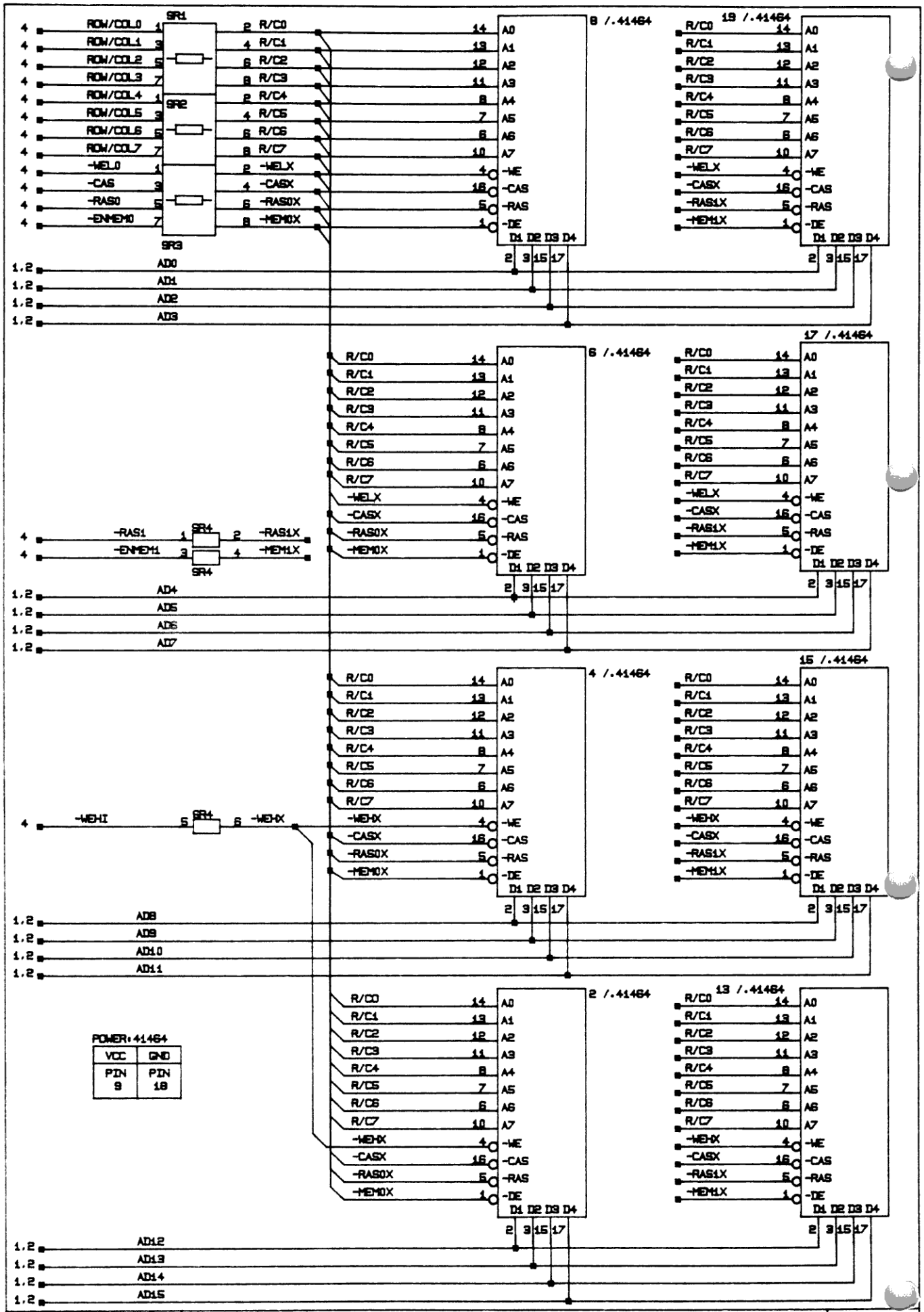
UNIT LAN452	DESIGN JKA		S2
DWG. NO.	DRAWN LIJ 880408		

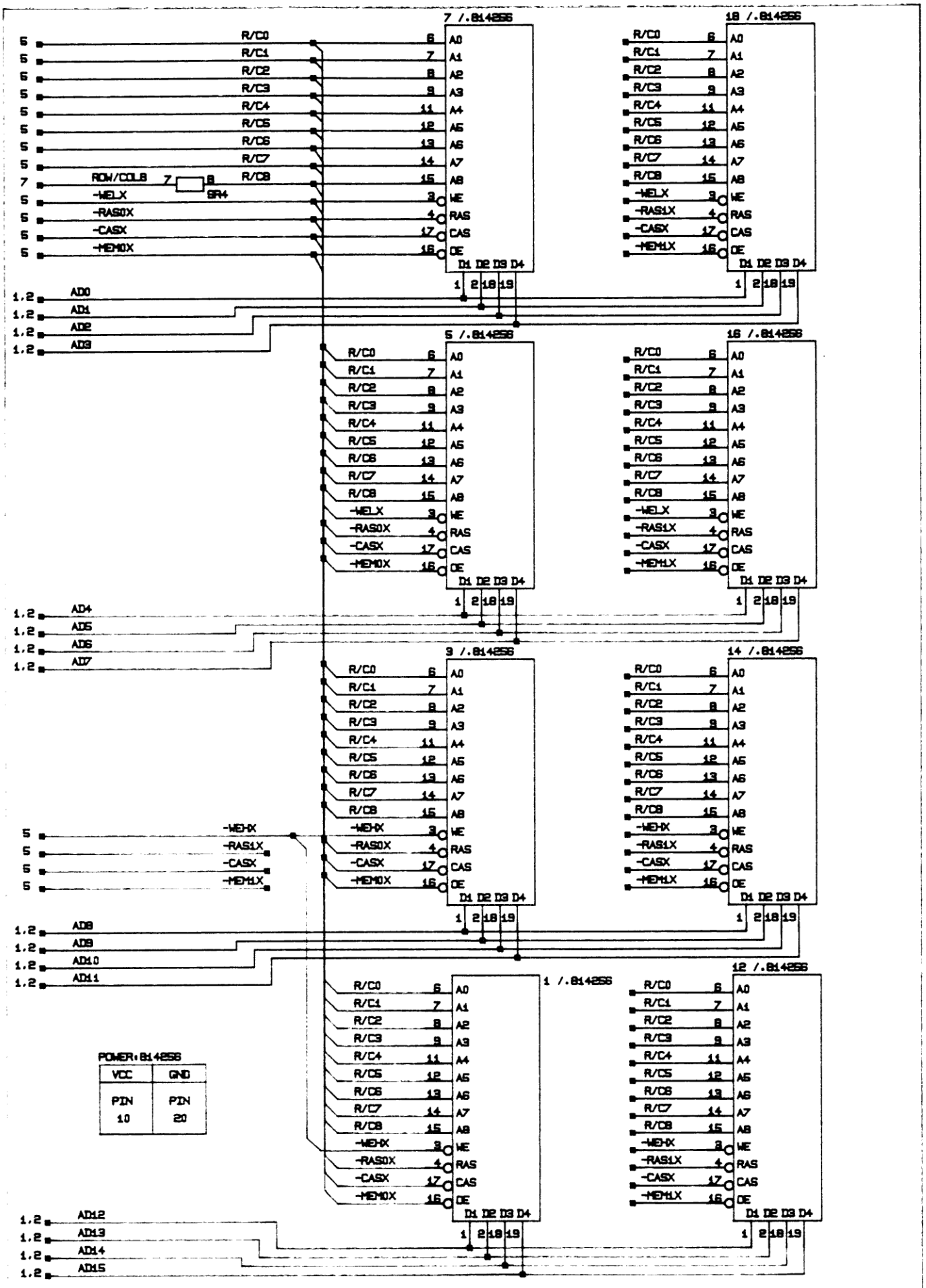


UNIT LAN452	DESIGN JKA		S3
DWG. NO.	DRAWN LIJ 880408		

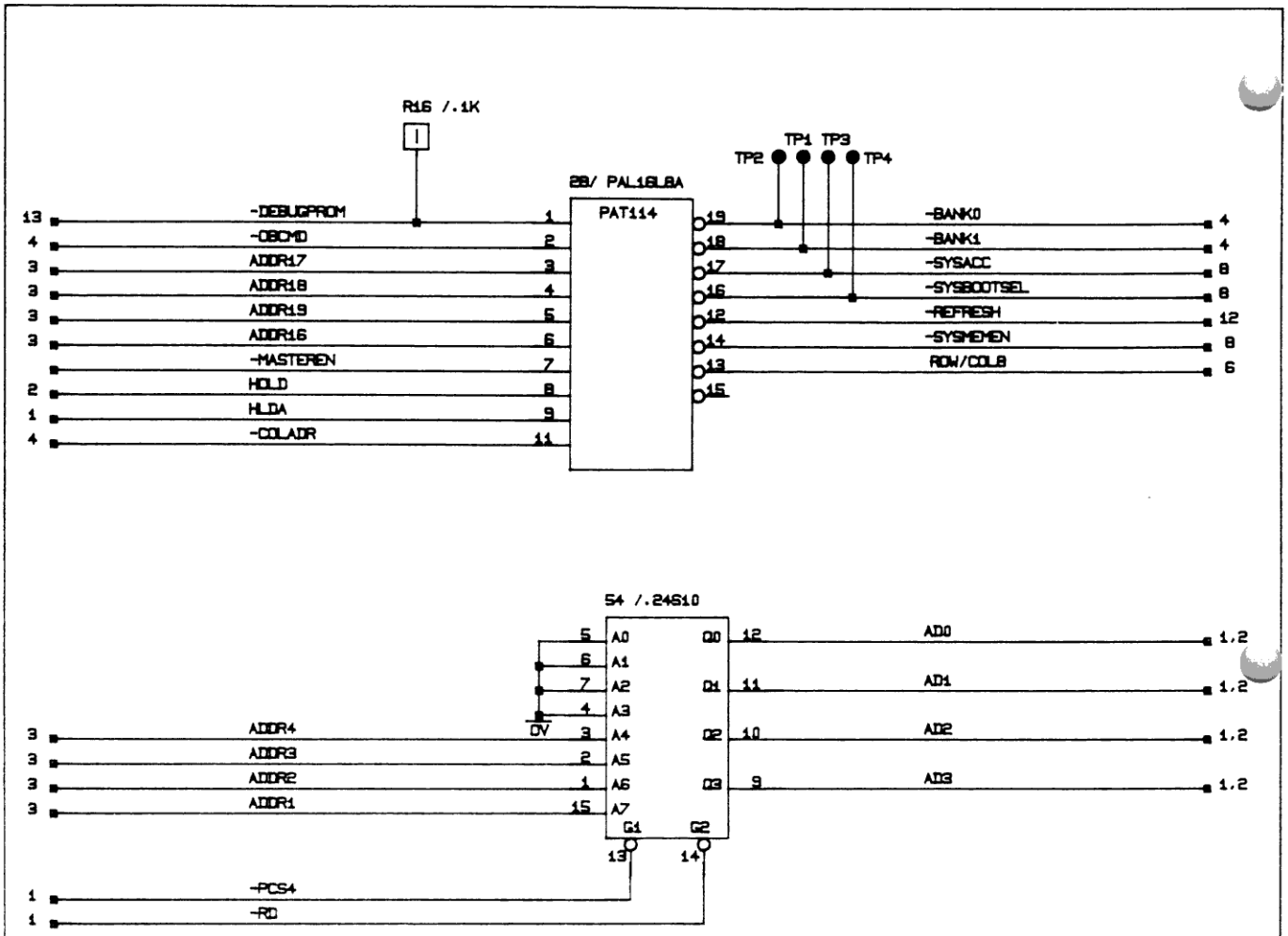


UNIT LAN452	DESIGN JKA	DRAM INTERFACE & REFRESH LOGIC	S4
DWG. NO.	DRAWN LIJ 880408		

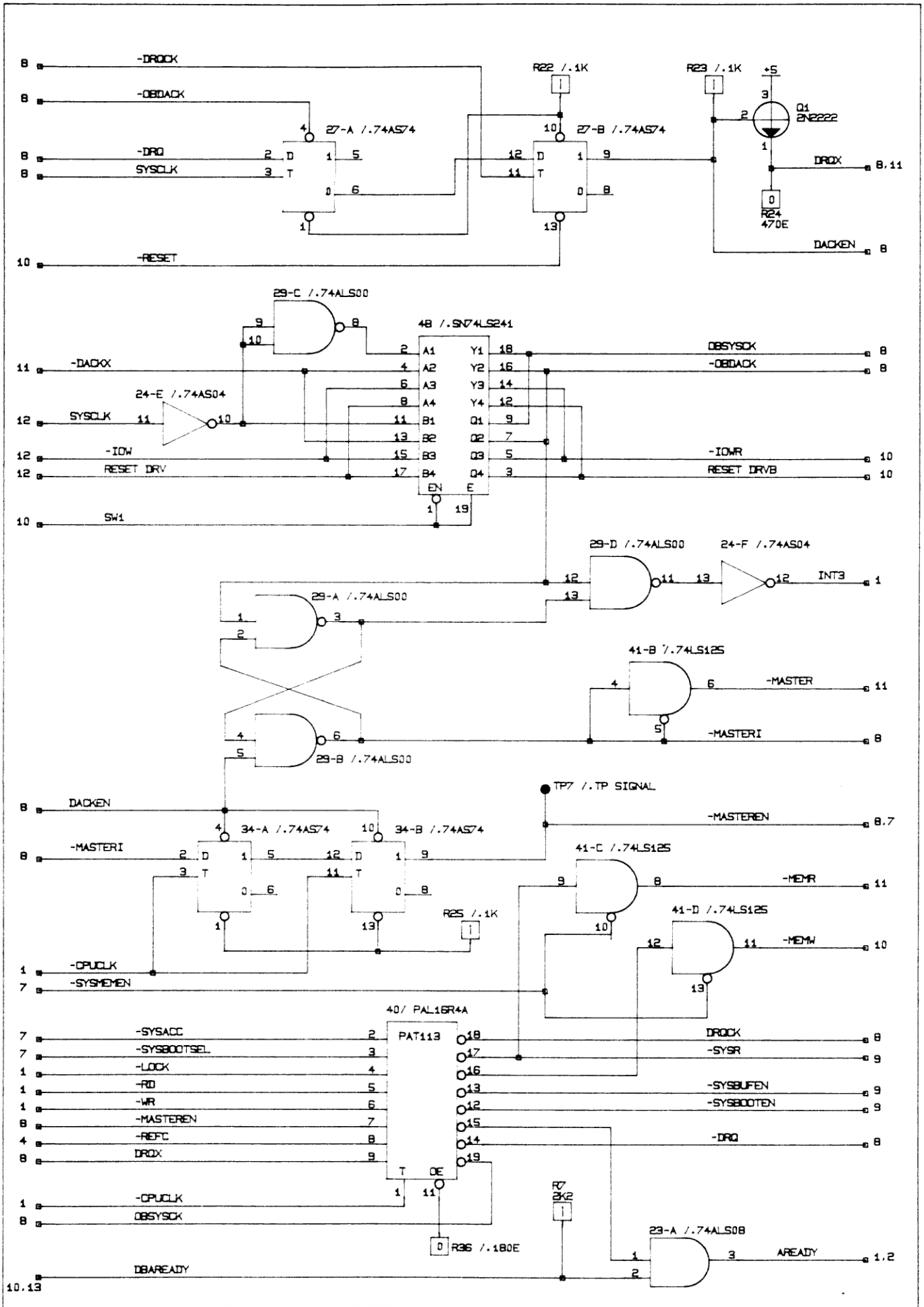

SR1
SR2
SR3
SR4
ROW/COL0
ROW/COL1
ROW/COL2
ROW/COL3
ROW/COL4
ROW/COL5
ROW/COL6
ROW/COL7
-WEL0
-CAS
-RAS0
-ENMEM0
R/C0
R/C1
R/C2
R/C3
R/C4
R/C5
R/C6
R/C7
-WELX
-CASX
-RAS0X
-MEM0X
-RAS1
-ENMEM1
-RAS1X
-MEM1X
-WEHI
-WEHX
8 /.41464
19 /.41464
6 /.41464
17 /.41464
4 /.41464
15 /.41464
2 /.41464
13 /.41464
A0
A1
A2
A3
A4
A5
A6
A7
-WE
-CAS
-RAS
-DE
D1 D2 D3 D4
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
POWER:41464
VCC
GND
PIN 9
PIN 18
UNIT
LAN452
DESIGN
JKA
DWG. NO.
DRAWN
LIJ
880408
128K/256K RAM ARRAY
S5



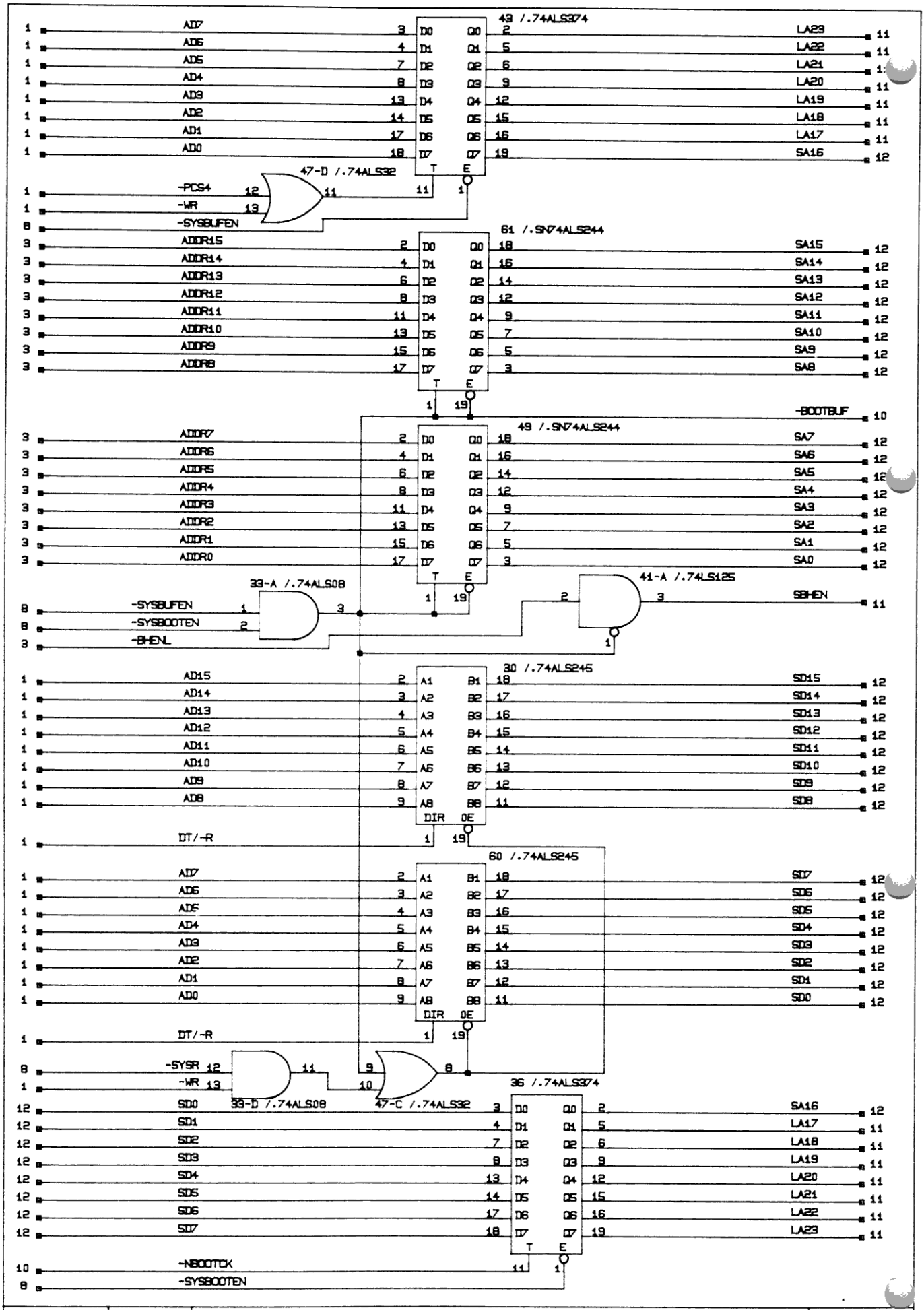
UNIT LAN452	DESIGN JKA	512K / 1M RAM ARRAY	S6
DWG. NO.	DRAWN LIJ 880408		



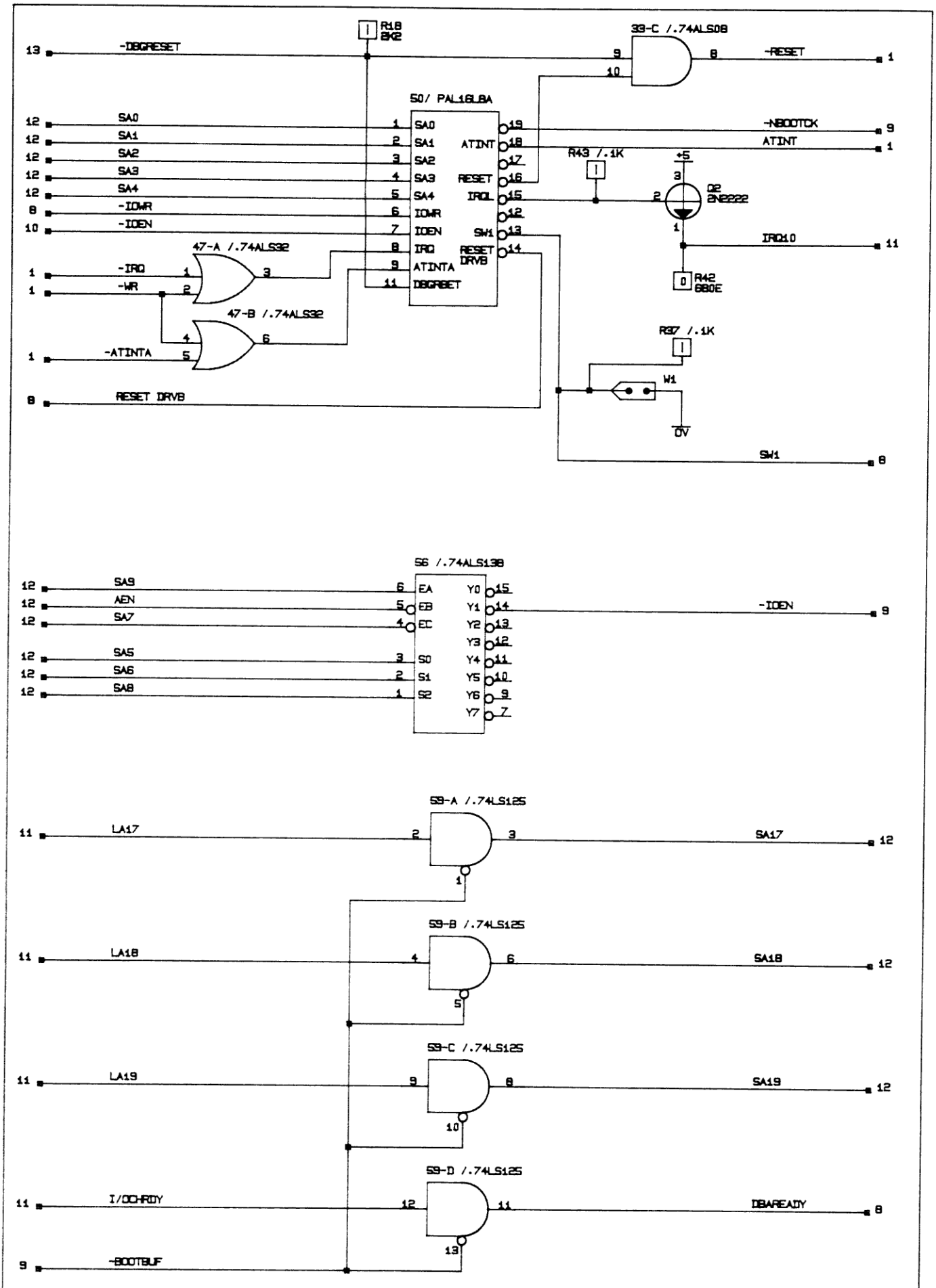
UNIT LAN452	DESIGN JKA		S7
DWG. NO.	DRAWN LIJ 880408		



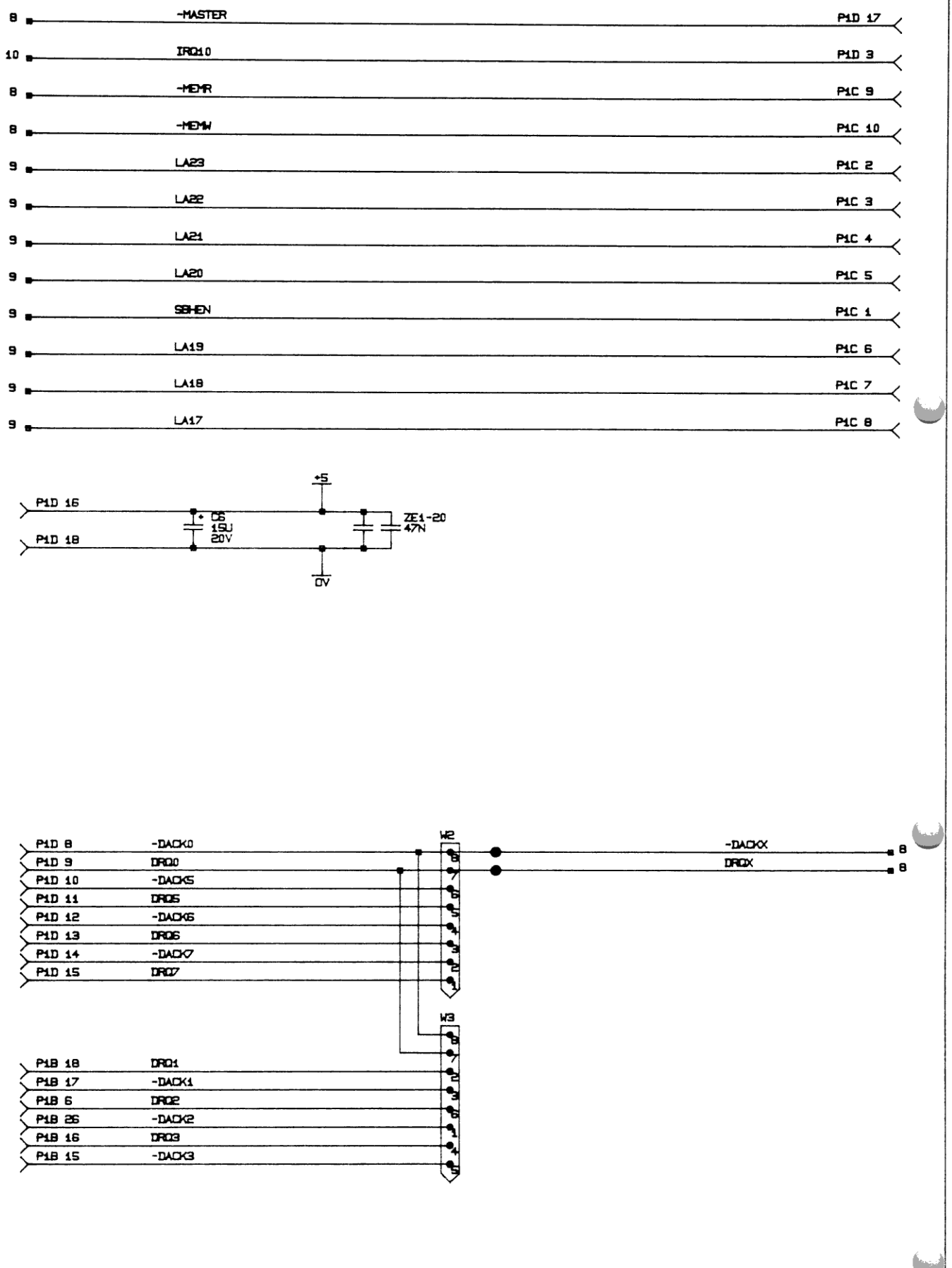
UNIT LAN452	DESIGN JKA	AT-BUS INTERFACE LOGIC	S8
DWG. NO.	DRAWN LIJ 880407		



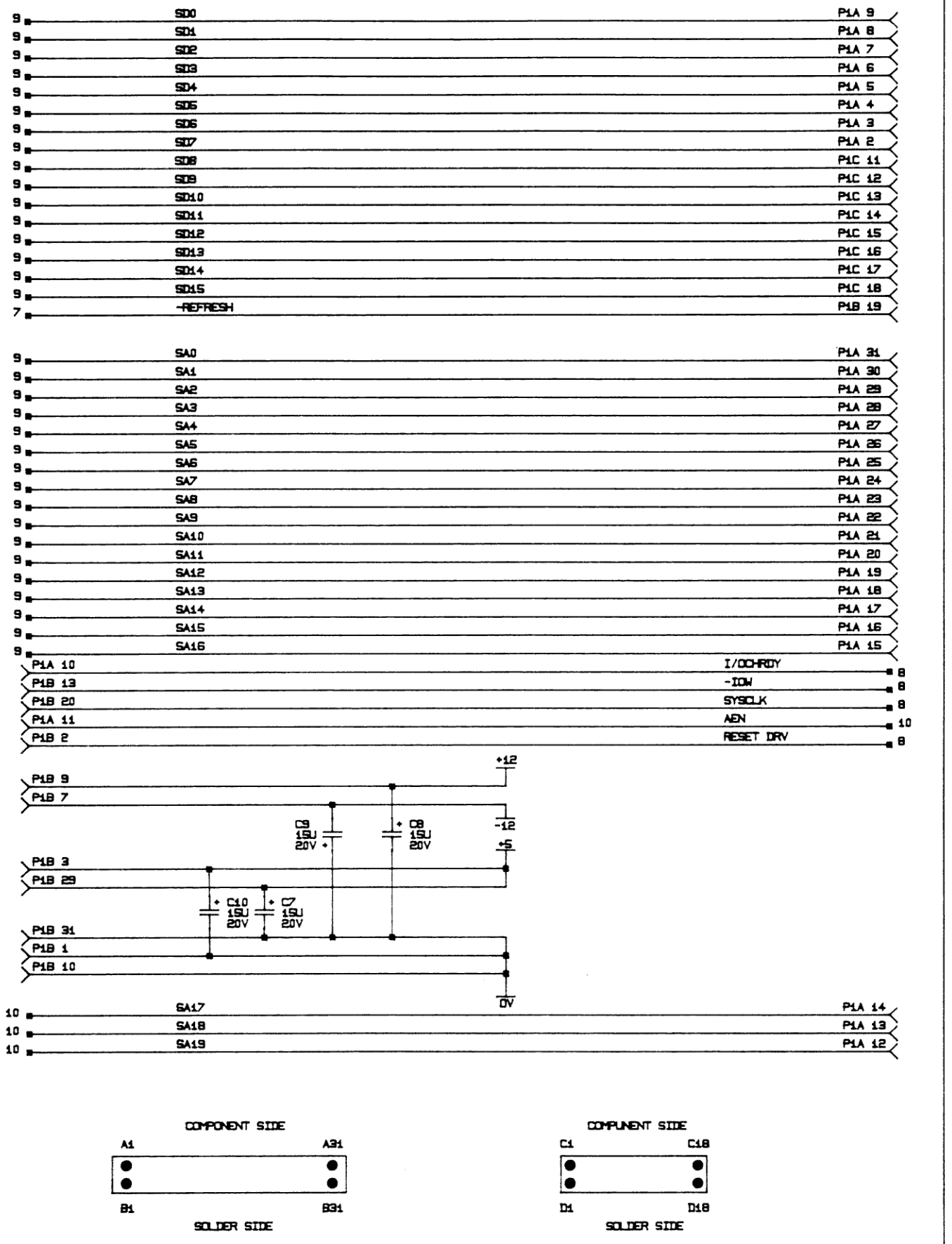
UNIT LAN452	DESIGN JKA	AT-BUS INTERFACE	S9
DWG. NO.	DRAWN LIU 880405		



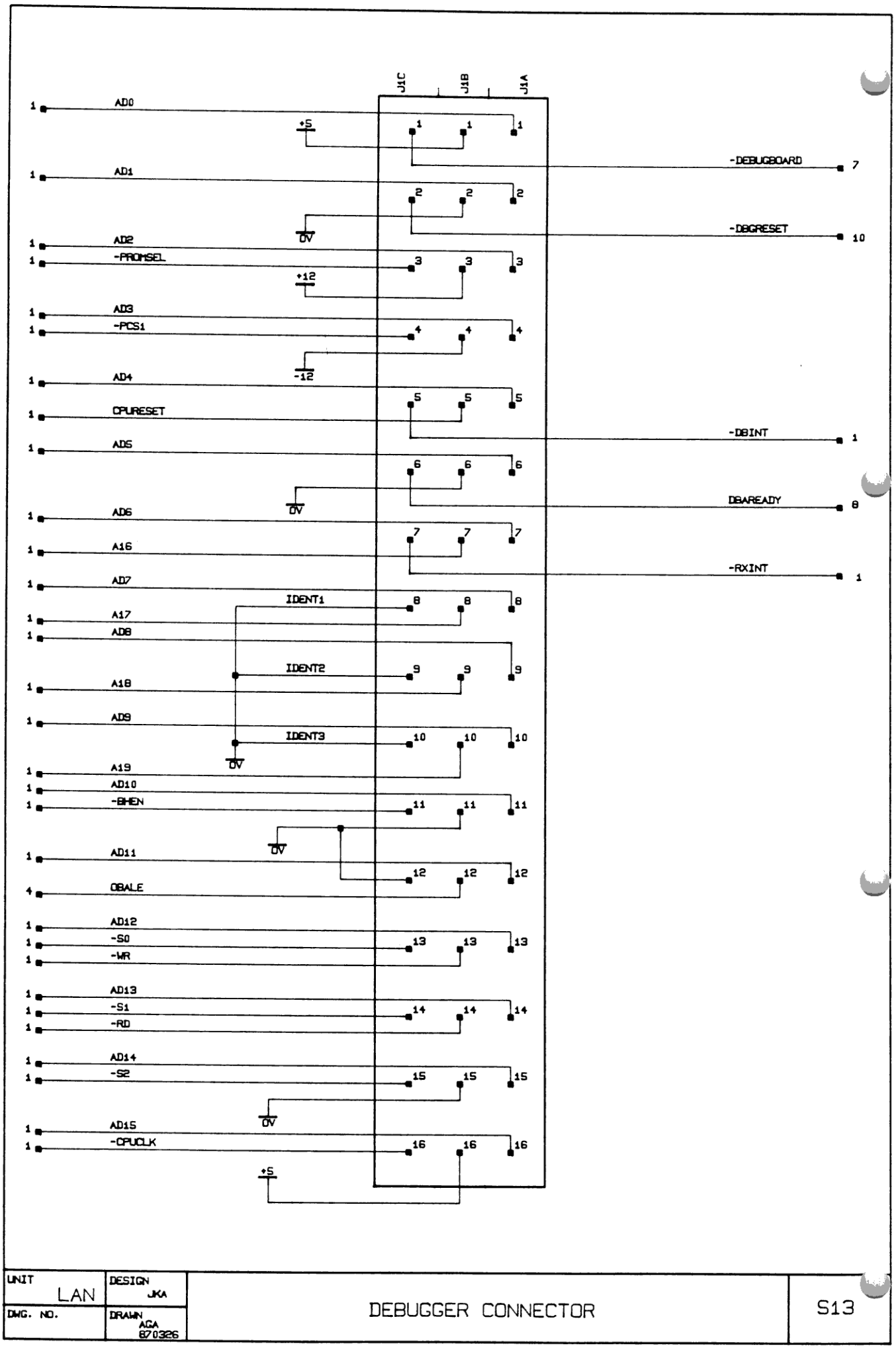
UNIT LAN452	DESIGN JKA	AT-BUS INTERFACE	S10
DWG. NO.	DRAWN LIJ 880408		



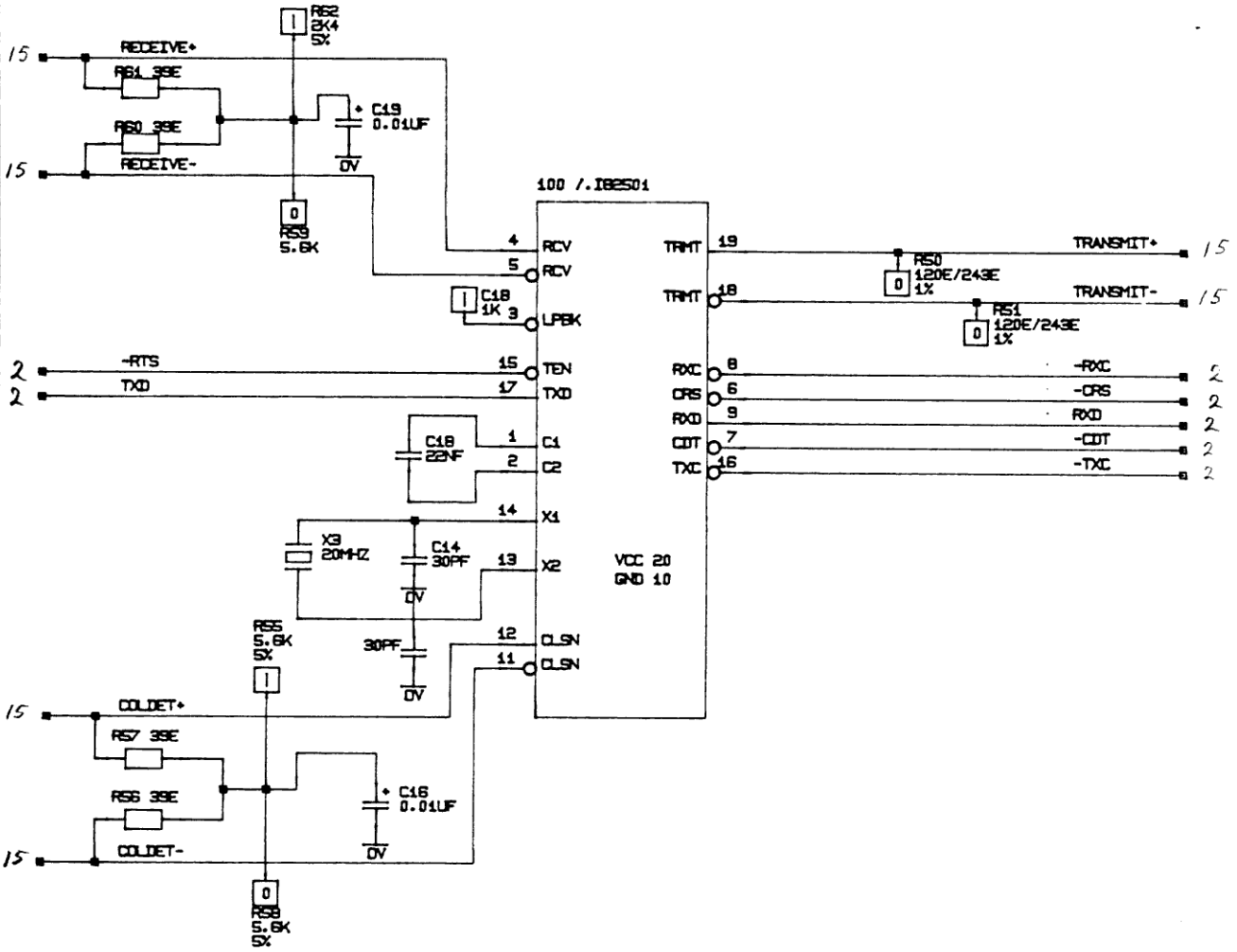
UNIT LAN452	DESIGN JKA	AT-BUS CONNECTOR	S11
DWG. NO.	DRAWN LIJ 880408		



UNIT LAN452	DESIGN JKA	AT-BUS CONNECTOR	S12
DWG. NO.	DRAWN LIJ 880408		

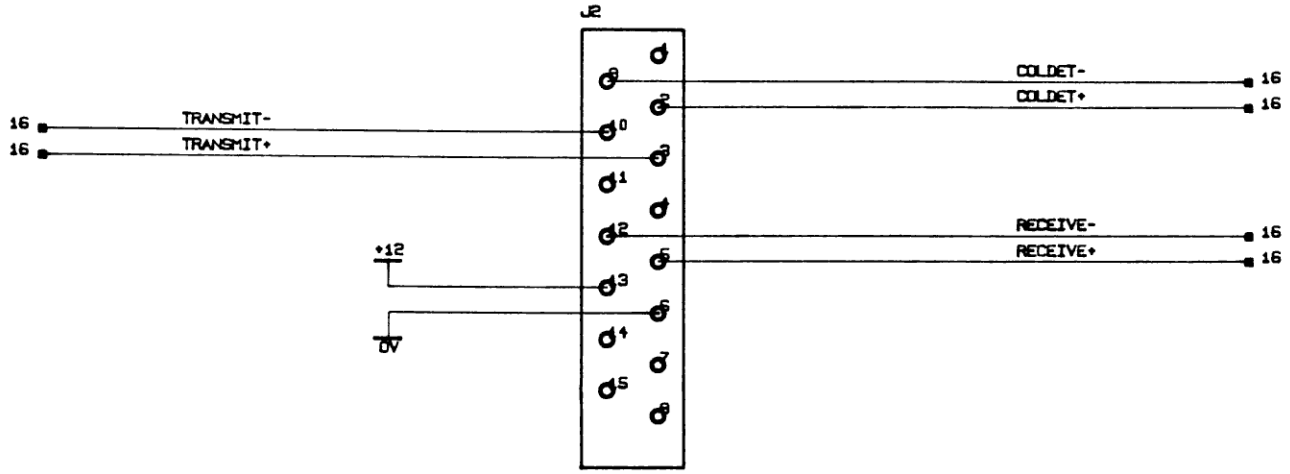


UNIT	DESIGN		
LAN	JKA	DEBUGGER CONNECTOR	S13
DWG. NO.	DRAWN AGA 870326		



	INTEL 82501	SEEQ 7023
R62, R59	INGEN	2.4K 5%
R55, R58	INGEN	2.6K 5%
R50, R51	120E	243E 1%

UNIT LAN452	DESIGN JKA	ETHERNET SERIAL INTERFACE	S14
DWG. NO.	DRAWN LIJ 871023		



UNIT LAN	DESIGN JKA		S15
DWG. NO.	DRAWN AGA 870326		

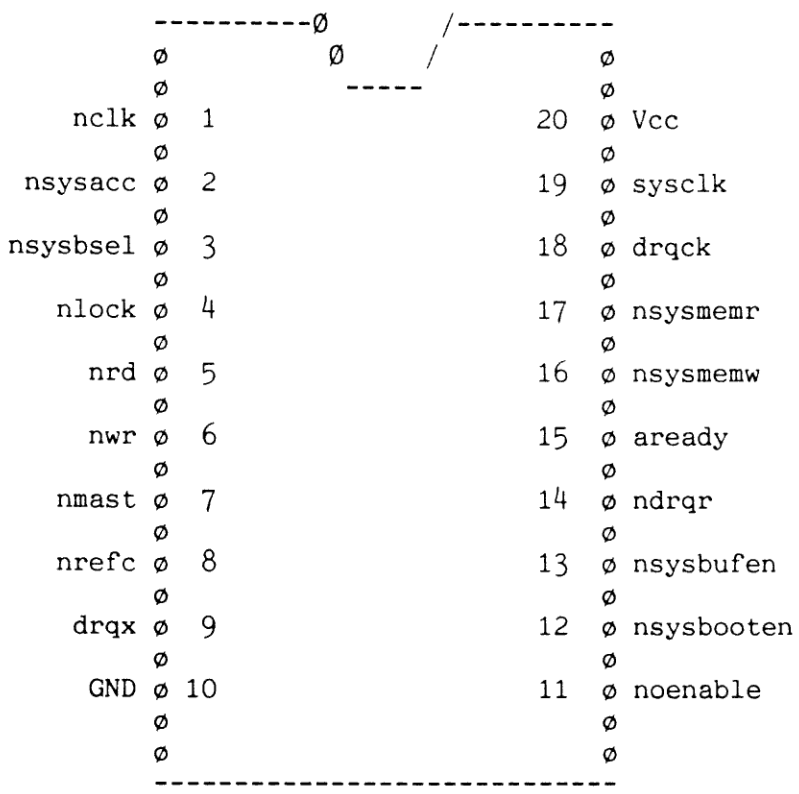
4.4 PAL and ROM description

```
                                                                    Page 1
ABEL(tm) Version 2.02a  -  Document Generator          03-Apr-87 01:42 PM
LAN451 I/O BUS Controller, 2. FEB. 1987 ,
               Jens K. Andreassen , Regnecentralen A/S,
               Ballerup
Equations for Module PAT113TX

Device PAT113


     Reduced Equations:

       enable nsysbooten = (1);

       enable nsysbufen = (1);

       enable drqck = (1);

       enable sysclk = (0);

       nsysbooten = !(!nsysbooten & !nsysmemr
                    # !nsysbooten & !nsysmemw
                    # !nmast & !nsysacc & !nsysbsel);


       nsysbufen = !(!nsysbufen & !nsysmemr
                   # !nsysbufen & !nsysmemw
                   # !nmast & !nsysacc & nsysbsel);


       ndrqr := !(!nsysacc # !ndrqr & !nlock);

       aready := !(nmast & !nsysacc
                 # !nrefc & nsysacc
                 # !nmast & nrd & nwr);


       nsysmemw := !(!nmast & !nsysacc & !nwr);

       nsysmemr := !(!nmast & !nrd & !nsysacc);

       drqck = !(sysclk
               # drqx & !ndrqr
               # drqx & sysclk
               # !ndrqr & sysclk
               # ndrqr & sysclk);
```

ABEL(tm) Version 2.02a - Document Generator 03-Apr-87 01:42 PM
LAN451 I/O BUS Controller, 2. FEB. 1987 ,
Jens K. Andreassen , Regnecentralen A/S,
Ballerup
Chip diagram for Module PAT113TX

Device PAT113

P16R4



end of module PAT113TX

ABEL(tm) Version 2.02a - Document Generator 03-Apr-87 01:40 PM
LAN451 I/O interrupt and reset , 2. FEB. 1987,
Jens K. Andreassen , Regnecentralen A/S,Ballerup
Equations for Module PAT115TX

Device PAT115

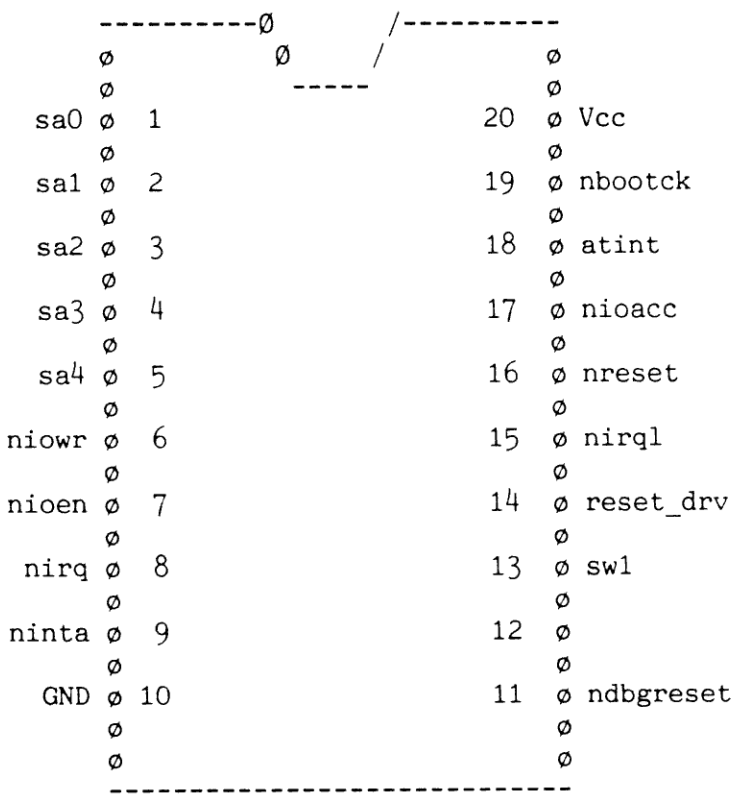
Reduced Equations:

```
enable nioacc = (1);

enable atint = (1);

enable reset_drv = (0);

enable sw1 = (0);

enable nirql = (1);

enable nreset = (1);

enable nbootck = (1);

nbootck = !(!nioacc & !sa0 & !sa1);

nioacc = !(!nioen & !niowr & !sa2 & !sa3 & !sa4 & sw1
         # !nioen & !niowr & sa2 & !sa3 & !sa4 & !sw1);


nreset = !(ndbgreset & reset_drv
         # ndbgreset & nioacc & !nreset
         # ndbgreset & !nreset & sa0
         # ndbgreset & !nreset & sa1
         # ndbgreset & !nioacc & sa0 & !sa1);


atint = !(!ndbgreset
        # !ninta
        # !nreset
        # !atint & nioacc
        # !atint & !sa0
        # !atint & !sa1);


nirql = !(!ndbgreset
        # !nreset
        # nirq & !nirql
        # !nioacc & !sa0 & sa1);
```

ABEL(tm) Version 2.02a - Document Generator 03-Apr-87 01:40 PM
LAN451 I/O interrupt and reset , 2. FEB. 1987,
Jens K. Andreassen , Regnecentralen A/S,Ballerup
Chip diagram for Module PAT115TX

Device PAT115

P16L8



end of module PAT115TX

ABEL(tm) Version 2.02a - Document Generator 03-Apr-87 12:40 PM
LAN451 DRAM controller .21 jan 1987
Jens K. Andreassen, Regnecentralen A/S, BALLERUP
Equations for Module PAT116TX

Device PAT116

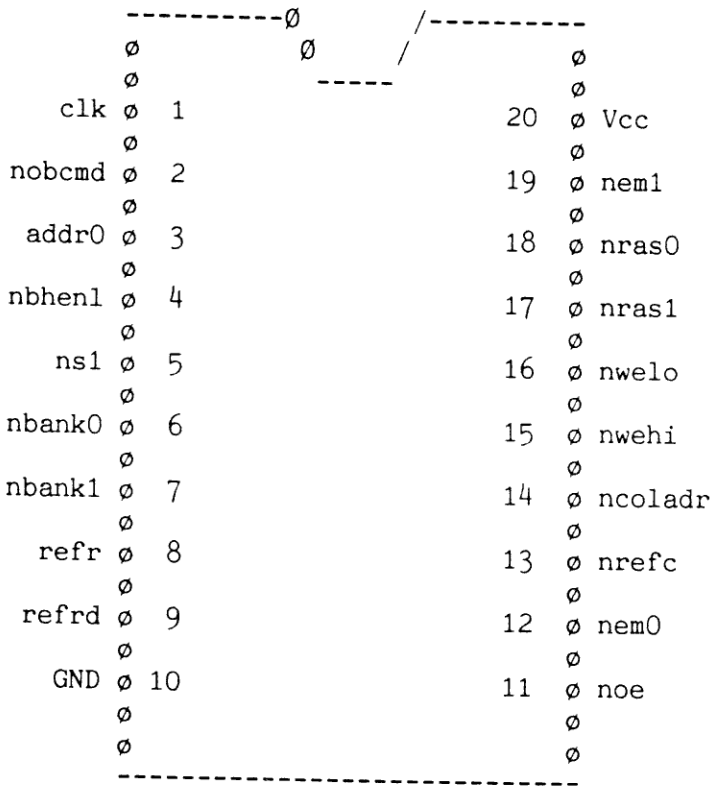
Reduced Equations:

```
enable nem0 = (1);

enable nem1 = (1);

nem0 = !(!ncoladr & !nras0 & nrefc & !ns1);

nem1 = !(!ncoladr & !nras1 & nrefc & !ns1);

nras0 := !(!ncoladr & !nrefc # !nbank0 & !nobcmd & nrefc);

nras1 := !(!ncoladr & !nrefc # !nbank1 & !nobcmd & nrefc);

nwelo := !(!addr0 & !nbank0 & ncoladr & !nobcmd & nrefc & ns1
        # !addr0 & !nbank1 & ncoladr & !nobcmd & nrefc & ns1);


nwehi := !(!nbank0 & !nbhen1 & ncoladr & !nobcmd & nrefc & ns1
        # !nbank1 & !nbhen1 & ncoladr & !nobcmd & nrefc & ns1);


nrefc := !(!ncoladr & !nrefc & refr & !refrd
        # nbank0 & nbank1 & nrefc & refr & !refrd
        # ncoladr & nras0 & !nrefc & refr & !refrd);


ncoladr := !(nras0 & !nrefc
          # !nbank0 & !nobcmd & nrefc
          # !nbank1 & !nobcmd & nrefc);
```

Jens K. Andreassen, Regnecentralen A/S, BALLERUP
Chip diagram for Module PAT116TX

Device PAT116

P16R6



end of module PAT116TX

ABEL(tm) Version 2.02a - Document Generator 05-May-87 01:38 PM
LAN451 Memory selector, 29. JAN. 1987,
Jens K. Andreassen, Regnecentralen A/S , Ballerup
Equations for Module PAT117TX

Device PAT117

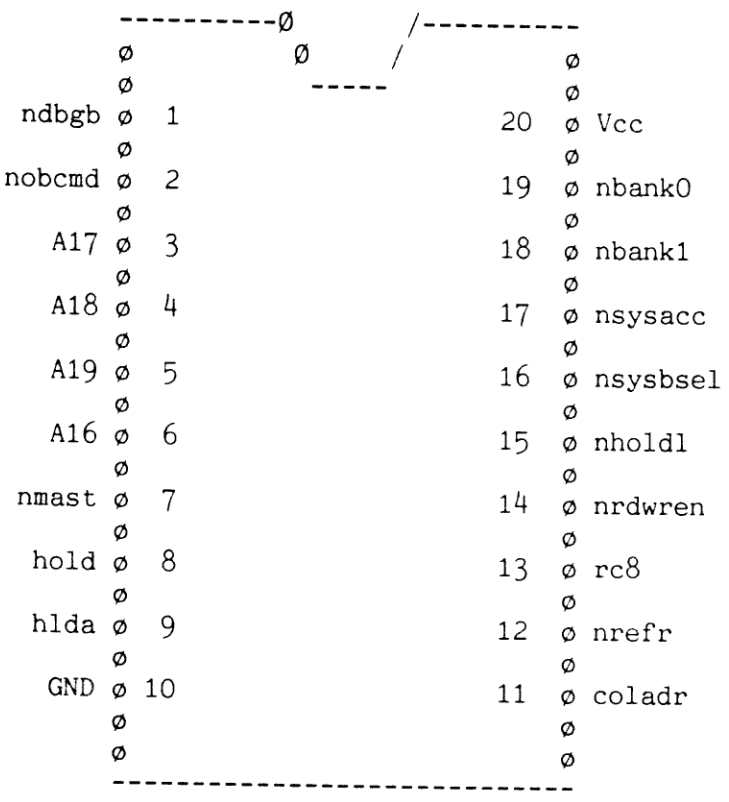
Reduced Equations:

```
enable nbank0 = (1);

enable nbank1 = (1);

enable nsysacc = (1);

enable nsysbsel = (1);

enable nrefr = (!nmast);

enable nrdwren = (1);

enable nholdl = (1);

enable rc8 = (1);

nbank0 = !(!A19 & !nobcmd # !nholdl & !nobcmd);

nbank1 = !(!A17 & A19 & nholdl & !nobcmd
         # !A18 & A19 & nholdl & !nobcmd);


nsysacc = !(!A16 & A17 & A18 & A19 & nholdl & !nobcmd
          # A16 & A17 & A18 & A19 & ndbgb & nholdl & !nobcmd);


nsysbsel = !(A16 & A17 & A18 & A19 & ndbgb & nholdl & !nobcmd);

rc8 = !(!A17 & !A18 # !A17 & coladr # !A18 & !coladr);

nholdl = !(hlda & hold # hold & !nholdl);

nrefr = !(!A17 & !nobcmd # !A18 & !nobcmd # !A19 & !nobcmd);

nrdwren = !(A17 & A18 & A19 & !nmast);
```

Chip diagram for Module PAT117TX

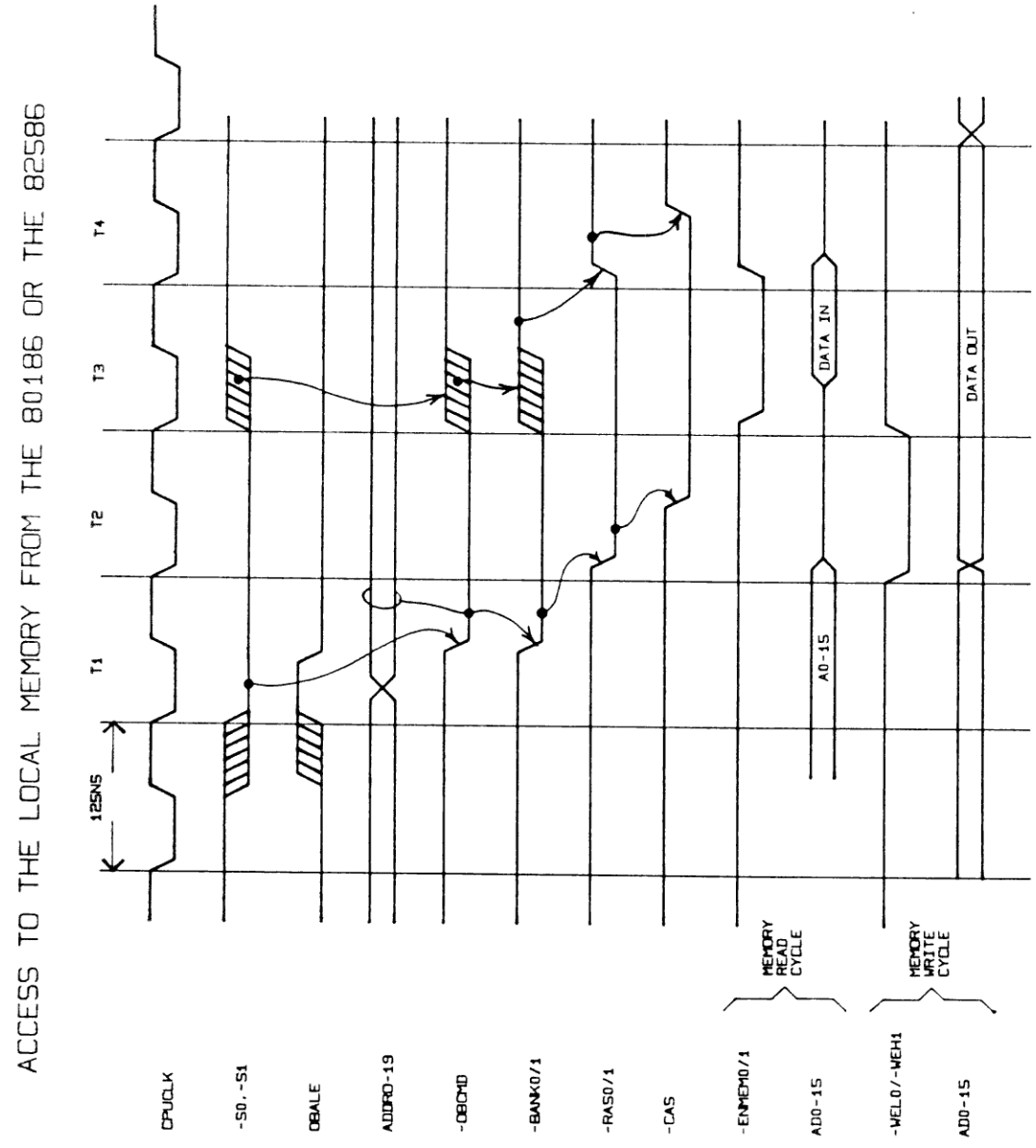
Device PAT117

P16L8



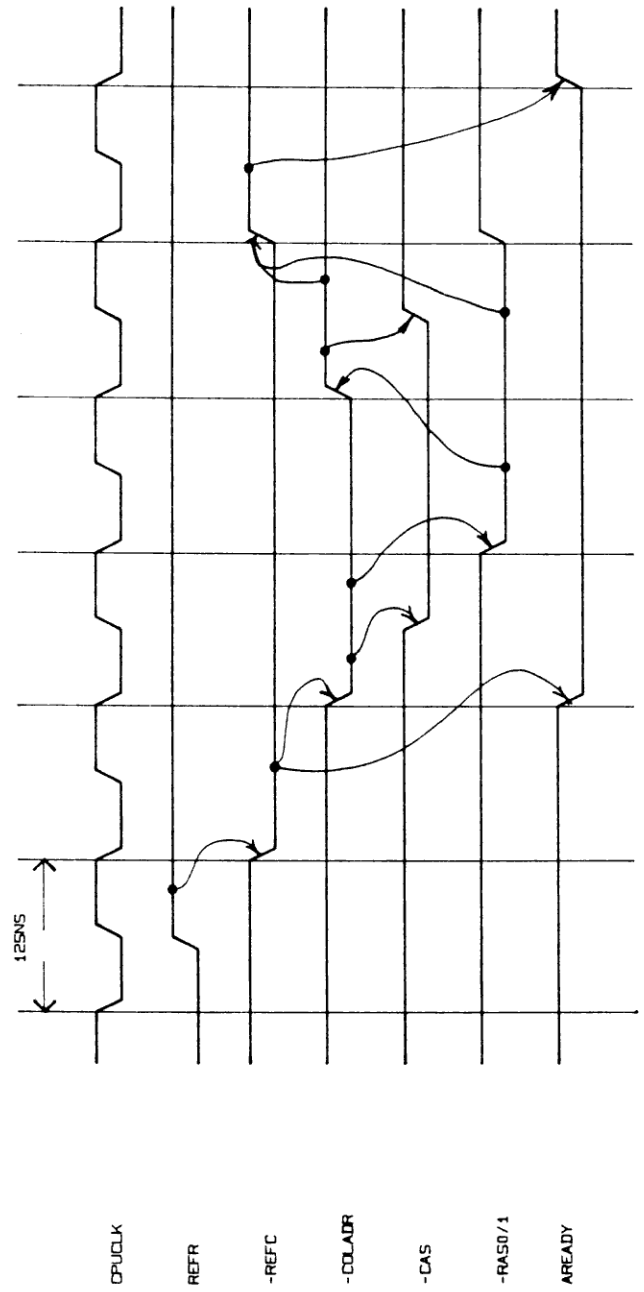
end of module PAT117TX

4.5 Timing diagrams

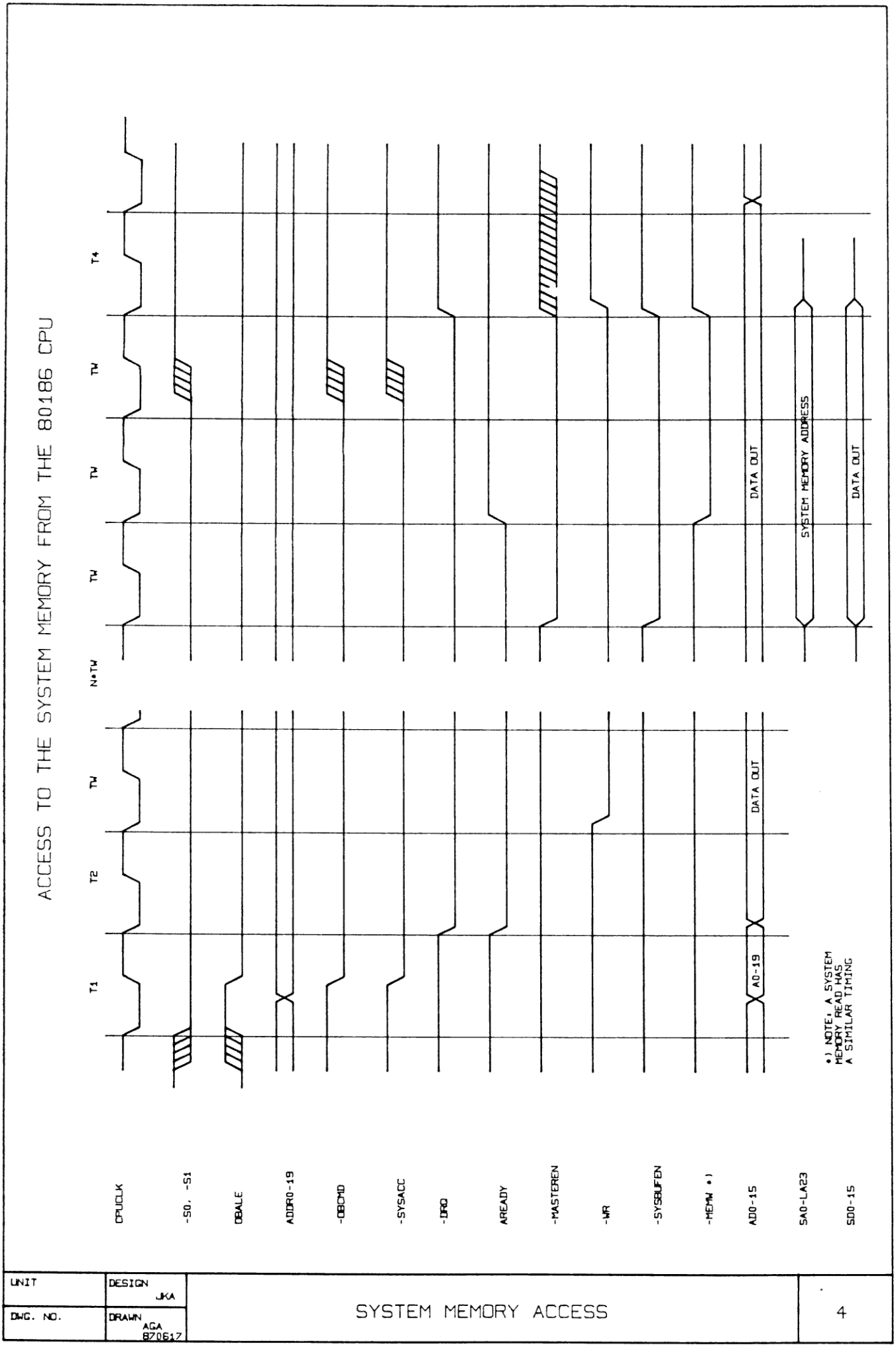


UNIT	DESIGN JKA	ON BOARD MEMORY ACCESS	6
DWG. NO.	DRAWN AGA 870617		

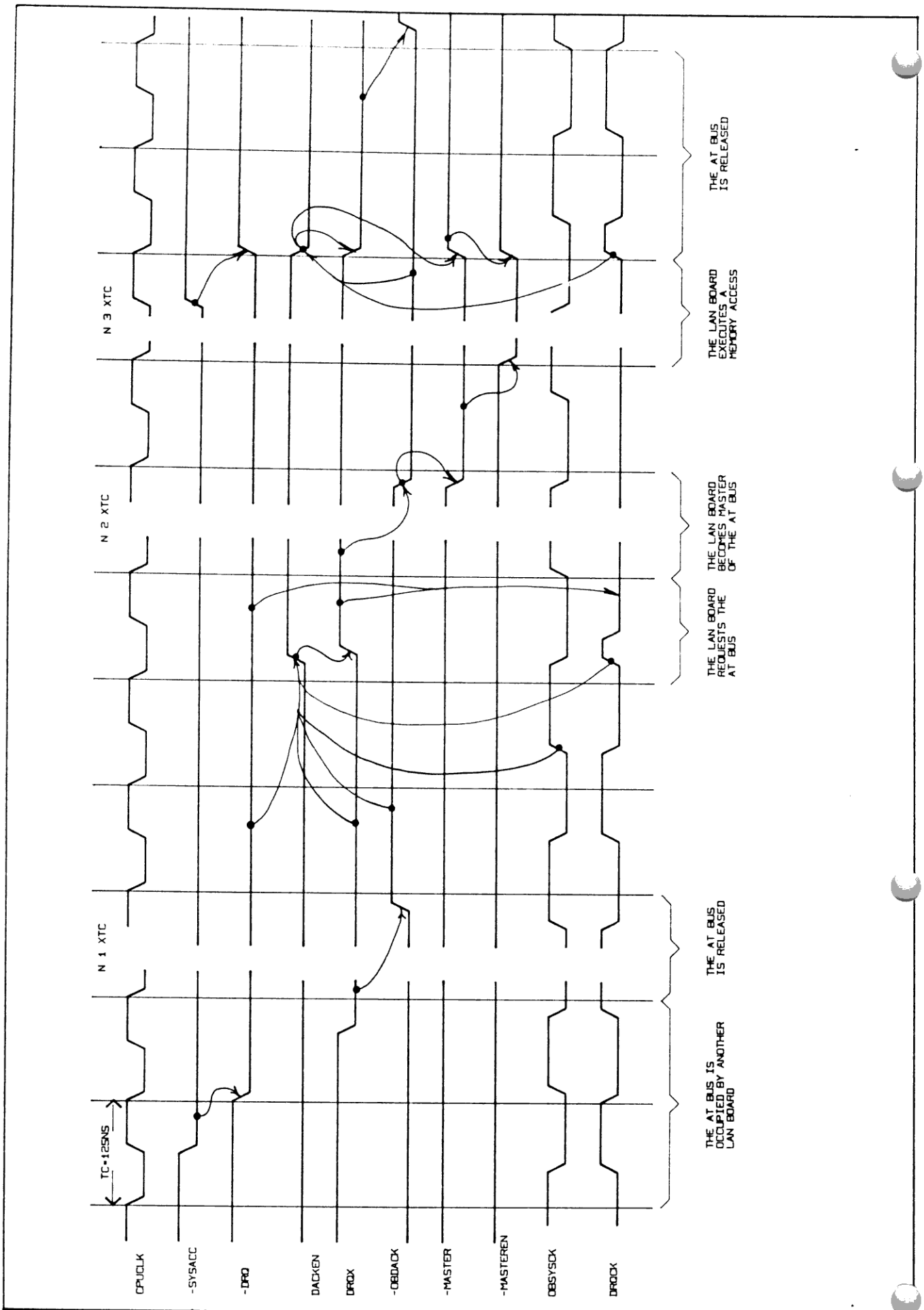
CAS BEFORE RAS MEMORY REFRESH



UNIT	DESIGN JKA	ON BOARD MEMORY REFRESH	7
DWG. NO.	DRAWN AGA 870617		

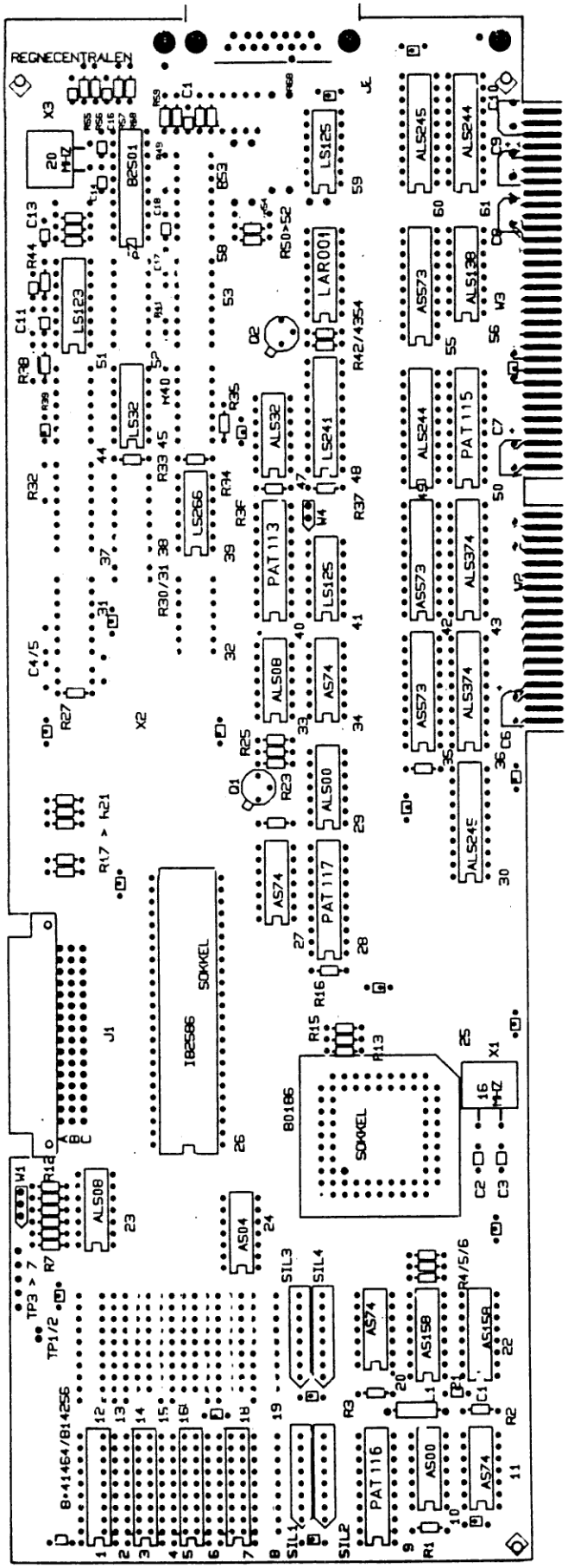


UNIT	DESIGN JKA	SYSTEM MEMORY ACCESS	4
DWG. NO.	DRAWN AGA 870617		



UNIT	DESIGN JKA	AT-BUS ARBITRATION CYCLE	5
DWG. NO.	DRAWN AGA 870617		

4.6 Assembly drawing



4.7 Plugs

4.7.1 AT bus connector

A side (component side)

I/O Pin	Signal Name
A1	-I/O CH CK (not connected to LAN452
A2	SD7
A3	SD6
A4	SD5
A5	AD4
A6	SD3
A7	SD2
A8	SD1
A9	SD0
A10	-I/O CH RDY
A11	AEN
A12	SA19
A13	SA18
A14	SA17
A15	SA16
A16	SA15
A17	SA14
A18	SA13
A19	SA12
A20	SA11
A21	SA10
A22	SA9
A23	SA8
A24	SA7
A25	SA6
A26	SA5
A27	SA4
A28	SA3
A29	SA2
A30	SA1
A31	SA0

B side (solder side):

I/O Pin	Signal Name	
B1	GND	
B2	RESET DRV	
B3	+5V	
B4	IRQ9	
B5	-5V	
B6	DRQ2	
B7	-12V	
B8	OWS	(not used)
B9	+12V	
B10	GND	
B11	-SMEMW	(not used)
B12	-SMEMR	(not used)
B13	-IOW	
B14	-IOR	(not used)
B15	-DACK3	(not used)
B16	DRQ3	(not used)
B17	-DACK1	(not used)
B18	DRQ1	(not used)
B19	-REFRESH	
B20	SYSCLK	
B21	IRQ7	(not used)
B22	IRQ6	(not used)
B23	IRQ5	(not used)
B24	IRQ4	(not used)
B25	IRQ3	(not used)
B26	-DACK2	(not used)
B27	T/C	(not used)
B28	BALE	(not used)
B29	+5V	
B30	OSC	(not used)
B31	GND	

C side (component side):

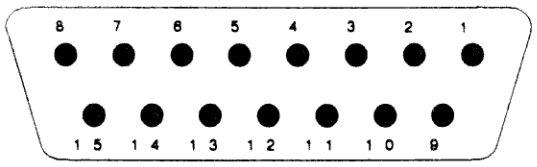
I/O Pin	Signal Name
C1	SBHE
C2	LA23
C3	LA22
C4	LA21
C5	LA20
C6	LA19
C7	LA18
C8	LA17
C9	-MEMR
C10	-MEMW
C11	SD8
C12	SD9
C13	SD10
C14	SD11
C15	SD12
C16	SD13
C17	SD14
C18	SD15

D side (solder side):

I/O Pin	Signal Name	
D1	-MEMCS16	(not used)
D2	-I/O CS16	(not used)
D3	IRQ10	
D4	IRQ11	(not used)
D5	IRQ12	(not used)
D6	IRQ15	(not used)
D7	IRQ14	(not used)
D8	-DACK0	
D9	DRQ0	
D10	-DACK5	(not used)
D11	DRQ5	(not used)
D12	-DACK6	(not used)
D13	DRQ6	(not used)
D14	-DACK7	(not used)
D15	DRQ7	(not used)
D16	+5V	
D17	-MASTER	
D18	GND	

4.7.2 LAN Connector

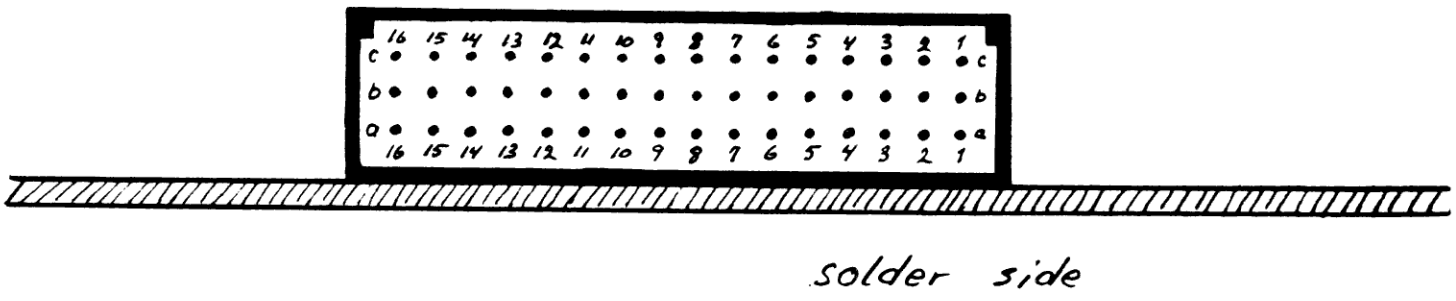
The LAN connector seen from the rear:



Pin	Signal Name
1	no connection
2	COLDET+
3	TRANSMIT+
4	No connection
5	RECEIVE+
6	GND
7	No connection
8	No connection
9	COLDET-
10	TRANSMIT-
11	No connection
12	RECEIVE-
13	+12V
14	No connection
15	No connection

4.7.3 Debug Board Connector

The Debug board Connector seen from the top.



Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	AD0	B1	+5V	C1	-DEBUG BOARD
A2	AD1	B2	0V	C2	-DEBUG RESET
A3	AD2	B3	+12V	C3	-PROMSEL
A4	AD3	B4	-12V	C4	-PCS1
A5	AD4	B5	CPURESET	C5	-DBINT
A6	AD5	B6	0V	C6	DBAREADY
A7	AD6	B7	A16	C7	-RXINT
A8	AD7	B8	A17	C8	IDENT1
A9	AD8	B9	A18	C9	IDENT2
A10	AD9	B10	A19	C10	IDENT3
A11	AD10	B11	0V	C11	-BHEN
A12	AD11	B12	OBALE	C12	0V
A13	AD12	B13	-WR	C13	-S0
A14	AD13	B14	-RD	C14	-S1
A15	AD14	B15	0V	C15	-S2
A16	AD15	B16	+5V	C16	-CPUCLK

5. REFERENCES

(1) Microsystem Components Handbook,
Vol I+II, INTEL, 1986.

(2) Microcommunications Handbook,
INTEL 1986.

(3) Technical Reference, Personal Computer AT
IBM 1984.

(4) Specifikation af Debug-kort,
Okt. 86,
Willian S. Jacobsen.

(5) SEEQ Data Book, SEEQ Technology, 1985