RC900

MUX451/MXX451 Multiplexer

Hardware reference manual

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PN: 99200389

RC Computer

Keywords:
MUX451, MXX451, Multiplexer for satellite connection, Multiplexer extension, RC950

Abstract:
This paper contains a hardware description of the MUX451 and the MXX451. The MUX451 is provided with an IBM-AT bus interface and two V.24 communication lines. MXX451 is an extension to the MUX451. The MXX contains six additional V.24 lines.

Date:
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This manual describes the MUX451 and the MXX451 boards. The MUX451 board is an intelligent satellite adapter (multiplexer) with IBM-AT I/O bus interface and 2 asynchronous communication channels. The MXX451 is an extension to the MUX451 which contains the hardware for 6 additonal communication channels.

The MUX451 is provided with a 80186 CPU and 128 Kbytes of local RAM. The MUX451 can become a master on the AT I/O bus, thus providing the board with the facility to read from and write to the system board memory. One DUART (Dual Asynchronous Receiver/ Transmitter) is used on the MUX451 thus providing two V.24 channels. MXX451 contains three additional DUART`s.

The manual is divided into basically two sections: The first section contains a short description and a short specification of the board. The second section contains a detailed hardware description of the board.

The necessary programming information of the MUX451 board can be found in "Programmer`s Technical Guide" (ref. 5).

Fig. 1 shows a block diagram of the MUX/MXX451 boards.

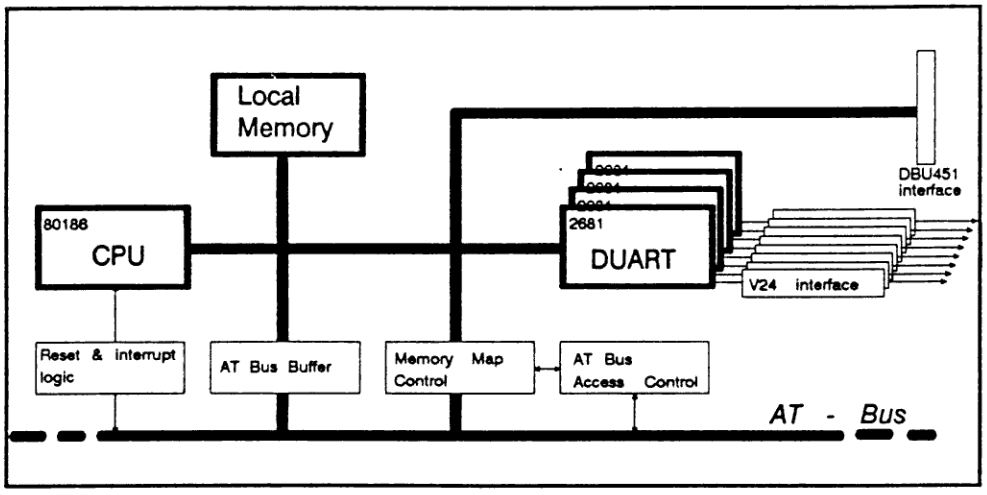


Fig. 1 Block diagram of MUX/MXX451

2. GENERAL INFORMATION

2.1 Short Description

The CPU is an 8MHz INTEL 80186 processor, see (1). The CPU is integrated with:

- 3 programmable timer.
- 5 interrupt input lines and an interrupt controller.
- Programmable waitstate generator.
- 2 programmable DMA controllers.
- 7 programmable I/O chip select lines.

The Local Memory consists of 128 Kbyte DRAM. No PROM is available on the MUX451 board. The Local Memory can only be accessed by the 80186 CPU.

The upper most 128K byte of the 80186 address space is mapped onto the system memory through the AT bus. The Boot Memory Map Register controlles the mapping of the upper most 64 Kbyte. The Buffer Memory Map Register controlles the mapping of the next 64 Kbyte.

After reset the 80186 starts executing code in the system memory in the Boot Memory address space.

The DUART on the MUX and the DUART`s on the MXX are accessed by the 80186 via a number of I/O-addresses.
Two 9p D-connectors on the MUX451 are used for satellite connection. Six additional satellites can be connected to the MXX451.

A 48 pol EURO connector on the MUX451 provides for testing the board with a Debug Board, DBU451, see (4). The DBU451 is provided with EPROMs. After reset, which may be generated by the DBU451 board, the 80186 may execute the code placed in these EPROMs.

Through the Reset and Interrupt Logic the MUX451 can generate an interrupt on the system board and the System Board can interrupt the MUX451 board. The system board can also generate a reset signal to the MUX451 board.

A maximum of two MUX boards can be mounted in the AT slots.

2.2 Specification

2.2.1 Performance Specifications

80186 CPU clock	: 8 MHz
Data Bus Size	: 16 bits
EPROM	: none
On board RAM capacity (Local Memory)	: 128 Kbyte expandable to 896 Kbyte by mounting extra DRAM devices.
Off board Memory	:
Boot Memory	: 64 Kbytes of the system memory.
Buffer Memory	: 64 Kbyte of the system memory.
Memory address range	:
Local Memory	: 00000H-1FFFFH
Boot Memory	: F0000H-FFFFFH
Buffer Memory	: E0000H-EFFFFH

2.2.2 Environmental Specifications

Operating Temperature	: $0^{o}C$ - $40^{o}C$.
Relative Humidity	: 20% - 80% (non condensing).

2.2.3 Physical Specification

MUX

Width	: 121.80 mm
Length	: 333.25 mm
Height	: 20 mm

MXX

Width	: 107.00 mm
Length	: 162.00 mm
Height	: 20 mm

2.2.4 Power Specification

	MUX
Power Dissipation	: 7.5 W
Vcc	: +5V +/- 5% (1.5 A max.)
+Vdd	: +12V +/- 10% (25mA max.)
-Vdd	: -12V +/- 10% (15mA max.)
	MUX & MXX
Power Dissipation	: 10.5 W
Vcc	: +5V +/- 5% (1.7 A max.)
+Vdd	: +12V +/- 10% (100mA max.)
-Vdd	: -12V +/- 10% (60mA max.)

2.3 Installation

The MUX451 board can be plugged into any of the AT-I/O slot. If a MUX451 is allready plugged into one of the slots a jumper must be mounted on one of the MUX451 boards. The jumper must be mounted at the position named S1 on the board. A maximum of two MUX boards can be installed in the AT slots.

3. TECHNICAL DESCRIPTION

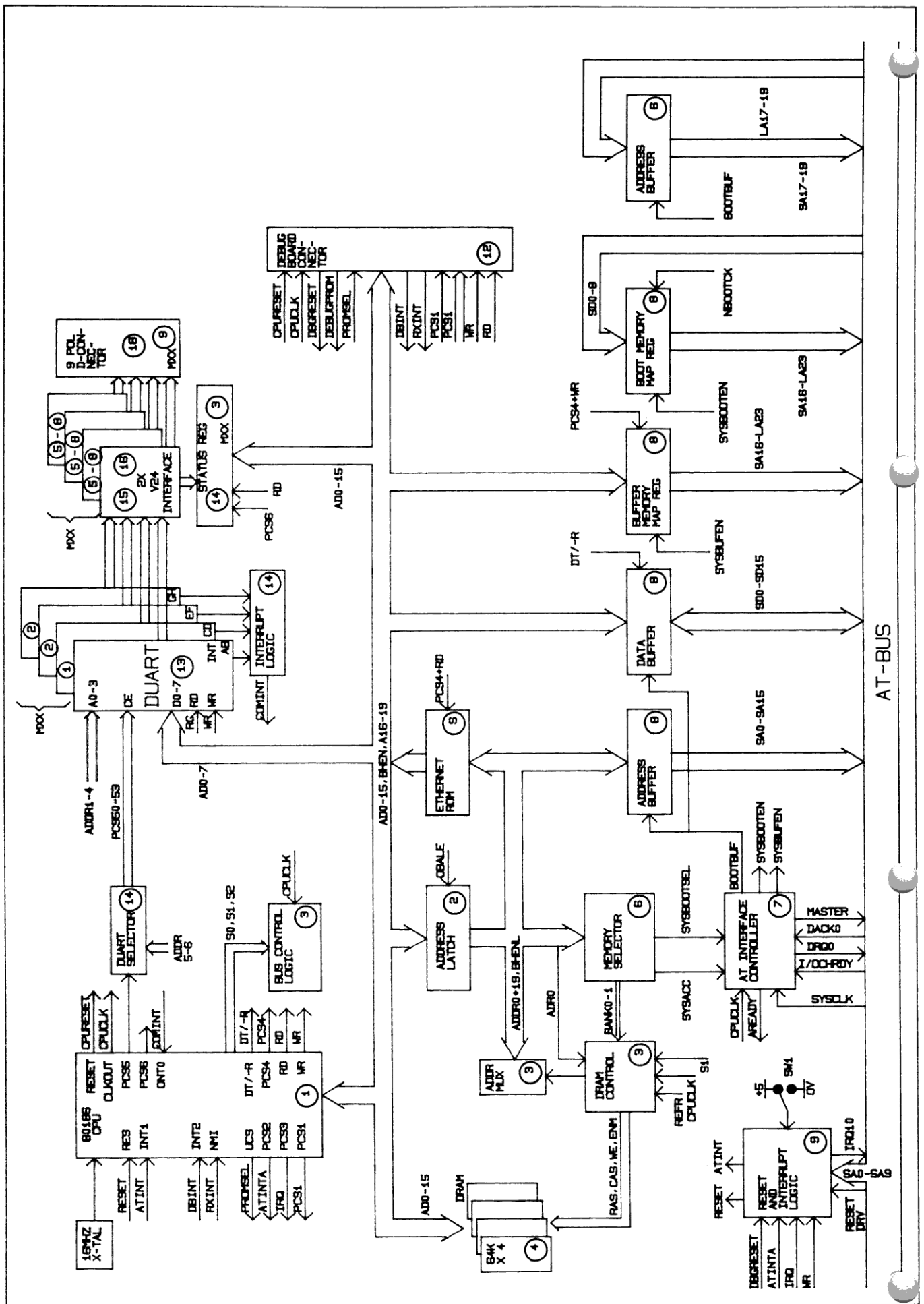
3.1 Introduction

This chapter contains a detailed technical description of the MUX451 hardware. Section 3.2 gives a survey of the MUX451 board. Section 3.3 contains the electrical diagrams of the MUX451 and should be readen together with section 3.2. Section 3.4 contains description of the MUX451 PAL's. Section 3.5 contains some relevant timing diagrams.

A description of the LSI components used is not given in this chapter. It is recommended that the reader consults the relevant data sheets (see chapter 4).

3.2 Short Technical description

Fig. 2 shows a more detailed block diagram of the MUX/MXX451 board. Some of the most important signal names are shown in fig. 2 and can be found in section 3.3. The numbers in circles refer to a diagram page number in section 3.3 where the group of logic can be found as electrical diagrams. In the rest of this section we refer to these diagram pages.



UNIT MUX451	DESIGN THU
DWG. NO.	DRAWN LIL 880316

Fig. 2 Detailed block diagram

3.2.1 The MUX diagram

Diagram page 1 shows the 80186 CPU. The 80186 CPU are connected to provide ALE, WR and RD signals (no queue status data). A 16 MHz x-tal is connected to the 80186 providing the board with an 8 MHz CPU clock.

Diagram page 2 shows the Address Latch.

Diagram page 3 contains three logic units:

- Bus Controll Logic
- DRAM Controller and
- DRAM Address Multiplexer.

The Bus Controll Logic generates the address latch enable signal 'OBALE' and an On Board Command signal for the Memory Selector and the DRAM Controller.

The DRAM Controller consists of a PAL16R6A device. the DRAM Controller generates controll signals to the DRAM devices:

- Row Address Strobe ('RAS0', 'RAS1')
- Column Address Strobe ('CAS')
- Write Enable ('WEHI', 'WELO')
- Enable Memory ('ENMEM0', 'ENMEM1')

Enable Memory is active when reading from the Local Memory.

On a request from the 80186 CPU timer0 ('REFR') the DRAM controller generates a 'CAS before RAS refresh' cycle to the DRAM devices. The DRAM devices contains an internal refresh counter. A refresh cycle can occur whenever the 80186 CPU is not accessing the Local Memory.

The DRAM Address Multiplexer generates the Row and Column addresses from the latched 16 addresses.

Diagram page 4 shows a Local Memory with 64Kx4bit DRAM devices. Only DRAM devices with even IC numbers are mounted providing the MUX451 with 128 Kbyte of local memory.

Diagram page 5 shows a Local Memory with 256Kx4bit DRAM devices. These devices are not mounted on the MUX451 board.

Diagram page 6 shows the serializer ROM and the Memory Selector. The serializer ROM is not mounted on MUX451.

The PAL16L8A constitutes the Memory Selector and the function can be described with the following table:

-DEBUG -OBCMD	PROM	A19	A18	A17	A16	-BANK0	-BANK1	-SYS ACC	-SYSBOOT SEL	
H	X	X	X	X	X	H	H	H	H	No access
L	X	0	X	X	X	L	H	H	H	80186 access
L	X	1	1	0	X	H	L	H	H	To Local Memory
L	X	1	1	1	0	H	H	L	H	80186 access to Buffer Memory
L	H	1	1	1	1	H	H	L	L	80186 access to Boot Memory
L	L	1	1	1	1	H	H	H	H	80186 access to Debug Board PROM

Notes: X indicates a dont care state
1 is equal to H (High) state
0 is equal to L (Low) state.

The 'SYSMENEN' enables two buffers, controlling the AT bus read and write signals, when the MUX451 board has gained access to the AT bus ('MASTEREN' is active). When the 80186 CPU has gained access to the AT bus ('MASTEREN' = L) and is reading from or writing to the Local Memory the PAL will activate the refresh signal on the AT bus ('-,REFRESH = L'). Refreshing the System Memory is done when the 80186 is activating the '-,LOCK' signal.

Diagram page 7 shows the AT Interface Controller. When the 80186 access the System Memory the following sequence will occure:

1. '-,SYSACC' becomes active (L).
2. '-,DRQ' is activated by the PAT113.
   The 'AREADY' becomes active.
3. If another MUX board has not activated the DRQ5 signal on the AT bus this MUX board will clock the '-,DRQ' signal through U27 and activate the DRQ5 signal on the AT bus.

4. The system board answer by activating the '-,DACK5' signal which is gated into the MUX451 board and the '-,OBDACK' signal becomes active.
5. 'OBDACK' is latched and the MUX451 board will activate the 'MASTER' signal on AT bus and the 'MASTEREN' signal on the MUX451 board.
6. The 80186 can now read from or write to the System Memory.
7. '-,SYSACC' is deactivated by the 80186 and the 'DRQ5' on the AT bus is also deactivated.

If the '-,LOCK' signal is activated by the 80186 the MUX451 will occupy the AT bus in more than one memory cycle.

Diagram page 8 contains address buffers and data buffers interfacing the AT address and data bus.

Diagram page 9 shows the Reset and Interrupt Logic that consist of a PAL16L8 and a 74LS138. A number of latches are implemented in the PAT133 and these latches can be set and reset by writing to I/O addresses from the 80186 CPU and from the System board. The following table shows how:

Signal	Set by (Writing)	Reset by (Writing)
ATINT (Interrupt to 80186)	System board on I/O address 317H(S1=L) or 313H (S1=H)	80186 with PCS2 asserted (I/O address 100H-17FH)
IRQ12 (interrupt to system board)	80186 with PCS3 (I/O address 180H-1FFH)	System board on I/O address 316H (S1=L) or 312H (S1=H).
RESET	System board on I/O address 315H (S1=L) or 311H (S1=H) or by System board RESET DRV signal	System board on I/O address 314H (S1=L) or 310H (S1=H) or by Debug board.

When the system board is deactivating the 'RESET' signal a clock signal will be generated to the Boot Memory Map register and this register will thus be loaded by the system board.

Diagram page 10 and 11 shows the AT bus connection.

Diagram page 12 shows the Debug Board connection.

Diagram page 13 shows the one DUART located on the MUX451. The clock for the DUART`s located on the MXX is generated from the X-tal.

Diagram page 14 shows the chip select generation for the DUART`s on the MXX.
The interrupts from the DUART`s are OR`ed in order to provide a single DUART interrupt.
An additional register is provided for reading the Carrier Detect (CD) and the Calling Indicator (CI) signals.

Diagram page 15 shows the line-drivers.

Diagram page 16 shows the line-receivers.

Diagram page 17 shows the MXX connector.

Diagram page 18 shows the two V.24 lines.

3.2.2 The MXX diagram

Diagram page 1, 2 and 3 shows the 3 DUART`s.

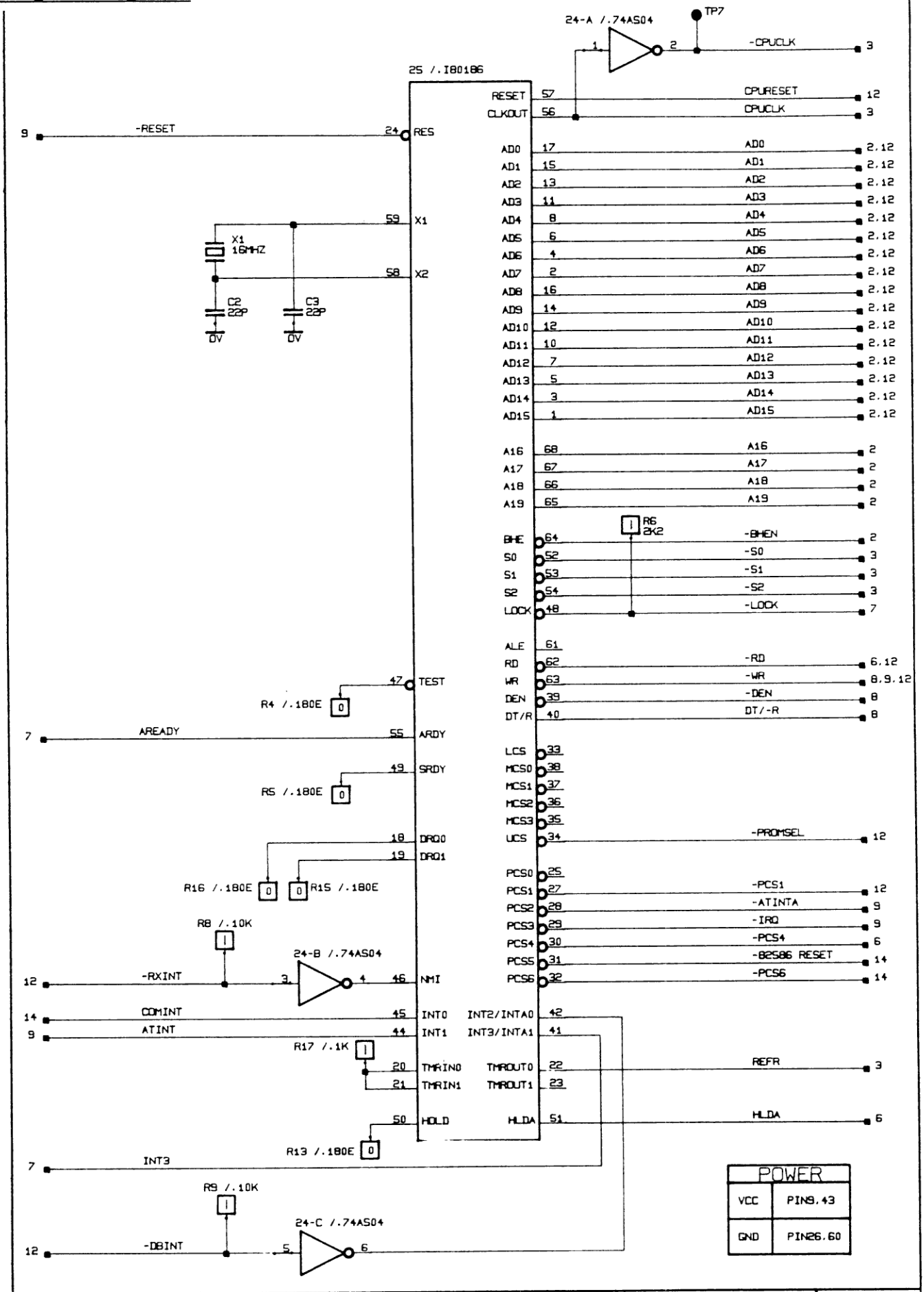
Diagram page 3 shows the additional register used for reading the CI and CD status signals.

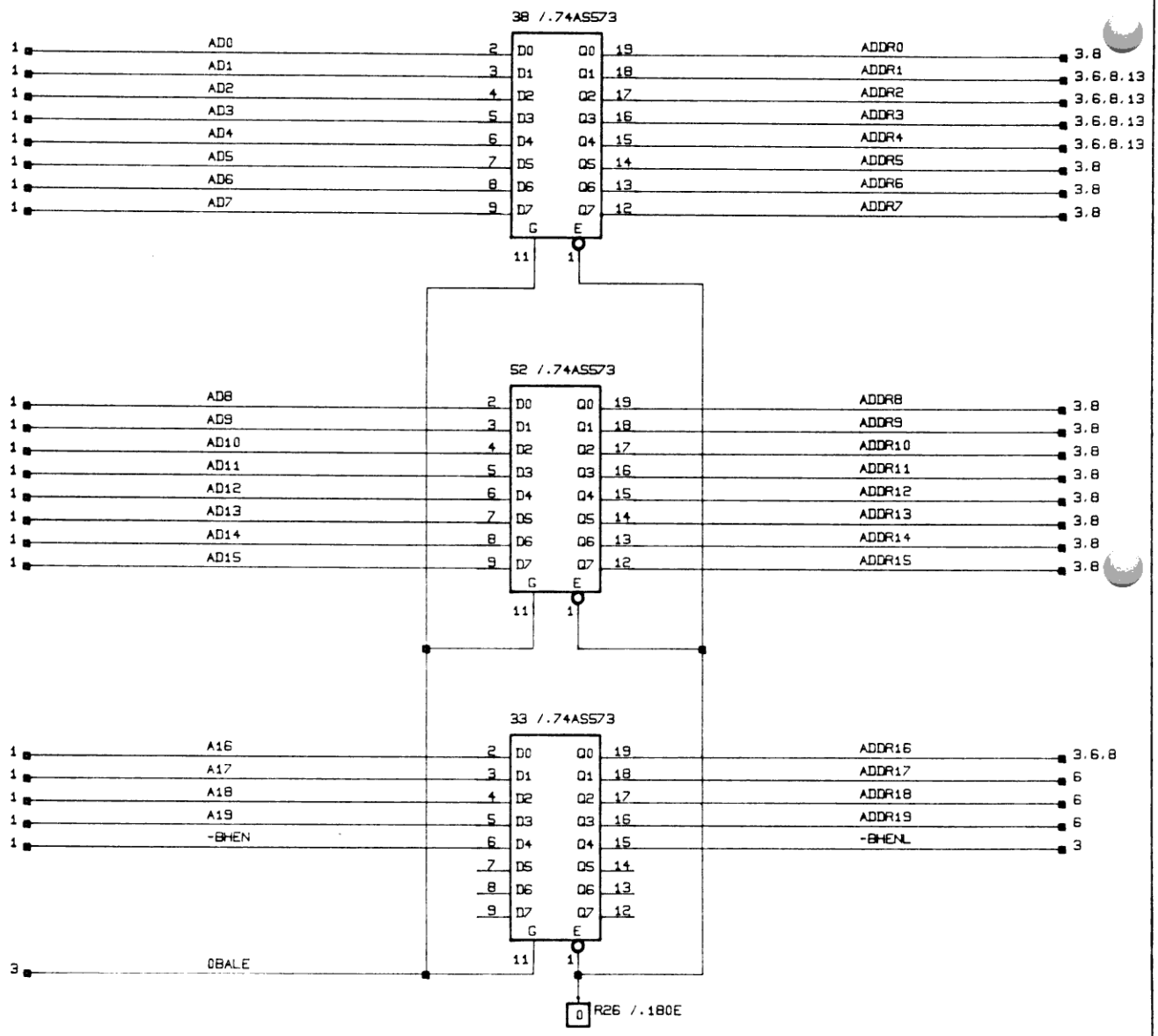
Diagram page 4 shows the MUX-MXX connector.

Diagram page 5,6,7 and 8 shows the line-drivers and the line-receivers.

Diagram page 9 shows the 6 V.24 connectors.

3.3 Logic Diagrams MUX





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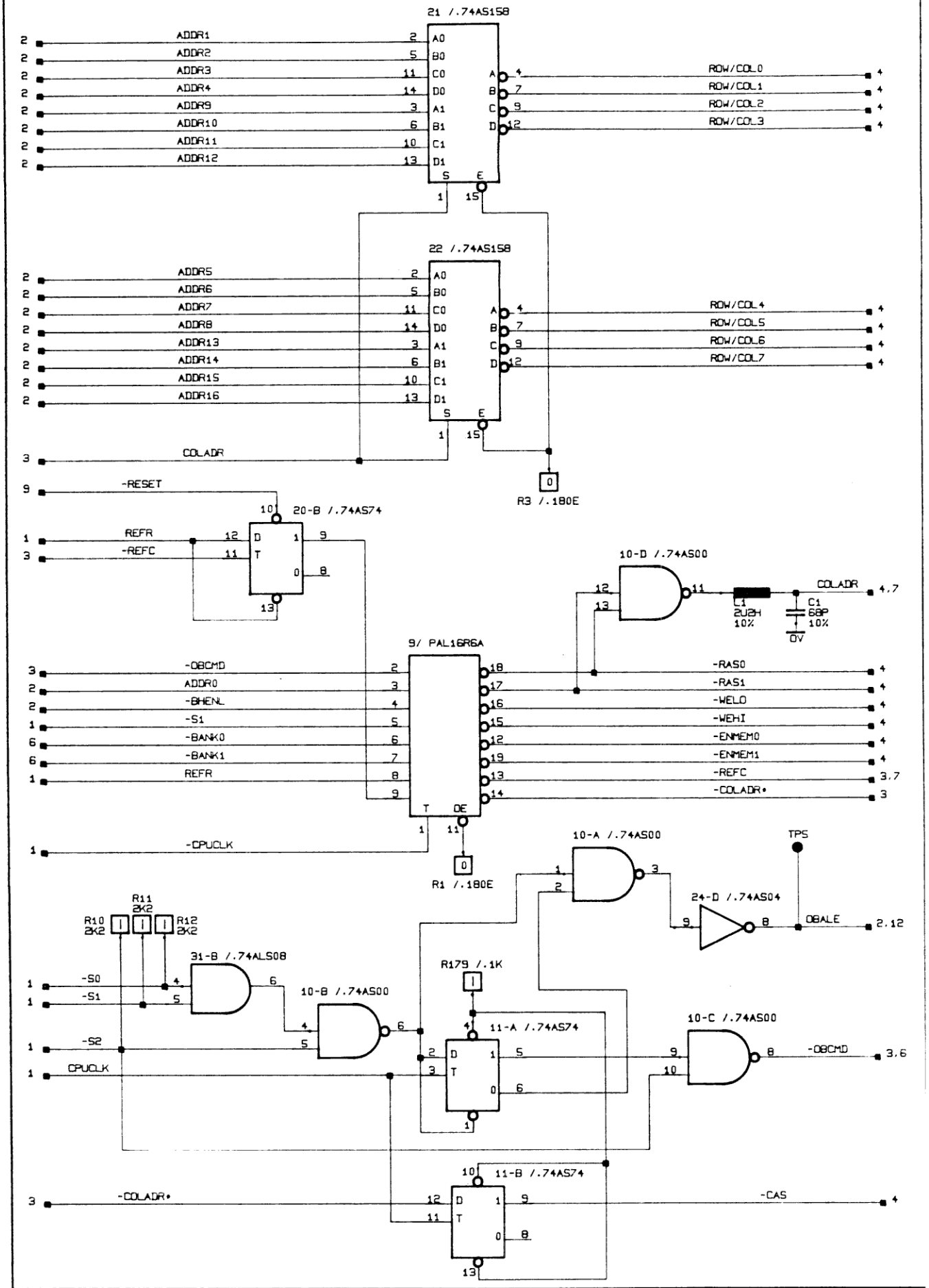

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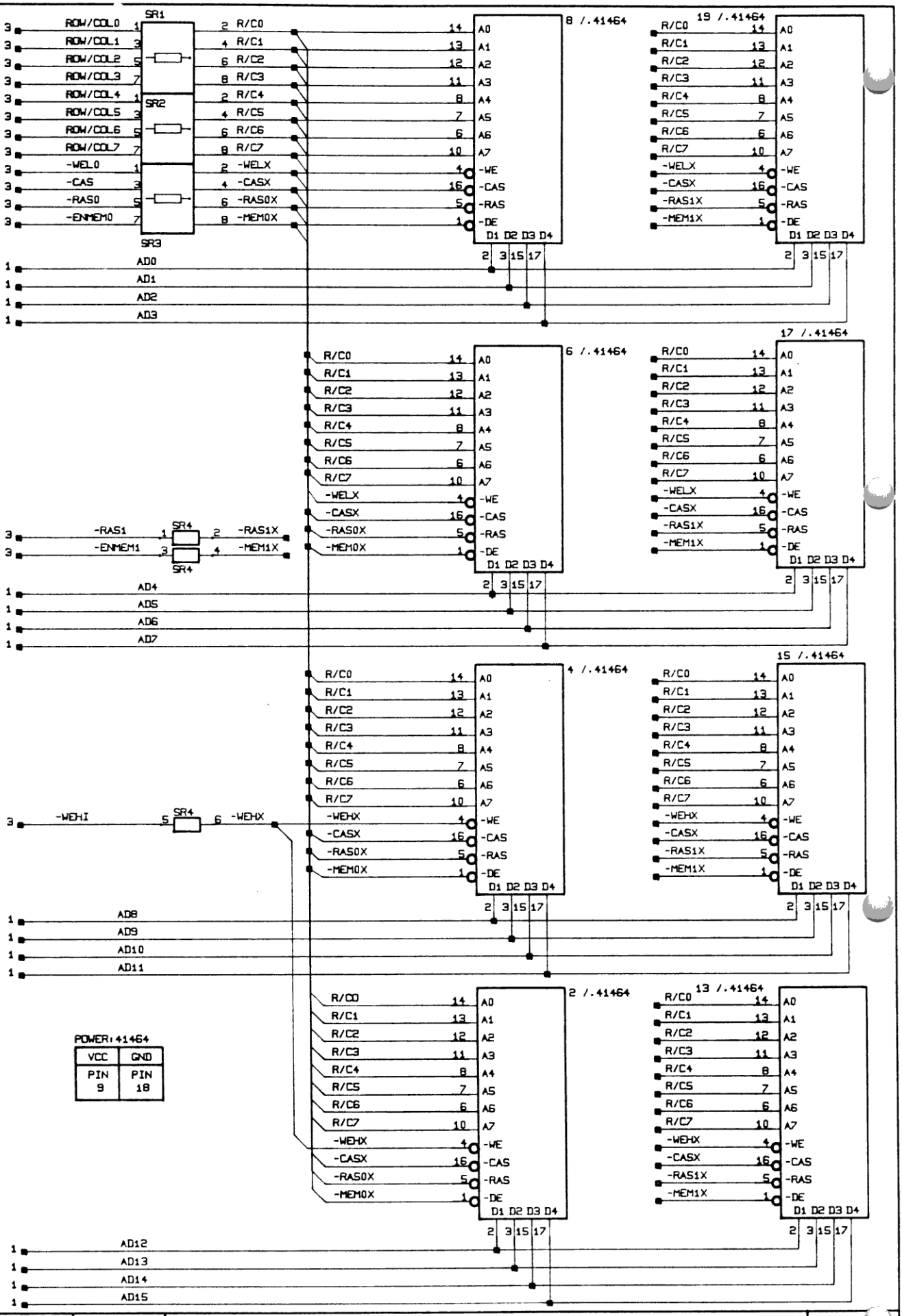
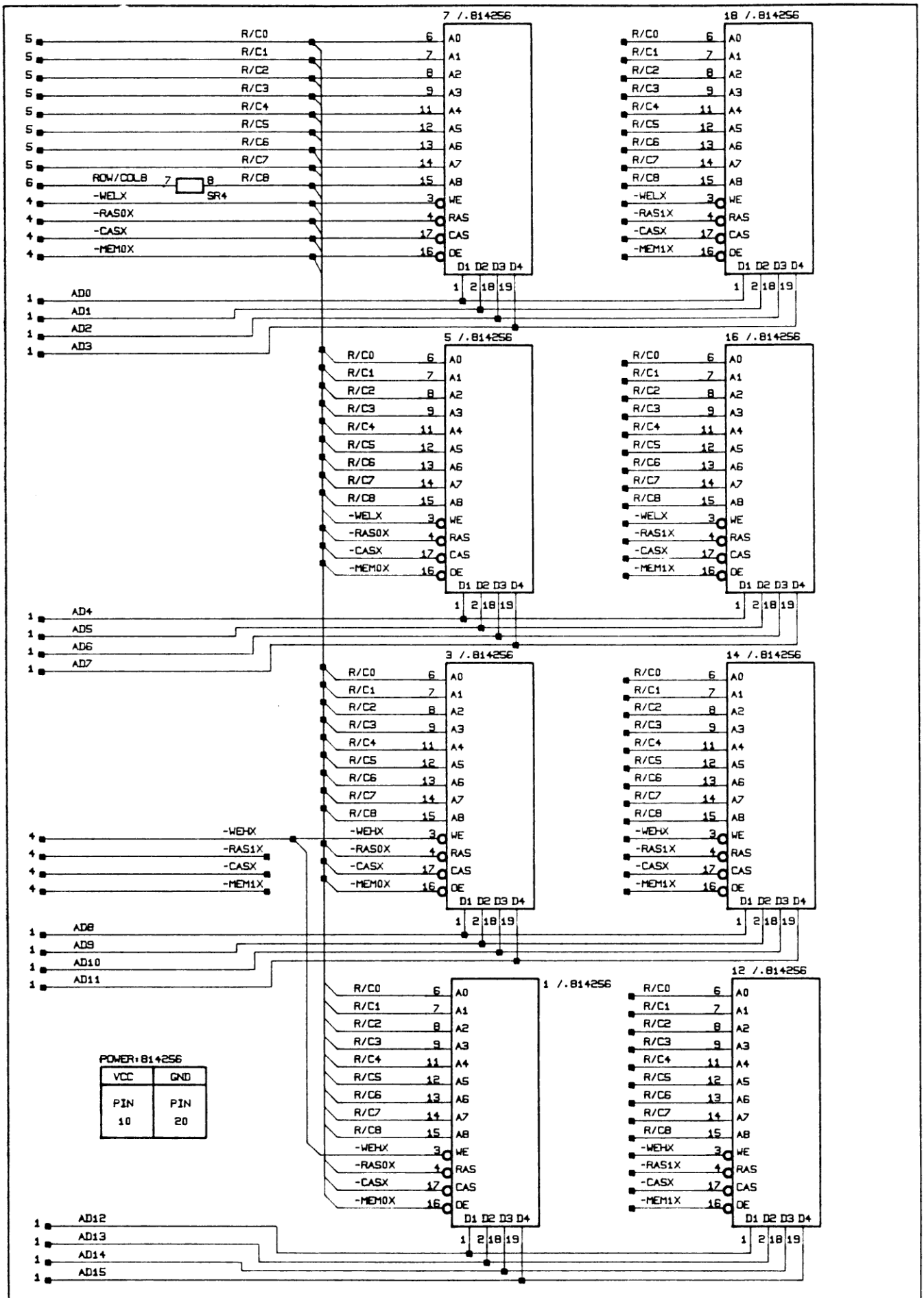
DWG. NO.	DRAWN AGA 870805		


SR1
SR2
SR3
SR4
ROW/COL0
ROW/COL1
ROW/COL2
ROW/COL3
ROW/COL4
ROW/COL5
ROW/COL6
ROW/COL7
-WEL0
-CAS
-RAS0
-ENMEM0
R/C0
R/C1
R/C2
R/C3
R/C4
R/C5
R/C6
R/C7
-WELX
-CASX
-RAS0X
-MEM0X
-RAS1X
-MEM1X
-ENMEM1
-WEHI
-WEHX
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
8 /.41464
19 /.41464
6 /.41464
17 /.41464
4 /.41464
15 /.41464
2 /.41464
13 /.41464
A0
A1
A2
A3
A4
A5
A6
A7
-WE
-CAS
-RAS
-DE
D1 D2 D3 D4
POWER:41464
VCC
GND
PIN 9
PIN 18
UNIT
MUX451
DESIGN
THJ. JKA
DWG. NO.
DRAWN
AGA
870805
128K/256K RAM ARRAY
4



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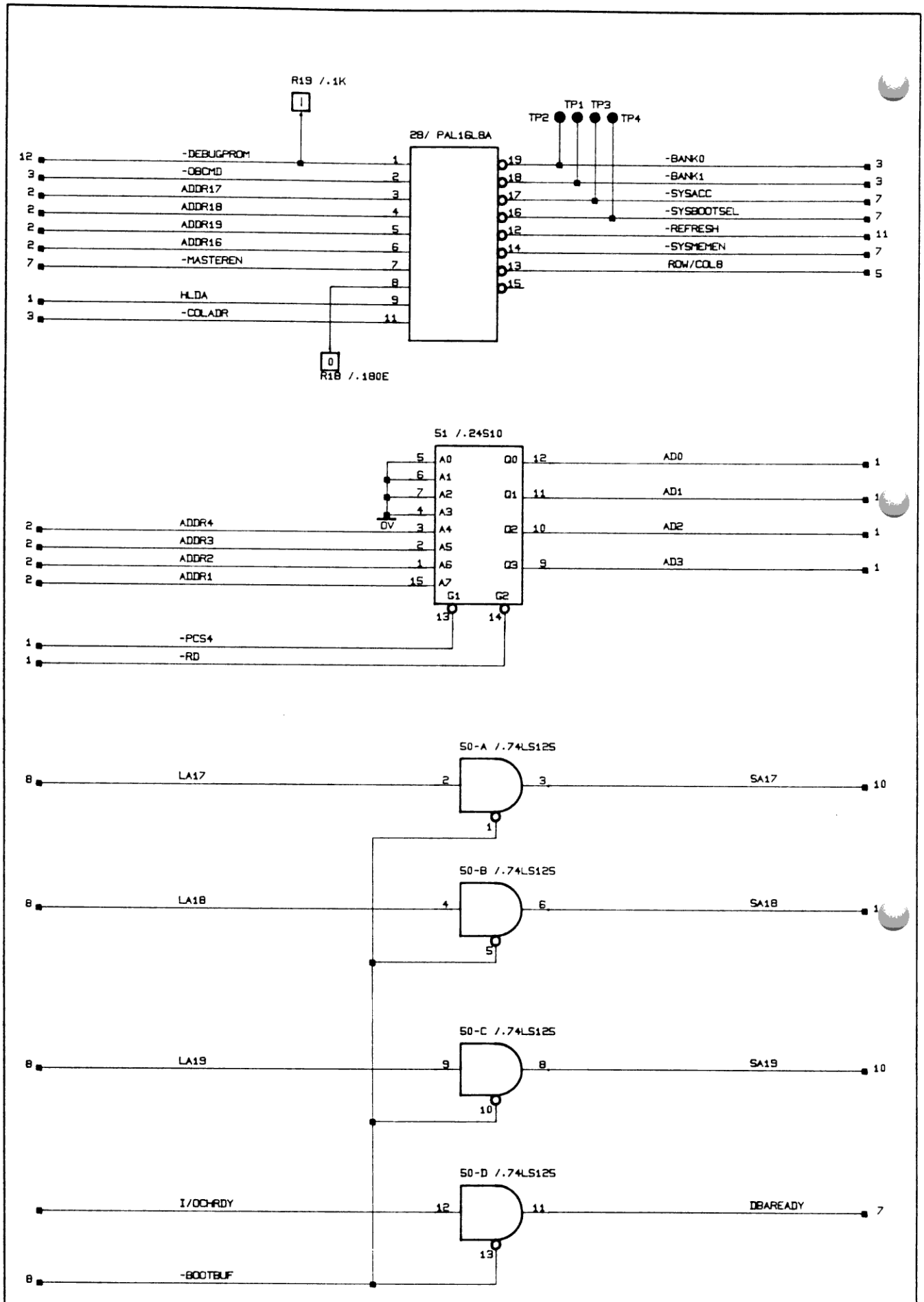

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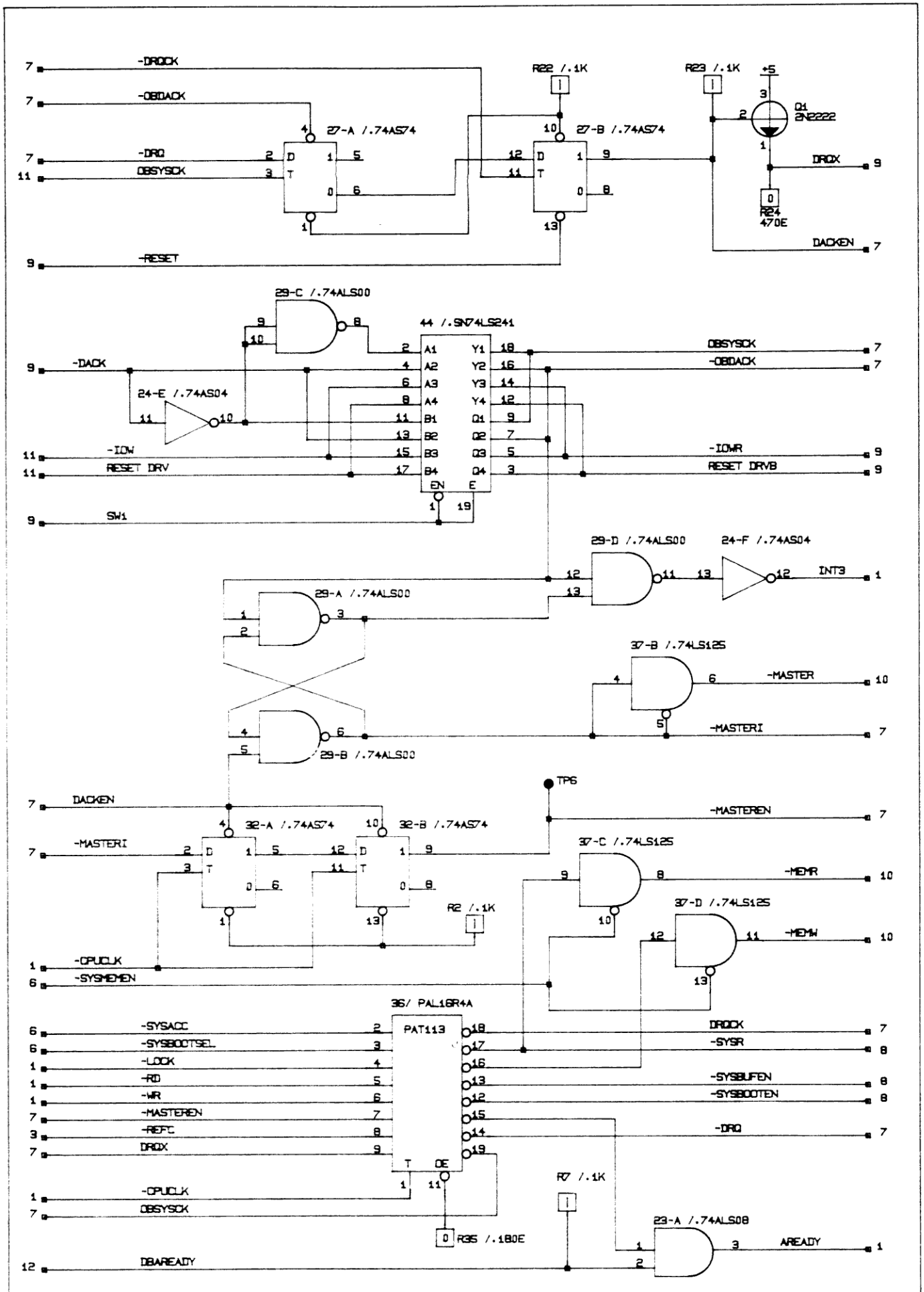

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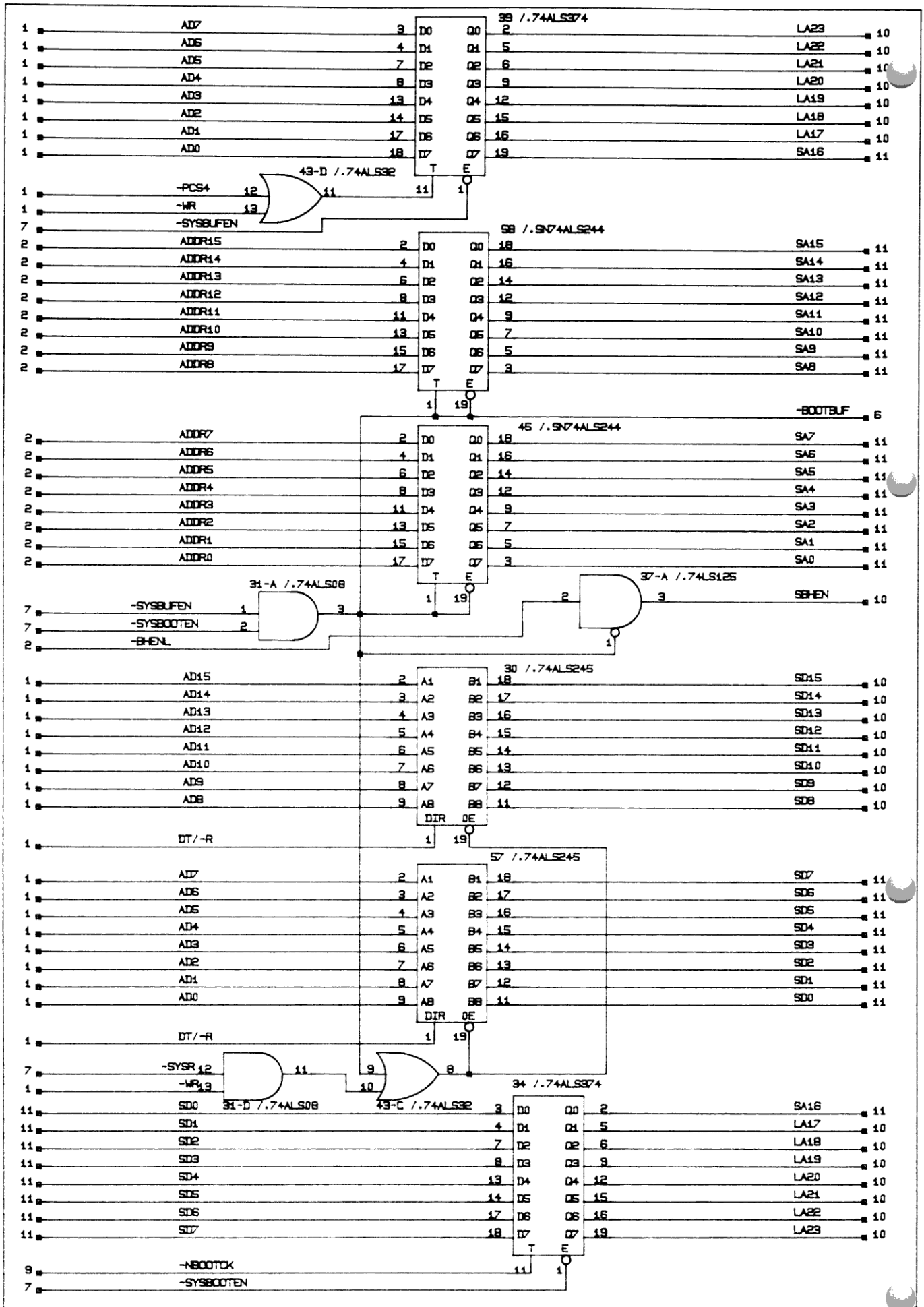

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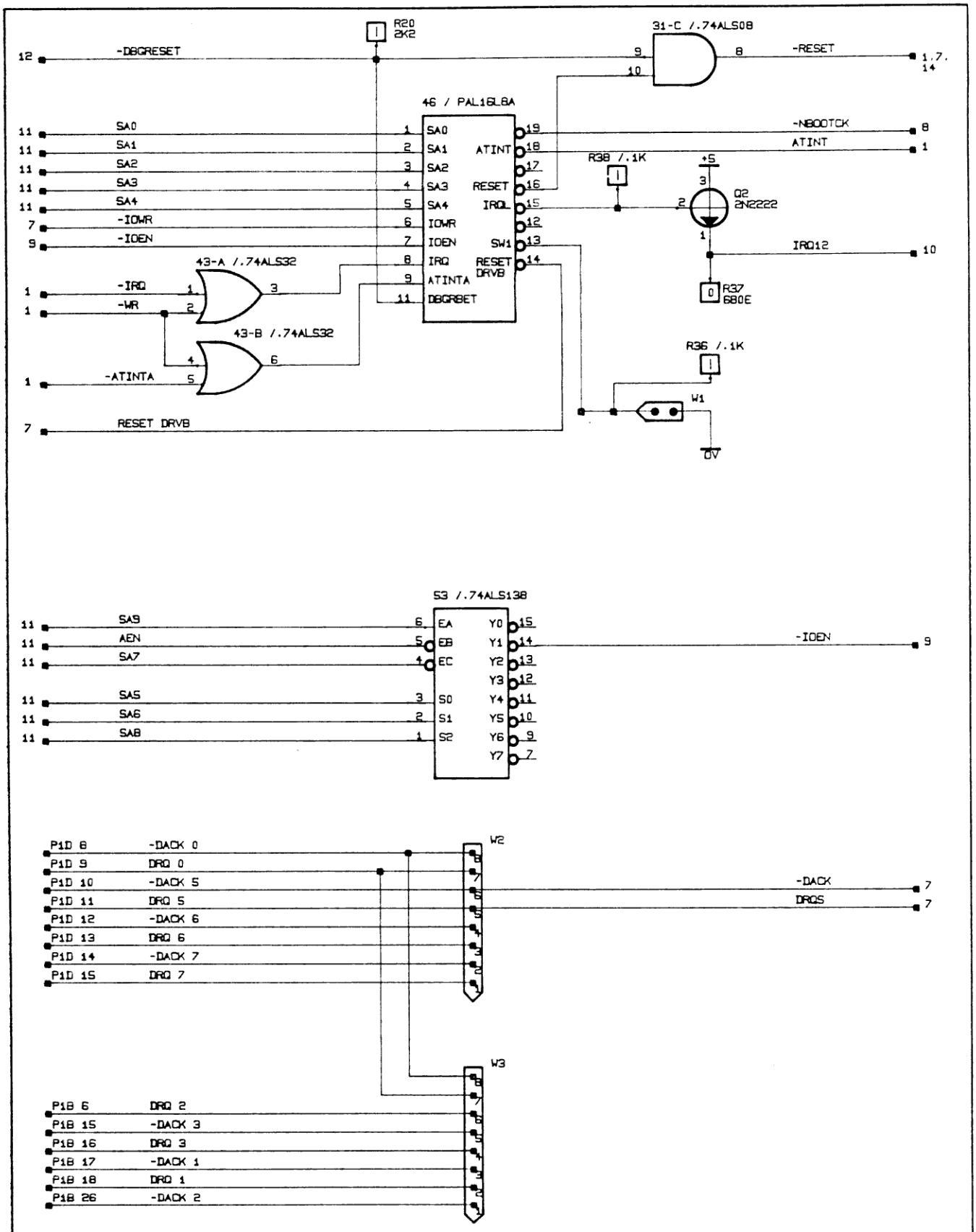

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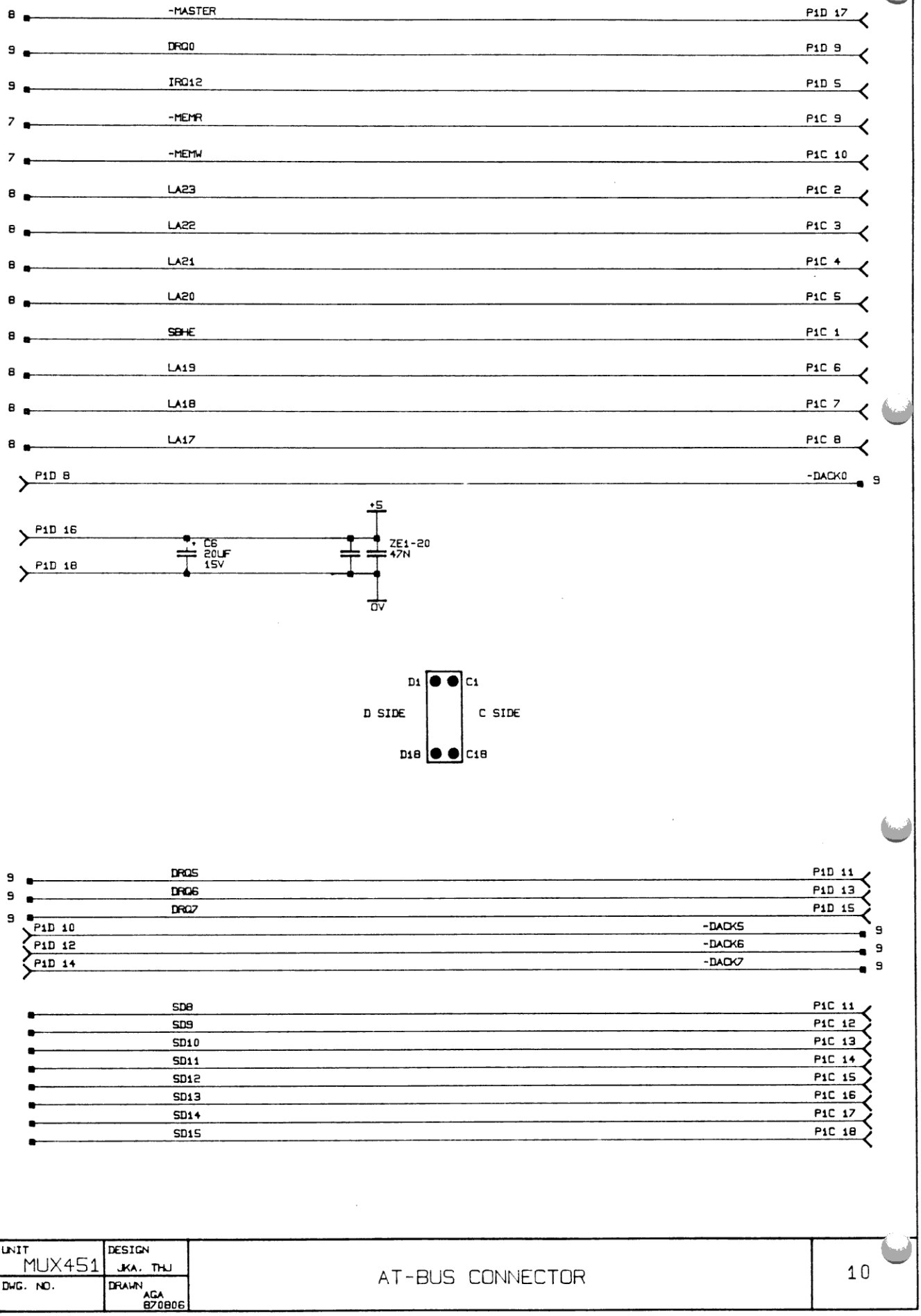

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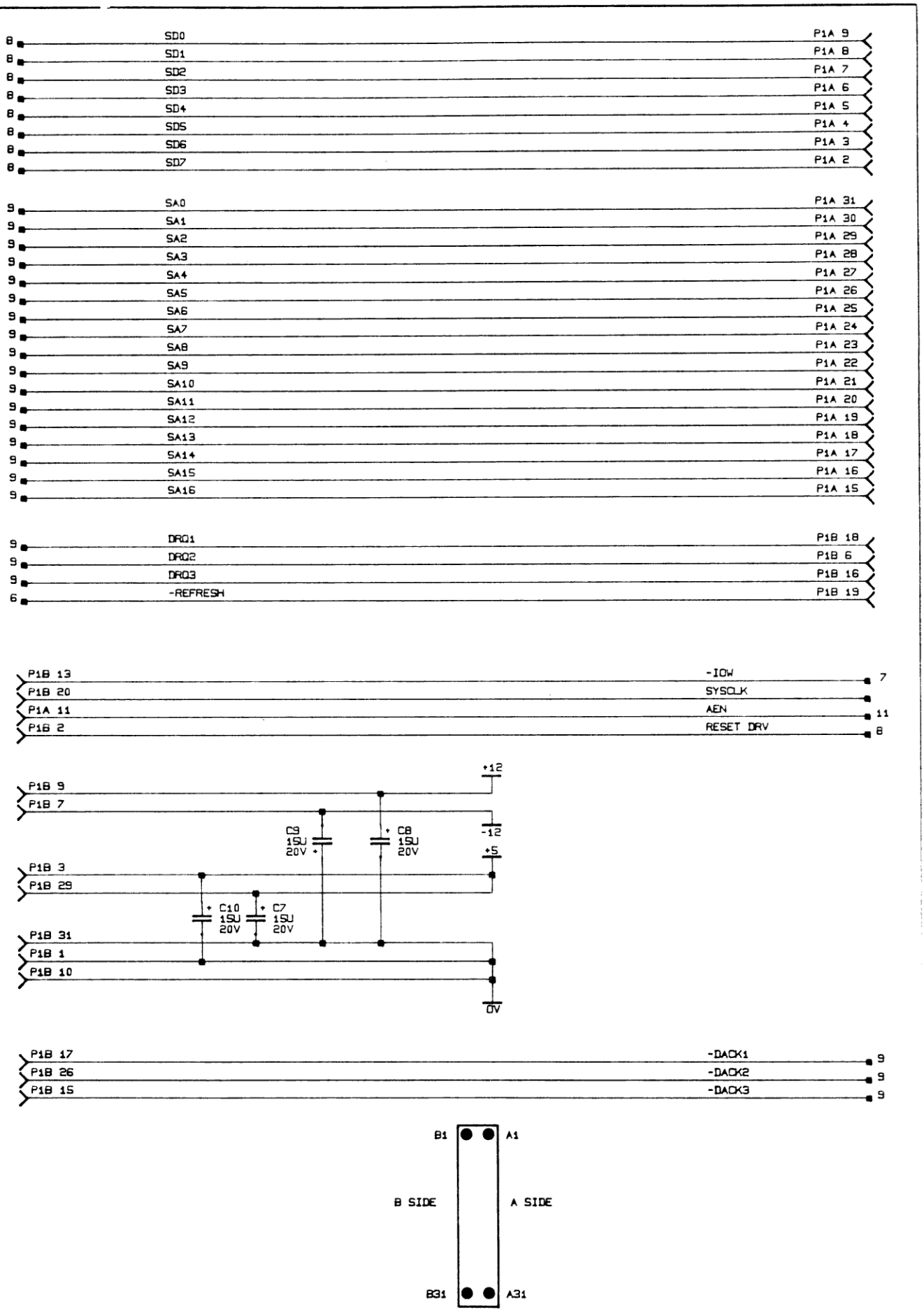

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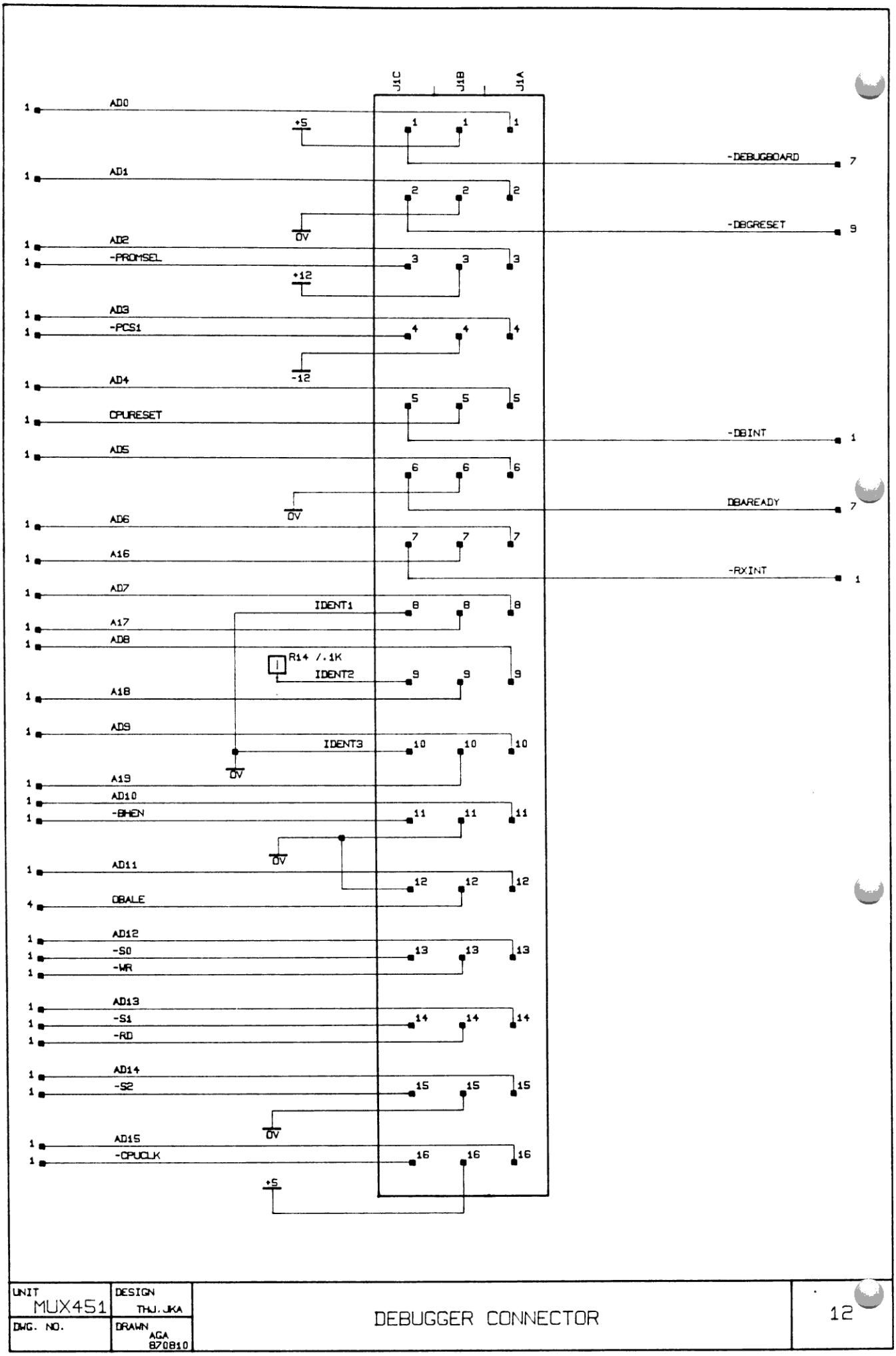

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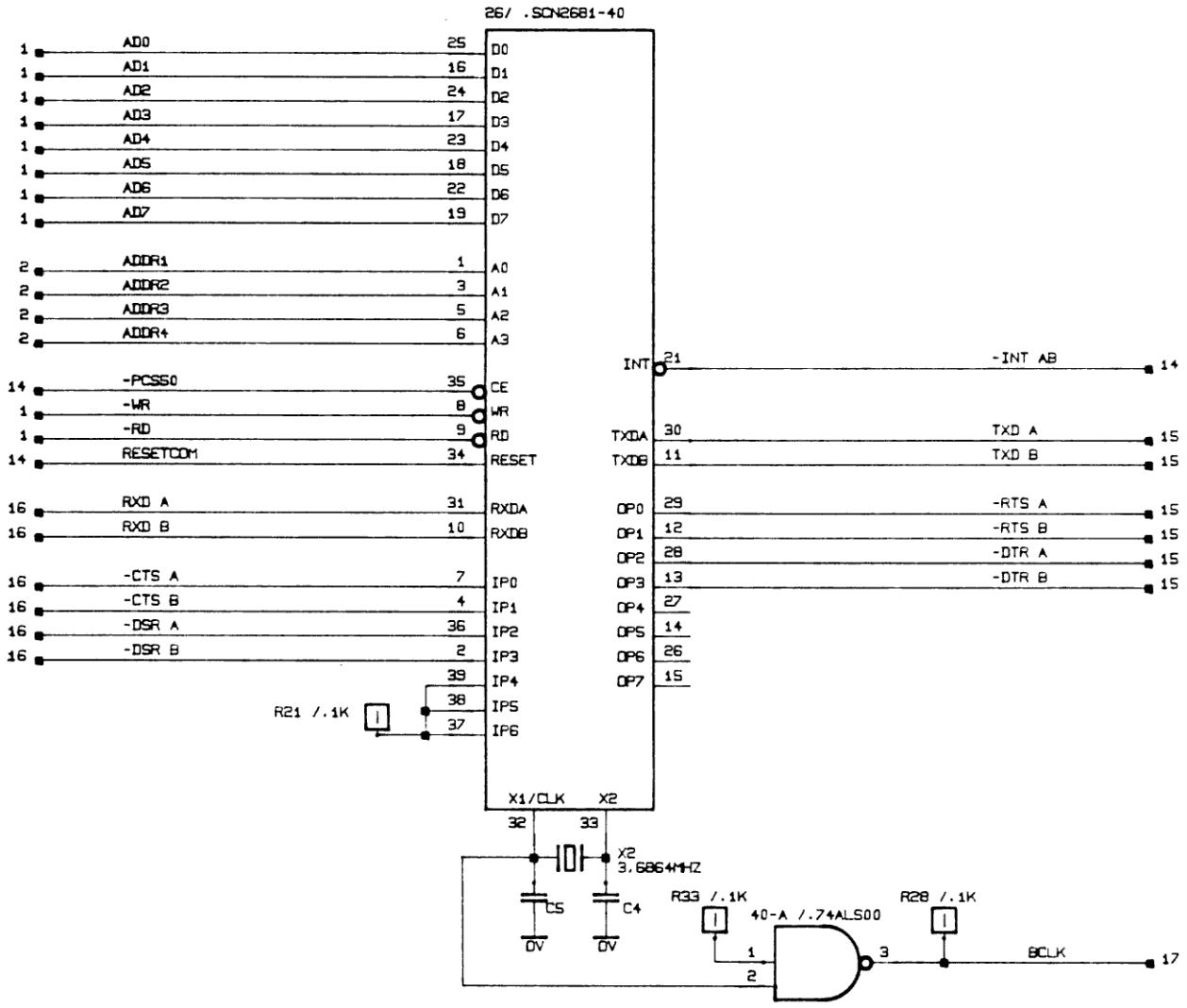

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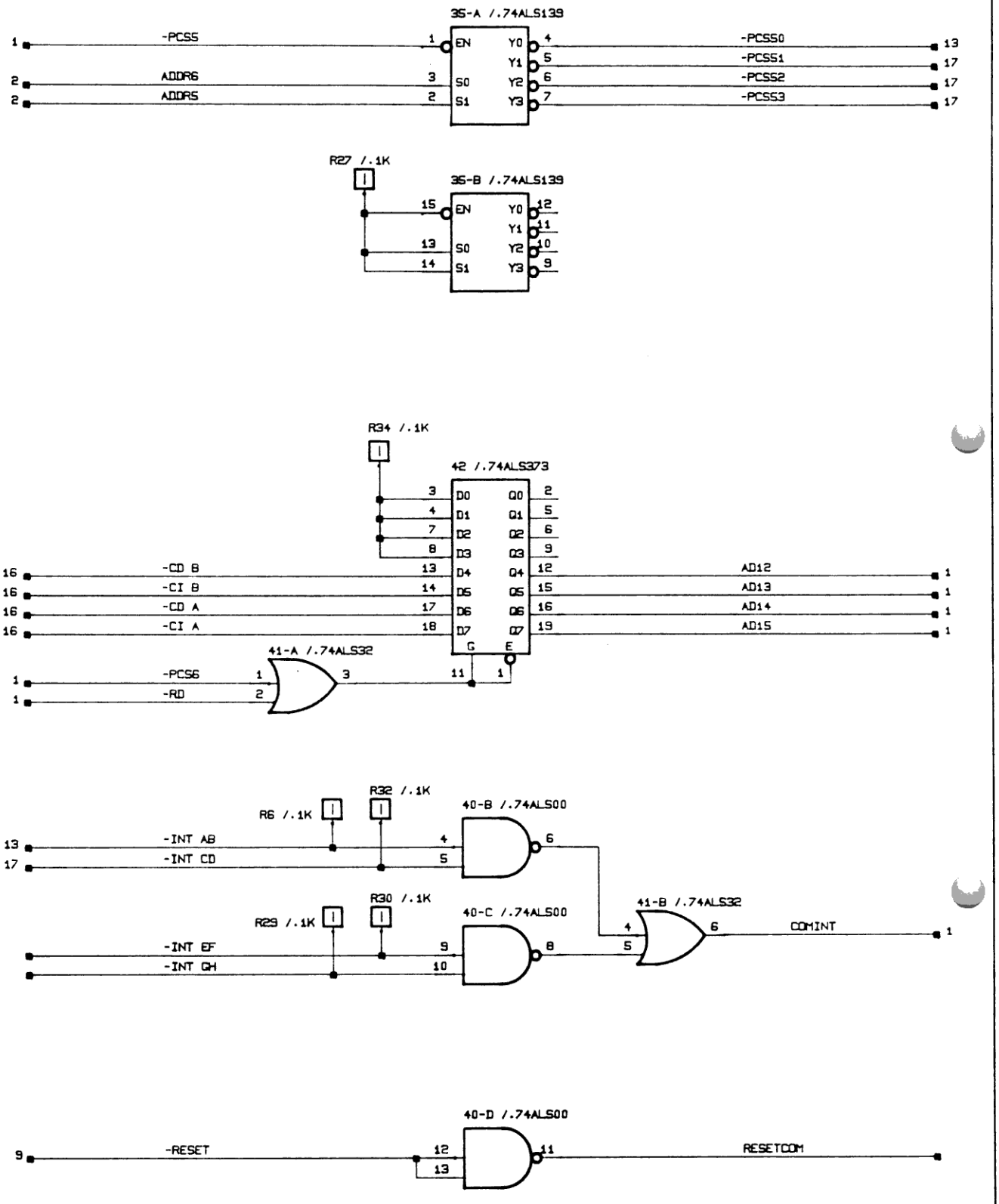

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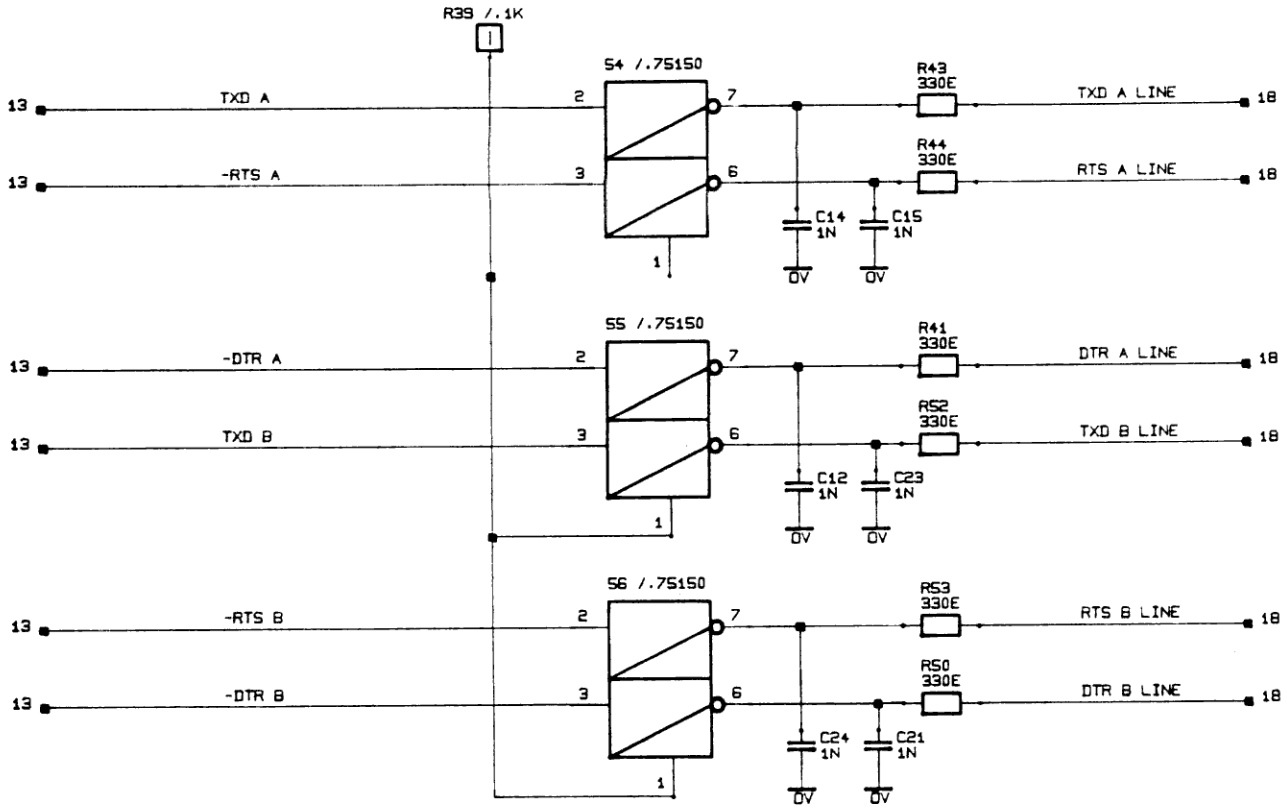

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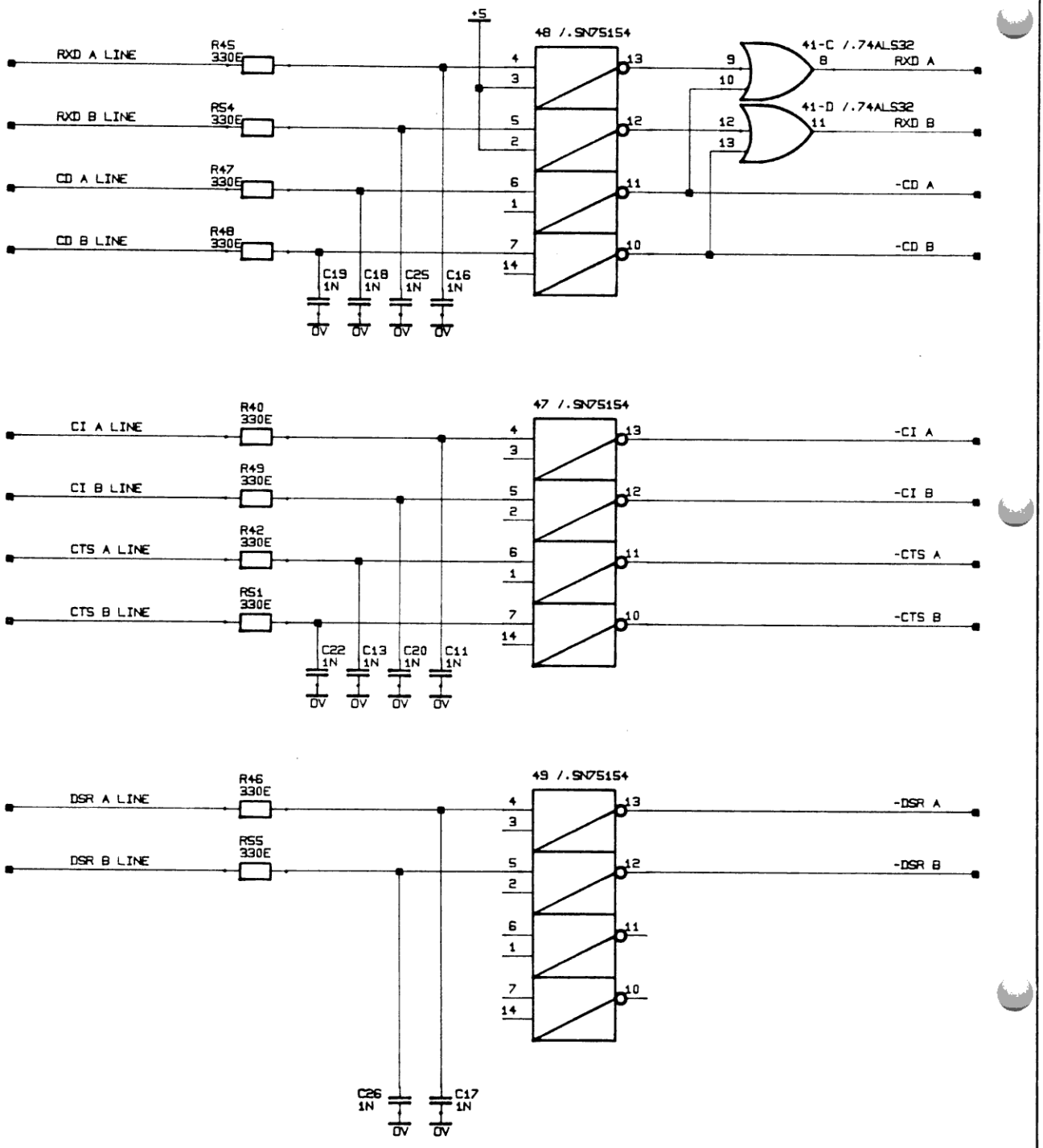

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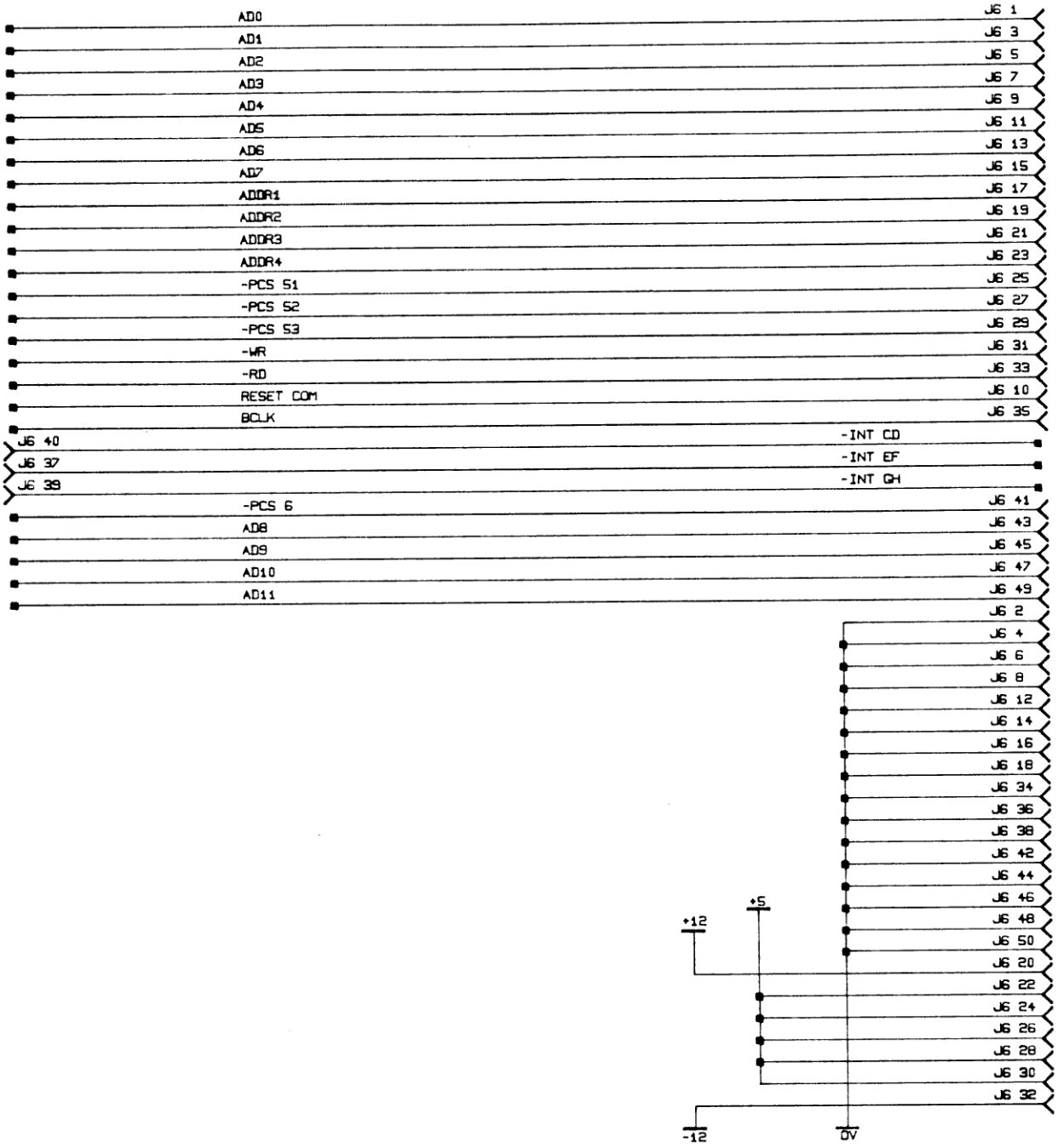

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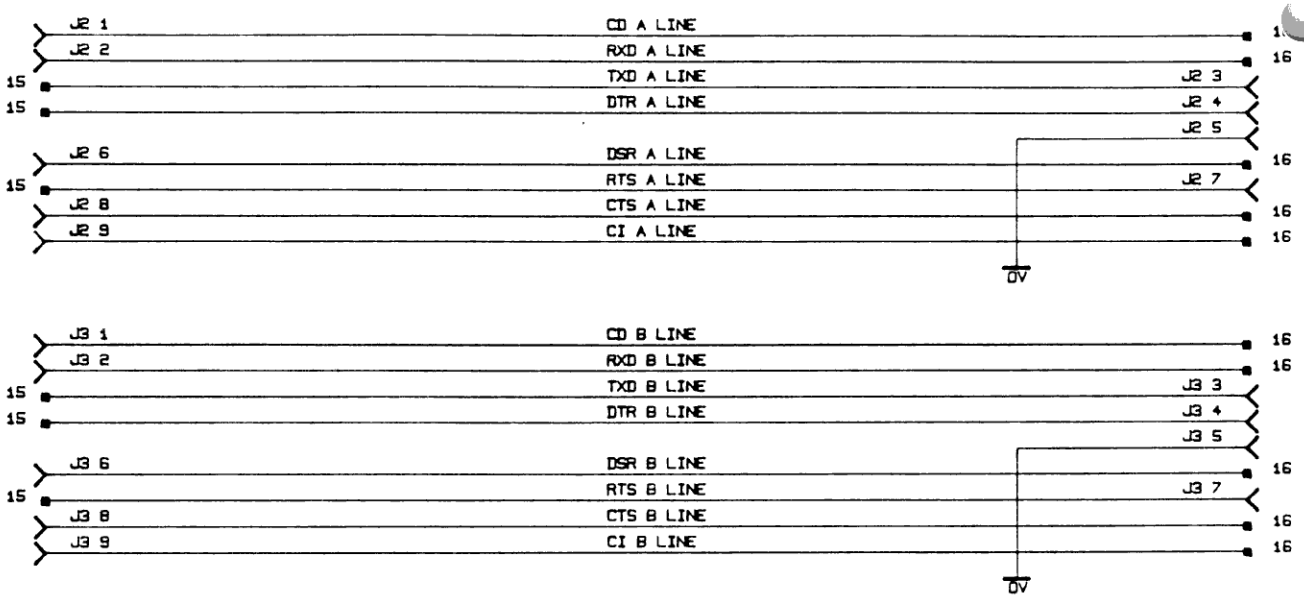

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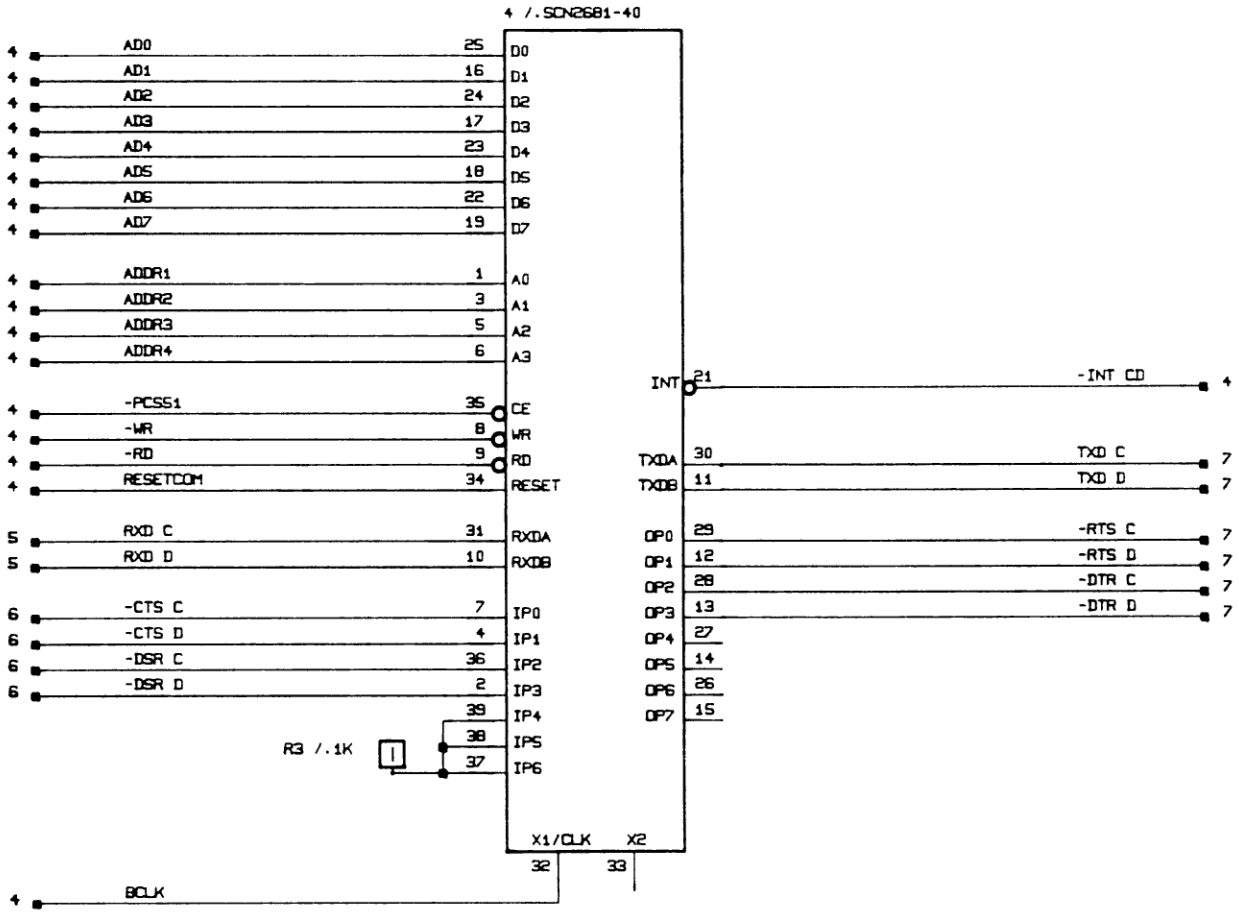
MXX



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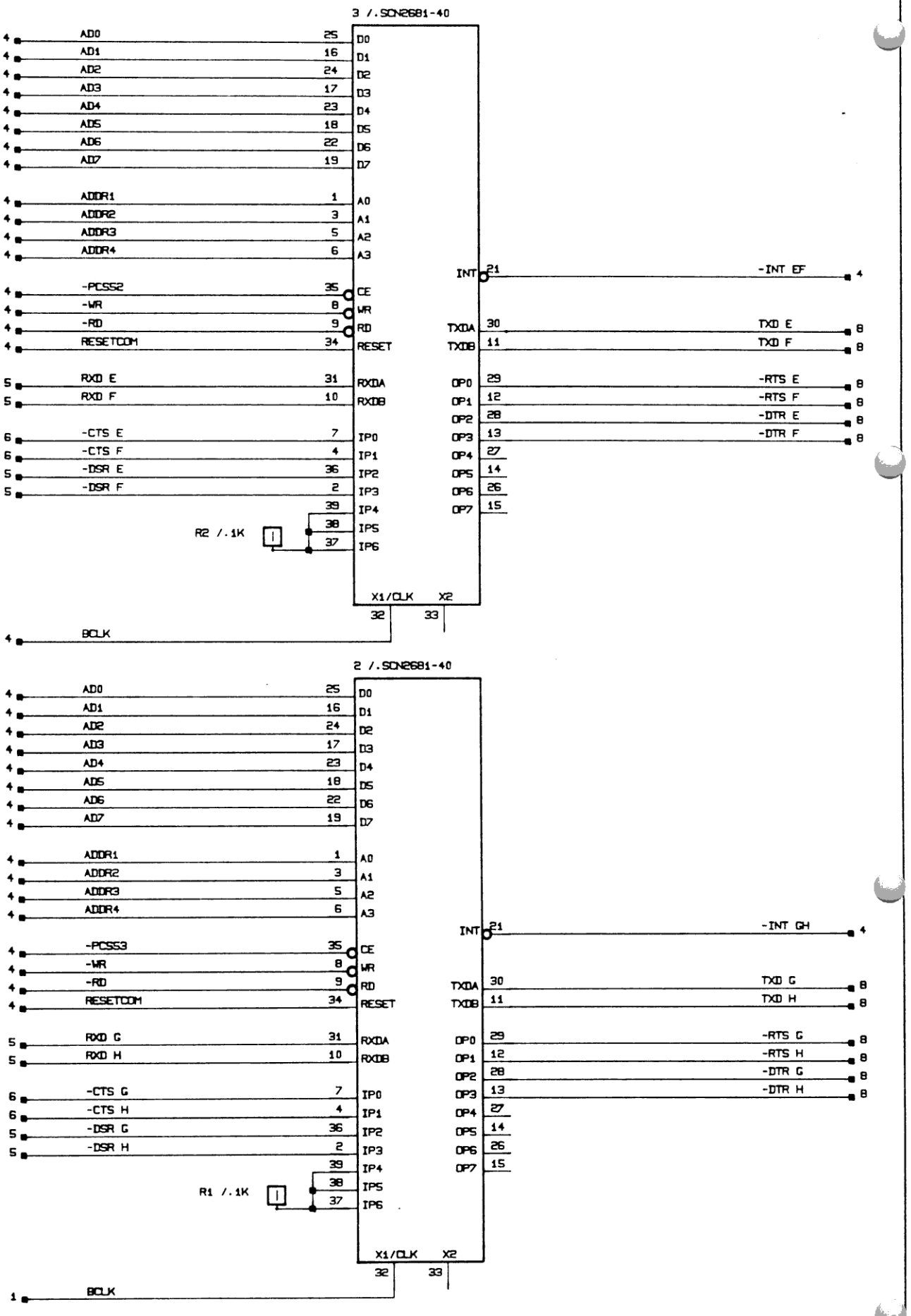

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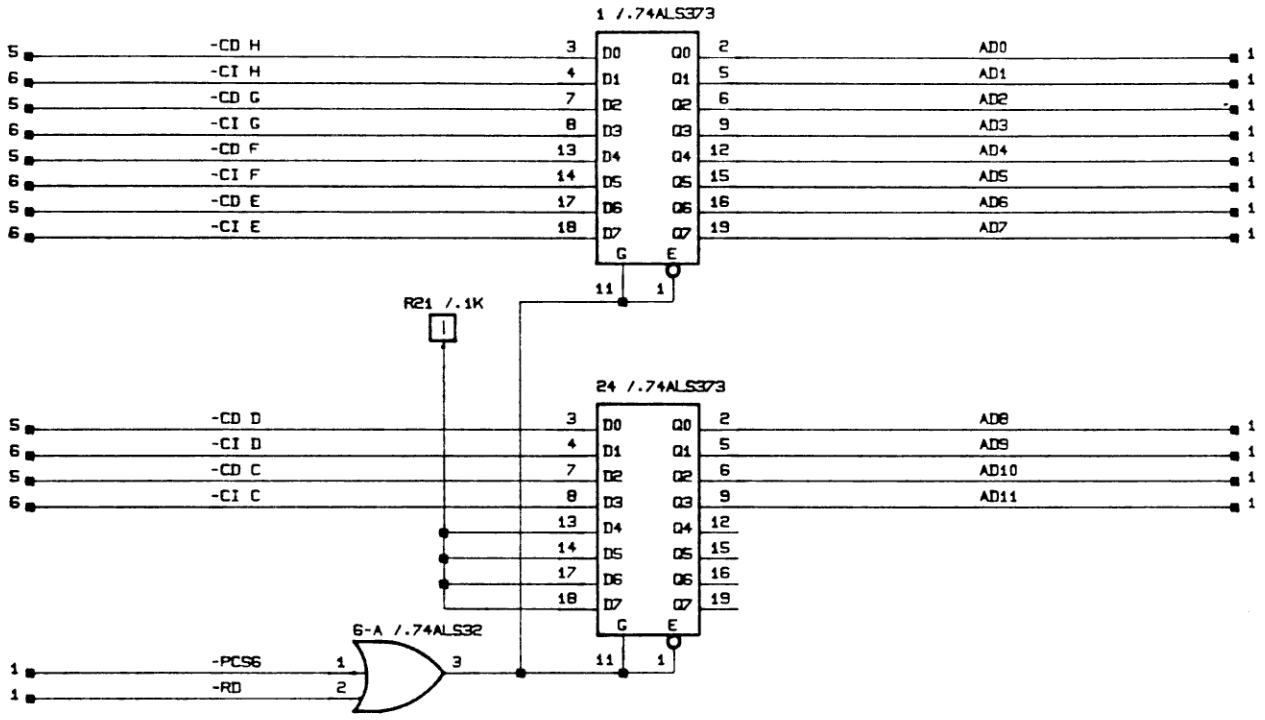

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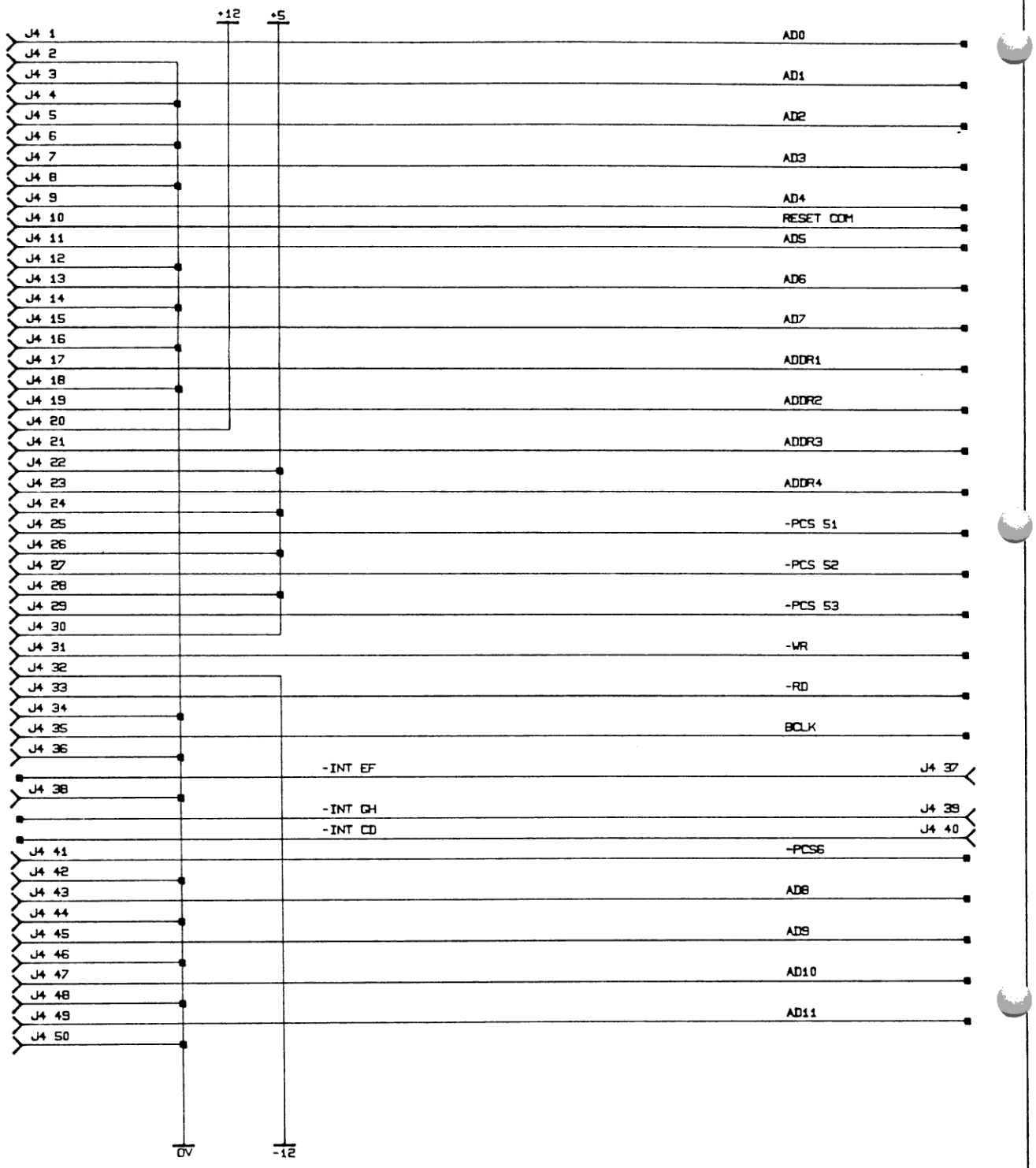

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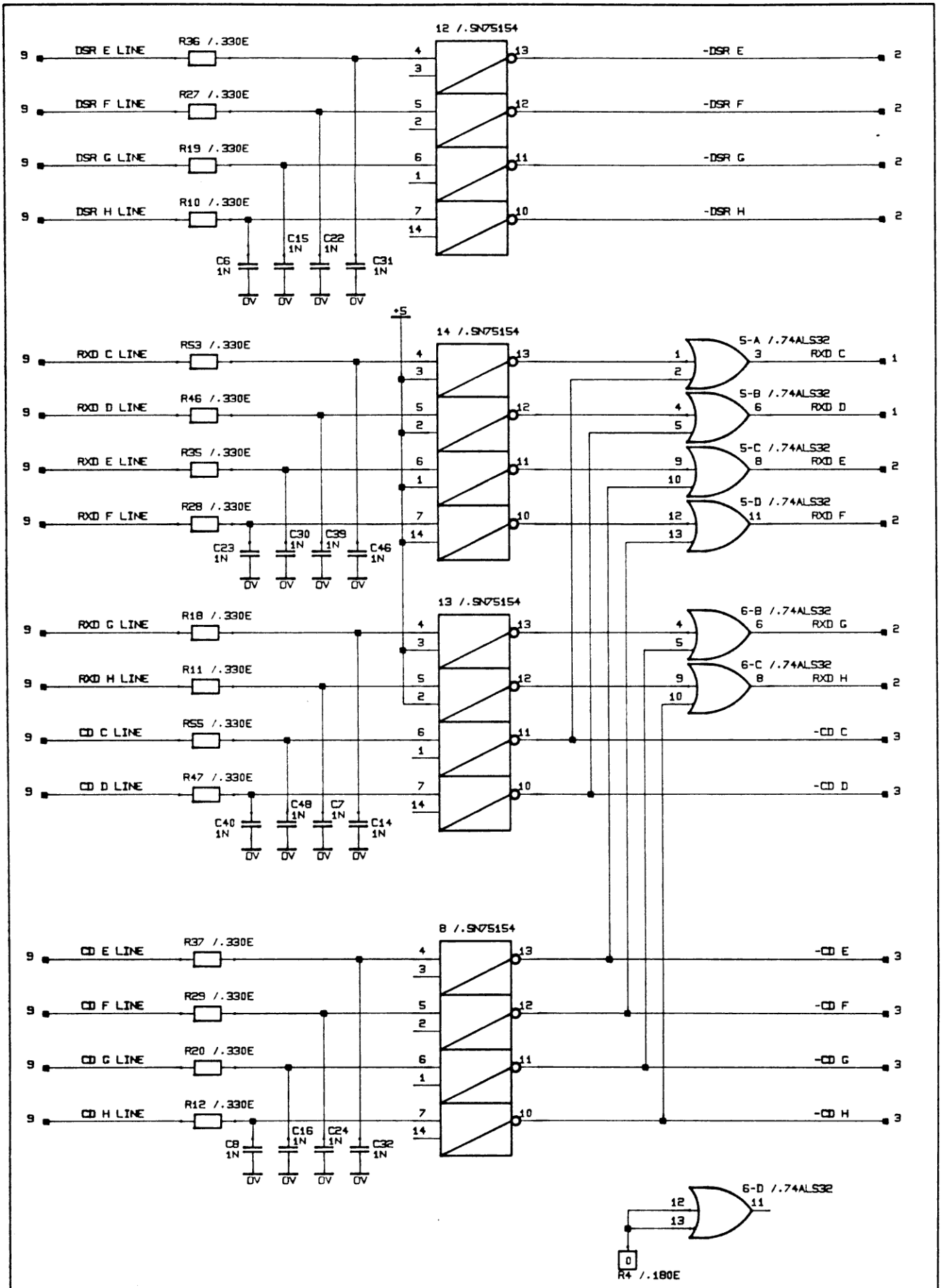

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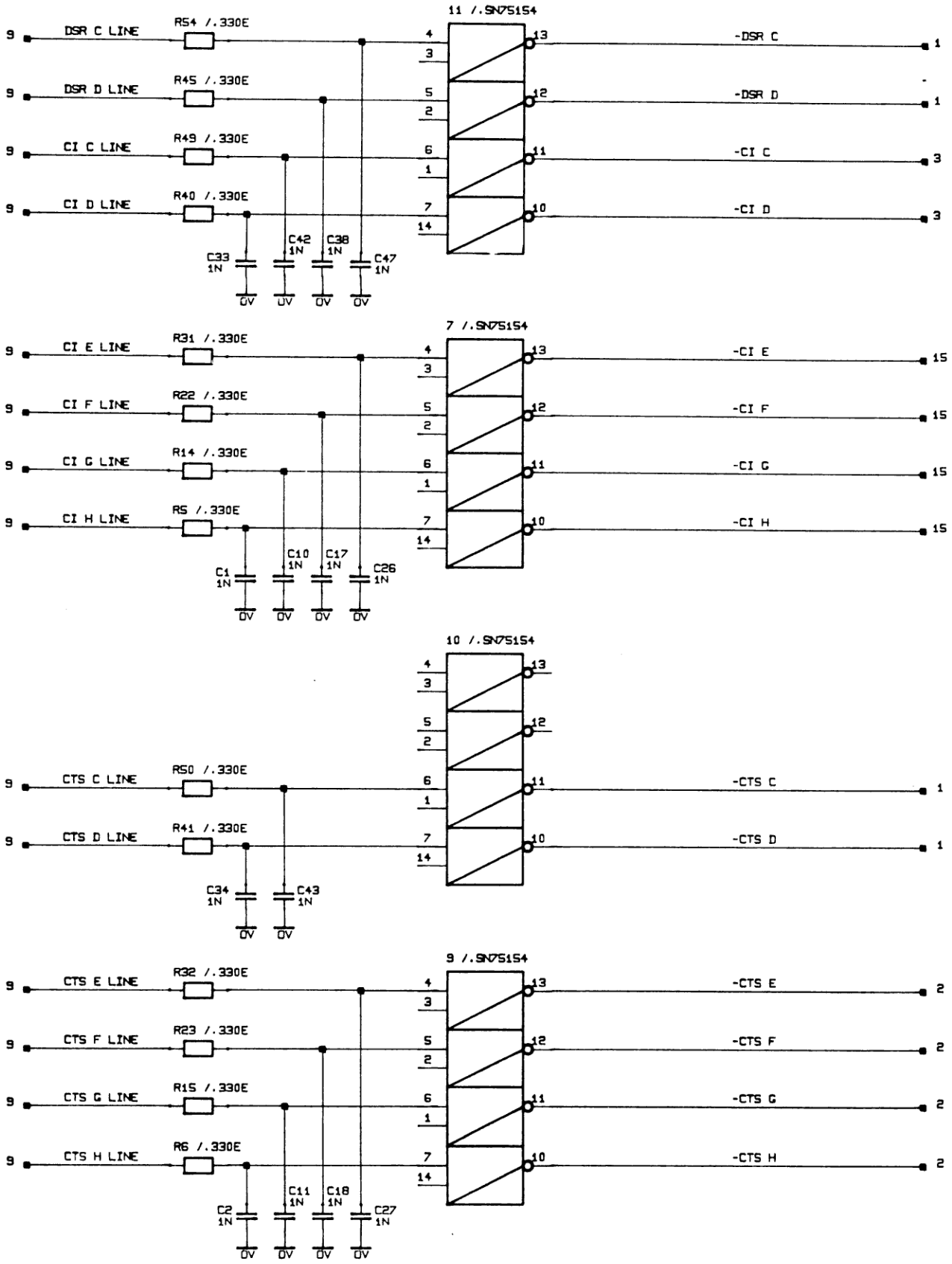

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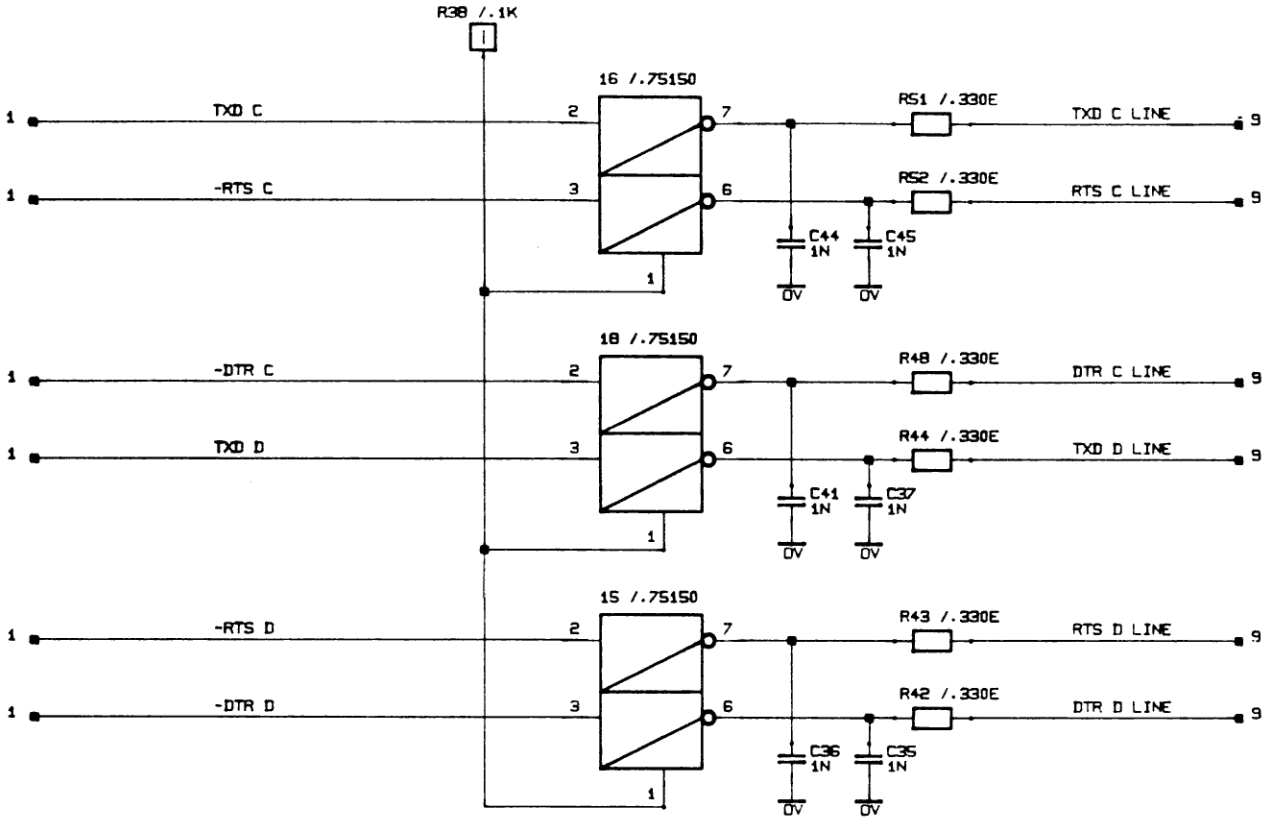

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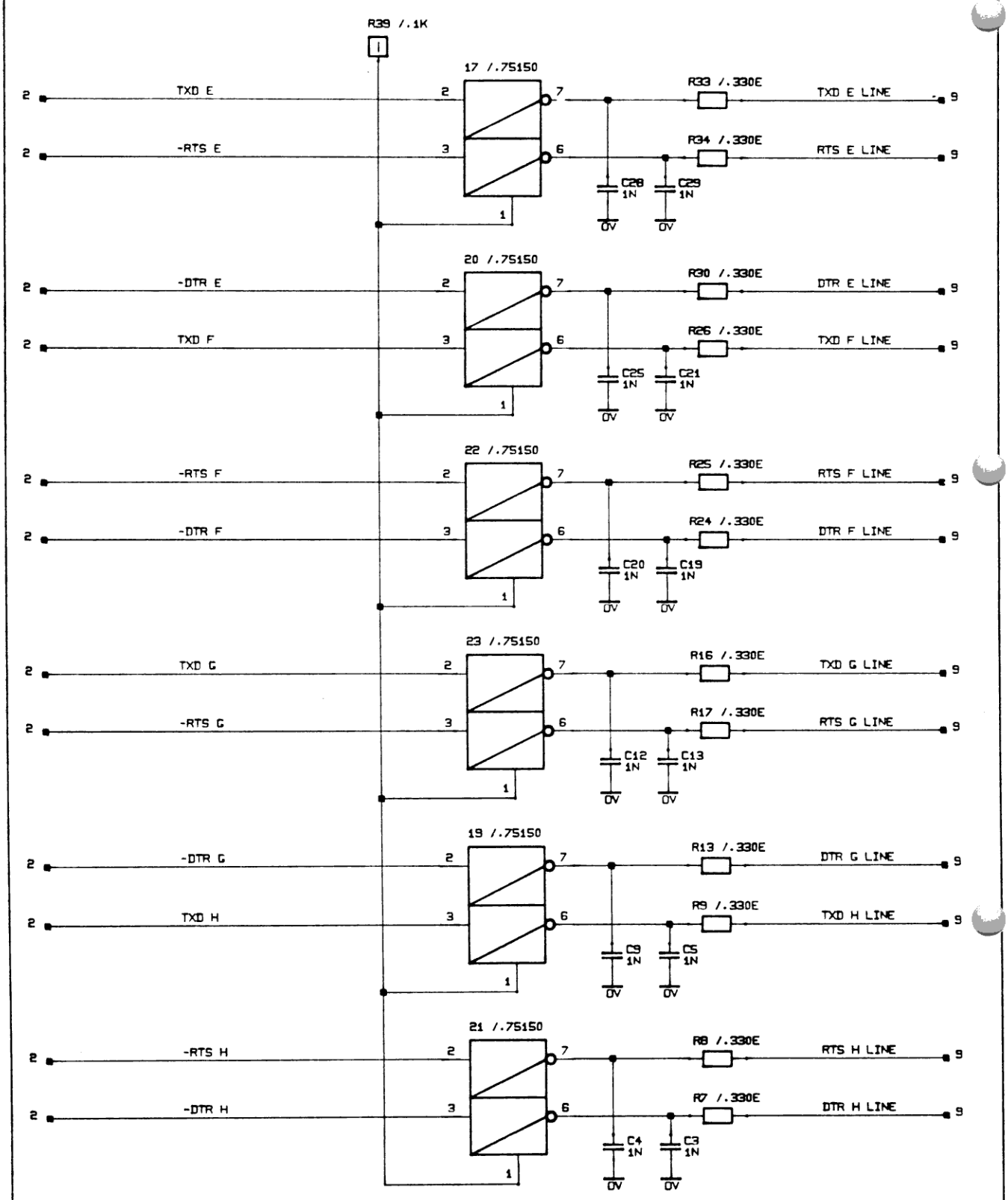
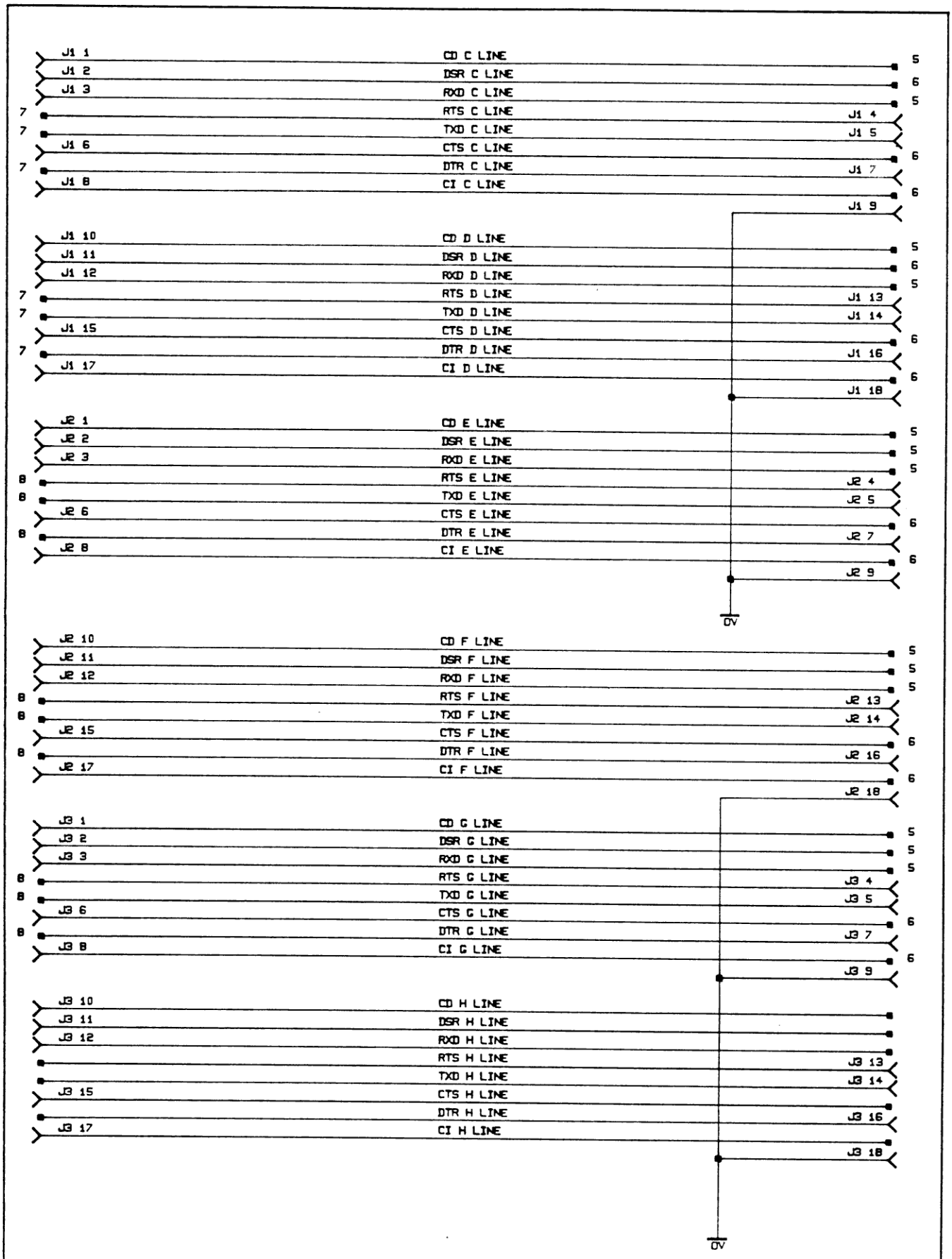
MXX451	JKA. THJ		7
DWG. NO.	DRAWN AGA 870817		



UNIT	DESIGN		
MXX451	JKA. THJ		8
DWG. NO.	DRAWN AGA 870817		



UNIT	DESIGN		
MXX451	JKA, THJ		9
DWG. NO.	DRAWN AGA 870817		

3.4 PAL descriptions


```
ABEL(tm) Version 2.02a - Document Generator   03-Apr-87 01:42 PM
LAN451 I/O BUS Controller, 2. FEB. 1987 ,
                Jens K. Andreassen , Regnecentralen A/S,
                Ballerup
Equations for Module PAT113TX

Device PAT113

     Reduced Equations:

       enable nsysbooten = (1);
       enable nsysbufen = (1);
       enable drqck = (1);
       enable sysclk = (0);
       nsysbooten = !(!nsysbooten & !nsysmemr
                    § !nsysbooten & !nsysmemw
                    § !nmast & !nsysacc & !nsysbsel);
       nsysbufen = !(!nsysbufen & !nsysmemr
                   § !nsysbufen & !nsysmemw
                   § !nmast & !nsysacc & nsysbsel);
       ndrqr := !(!nsysacc § !ndrqr & !nlock);
       aready := !(nmast & !nsysacc
                 § !nrefc & nsysacc
                 § !nmast & nrd & nwr);
       nsysmemw := !(!nmast & !nsysacc & !nwr);
       nsysmemr := !(!nmast & !nrd & !nsysacc);
       drqck = !(sysclk
               § drqx & !ndrqr
               § drqx & sysclk
               § !ndrqr & sysclk
               § ndrqr & sysclk);
```

ABEL(tm) Version 2.02a - Document Generator 03-Apr-87 01:42 PM

LAN451 I/O BUS Controller, 2. FEB. 1987 ,

Jens K. Andreassen , Regnecentralen A/S,
Ballerup

Chip diagram for Module PAT113TX

Device PAT113

P16R4

ABEL(tm) Version 2.02a - Document Generator 27-Apr-87 01:43 PM

LAN451,COM451 and MUX451 Memory selector, 29. JAN. 1987,

Jens K. Andreassen, Regnecentralen A/S , Ballerup

Equations for Module PAT114TX

Device PAT114

Reduced Equations:

```
enable nbank0 = (1);
enable nbank1 = (1);
enable nsysacc = (1);
enable nsysbsel = (1);
enable nrefr = (!nmast);
enable nrdwren = (1);
enable nhold1 = (1);
nbank0 = !(!A17 & !nhold1 & !nobcmd
         § !A17 & !A18 & !A19 & !nobcmd);
nbank1 = !(A17 & !nhold1 & !nobcmd § A17 & !A18 & !A19 &
         !nobcmd);
nsysacc = !(!A16 & A17 & A18 & A19 & nhold1 & !nobcmd
          § A16 & A17 & A18 & A19 & ndbgb & nhold1 &
          !nobcmd);
nsysbsel = !(A16 & A17 & A18 & A19 & ndbgb & nhold1 &
           !nobcmd);
rc8 = !(!A17 & !A18 § !A17 & coladr § !A18 & !coladr);
nhold1 = !(hlda & hold § hold & !nhold1);
nrefr = !(!A18 & !A19 & !nobcmd);
nrdwren = !(A18 & !nmast § A19 & !nmast § !nmast &
          nobcmd);
```

ABEL(tm) Version 2.02a - Document Generator 27-Apr-87 01:43 PM

LAN451,COM451 and MUX451 Memory selector, 29. JAN. 1987,

Jens K. Andreassen, Regnecentralen A/S , Ballerup

Chip diagram for Module PAT114TX

Device PAT114

P16L8

ABEL(tm) Version 2.02a - Document Generator 03-Apr-87 12:40 PM

LAN451 DRAM controller .21 jan 1987

Jens K. Andreassen, Regnecentralen A/S, BALLERUP

Equations for Module PAT116TX

Device PAT116

Reduced Equations:

```
enable nem0 = (1);
enable nem1 = (1);
nem0 = !(!ncoladr & !nras0 & nrefc & !ns1);
nem1 = !(!ncoladr & !nras1 & nrefc & !ns1);
nras0 := !(!ncoladr & !nrefc § !nbank0 & !nobcmd & nrefc);
nras1 := !(!ncoladr & !nrefc § !nbank1 & !nobcmd & nrefc);
nwelo := !(!addr0 & !nbank0 & ncoladr & !nobcmd & nrefc &
         ns1 § !addr0 & !nbank1 & ncoladr & !nobcmd &
         nrefc & ns1);
nwehi := !(!nbank0 & !nbhen1 & ncoladr & !nobcmd & nrefc &
         ns1 § !nbank1 & !nbhen1 & ncoladr & !nobcmd &
         nrefc & ns1);
nrefc := !(!ncoladr & !nrefc & refr & !refrd
         § nbank0 & nbank1 & nrefc & refr & !refrd
         § ncoladr & nras0 & !nrefc & refr & !refrd);
ncoladr := !(nras0 & !nrefc
           § !nbank0 & !nobcmd & nrefc
           § !nbank1 & !nobcmd & nrefc);
```

ABEL(tm) Version 2.02a - Document Generator 03-Apr-87 12:40 PM

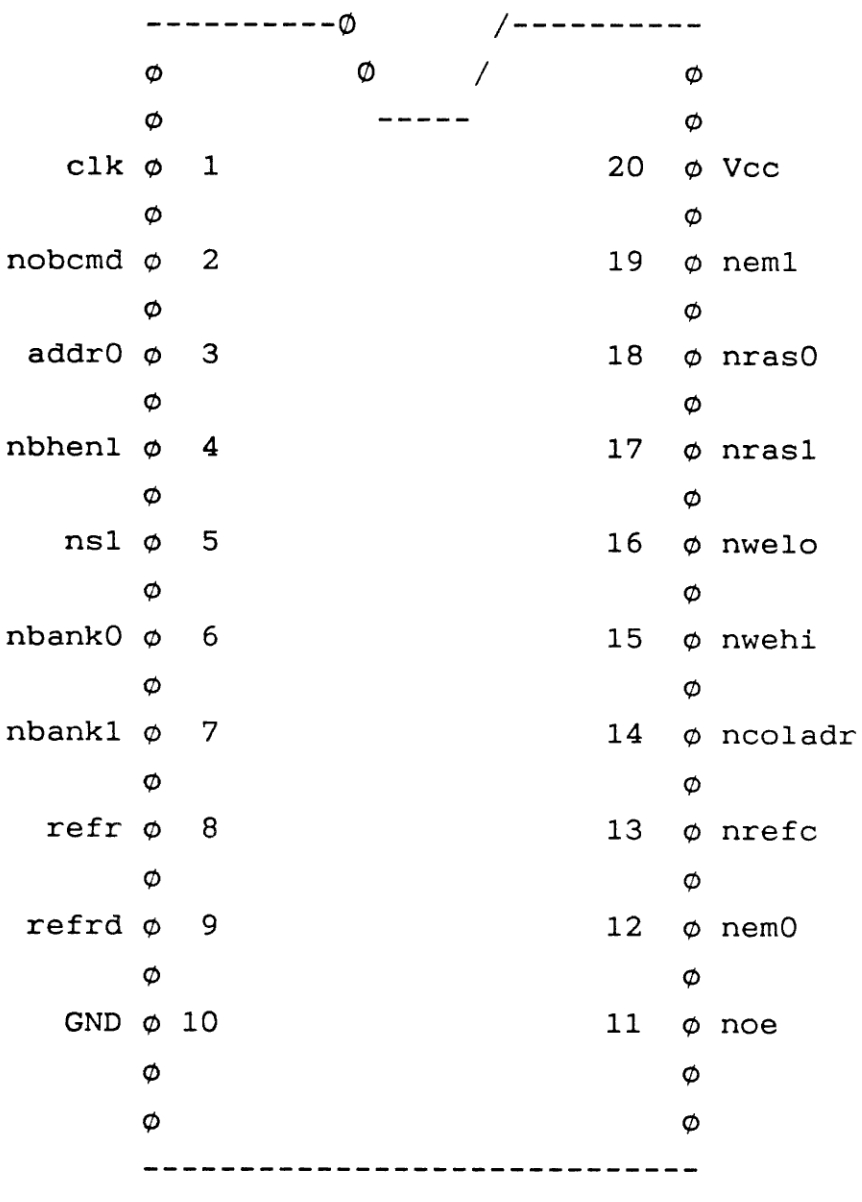
LAN451 DRAM controller .21 jan 1987

Jens K. Andreassen, Regnecentralen A/S, BALLERUP

Chip diagram for Module PAT116TX

Device PAT116

P16R6



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ABEL(tm) Version 2.02a - Document Generator  22-May-87 11:45 AM
MUX451 I/O interrupt and reset , 22. MAY  1987,
          Troels H. Johansen , Regnecentralen A/S,Ballerup
Equations for Module PAT133TX

Device PAT133

     Reduced Equations:

       enable nioacc = (1);
       enable atint = (1);
       enable reset_drv = (0);
       enable sw1 = (0);
       enable nirq1 = (1);
       enable nreset = (1);
       enable nbootck = (1);
       nbootck = !(!nioacc & !sa0 & !sa1);
       nioacc = !(!nioen & !niowr & !sa2 & !sa3 & sa4 & sw1
                # !nioen & !niowr & sa2 & !sa3 & sa4 & !sw1);
       nreset = !(ndbgreset & reset_drv
                # ndbgreset & nioacc & !nreset
                # ndbgreset & !nreset & sa0
                # ndbgreset & !nreset & sa1
                # ndbgreset & !nioacc & sa0 & !sa1);
       atint = !(!ndbgreset
               # !ninta
               # !nreset
               # !atint & nioacc
               # !atint & !sa0
               # !atint & !sa1);
      nirq1 = !(!ndbgreset
               # !nreset
               # nirq & !nirq1
               # !nioacc & !sa0 & sa1);
```

ABEL(tm) Version 2.02a - Document Generator 22-May-87 11:45 AM

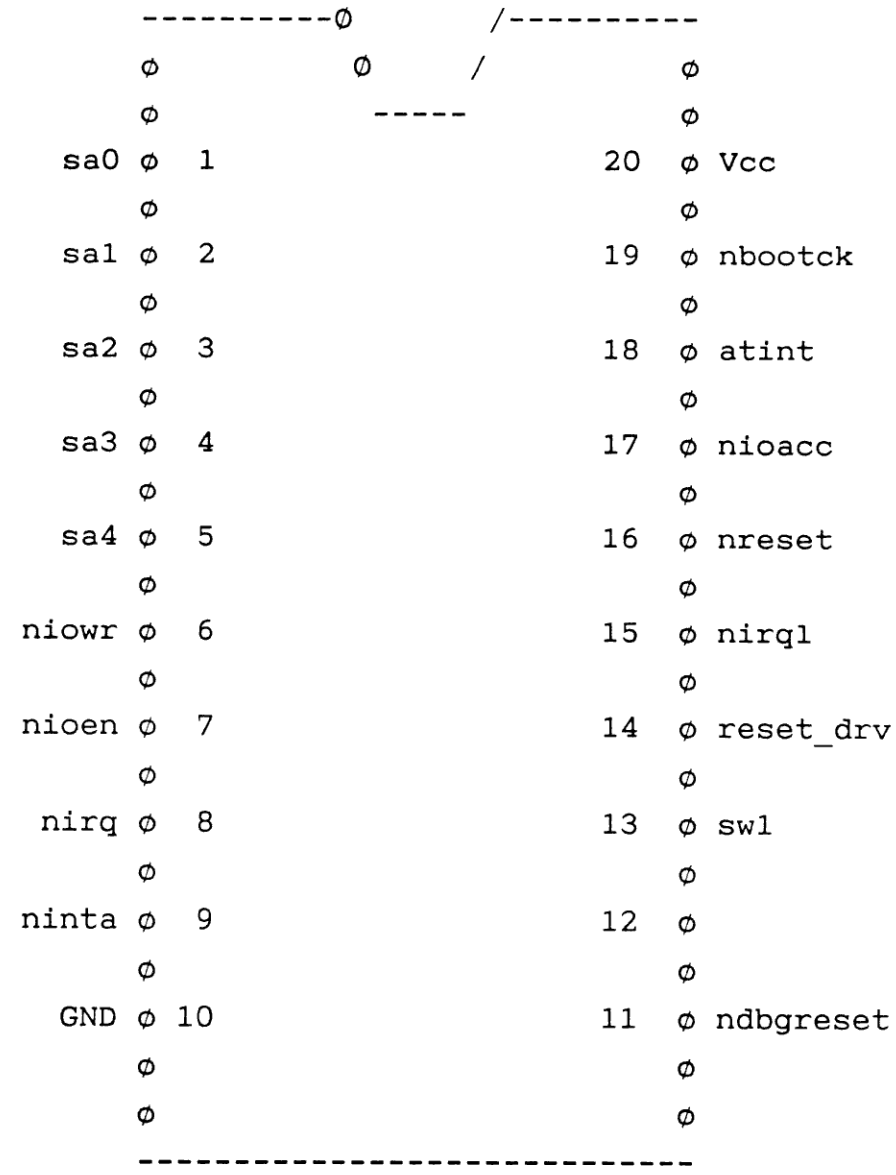
MUX451 I/O interrupt and reset , 22. MAY 1987,

Troels H. Johansen , Regnecentralen A/S,Ballerup

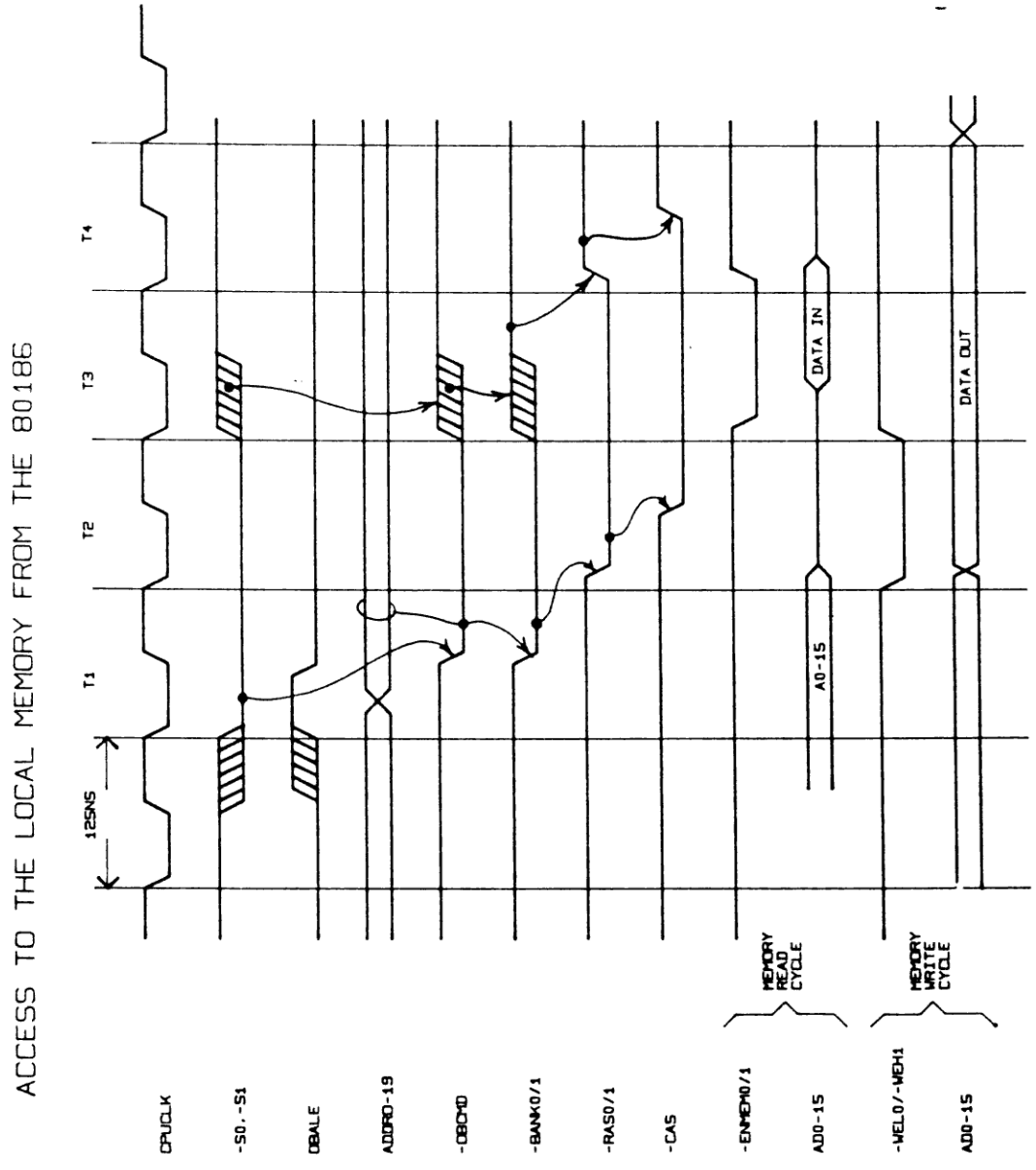
Chip diagram for Module PAT133TX

Device PAT133

P16L8

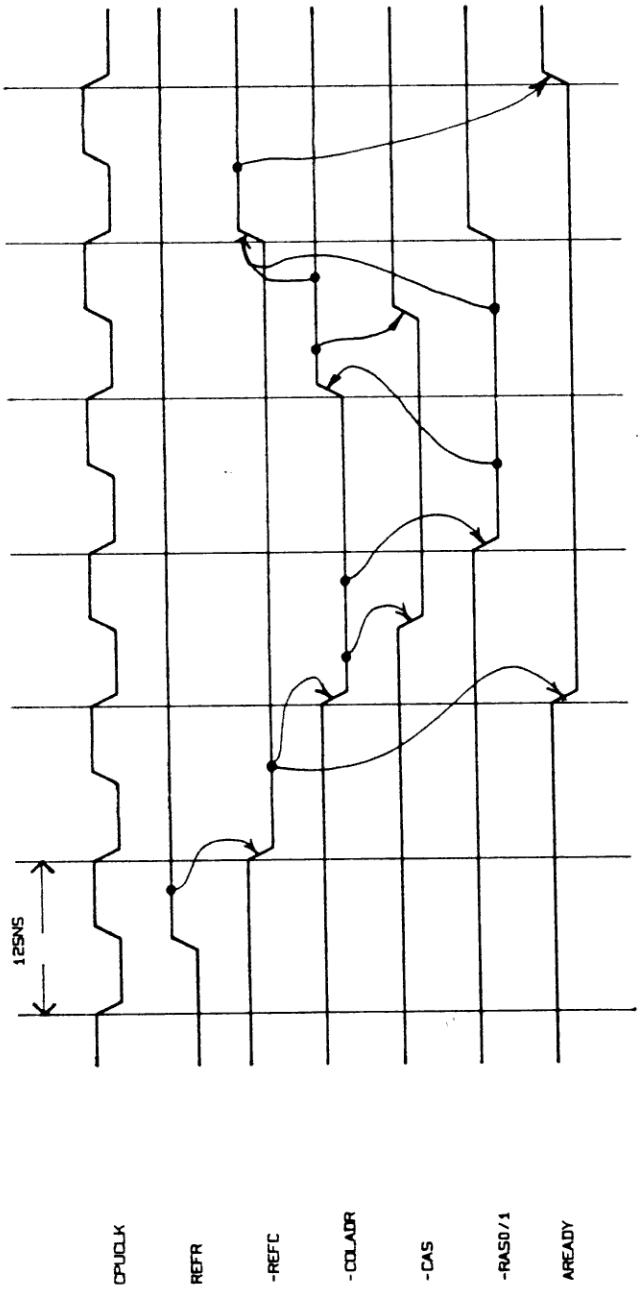


3.5 Timing diagrams

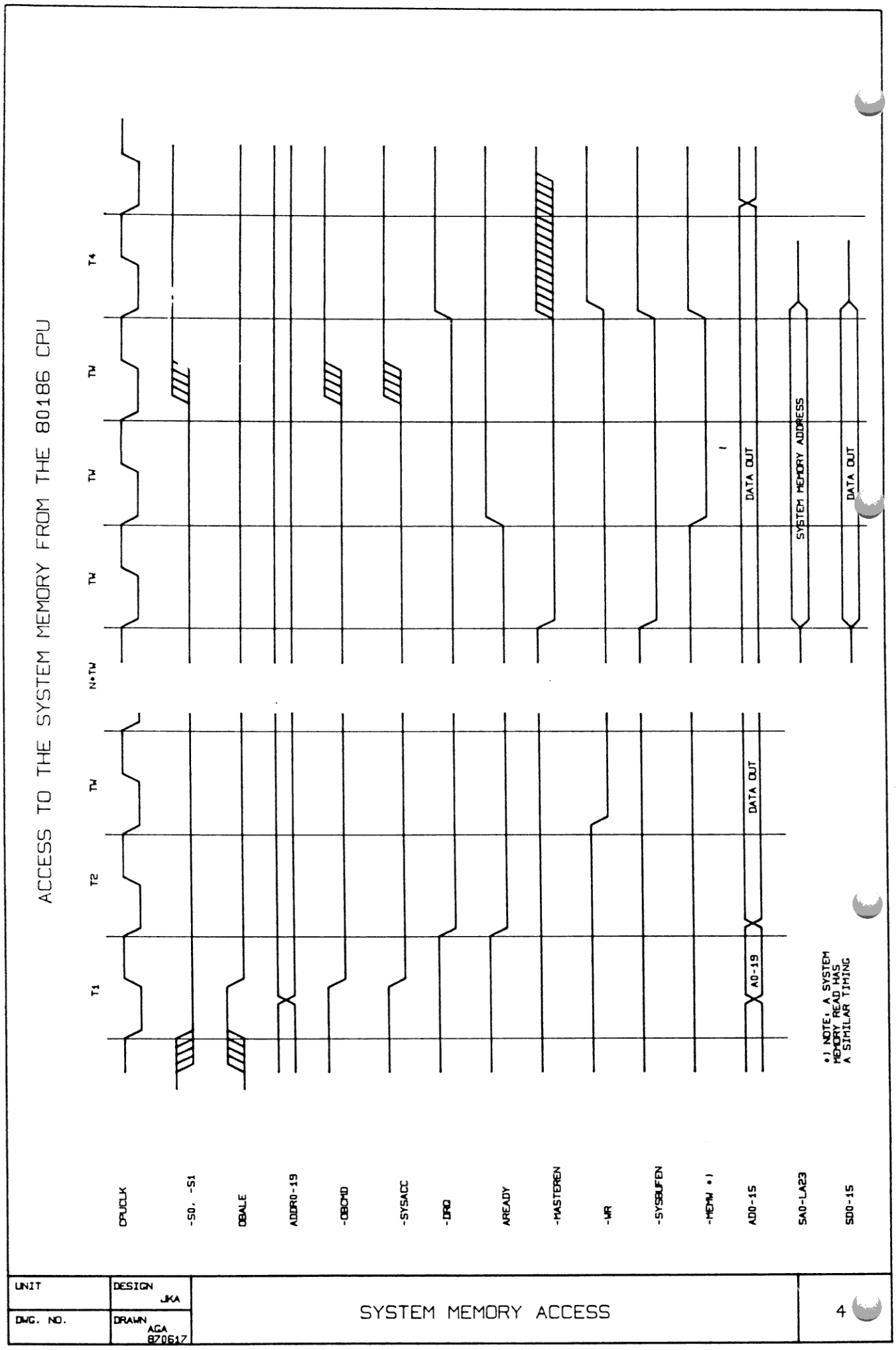


UNIT	DESIGN JKA	ON BOARD MEMORY ACCESS	6
DWG. NO.	DRAWN AGA 870617		

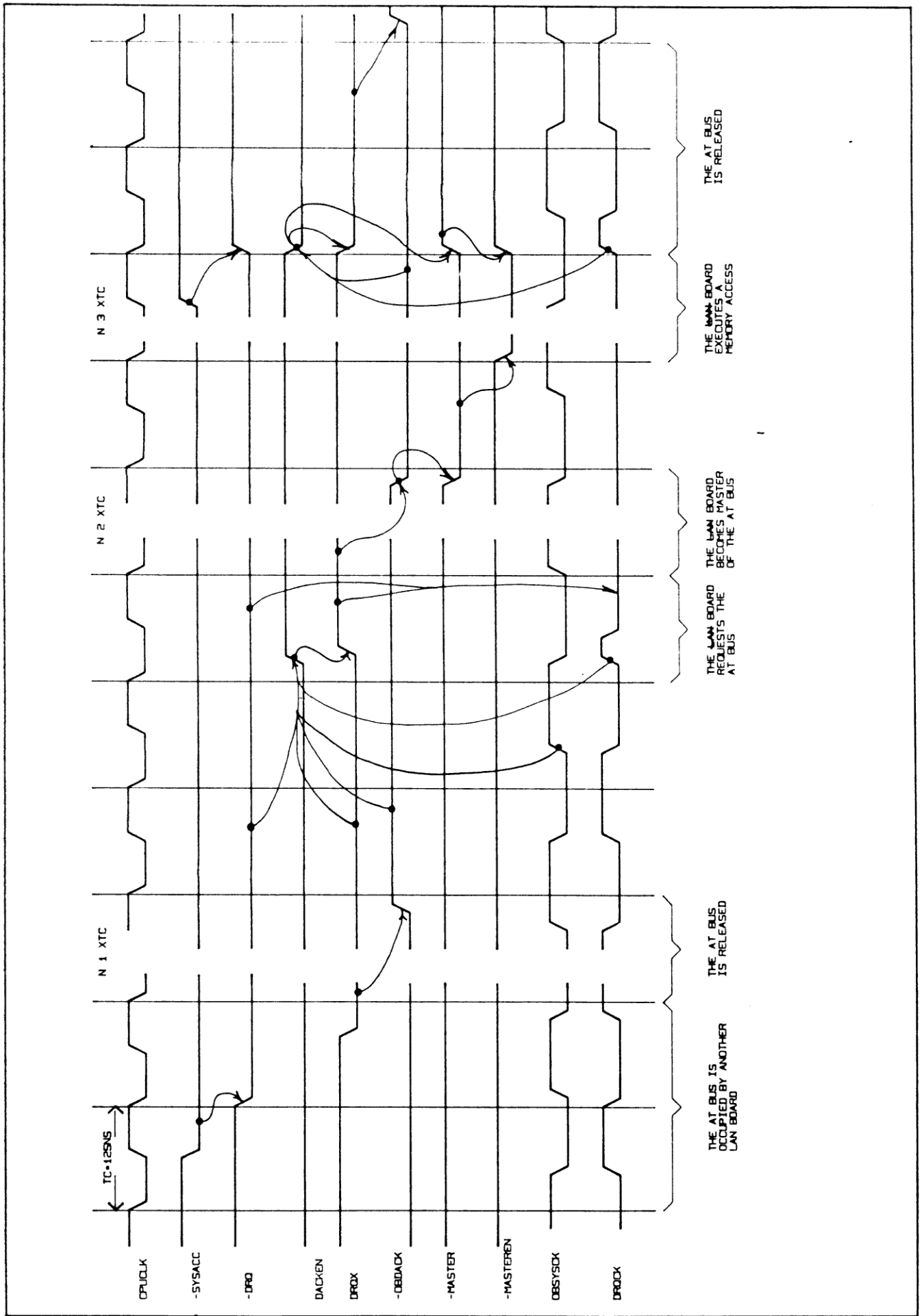
CAS BEFORE RAS MEMORY REFRESH



UNIT	DESIGN JKA	ON BOARD MEMORY REFRESH	7
DWG. NO.	DRAWN AGA 870617		

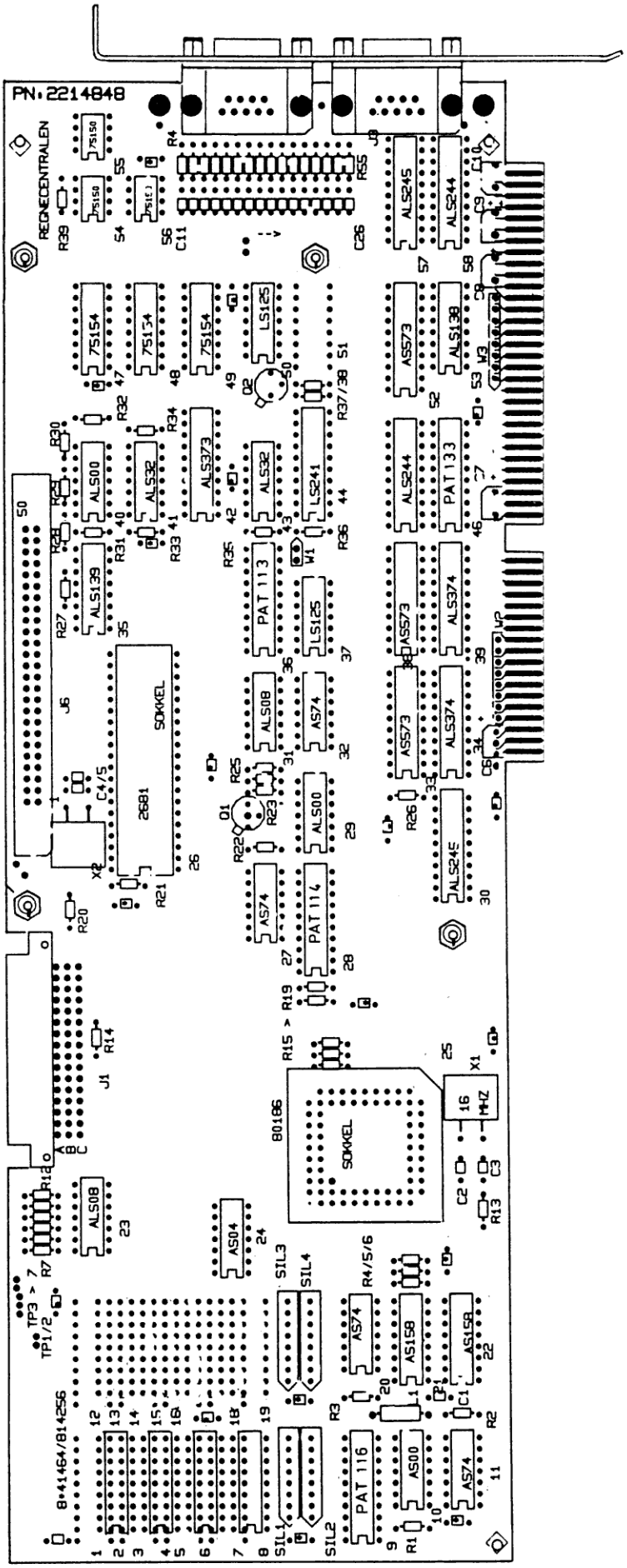


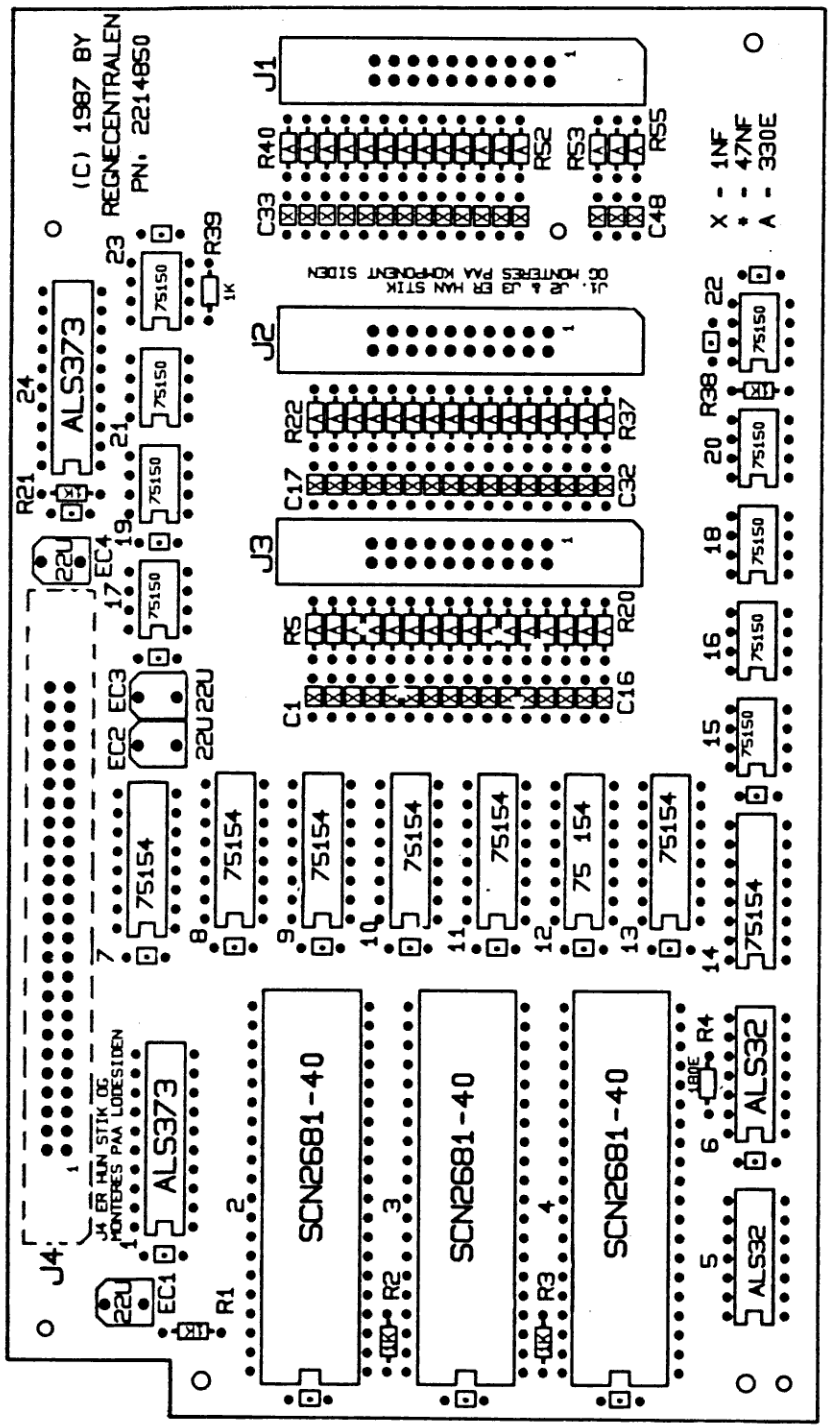
UNIT	DESIGN JKA	SYSTEM MEMORY ACCESS	4
DWG. NO.	DRAWN AGA 870617		



UNIT	DESIGN JKA	AT-BUS ARBITRATION CYCLE	5
DWG. NO.	DRAWN AGA 870617		

3.6 Assembly drawing




(C) 1987 BY
REGNECENTRALEN
PN: 2214850
J4
J1
J2
J3
SCN2681-40
SCN2681-40
SCN2681-40
ALS373
ALS373
ALS32
ALS32
75154
75150
22U
X - 1NF
* - 47NF
A - 330E

3.7 Plugs

3.7.1 AT bus connector

A side (component side)

I/O Pin	Signal Name
A1	-I/O CH CK (not connected to MUX451
A2	SD7
A3	SD6
A4	SD5
A5	AD4
A6	SD3
A7	SD2
A8	SD1
A9	SD0
A10	-I/O CH RDY
A11	AEN
A12	SA19
A13	SA18
A14	SA17
A15	SA16
A16	SA15
A17	SA14
A18	SA13
A19	SA12
A20	SA11
A21	SA10
A22	SA9
A23	SA8
A24	SA7
A25	SA6
A26	SA5
A27	SA4
A28	SA3
A29	SA2
A30	SA1
A31	SA0

B side (solder side):

I/O Pin	Signal Name	
B1	GND	
B2	RESET DRV	
B3	+5V	
B4	IRQ9	
B5	-5V	
B6	DRQ2	
B7	-12V	
B8	OWS	(not used)
B9	+12V	
B10	GND	
B11	-SMEMW	(not used)
B12	-SMEMR	(not used)
B13	-IOW	
B14	-IOR	(not used)
B15	-DACK3	(not used)
B16	DRQ3	(not used)
B17	-DACK1	(not used)
B18	DRQ1	(not used)
B19	-REFRESH	
B20	SYSCLK	
B21	IRQ7	(not used)
B22	IRQ6	(not used)
B23	IRQ5	(not used)
B24	IRQ4	(not used)
B25	IRQ3	(not used)
B26	-DACK2	(not used)
B27	T/C	(not used)
B28	BALE	(not used)
B29	+5V	
B30	OSC	(not used)
B31	GND	

C side (component side):

I/O Pin	Signal Name
C1	SBHE
C2	LA23
C3	LA22
C4	LA21
C5	LA20
C6	LA19
C7	LA18
C8	LA17
C9	-MEMR
C10	-MEMW
C11	SD8
C12	SD9
C13	SD10
C14	SD11
C15	SD12
C16	SD13
C17	SD14
C18	SD15

D side (solder side):

I/O Pin	Signal Name	
D1	-MEMCS16	(not used)
D2	-I/O CS16	(not used)
D3	IRQ10	(not used)
D4	IRQ11	(not used)
D5	IRQ12	
D6	IRQ15	(not used)
D7	IRQ14	(not used)
D8	-DACK0	(not used)
D9	DRQ0	(not used)
D10	-DACK5	
D11	DRQ5	
D12	-DACK6	(not used)
D13	DRQ6	(not used)
D14	-DACK7	(not used)
D15	DRQ7	(not used)
D16	+5V	
D17	-MASTER	
D18	GND	

3.7.2 V.24 Connector

The V.24 connector seen from the rear:

Pin	Signal Name
1	CD (Carrier detect)
2	RXD (Receive Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	Signal Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	CI (Calling Indicator)

3.7.3 Debug Board Connector

The Debug board Connector seen from the top.

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	AD0	B1	+5V	C1	-DEBUG BOARD
A2	AD1	B2	0V	C2	-DEBUG RESET
A3	AD2	B3	+12V	C3	-PROMSEL
A4	AD3	B4	-12V	C4	-PCS1
A5	AD4	B5	CPURESET	C5	-DBINT
A6	AD5	B6	0V	C6	DBAREADY
A7	AD6	B7	A16	C7	-RXINT
A8	AD7	B8	A17	C8	IDENT1
A9	AD8	B9	A18	C9	IDENT2
A10	AD9	B10	A19	C10	IDENT3
A11	AD10	B11	0V	C11	-BHEN
A12	AD11	B12	OBALE	C12	0V
A13	AD12	B13	-WR	C13	-S0
A14	AD13	B14	-RD	C14	-S1
A15	AD14	B15	0V	C15	-S2
A16	AD15	B16	+5V	C16	-CPUCLK

4. REFERENCES

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Vol I+II, INTEL, 1986.

(2) SCN2681 Dual Asynchronous Receiver/Transmitter (DUART)
Product Specification
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(3) Technical Reference, Personal Computer AT
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(4) Specifikation af Debug-kort,
Okt. 86,
Willian S. Jacobsen.

(5) Programmer`s Technical Guide, RC900
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