RC900

COM451 Communications Contr.

Hardware reference manual

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RC Computer

Keywords:
COM451, Communication Controller, RC950

Abstract:
This paper contains a hardware description of the Communication Controller board, COM451. The COM451 is provided with an IBM-AT bus interface. The board is also provided with a V.24/X.21 synchronous channel for communication.

Date:
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Author:
Jens K. Andreassen

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1. INTRODUCTION

This manual describes the COM451 board. The COM451 board is an intelligent Serial Communication adapter with IBM-AT I/O bus interface.

The COM451 is provided with a 80186 CPU and 896 k bytes of local RAM. The COM451 can become a master on the AT I/O bus, thus providing the board with the facility to read from and write to the system board memory. The Intel 82530 Communication controller is used on the board.

The manual is divided into basically three sections. The first section contains a short description and a short specification of the board. The second section contains a description which is relevant for the programmer of the board. The last section contains a detailed hardware description of the board.

2. GENERAL INFORMATION

2.1 Short Description

Fig. 1 shows a block diagram of the COM451 board.

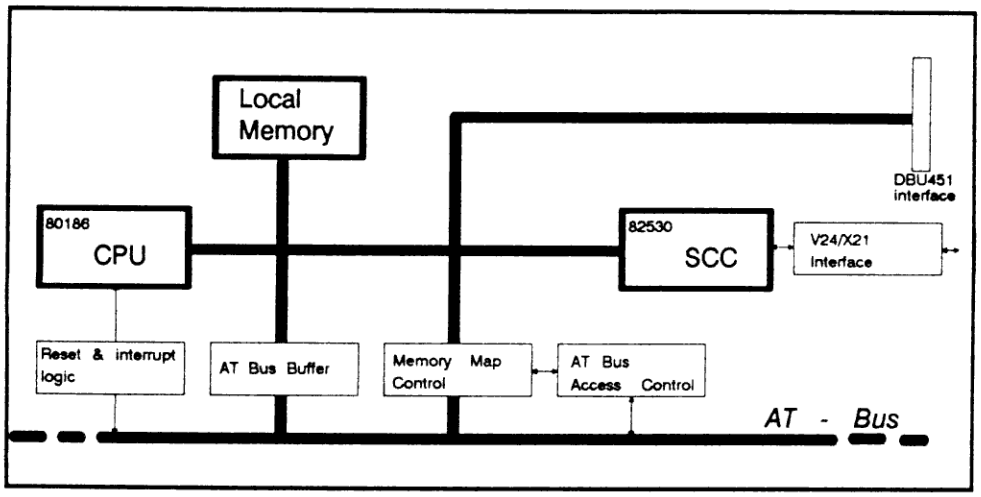


Fig. 1: COM451 Block diagram.

The CPU is an 8MHz INTEL 80186 processor, see (1). The CPU is integrated with

- 3 programmable timer.
- 5 interrupt input lines and an interrupt controller.
- Programmable waitstate generator.
- 2 programmable DMA controllers.
- 7 programmable I/O chip select lines.

The INTEL 82530 Seriel Communication Controller is provided with two serial channels of witch channel A is used on the board. The 82530 together with the V.24/X.21 interface allow for supporting SDLC and BSC synchronous communication protocols. The 82530 is also programmable for NRZI data encoding/decoding.

The Local Memory consists of 896 Kbyte DRAM. No PROM is available on the COM451 board. The Local Memory can only be accessed by the 80186 CPU. The upper most 128K byte of the 80186 address space is mapped onto the system memory through the AT bus. The Boot Memory

Map Register controlles the mapping of the upper most 64 Kbyte. The Buffer Memory Map Register controlles the mapping of the next 64 Kbyte.

After reset the 80186 starts executing code in the system memory in the Boot Memory address space.

Through a 25 pol D-connector the COM451 board can be connected with a V.24 modem cable or a X.21 modem cable.

A 48 pol EURO connector on the COM451 provides for testing the board with a Debug Board, DBU451, see (4). The DBU451 is provided with EPROMs. After reset, which may be generated by the DBU451 board, the 80186 may execute the code placed in these EPROMs.

Through the Reset and Interrupt Logic the COM451 can generate an interrupt on the system board and the System Board can interrupt the COM451 board. The system board can also generate a reset signal to the COM451 board.

A maximum of two COM451 boards can be mounted in the AT slots.

2.2 Specification

2.2.1 Performance Specifications

80186 CPU clock	: 8 MHz
Data Bus Size	: 16 bits
EPROM	: none
On board RAM capacity (Local Memory)	: 896 Kbyte
Off board Memory	:
Boot Memory	: 64 Kbytes of the system memory.
Buffer Memory	: 64 Kbyte of the system memory.
Memory address range	:
Local Memory	: 00000H-DFFFFH
Boot Memory	: F0000H-FFFFFH
Buffer Memory	: E0000H-EFFFFH

2.2.2 Environmental Specifications

Operating Temperature	: $0^{o}C$ - $40^{o}C$.
Relative Humidity	: 20% - 80% (non condensing).

2.2.3 Physical Specification

Width	: 121.80 mm
Length	: 333.25 mm
Height	: 20 mm

2.2.4 Power Specification

Power Dissipation	: 7.5 W max.
Vcc	: +5V +/- 5% (1.5 A max.)
Vdd	: +12V +/- 10% (0.5 A max.)

2.3 Installation

The COM451 board can be plugged into any of the AT-I/O slot. If another COM451 is allready plugged into one of the slots a jumper must be mounted on one of the COM451 boards. The jumper must be mounted at the position named S1 on the board. A maximum of two COM451 boards can be installed in the AT slots.

3. PROGRAMMING INFORMATION

This chapter contains the necessary programming information of the COM451 board.

3.1 The 80186 CPU

The COM board is based on an INTEL 80186 single chip CPU. The reader should read (1) and (2) in conjunction with reading this chapter. Abbreviations from (1) and (2) are used in this chapter.

An 16 MHz x-tal is connected to the on-chip clock generator providing the board with an 8 MHz clock signal. This means that an local memory access takes 0.5 us, i.e. with no wait states. The R0-2 fields in the 80186 UMCS, LMCS and MMCS register should be programmed to 000B. This means external generated RDY signal and no internal generated wait states.

3.1.1 Interrupts to the 80186 CPU

The 80186 interrupt controller are connected to the following interrupt sources:

80186 interrupt pin	Interrupt source
INT0	82530 interrupt
INT1	Interrupt from the system board
INT2	Transmit interrupt from Debug Board
INT3	reserved
NMI	Receive interrupt from Debug Board

The interrupt vectors must be generated by the 80186 interrupt controller it self. The 80186 must be programmed in the fully nested mode providing the board with up to five external interrupt sources.

3.1.2 The 80186 DMA controller

The 80186 has two integrated DMA channels. DMA0 and DMA1. The 82530 SCC utilizes these DMA channels and is connected in the following way:

80186 DMA channel	82530 DMA request
DMA1	TXDRQ (The DTRA/REQA pin on 82530)
DMA0	RXDRQ (The RDYA/REQA pin on 82530).

3.1.3 The 80186 Timers

The 80186 has three integrated timers. Timer 0 is dedicated as a DRAM refresh request source. The timer must be programmed to generate a signal with a duty cycle of appr. 50% and a cycle time of max. 14 usec. The DRAM on the board then performs a CAS before RAS refresh cycle every 14 usec. An initial pause of 200 usec is required after power-up. After the pause a minimum of 8x256 refresh cycles are required. Timer 1 and timer 2 are not used.

3.1.4 The 80186 peripheral chip select

The 80186 has seven integrated peripheral chip select lines. On the COM451 board these lines are used in the following way:

80186 chip select pin	I/O Address range	Desitnation
!PCS0	! PBA-PBA+7FH	! not used
!	!	!
!PCS1	! PBA+80H -	! Chip select to Debug
!	! PBA+0FFH	! Board
!PCS2	! PBA+100H -	! Acknowledges an interrupt
!	! PBA+17FH	! from the system board
!PCS3	! PBA+180H -	! Generates an interrupt
!	! PBA+1FFH	! on the AT-bus (IRQ11)
!PCS4	! PBA+200H -	! Memory
!	! PBA+27FH	! Map Register load
!PCS5	! PBA+280H -	! 82530 Transmit data (used
!	! PBA+2FFH	! by the DMA1 channel)
!PCS6	! PBA+300H -	! 82530 control and receive
!	! PBA+37FH	! data (used by the DMA0
!	!	! channel)

PBA is the I/O offset address contained in the 80186 PACS register.

The MS bit in the 80186 MPCS register must be loaded with 0H, i.e. peripherals are mapped into I/O space.

The R2-R0 bits in the PACS register should be programmed with 101B, i.e. one wait state in I/O cycles for PCS0-PCS3 asserted.

The R2-R0 bits in the MPCS register should be programmed with 111B, i.e. three wait states for PCS4-PCS6 asserted.

PCS1 is asserted when reading from or writing to the Debug Board.

An I/O cycle asserting the PCS3 signal will generate an interrupt on the AT-bus (IRQ11). This interrupt signal may be deasserted by the system board, see chapter 3.4.3.

The 80186 can deassert an interrupt from the AT-bus (INT1, see chapter 3.1.1) by executing an I/O write cycle with PCS2 asserted.

Reading from an I/O address with PCS4 asserted will return some control bits from the serial interface:

	Data bit	Signal Name	Signal description
MSB	7	DTR	V.24, Data Terminal Ready
	6	CD	V.24, Carrier Detect
	5	CTS	V.24, Clear To Send
	4	TI	V.24, Test Indicator
	3	X.21 Sel	X.21, Cable installed
	2	RECEIVE	X.21, Receive Signal
	1	DSR	V.24, Data Set Ready
LSB	0	CI	V.24, Calling Indicator

Writing to an I/O address with PCS4 asserted will load the Memory Map Register, see chapter 3.2.2. The Memory Map Register is loaded with the contents of the lowermost eight data bits.

PCS5 and PCS6 are gated together, which means that any of the two signals can be used to access the 82530 device, but if the DMA controller in the 80186 are used PCS5 cannot be used by any other device but the DMA controller 1, see 3.3.1.

3.2 COM451 Memory

The 80186 1 Mbyte address space on the COM451 is divided into three parts:

1. Local Memory Address space: 00000H-DFFFFH
2. Buffer Memory Address space: E0000H-EFFFFH
3. BOOT Memory Address space: F0000H-FFFFFH.

Fig. 2 shows the organization of the 1 Mbyte memory space.

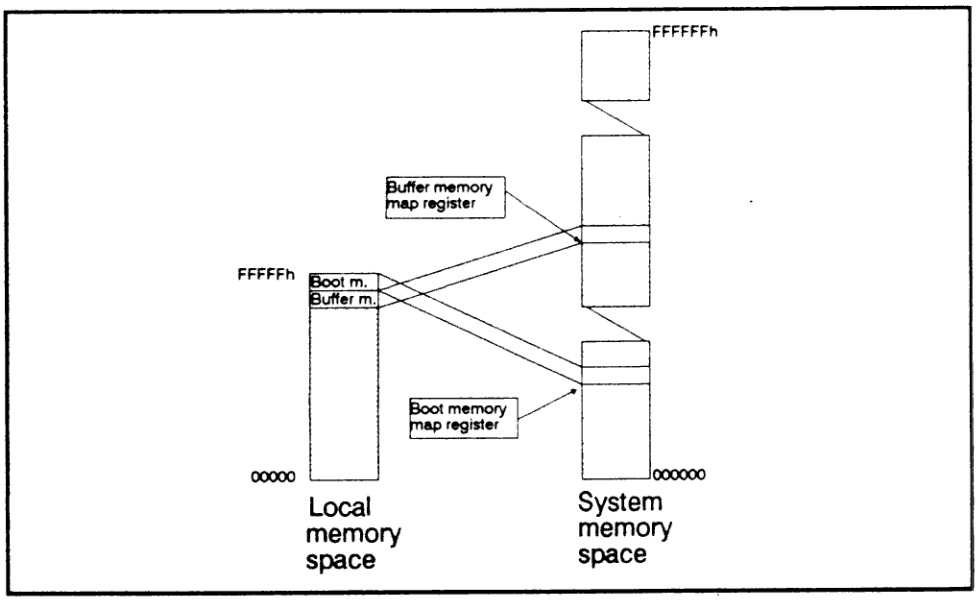


Fig. 2. COM451 memory organization and system memory map.

3.2.1 Local Memory

The Local Memory consists of 896 Kbytes of on-board DRAM. 256Kx4bit DRAM chips are used. This memory can only be accessed by the 80186 CPU. The memory chips are fast enough to avoid insertion of wait states.

The Local Memory is automatically refreshed by the 80186 Timer 0 see chapter 3.1.3.

3.2.2 Buffer Memory

The Buffer Memory is a memory map of the 80186 CPU address space onto the system memory. When accessing this memory the COM451 board becomes a master of the AT-bus. Due to the arbitration a number of wait states are inserted.

The memory mapping of the buffer memory is controlled by the 80186 CPU through the Buffer Memory Map register. This register is loaded by the 80186 CPU by writing to the I/O device with PCS4 asserted, see section 3.1.4. The Memory Map register contains the following bit:

7	6	5	4	3	2	1	0
LA23	LA22	LA21	LA20	LA19	LA18	LA17	SA16

The MSB of the register controlles the most significant address bit, LA23, on the AT-bus. The LSB of the register controlles the AT-address signal SA16, when accessing the Buffer Memory. The Buffer Memory Map register selects a 64 Kbyte boundary in the system memory.

By using the 80186 LOCK prefix it is possible to move or compare a block of data to or from the system memory. Normally a device on the AT-bus is not allowed to be a master on the AT-bus in more than 14 usec. The floppy must be serviced within 14 usec. on a DMA request. If the COM451 is master, by using the REP/LOCK prefix in more than 14 usec. data to or from the floppy controller may be lost and data in the system memory may be lost due to lack of refresh. Though, the system memory will be refreshed by the COM451 board if one of the following instructions are used:

```
REP LOCK MOVS or
REP LOCK CMPS.
```

3.2.3 Boot Memory

The upper 64 Kbytes of the 80186 memory space is normally of the Read Only Memory type. In this manual this is called the Boot Memory. This memory space is mapped into the system memory through the Boot Memory Map register. The Boot Memory Map register is loaded by the system board by an I/O write cycle, see section 3.4.1.

The least significant byte on the AT data bus is loaded into the Boot Memory Map register. The Boot Memory Map register contains the following bits.

7	6	5	4	3	2	1	0
LA23	LA22	LA21	LA20	LA19	LA18	LA17	SA16

The MSB of the register controlles the most significant address signal, LA23, on the AT-bus. The LSB of the register controlles the least significant address signal, SA16, on the AT-bus. The Boot Memory Map register selects a 64 Kbyte boundary in the 16 Mbyte system memory.

3.3 Communication Interface

The communication interface consists of the 82530 Serial Communication Controller and hardware to provide the board with a V.24/ X.21 interface channel.

The 82530 device is described in detail in (2) and in (5).

3.3.1 the 82530 SCC

The 82530 is clocked by a 4 MHz signal which is half the 80186 clockout signal. This clock can be used as a clock to the baud rate generator integrated on the 82530 chip.

The RDY_A/REQ_A pin on the 82530 is connected to the DRQ0 pin on the 80186. Thus the DMA channel 0 on the 80186 is used as receive DMA channel. The DTR_A/REQ_A pin on 80186. This connection is used as a transmit DMA request connection to the 80186 CPU.

In order to reset the flip flop again the DMA channel 1 controller must assert PCS5 when moving data to the 82530 transmitter. The DMA channel 0 controller in the 80186 CPU must assert PCS6 when moving data from the 82530 to memory.

The 80186 CPU must assert PCS6 when writing commands and data (not DMA) to the 80530 and the 80186 CPU must assert PCS6 when reading status and data from the 80530.

The 80186 must insert three waitstates when accessing the 82530.

The 82530 is addressed by the 80186 in the following way:

I/O base address	82530 device
300 H	register ch.B
302 H	data ch.B
304 H	register ch.A
306 H	data ch.A
308 H	interrupt acknowledge (read)
206 H	data ch.A through DMA

Interrupts from the 82530 is acknowledged by the 80186 by reading in the I/O address 308 H. An interruptvector is read from the 82530.

3.3.2 Serial Interface

The 82530 serial channel A and channel B are both used in the communication. Data is transferred through channel A only. One of the output pin from channel B is used, see below:

Serial function V.24/X.21	82530 Symbol	82530 pin
RTS	RTS_A	17
DTR	$DTR_B REQ_B$	24
TXD	TXDA	15
TXC	TRXCA	14
CD	CDA	19
CTS	CTSA	18
RXD	RXDA	13
RXC	RTXCA	12

The 82530 is provided with a baudrate generator and NRZI encoding/decoding logic.

The control signals CI, DSR, RECEIVE, X21SEL, TI, CTS, CD and DTR are read through a buffer, see chapter 3.1.4.

3.4 IBM-AT Bus Interface

Some of the AT-interface characteristica are mentioned in section 3.2. This section contains information on how to select AT-I/O addresses, DMA channels and AT interrupt signals. The reader should also consult (3).

3.4.1 AT I/O addresses

Through the jumper S1 the I/O addresses is slected:

S1	I/O address space	
On	30CH-30FH	(the jumper is mounted)
Off	308H-30BH	(the jumper is not mounted)

If two COM451 borads are mounted in the AT slots, one and only one of them must be configured with S1 in the off position.

The COM451 will recognize four AT I/O addresses:

S1=on	S4=off	
30CH	308H	Deassert the reset signal on the COM451 board and load the Boot Memory MAP register.
30DH	309H	Activate the reset signal on the COM451.
30EH	30AH	Acknowledge from the system board on an interrupt from the COM451.
30FH	30BH	Interrupt to the COM451 CPU 80186.

3.4.2 AT DMA Channel Select

The COM451 board uses the DMA channel 3 on the AT bus to become a Master on the AT bus. If two COM451 boards are installed arbitration logic on the boards will select one of the boards to become Master if they request the bus at the same time.

3.4.3 AT interrupt

The COM451 board can activate the IRQ11 interrupt signal on the AT bus. If two COM451 boards are mounted in the AT slots they will both activate IRQ11.

3.5 Debug Board Interface

A debug board, DBU451, can be plugged into a 36 pin connector on the COM451 board, providing the technician with debug facilities. The reader should consult (4) for further information.

4. TECHNICAL DESCRIPTION

4.1 Introduction

This chapter contains a detailed technical description of the COM451 hardware. Section 4.2 gives a survey of the COM451 board. Section 4.3 contains the electrical diagrams of the COM451 and should be readen together with section 4.2. Section 4.4 contains description of the COM451 PAL's and Ethernet ROM. Section 4.5 contains some relevant timing diagrams.

A description of the LSI components used is not given in this chapter. It is recommended that the reader consults the relevant data sheets (see chapter 5).

4.2 Short Technical description

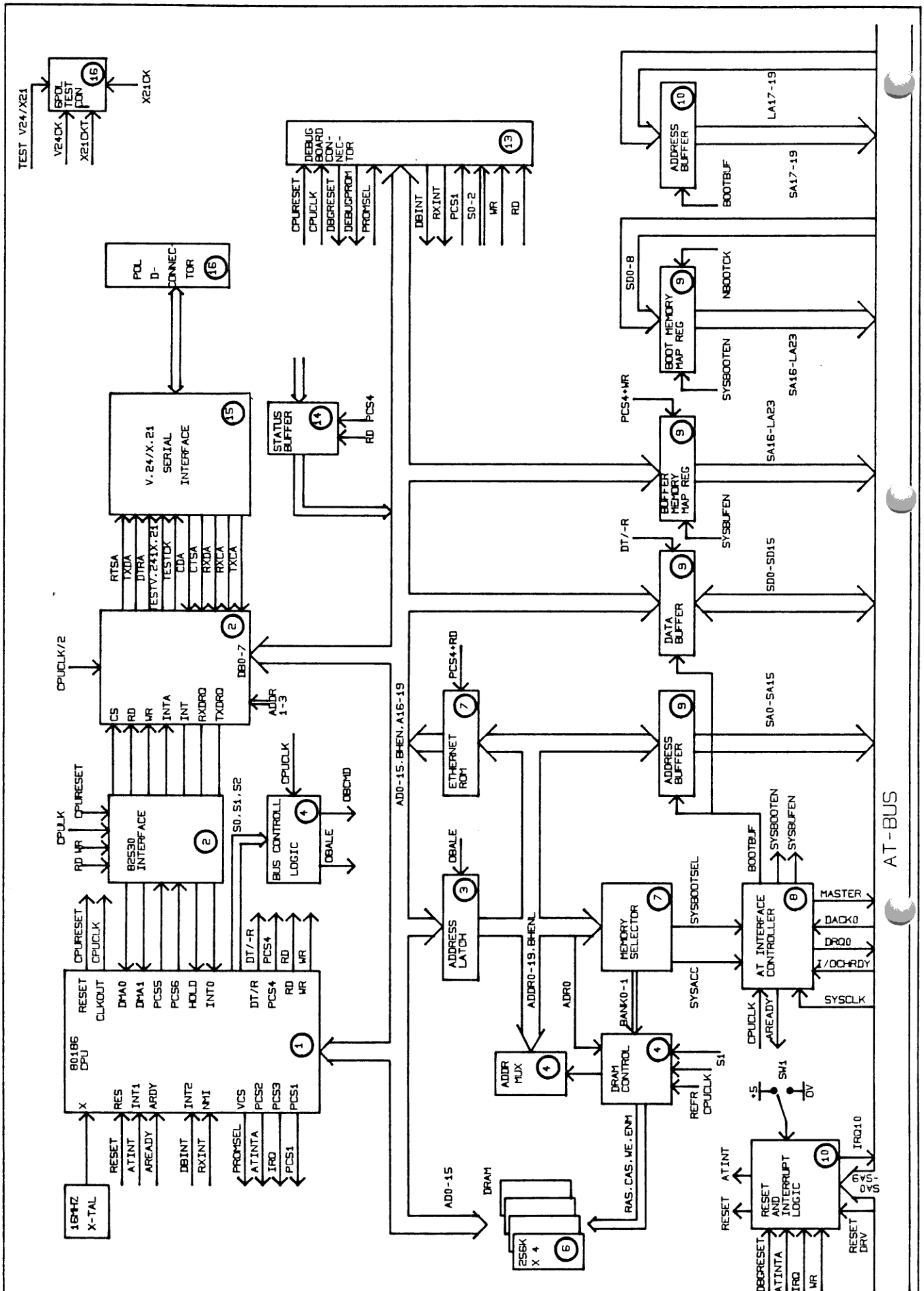
Fig. 3 shows a more detailed block diagram of the COM451 board. Some of the most important signal names are shown in fig. 3 and can be found in section 4.3. The numbers in circles refer to a diagram page number in section 4.3 where the group of logic can be found as electrical diagrams. In the rest of this section we refer to these diagram pages.

Diagram page 1 shows the 80186 CPU. The 80186 CPU are connected to provide ALE, WR and RD signals (no queue status data). A 16 MHz x-tal is connected to the 80186 providing the board with an 8 MHz CPU clock.

Diagram page 2 shows the 82530 Serial Communication controller and some interface logic to the 80186 CPU. The 82530 is clock by half the cpuclk i.e. by a 4 MHz clock signal.

The transmitting DMA request from the 82530 is clocked into a flip flop. This flip flop will be reset by the following writing to the 82530 with PCS5 asserted. PCS5 is controlled by the 80186 CPU.

The 82530 is reset by asserting the RD and WR input pins at the same time.



UNIT	DESIGN	
LAN451	JKA	
DWG. NO.	DRAWN AGA 870812	5

FIG.3

Interrupt acknowledge is performed by the 80186 CPU by asserting the PCS6 signal and placing a binary one on the ADDR3 address line.

Diagram page 3 shows the Address Latches and hold request logic. A read or write cycle to the 82530 will allways generate a hold request to the 80186 CPU. The duration of the hold request is approximately 2usec. This will delay the 80186 CPU preventing the CPU from accessing the 80530 SCC until 2usec. after the previous access.

Diagram page 4 contains three logic units:

- Bus Controll Logic
- DRAM Controller and
- DRAM Address Multiplexer.

The Bus Controll Logic generates the address latch enable signal 'OBALE' and an On Board Command signal for the Memory Selector and the DRAM Controller.

The DRAM Controller consists of a PAL16R6A device. the DRAM Controller generates controll signals to the DRAM devices:

- Row Address Strobe ('RAS0', 'RAS1')
- Column Address Strobe ('CAS')
- Write Enable ('WEHI', 'WELO')
- Enable Memory ('ENMEM0', 'ENMEM1')

Enable Memory is active when reading from the Local Memory.

On a request from the 80186 CPU timer0 ('REFR') the DRAM controller generates a 'CAS before RAS refresh' cycle to the DRAM devices. The DRAM devices contains an internal refresh counter. A refresh cycle can occur whenever the 80186 CPU are not accessing the Local Memory.

The DRAM Address Multiplexer generates the Row and Column addresses from the latched 16 addresses.

Diagram page 5 shows a Local Memory with 64Kx4bit DRAM devices. These devices is not mounted on the COM451 board.

Diagram page 6 shows a Local Memory with 256Kx4bit DRAM devices.

Diagram page 7 shows the Memory Selector.

The PAL16L8A constitutes the Memory Selector and the function can be described with the following table:

-,OBCMD	-,DEBUG PROM	A19	A18	A17	A16	-,BANK0	-,BANK1	-,SYS ACC	-,SYSBOOT SEL	
H	X	X	X	X	X	H	H	H	H	No access
L	X	0	X	X	X	L	H	H	H	80186 access
L	X	1	1	0	X	H	L	H	H	To Local Memory
L	X	1	1	1	0	H	H	L	H	80186 access to Buffer Memory
L	H	1	1	1	1	H	H	L	L	80186 access to Boot Memory
L	L	1	1	1	1	H	H	H	H	80186 access to Debug Board PROM

Notes: X indicates a dont care state
1 is equal to H (High) state
0 is equal to L (Low) state.

The 'SYSMENEN' enables two buffers, controlling the AT bus read and write signals, when the COM451 board has gained access to the AT bus ('MASTEREN' is active). When the 80186 CPU has gained access to the AT bus ('MASTEREN' = L) and is reading from or writing to the Local Memory the PAL will activate the refresh signal on the AT bus ('-,REFRESH = L'). Thus refreshing the System Memory is done when the 80186 is activating the '-,LOCK' signal.

Diagram page 8 shows the AT Interface Controller. When the 80186 access the System Memory the following sequence will occure:

1. '-,SYSACC' becomes active (L).
2. '-,DRQ' is activated by the PAT113.
   The 'AREADY' becomes active.
3. If another COM451 board has not activated the DRQ3 signal on the AT bus this COM451 board will clock the '-,DRQ' signal through U26 and activate the DRQ3 signal on the AT bus.

4. The system board answer by activating the '-,DACK0' signal which is gated into the COM451 board and the '-,OBDACK' signal becomes active.
5. 'OBDACK' is latched and the COM451 board will activate the 'MASTER' signal on AT bus and the 'MASTEREN' signal on the COM451 board.
6. The 80186 can now read from or write to the System Memory.
7. '-,SYSACC' is deactivated by the 80186 and the 'DRQ3' on the AT bus is also deactivated.

If the '-,LOCK' signal is activated by the 80186 the COM451 will occupy the AT bus in more than one memory cycle.

Diagram page 9 contains address buffers and data buffers interfacing the AT address and data bus.

Diagram page 10 shows the Reset and Interrupt Logic that consist of a PAL618 and a 74LS138. A number of latches are implemented in the PAT131 and these latches can be set and reset by writing to I/O addresses from the 80186 CPU and from the System board. The following table shows how:

Signal	Set by (Writing)	Reset by (Writing)
ATINT (Interrupt to 80186)	System board on I/O address 30FH(S1=L) or 30BH (S1=H)	80186 with PCS2 asserted (I/O address 100H-17FH)
IRQ11 (interrupt to system board)	80186 with PCS3 (I/O address 180H-1FFH)	System board on I/O address 30EH (S1=L) or 30AH (S1=H).
RESET	System board on I/O address 30DH (S1=L) or 309H (S1=H) or by System board RESET DRV signal	System board on I/O address 30CH (S1=L) or 308H (S1=H) or by Debug board.

When the system board is deactivating the 'RESET' signal a clock signal will be generated to the Boot Memory Map register and this register will thus be loaded by the system board.

Diagram page 11 and 12 shows the AT bus connection.

Diagram page 13 shows the Debug Board connection.

Diagram page 14 shows a buffer through which the 80186 CPU can read a number of control signals from the serial V.24 and X.21 interface. The SELX.21 signal is asserted if an X.21 cable is connected to the COM451 board.

Diagram page 15 shows the V.24 and X.21 serial interface.
the V.24 interface includes the following signals:

REQ TO SEND
DATA TERM READY
TRANSMIT DATA
REC DATA
REC CLOCK
TRANSM CLOCK
TEST INDICATOR
CALLING INDICATOR
DATA CARRIER DET
DATA SET READY
CLEAR TO SEND

The X.21 interface includes the following blanced signals:

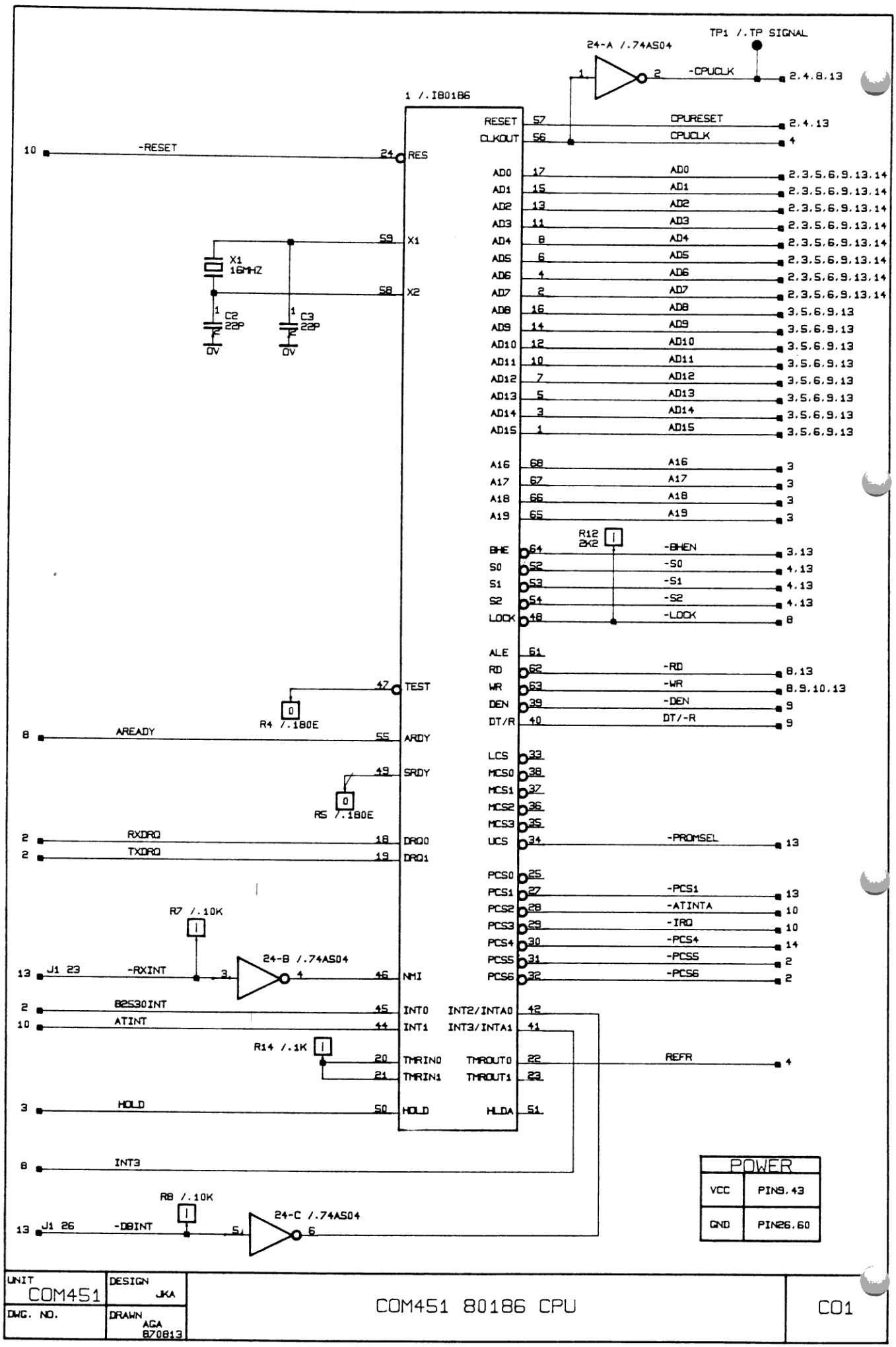
T(B),T(A)
C(B),C(A)
R(B),R(A)
I(B),I(A)
S(B),S(B)

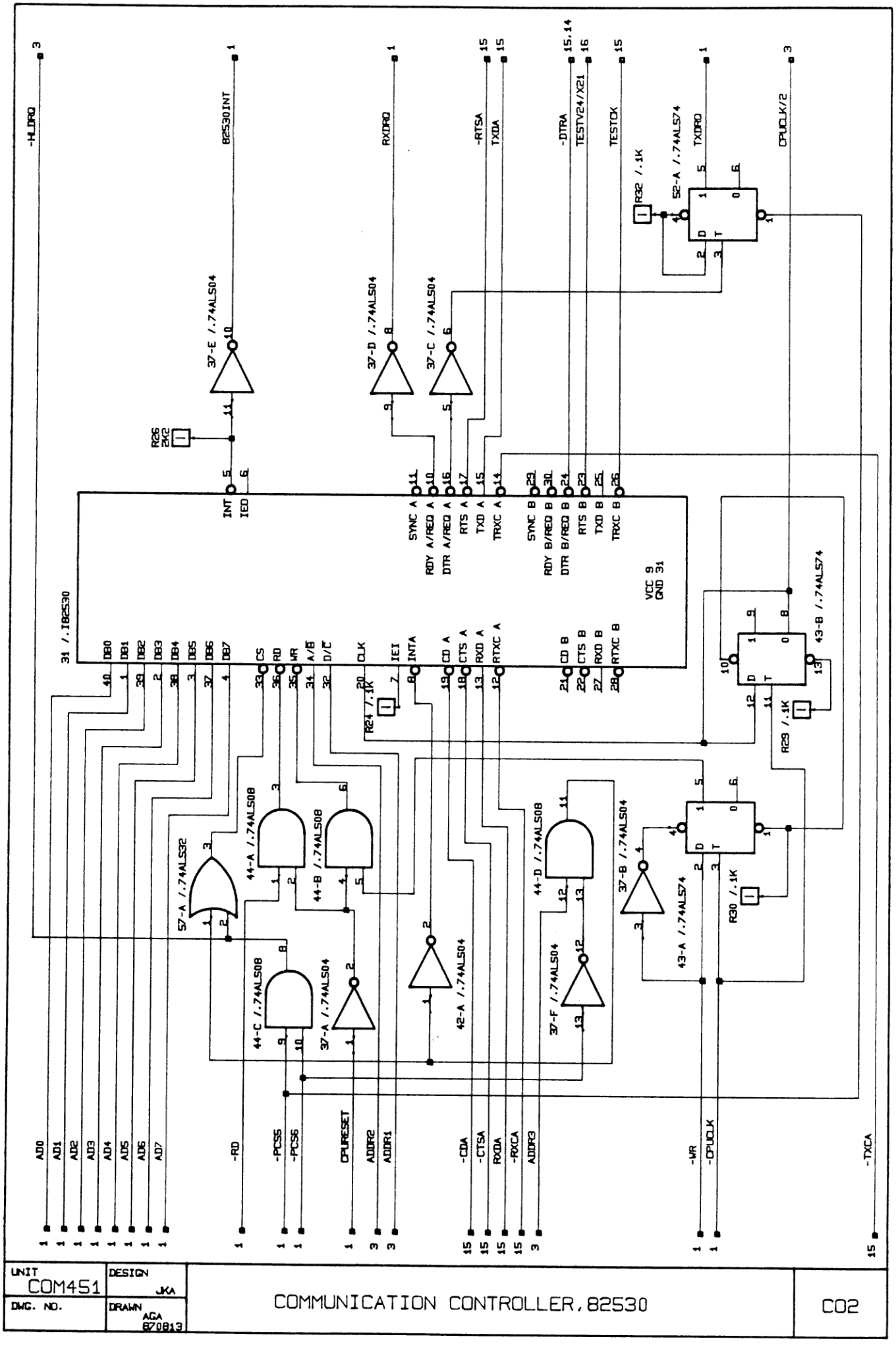
The following signals are testsignals:

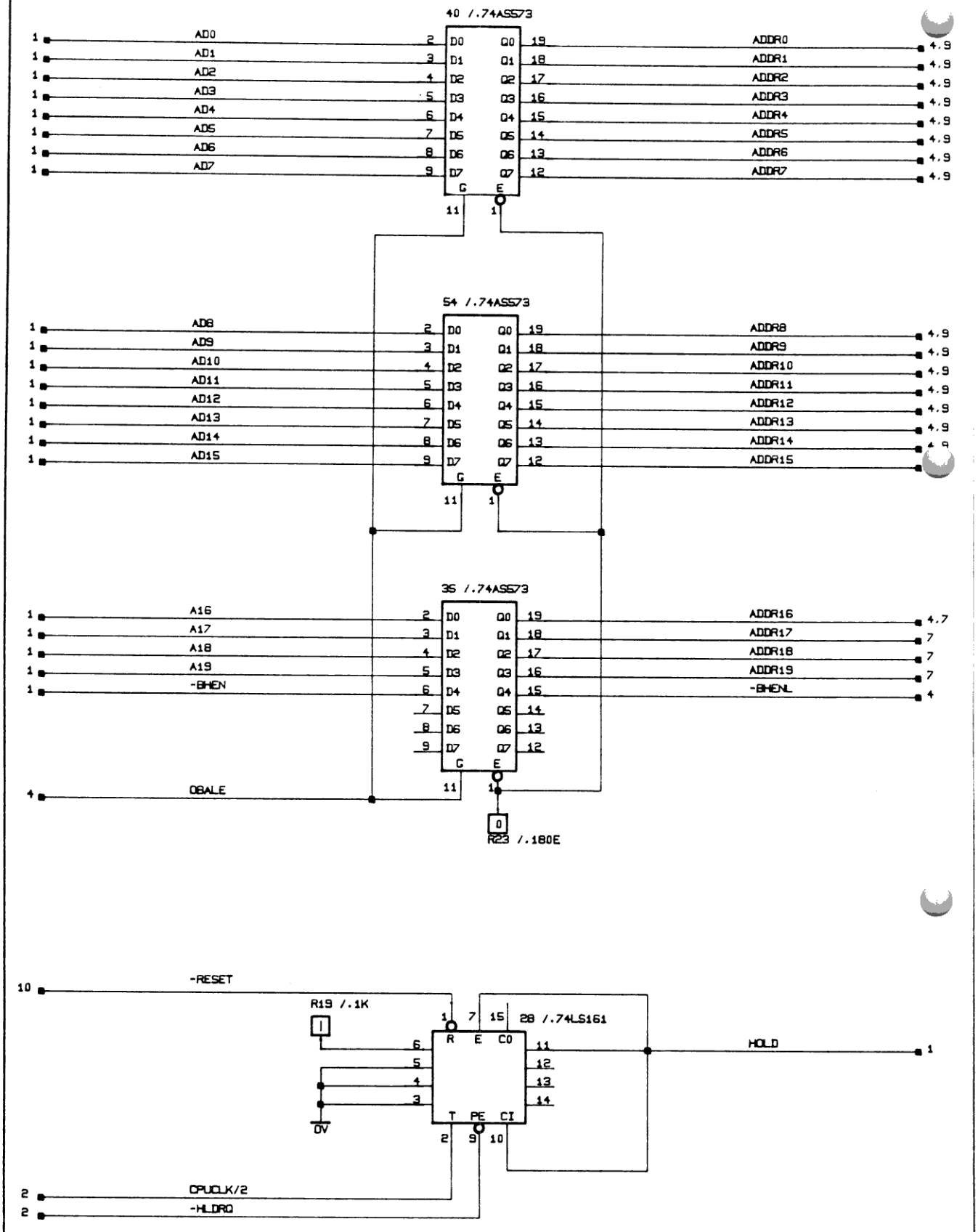
V24CK
X21CK+, X21CK-

Diagram page 16 shows the 25 pol D-connector for modem connection and a 6 pol test connector. A test cable (KBL889) can be plugged into the 25 pol D-connector and INTO the test connector providing the technician with facilities to test the serial interface, see (4).

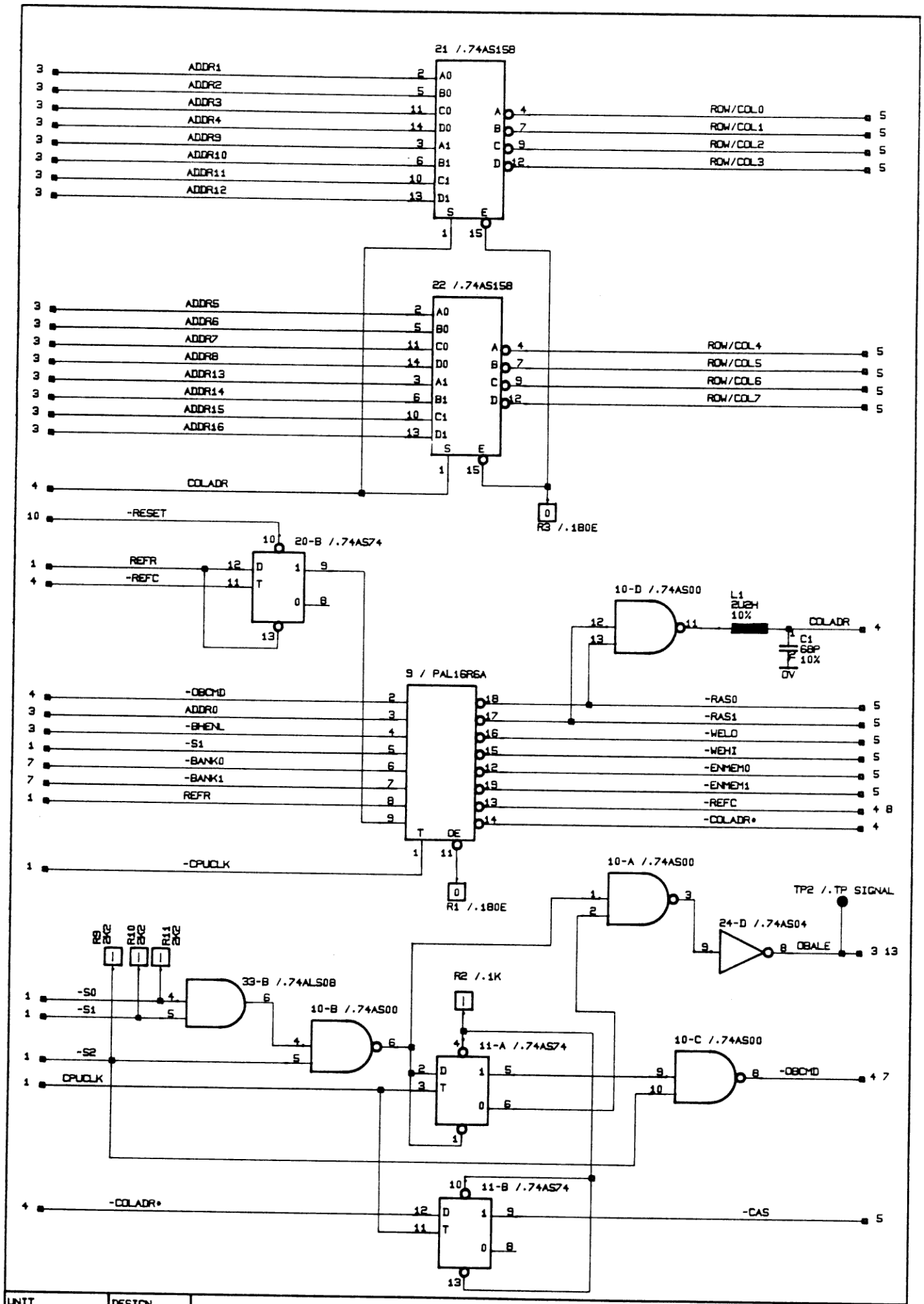
4.3 Logic Diagrams

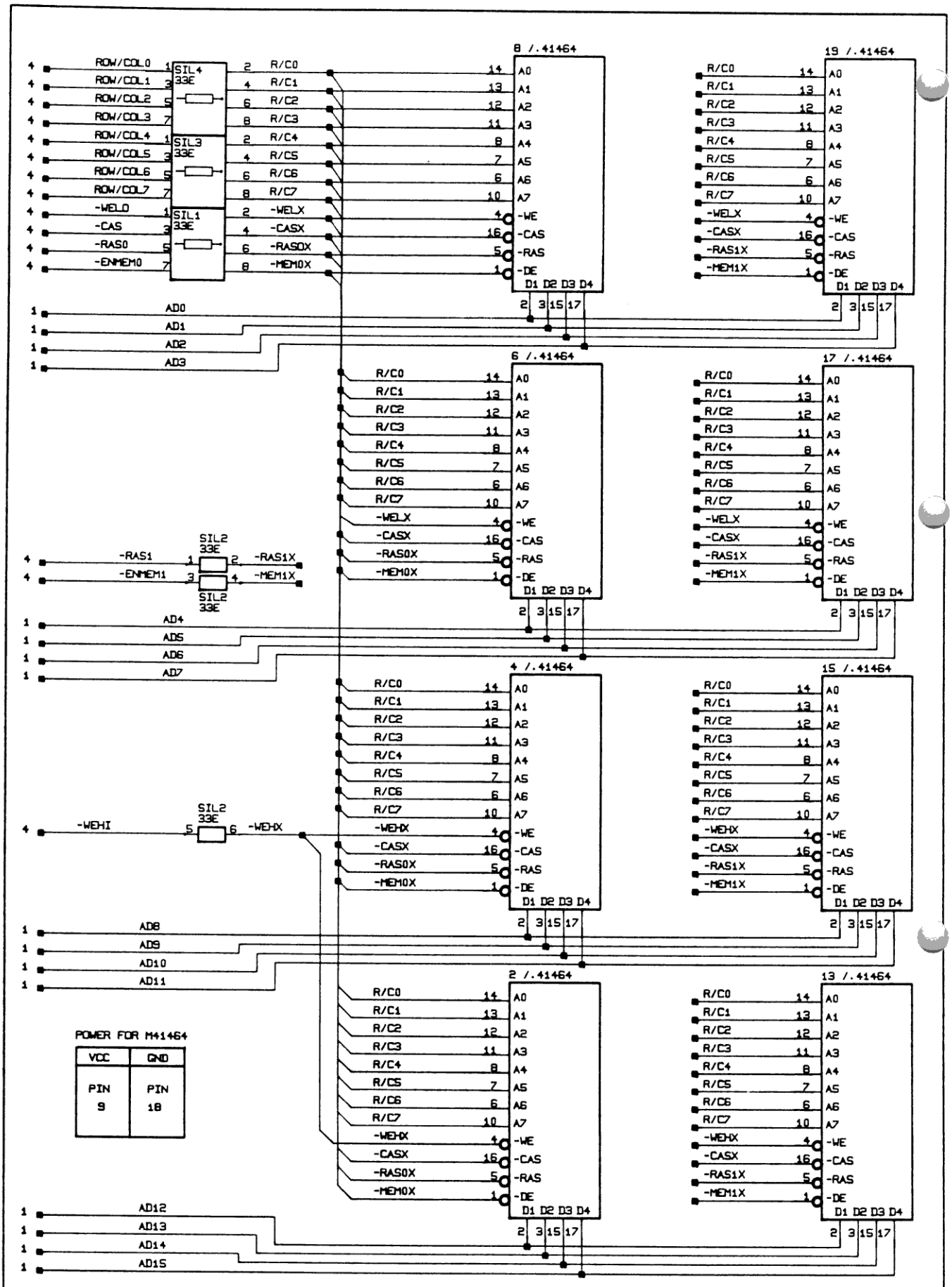

TP1 /.TP SIGNAL
24-A /.74AS04
-CPUCLK
2,4,8,13
1 /.I80186
RESET
CLKOUT
CPURESET
CPUCLK
-RESET
RES
X1
X2
X1
16MHZ
C2
22P
C3
22P
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
A16
A17
A18
A19
R12
2K2
BHE
S0
S1
S2
LOCK
-BHEN
-S0
-S1
-S2
-LOCK
ALE
RD
WR
DEN
DT/R
-RD
-WR
-DEN
DT/-R
TEST
R4 /.180E
AREADY
ARDY
SRDY
R5 /.180E
RXDRQ
TXDRQ
DRQ0
DRQ1
LCS
MCS0
MCS1
MCS2
MCS3
UCS
-PROMSEL
PCS0
PCS1
PCS2
PCS3
PCS4
PCS5
PCS6
-PCS1
-ATINTA
-IRQ
-PCS4
-PCS5
-PCS6
R7 /.10K
24-B /.74AS04
J1 23
-RXINT
NMI
82530INT
ATINT
INT0
INT1
INT2/INTA0
INT3/INTA1
R14 /.1K
TMRIN0
TMRIN1
TMROUT0
TMROUT1
REFR
HOLD
HLDA
INT3
R8 /.10K
24-C /.74AS04
J1 26
-DBINT
POWER
VCC
PIN9,43
GND
PIN26,60
UNIT
COM451
DESIGN
JKA
DWG. NO.
DRAWN
AGA
870813
COM451 80186 CPU
C01


-HLDRQ
82530INT
RXDRQ
-RTSA
TXDA
-DTRA
TESTV24/X21
TESTCK
CPUCLK/2
TXDRQ
31 /.182530
37-E /.74ALS04
37-D /.74ALS04
37-C /.74ALS04
52-A /.74ALS74
R32 /.1K
R26 2K2
R24 /.1K
R29 /.1K
R30 /.1K
43-B /.74ALS74
43-A /.74ALS74
44-A /.74ALS08
44-B /.74ALS08
44-C /.74ALS08
44-D /.74ALS08
57-A /.74ALS32
37-A /.74ALS04
37-B /.74ALS04
37-F /.74ALS04
42-A /.74ALS04
INT
IED
SYNC A
RDY A/REQ A
DTR A/REQ A
RTS A
TXD A
TRXC A
SYNC B
RDY B/REQ B
DTR B/REQ B
RTS B
TXD B
TRXC B
VCC 9
GND 31
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
CS
RD
WR
A/B
D/C
CLK
IEI
INTA
CD A
CTS A
RXD A
RTXC A
CD B
CTS B
RXD B
RTXC B
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
-RD
-PCS5
-PCS6
CPURESET
ADDR2
ADDR1
-CDA
-CTSA
RXDA
-RXCA
ADDR3
-WR
-CPUCLK
-TXCA
UNIT
COM451
DESIGN
JKA
DWG. NO.
DRAWN
AGA
870813
COMMUNICATION CONTROLLER, 82530
C02

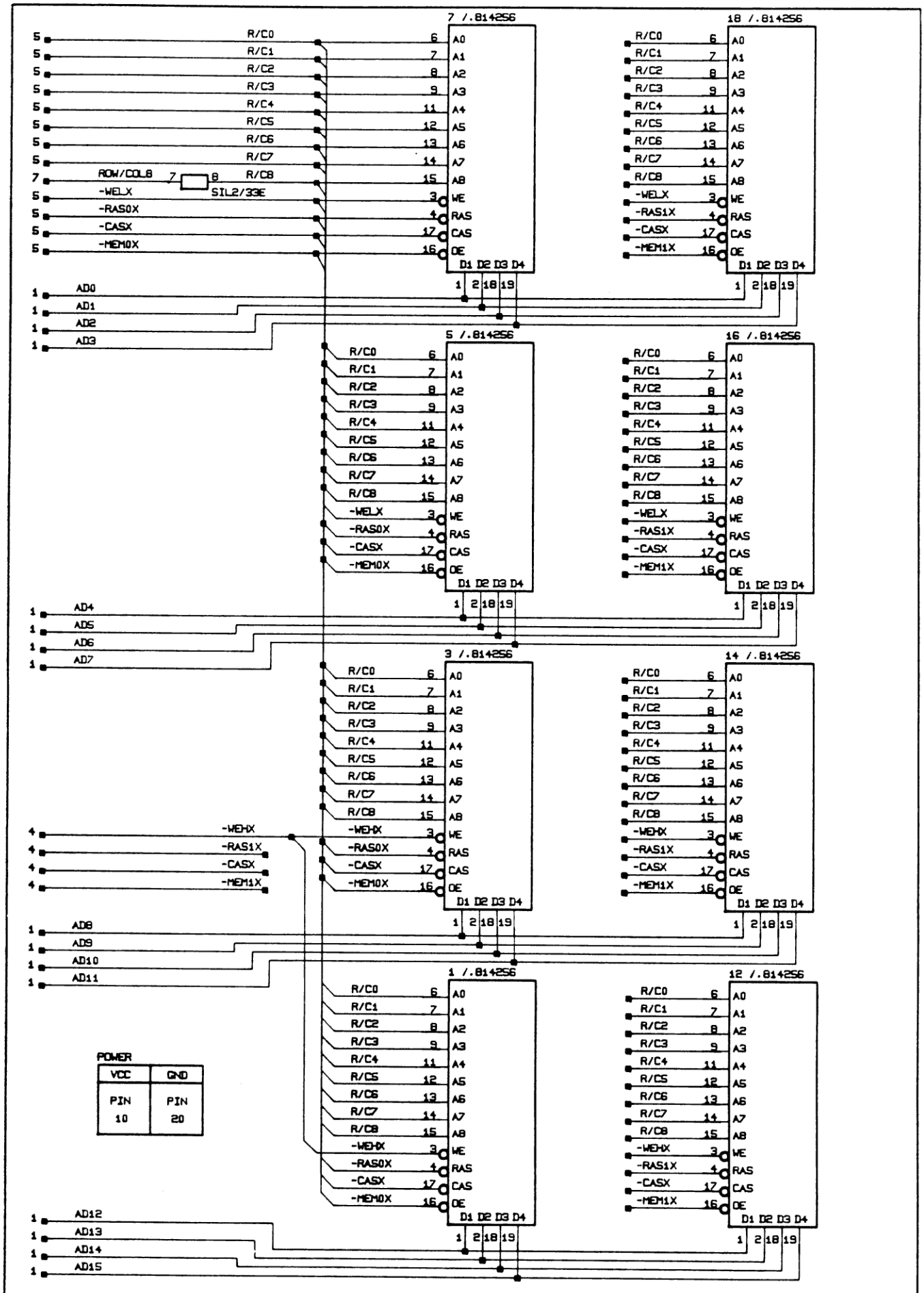


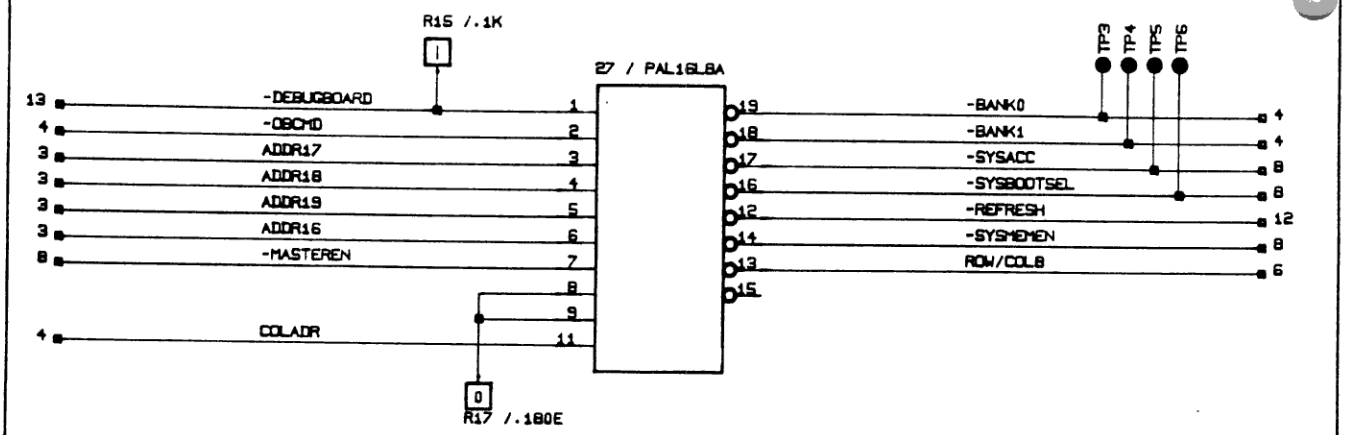
UNIT	DESIGN		
COM451	JKA	ADDRESS LATCH AND HOLD REQUEST LOGIC	C03
DWG. NO.	DRAWN AGA 870813		


21 /.74AS158
ADDR1
ADDR2
ADDR3
ADDR4
ADDR9
ADDR10
ADDR11
ADDR12
ROW/COL0
ROW/COL1
ROW/COL2
ROW/COL3
22 /.74AS158
ADDR5
ADDR6
ADDR7
ADDR8
ADDR13
ADDR14
ADDR15
ADDR16
ROW/COL4
ROW/COL5
ROW/COL6
ROW/COL7
COLADR
R3 /.180E
-RESET
20-B /.74AS74
REFR
-REFC
10-D /.74AS00
L1
2U2H
10%
C1
68P
10%
9 / PAL16R6A
-OBCMD
ADDR0
-BHENL
-S1
-BANK0
-BANK1
-CPUCLK
-RAS0
-RAS1
-WELO
-WEHI
-ENMEM0
-ENMEM1
-REFC
-COLADR*
R1 /.180E
10-A /.74AS00
TP2 /.TP SIGNAL
24-D /.74AS04
OBALE
R9 2K2
R10 2K2
R11 2K2
33-B /.74ALS08
-S0
-S1
-S2
CPUCLK
10-B /.74AS00
R2 /.1K
11-A /.74AS74
10-C /.74AS00
11-B /.74AS74
-CAS
UNIT COM451
DESIGN JKA
DWG. NO.
DRAWN AGA 870813
DRAM CONTROLLER
C04

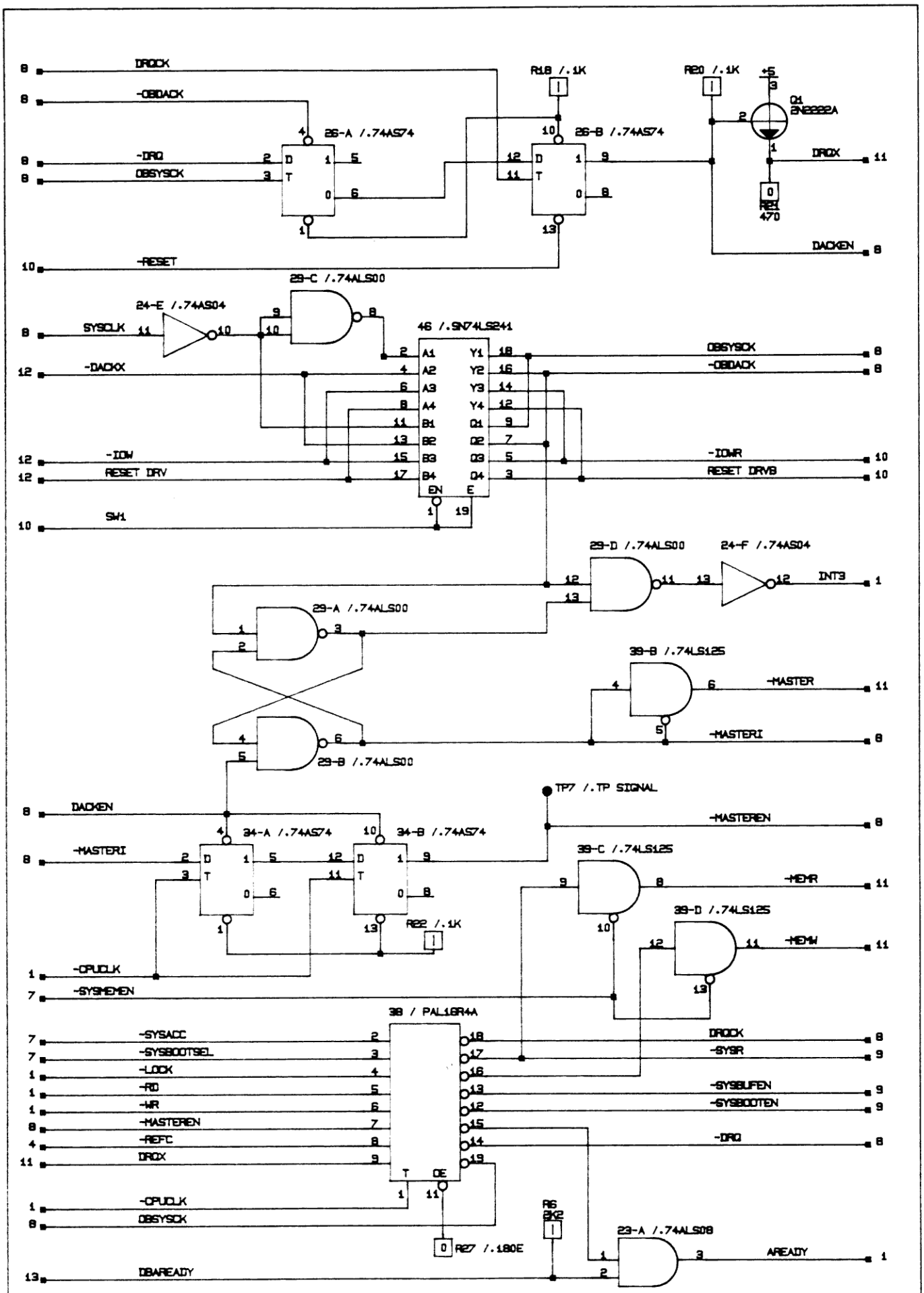


UNIT	DESIGN		
COM451	JKA. THJ	128K/256K RAM ARRAY	C05
DWG. NO.	DRAWN AGA 870813		

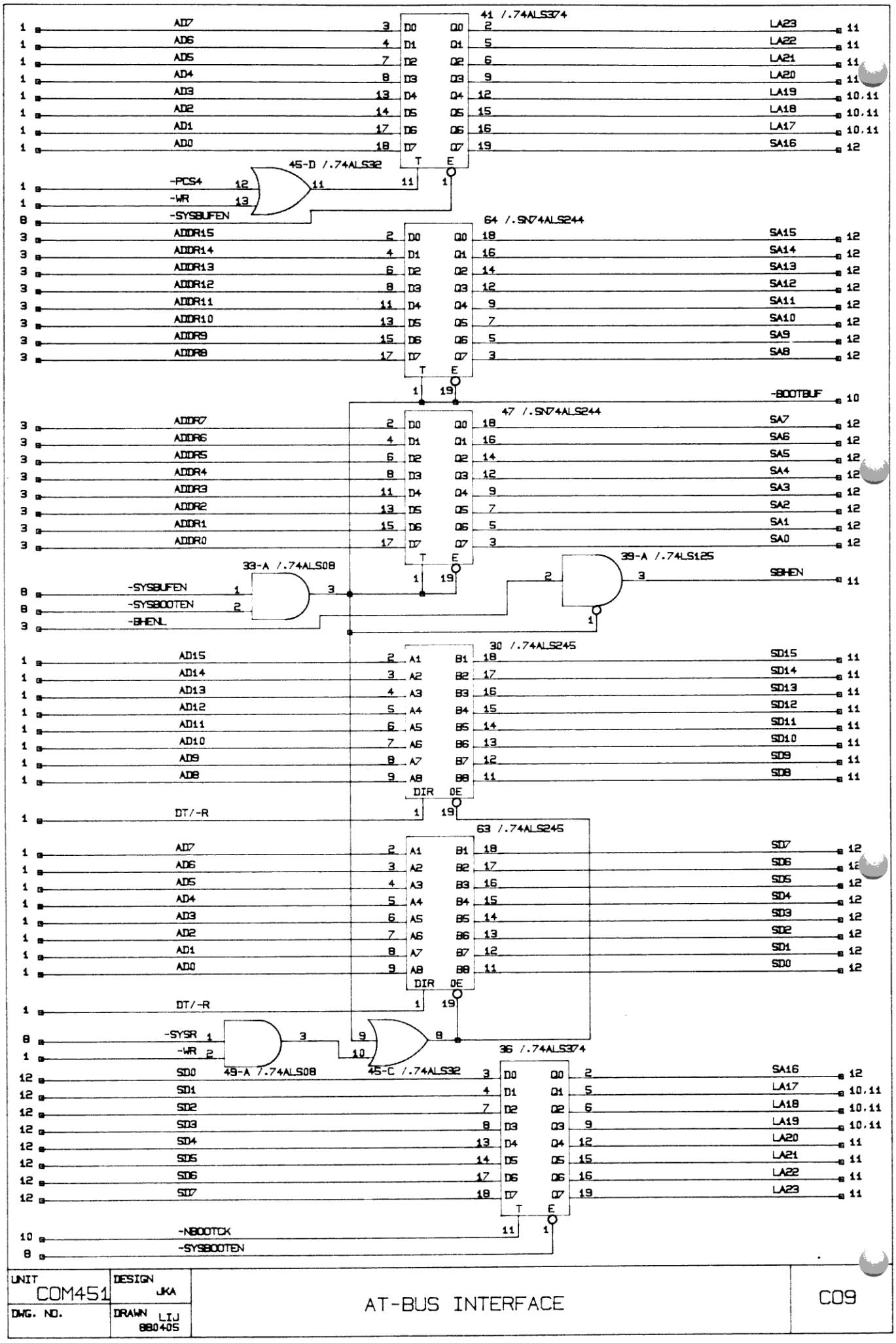

7 /.814256
18 /.814256
5 /.814256
16 /.814256
3 /.814256
14 /.814256
1 /.814256
12 /.814256
R/C0
R/C1
R/C2
R/C3
R/C4
R/C5
R/C6
R/C7
R/C8
ROW/COL8
SIL2/33E
-WELX
-RAS0X
-CASX
-MEM0X
-RAS1X
-MEM1X
-WEHX
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
A0
A1
A2
A3
A4
A5
A6
A7
A8
WE
RAS
CAS
OE
D1 D2 D3 D4
POWER
VCC
GND
PIN 10
PIN 20
UNIT
COM451
DESIGN
THU.JKA
DWG. NO.
DRAWN
AGA 870813
512K / 1M RAM ARRAY
C06



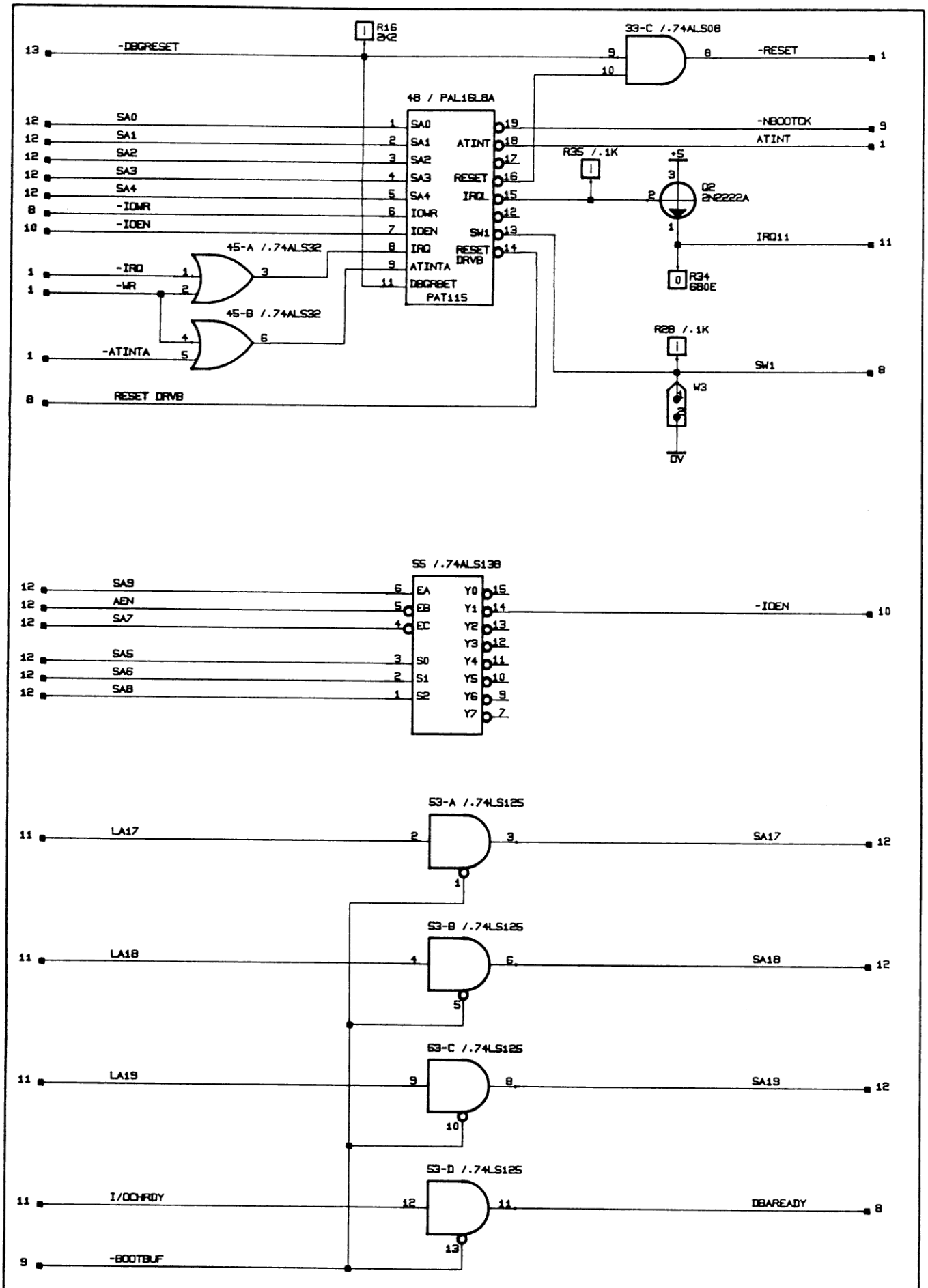
UNIT COM451	DESIGN JKA	MEMORY ADDRESS DECODER	C07
DWG. NO.	DRAWN AGA 870813		



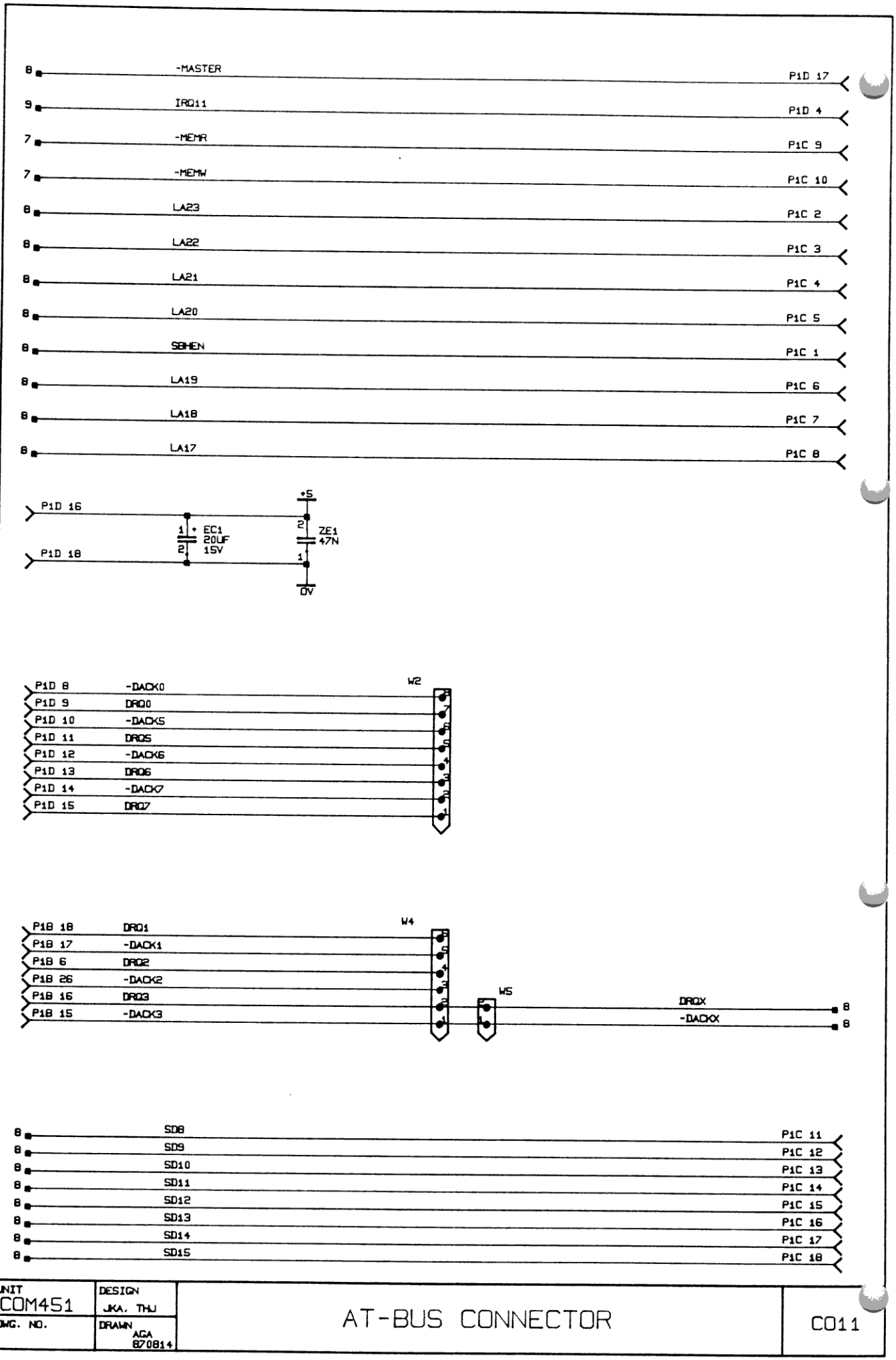
UNIT COM451	DESIGN JKA	AT-BUS INTERFACE CONTROLLER	C08
DWG. NO.	DRAWN LIJ 880407		



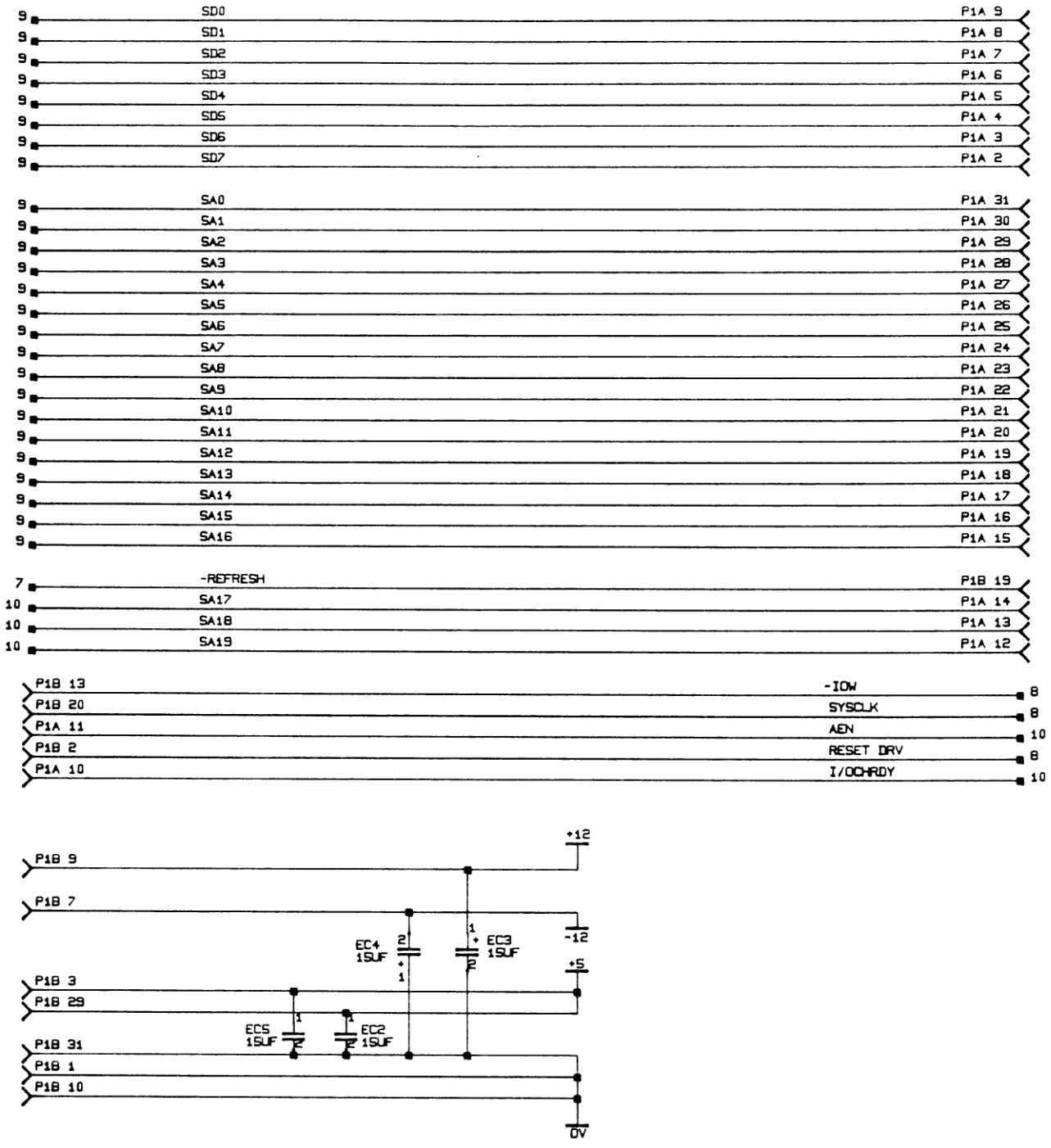
UNIT	DESIGN		
COM451	JKA	AT-BUS INTERFACE	C09
DWG. NO.	DRAWN LIJ 880405		



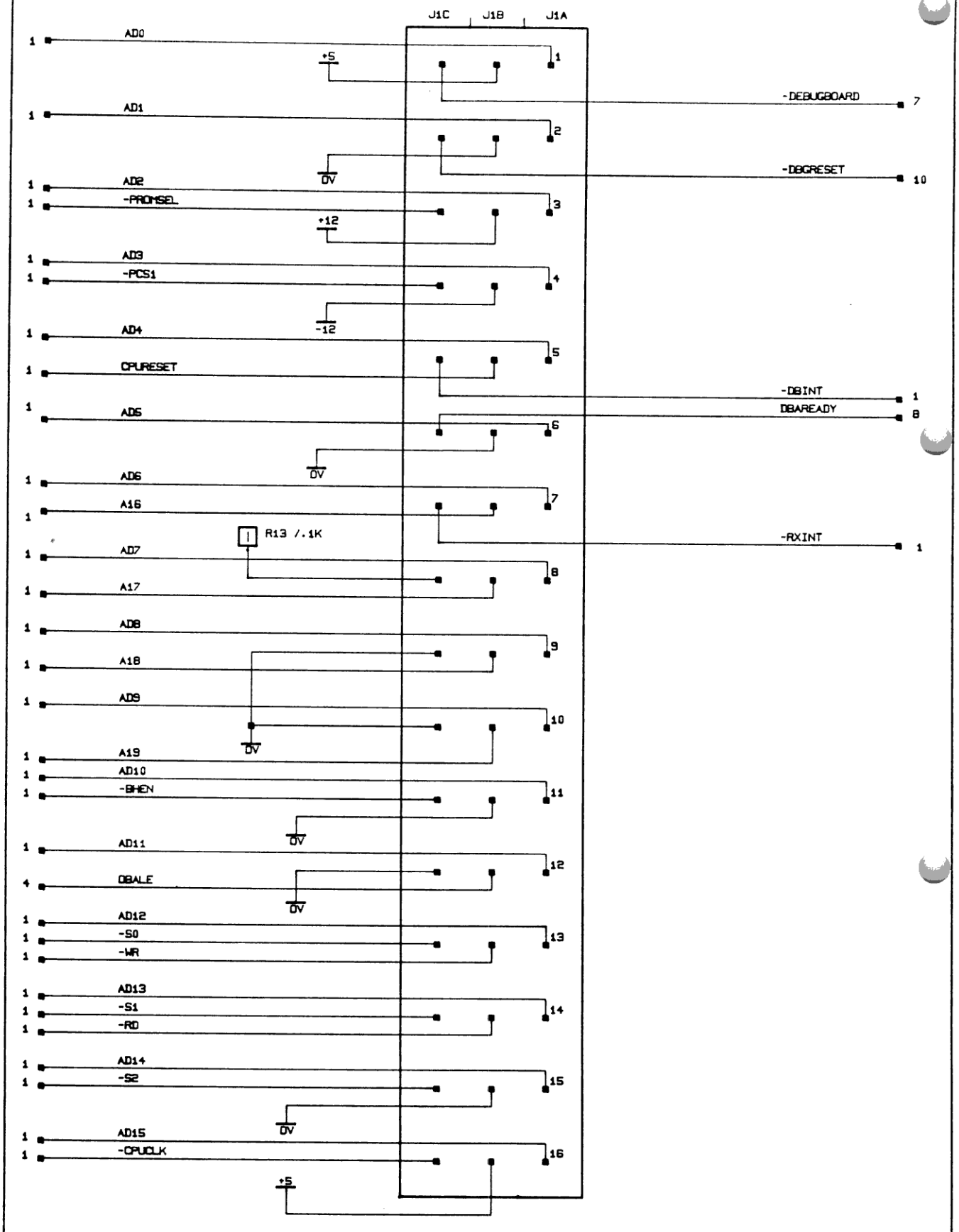
UNIT	DESIGN		
COM451	JKA	RESET AND INTERRUPT LOGIC	C010
DWG. NO.	DRAWN AGA 870814		



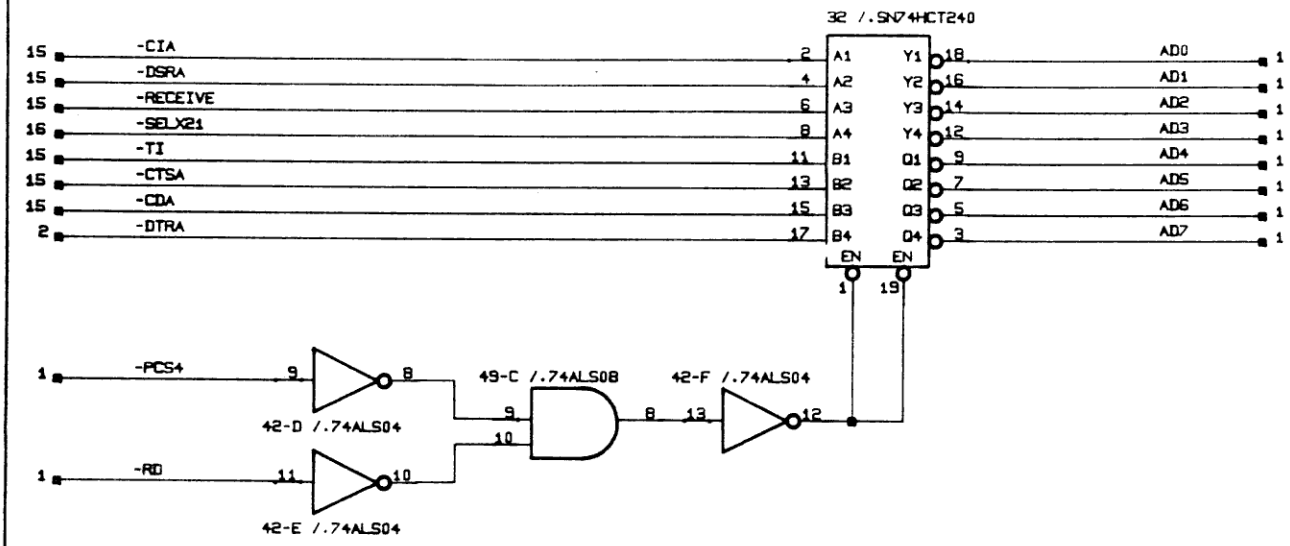
UNIT	DESIGN		
COM451	JKA, THJ	AT-BUS CONNECTOR	C011
DWG. NO.	DRAWN AGA 870814		



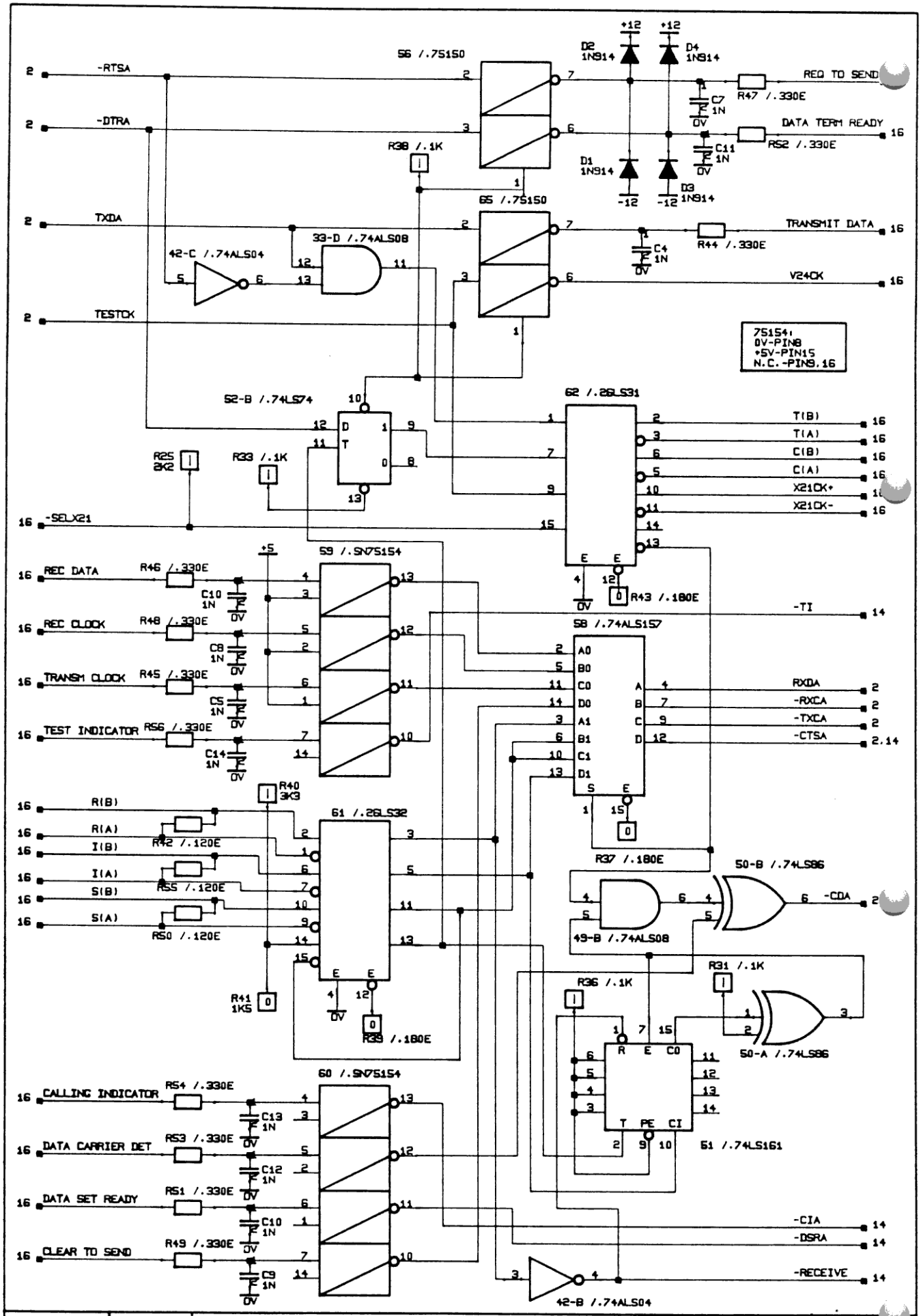
UNIT	DESIGN		
COM451	JKA	AT-BUS CONNECTOR	C012
DWG. NO.	DRAWN AGA 870814		

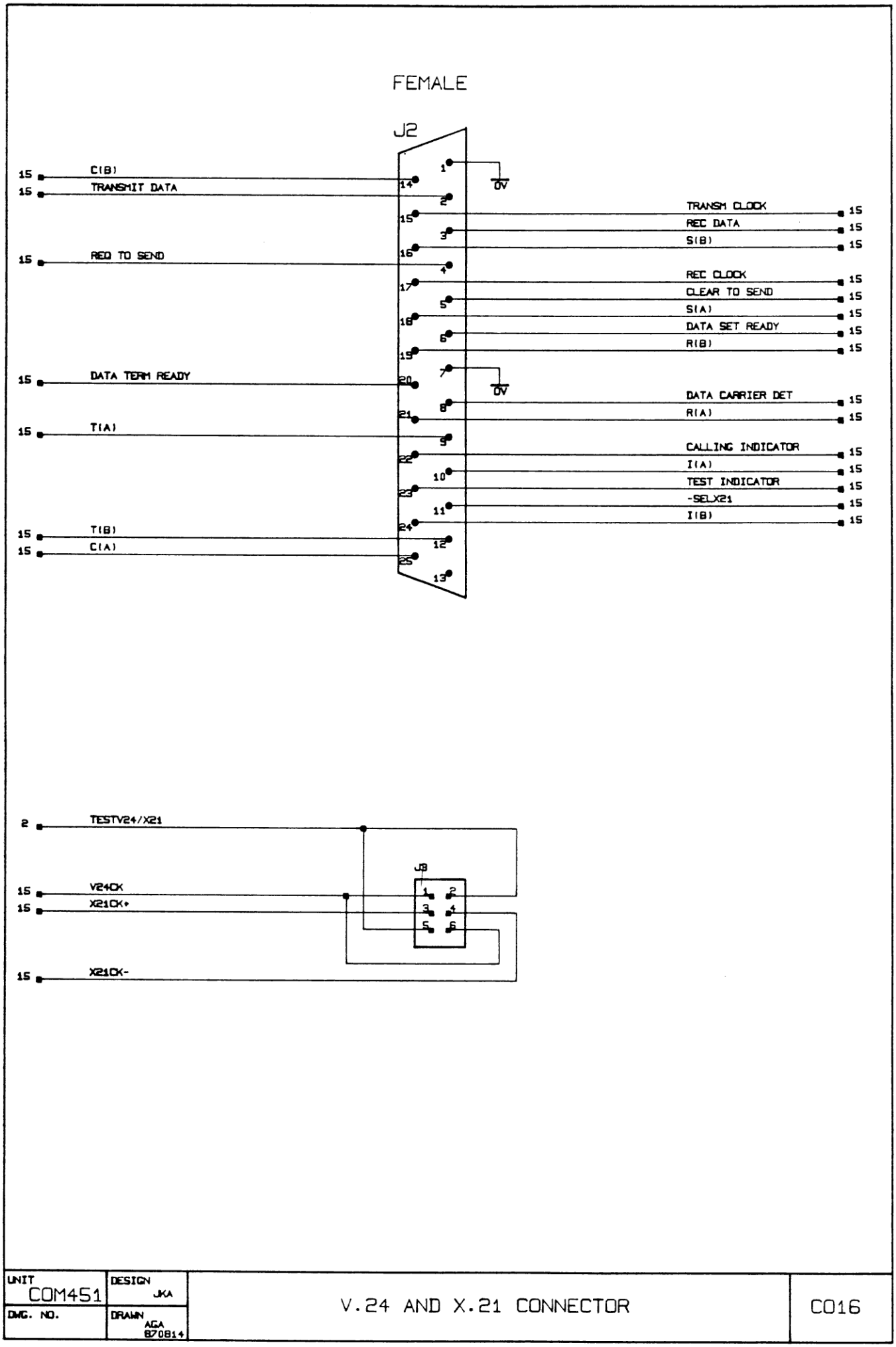


UNIT	DESIGN		
COM451	JKA	DEBUG BOARD CONNECTOR	C013
DWG. NO.	DRAWN AGA 870814		



UNIT	DESIGN		
COM451	JKA	V.24 AND X.21 CONTROL SIGNAL BUFFER	CO14
DWG. NO.	DRAWN AGA 870814		


56 /.75150
65 /.75150
D2 1N914
D4 1N914
D1 1N914
D3 1N914
+12
-12
-RTSA
-DTRA
TXDA
TESTCK
REQ TO SEND
DATA TERM READY
TRANSMIT DATA
V24CK
R47 /.330E
RS2 /.330E
R44 /.330E
C7 1N
C11 1N
C4 1N
R38 /.1K
33-D /.74ALS08
42-C /.74ALS04
75154: 0V-PIN8 +5V-PIN15 N.C.-PINS 16
52-B /.74LS74
62 /.26LS31
T(B)
T(A)
C(B)
C(A)
X21CK+
X21CK-
R25 2K2
R33 /.1K
-SELX21
R43 /.180E
59 /.SN75154
REC DATA
REC CLOCK
TRANSM CLOCK
TEST INDICATOR
R46 /.330E
R48 /.330E
R45 /.330E
RS6 /.330E
C10 1N
C8 1N
C5 1N
C14 1N
-TI
58 /.74ALS157
RXDA
-RXCA
-TXCA
-CTSA
R40 3K3
R(B)
R(A)
I(B)
I(A)
S(B)
S(A)
R42 /.120E
RS5 /.120E
RS0 /.120E
61 /.26LS32
R41 1K5
R39 /.180E
R37 /.180E
50-B /.74LS86
49-B /.74ALS08
-CDA
R31 /.1K
R36 /.1K
50-A /.74LS86
60 /.SN75154
CALLING INDICATOR
DATA CARRIER DET
DATA SET READY
CLEAR TO SEND
RS4 /.330E
RS3 /.330E
RS1 /.330E
R49 /.330E
C13 1N
C12 1N
C10 1N
C9 1N
51 /.74LS161
-CIA
-DSRA
-RECEIVE
42-B /.74ALS04
UNIT COM451
DESIGN JKA
DWG. NO.
DRAWN AGA 870814
V.24 AND X.21 SERIAL INTERFACE
C015



UNIT	DESIGN		
COM451	JKA	V.24 AND X.21 CONNECTOR	C016
DWG. NO.	DRAWN AGA 870814		

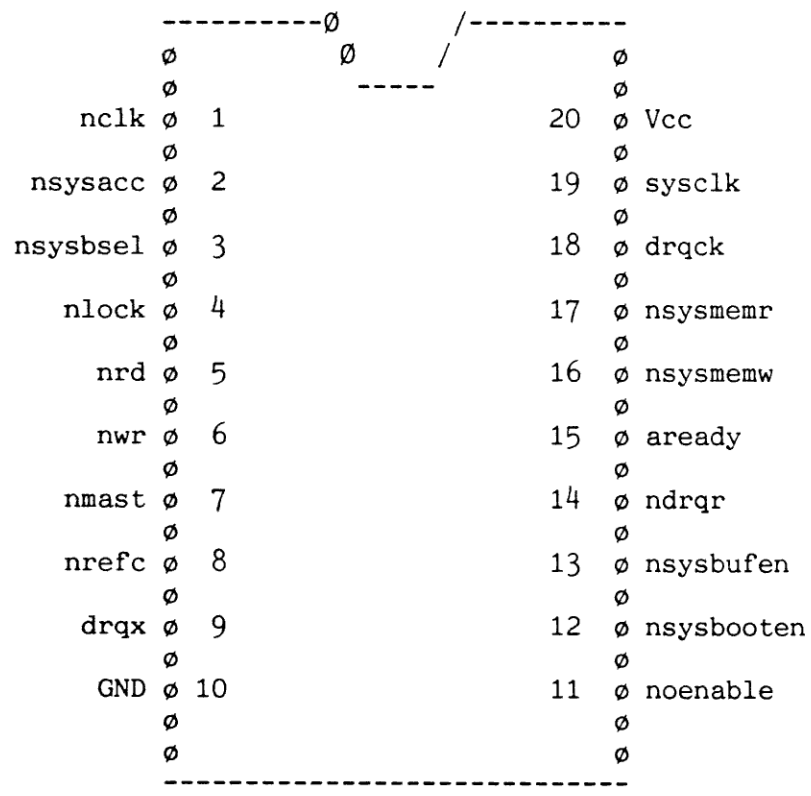
4.4 PAL and ROM description

```
                                                                    Page 1
ABEL(tm) Version 2.02a  -  Document Generator          03-Apr-87 01:42 PM
LAN451 I/O BUS Controller, 2. FEB. 1987 ,
                Jens K. Andreassen , Regnecentralen A/S,
                Ballerup
Equations for Module PAT113TX

Device PAT113


     Reduced Equations:

       enable nsysbooten = (1);

       enable nsysbufen = (1);

       enable drqck = (1);

       enable sysclk = (0);

       nsysbooten = !(!nsysbooten & !nsysmemr
                    # !nsysbooten & !nsysmemw
                    # !nmast & !nsysacc & !nsysbsel);


       nsysbufen = !(!nsysbufen & !nsysmemr
                   # !nsysbufen & !nsysmemw
                   # !nmast & !nsysacc & nsysbsel);


       ndrqr := !(!nsysacc # !ndrqr & !nlock);

       aready := !(nmast & !nsysacc
                 # !nrefc & nsysacc
                 # !nmast & nrd & nwr);


       nsysmemw := !(!nmast & !nsysacc & !nwr);

       nsysmemr := !(!nmast & !nrd & !nsysacc);

       drqck = !(sysclk
               # drqx & !ndrqr
               # drqx & sysclk
               # !ndrqr & sysclk
               # ndrqr & sysclk);
```

ABEL(tm) Version 2.02a - Document Generator 03-Apr-87 01:42 PM
LAN451 I/O BUS Controller, 2. FEB. 1987 ,
Jens K. Andreassen , Regnecentralen A/S,
Ballerup
Chip diagram for Module PAT113TX

Device PAT113

P16R4



end of module PAT113TX

COM451 I/O interrupt and reset , 30. MARTS 1987,
Jens K. Andreassen , Regnecentralen A/S,Ballerup
Equations for Module PAT131TX

Device PAT131

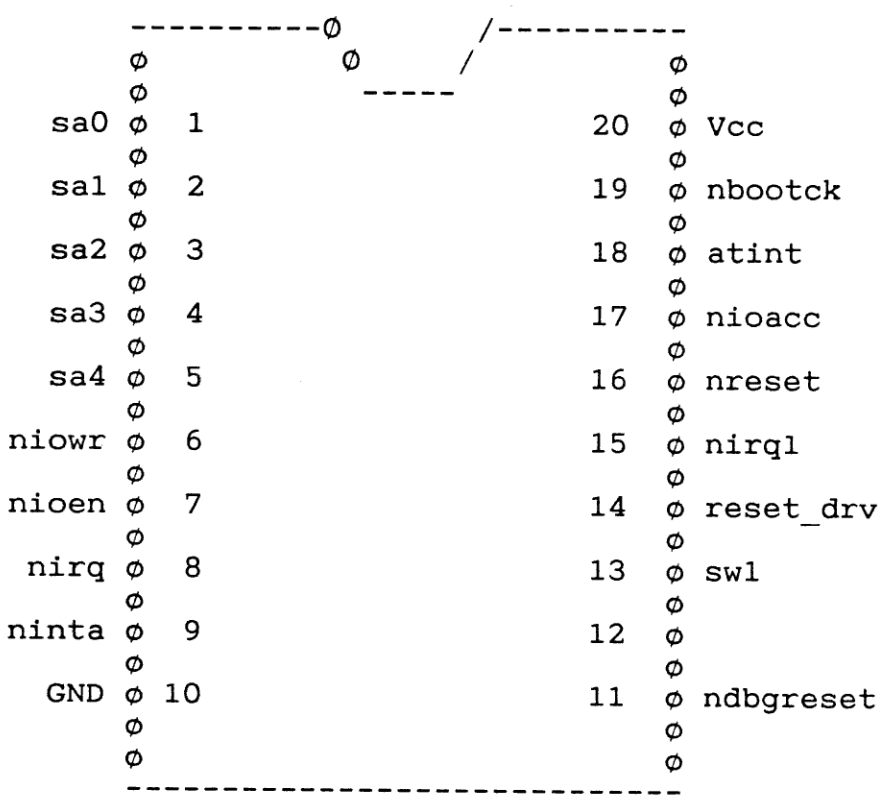
Reduced Equations:

```
enable nioacc = (1);

enable atint = (1);

enable reset_drv = (0);

enable sw1 = (0);

enable nirq1 = (1);

enable nreset = (1);

enable nbootck = (1);

nbootck = !(!nioacc & !sa0 & !sa1);

nioacc = !(!nioen & !niowr & !sa2 & sa3 & !sa4 & sw1
         # !nioen & !niowr & sa2 & sa3 & !sa4 & !sw1);


nreset = !(ndbgreset & reset_drv
          # ndbgreset & nioacc & !nreset
          # ndbgreset & !nreset & sa0
          # ndbgreset & !nreset & sa1
          # ndbgreset & !nioacc & sa0 & !sa1);


atint = !(!ndbgreset
         # !ninta
         # !nreset
         # !atint & nioacc
         # !atint & !sa0
         # !atint & !sa1);


nirq1 = !(!ndbgreset
         # !nreset
         # nirq & !nirq1
         # !nioacc & !sa0 & sa1);
```

ABEL(tm) Version 2.02a - Document Generator 03-Apr-87 01:55 PM
COM451 I/O interrupt and reset , 30. MARTS 1987,
Jens K. Andreassen , Regnecentralen A/S,Ballerup
Chip diagram for Module PAT131TX

Device PAT131

P16L8



end of module PAT131TX

Jens K. Andreassen, Regnecentralen A/S, BALLERUP
Equations for Module PAT116TX

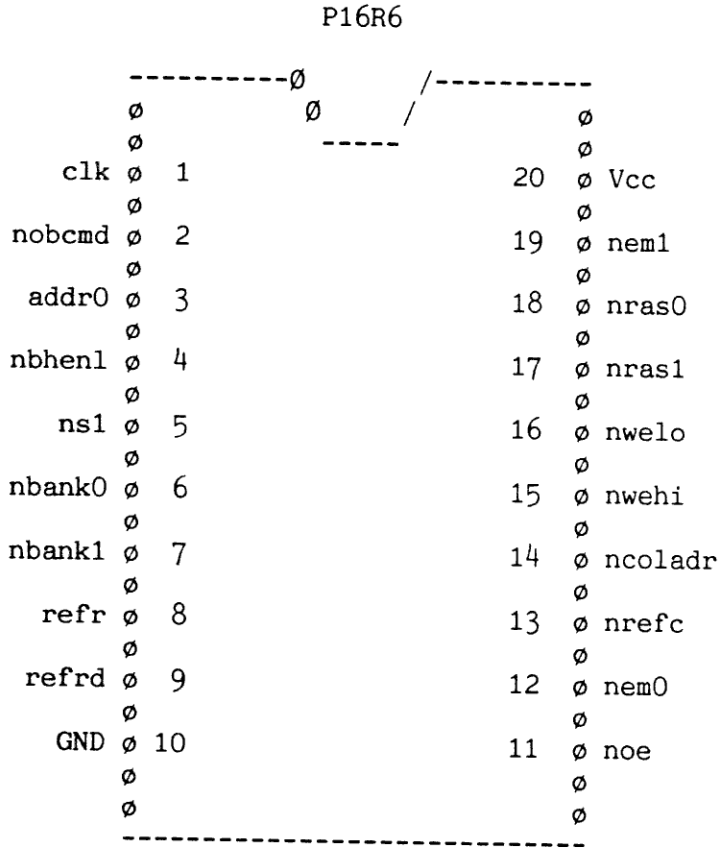
Device PAT116

Reduced Equations:

```
enable nem0 = (1);

enable nem1 = (1);

nem0 = !(!ncoladr & !nras0 & nrefc & !ns1);

nem1 = !(!ncoladr & !nras1 & nrefc & !ns1);

nras0 := !(!ncoladr & !nrefc # !nbank0 & !nobcmd & nrefc);

nras1 := !(!ncoladr & !nrefc # !nbank1 & !nobcmd & nrefc);

nwelo := !(!addr0 & !nbank0 & ncoladr & !nobcmd & nrefc & ns1
        # !addr0 & !nbank1 & ncoladr & !nobcmd & nrefc & ns1);


nwehi := !(!nbank0 & !nbhen1 & ncoladr & !nobcmd & nrefc & ns1
        # !nbank1 & !nbhen1 & ncoladr & !nobcmd & nrefc & ns1);


nrefc := !(!ncoladr & !nrefc & refr & !refrd
        # nbank0 & nbank1 & nrefc & refr & !refrd
        # ncoladr & nras0 & !nrefc & refr & !refrd);


ncoladr := !(nras0 & !nrefc
          # !nbank0 & !nobcmd & nrefc
          # !nbank1 & !nobcmd & nrefc);
```

ABEL(tm) Version 2.02a - Document Generator 03-Apr-87 12:40 PM
LAN451 DRAM controller .21 jan 1987
Jens K. Andreassen, Regnecentralen A/S, BALLERUP
Chip diagram for Module PAT116TX

Device PAT116



end of module PAT116TX

ABEL(tm) Version 2.02a - Document Generator 05-May-87 01:38 PM
LAN451 Memory selector, 29. JAN. 1987,
Jens K. Andreassen, Regnecentralen A/S , Ballerup
Equations for Module PAT117TX

Device PAT117

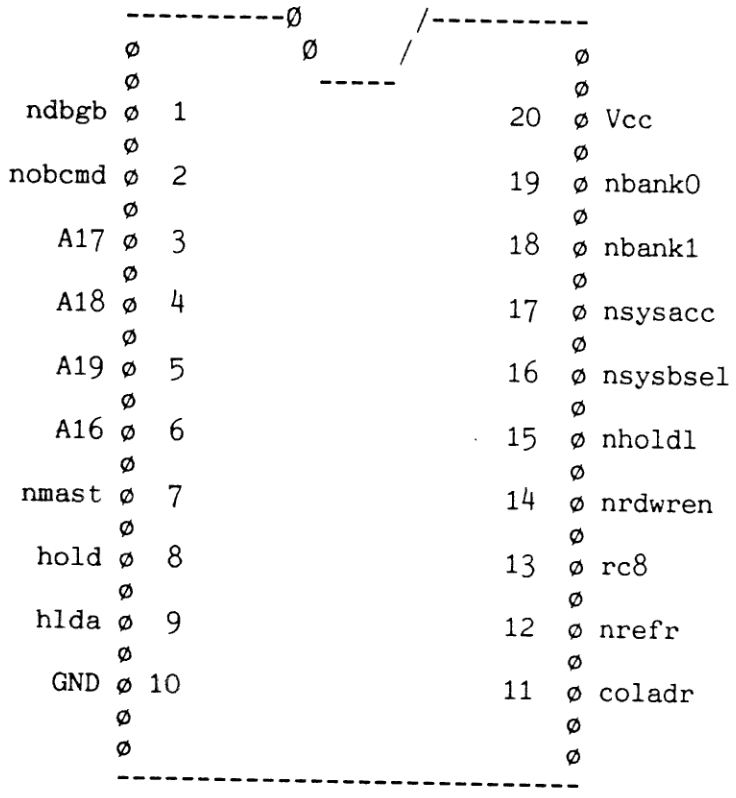
Reduced Equations:

```
enable nbank0 = (1);

enable nbank1 = (1);

enable nsysacc = (1);

enable nsysbsel = (1);

enable nrefr = (!nmast);

enable nrdwren = (1);

enable nholdl = (1);

enable rc8 = (1);

nbank0 = !(!A19 & !nobcmd # !nholdl & !nobcmd);

nbank1 = !(!A17 & A19 & nholdl & !nobcmd
         # !A18 & A19 & nholdl & !nobcmd);


nsysacc = !(!A16 & A17 & A18 & A19 & nholdl & !nobcmd
          # A16 & A17 & A18 & A19 & ndbgb & nholdl & !nobcmd);


nsysbsel = !(A16 & A17 & A18 & A19 & ndbgb & nholdl & !nobcmd);

rc8 = !(!A17 & !A18 # !A17 & coladr # !A18 & !coladr);

nholdl = !(hlda & hold # hold & !nholdl);

nrefr = !(!A17 & !nobcmd # !A18 & !nobcmd # !A19 & !nobcmd);

nrdwren = !(A17 & A18 & A19 & !nmast);
```

ABEL(tm) Version 2.02a - Document Generator 05-May-87 01:38 PM
LAN451 Memory selector, 29. JAN. 1987,
Jens K. Andreassen, Regnecentralen A/S , Ballerup
Chip diagram for Module PAT117TX

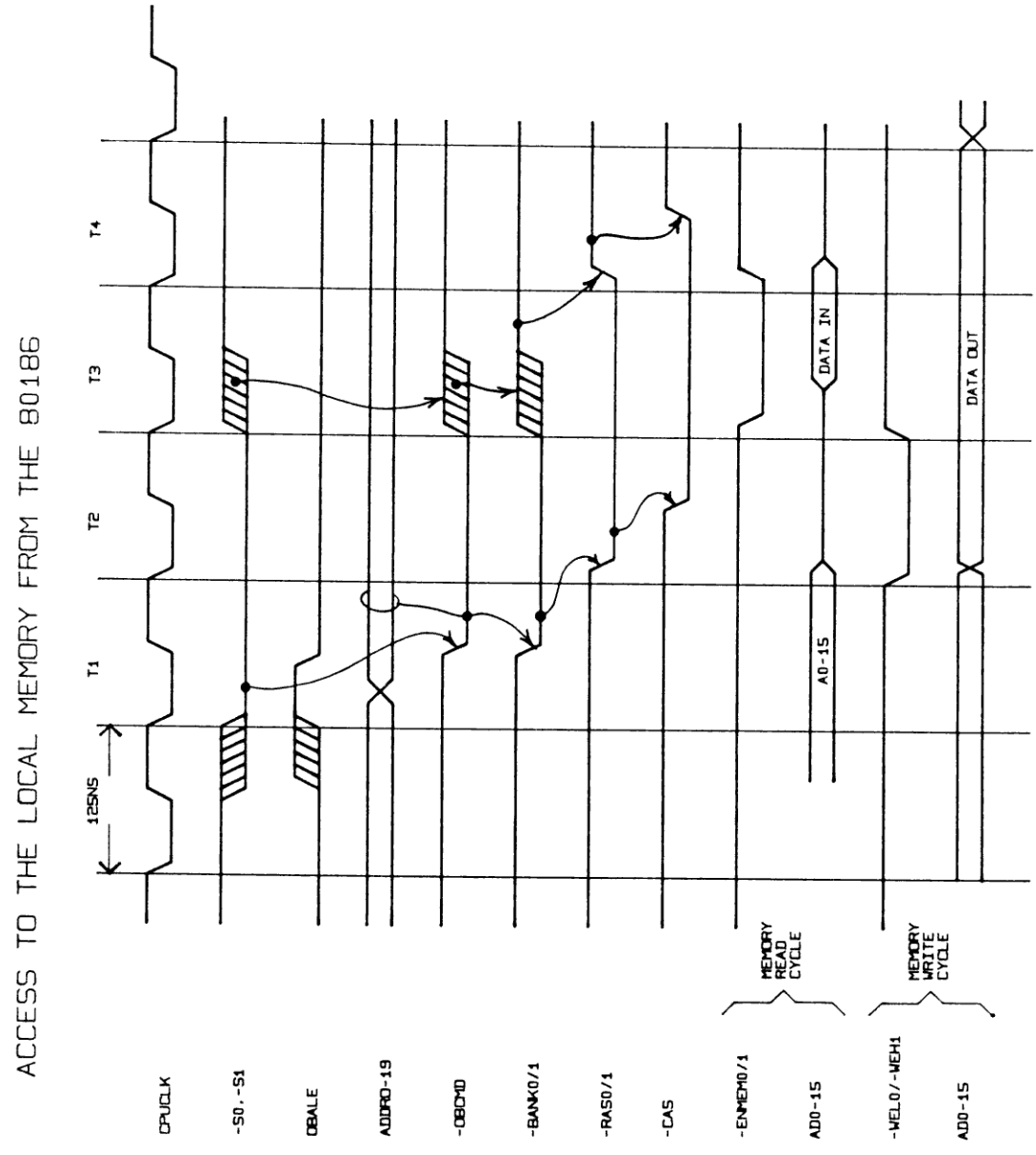
Device PAT117

P16L8



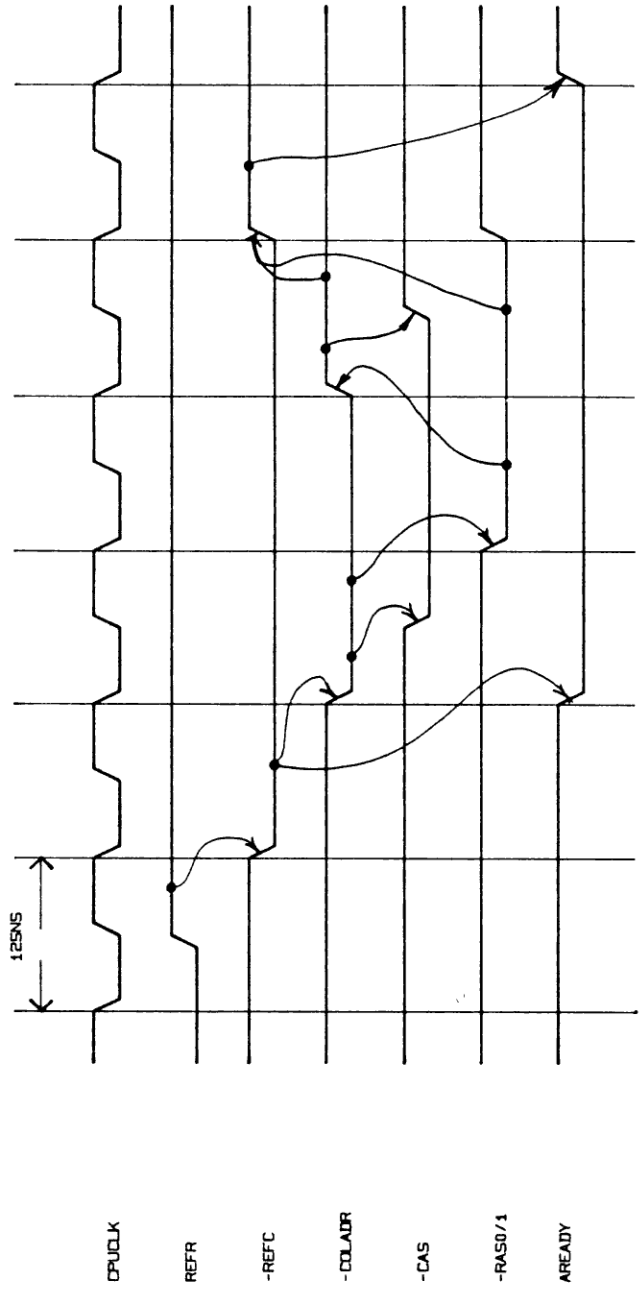
end of module PAT117TX

4.5 Timing diagrams

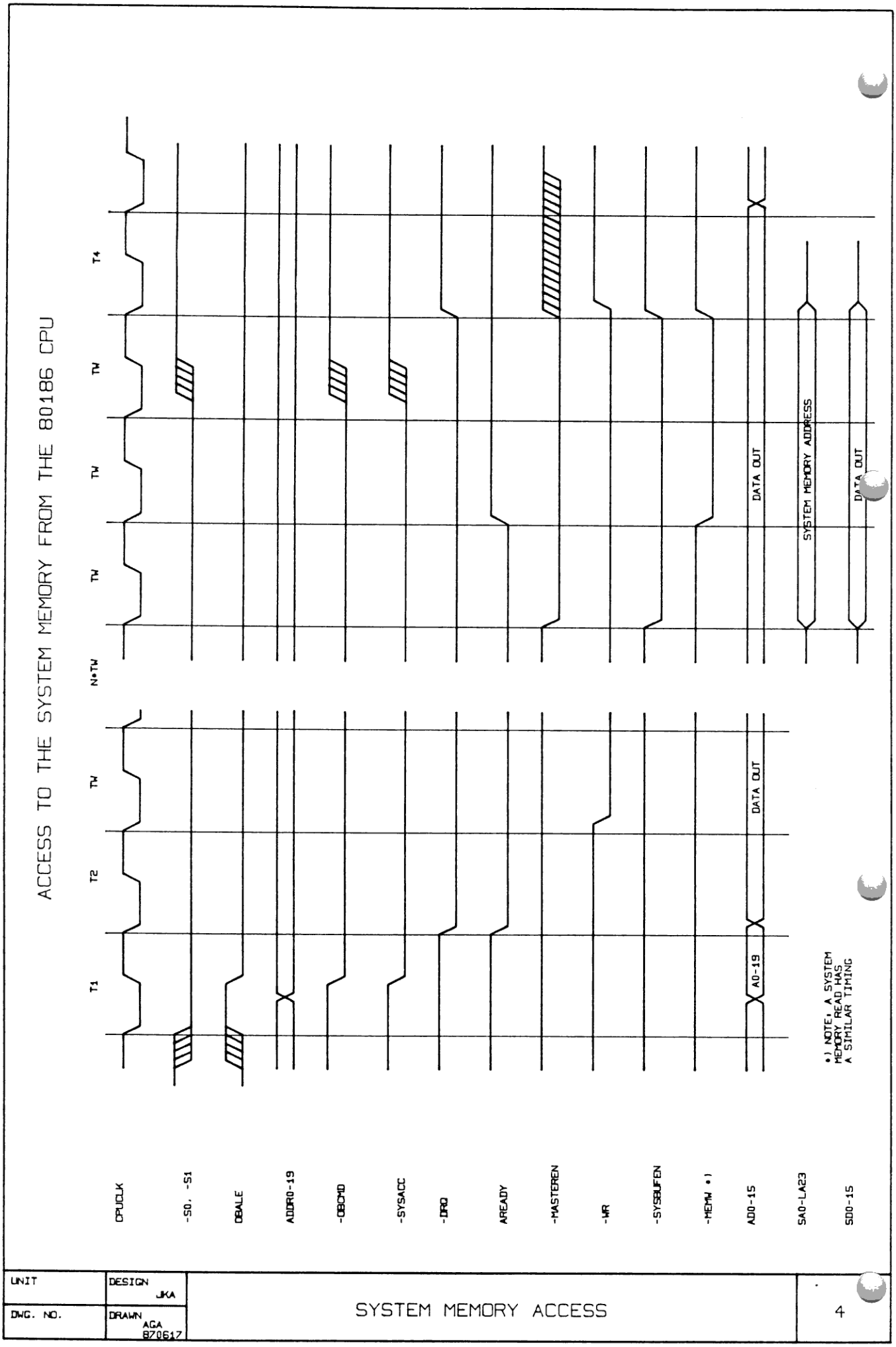


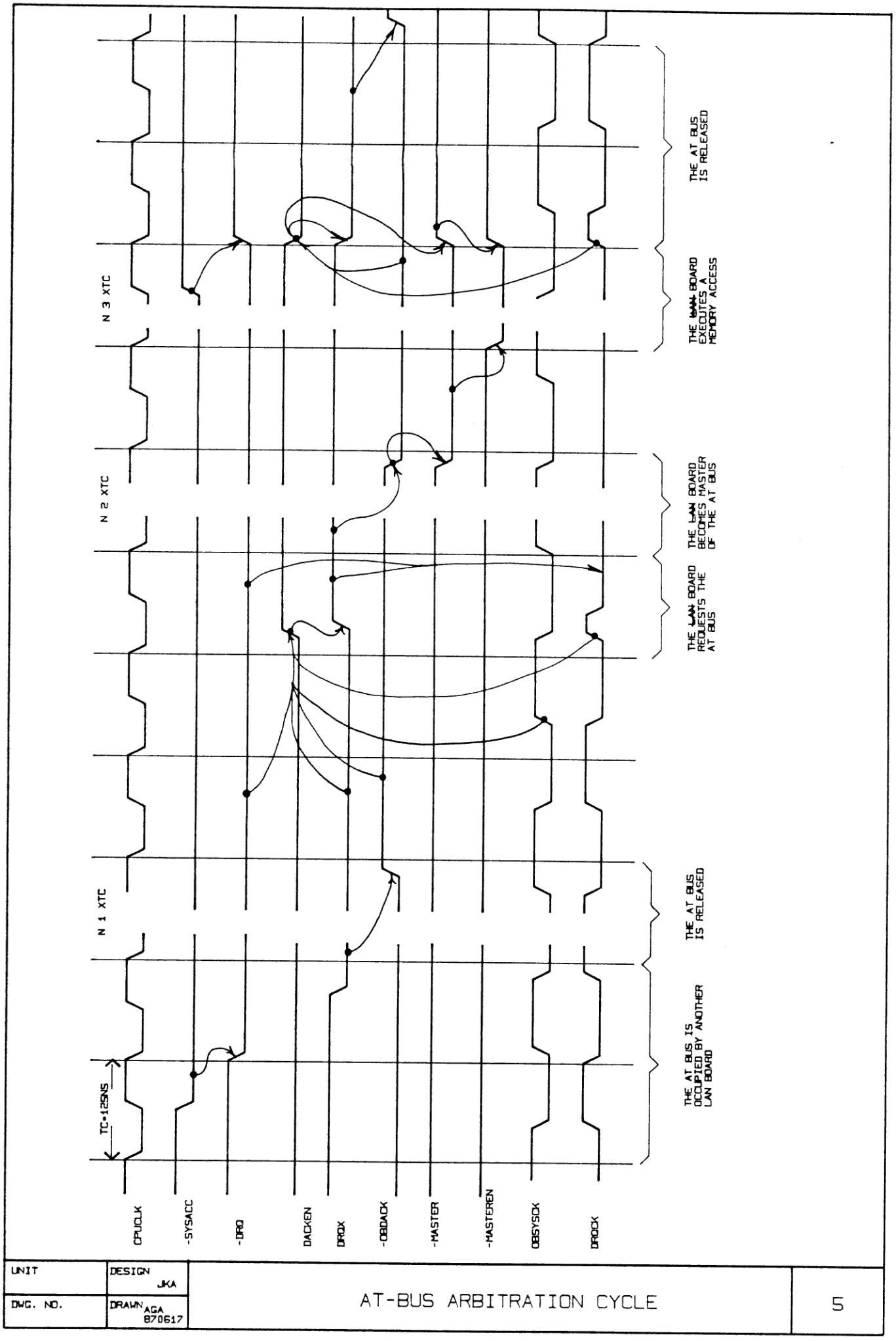
UNIT	DESIGN JKA	ON BOARD MEMORY ACCESS	6
DWG. NO.	DRAWN AGA 870617		

CAS BEFORE RAS MEMORY REFRESH



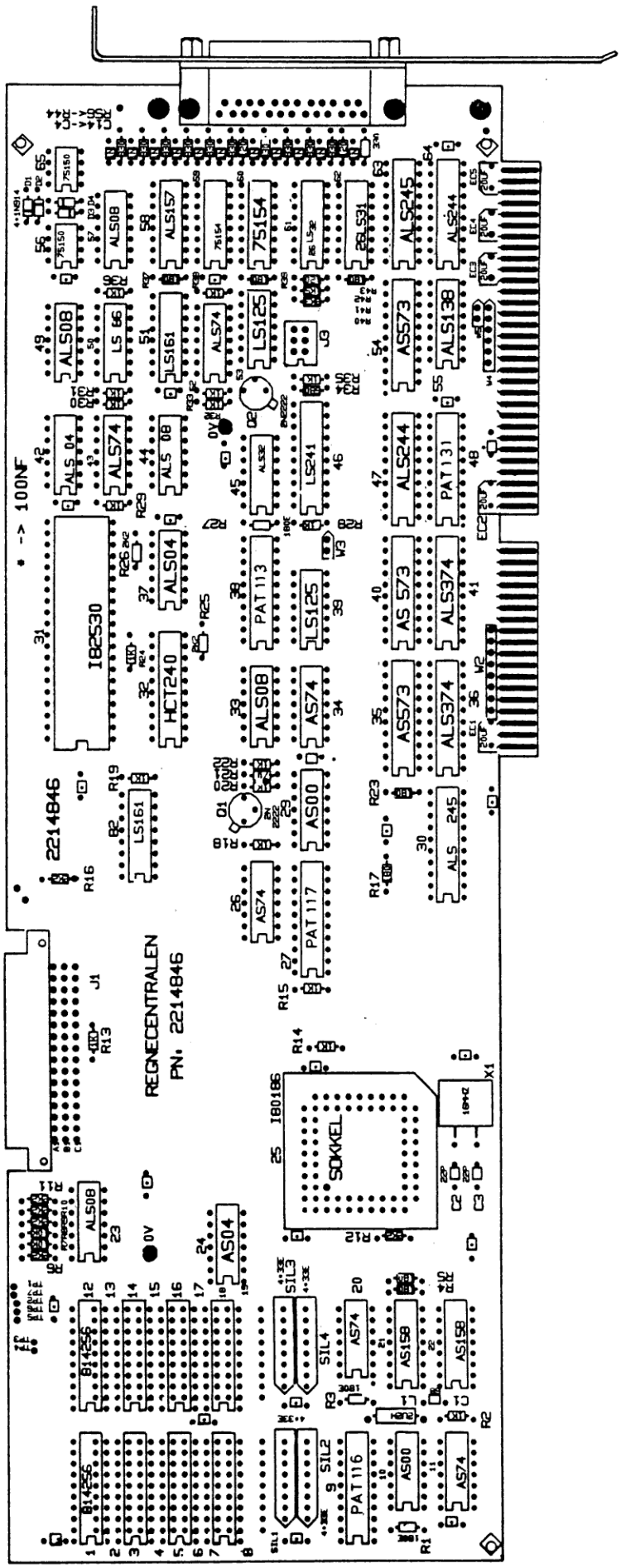
UNIT	DESIGN JKA	ON BOARD MEMORY REFRESH	7
DWG. NO.	DRAWN AGA 870617		


ACCESS TO THE SYSTEM MEMORY FROM THE 80186 CPU
T1
T2
TW
N•TW
TW
TW
T4
CPUCLK
-S0, -S1
DBALE
ADDR0-19
-DBDMD
-SYSACC
-DRQ
AREADY
-MASTEREN
-MR
-SYSBUFEN
-MEMW •)
AD0-15
SA0-LA23
SD0-15
A0-19
DATA OUT
DATA OUT
SYSTEM MEMORY ADDRESS
DATA OUT
•) NOTE: A SYSTEM MEMORY READ HAS A SIMILAR TIMING
UNIT
DESIGN JKA
DWG. NO.
DRAWN AGA 870617
SYSTEM MEMORY ACCESS
4



UNIT	DESIGN JKA	AT-BUS ARBITRATION CYCLE	5
DWG. NO.	DRAWN AGA 870617		

4.6 Assembly drawing



ENHED / BETEGNELSE						
COM 451						6
MONT. TEGN						5
						4
						3
						2
						1
Regnecentralen a·s			DATO / SIGN 870728HC	TEGN NR 762081/0		0

4.7 Plugs

4.7.1 AT bus connector

A side (component side)

I/O Pin	Signal Name
A1	-I/O CH CK (not connected to COM451
A2	SD7
A3	SD6
A4	SD5
A5	AD4
A6	SD3
A7	SD2
A8	SD1
A9	SD0
A10	-I/O CH RDY
A11	AEN
A12	SA19
A13	SA18
A14	SA17
A15	SA16
A16	SA15
A17	SA14
A18	SA13
A19	SA12
A20	SA11
A21	SA10
A22	SA9
A23	SA8
A24	SA7
A25	SA6
A26	SA5
A27	SA4
A28	SA3
A29	SA2
A30	SA1
A31	SA0

B side (solder side):

I/O Pin	Signal Name	
B1	GND	
B2	RESET DRV	
B3	+5V	
B4	IRQ9	
B5	-5V	
B6	DRQ2	
B7	-12V	
B8	OWS	(not used)
B9	+12V	
B10	GND	
B11	-SMEMW	(not used)
B12	-SMEMR	(not used)
B13	-IOW	
B14	-IOR	(not used)
B15	-DACK3	(not used)
B16	DRQ3	(not used)
B17	-DACK1	(not used)
B18	DRQ1	(not used)
B19	-REFRESH	
B20	SYSCLK	
B21	IRQ7	(not used)
B22	IRQ6	(not used)
B23	IRQ5	(not used)
B24	IRQ4	(not used)
B25	IRQ3	(not used)
B26	-DACK2	(not used)
B27	T/C	(not used)
B28	BALE	(not used)
B29	+5V	
B30	OSC	(not used)
B31	GND	

C side (component side):

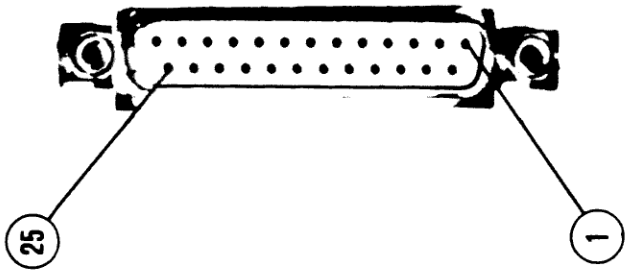
I/O Pin	Signal Name
C1	SBHE
C2	LA23
C3	LA22
C4	LA21
C5	LA20
C6	LA19
C7	LA18
C8	LA17
C9	-MEMR
C10	-MEMW
C11	SD8
C12	SD9
C13	SD10
C14	SD11
C15	SD12
C16	SD13
C17	SD14
C18	SD15

D side (solder side):

I/O Pin	Signal Name	
D1	-MEMCS16	(not used)
D2	-I/O CS16	(not used)
D3	IRQ10	
D4	IRQ11	(not used)
D5	IRQ12	(not used)
D6	IRQ15	(not used)
D7	IRQ14	(not used)
D8	-DACK0	
D9	DRQ0	
D10	-DACK5	(not used)
D11	DRQ5	(not used)
D12	-DACK6	(not used)
D13	DRQ6	(not used)
D14	-DACK7	(not used)
D15	DRQ7	(not used)
D16	+5V	
D17	-MASTER	
D18	GND	

4.7.2 The 25 pol D-connector

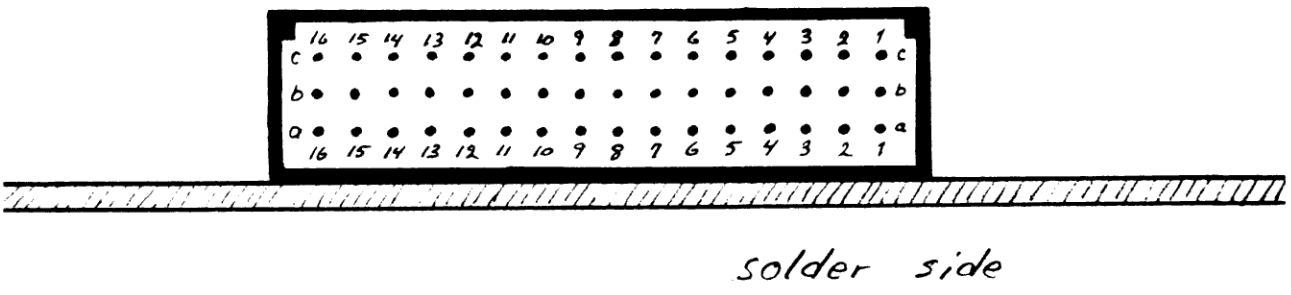
The D-connector seen from the rear:



Pin	Signal Name	Pin	Signal Name
1	Shield	14	C(B)
2	TRANSMIT DATA	15	TRANSM CLOCK
3	REC DATA	16	S(B)
4	REQ TO SEND	17	REC CLOCK
5	CLEAR TO SEND	18	S(A)
6	DATA SET READY	19	R(B)
7	GND	20	DATA TERM READY
8	DATA CARRIER DET	21	R(A)
9	T(A)	22	CALLING INDICATOR
10	I(A)	23	TEST INDICATOR
11	-SELX21	24	I(B)
12	T(B)	25	C(A)
13	N.C.		

4.7.3 Debug Board Connector

The Debug board Connector seen from the top.



Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	AD0	B1	+5V	C1	-DEBUG BOARD
A2	AD1	B2	0V	C2	-DEBUG RESET
A3	AD2	B3	+12V	C3	-PROMSEL
A4	AD3	B4	-12V	C4	-PCS1
A5	AD4	B5	CPURESET	C5	-DBINT
A6	AD5	B6	0V	C6	DBAREADY
A7	AD6	B7	A16	C7	-RXINT
A8	AD7	B8	A17	C8	IDENT1
A9	AD8	B9	A18	C9	IDENT2
A10	AD9	B10	A19	C10	IDENT3
A11	AD10	B11	0V	C11	-BHEN
A12	AD11	B12	OBALE	C12	0V
A13	AD12	B13	-WR	C13	-S0
A14	AD13	B14	-RD	C14	-S1
A15	AD14	B15	0V	C15	-S2
A16	AD15	B16	+5V	C16	-CPUCLK

5. REFERENCES

(1) Microsystem Components Handbook,
Vol I+II, INTEL, 1986.

(2) Microcommunications Handbook,
INTEL 1986.

(3) Technical Reference, Personal Computer AT
IBM 1984.

(4) Specifikation af Debug-kort,
Okt. 86,
Willian S. Jacobsen.