
RC900

CPU452 System Board

Hardware reference manual

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CPU452 System Board

Keywords:

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Abstract:

This paper contains a hardware description of the CPU452 system board. The CPU452 provides 80386 CPU, memory control, AT bus, keyboardcontrol, BIOS ROMS, EGA, Printer, Serial IO and Floppy control.

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CPU452 System Board

1. GENERAL INFORMATION

1.1 Introduction

The CPU452 is a 20MHz intel 80386 based PC/AT compatible processorboard.

The board provides:

- * A socket for insertion of CAM451 that contains a 20MHz i80386 CPU and 32Kbytes of cache memory.
- * Slots for up to 16Mbytes of memory
- * Onboard Enhanced Graphics Adaptor with 256 Kbytes of pixelmemory
- * Floppydisc controller
- * 2 serial ports
- * Parallel printer port
- * A socket for the i80387 option.

This manual describes the CPU452 board in three major sections. The first section gives a short description and specification of the board. The second section contains a functional description. The third section is devoted to the detailed hardware description with circuit- logic- and timing-diagrams. Figure 1 below contains a block diagram of the CPU452 combined with the CAM451 cache memory.

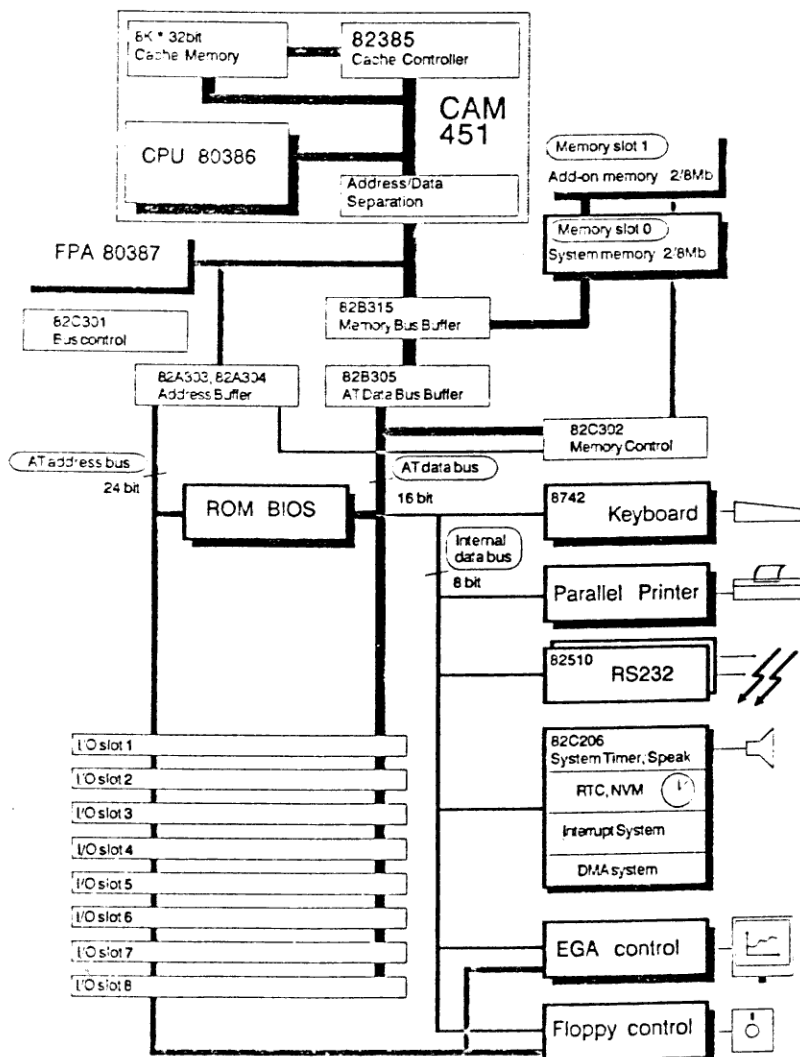


Fig.1 CPU452 Block diagram.

1.2 Short description

The CPU452 basically contains 4 different busses connecting the various elements.

- * A 32 bit Local bus that interconnects the CAM451, the 80387, the memory controller and the busbuffers.
- * A 32 bit Memory bus that connects the memory to the busbuffers.
- * A 16 bit System bus that connects all I/O including the PC/AT-slots and the X bus to the busbuffers.
- * A 8 bit X bus that connects the systemboard controllers to the Systemboard.

The bussystem is controlled by a so called *Chipset* being a five chip gatearray system including memory controller, bus controller and bus buffers/latches.

The board provides a broad spectrum of clock frequencies for driving as well the CPU as the Systembus at different speeds, as might be required in different compatible applications.

The memory system is a banked dynamic memory with access times of 100 or 120 nanoseconds and provides 1 waitstate (20MHz) when hits to interleaved pages are obtained.

Three BIOS PROM's are provided. Two contains the CPU-initialization, the PowerOnSystemTest (POST) and the compatible standard Basic I/O System. One contains BIOS for the EGA.

One LSI-chip C&T 82C206 integrates the compatible system controllers:

- two 8259 interrupt ctr's,
- two 8237 DMA ctr's with the 74LS612 addressmapper,
- 8254 timer/counter,
- 146818 Real Time Clock and
- (extended) CMOS RAM

A compatibel Keyboard controller utilizing an 8742 is, provided. The keyboard interface is connected to both a seperate connector and to some pins in the CRT connector for attachment of the keyboard to the monitor (simplifying cabling).

Eight completely compatible PC/AT I/O slots are provided.

An Enhanced Graphics Adapter is integrated on two LSI gatearrays C&T 82C435 and 82A436. The EGA is expanded with clock frequencies for driving the 73 Hz RC940. These frequencies are automatically selected, when an RC940 cable is inserted in the monitor connector. In that case a special version of the EGA-BIOS residing in the second half of the EGA-BIOS-ROM is also selected, ensuring an initialization of the EGA corresponding to the RC940. The monitor connector also contains connection for the keyboard and a mouse. A strapping option disables the EGA.

Two compatible Seriel ports are implemented in two i82510's. Each of these are strap configurable as not included, first- and second- seriel ports. One is connected via a special "polarity-correcting" circuit to the monitor connector for the connection of several types of mice to the monitor.

A parallel printer port is provided. The port is AT- and (at plug level) Partner-compatible. A strapping option excludes the port or configures it as first- or second-printer port.

A compatible Floppy disc controller is based on Western Digital's WD37C65. The controller may be strapped as first or second or not included.

A battery is mounted on the the board for maintaining power for the RealTimeClock and the Non Volatile CMOS Memory.

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1.3 Specifications

1.3.1 Performance specifications

80386 CPU clock	20 MHz
80387 NPX clock	20 MHz
Local bus size	32 bits

Memory:

capacity	2 slots for insertion of any combination of 2 or 8 Megabytes memory boards.
organization	2 banks in each slot divided in pages of 2 or 8 Kbytes depending on the installed memory module.
word length	32 bits.
operation	Page interleaving.
access time	Page hit : 1 wait states. Page miss: 5 wait states. The installed cache CAM451 however reduces wait states as seen by the 80386 CPU to approximately zero. CAM451 contains 32Kb 35nS cache memory.

ROM BIOS:

capacity	32 Kbytes.
wordlength	16 bits.
access time	Depends on the programmed System bus speed. During POST the BIOS is transferred to the overlaying memory (RAM) and is then accessible with the performance described for memory.

PC/AT bus:

slots	8.
bus width	8/16 bit.
addressing range	16 Mega bytes
transfer speed	programmable from 0.3 Mbytes/second to 10 Mbytes/second.

EGA:

compatibility	CGA and EGA compatible.
RC940 support	65 Hz CGA and 73 Hz EGA.
memory size	256 Kilo bytes.
BIOS size	64 Kilo bytes (32Kbytes selected by the monitor cable).
bus size	8 bit. During POST the EGA BIOS is transferred to the overlaying memory (RAM) and is then accessible with the performance described for memory.

1.3.2 Environmental Specifications

Operating temperature : 0 to 40 degrees C.
Relative Humidity : 20% to 80% (non condensing).
Altitude : 0 to 6,000 feet.

1.3.3 Physical Specification

Width : 330 mm
Length : 440 mm
Height : 34 mm
Weight : 1300 gram

1.3.4 Power Specification

Power consumption (CPU452 only)

Dissipation : 15 W max.
Vcc : +5V +/- 5% (2.5A max.)
+12V : +12V +/- 10% (200mA max.)
-12V : -12V +/- 10% (50mA max.)

To this should be added the consumption of installed memory- and I/O- boards.
Total power outlet to expansion slots:

Vcc : 10 A max
+12V : 1.0 A max
-12V : 300mA max
-5V : 100mA max

2 FUNCTIONAL DESCRIPTION

In this section, the function of all parts of the CPU452 board is described. The description comprises the following functional entities:

1. 80386 Socket for connection to CAM451
2. 80387 NPX
3. Bussystem
4. Memory control
5. BIOS ROMs
6. Integrated Peripherals Controller
 - 6.1 Interrupt controller
 - 6.2 Direct Memory Access controller
 - 6.3 Non Volatile Memory
 - 6.4 Real Time Clock
 - 6.5 Timer/counter
7. Keyboard controller
8. Enhanced Graphics Adapter
9. Serial In/Out
10. Parallel Printer Port
11. Floppy controller

2.1 i80386 Socket for connection to CAM451

CPU452 uses a 20MHz version of the Intel 80386 CPU. The 80386 CPU is an advanced, high performance microprocessor with a non multiplexed 32 bit data and addressbus, integrated memory management, memory protection, an extensive instruction set and two modes of operation:

Real address mode,
Protected mode.

The real address mode is entered after power up. The memory addresses are physical addresses in a contiguous array of one megabytes generated on the address lines BE0 to BE3 and A2 to A19. The addressing mechanism, interrupt handling, are all identical to the Real Address Mode of the 80286. In this mode the processor is setup for Protected mode operation. Protected mode provides access to the entire installed memory, memory management, paging and privilege capabilities of the processor.

In protected mode, software can perform a task switch to enter into tasks designated as Virtual 8086 Mode tasks. Each such task behaves with 8086 semantics, thus allowing 8086 software (an application program or an entire operating system) to execute. The Virtual 8086 tasks can be isolated and protected from one another and the host 80386 operating system, by the use of paging, and the I/O permission bitmap.

For detailed information on the 80386 please refer to reference A.

The 80386 socket however is not occupied by the 80386 as on CPU451. Instead this socket is occupied by the cache memory board CAM451, which also contains the 80386 itself.

The CAM451 is via the local bus (D0 to D31, BE0 to BE3 and A2 to A31) connected to the 80387 NPU, the 80A305 data buffers, the 80A303 and 80A304 addressbuffers and the 80C301 buscontroller.

The CPU clock (CLK2) is generated by the 80C301 buscontroller from the 40MHz CLK2in clock.

The RESET signal is generated by the 80C301 buscontroller on basis of powerreset and "SRC" from the keyboard controller. After reset, the keyboard controller pulls BUSY putting the 80386 into a selftest cycle.

The busstatus signals W/SR, D/SC, M/SIO, SADS and HLDA are monitored by the 80C301 buscontroller, wick on basis of these and the decoded addresses directs the various buffers.

The "NextAddress" input is strapped active, forcing the CAM451 into pipelining mode when ever possible.

The "BusSize16" input is strapped inactive, ensuring that datatransfers always occur over the widest possible databus.

The READY signal, which is used to insert the nessecary number of waitstates in a datatransfer, is generated by 80C301 or when the NPU is addressed by PAT330 in position 78.

The HOLD signal is controlled by the 80C301 and used to achieve the bus for DMA cycles other masters or memory refresh cycles.

2.2 i80387 NPX

The socket in position 71 is for the i80387 Numerical Processor Extension option. The 80387 is a high-performance NPX that extends the 80386 architecture with floating point, extended integer and BCD data types.

The NPX provides arithmetic instructions for a variety of numeric datatypes. It also executes numerous built-in transcendental functions (e.g. tangent, sine, cosine and log).

The 80387 works the same whether the 80386 is executing in real-address mode or in protected mode. All memory access is handled by the 80386; the 80387 merely operates on instructions and data passed to it by the 80386. Therefore, the 80387 is not sensitive to the processing mode of the 80386.

The presense of an 80387 is indicated to the 80387 just after reset by holding the **SERROR** input active until the first busaccess. The **SERROR** input is connected to the **NPID** output on the **PAT257** (see the timing diagram in fig.2).

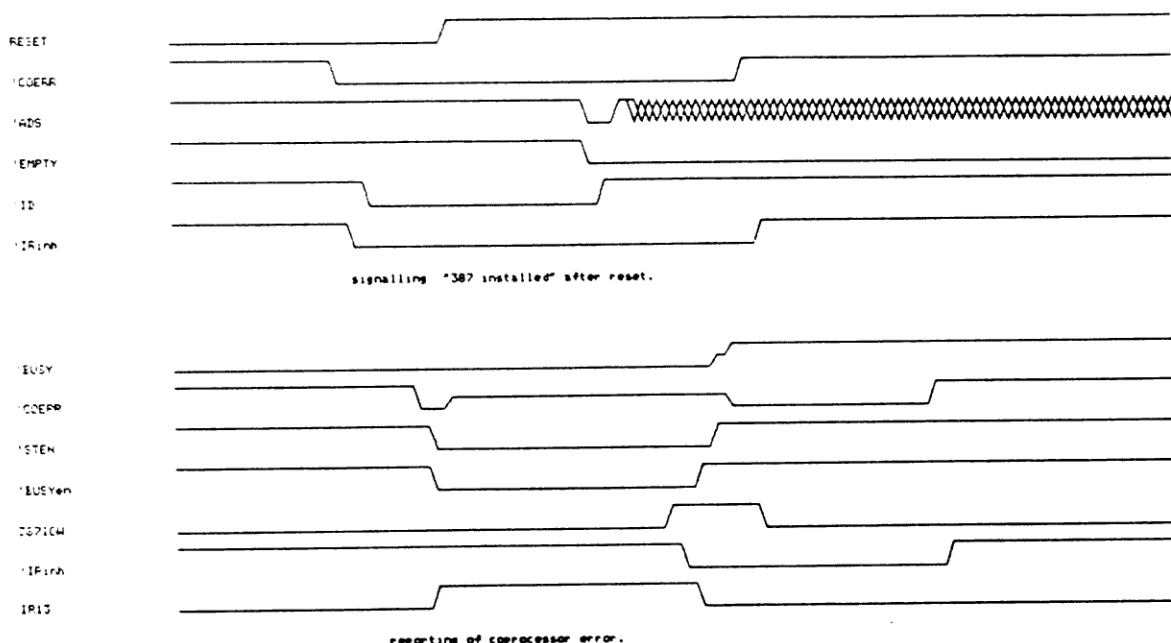


Fig. 2 Compatible NPX interface signalling.

The 80387 is activated by the 80386 via I/O addresses 800000F8h and 800000FCh. As I/O space does not extend beyond 64k, the A31 addressbit together with the M/SIO signal are used to address the 80387. A2 is used to distinguish between opcode- and operand-register. If the NPX has encountered an instruction, which requires parameters or operands, and the NPX is ready for it, it rises the PEREQ signal, which causes the CPU to send or receive data on I/O address 800000FCh. The NPX uses the BUSY signal to indicate to the CPU, that it is not yet ready to take the next instruction. When executing certain "ESC" instructions (80387 instructions), the 80386 waits for BUSY to be set before it proceeds to the next instruction. Most "ESC" instructions and the "WAIT" instruction are not initiated before the 80387 has dropped BUSY.

When the NPX finds an arithmetic error, this is signalled by setting the SERROR output from the NPX. This signal logically anded with the BUSY signal is used by the PAT257 to set the IRQ13 flip flop. At the same time the PAT257 clears STEN causing the NPX to disconnect all transmitters, allowing the PAT257 to prolonge the BUSY signal, inhibiting the CPU from executing another NPX-instruction, until the IRQ13 interrupt is serviced. The IRQ13 is cleared by means of an IO write on address E0h to FFh. For the detailed relative timing of this signalling see fig.2.

For detailed information on the 80387 please refer to reference B.

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2.3 Bussystem

The CPU452 has a number of data- and address- buses on the board. The buses have different widths and functions and are controlled by the 80C301 buscontroller, and are interconnected via various busbuffers and latches.

Data is transferred via five buses:

The Local bus (D0:D31),
the Memory bus (MD0:MD31),
the System bus (SD0:SD15) (the PC/AT bus),
the X bus (XD0:XD7) and
the B bus (BD0:BD7) (used for the onboard devices).

The three first buses are interconnected via the 80B305 bus buffer/latches. These gate data from one bus to one or more other buses, and convert between bus widths.

The 80C301 directs the 80B305 by means of a four bit action code plus five other buscontrol signals. This chip also transforms a 32 bit transfer into several 8 or 16 bit transfers if so required.

The data conversion between the System bus and the Local bus / Memory bus depends on the action code in the following way:

AC3:AC0	From	To
0	D15:D0	SD15:SD0
1	D15:D8	SD15:SD8, SD7:SD0
2	D31:D16	SD15:SD0
3	D31:D24	SD15:SD8, SD7:SD0
4	D31:D0	SD31:SD0 (not used)
5	SD7:SD0	D7:D0
6	SD7:SD0	D15:D8
7	SD7:SD0	D23:D16
8	SD7:SD0	D31:D24
9	SD15:SD0	D15:D0
A	SD15:SD0	D31:D16
B	reserved	
C	SD31:SD0	D31:D0 (not used)
D,E,F	reserved	

The bus connections are controlled in the following way:

Cycle type	HLDA1	\$ATEN	\$MRD	\$DIR	\$LDEN	From bus	To bus
Local write	0	1	1	x	x	D	MD
Local read	0	1	0	x	x	MD	D
AT write	0	0	x	1	x	D	SD
AT read	0	0	x	0	x	SD	D
DMA write	1	1	1	0	x	SD	MD,D
DMA read	1	1	0	1	x	MD	SD

The X bus and the B bus are eight bit subbusses both connected to SD7:SD0 via 74LS245 "bidi"-buffers.

The X bus attaches the eight bit ports in 80C301, 80C302, 80C206, the 8742 Keyboard controller, the memory ID port and the power control ports.

The B bus attaches the on board serial controllers, parallel printer controller and the Floppydisc controller.

The address lines are grouped in three buses:

A2:A31 ; the address part of the Local bus.
SA0:SA23 ; the address part of the System bus.
XA0:XA23 ; the address part of the X bus.

These buses are interconnected via the 82A303 and 82A304 address buffers as a function of the buscontrols in the following way:

Cycle type	HLDA1	SATEN	SREF	SMMASTER	From bus	To bus
Local	0	1	1	1	A	none
CPU-ATbus	0	0	1	1	A	SA,XA
CPU refresh	0	1	0	1	XA	SA
DMA	1	1	1	1	XA	A,SA
Master	1	1	1	0	SA	A,XA
Master ref.	1	1	0	0	counter	SA

During a Master refresh cycle, the low order address bits SA0:SA11 are derived from a refresh counter in 82A304, whereas SA12:SA23 are forced to zero by the 82A303.

During a DMA cycle the address is generated by the 82C206 and driven onto the XA bus by the 82C206 and one of two 74ALS373's in positions 10 and 11 depending on whether an eight- or sixteen-bit DMA channel is active.

During a Master cycle the "AT-master" (the AT-bus attached peripheral having taken the AT-bus (System bus)), is responsible for driving an address onto the SA bus.

The 82C301 activates the different buscycles on basis of CPU status, addresses and the SAF32, SIOCS8, SIOCS16, SMCS8 and SMCS16 signals.

The SAF32 signal is activated either by the 82C302 memory controller or the PAT330. In the first case, the 82C302 must also generate SREADY, when the memory cycle has finished. In the second case a local bus cycle for the 80387 is indicated, and the PAT330 terminates the cycle with SREADY.

2.4 MEMORY CONTROL

The memory is not integrated on CPU452 but must be installed in positions JX and/or JY to allow the CPU to initialize.

The memory boards are organized in two banks for interleaved operation. The memory controller 82C302 supports interleaving in pagemode in two banks. When using 256KByte RAMs as on the MEM451 board, the pages are 512 words of 32 bits each i.e. 2KBytes, whereas the 1MByte RAMs provided with the MEM452 board give 1024 words of 32 bits i.e. 4KBytes per page.

When an access is made to the same page, to which the former access was made, the access is made in pagemode only requiring CAS to be set. This is about twice as fast as a normal access, where RAS is set following by CAS each signal latching a portion of the address.

When an access is to another page than the current, RAS has to be dropped, a delay (the RAS precharge time) must be inserted, before the RAS-CAS sequence can be entered.

A memoryboard inserted in a memorysocket identifies itself by shorting one of the two signals \$2MB or \$8MB to GND, these signals plus two speed indicator signals "20nS" and "40nS" exist in two versions, one per memorysocket. They are pulled up by 10K resistors and fed into a read gate addressed on I/O address 26h. By means of this gate the BIOS may initialize the 82C302 to the actual installed installation. Due to the programmable memory organisation any memory board may be inserted in any memory slot.

The ident signals are grounded on the memoryboards according to the following scheme:

\$2MB	\$8MB	Installed memory
H	H	none
L	H	2MByte
H	L	8MByte
L	L	reserved

20nS	40nS	Memory speed
H	H	120 nSec
L	H	100 nSec
H	L	80 nSec
L	L	60 nSec

The ident signals for slot J17 are indexed with a 0 and those for slot J18 with a 1:

slot J17: \$2MB0, \$8MB0, 20nS0, 40nS0
slot J18: \$2MB1, \$8MB1, 20nS1, 40nS1

Four RAS signals and four CAS signals for the main memory exist on the CPU452. They are distributed to the memory slots in the following way:

Slot	Bank0	Bank1
J17	\$RAS0,\$CAS0	\$RAS1,\$CAS1
J18	\$RAS2,\$CAS2	\$RAS3,\$CAS3

The CAS signals are gated with the four LatchedByteEnable signals SLBE0 to SLBE3 on the memory boards to generate a CAS signal per byte per bank.

The paritybits are generated and checked in the 82B305's and the 82A306. If even parity is detected during a memory read, and parity check is enabled, a NMI is generated.

The 82C302 generates refresh cycles by activating all RAS signals in a staggered fashion to reduce the rate of change in the memory current consumption.

2.5 BIOS ROMS

The BIOS contains bootstrap program, power on system test, initialization and the basic I/O drivers and interrupt handlers.

The BIOS program is developed by PHOENIX TECHNOLOGIES and is located in two 27128 PROMS giving storage to 32KBytes.

The PROMS are situated in positions 19 and 20 with the odd rom module number (ROE019) in pos 19 and the even (ROE018) in pos 20.

The contents are accessed via the 74ALS541 busbuffers in pos. 18 and 19 (see diagram 21) and the Sbus on the addresses E8000 through FFFFF hex, untill the 82C302 is reconfigured to access the main memory on these addresses. This is done by the BIOS when the PROM contents is copied into the same addresses in the main memory obtaining a faster access speed.

Two strapping options (W3 and W4) are located near the PROMs for enabling the possible extension of the PROM capacity:

W3	W4	PROMtype
A	C	27128
B	C	27256
A	D	not used
B	D	27512

2.6 Integrated Peripherals Controller

The 82C206 is a LSI containing the peripherals inherent to an AT architecture:

- 6.1 Interrupt controller
- 6.2 Direct Memory Access controller
- 6.3 Non Volatile Memory
- 6.4 Real Time Clock
- 6.5 Timer/counter

Moreover has the chip various registers for programming DMA speed.
For detailed information on the 82C206 please refer to reference D.

2.6.1 Interrupt controller

Integrated on the chip are the equivalent of two cascaded 8259 interrupt controllers. The output of these is connected to the interrupt input of the 80386 CPU. The 16 inputs are disposed in the following way:

Controller	Channel	Interrupt source
1	IR0	Counter/Timer 0
	IR1	IRQ1 Sbus pin B18
	IR2	Cascade interrupt from controller 2
	IR3	IRQ3 Sbus pin B25, on board SIO
	IR4	IRQ4 Sbus pin B24, on board SIO
	IR5	IRQ5 Sbus pin B23, on board printer
	IR6	IRQ6 Sbus pin B22, on board FD ctr.
	IR7	IRQ7 Sbus pin B21, on board printer
2	IR0	Real time clock
	IR1	IRQ9 Sbus pin B4, on board EGA
	IR2	IRQ10 Sbus pin D3
	IR3	IRQ11 Sbus pin D4
	IR4	IRQ12 Sbus pin D5
	IR5	80387 error
	IR6	IRQ14 Sbus pin D7
	IR7	IRQ15 Sbus pin D6

2.6.2 Direct Memory Access controller

Integrated on the chip are the equivalent of two cascaded 8237A DMA controllers. A DMA request to one of the DMA channels results in a HRQ1 to the 82301 which in turn transforms this into a HOLD request to the 80386. This when releasing the Local bus sets the HLDA signal causing the 82C301 to transmit HLDA1 to the 82C206 which sends DACK on the line corresponding to the requesting line with the highest priority.

If the requested DMA channel is so programmed, and the requesting device wants to gain total control over the bus, this sets the \$MASTER signal causing the DMA controller to treestate its address and control drivers.

Otherwise the DMA controller will generate a memory address, the AEN signal and the read and write signals depending on the programmed direction of transfer. After such transfer the address register and bytecount register are incremented by one each.

The two DMA controllers provide four channels each, one of which is used for cascading controller 2 to controller 1.

When addresses are generated by controller 2, they are shifted one (multiplied by 2) before they are applied to the addressbus, resulting in wordwise addressing of the memory. So the channels on controller 1 are used for byte transfers while the channels on controller 2 are used for 16 bit transfers.

Both controllers may be used by busmasters for arbitration.

Controller	Channel	n	DRQ(n)	\$DACK(n)
DMA1	0	0	D9	D8
	1	1	B18	B17
	2	2	B6	B26
	3	3	B16	B15
DMA2	0		Cascade from DMA1	
	1	5	D11	D10
	2	6	D13	D12
	3	7	D15	D14

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2.6.3 Non Volatile Memory

The CMOS NMV which is standard in an AT is integrated on the 82C206 and addressable as described in the technical information from CHIPS.

2.6.4 Real Time Clock

The Real Time Clock integrated in the 82C206 is compatible with Motorola's 146818.

The 32768 Hz clock for this is generated by a specially low power requiring crystal oscillator implemented with a CMOS 14069 inverter circuit.

The 82C206 is powered from a circuit which switches to battery supply when the voltage on the 5 volt supply gets too low. This is to retain data in the NVM, and maintain real time.

2.6.5 Timer/counter

The Timer/counter integrated in the 82C206 is compatible with the Intel 8254. The timers are used in the AT compatible style:

- timer 0 is connected to IRQ0,
- timer 1 controls memory refresh and
- timer 2 drives the Speaker.

2.7 Keyboard controller

The keyboard is connected to the CPU452 via an 8742 programmable peripheral, programmed to serve the RC930 keyboard (or any PC/AT keyboard if so desired). However neither the plug nor the supply voltage for the keyboard are compatible. The keyboard is powered through a 9 volt regulator, which serves as currentlimitor.

The KBDCLK and KBDDATA signals found on diagram 19 and 36 are used for both transmission of commands to the keyboard and for reception of data from the keyboard. As receivers are used LM339 comparators to obtain a more well defined threshold voltage at app. 2.5 volts allowing for voltage drop in the ground line.

Three outputs from the 8742 not used for keyboard support are assigned to special functions:

The signal "-RC" will when activated cause reset of the CPU452. This is due to the fact, that the 80286 originally found in AT's is unable to enter real adress mode from protected mode in any other way.

The signal "A20GATE" ensures when false, that adresses between 100000H and 1FFFFFFH wrap around to 0H thru FFFFFFFH, which is required for PC-compatibility.

The signal "-CPUTST" pulls BUSY for 80386 after reset, putting the microprocessor into a selftest cycle that completes in 60mS.

2.8 Enhanced Graphics Adapter

The CRT controller incorporated on CPU452 is a "chipset" from Chips & Technology with the IC's 82C435 and 82A436, and detailed information about these are found in reference E. This chipset emulates the standards EGA (Enhanced Graphics Adaptor), the CGA (Colour Graphics Adaptor), the MDA (Monochrome Display Adaptor) and the Hercules.

The CRT controller is drawn on diagrams 30 thru 35, showing the chipset, the CRT refresh memory consisting of eight 64K by 4 DRAMs organised in two banks, bank A on diagram 32 and bank B on 33. Diagram 34 shows the video signal drivers (SN74ALS244 pos 44), the "feature connector" through which both sides of the video signal driver IC as well as the enable signal for this are accessible.

Diagram 34 also shows the Dot frequency selection and the mode selection switches. The signal "N60Hz" is a strap option in the CRT connector (diagram 35) used to select the non AT standard frequency needed for RC940 to produce 75Hz frame frequency.

2.9 Serial In/Out

Diagrams 25 to 29 show the two serial I/O ports implemented on the CPU board using 182510 asynchronous transceivers. The board is prepared for National Semiconductors 16450 as second source for the Intel parts. Dia.25 shows the xtal oscillator used, which should run 18.432MHz when 82510 is installed and 1.8432MHz if the NS16450 is mounted.

Diagram 25 also shows the mouse polarisation circuit, which automatically detects the representation of the mark and space levels of the received data from the mouse connected via the monitor. The circuit operates as follows: The differentiator implemented in 55-A, 56-C, R92 and C46 detects any level shift in the signal "RXMOUSE" generating a trigger pulse to the retriggerable oneshots 52-A and 52-B. If 20 microseconds elapse between levelshifts, oneshot 52-A resets and clocks the current value of "RXMOUSE" into flipflop 54-A. If still no level shifts are detected for 20 more microseconds, the oneshot 52-B runs out too and clocks the latched value into flipflop 54-B. The output of this is considered the polarity of mark and used to modify "RXMOUSE" by means of 55-B.

If no mouse is connected to the monitor, the output of 55-B is high, assuring that serial port A may be used from J4.

The strapfield shown on dia.22 selects one of two possible I/O addresses and interrupt lines for the serial ports. If no straps are inserted in this position, the ports appear as non existent to the system.

2.10 Parallel Printer Port

Diagrams 23 and 24 show the Parallel Printerport. This is identical to the AT implementation except for an extra bit introduced in the control signal register controlling the tristate output of the data register, making it possible to input parallel data from the port. The printer connection J1 is shown on dia.29.

The strapfield shown on diagram 22 selects one of two possible I/O addresses and interrupt lines for the printer port. If no straps are inserted in this position, the port appears as non existent to the system.

2.11 Floppy controller

Diagram 36 shows the floppy controller chip from Western Digital WD37C65 which includes a high resolution digital data separator as well as all logic needed for compatible floppy disc control.

A pal (pat118) is added for address decoding, to gate the "DCHG" (Disc changed) signal to the data bus. The PAL also controls the databuffer (74ALS245 pos.25 shown on diagram 22) between the SD bus and the BD bus.

For detailed information on the WD37C65 please refer to reference F.

The straps W15 and W16 on diagram 36 are used to define the Floppy disc controller as primary or secondary controller or to disable it totally. W17 and W18 are not used.

3. TECHNICAL DESCRIPTION

3.1 Introduction

This section gives the detailed description of the CPU452 circuit board until the chip level. For the technical description of the used chips please refer to the manufacturer manuals in the References.

3.2 Block diagram

Figure 3 and 4 shows a detailed blockdiagram of the CPU452 intended to provide an overview of the board. The blocks correspond to physical and or logical entities and are labeled with numbers referring to the logic diagrams in section 3.3, where the exact electrical connections are drawn. Two or more numbers separated with commas indicates that the block is spread over more diagrams.

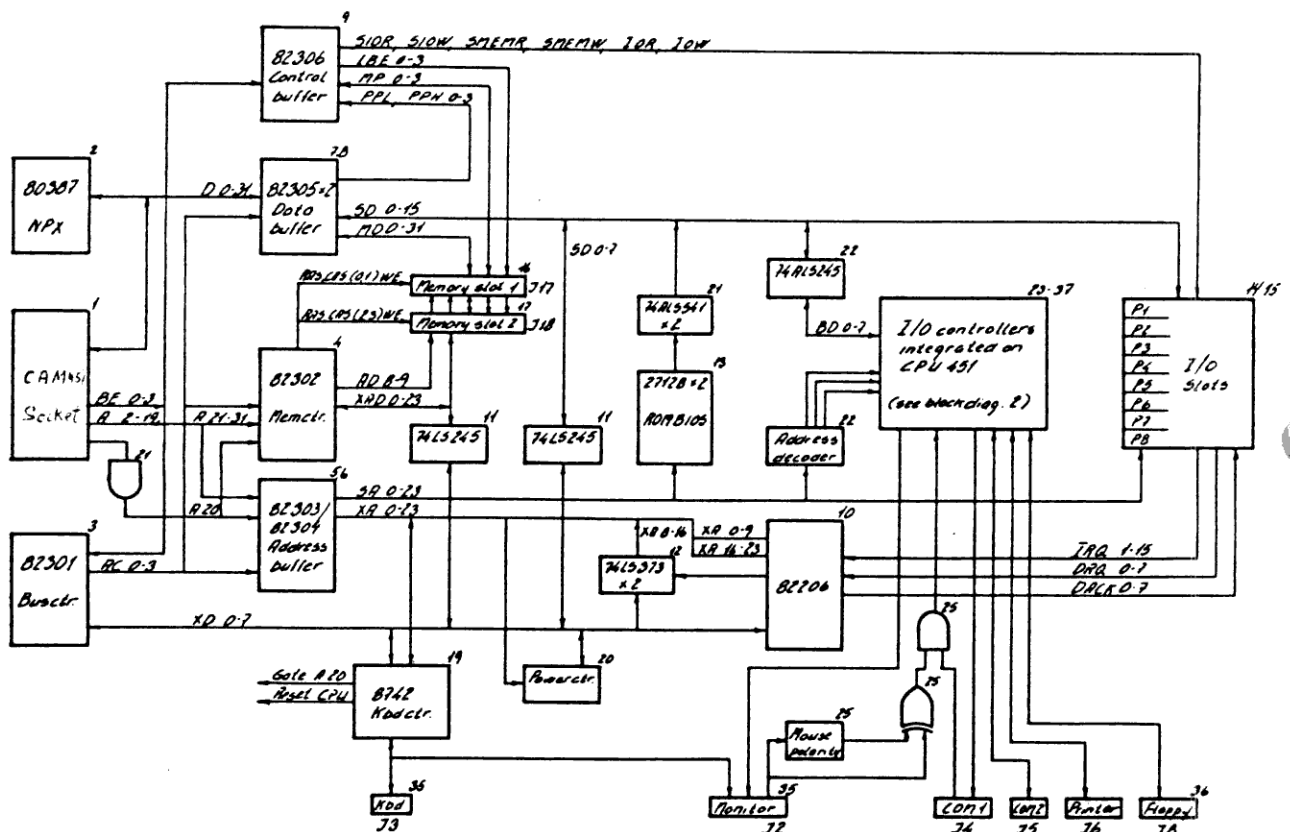


Fig. 3 detailed block diagram.

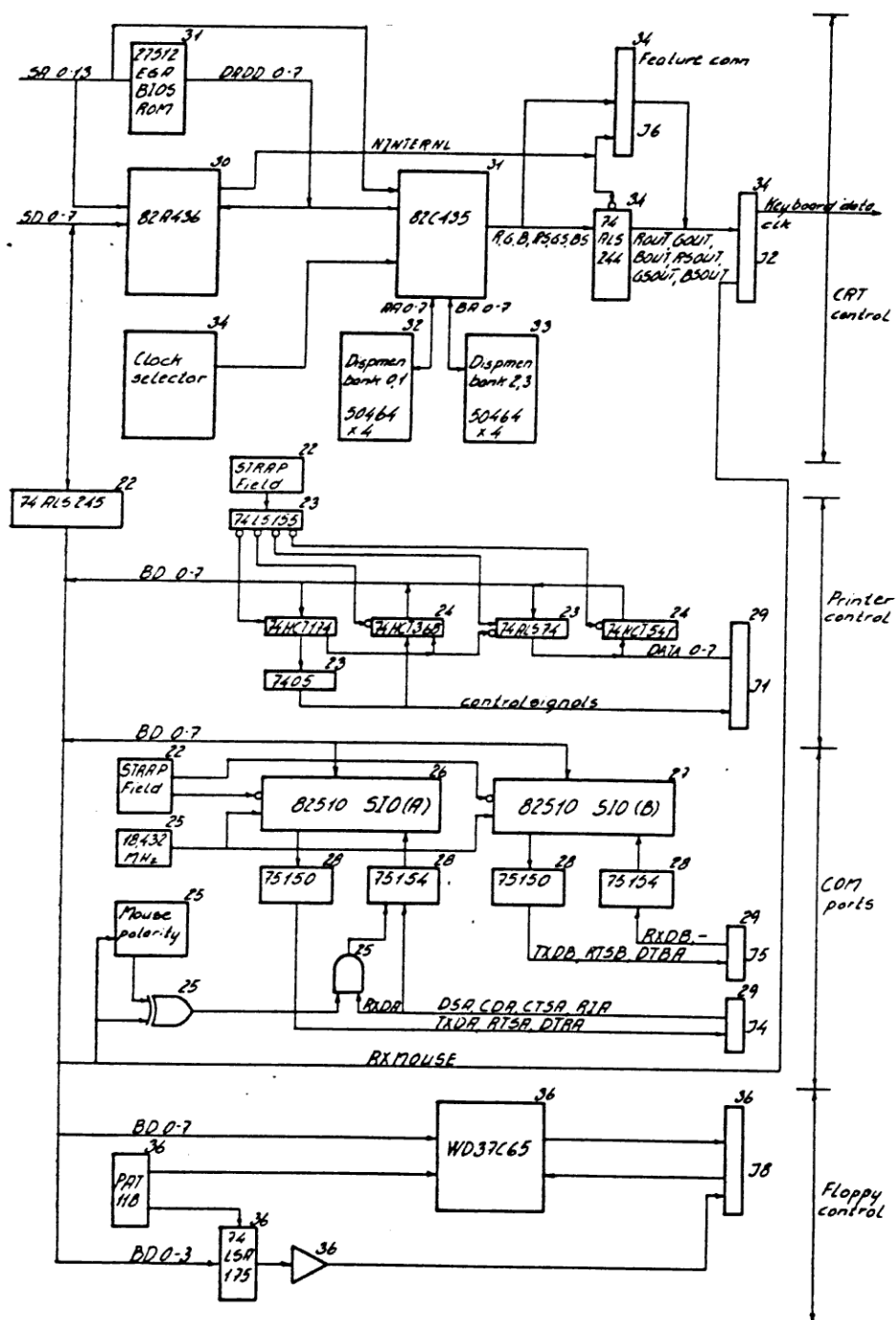


Fig. 4 detailed block diagram for the I/O section.

CPU452 System Board

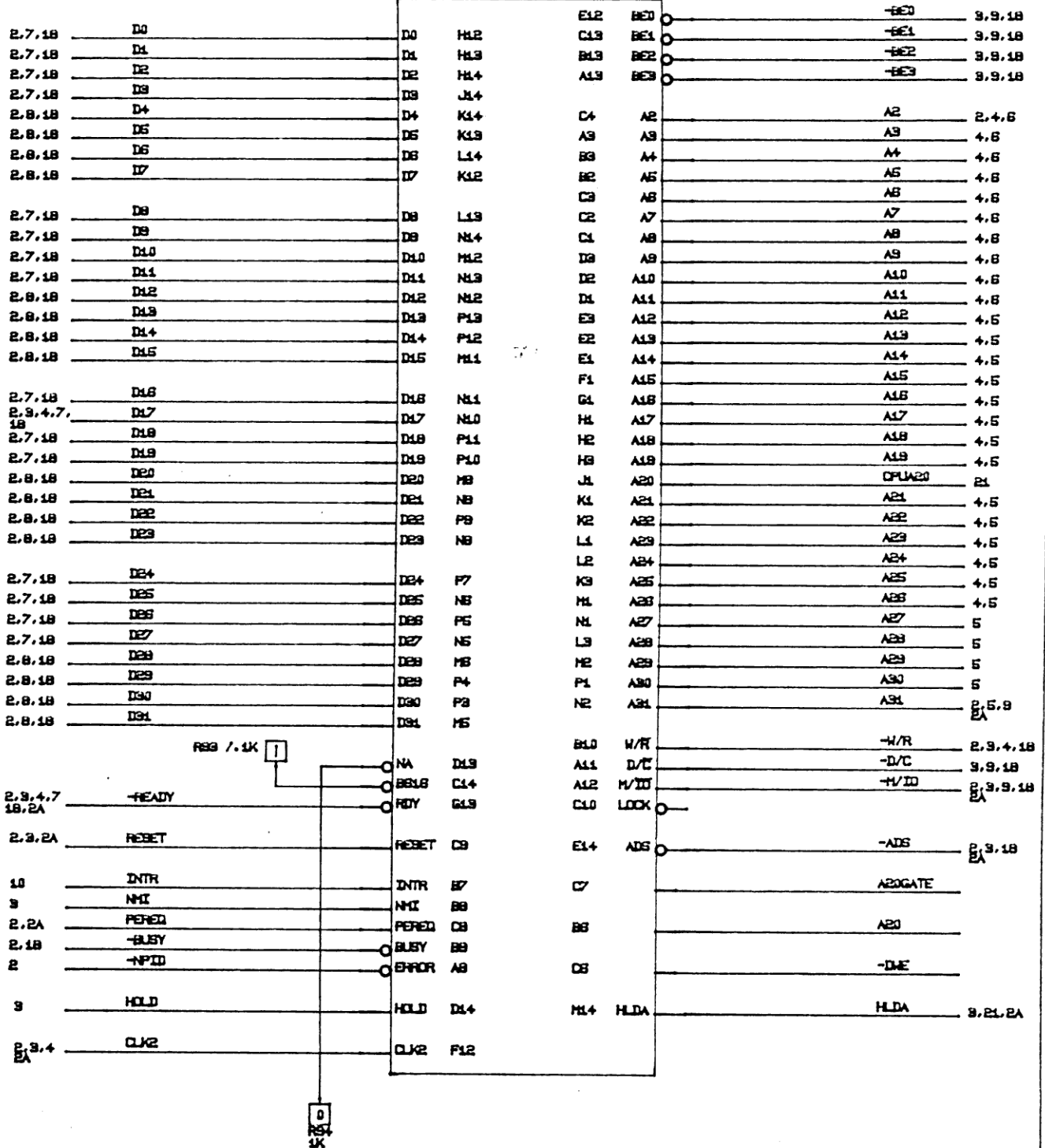
3.3 Logic diagrams

This section contains the logic diagrams of the CPU452.

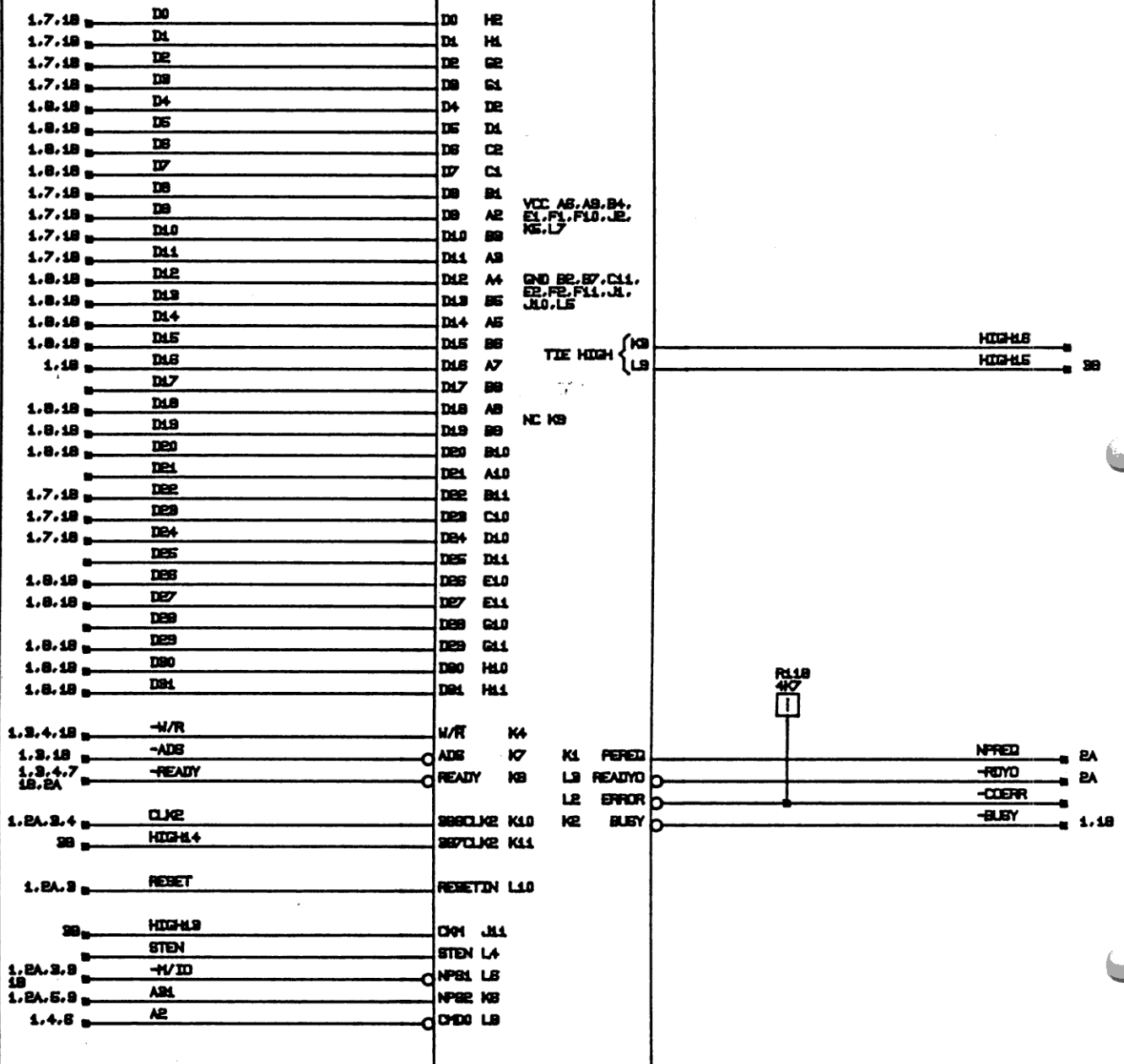
The pages of the diagram are numbered separately from the pagination of the manual. These diagram numbers are used on the diagrams for source and destination references, where signals enter or leave a page.

The position code found above each component on the diagrams corresponds to the position number marked on the printed circuit board.

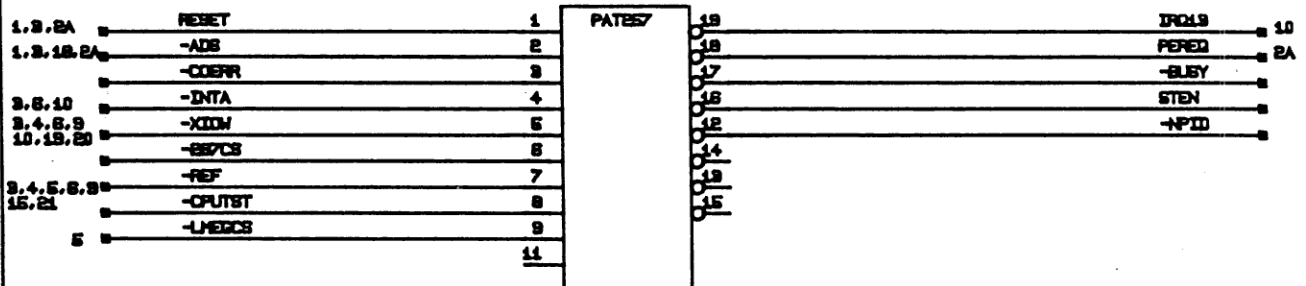
CAM451-SOCKET

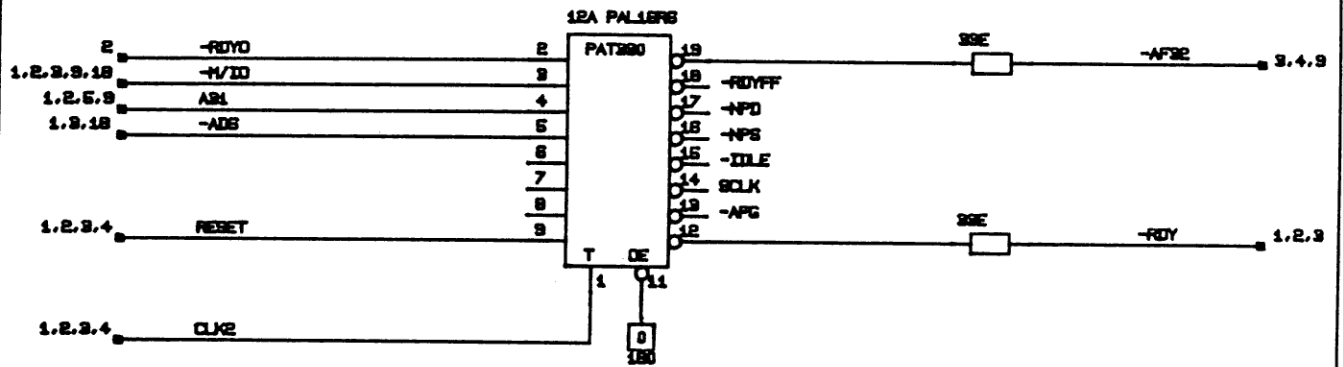


U72/ D8087

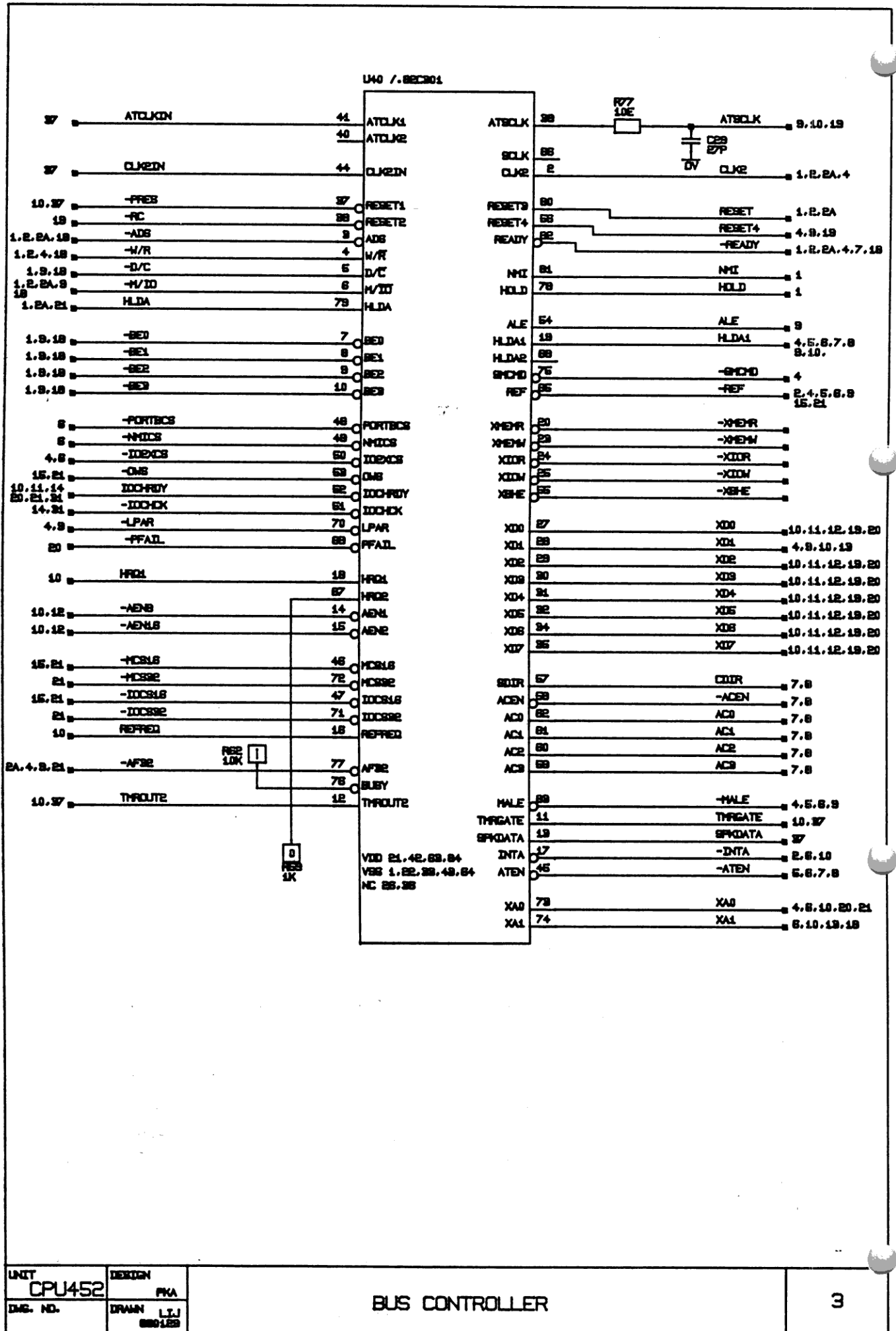


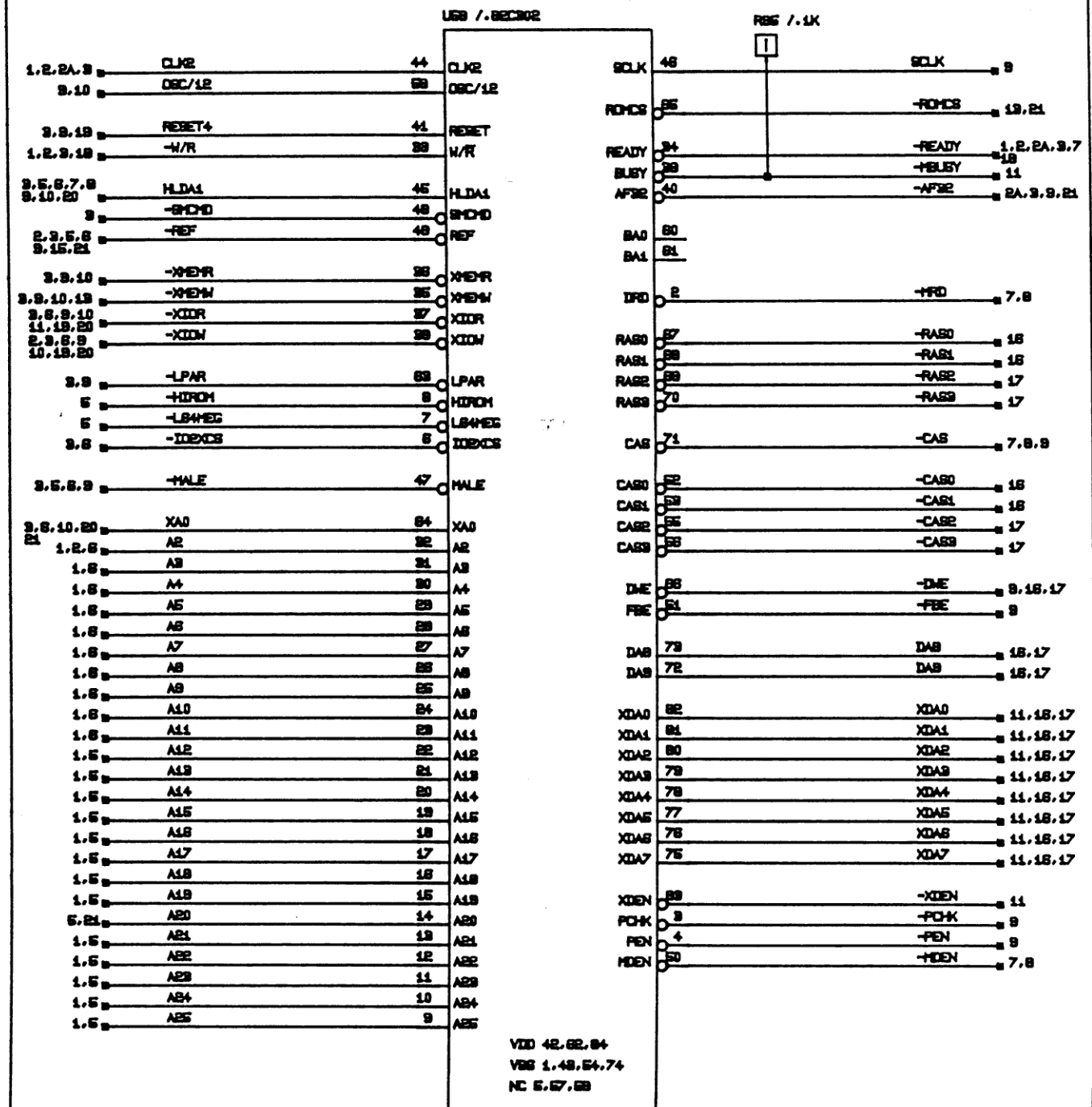
U73/ PAL18L8



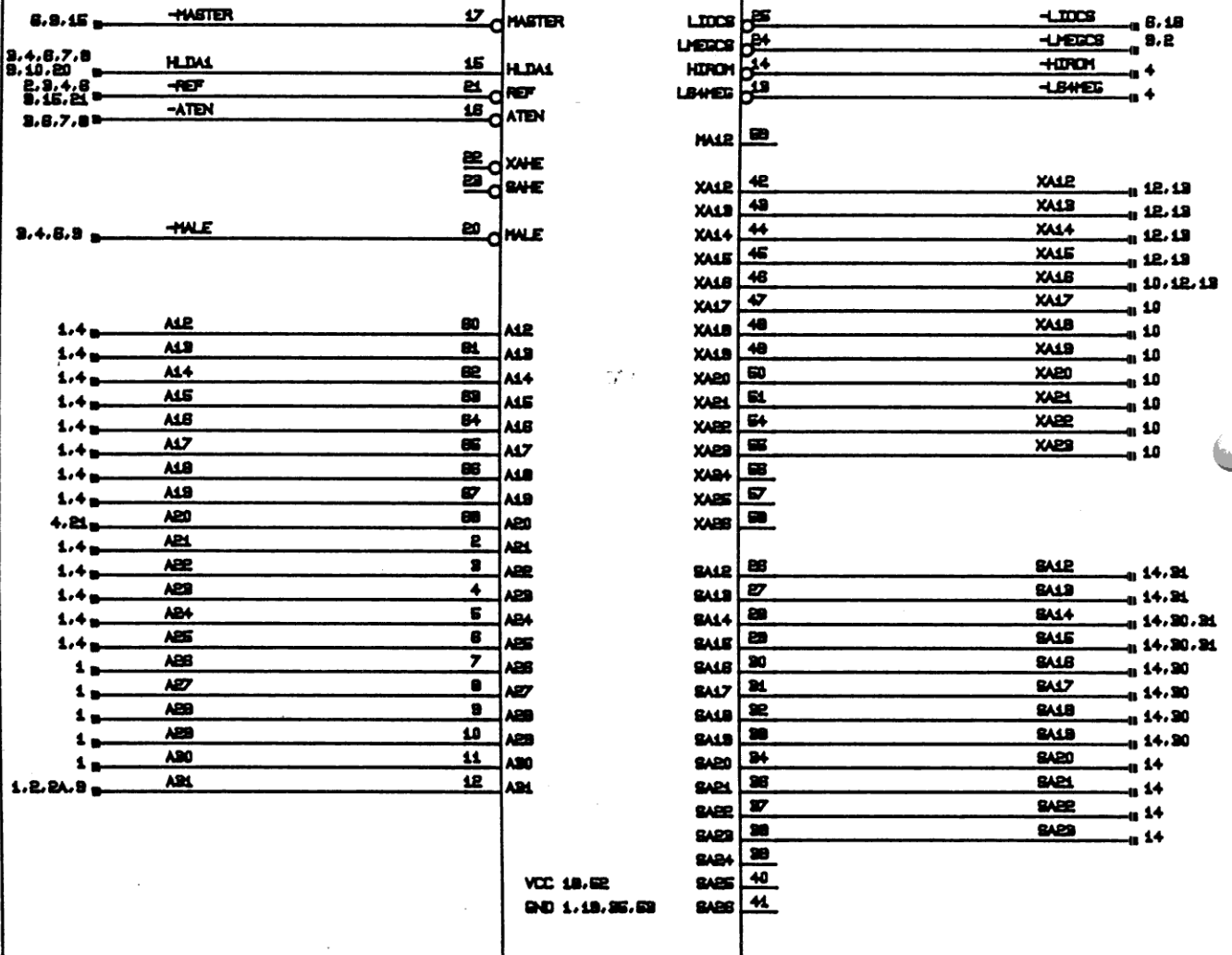


UNIT	DESIGN	NPX GLUE	2A
CPU452	FKA		
ENG. NO.	DRAWN	NPX GLUE	2A
	L.J.J. 080123		

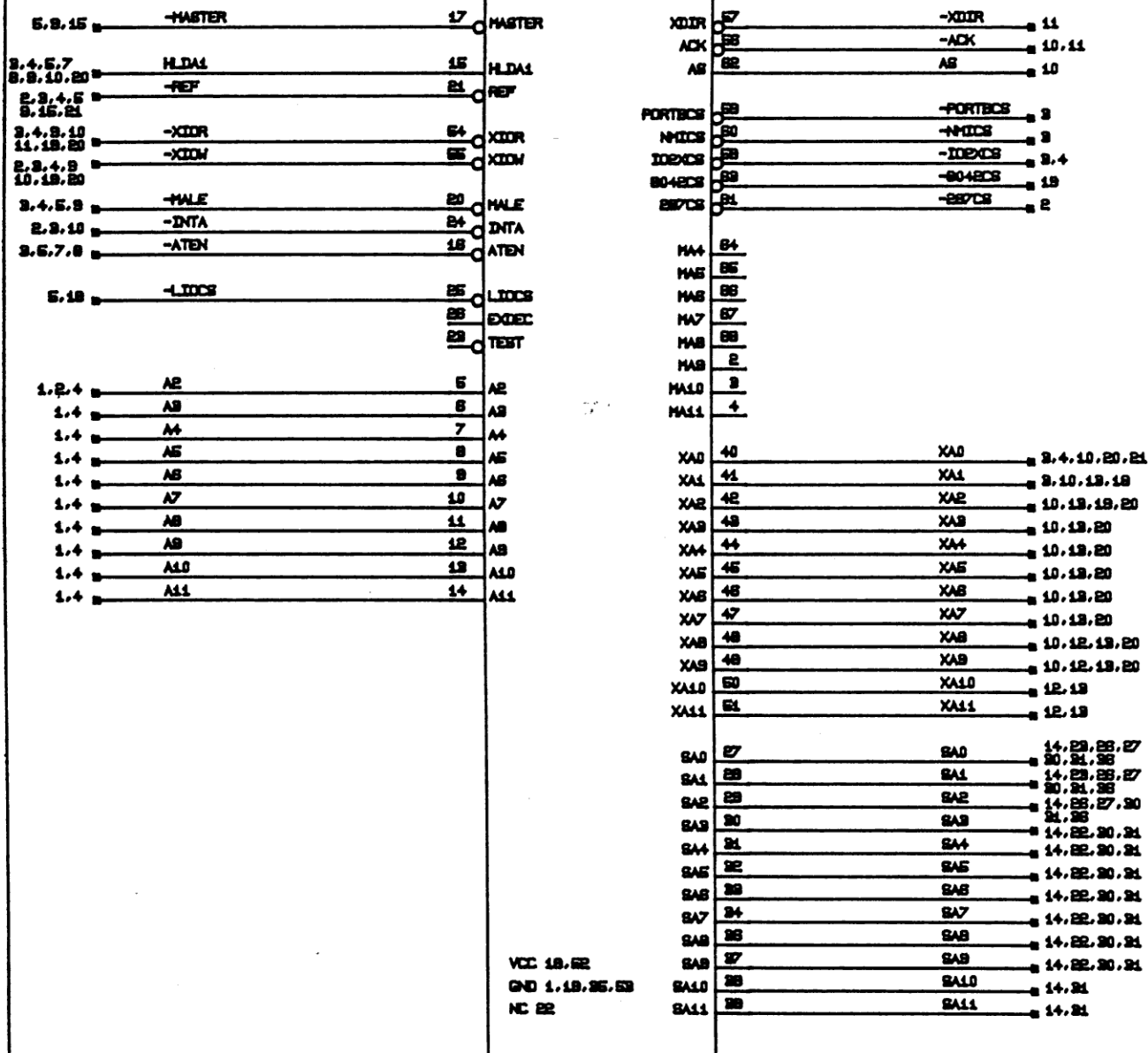




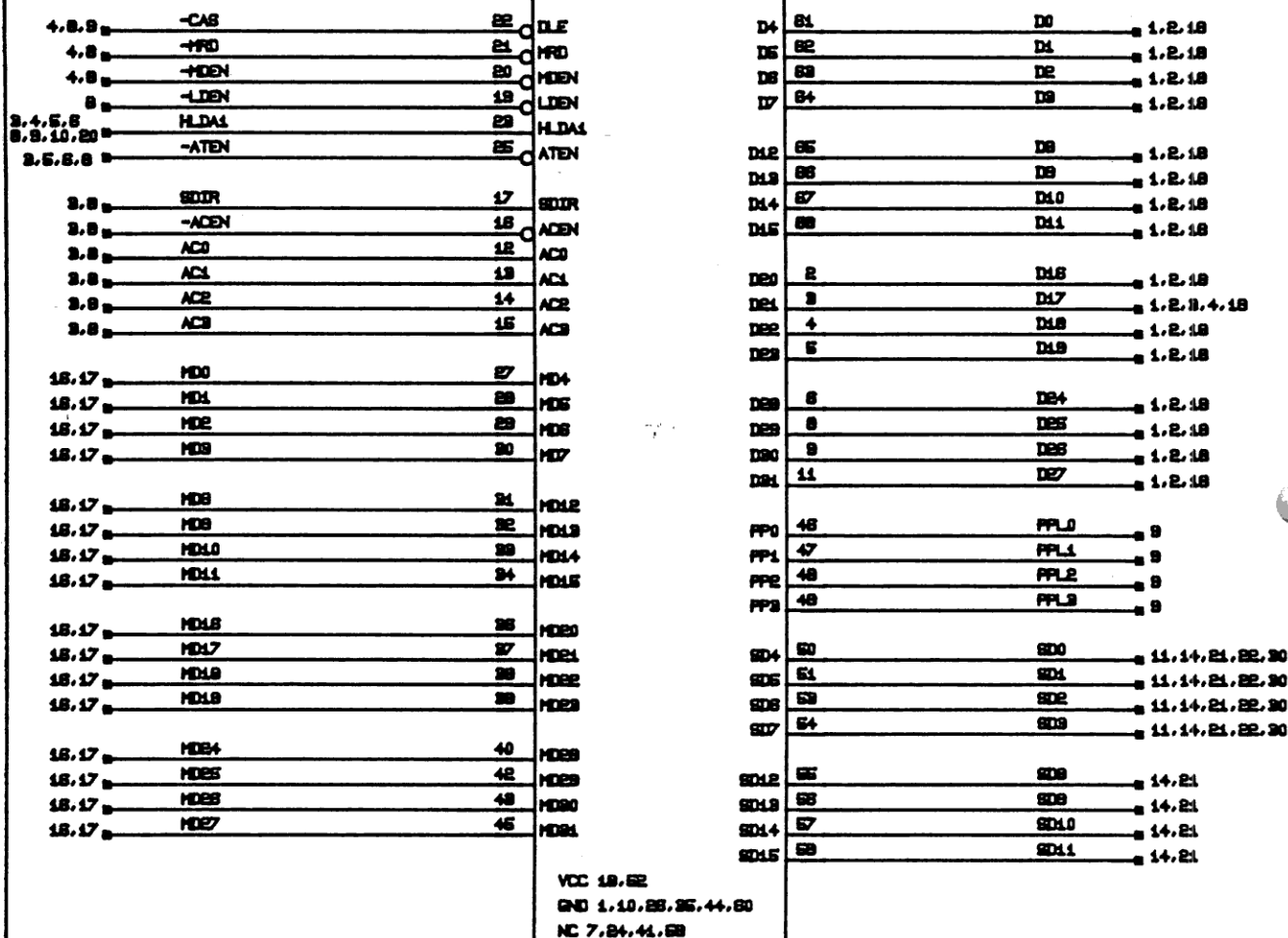
U41 7.82A303



UB0 / .82A804



U74 / .82A305

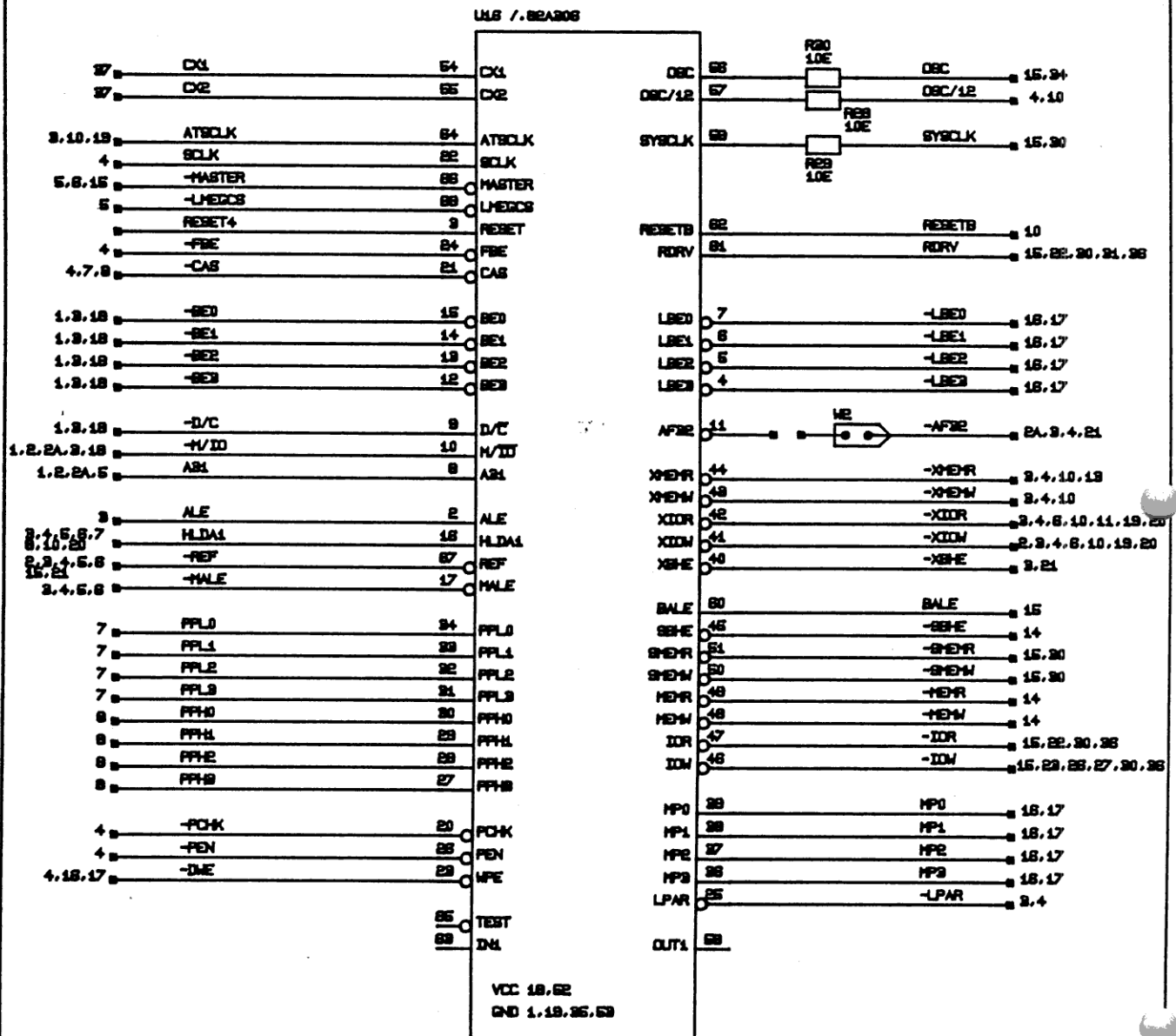


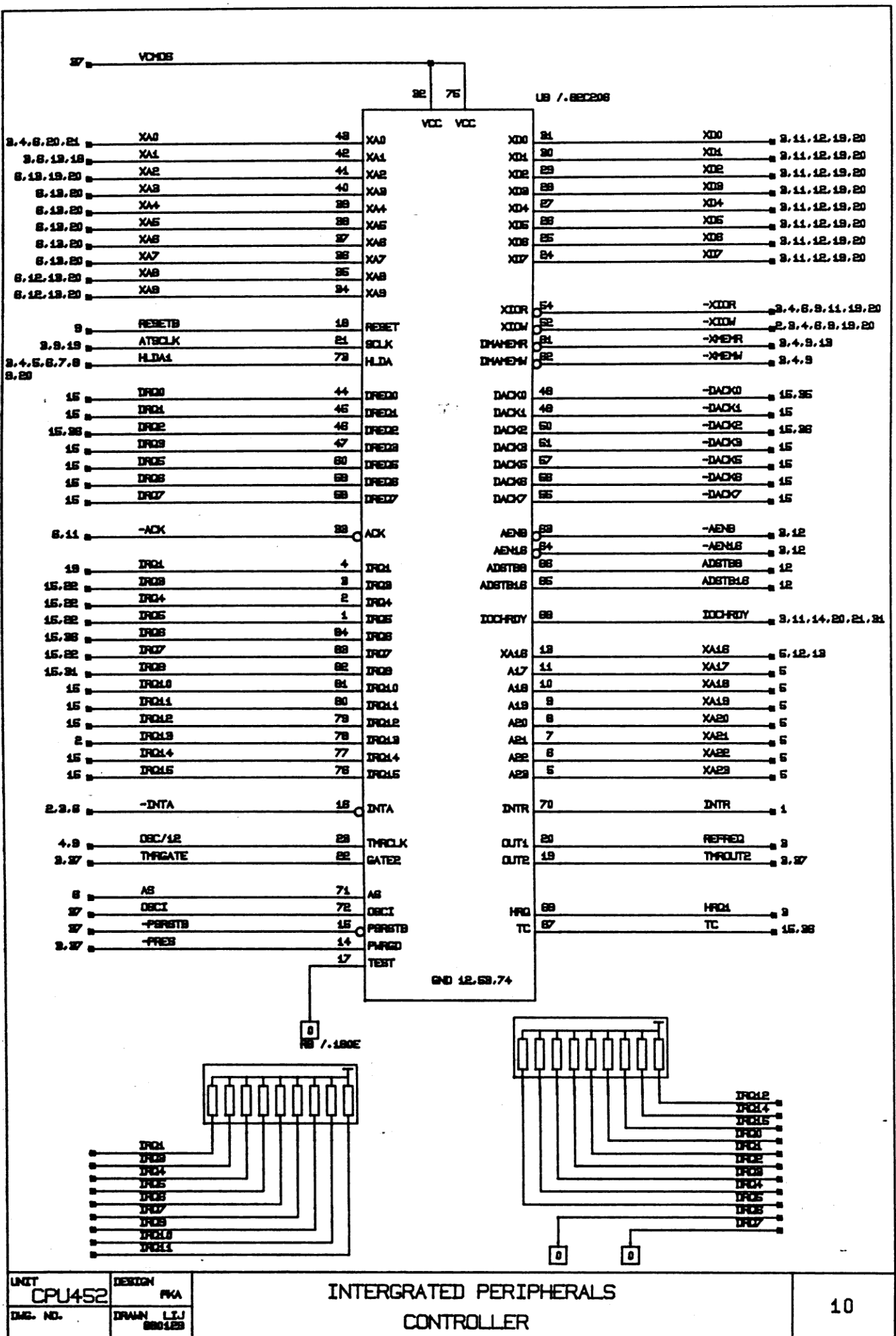
LIBS / .BEAS06

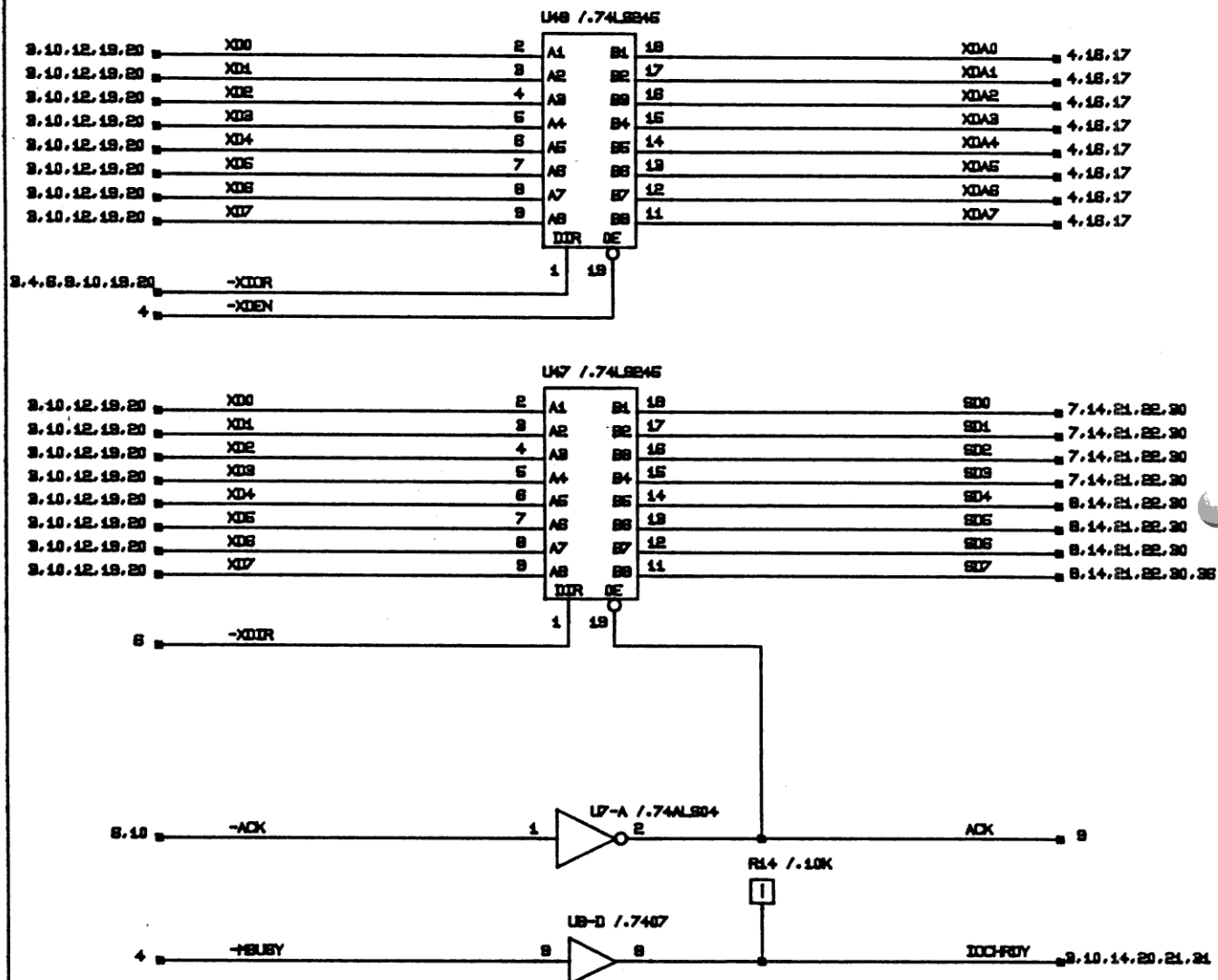
4,7,8	-CAS	22	DLE
4,7	-HFB	21	HFB
4,7	-HDEN	20	HDEN
7	-LDEN	18	LDEN
3,4,5,6,7	H.LDA1	25	H.LDA1
3,5,6,7	-ATEN	26	ATEN
3,7	SDDR	17	SDDR
3,7	-ACEN	16	ACEN
3,7	AC0	12	AC0
3,7	AC1	13	AC1
3,7	AC2	14	AC2
3,7	AC3	15	AC3
18,17	MD4	27	MD4
18,17	MD5	28	MD5
18,17	MD6	29	MD6
18,17	MD7	30	MD7
18,17	MD12	31	MD12
18,17	MD13	32	MD13
18,17	MD14	33	MD14
18,17	MD15	34	MD15
18,17	MD20	35	MD20
18,17	MD21	37	MD21
18,17	MD22	38	MD22
18,17	MD23	39	MD23
18,17	MD28	40	MD28
18,17	MD29	42	MD29
18,17	MD30	43	MD30
18,17	MD31	45	MD31

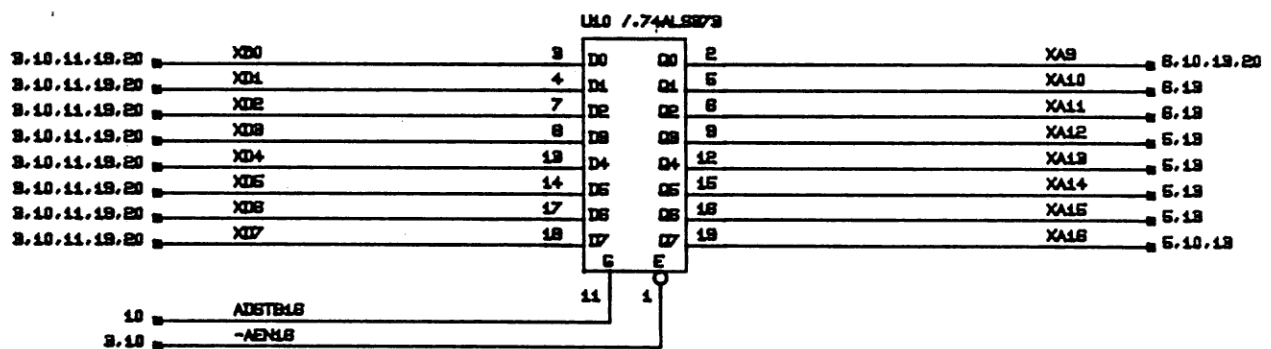
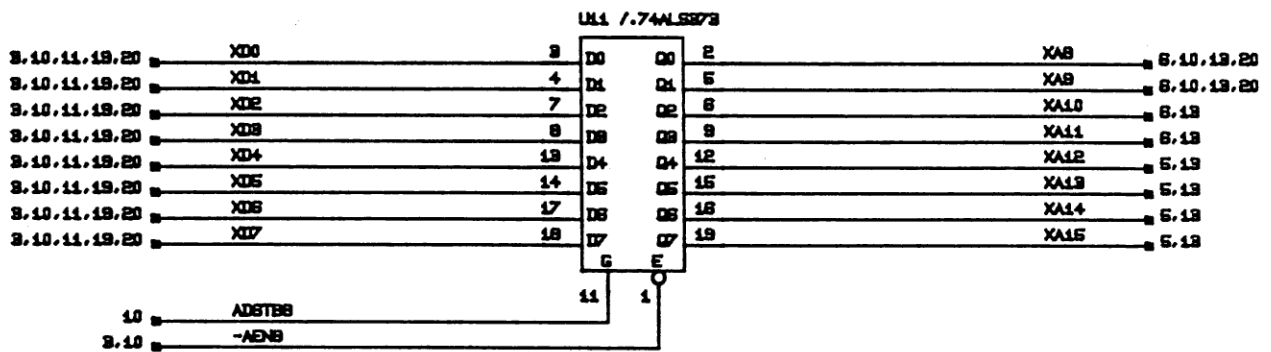
VCC 18,32
GND 1,10,25,26,44,60
NC 7,24,41,63

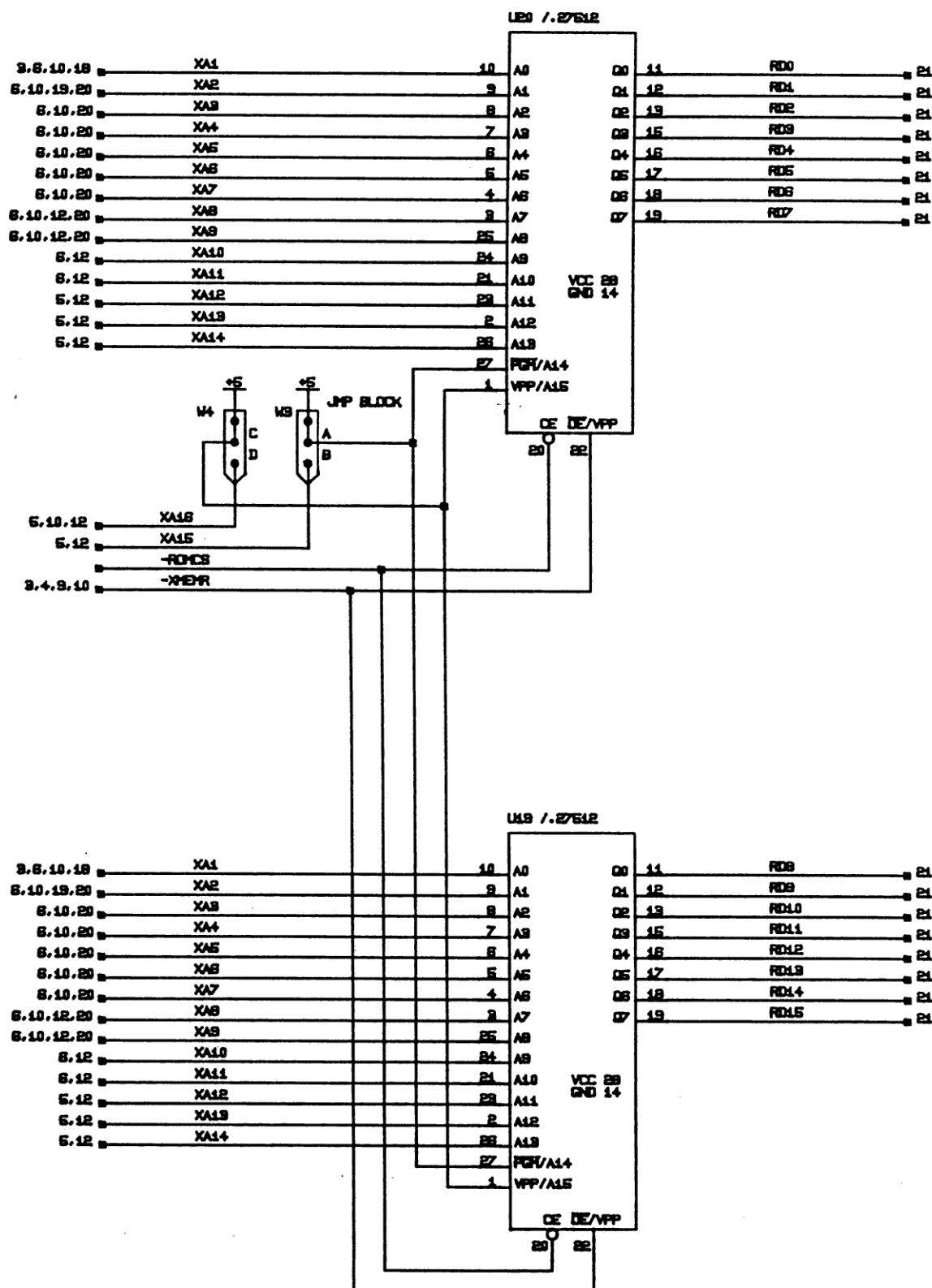
D4	81	D4	1,2,18
D5	82	D5	1,2,18
D6	83	D6	1,2,18
D7	84	D7	1,2,18
D12	85	D12	1,2,18
D13	86	D13	1,2,18
D14	87	D14	1,2,18
D15	88	D15	1,2,18
D20	2	D20	1,2,18
D21	3	D21	1,2,18
D22	4	D22	1,2,18
D23	5	D23	1,2,18
D28	6	D28	1,2,18
D29	8	D29	1,2,18
D30	9	D30	1,2,18
D31	11	D31	1,2,18
PP0	46	PP10	9
PP1	47	PP11	9
PP2	48	PP12	9
PP3	49	PP13	9
SD4	50	SD4	11,14,21,22,30
SD5	51	SD5	11,14,21,22,30
SD6	52	SD6	11,14,21,22,30
SD7	54	SD7	11,14,21,22,30,36
SD12	55	SD12	14,21
SD13	56	SD13	14,21
SD14	57	SD14	14,21
SD15	58	SD15	14,21







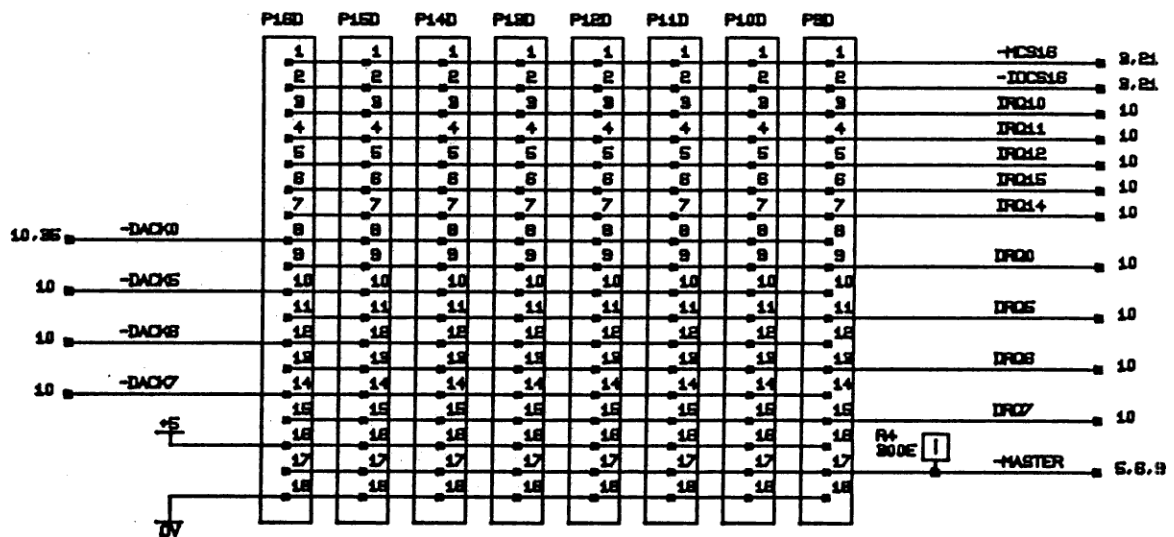
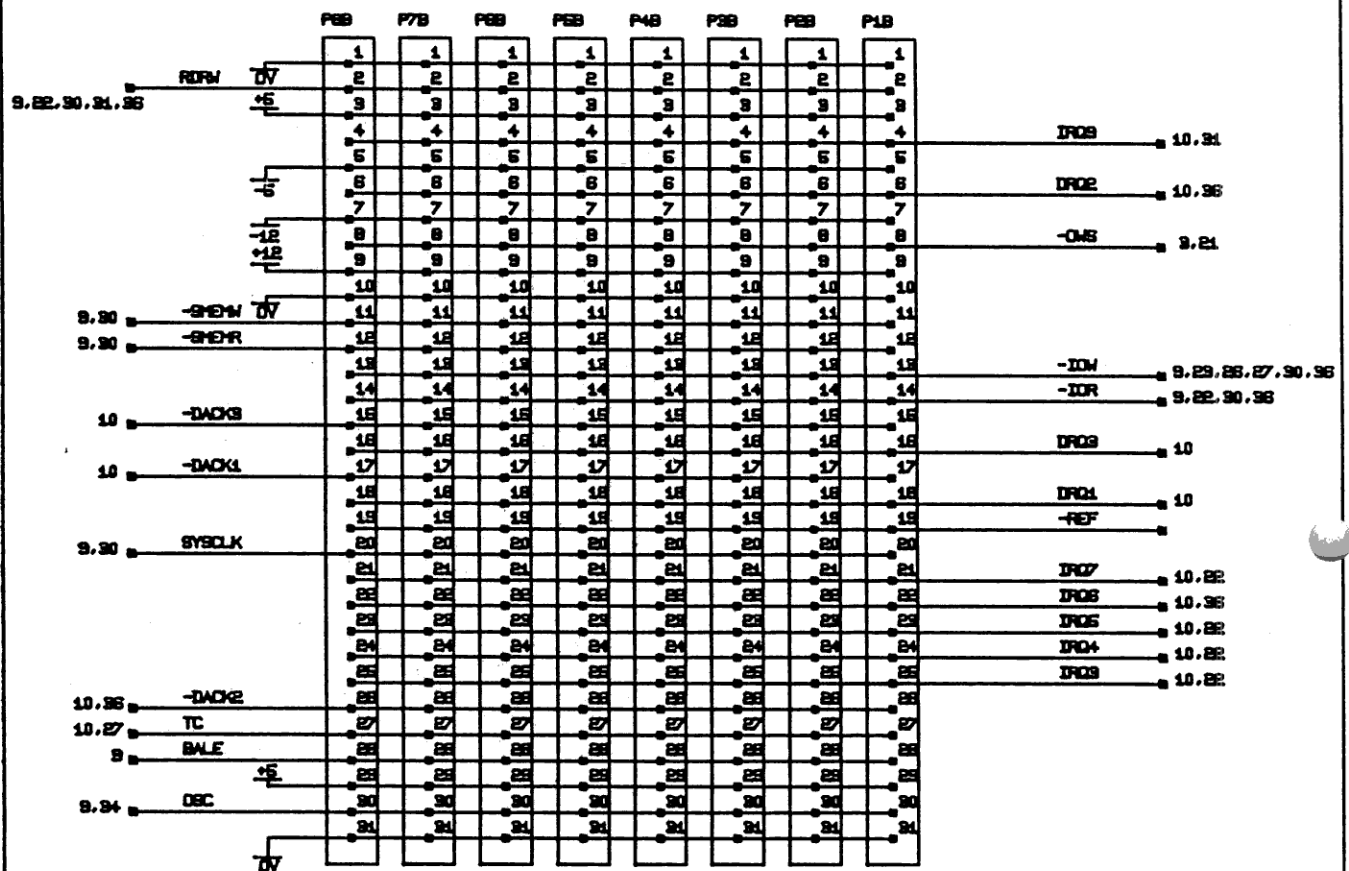


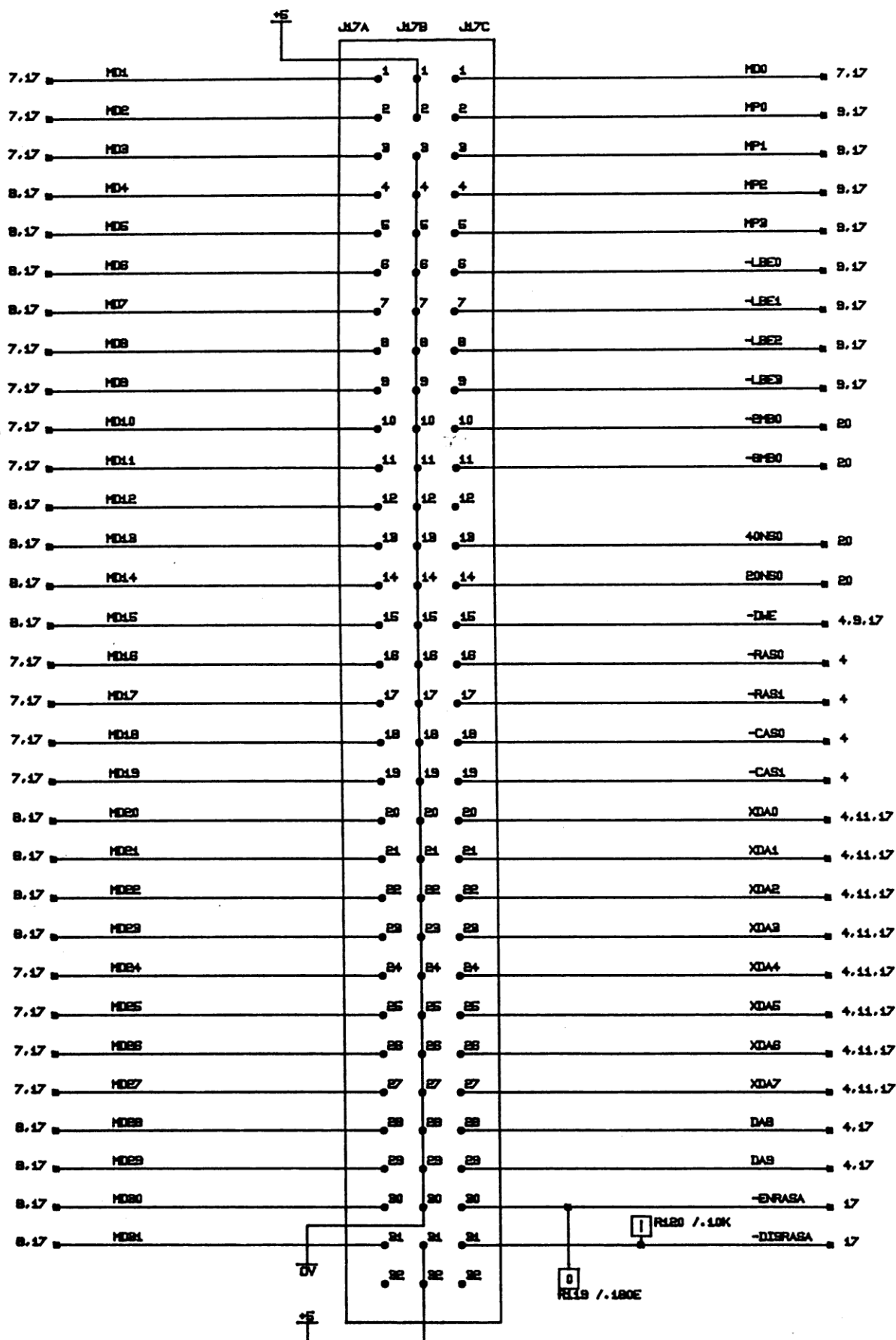


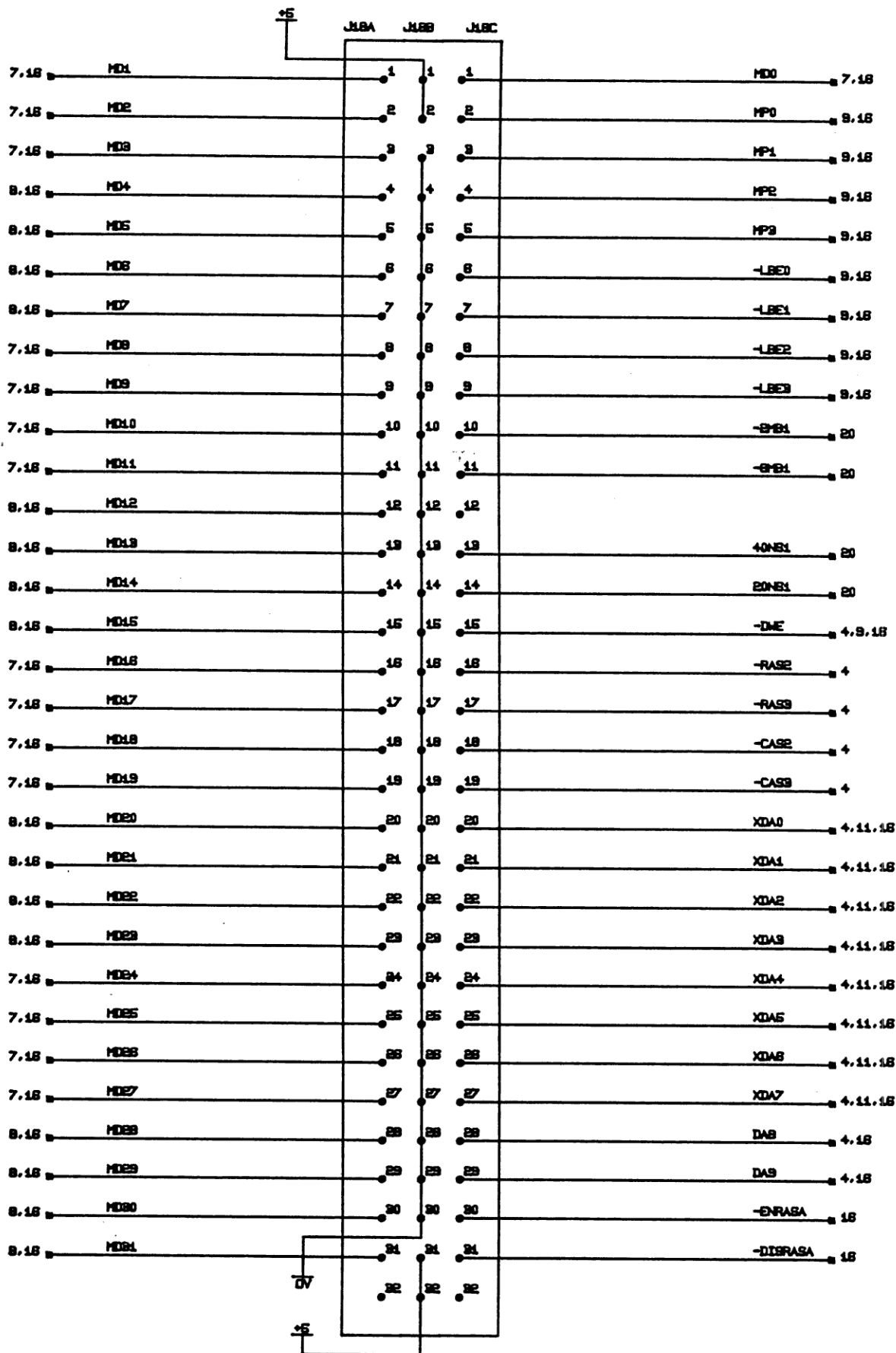
2 X 27128 - 200 JUMPER A+C
 2 X 27256 - 200 JUMPER B+C
 2 X 27642 - 200 JUMPER B+D

		P6A	P7A	P6A	P6A	P4A	P2A	P2A	P1A	
		1	1	1	1	1	1	1	1	-IOCHK → 9
		2	2	2	2	2	2	2	2	SD7 → 8, 11, 21, 22, 30, 36
		3	3	3	3	3	3	3	3	SD6 → 8, 11, 21, 22, 30
		4	4	4	4	4	4	4	4	SD5 → 8, 11, 21, 22, 30
		5	5	5	5	5	5	5	5	SD4 → 8, 11, 21, 22, 30
		6	6	6	6	6	6	6	6	SD3 → 7, 11, 21, 22, 30
		7	7	7	7	7	7	7	7	SD2 → 7, 11, 21, 22, 30
		8	8	8	8	8	8	8	8	SD1 → 7, 11, 21, 22, 30
		9	9	9	9	9	9	9	9	SD0 → 7, 11, 21, 22, 30
		10	10	10	10	10	10	10	10	IOCHK → 8, 10, 11, 20, 21, 24
9, 20, 22, 36	AEN	11	11	11	11	11	11	11	11	
6, 30	SA19	12	12	12	12	12	12	12	12	
6, 30	SA18	13	13	13	13	13	13	13	13	
6, 30	SA17	14	14	14	14	14	14	14	14	
6, 30	SA16	15	15	15	15	15	15	15	15	
6, 30, 34	SA15	16	16	16	16	16	16	16	16	
6, 30, 34	SA14	17	17	17	17	17	17	17	17	
6, 34	SA13	18	18	18	18	18	18	18	18	
6, 34	SA12	19	19	19	19	19	19	19	19	
6, 34	SA11	20	20	20	20	20	20	20	20	
6, 34	SA10	21	21	21	21	21	21	21	21	
6, 22, 30, 34	SA9	22	22	22	22	22	22	22	22	
6, 22, 30, 34	SA8	23	23	23	23	23	23	23	23	
6, 22, 30, 34	SA7	24	24	24	24	24	24	24	24	
6, 22, 30, 34	SA6	25	25	25	25	25	25	25	25	
6, 22, 30, 34	SA5	26	26	26	26	26	26	26	26	
6, 22, 30, 34	SA4	27	27	27	27	27	27	27	27	
6, 22, 30, 34	SA3	28	28	28	28	28	28	28	28	
6, 22, 27, 30, 34, 36	SA2	29	29	29	29	29	29	29	29	
6, 22, 28, 27, 30, 34, 36	SA1	30	30	30	30	30	30	30	30	
6, 22, 28, 27, 30, 34, 36	SA0	31	31	31	31	31	31	31	31	

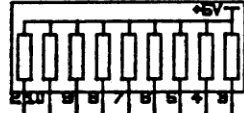
		P16C	P16C	P14C	P16C	P16C	P11C	P10C	P8C	
9	-BHE	1	1	1	1	1	1	1	1	
6	SA29	2	2	2	2	2	2	2	2	
6	SA28	3	3	3	3	3	3	3	3	
6	SA21	4	4	4	4	4	4	4	4	
6	SA20	5	5	5	5	5	5	5	5	
6, 30	SA19	6	6	6	6	6	6	6	6	
6, 30	SA18	7	7	7	7	7	7	7	7	
6, 30	SA17	8	8	8	8	8	8	8	8	
9	-MEM	9	9	9	9	9	9	9	9	
9	-MEM	10	10	10	10	10	10	10	10	
		11	11	11	11	11	11	11	11	SD8 → 7, 21
		12	12	12	12	12	12	12	12	SD9 → 7, 21
		13	13	13	13	13	13	13	13	SD10 → 7, 21
		14	14	14	14	14	14	14	14	SD11 → 7, 21
		15	15	15	15	15	15	15	15	SD12 → 8, 21
		16	16	16	16	16	16	16	16	SD13 → 8, 21
		17	17	17	17	17	17	17	17	SD14 → 8, 21
		18	18	18	18	18	18	18	18	SD15 → 21







RP17/.9-10K



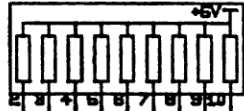
D0 1.2.7
D1 1.2.7
D2 1.2.7
D3 1.2.7
D4 1.2.8
D5 1.2.8
D6 1.2.8
D7 1.2.8
-READY 1.2.9,4,7

RP14/.9-10K



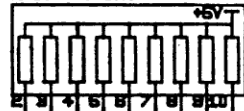
D8 1.2.7
D9 1.2.7
D10 1.2.7
D11 1.2.7
D12 1.2.8
D13 1.2.8
D14 1.2.8
D15 1.2.8
-ADS 1.2.2A,3

RP15/.9-10K



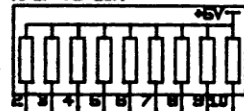
D16 1.2.7
D17 1.2.9,4,7
D18 1.2.7
D19 1.2.7
D20 1.2.8
D21 1.2.8
D22 1.2.8
D23 1.2.8
-BUSY 1.2

RP16/.9-10K



D24 1.2.7
D25 1.2.7
D26 1.2.7
D27 1.2.7
D28 1.2.8
D29 1.2.8
D30 1.2.8
D31 1.2.8
-W/R 1.2.9,4

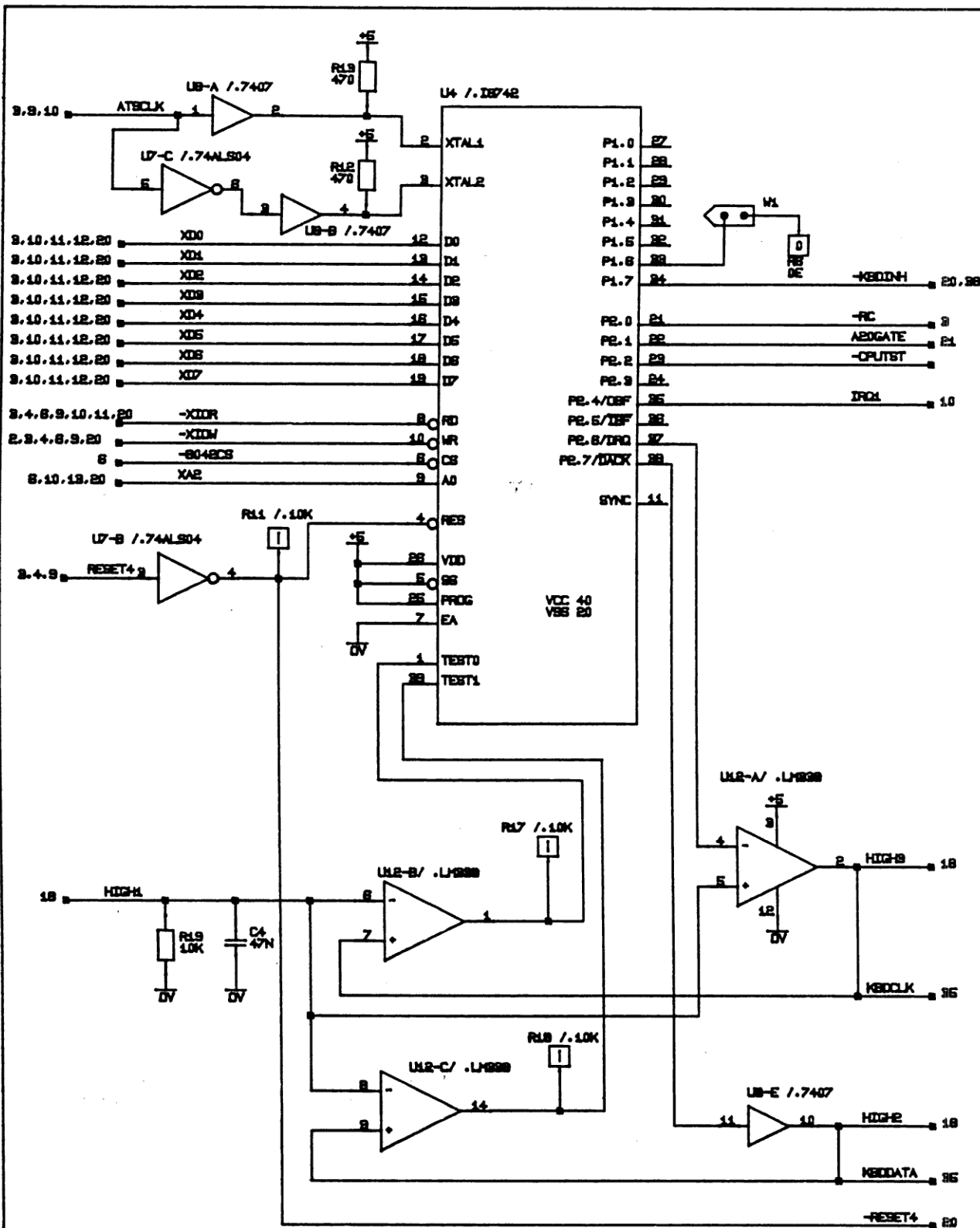
RP1/.9-10K

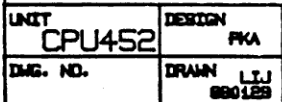


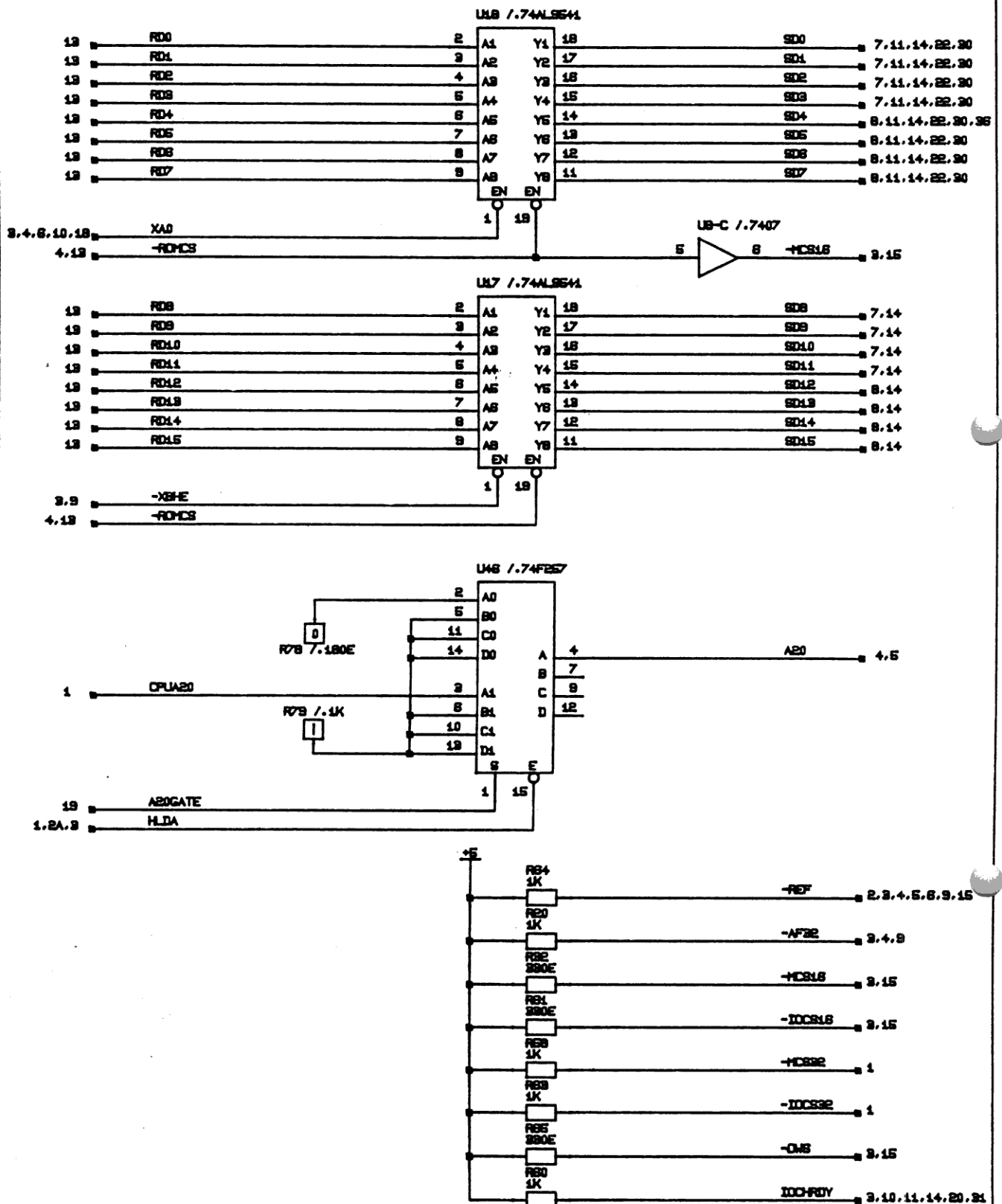
-BE0 1.3.9
-BE1 1.3.9
-BE2 1.3.9
-BE3 1.3.9
-D/C 1.3.9
-V/ID 1.2.2A,9,9
HIGH1 19,25
HIGH2 19
HIGH3 19,35

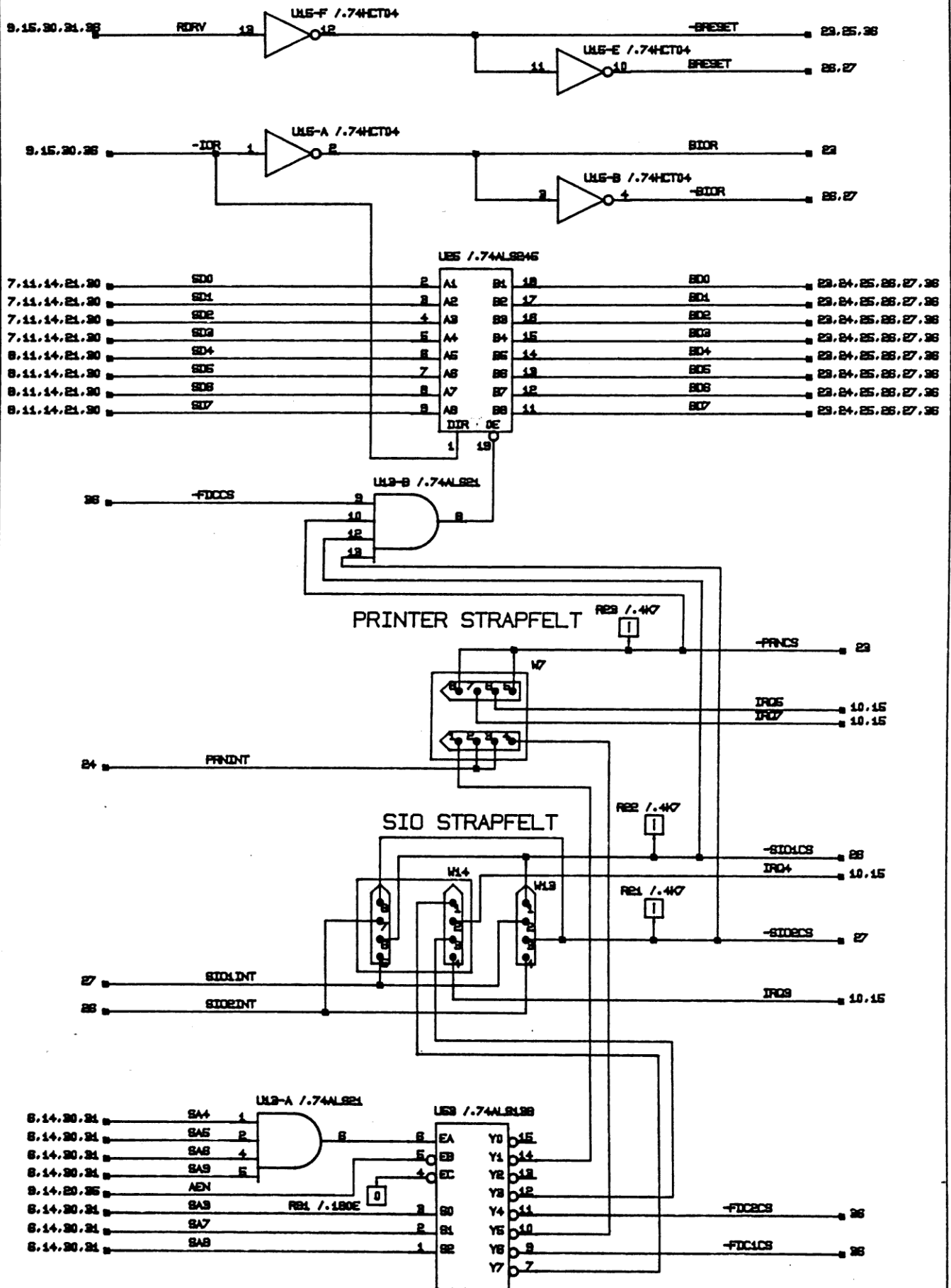
UNIT	DESIGN
CPU452	PKA
DMC. NO.	DRAWN L.I.J.
	880107

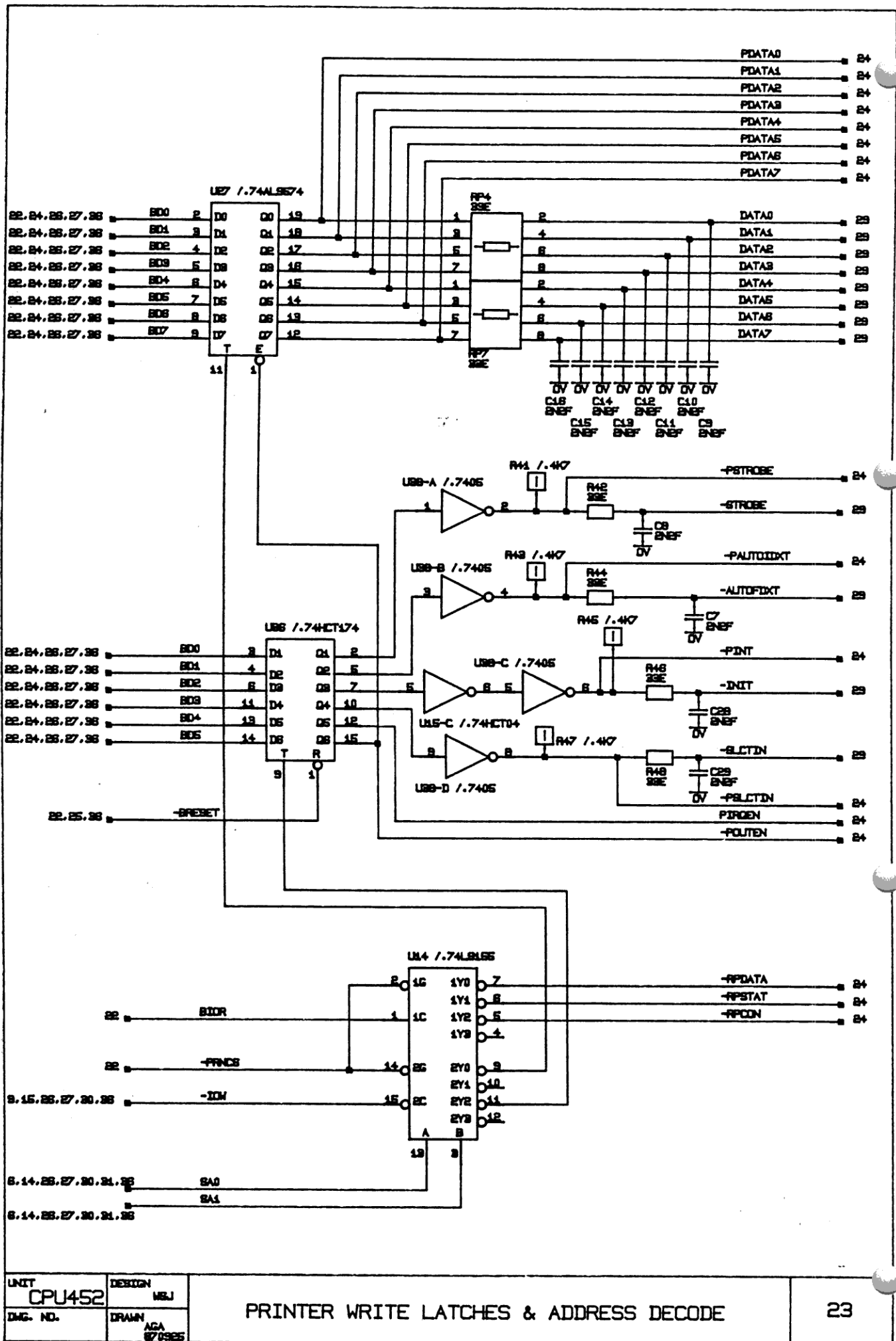
PULL UP

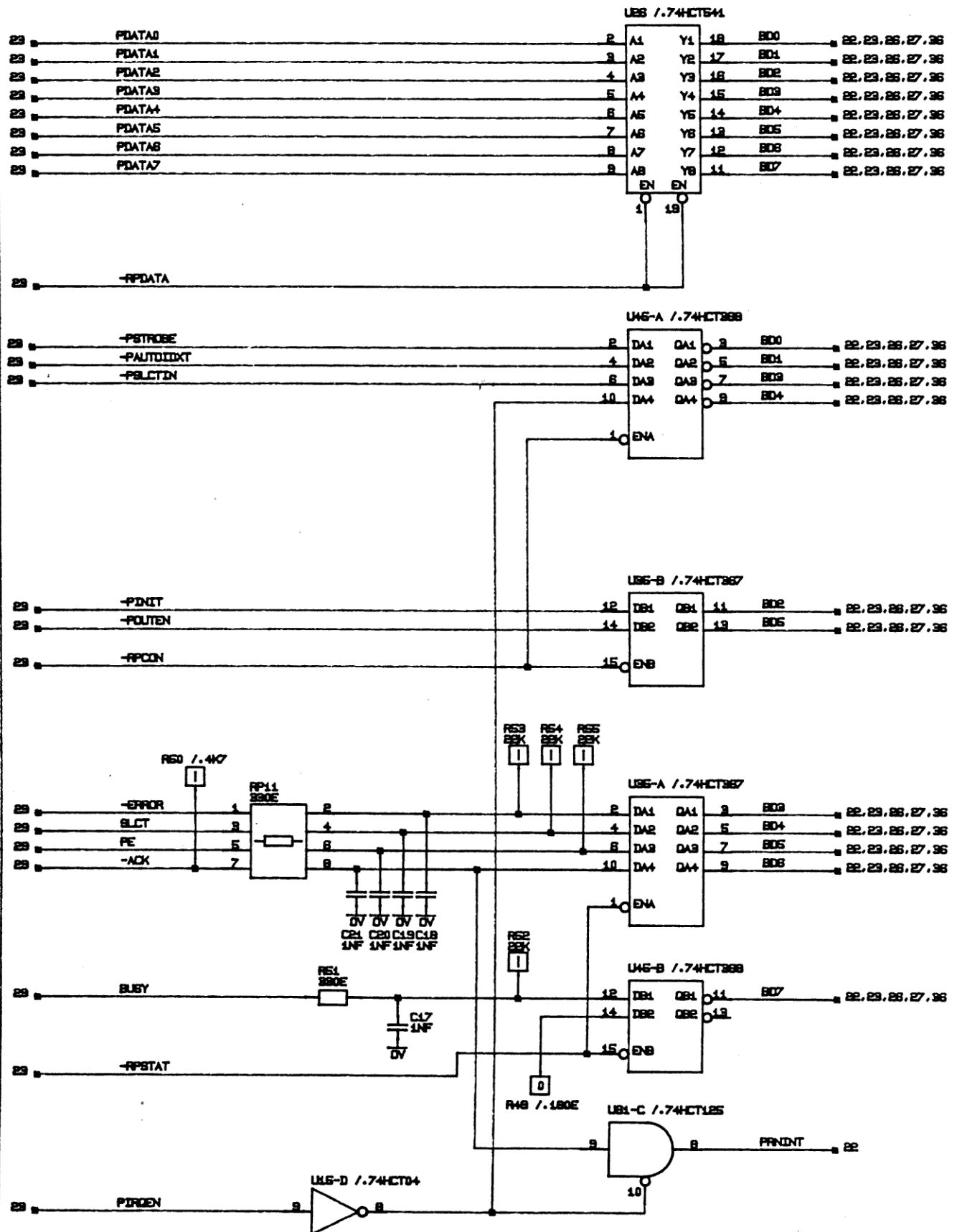


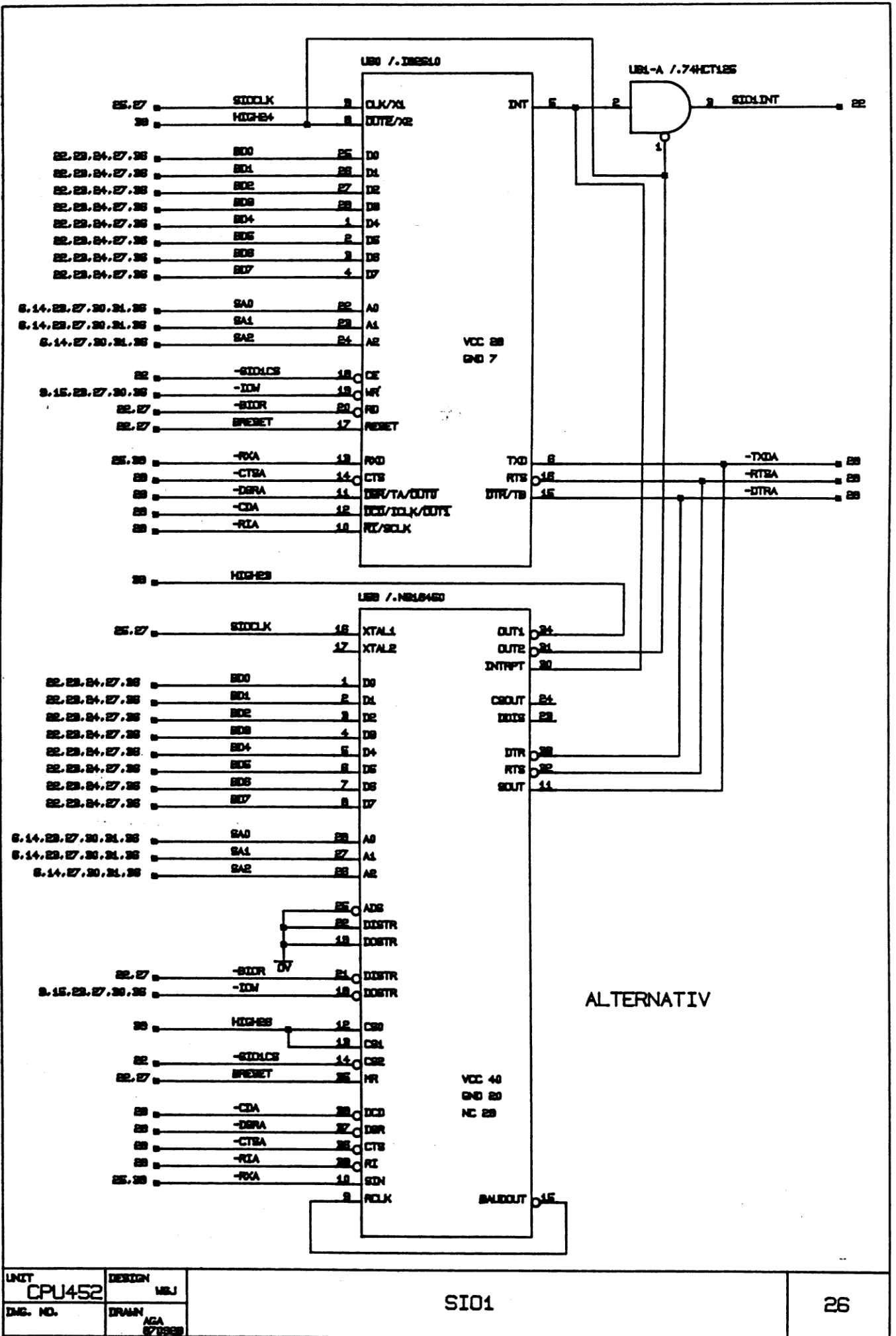


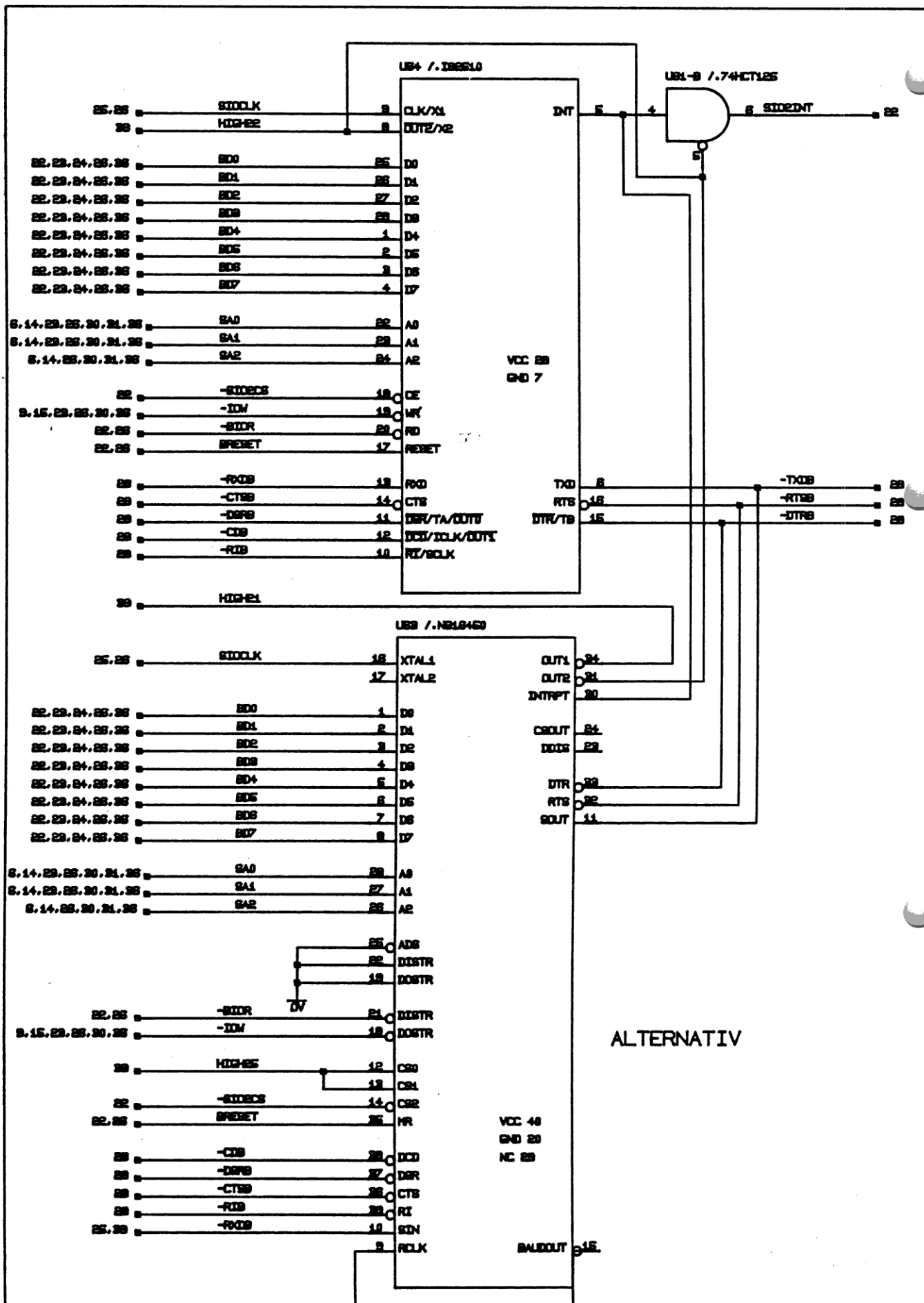


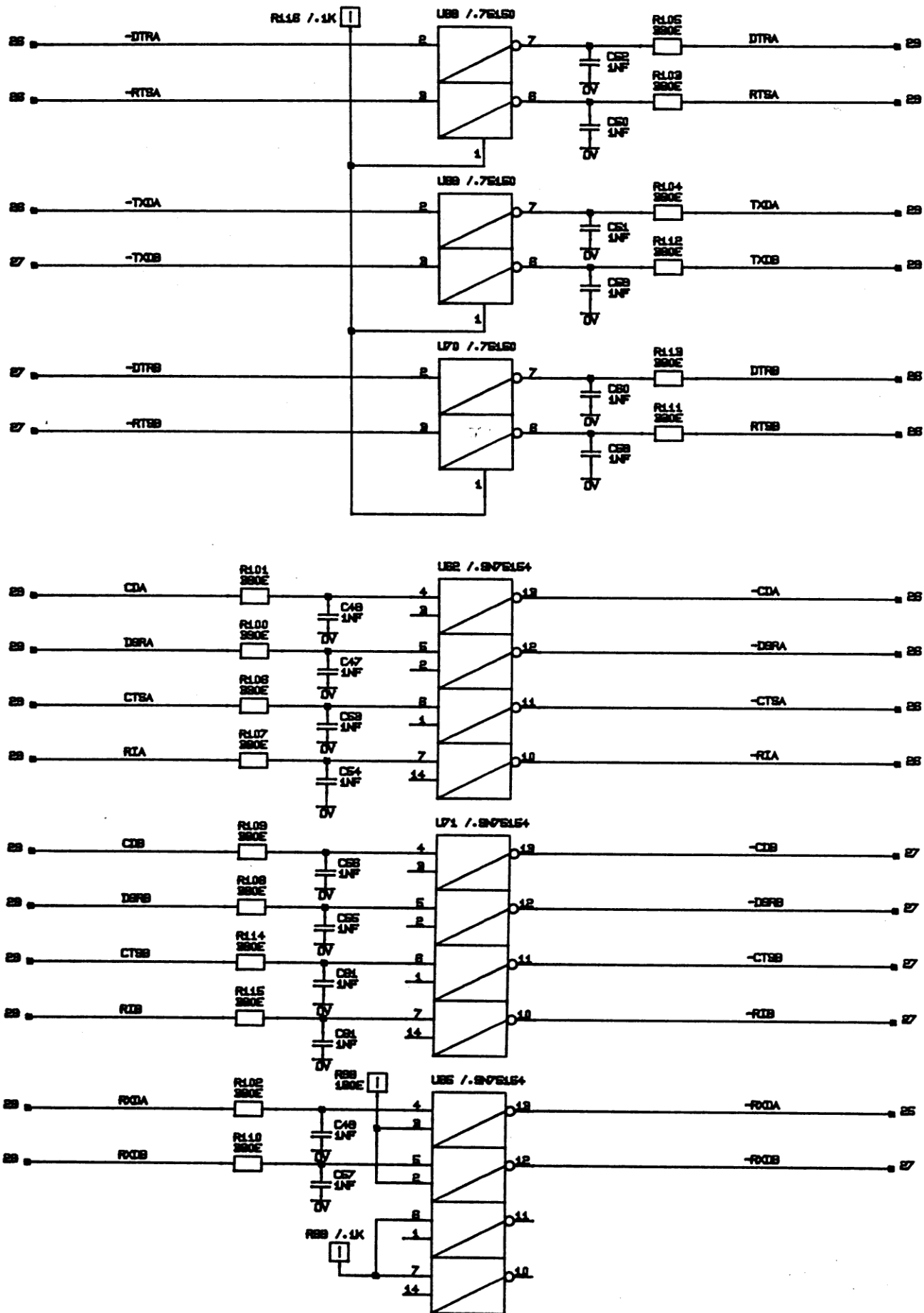








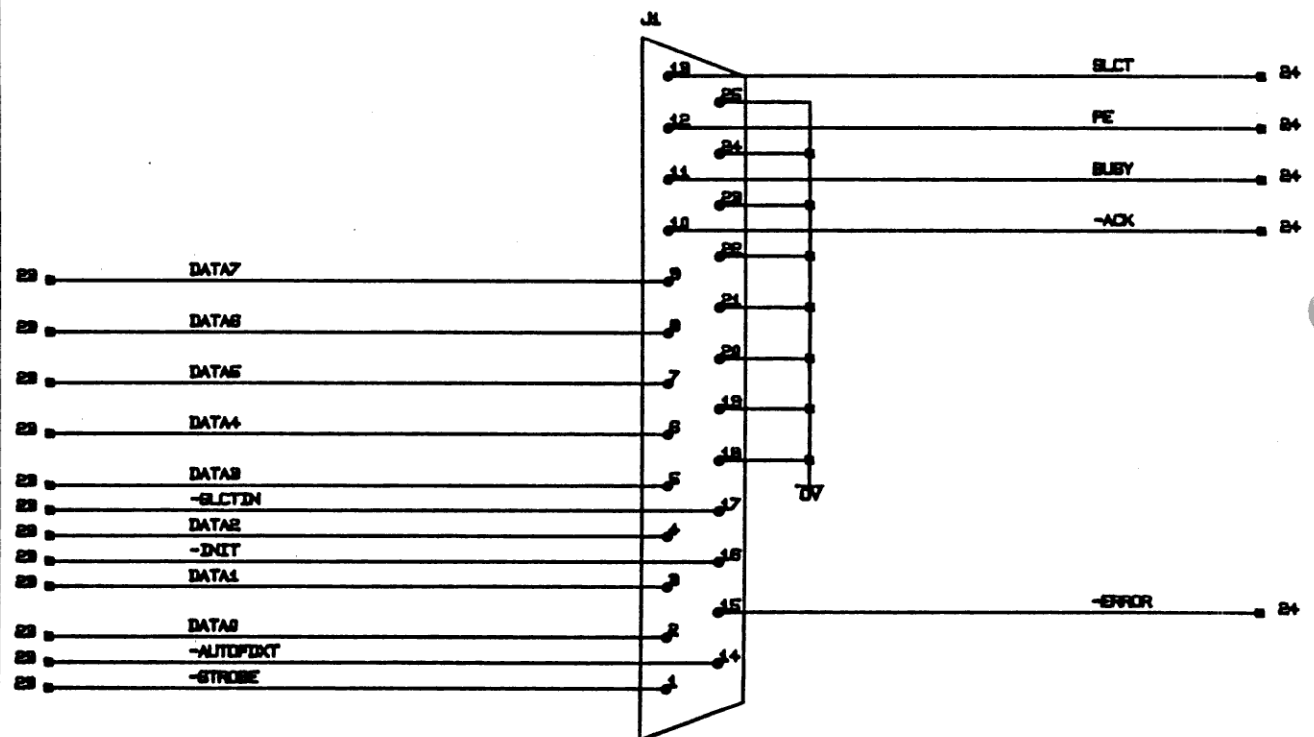
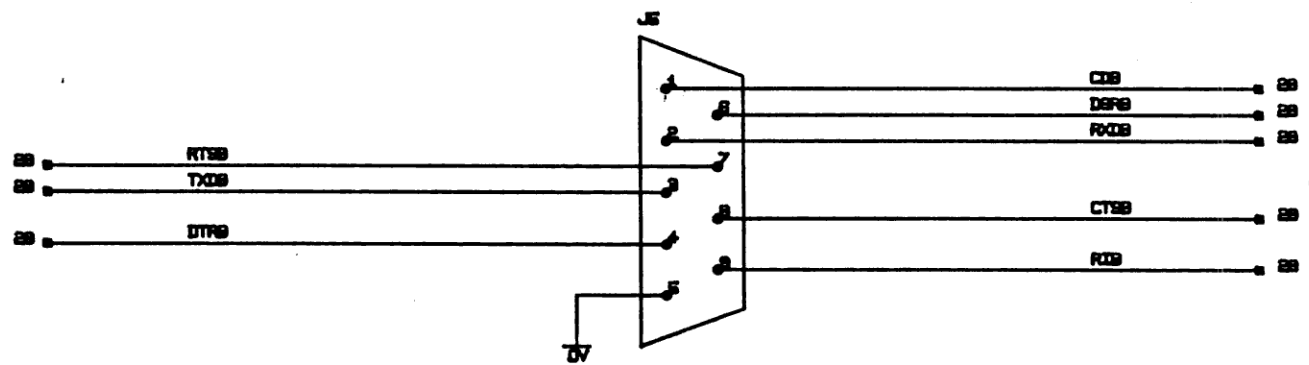
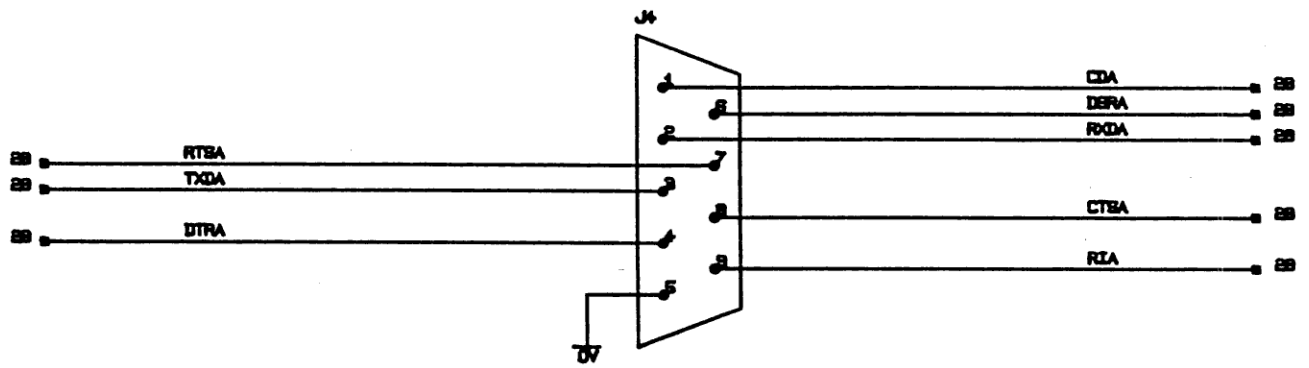




UNIT	DESIGN
CPU452	MSJ
DMG. NO.	DRAWN
	ACA
	07/09/90

V24 INTERFACE

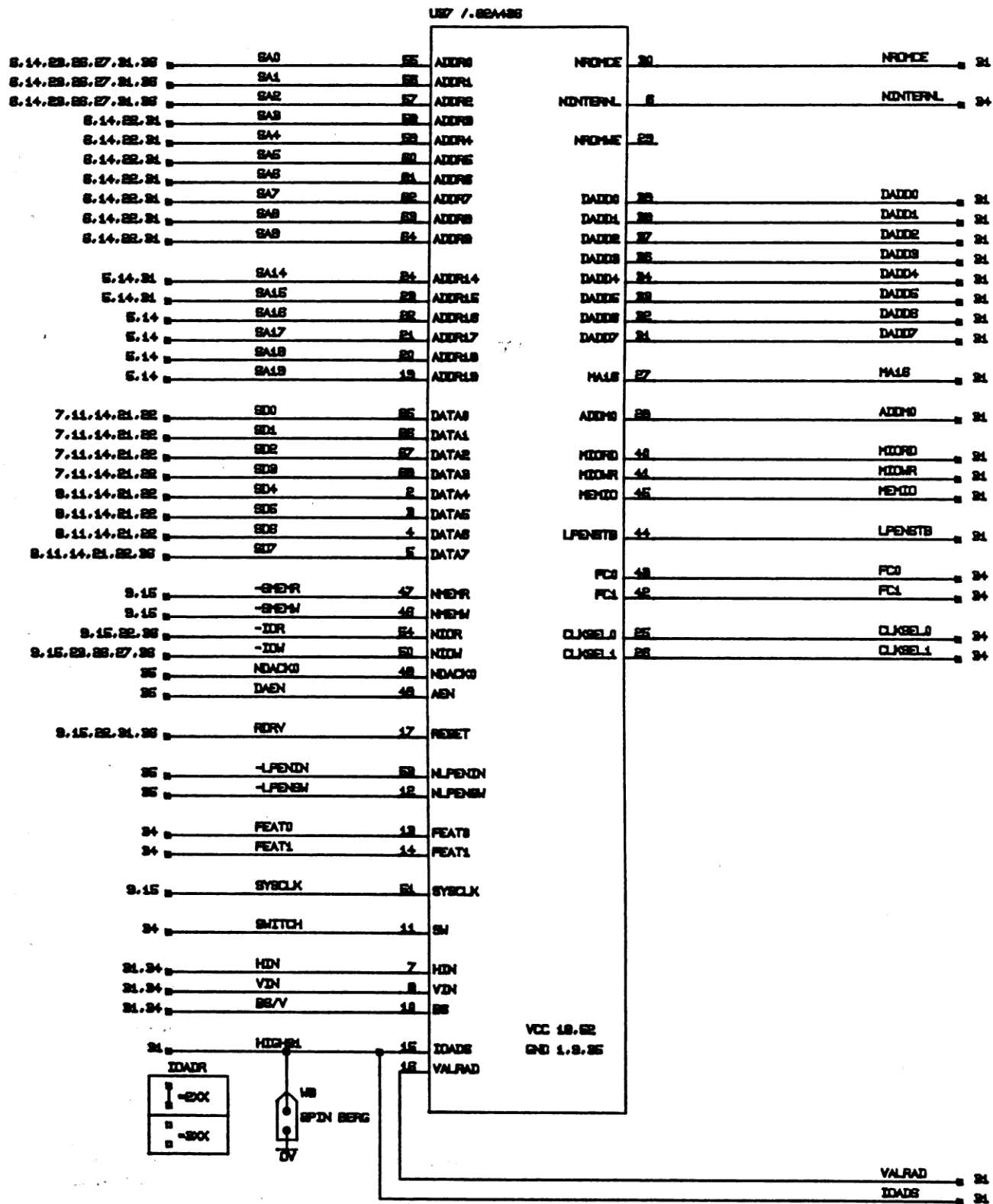
28

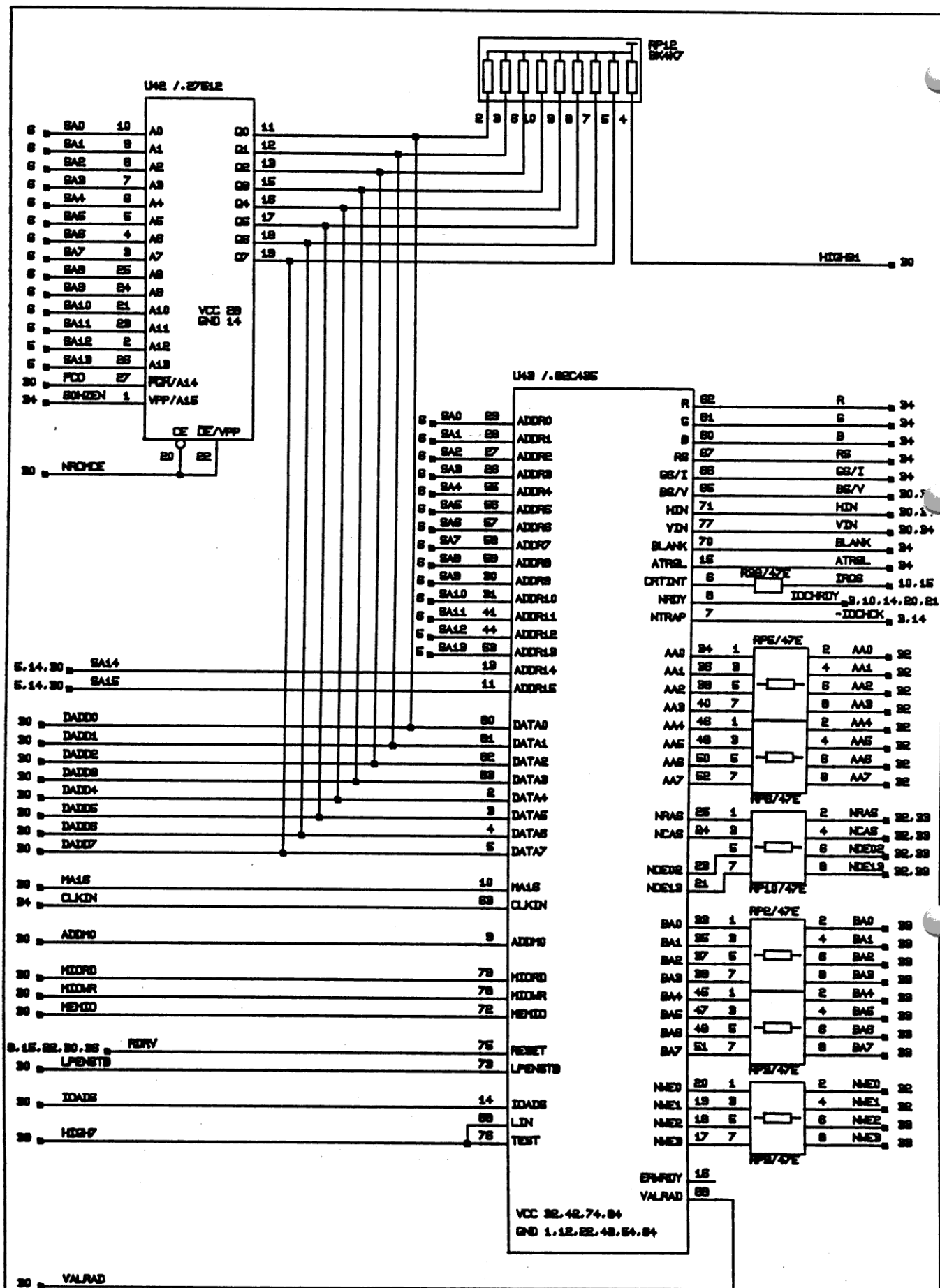


UNIT	DESIGN
CPU452	MSJ
ENG. NO.	DRAWN
	ACA
	07/1980

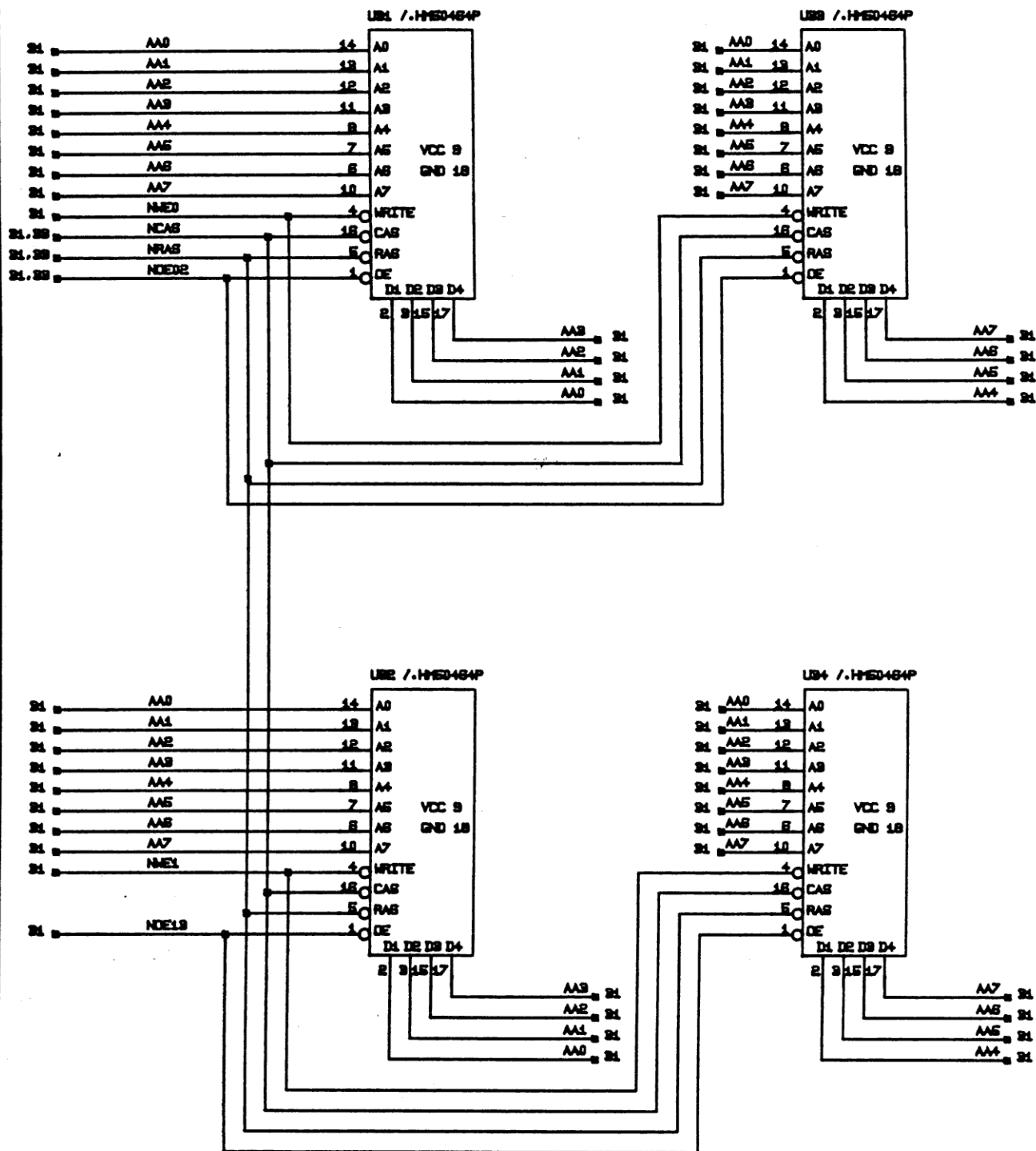
CONNECTORS

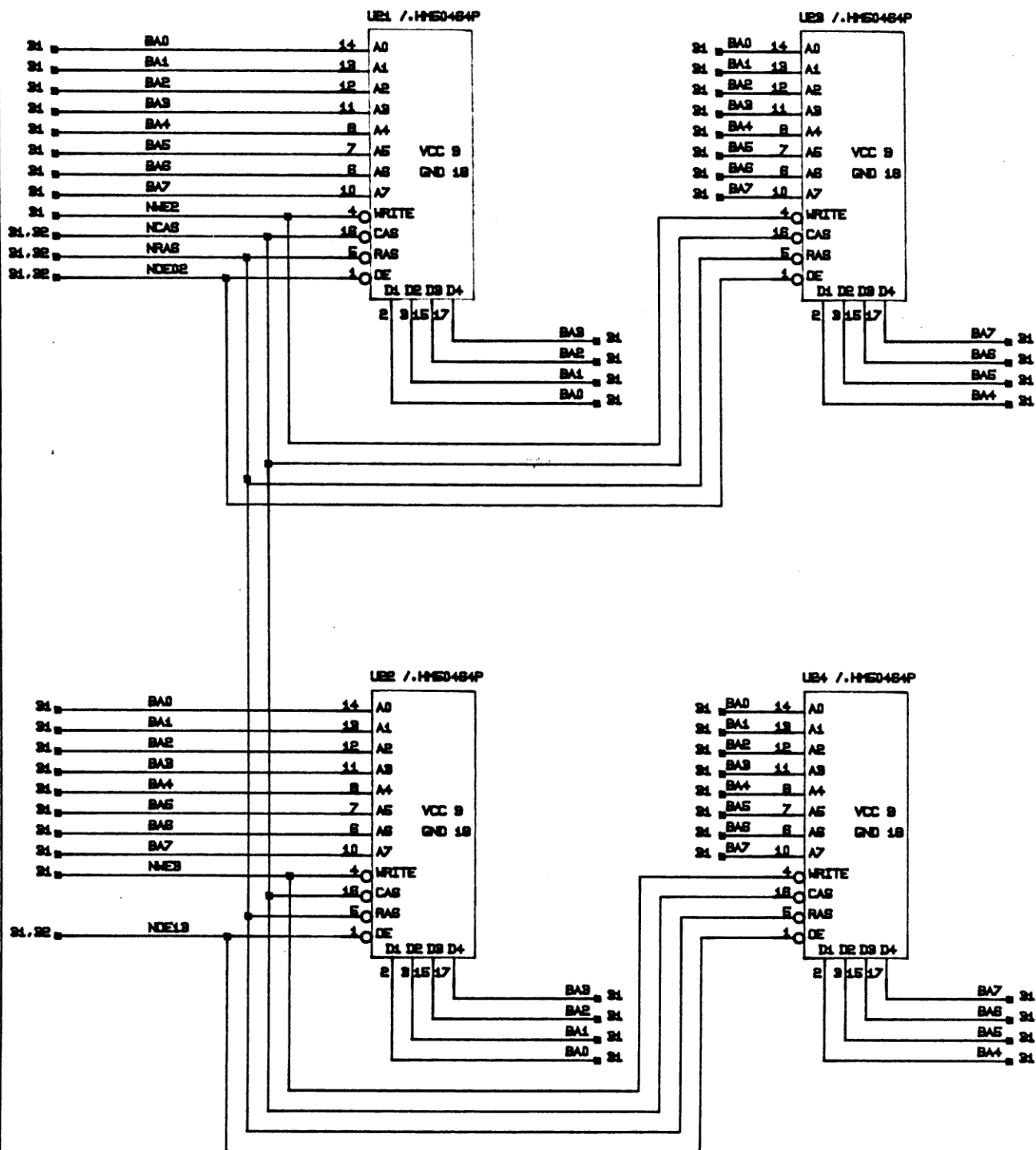
29

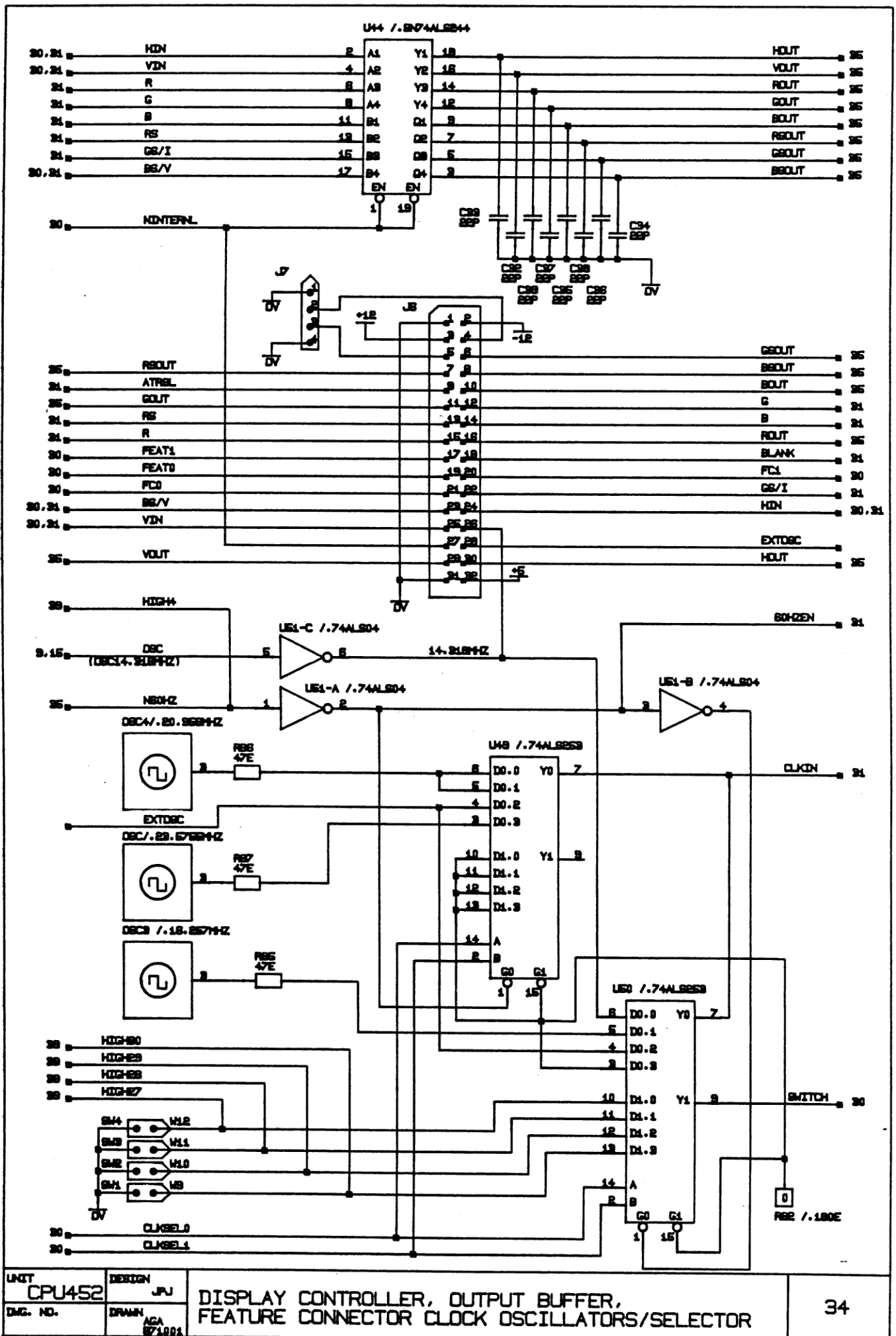


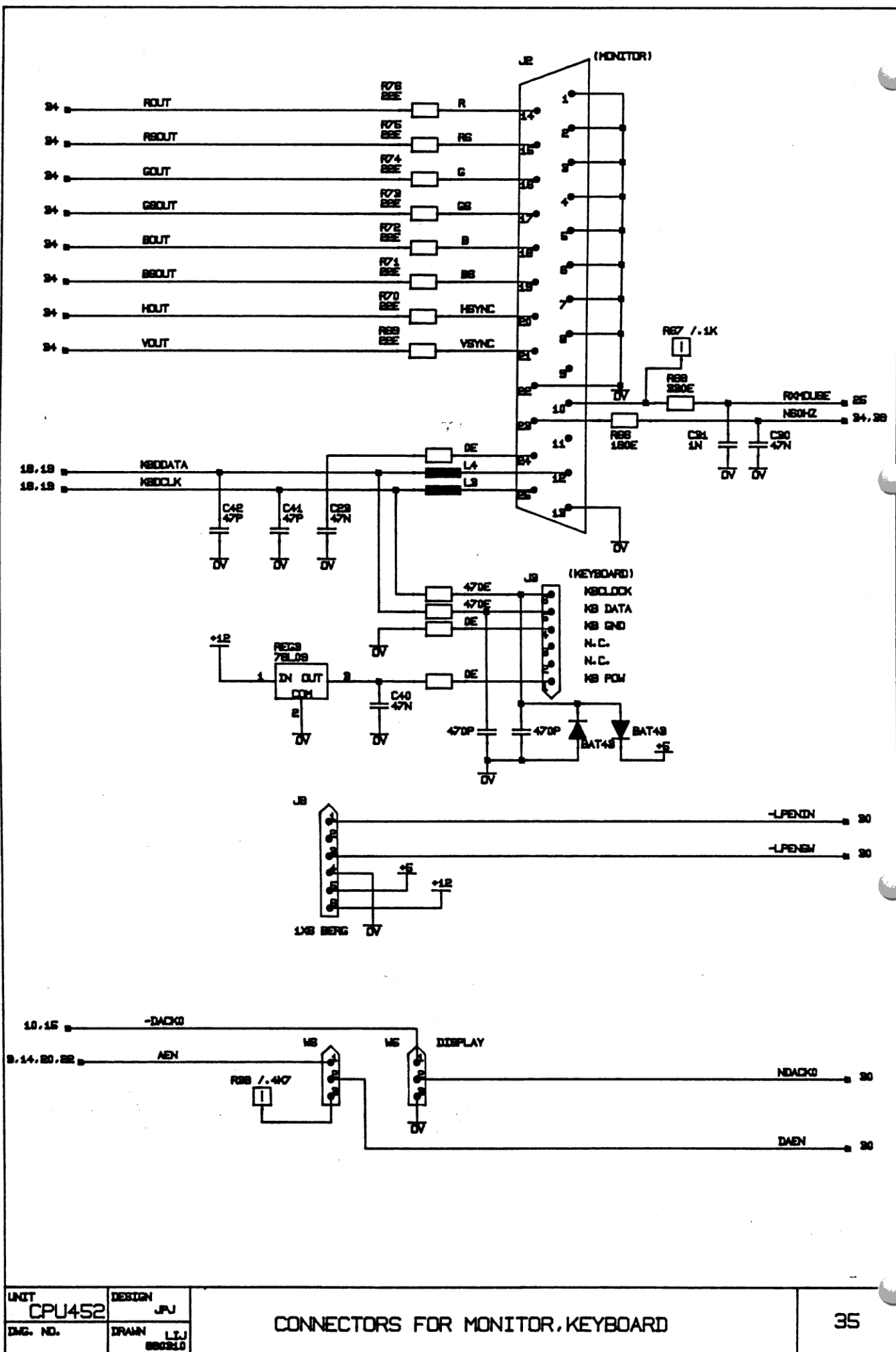


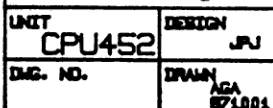
UNIT	DESIGN
CPU452	JPU
DWG. NO.	DRAWN
	AGA
	87/0580



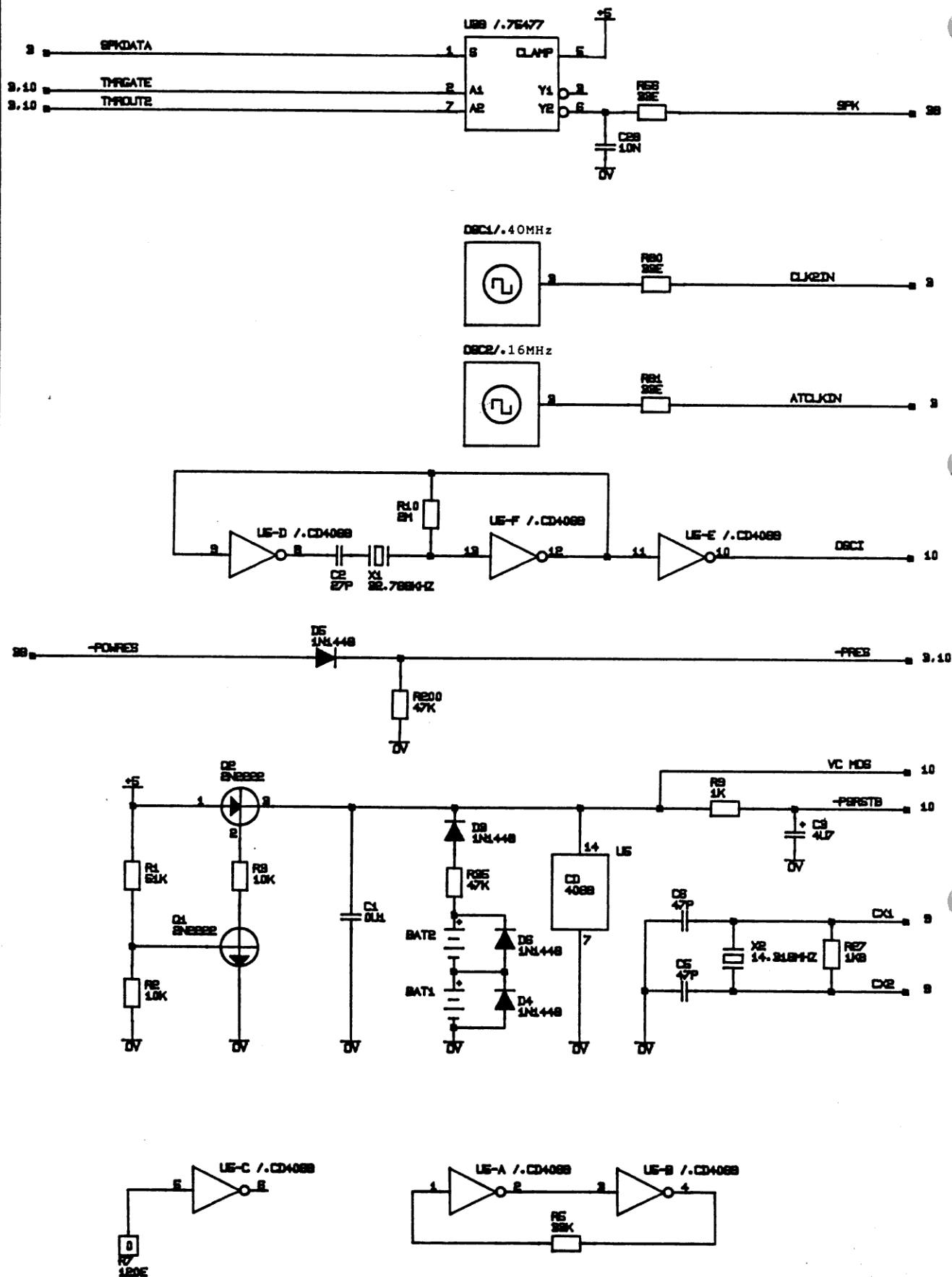


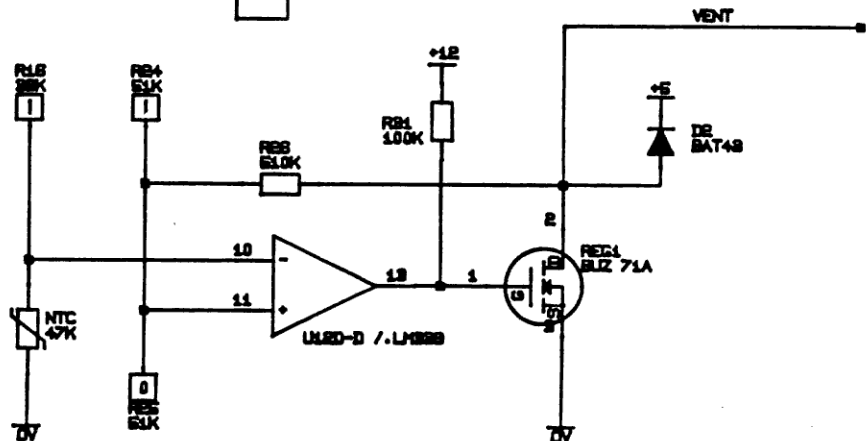
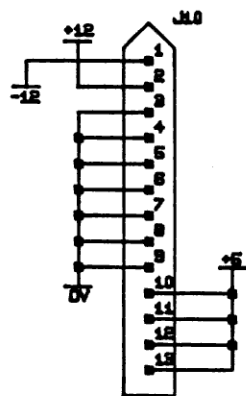
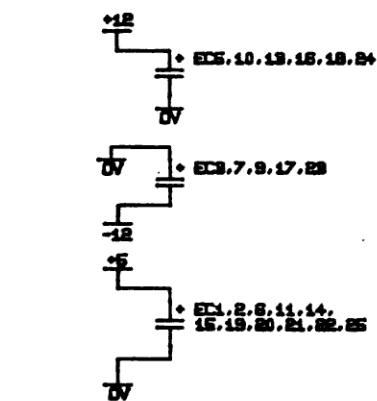
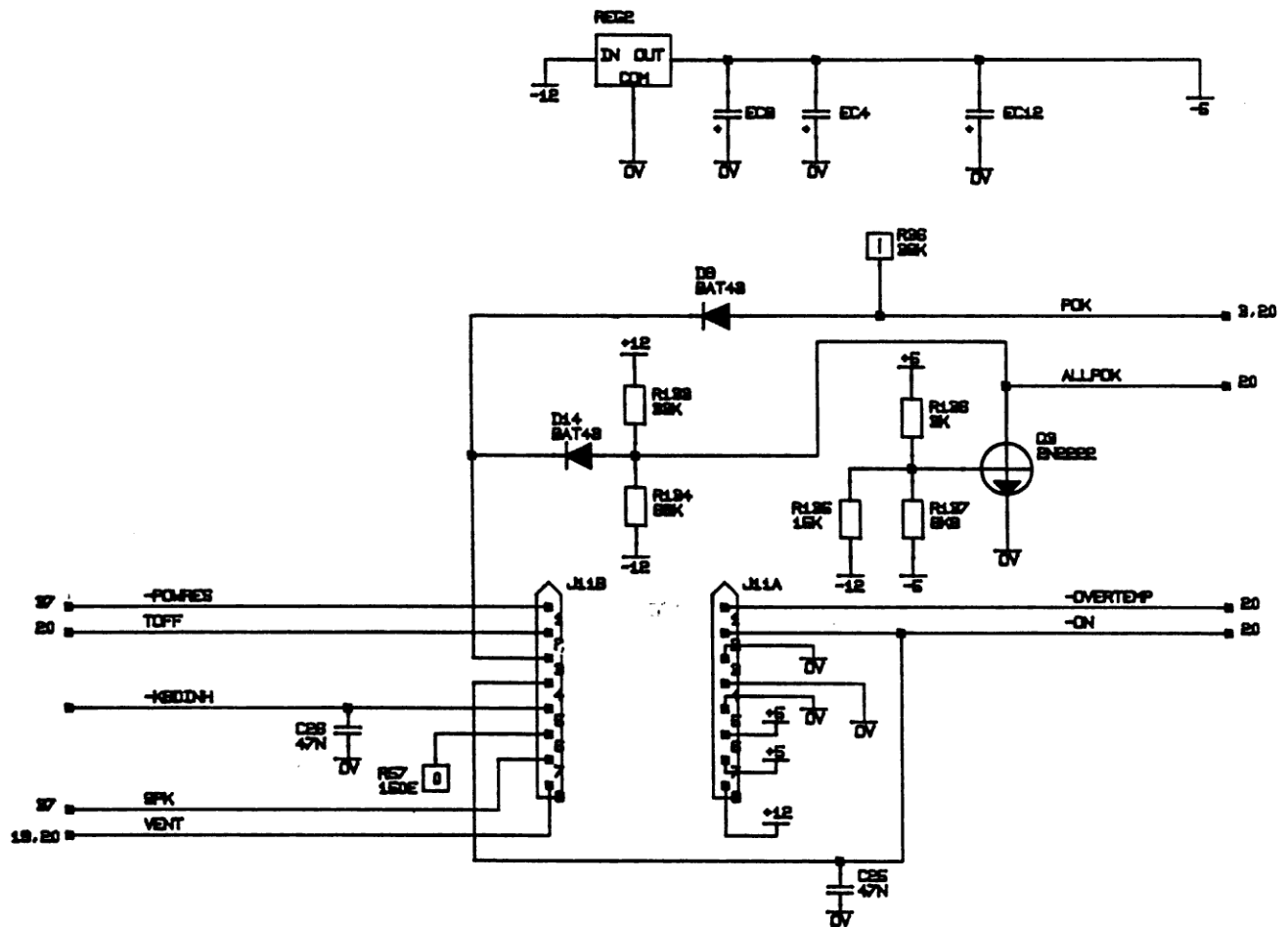


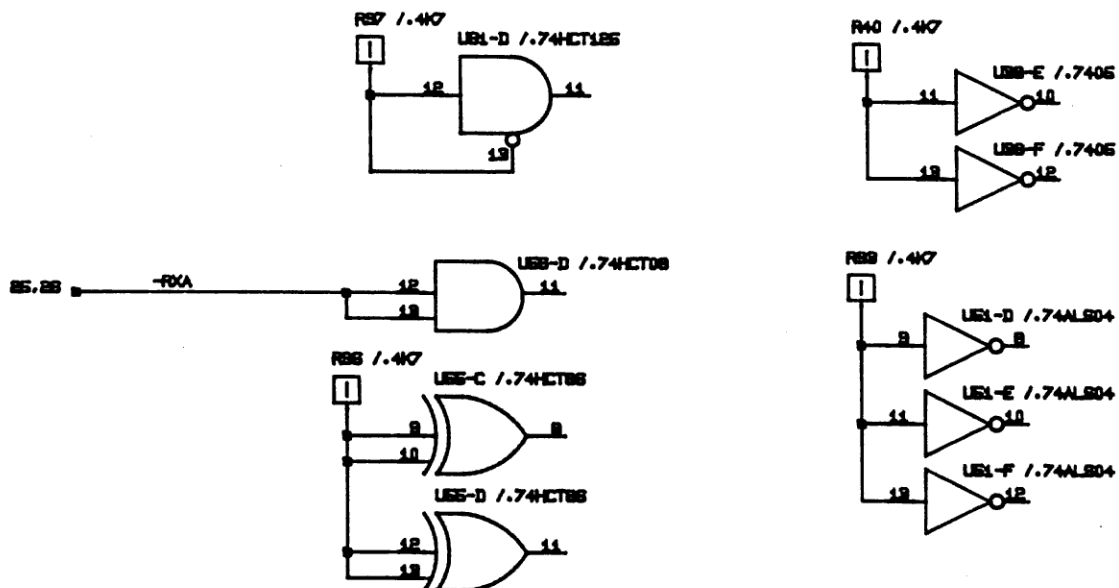
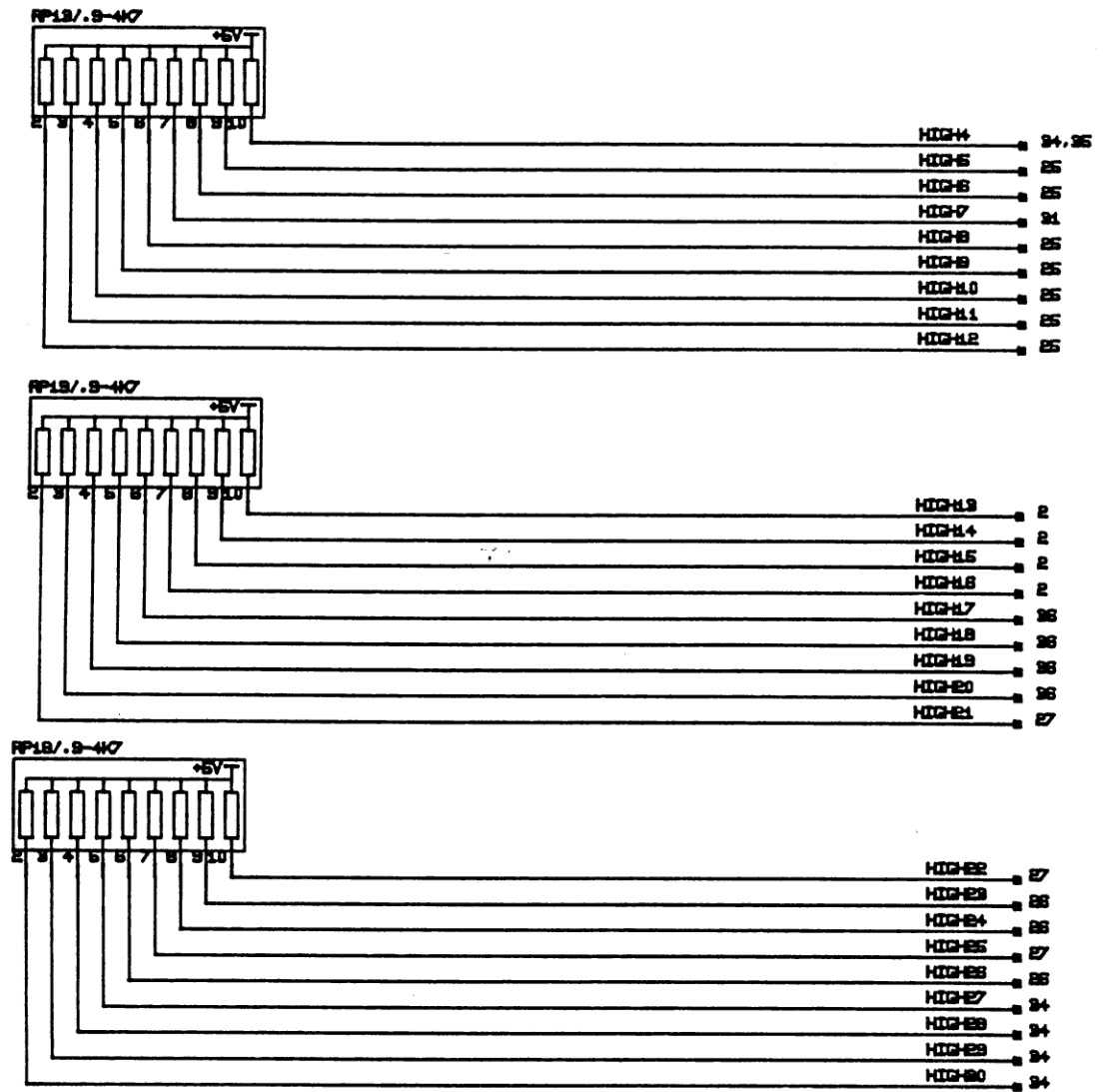




36







3.4 PAL descriptions

Below descriptions for the following PAL's are given:

- * PAT257 Glue-PAL for i80387
- * PAT330 Adaptor for i80387
- * PAT118 Address decoder for WD37C65

CPU452 System Board

Module pal387

Title 'Glue-PAL for i80387 with AT -compability

Author: Peter Koch Andersson

Edition: 25/4-1988

Revision: 5

A/S Regnecentralen.'

PAT257 device 'P16L8';

EMPTY	pin 14;	" 0	true after first 386-busaccess if no i387 is mounted
!ID	pin 12;	" 0	indicates the presence of i387 to the CPU
RESET	pin 1;	" I	common reset for i387 and i386
!ADS	pin 2;	" I	Address Strobe from the CPU
!COERR	pin 3;	" I	-ERROR output from i387
IR13	pin 19;	" 0	Interrupt Request
!IRinh	pin 13;	" X	inhibition of IR13
!BUSY	pin 17;	" I/O	i387 busy
!BUSYen	pin 15;	" X	internal Busy enable
PEREQ	pin 18;	" I/O	i387 data request
STEN	pin 16;	" 0	Status ENable, disables i387- drivers when low.
!CS287	pin 6;	" I	low when IO add. 0E0-0FFH is accessed.
!INTA	pin 4;	" I	INTerrupt Acknowledge
!XIOW	pin 5;	" I	Xbus IO Write
!REF	pin 7;	" I	memory REFresh
!LMEGCS	pin 9;	" I	Low, if A(20:31)=0
!CPUTST	pin 8;	" I	Active around the trailing edge of RESET to enable 80386 selftest re- quest.

Equations

```

!EMPTY = (COERR & ADS & !RESET) $ (!EMPTY & !RESET);

ID      = COERR & EMPTY;

IRinh   = RESET
$ IRinh & EMPTY & !ADS
$ IRinh & COERR
$ !EMPTY & LMEGCS & CS287 & XIOW & !INTA;

!STEN   = COERR & BUSY & !IRinh & !EMPTY
$ !STEN & BUSYen & !EMPTY
$ CPUTST;

!IR13   = STEN $ EMPTY;

!PEREQ  = EMPTY;
enable PEREQ = !STEN;

BUSYen  = COERR & BUSY & !IRinh
$ EMPTY & !COERR
$ BUSYen & !IRinh
$ CPUTST;

BUSY    = !EMPTY $ (REF & !IRinh) $ CPUTST;
enable BUSY = BUSYen;

```

Title 'Adaptor for i80387 to C&T 386-chipset
 Author: Peter Koch Andersson
 Edition: 14/9-1987
 Revision:1
 A/S Regnecentralen.'

PAT330 device 'P16R6';

" The adaptor-pal has two missions:
 "
 " 1: To insert one waitstate in nonpipelined
 " 387-buscycles to ensure fastest transition
 " to pipelining (The C&T-chipset requires so).
 " 2: To generate AF32 when buscycles are for 387.
 " (AF32 indicates a local buscycle).

RESET pin 9; " I common i387 and i386 reset
 !ADS pin 5; " I Address Strobe from the CPU
 !RDYO pin 2; " I Low,when 80387 is ready for new
 " buscycl.
 !NPS1 pin 3; " I Num.processor select.
 NPS2 pin 4; " I Num.processor select.
 !RDY pin 12; " I/O Tristate connection to !Ready.
 !AF32 pin 19; " O Tristate connection to !AF32 on
 " the systemboard.
 SCLK pin 14; " Phase counter synchronous with
 " Systemclk.
 !IDLE pin 15; " Active when the 386bus is idle.
 !NPS pin 16; " Active when the NP is selected
 " until rdy is active.
 !NPD pin 17; " Active one SCLK after the activation
 " of NPS, until RDY inactive.
 !RDYFF pin 18; " Used to gate RDY out.
 !AFG pin 13; " Delayed NPD.
 true = 1;
 false = 0;

Equations

!SCLK :=SCLK & !RESET;

IDLE :=RDY & !ADS & SCLK
 \$ IDLE & !ADS
 \$ IDLE & !SCLK
 \$ RESET;

NPS :=NPS1 & NPS2 & ADS & IDLE & SCLK
 \$ NPS1 & NPS2 & ADS & RDY & SCLK
 \$ NPS & !RDYFF
 \$ NPS & !NPD;

NPD :=NPS & SCLK
 \$ NPD & NPS;

enable AF32 = NPS & !AFG;
 AF32 = NPS;

enable RDY = RDYFF & NPD;
 RDY = RDYFF;

RDYFF :=NPD & SCLK
 \$ NPD & RDYFF;

AFG :=NPD & NPS;

End

CPU452 System Board

MODULE PT118

TITLE 'CPU 451 ADDR DEKODER FOR WD37C65,
JPJ , Regnecentralen A/S,Ballerup'

PAT118 DEVICE 'P16L8' ;

nfdc1cs, nfdc2cs PIN 1,2 ;
nior, niow PIN 3,4 ;
sa0,sa1,sa2 PIN 5,6,7 ;
ndchng,ndack2,tc PIN 8,9,11 ;
dacktc,sd7 PIN 12,13 ;
dmaen,nwrwr PIN 14,19 ;
nldor,nldcr PIN 16,15 ;
nfdcs,nfdccs PIN 18,17 ;

H,L,X,C,Z = 1,0,.x.,.c.,.z.;

input = !nfdc1cs,nfdc2cs,sa2,sa1,sa0,
nior,niow,dmaen,ndchng,ndack2,tc!;
output = !nfdcs,nfdccs,nldor,nldcr,nwrwr,dacktc,sd7 ! ;

EQUATIONS

ENABLE nfdcs = H;
ENABLE nfdccs = H;
ENABLE nldor = H;
ENABLE nldcr = H;
ENABLE dmaen = L;
ENABLE nwrwr = H;
ENABLE dacktc = H;
ENABLE sd7 = !nldcr & !nior ;

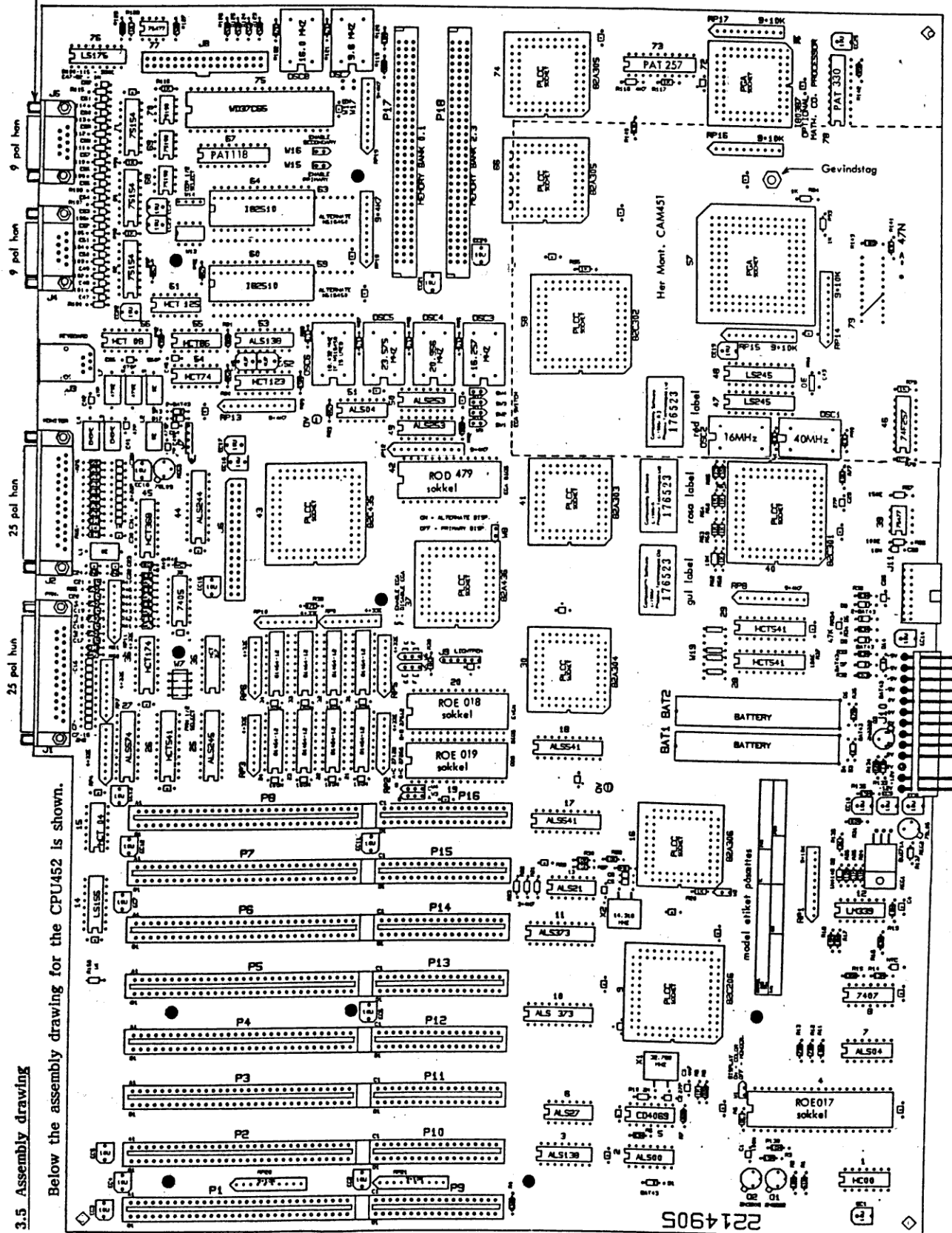
sd7 = !ndchng ;
!nfdcs = (!nfdc1cs \$!nfdc2cs) & sa2 & !sa1 ;
!nfdccs = !nfdc1cs & !sa2 & sa1 & !sa0
\$!nfdc2cs & !sa2 & sa1 & !sa0
\$!nfdc1cs & sa2 & !sa1
\$!nfdc2cs & sa2 & !sa1
\$!nfdc1cs & sa2 & sa1 & sa0 & !niow
\$!nfdc2cs & sa2 & sa1 & sa0 & !niow
\$!ndack2 & dmaen ;
!nldcr = (!nfdc1cs \$!nfdc2cs) & sa2 & sa1 & sa0 ;
!nldor = (!nfdc1cs \$!nfdc2cs) & !sa2 & sa1 & !sa0 ;
!nwrwr = (!nfdc1cs \$!nfdc2cs) & !sa2 & sa1 & !sa0 & !niow;
dacktc = tc & !ndack2 ;

test_vectors in PAT118

```
(Enfdclcs,nfdc2cs,nior,niow,sa0,sa1,sa2,
ndchnng,ndack2,tc,sd7,dmaenA ->
Edacktc,sd7,dmaen,nldcr,nldor,nfdccs,nfdcs,nwrora)
Æ1,1,0,1,0,0,1,0,1,1,1,0A -> Æ.X.,.X.,.X.,.X.,.X.,1,.X.,.X.A;
Æ1,1,0,1,0,0,1,0,1,1,1,0A -> Æ.X.,.X.,.X.,.X.,.X.,.X.,1,.X.A;
Æ1,1,0,1,0,0,1,0,1,1,1,0A -> Æ.X.,.X.,.X.,.X.,.X.,.X.,1,.X.A;
Æ1,1,0,1,0,0,1,0,1,1,1,0A -> Æ.X.,.X.,.X.,.X.,.X.,1,.X.,.X.A;
Æ0,1,1,0,1,0,1,1,0,0,0,0A -> Æ.X.,.X.,.X.,.X.,.X.,0,.X.,.X.A;
Æ1,0,1,0,0,1,0,1,0,0,0,0A -> Æ.X.,.X.,.X.,.X.,.X.,0,.X.,.X.A;
Æ1,1,1,0,1,1,1,1,0,0,0,0A -> Æ0,.X.,.X.,1,.X.,1,.X.,.X.A;
Æ0,1,0,0,0,1,0,1,1,1,0,1A -> Æ.X.,.X.,.X.,.X.,.X.,.X.,.X.,0A;
Æ0,1,0,0,0,1,0,1,1,1,0,1A -> Æ.X.,.X.,.X.,.X.,.X.,0,.X.,.X.A;
Æ0,1,0,0,0,1,0,1,1,1,0,1A -> Æ.X.,.X.,.X.,.X.,0,.X.,.X.,.X.A;
Æ0,1,0,0,1,1,1,1,1,0,1A -> Æ.X.,0,.X.,.X.,.X.,.X.,.X.,.X.A;
Æ0,1,0,0,1,1,1,1,1,0,1A -> Æ.X.,.X.,.X.,0,.X.,.X.,.X.,.X.A;
Æ0,1,1,0,1,0,1,1,1,0,0,1A -> Æ.X.,.X.,.X.,.X.,.X.,.X.,0,.X.A;
Æ0,0,1,0,0,0,0,1,1,0,0,1A -> Æ.X.,.X.,.X.,.X.,.X.,1,.X.,.X.A;
Æ1,0,1,0,1,0,1,1,1,0,0,1A -> Æ.X.,.X.,.X.,.X.,.X.,0,.X.,.X.A;
Æ0,1,1,0,1,1,1,1,1,0,0,1A -> Æ.X.,.X.,.X.,.X.,.X.,0,.X.,.X.A;
Æ1,0,1,0,1,1,1,1,1,0,0,1A -> Æ.X.,.X.,.X.,.X.,.X.,0,.X.,.X.A;
Æ0,0,1,1,1,1,1,1,1,0,0,1A -> Æ.X.,.X.,.X.,.X.,.X.,1,.X.,.X.A;
Æ0,0,1,0,1,1,0,1,1,0,0,1A -> Æ.X.,.X.,.X.,.X.,.X.,1,.X.,.X.A;
Æ0,0,0,0,0,1,0,1,1,0,.X.,1A -> Æ.X.,.Z.,.X.,.X.,.X.,.X.,.X.,.X.A;
Æ1,0,0,0,0,1,0,1,0,1,1,1A -> Æ.X.,.X.,.X.,.X.,.X.,.X.,.X.,0A;
Æ1,0,0,0,1,0,1,1,0,1,1,1A -> Æ.X.,.X.,.X.,.X.,.X.,.X.,0,.X.A;
Æ0,0,0,0,0,0,0,1,0,1,1,1A -> Æ.X.,.X.,.X.,.X.,1,0,1,1A;
Æ0,1,0,0,1,0,1,1,0,1,1,1A -> Æ.X.,.X.,.X.,1,.X.,.X.,.X.,.X.A;
Æ1,0,0,0,1,0,1,1,0,1,1,1A -> Æ.X.,.X.,.X.,1,.X.,.X.,.X.,.X.A;
Æ1,0,0,0,0,1,0,1,0,1,1,1A -> Æ.X.,.X.,.X.,.X.,0,.X.,.X.,.X.A;
Æ1,0,0,0,1,1,1,1,0,1,0,1A -> Æ.X.,0,.X.,0,.X.,.X.,.X.,.X.A;
Æ0,0,0,0,1,1,0,1,0,1,1,1A -> Æ.X.,.X.,.X.,1,1,.X.,.X.,1A;
Æ0,0,0,1,0,1,0,1,1,1,1,1A -> Æ0,.X.,.X.,.X.,.X.,.X.,.X.,1A;
Æ1,1,0,0,0,1,0,1,1,0,1,1A -> Æ.X.,.X.,.X.,.X.,1,1,.X.,1A;
Æ0,0,0,0,0,1,1,1,0,1,1,0A -> Æ.X.,.X.,.X.,1,1,1,1,1A;
Æ1,0,1,0,1,1,1,1,0,1,.X.,1A -> Æ.X.,.Z.,.X.,.X.,.X.,.X.,.X.,.X.A;
Æ1,0,0,0,1,1,1,0,0,1,1,1A -> Æ1,1,.X.,.X.,.X.,.X.,.X.,.X.A;
```

END PT118

Below the assembly drawing for the CPU452 is shown.



Alle skruest filteres med 2 flader pløse med printer.

W7, W13: 8 pins sokkel.
W14: 1/2 8 pins sokkel.

I pos. W7 mont. programmerbar dip shunt.
I pos. W13 mont. dipswitch 2 x 2 on / off.

W17, W18 mont. ikke.

I pos. W19 mont. 4 stk. 1K modstande.

I pos. R137 mont. 5K6.

Kredse i PLCC sokkel mont. efter IN CIRCUIT TEST.

BAT1, BAT2,

X1, X2, REG1 fastgøres med dobb. sided tape.

Gevindring for CAM451 mont. i glideboks.

I stk. lus mont. mellem 79 - 5 og 79 - 19.

Modification:

C5 = 47pF

C6 = 47pF

Kontakt stift fjernes på etiket inden mont.

FINISH / BETYDELSE

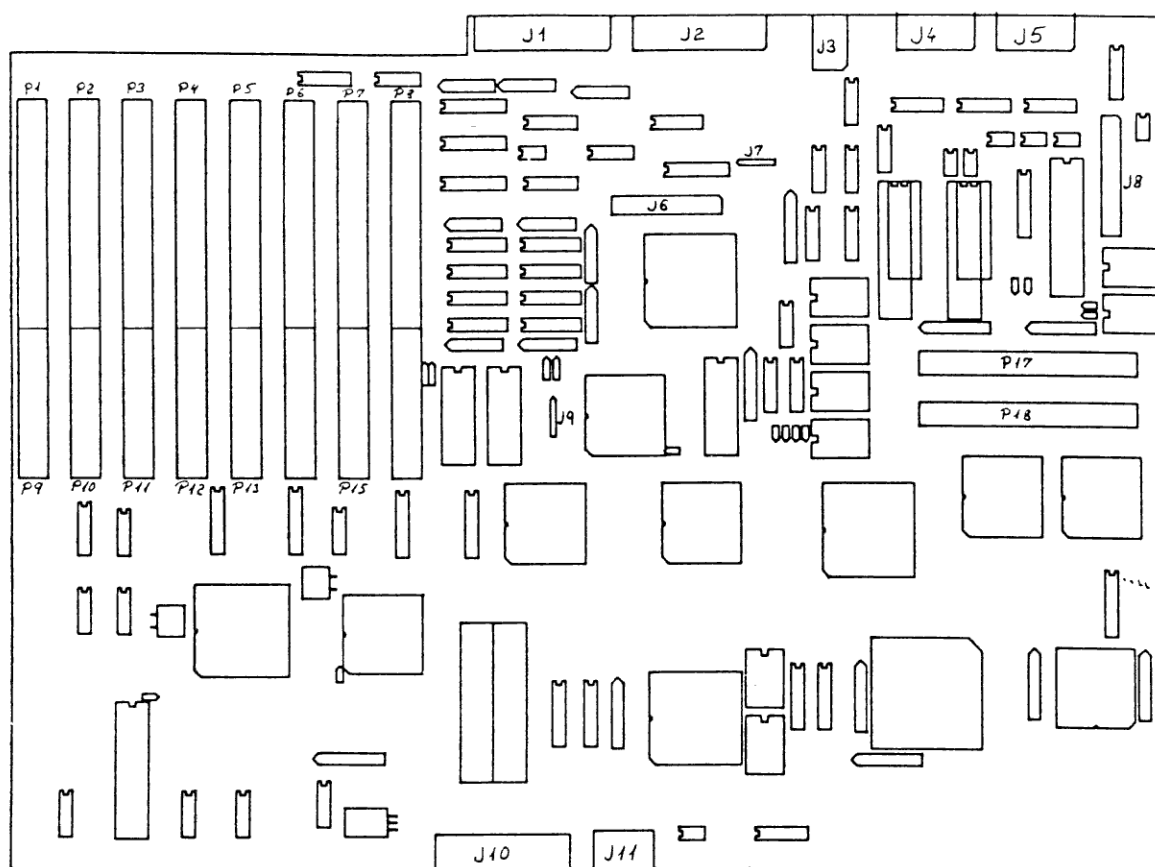
CPU452
Montage tegning

Regnecentralen as

DATE / SIGN
880920HC

TECH. NR.
76219190

3.6 Connectors



Board layout showing the connectors on CPU452.

The system board has the following connectors:

Parallel printer connector	(J1)
Monitor connector	(J2)
Keyboard connector	(J3)
Serial communications connector COM1	(J4)
Serial communications connector COM2	(J5)
Feature connector	(J6)
Video connector	(J7)
Floppy drive connector	(J8)
Lightpen connector	(J9)
Power-supply connector	(J10)
System control connector	(J11)
I/O expansion slots	(P1 -P16)
Memory bank 0,1 connector	(P17)
Memory bank 2,3 connector	(P18)

CPU452 System Board

The Pin assignments for the Parallel printer connector are as follows:

Pin	Function	Pin	Function
1	-STROBE	14	-AUTOFDXT
2	DATA0	15	-ERROR
3	DATA1	16	-INIT
4	DATA2	17	-SELECTIN
5	DATA3	18	0 Volt
6	DATA4	19	0 Volt
7	DATA5	20	0 Volt
8	DATA6	21	0 Volt
9	DATA7	22	0 Volt
10	-ACK	23	0 Volt
11	BUSY	24	0 Volt
12	PE	25	0 Volt
13	SELECT		

Parallel printer connector

The Pin assignments for the Monitor connector (J2) are as follows:

Pin	Function	Pin	Function
1	0 Volt	14	Red
2	0 Volt	15	Red Secondary
3	0 Volt	16	Green
4	0 Volt	17	Green Secondary
5	0 Volt	18	Blue
6	0 Volt	19	Blue Secondary
7	0 Volt	20	HSYNC
8	0 Volt	21	VSNC
9	0 Volt	22	0 Volt
10	RxD (mouse)	23	N60Hz
11	Not connected	24	KeyBoardPWR
12	KeyBoardDATA	25	KeyBoardCLK
13	0 Volt		

Monitor connector

The Pin assignments for the Keyboard connector (J3) are as follows:

Pin	Function
1	Keyboard Power (+9V)
2	Not Connected
3	Not Connected
4	Keyboard return
5	Keyboard Data
6	Keyboard Clock

Keyboard connector

The Pin assignments for the Serial communications connectors (J4 and J5) are as follows:

Pin	Function
1	Carrier Detect
2	Received Data
3	Transmitted Data
4	Data Terminal Ready
5	Ground
6	Data Set Ready
7	Request To Send
8	Clear To Send
9	Ringing Indicator

Serial communications connectors

The Pin assignments for the Feature connector (J6) are as follows:

Pin	Function	Pin	Function
1	0 Volt	2	-12 Volt
3	+12 Volt	4	J7 pin 4
5	J7 pin 3	6	GSOUT
7	RSOUT	8	BSOUT
9	ATRSL	10	BOUT
11	GOUT	12	G
13	RS	14	B
15	R	16	ROUT
17	FEAT1	18	BLANK
19	FEAT0	20	FC1
21	FC0	22	GS/I
23	BS/V	24	HIN
25	VIN	26	14.318 MHz
27	NINTERNL	28	EXTOSC
29	VOUT	30	HOUT
31	0 Volt	32	+5 Volt

Feature connector

The Pin assignments for the Video connector (J7) are as follows:

Pin	Function
1	0 Volt
2	J6 pin 4
3	J6 pin 5
4	0 Volt
5	Reserved
6	Reserved

Video connector

CPU452 System Board

The Pin assignments for the Floppy Drive connector (J8) are as follows:

Pin	Function	Pin	Function
1	0 Volt	2	RMM/RWC
3	speedsel	4	
5	0 Volt	6	
7	0 Volt	8	IDX
9	0 Volt	10	M01
11	0 Volt	12	DS2
13	0 Volt	14	DS1
15	0 Volt	16	M02
17	0 Volt	18	DIRC
19	0 Volt	20	STEP
21	0 Volt	22	WD
23	0 Volt	24	WE
25	0 Volt	26	TROO
27	0 Volt	28	WP
29	0 Volt	30	RDD
31	0 Volt	32	HS
33	0 Volt	34	-DCHNG

Floppy Drive connector

The Pin assignments for the Lightpen connector (J9) are as follows:

Pin	Function
1	-LPENIN
2	Not connected
3	-LPENSW
4	0 Volt
5	+5 Volt
6	+12 Volt

Lightpen connector

The Pin assignments for the Power-supply connector (J10) are as follows:

Pin	Function
1	-12 volt
2	+12 volt
3	Key
4-9	Ground
10-13	+5 volt

Power-supply connector

The Pin assignments for the System control connector (J11) are as follows:

Pin	Function	Pin	Function
1A	-OVERTEMP	1B	-POWRESet
2A	-ON	2B	TurnOFF
3A	0 Volt	3B	Power OK
4A	-ON return	4B	-ON
5A	-KBDINH return	5B	-KBDINH
6A	+5V (LED pwr)	6B	LED pwr return
7A	+5V (SPKR pwr)	7B	SPK
8A	+12V(Vent pwr)	8B	VENT

System control connector

CPU452 System Board

The Pin assignments for the I/O expansion connectors (P1 through P16) are as follows:

Pin	Function	Pin	Function
1A	-IOCHK	1B	0 Volt
2A	SD7	2B	RDRV
3A	SD6	3B	+5 Volt
4A	SD5	4B	IRQ9
5A	SD4	5B	-5 Volt
6A	SD3	6B	DRQ2
7A	SD2	7B	-12 Volt
8A	SD1	8B	-OWS
9A	SD0	9B	+12 Volt
10A	IOCHRDY	10B	0 Volt
11A	AEN	11B	-SMEMW
12A	SA19	12B	-SMEMR
13A	SA18	13B	-IOW
14A	SA17	14B	-IOR
15A	SA16	15B	-DACK3
16A	SA15	16B	DRQ3
17A	SA14	17B	-DACK1
18A	SA13	18B	DRQ1
19A	SA12	19B	-REF
20A	SA11	20B	SYSCLK
21A	SA10	21B	IRQ7
22A	SA9	22B	IRQ6
23A	SA8	23B	IRQ5
24A	SA7	24B	IRQ4
25A	SA6	25B	IRQ3
26A	SA5	26B	-DACK2
27A	SA4	27B	TC
28A	SA3	28B	BALE
29A	SA2	29B	+5 Volt
30A	SA1	30B	OSC
31A	SA0	31B	0 Volt

I/O expansion (PCbus-) connectors (P1 - P8)

Pin	Function	Pin	Function
1C	-SBHE	1D	-MCS16
2C	SA23	2D	-IOCS16
3C	SA22	3D	IRQ10
4C	SA21	4D	IRQ11
5C	SA20	5D	IRQ12
6C	SA19	6D	IRQ15
7C	SA18	7D	IRQ14
8C	SA17	8D	-DACK0
9C	-MEMR	9D	DRQ0
10C	-MEMW	10D	-DACK5
11C	SD8	11D	DRQ5
12C	SD9	12D	-DACK6
13C	SD10	13D	DRQ6
14C	SD11	14D	-DACK7
15C	SD12	15D	DRQ7
16C	SD13	16D	+5 Volt
17C	SD14	17D	-MASTER
18C	SD15	18D	0 Volt

I/O expansion (ATbus-) connectors (P9 - P16)

The Pin assignments for the Memory connectors (P17,P18) are as follows:

Pin	Function	Pin	Function	Pin	Function P17/P18
1A	MD1	1B	+5 Volt	1C	MD0
2A	MD2	2B	+5 Volt	2C	MP0
3A	MD3	3B	0 Volt	3C	MP1
4A	MD4	4B	0 Volt	4C	MP2
5A	MD5	5B	0 Volt	5C	MP3
6A	MD6	6B	0 Volt	6C	-LBE0
7A	MD7	7B	0 Volt	7C	-LBE1
8A	MD8	8B	0 Volt	8C	-LBE2
9A	MD9	9B	0 Volt	9C	-LBE3
10A	MD10	10B	0 Volt	10C	-2MB0/-2MB1
11A	MD11	11B	0 Volt	11C	-8MB0/-8MB1
12A	MD12	12B	0 Volt	12C	Reserved
13A	MD13	13B	0 Volt	13C	40NS0/40NS1
14A	MD14	14B	0 Volt	14C	20NS0/20NS1
15A	MD15	15B	0 Volt	15C	-DWE
16A	MD16	16B	0 Volt	16C	-RAS0/-RAS2
17A	MD17	17B	0 Volt	17C	-RAS1/-RAS3
18A	MD18	18B	0 Volt	18C	-CAS0/-CAS2
19A	MD19	19B	0 Volt	19C	-CAS1/-CAS3
20A	MD20	20B	0 Volt	20C	XDA0
21A	MD21	21B	0 Volt	21C	XDA1
22A	MD22	22B	0 Volt	22C	XDA2
23A	MD23	23B	0 Volt	23C	XDA3
24A	MD24	24B	0 Volt	24C	XDA4
25A	MD25	25B	0 Volt	25C	XDA5
26A	MD26	26B	0 Volt	26C	XDA6
27A	MD27	27B	0 Volt	27C	XDA7
28A	MD28	28B	0 Volt	28C	DA8
29A	MD29	29B	0 Volt	29C	DA9
30A	MD30	30B	0 Volt	30C	-ENRASA
31A	MD31	31B	+5 Volt	31C	-DISRASA
32A	Reserved	32B	+5 Volt	32C	Reserved

Memory connectors

CPU452 System Board

References:

- A: Intel 80386.
- B: Intel 80387.
- C: Chips & Technologies CS8230: AT/386 CHIPSet.
- D: Chips & Technologies 82C206 Integrated Peripherals controller.
- E: Chips & Technologies 82C435 Enhanced Graphics Controller 82A436 Bus Interface.
- F: Western Digital WD37C65.
- G: CAM451 Cache Memory Hardware Reference Manual
Regnecentralen a-s.

Appendix A. Differences between CPU451 and CPU452

CPU451 and CPU452 are based on the same Printed Circuit Board. Only a few components are changed to enhance the performance:

- pos 57 The 80386 is removed from its socket. A 20MHz version is used instead and is installed in the CAM451, that is plugged into the PGA socket instead.
Three unused pins in the socket are used for CAM451 purposes:
 - a) Pin B6 is connected to pin 4 (A20) of pos. 46.
 - b) Pin C6 is connected to pin 66 (-DWE) of pos. 58.
 - c) Pin C7 is connected to pin 1 (A20GATE) of pos 46.
- pos 40, 58, 66, 74
The 82C301, 82C302, and the two 82A305 are changed to 20MHz versions.
- pos 78 PAT330 is changed from a 'B' (PAT190) version to the faster 'D' version.
- pos 79 PAT193 is removed completely and a strap from its former pin 5 to pin 19 is inserted instead.
- pos OSC1 The oscillator is changed from 32MHz to 40MHz.
This X-tal is used as the source for the system clock.
- pos OSC2 The oscillator is changed from 12MHz to 16MHz.
This X-tal is used as the clock source for the AT-state machine.
- pos 28 The version number set at pins 6-9 is changed from 1 to 2. I.e. pins 6,8,9 are tied low and pin 7 is tied high through resistors in the selection area W19.

Finally new BIOS ROM's (pos 19 and pos 20 - ROE019 and ROE18) are installed, that include new POST code for initializing the CPU452. These BIOS' however are backward compatible and may be used also in CPU451.