RC900

CPU451B System Board

Hardware reference manual

PN: 99111392

RC Computer

Keywords:
CPU451B, RC900 System Board

Abstract:
This paper contains a description of the deviations from CPU451 systemboard. For the description of CPU451 please refer to "CPU451 System Board Hardware reference manual" PN:99111109.

Date:
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Author:
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1. Generel Information

The primary purpose with CPU451B is to incorporate the detected errors (Field Change Orders) on the printed circuit board.

To ease the fabrication and trouble shooting, some new test facilities are introduced as compared with CPU451.

A version number is readabel for the BIOS to decide what tests may be done.

2. List of corrected errors.

1.	FCO 23-002	ROD479(EGA BIOS).
2.	FCO 23-004	"No timer tick interrupt".
3.	FCO 23-005A	Dip switch in W13 and W14.
4.	FCO 23-008	Mechanical support in lower left corner.
5.	FCO 23-010	Wrong tantalum capacitors.
6.	FCO 23-019	Missing pullup on IOChck.
7.	FCO 23-020	ROE017(KBD controller).
8.	FCO 23-023A	ROE018,ROE019(BIOS).

3. Description of new functionality.

3.1 CPU selftest.

The 80386 has an on-chip selftest facility which may be activated by having BUSY active at the trailing edge of RESET. This is done by PAT257 on command from the KBD controller.

After the test, the CPU has an error syndrome in the CE register. If the syndrome equals zero, no errors have been detected.

3.2 Voltage control.

Bit 0 in IO read register 26H is 1 only if all voltages (+5V, +12V, -12V and -5V) are on or beyond their nominal values.

In CPU451B bits (4,5,6,7) in this register are strapped to (1,0,0,0).

Reference: CPU451 System Board Hardware reference manual.
PN: 99111109

RC900

CPU451 System Board

Hardware reference manual

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RC Computer

Keywords:
CPU451, RC900 System Board

Abstract:
This paper contains a hardware description of the CPU451 sytem board. The CPU451 provides 80386 CPU, memory control, AT bus, keyboard control, BIOS ROMS, EGA, Printer, Seriel I/O and Floppy control.

Date:
March 1988

Author:
Peter Koch Anderson

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1. GENERAL INFORMATION

1.1 Introduction

The CPU451 is a 16MHz intel80386 based PC/AT compatibel processorboard.

The board provides:

* 16MHz i80386 CPU
* slots for up to 16Mbytes of memory
* onboard Enhanced Graphics Adaptor with 256 Kbytes of pixelmemory
* Floppydisc controller
* 2 serial ports
* parallel printer port
* socket for the i80387 option.

This manual describes the CPU451 board in three major sections. The first section gives a short description and specification of the board. The second section contains a functional description. The third section is devoted to the **detailed** hardware description with circuit- logic- and timing-diagrams.

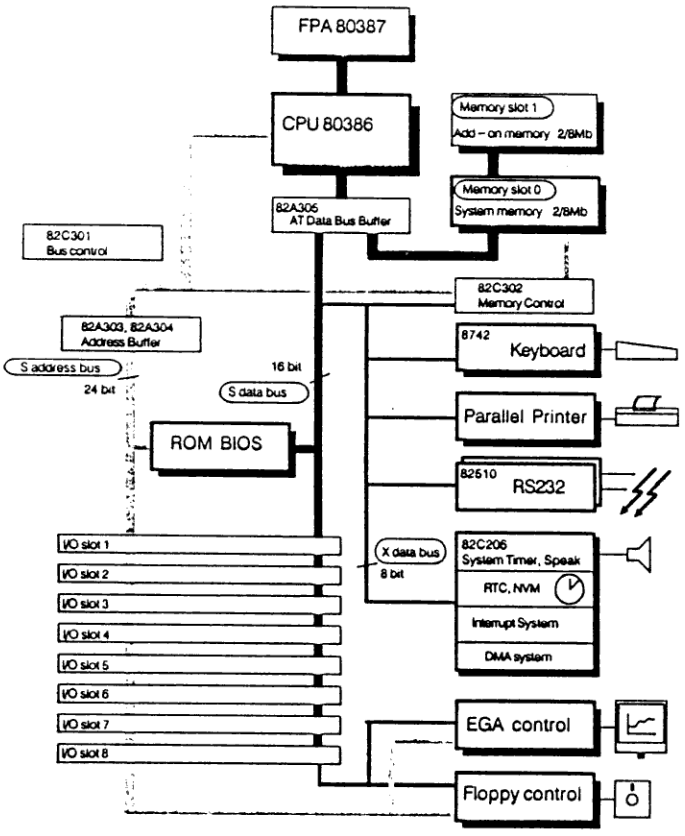


Fig.1 CPU451 Block diagram.

1.2 Short description

The CPU451 basically contains 4 different busses connecting the various elements.

The 32 bit Local bus interconnects the 80386, the 80387 ,the memory controller and the busbuffers.
The 32 bit Memory bus connects the memory to the busbuffers.
The 16 bit System bus connects all I/O including the PC/AT-slotsand the X bus to the busbuffers.
The 8 bit X bus connects systemboard controllers to the Systemboard.

The bussystem is controlled by a so called Chipset being a five chip gatearray system including memory controller, bus controller and bus buffers/latches.

The board provides a broad spectrum of clock frequencies for driving as well the CPU as the Systembus at different speeds as might be required in different compatible applications.

The memory system assumes banked dynamic memory with access times of 100 or 120 nanoseconds and provides 0 or 1 waitstate (16MHz) when hits to interleaved pages are obtained.

Three BIOS PROM's are provided. Two contains the CPU-initialization, the PowerOnSystemTest and the compatible standard Basic I/O System. One contains BIOS for the EGA.

The compatible system controllers:
- two 8259 interrupt ctr's,
- two 8237 DMA ctr's with the 74LS612 addressmapper,
- 8254 timer/counter,
- 146818 Real Time Clock and
- (extended) CMOS RAM

are all integrated in one LSI-chip C&T 82C206.

A compatibel Keyboard controller utilizing a 8742 is, provided. The keyboard interface is connected to both a seperat connector and to some pins in the CRT connector for attachment of the keyboard to the monitor (simplyfing cabling).

Eight completely compatible PC/AT I/O slots are provided.

An Enhanced Graphics Adapter is integrated on two LSI gatearrays C&T 82C435 and 82A436. The EGA is expanded with clock frequencies for driving the 73 Hz RC940. These frequencies are automatically selected, when an RC940 cable is inserted in the monitor connector. In that case a special version of the EGA-BIOS residing in the second half of the EGA-BIOS-ROM is also selected, ensuring an initialization of the EGA corresponding to the RC940. The monitor connector also contains connection for the keyboard and a mouse. A strapping option disables the EGA.

Two compatible Seriel ports are implemented in two i82510's. Each is per straps configurable as not included, first- and second- seriel port. One is connected via a special "polarity-correcting" circuit to the monitor connector for the connection of several types of mouses to the monitor.

A parallel printer port is provided. The port is AT- and (at plug level) Partner- compatible. A strapping option excludes the port or configures it as first- or second- printer port.

A compatible Floppy disc controller is based on Western Digitals WD37C65. The controller may be strapped as first or second or not included.

A battery is mounted on the the board for maintaining power for the RealTimeClock and the Non Volatile cmos Memory.

1.3 Specifications

1.3.1 Performance specifications

80386 CPU clock	: 16 MHz
80387 NPX clock	: 16 MHz
Local bus size	: 32 bits

Memory:

capacity	: 2 slots for insertion of any combination of 2- or 8-Mega byte memory boards.
organization	: 2 banks in each slot divided in pages of 2 or 8 Kbytes depending on the installed memory module.
word length	: 32 bits.
operation	: Page interleaving.
access time	: Page hit : 0 wait states. Page miss: 3 wait states.

ROM BIOS:

capacity	: 32 Kbytes.
wordlength	: 16 bits.
access time	: Depends on the programmed System bus speed.

The BIOS transfers itself to the overlaying memory and is after that accessible with the performance described for memory.

PC/AT bus:

slots	: 8.
bus width	: 8/16 bit.
addressing range	: 16 Mega bytes
transfer speed	: programmable from 0.3 Mbytes/second to 8 Mbytes/second.

EGA:

compatibility	: CGA and EGA compatible.
RC940 support	: 65 Hz CGA and 73 Hz EGA.
memory size	: 256 Kilo bytes.
BIOS size	: 64 Kilo bytes (32Kbytes selected by the monitor cable).
bus size	: 8 bit.

The EGA BIOS is transferred to the overlaying memory and is after that accessible with the performance described for memory.

1.3.2 Environmental Specifications

Operating temperature : 0 to 40 degrees C.

Relative Humidity : 20% to 80% (non condensing).

Altitude : 0 to 6,000 feet.

1.3.3 Physical Specification

Width : 330 mm

Length : 440 mm

Hight : 34 mm

Weight : 1300 gram

1.3.4 Power Specification

Power consumption (CPU451 only)

Dissipation : 15 W max.

Vcc : +5V +/- 5% (2.5A max.)

+12V : +12V +/- 10% (200mA max.)

-12V : -12V +/- 10% (50mA max.)

To this should be added the consumption of installed memory- and IO- boards.

Total power outlet to expansion slots:

Vcc : 10 A max

+12V : 1.0 A max

-12V : 300mA max

-5V : 100mA max

2 FUNCTIONAL DESCRIPTION

In this section, the function of all parts of the CPU451 board is described.

The description comprises the following functional entities:

1. 80386 CPU

2. 80387 NPX

3. Bussystem

4. Memory control

5. BIOS ROMs

6. Integrated Peripherals Controller

   6.1 Interrupt controller
   6.2 Direct Memory Access controller
   6.3 Non Volatile Memory
   6.4 Real Time Clock
   6.5 Timer/counter

7. Keyboard controller

8. Enhanced Graphics Adapter

9. Serial In/Out

10. Parallel Printer Port

11. Floppy controller

2.1 i80386 CPU

The CPU is shown on diagram no. 1.

The 80386 CPU is an advanced, high performance microprocessor with a non multiplexed 32 bit data and adressbus, integrated memory management, memory protection, an extensive instruction set and two modes of operation:

Real address mode,
Protected mode.

The real address mode is entered after power up. The memory addresses are physical addresses in a contiguous array of one mega bytes generated on the address lines BE0 to BE3 and A2 to A19. The addressing mechanism, interrupt handling, are all identical to the Real Address Mode of the 80286. In this mode the processor is setup for Protected mode operation. Protected mode provides access to the entire installed memory, memory management, paging and privilege capabilities of the processor.

Within protected mode, software can perform a task switch to enter into tasks designated as Virtual 8086 Mode tasks. Each such task behaves with 8086 semantics,thus allowing 8086 software (an application program or an entire operating system) to execute. The Virtual 8086 tasks can be isolated and protected from one another and the host 80386 operating system, by the use of paging, and the I/O permission bitmap.

For detailed information on the 80386 please refer to reference A.

The CPU is via the local bus (D0 to D31, BE0 to BE3 and A2 to A31) connected to the 80387 NPU, the 80A305 data buffers, the 80A303 and 80A304 addressbuffers and the 80C301 buscontroller.

The CPU clock (CLK2) is generated by the 80C301 buscontroller from the 32MHz CLK2in clock.

The RESET signal is generated by the 80C301 buscontroller on basis of powerreset and "§RC" from the keyboardcontroller.

The busstatus signals W/§R, D/§C, M/§IO, §ADS and HLDA are monitored by the 80C301 buscontroller, wich on basis of these and the decoded addresses directs the various buffers.

The "NextAddress" input is strapped active, forcing the CPU into pipelining mode when ever possible.

The "BusSize16" input is strapped inactive, ensuring that datatransfers always occur over the widest possible databus.

The READY signal, which is used to insert the nessecary number of waitstates in a datatransfer, is generated by 80C301 or when the NPU is addressed by PAT190 i position 73.

The HOLD signal is controlled by the 80C301 and used to achieve the bus for DMA cycles other masters or memory refresh cycles.

2.2 i80387 NPX

The socket in position 71 is for the i80387 Numerical Processor Extension option. The 80387 is a high-performance NPX that extends the 80386 architecture with floating point, extended integer and BCD data types.

The NPX provides arithmetic instructions for a variety of numeric datatypes. It also executes numerous built-in transcendental functions (e.g. tangent, sine, cosine and log).

The 80387 works the same whether the 80386 is executing in real-address mode or in protected mode. All memory access is handled by the 80386; the 80387 merely operates on instructions and data passed to it by the 80386. Therefore, the 80387 is not sensitive to the processing mode of the 80386.

The presense of an 80387 is indicated to the 80387 just after reset by holding the §ERROR input active until the first busaccess. The §ERROR input is connected to the NPID output on the PAT147 (see the timing diagram in fig.2).

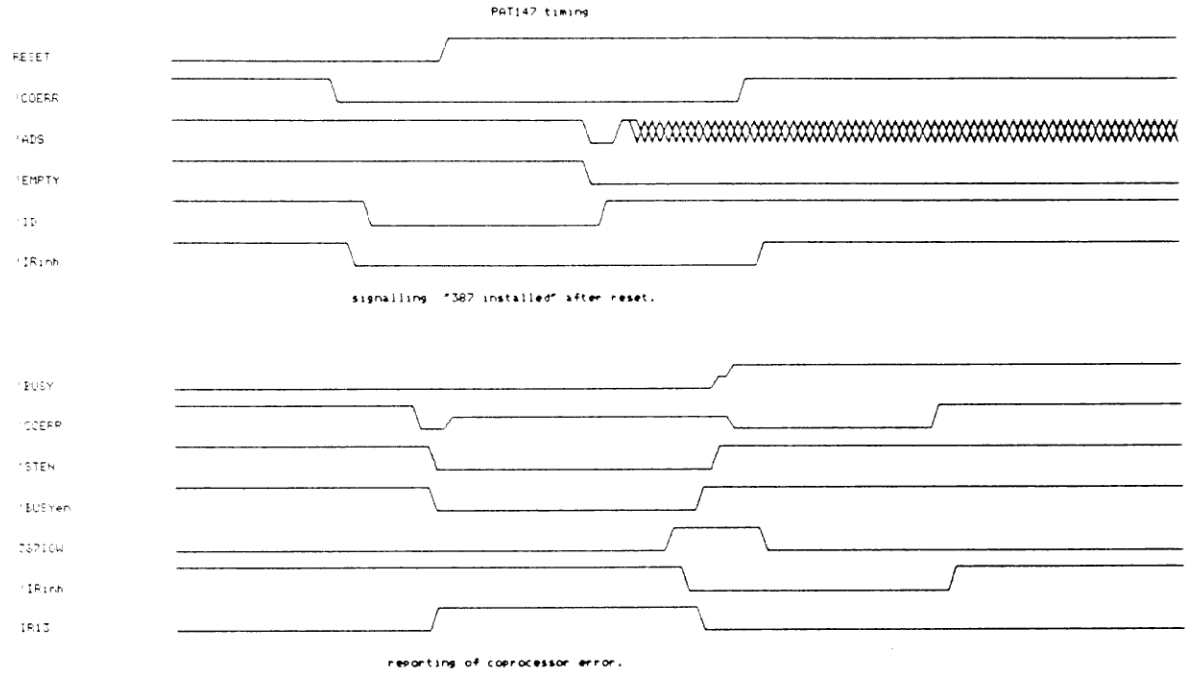


Fig. 2 Compatible NPX interface signalling.

The 80387 is activated by the 80387 via I/O addresses 800000F8h and 800000FCh. As I/O space does not extend beyond 64k, the A31 addressbit together with the M/§IO signal are used to address the 80387. A2 is used to distinguish between opcode- and operand-register. If the NPX has encountered an instruction, which requires parameters or operands, and the NPX is ready for it, it rises the PEREQ signal, which causes the CPU to send or receive data on I/O address 800000FCh. The NPX uses the BUSY signal to indicate to the CPU, that it isnot yet ready to take the next instruction. When executing certain "ESC" instructions (80387 instructions), the 80386 waits for BUSY to be set before it proceeds to the next instruction. Most "ESC" instructions and the "WAIT" instruction are not initiated before the 80387 has dropped BUSY.

When the NPX finds an arithmetic error, this is signalled by setting the §ERROR output from the NPX. This signal logically anded with the BUSY signal is used by the PAT147 to set the IRQ13 flip flop. At the same time the PAT147 clears STEN causing the NPX to disconnect all transmitters, allowing the PAT147 to prolonge the BUSY signal, inhibiting the CPU from executing another NPX-instruction, until the IRQ13 interrupt is serviced. The IRQ13 is cleared by means of an IO write on address E0h to FFh. For the detailed relative timing of this signalling see fig.2.

For detailed information on the 80387 please refer to reference B.

2.3 Bussystem

The CPU451 has a number of data- and address- buses on the board. The buses have different withs and functions and are controlled by the 80C301 buscontroller, and are interconnected via various busbuffers and latches.

Data is transferred via five buses:

The Local bus (D0:D31),
the Memory bus (MD0:MD31),
the System bus (SD0:SD15) (the PC/AT bus),
the X bus (XD0:XD7) and
the B bus (BD0:BD7) (used for the onboard devices).

The three first buses are interconnected via the 80305 bus buffer/latches. Theese gate data from one bus to one or more other buses, and convert between bus withs.

The 80C301 directs the 80A305 by means of a four bit action code plus five other buscontrol signals. This chip also transforms a 32 bit transfer into several 8 or 16 bit transfers if so required.

The data conversion between the System bus and the Local bus / Memory bus depends on the action code in the following way:

AC3:AC0	From	To	
0	D15:D0	SD15:SD0	
1	D15:D8	SD15:SD8,	SD7:SD0
2	D31:D16	SD15:SD0	
3	D31:D24	SD15:SD8,	SD7:SD0
4	D31:D0	SD31:SD0	not used
5	SD7:SD0	D7:D0	
6	SD7:SD0	D15:D8	
7	SD7:SD0	D23:D16	
8	SD7:SD0	D31:D24	
9	SD15:SD0	D15:D0	
A	SD15:SD0	D31:D16	
B	reserved		
C	SD31:SD0	D31:D0	not used
D,E,F	reserved		

The bus connections are controlled in the following way:

cycle type	HLDA1	§ATEN	§MRD	SDIR	§LDEN	from bus	to bus
Local write	0	1	1	x	x	D	MD
Local read	0	1	0	x	x	MD	D
AT write	0	0	x	1	x	D	SD
AT read	0	0	x	0	x	SD	D
DMA write	1	1	1	0	x	SD	MD,D
DMA read	1	1	0	1	x	MD	SD

The X bus and the B bus are eight bit subbusses both connected to SD7:SD0 via 74LS245 "bidi"-buffers.
The X bus attaches the eight bit ports in 80C301, 80C302, 80C206, the 8742 Keyboard controller, the memory ID port and the power control ports.

The B bus attaches the on board serial controllers, parallel printer controller and the Floppydisc controller.

The address lines are grouped in three buses:

```
A2:A31      ; the address part of the Local bus.
SA0:SA23    ; the address part of the System bus.
XA0:XA23    ; the address part of the X bus.
```

These buses are interconnected via the 82A303 and 82A304 address buffers as a function of the buscontrols in the following way:

cycle type	HLDA1	§ATEN	§REF	§MASTER	from bus	to bus
Local	0	1	1	1	A	none
CPU-ATbus	0	0	1	1	A	SA,XA
CPU refresh	0	1	0	1	XA	SA
DMA	1	1	1	1	XA	A,SA
Master	1	1	1	0	SA	A,XA
Master ref.	1	1	0	0	counter	SA

During a Master refresh cycle, the low order address bits SA0:SA11 are derived from a refresh counter in 82A304, whereas SA12:SA23 are forced to zero by the 82A303.

During a DMA cycle the address is generated by the 82C206 and driven onto the XA bus by the 82C206 and one of two 74ALS373's in positions 10 and 11 depending on whether an eight- or sixteen-bit DMA channel is active.

During a Master cycle the "AT-master" (the AT-bus attached peripheral having taken the AT-bus (System bus)), is responsible for driving an address onto the SA bus.

The 82C301 activates the different buscycles on basis of CPU status, addresses and the §AF32, §IOCS8, §IOCS16, §MCS8 and §MCS16 signals.

The §AF32 signal is activated either by the 82C302 memory controller or the PAT190. In the first case, the 82C302 must also generate §READY, when the memory cycle has finished. In the second case a local bus cycle for the 80387 is indicated, and the PAT190 terminates the cycle with §READY.

2.4 MEMORY CONTROL

The memory is not integrated on CPU451 but must be installed in positions JX and/or JY to alow the CPU to initialize.

The memory boards are organized in two banks for interleaved operation. The memory controller 82302 supports interleaving in pagemode in two banks. When using 256KByte RAMs as on the MEM451 board, the pages are 512 words of 32 bits each i.e. 2KBytes, whereas the 1MByte RAMs provided with the MEM452 board give 1024 words of 32 bits i.e. 4KBytes per page.

When an access is made to the same page, to which the former access was made, the access is made in pagemode only requiring CAS to be set. This is about twice as fast as a normal access, where RAS is set following by CAS each signal accompagned by a portion of the address.

When an access is to another page than the current, RAS has to be dropped, a delay (the RAS precharge time) must be inserted, before the RAS-CAS sequence can be entered.

A memoryboard inserted in a memorysocket identifies itself by shorting one of the two signals §2MB or §8MB to GND, these signals plus two speed indicator signals "20nS" and "40nS" exist in two versitions, one per memorysocket. They are pulled up by 10K resistors and fed into a read gate addressed on I/O address 26h. By means of this gate the BIOS may initialize the 82C302 to the actual installed installation. Due to the programmable memory organisation any memory bord may be inserted in any memory slot.

The ident signals are grounded on the memorybords according to the following scheme:

§2MB	§8MB	installed memory
H	H	none
L	H	2MByte
H	L	8MByte
L	L	reserved

20nS	40nS	memory speed
H	H	120 nSec
L	H	100 nSec
H	L	80 nSec
L	L	60 nSec

The ident signals for slot J17 are indexed with a 0 and those for slot J18 with a 1:

slot J17: §2MB0, §8MB0, 20nS0, 40nS0
slot J18: §2MB1, §8MB1, 20nS1, 40nS1

Four RAS signals and four CAS signals for the main memory exist on the CPU451. They are distributed to the memory slots in the following way:

slot	Bank0	Bank1
J17	§RAS0,§CAS0	§RAS1,§CAS1
J18	§RAS2,§CAS2	§RAS3,§CAS3

The CAS signals are gated with the four LachedByteEnable signals §LBE0 to §LBE3 on the memory boards to generate a CAS signal per byte per bank.

The paritybits are generated and checked in the 82A305's and the 82A306. If even parity is detected during a memory read, and parity check is enabled, a NMI is generated.

The 82C302 generates refresh cycles by activating all RAS signals in a staggered fashion to reduce the rate of change in the memory current consumption.

2.5 BIOS ROMS

The BIOS contains bootstrap program, power on system test, initialization and the basic I/O drivers and interrupt handlers.

The BIOS program is developed by PHOENIX TECHNOLOGIES and is located in two 27128 PROMS giving storage to 32KBytes.

The PROMS are situated in positions 19 and 20 with the odd rom module number (RODno.) in pos 19 and the even in pos 20.

The contents are accessed via the 74ALS541 busbuffers in pos. 18 and 19 (see diagram 21) and the Sbus on the addresses E8000 through FFFFF hex, untill the 82302 is reconfigurated to access the main memory on these addresses. This is done by the BIOS when the PROM contends are copied into the same addresses in the main memory obtaining a faster access speed.

Two strapping options (W3 and W4) are located near the PROMs for enabling the possible extension of the PROM capacity:

W3	W4	PROMtype
A	C	27128
B	C	27256
A	D	not used
B	D	27512

2.6 Integrated Peripherals Controller

The 82C206 is a LSI containing the peripherals inherent to an AT architechture:

6.1 Interrupt controller
6.2 Direct Memory Access controller
6.3 Non Volatile Memory
6.4 Real Time Clock
6.5 Timer/counter

Moreover has the chip various registers for programming DMA speed.
For detailed information on the 82C206 please refer to reference D.

2.6.1 Interrupt controller

Integrated on the chip are the equivalent of two cascaded 8259 interrupt controllers. The output of these is connected to the interrupt input of the 80386 CPU. The 16 inputs are disponed in the folloving way:

Controller	channel	Interrupt source
1	IR0	Counter/Timer 0
	IR1	IRQ1 Sbus pin B18
	IR2	Cascade interrupt from controller 2
	IR3	IRQ3 Sbus pin B25, on board SIO
	IR4	IRQ4 Sbus pin B24, on board SIO
	IR5	IRQ5 Sbus pin B23, on board printer
	IR6	IRQ6 Sbus pin B22, on board FD ctr.
	IR7	IRQ7 Sbus pin B21, on board printer
2	IR0	Real time clock
	IR1	IRQ9 Sbus pin B4, on board EGA
	IR2	IRQ10 Sbus pin D3
	IR3	IRQ11 Sbus pin D4
	IR4	IRQ12 Sbus pin D5
	IR5	80387 error
	IR6	IRQ14 Sbus pin D7
	IR7	IRQ15 Sbus pin D6

2.6.2 Direct Memory Access controller

Integrated on the chip are the equivalent of two cascaded 8237A DMA controllers. A DMA request to one of the DMA channels results in a HRQ1 to the 82301 which in turn transforms this into a HOLD request to the 80386. This when releasing the Local bus sets the HLDA signal causing the 82C301 to transmit HLDA1 to the 82C206 which sends DACK on the line corresponding to the requesting line with the highest priority.

If the requested DMA channel is so programmed, and the requesting device wants to gain total control over the bus, this sets the §MASTER signal causing the DMA controller to treestate its address and control drivers.

Otherwise the DMA controller will generate a memory address, the AEN signal and the read and write signals depending on the programmed direction of transfer. After such transfer the address register and bytecount register are incremented by one each.

The two DMA controllers provide four channels each, one of which is used for cascading controller 2 to controller 1.

When addresses are generated by controller 2, they are shifted one (multiplied by 2) before they are applied to the addressbus, resulting in wordwise addressing of the memory. So the channels on controller 1 are used for byte transfers while the channels on controller 2 are used for 16 bit transfers.

Both controllers may be used by busmasters for arbitration.

Controller	channel	n	DRQ(n)	§DACK(n)
DMA1	0	0	D9	D8
	1	1	B18	B17
	2	2	B6	B26
	3	3	B16	B15
DMA2	0	Cascade from DMA1		
	1	5	D11	D10
	2	6	D13	D12
	3	7	D15	D14

2.6.3 Non Volatile Memory

The CMOS NMV which is standard in an AT is integrated on the 82C206 and addressable as described in the technical information from CHIPS.

2.6.4 Real Time Clock

The Real Time Clock integrated in the 82C206 is compatible with Motorola's 146818.

The 32768 Hz clock for this is generated by a specially low power requiring crystal oscillator implemented with a CMOS 14069inverter circuit.

The 82C206 is powered from a circuit which switches to battery supply when the voltage on the 5 volt supply gets too low. This is to retain data in the NVM, and maintain real time.

2.6.5 Timer/counter

The Timer/counter integrated in the 82C206 is compatible with the Intel 8254. The timers are used in the AT compatible style:

timer 0 is connected to IRQ0,
timer 1 controles memory refresh and
timer 2 drives the Speaker.

2.7 Keyboard controller

The keyboard is connected to the CPU451 via an 8742 programmable peripheral, programmed to serve the RC930 keyboard (or any PC/AT keybord if so desired). However neither the plug nor the supply voltage for the keyboard are compatible.
The keyboard is powered through a 9 volt regulator, which serves as currentlimitor.

The KBDCLK and KBDDATA signals found on diagram 19 and 36 are used for both transmission of commands to the keyboard and for reception of data from the keyboard. As receivers are used LM339 comparators to obtain a more well defined treshold voltage at app. 2.5 volts alowing for voltage drop in the ground line.

Two outputs from the 8742 not used for keyboard support are assigned to special functions:

The signal "-RC" will when activated cause reset of the CPU451. This is due to the fact, that the 80286 originally found in AT's is unable to enter real adress mode from protected mode in any ather way.

The signal "A20GATE" ensures when false, that adresses between 100000H and 1FFFFFH wrap around to 0H thru FFFFFH, which is required for PC-compatibility.

2.8 Enhanced Graphics Adapter

The CRT controller incorporated on CPU451 is a "chipset" from Chips & Technology whith the IC's 82C435 and 82A436, and detailled information about theese are found in appendix E. This chipset emulates the standards EGA (Enhanced Graphics Adaptor), the CGA (Colour Graphics Adaptor), the MDA (Monochrome Display Adaptor) and the Hercules.

The CRT controller is drawn on diagrams 30 thru 35, showing the chipset, the CRT refresh memory consisting of eight 64K by 4 DRAMs organised in two banks, bank A on diagram 32 and bank B on 33. Diagram 34 shows the video signal drivers (SN74ALS244 pos 44), the "feature connector" through which both sides of the video signal driver IC as well as the enable signal for this are accessible.

Diagram 34 also shows the Dot frequency selection and the mode selection switches. The signal "N60Hz" is a strap option in the CRT connector (diagram 35) used to select the non AT standard frequency needed for RC940 to produce 75Hz frame frequency.

2.9 Serial In/Out

Diagrams 25 to 29 show the two serial I/O ports implemented on the CPU board using I82510 asyncronous transceivers. The board is prepaired for Natinal Semiconductors 16450 as second source for the Intel parts. Dia.25 shows the xtal oscillator used, which should run 18.432MHz when 82510 is installed and 1.8432MHz if the NS16450 is mounted.

Diagram 25 also shows the mouse polarisation circuit, which automatically detects the representation of the mark and space levels of the received data from the mouse connected via the monitor. The circuit operates as follows: The differentiator implemented in 55-A, 56-C, R92 and C46 detects any level shift in the signal "RXMOUSE" generating a trigger pulse to the retriggerable oneshots 52-A and 52-B. If 20 microseconds elapse between levelshifts, oneshot 52-A resets and clocks the current value of "RXMOUSE" into flipflop 54-A. If still no level shifts are detected for 20 more microseconds, the oneshot 52-B runs out too and clocks the latced value into flipflop 54-B. The output of this is considered the polarity of mark and used to modify "RXMOUSE" by means of 55-B.

If no mouse is connected to the monitor, the output of 55-B is high, assuring that serial port A may be used from J4.

The strapfield shown on dia.22 selects one of two possible I/O addresses and interrupt lines for the serial ports. If no straps are inserted in this position, the ports appear as non existent to the system.

2.10 Parallel Printer Port

Diagrams 23 and 24 show the Parallel Printerport. This is identical to the AT implementation exept for an extra bit introduced in the control signal register controlling the tristate output of the dataregister, making it possible to input parallel data from the port. The printer connection J1 is shown on dia.29.

The strapfield shown on dia.22 selects one of two possible I/O addresses and interrupt lines for the printer port. If no straps are inserted in this position, the port appears as non existent to the system.

2.11 Floppy controller

Diagram 36 shows the floppy controller chip from Western Digital WD37C65 which includes a high resolution digital dataseparator as well as all logic needed for compatible floppy disc control.

A pal (pat118) is added for address decoding, to gate the "DCHG" (Disc changed) signal to the data bus. The PAL also controls the databuffer (74ALS245 pos.25 shown on diagram 22) between the SD bus and the BD bus.

For detailed information on the WD37C65 please refer to reference F.

The straps W15 and W16 on diagram 36 are used to define the Floppy disc controller as primary or secondary controller or to disable it totally. W17 and W18 are not used.

3. TECHNICAL DESCRIPTION

3.1 Introduction

This section gives the detailled description of the CPU451 circuit board until the chip level. For the technical description of the used chips please refer to the manufacturer manuals in the **References.**

3.2 Technical overwiew

Figure 3 and 4 shows a detailled blockdiagram of the CPU451 intended to provide an overwiev of the board. The blocks correspond to physical and or logical entities and are labeled with numbers referring to the logic diagrams in section 3.3, where the exact electrical connections are drawn. Two or more numbers separated with commas indicates that the block is spread over more diagrams.

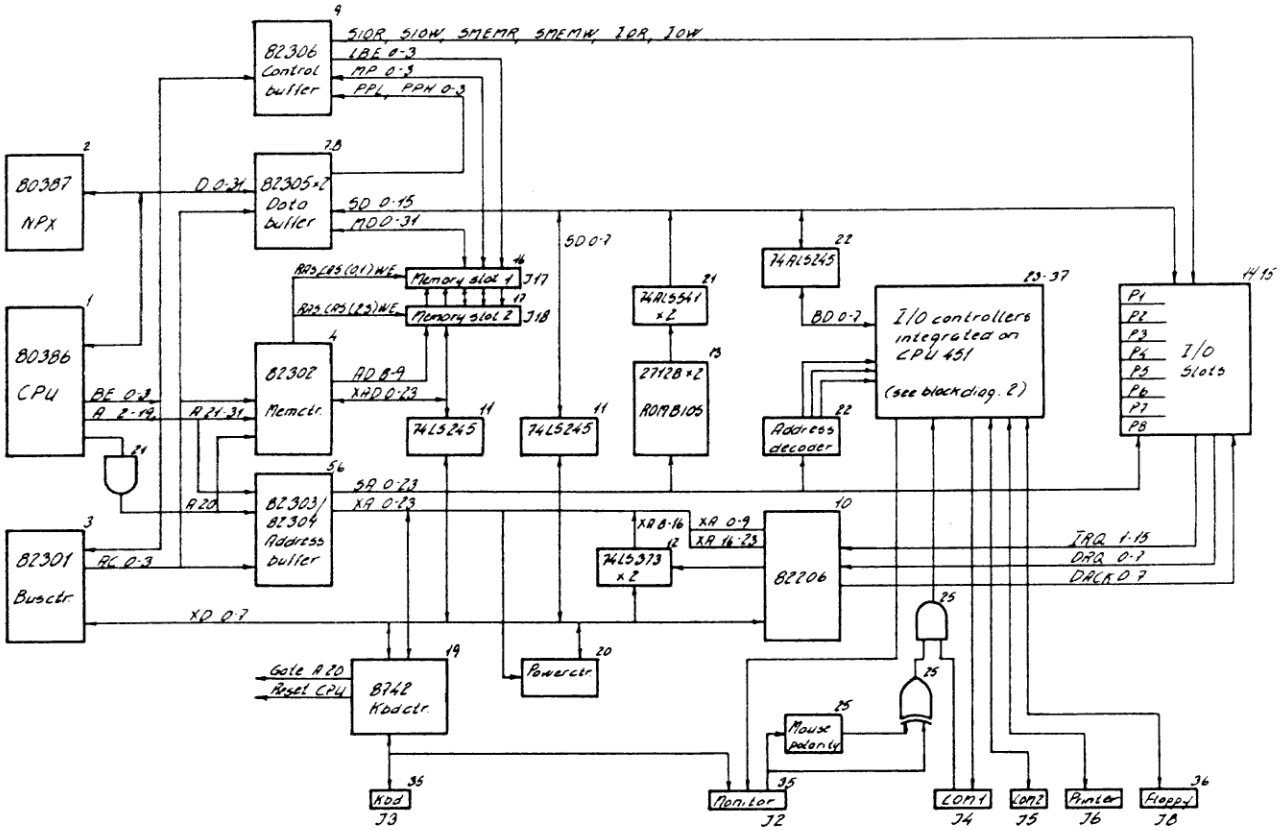


Fig. 3 detailled block diagram.

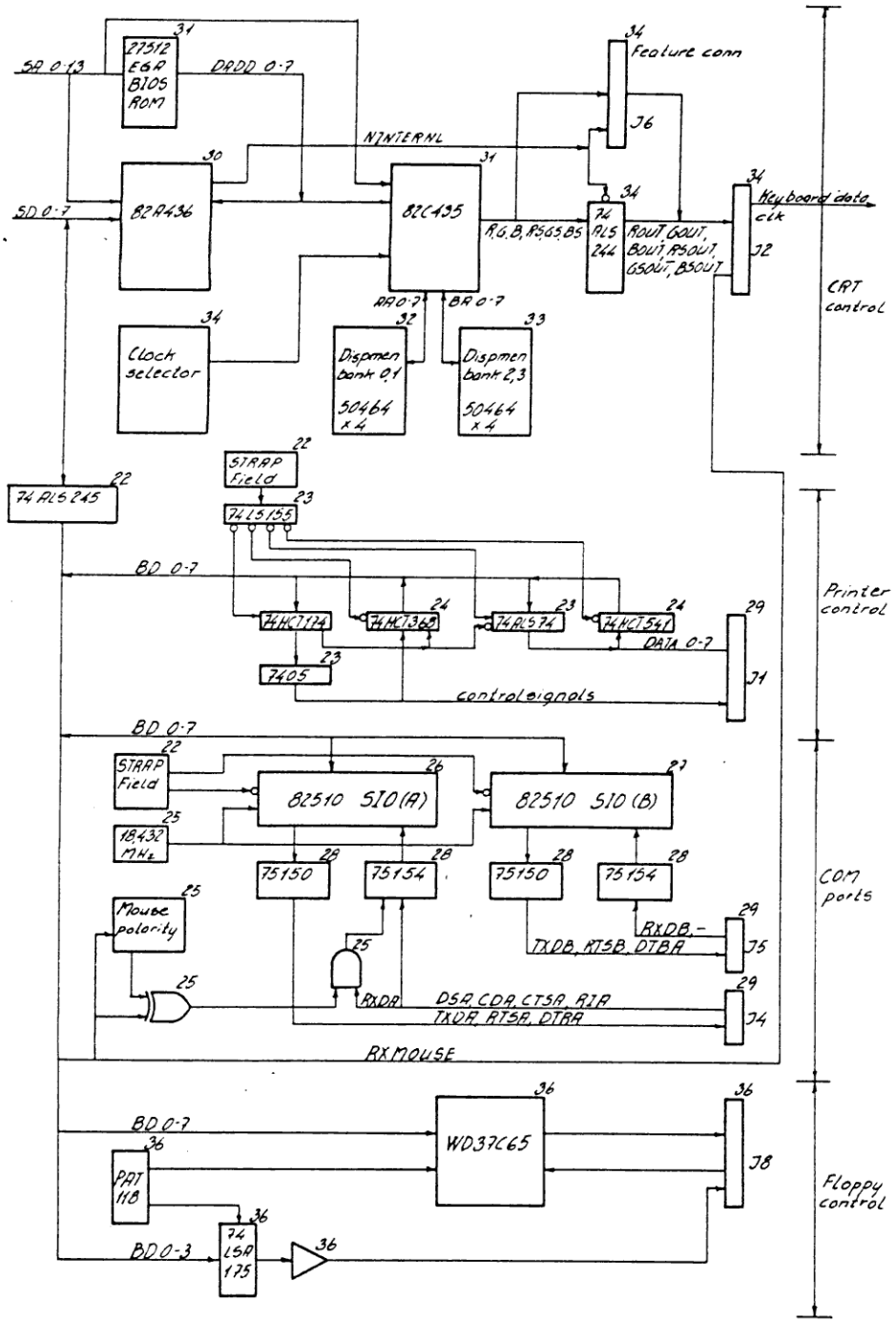


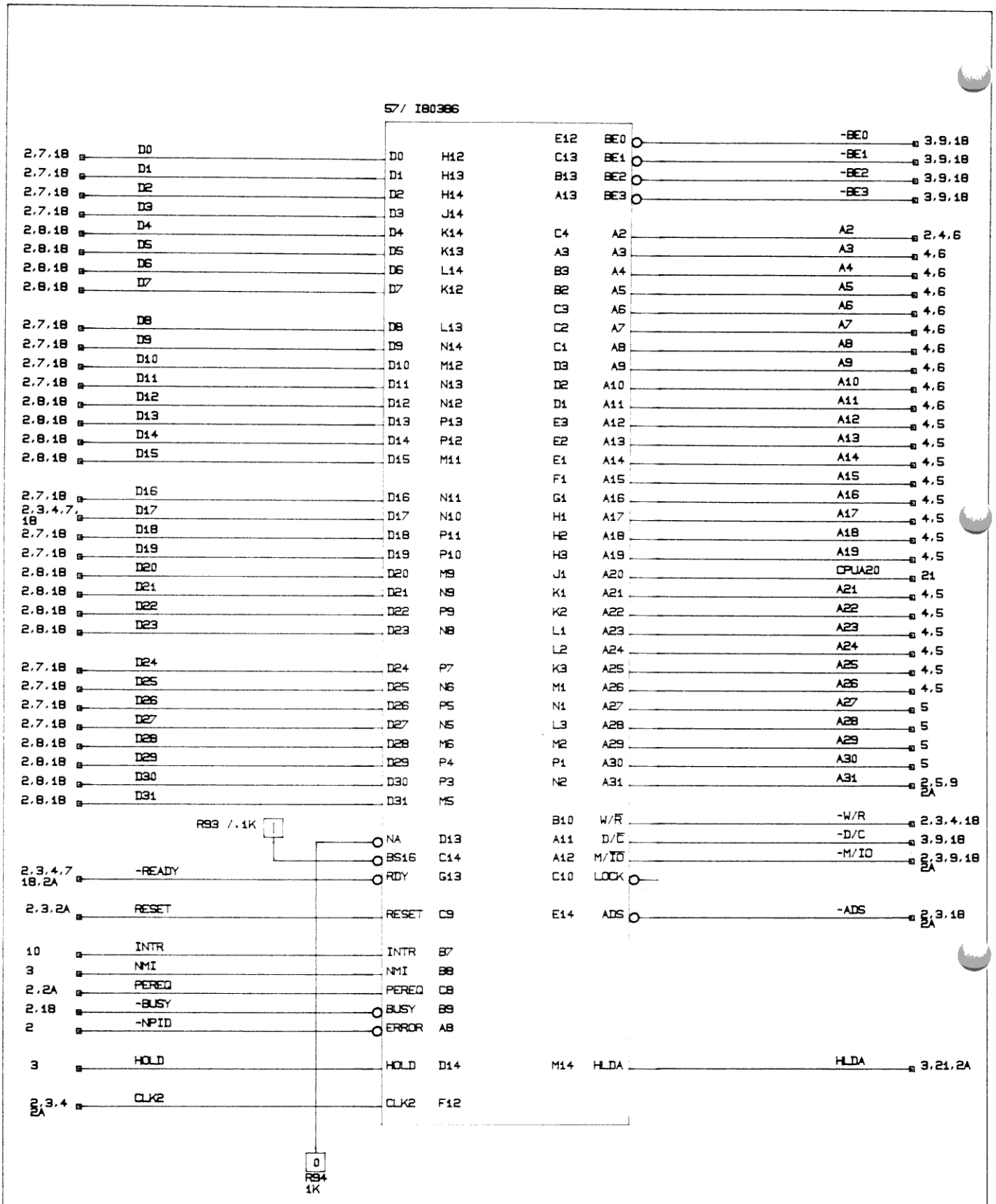
Fig. 4 **detailed** block diagram for the I/O section.

3.3 Logic diagrams

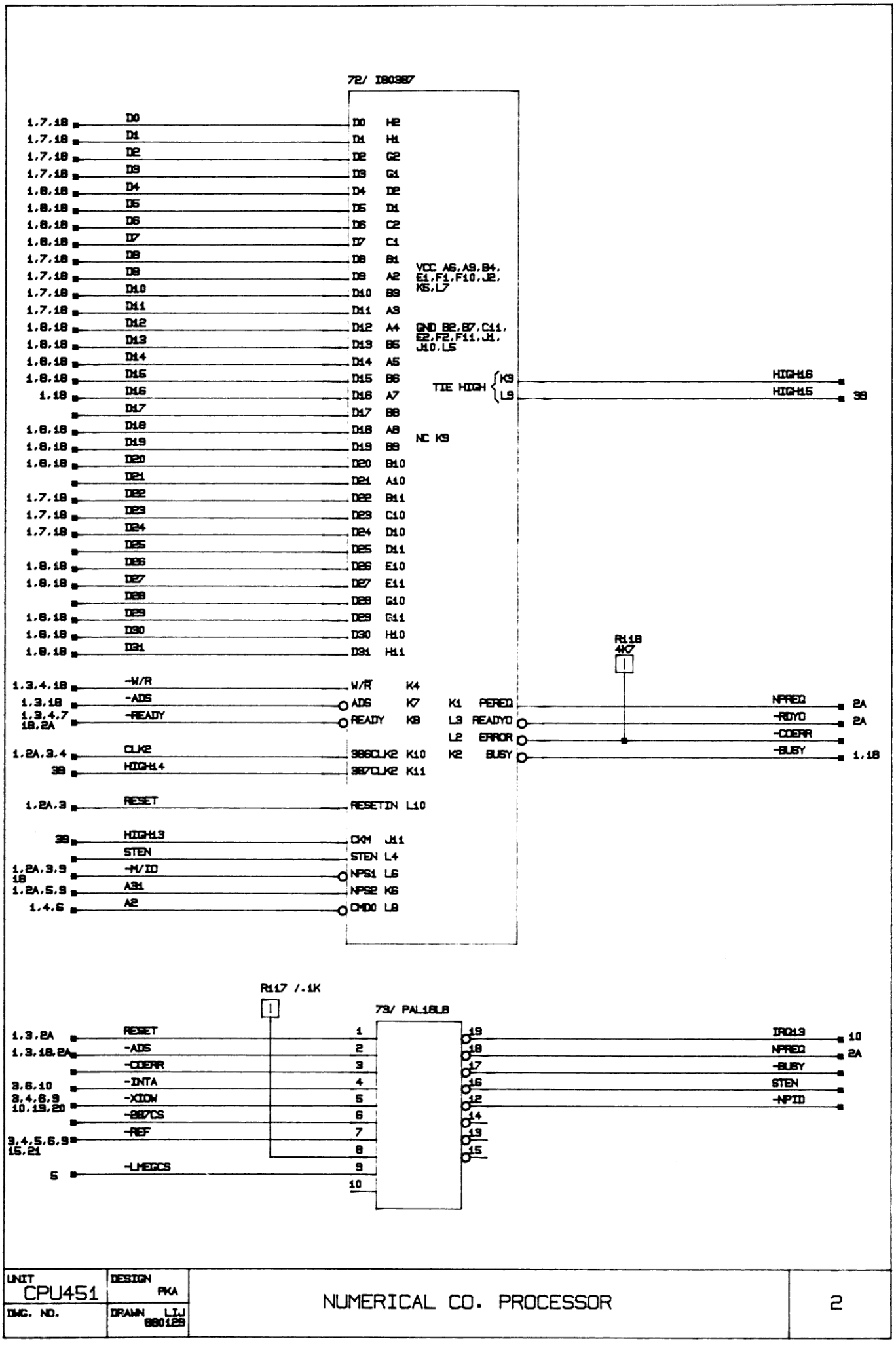
This section contains the logic diagrams of the CPU451.

The pages of the diagram are numbered separately from the pagination of the manual. These dragram numbers are used on the diagrams for source and destination references where signals enter or leave a page.

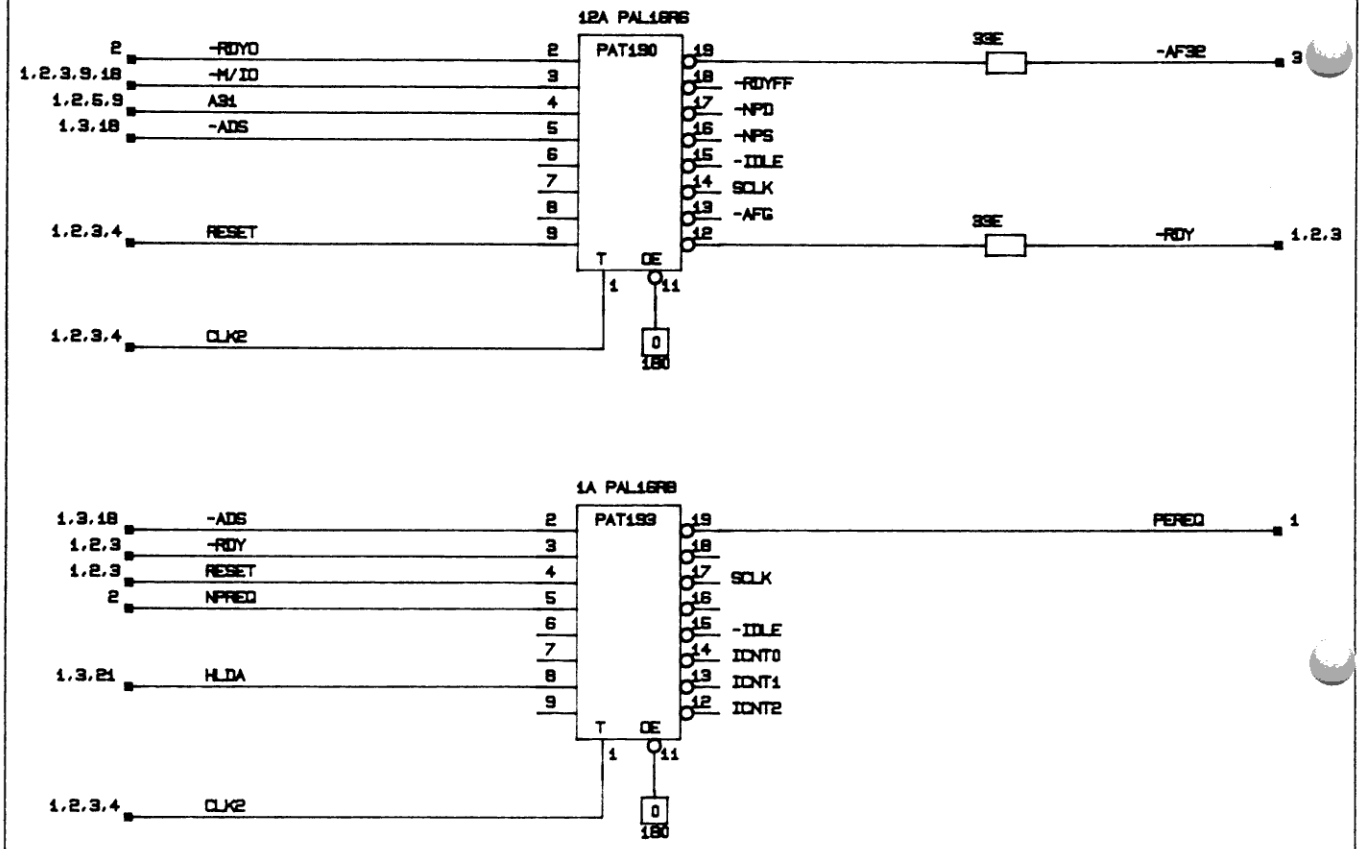
The position code found above each component on the diagrams coresponds to the position number marked on the printed circuit board.



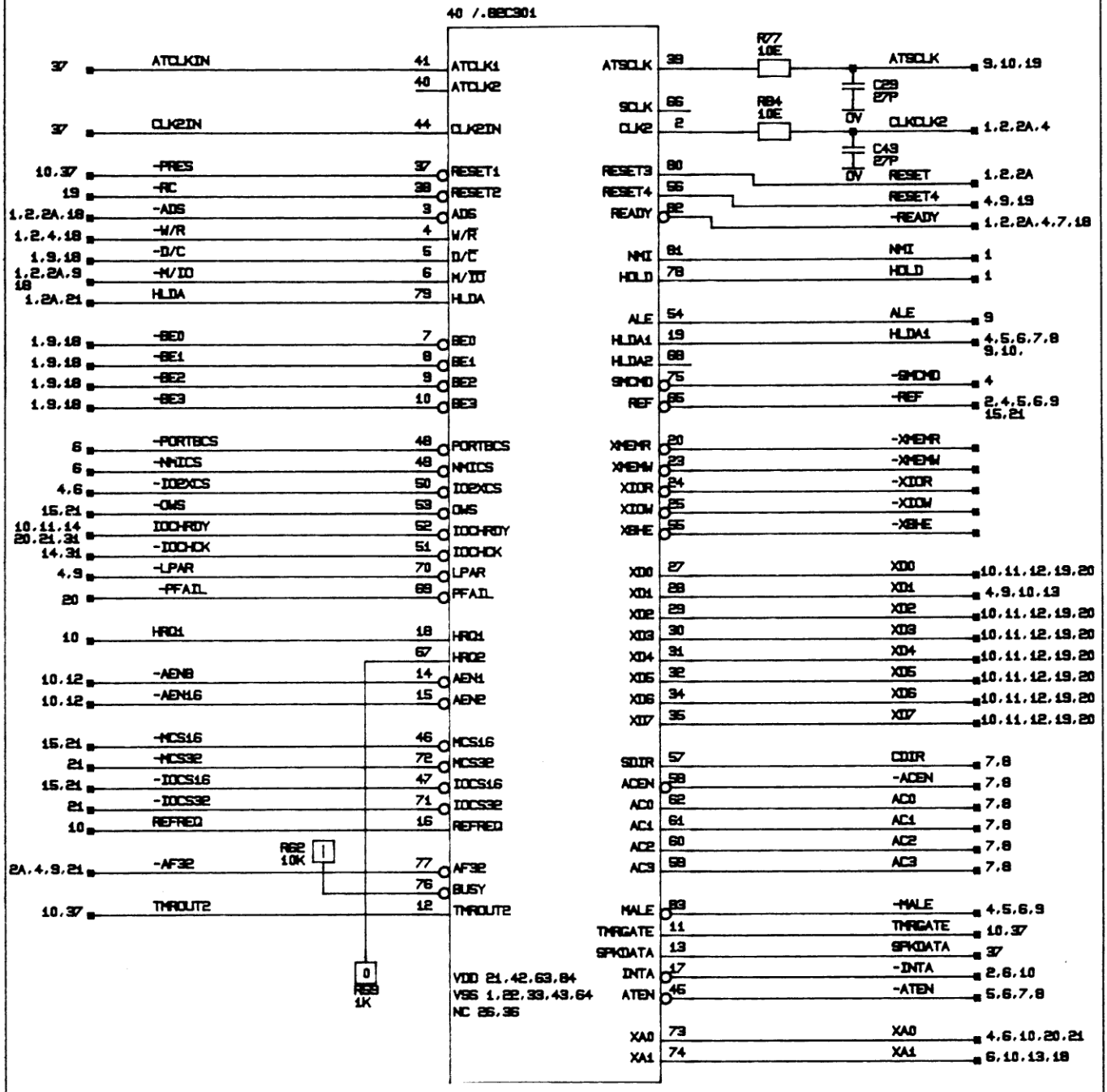
UNIT	DESIGN		
CPU451	PKA	CPU	1
DWG. NO.	DRAWN LIJ 880107		



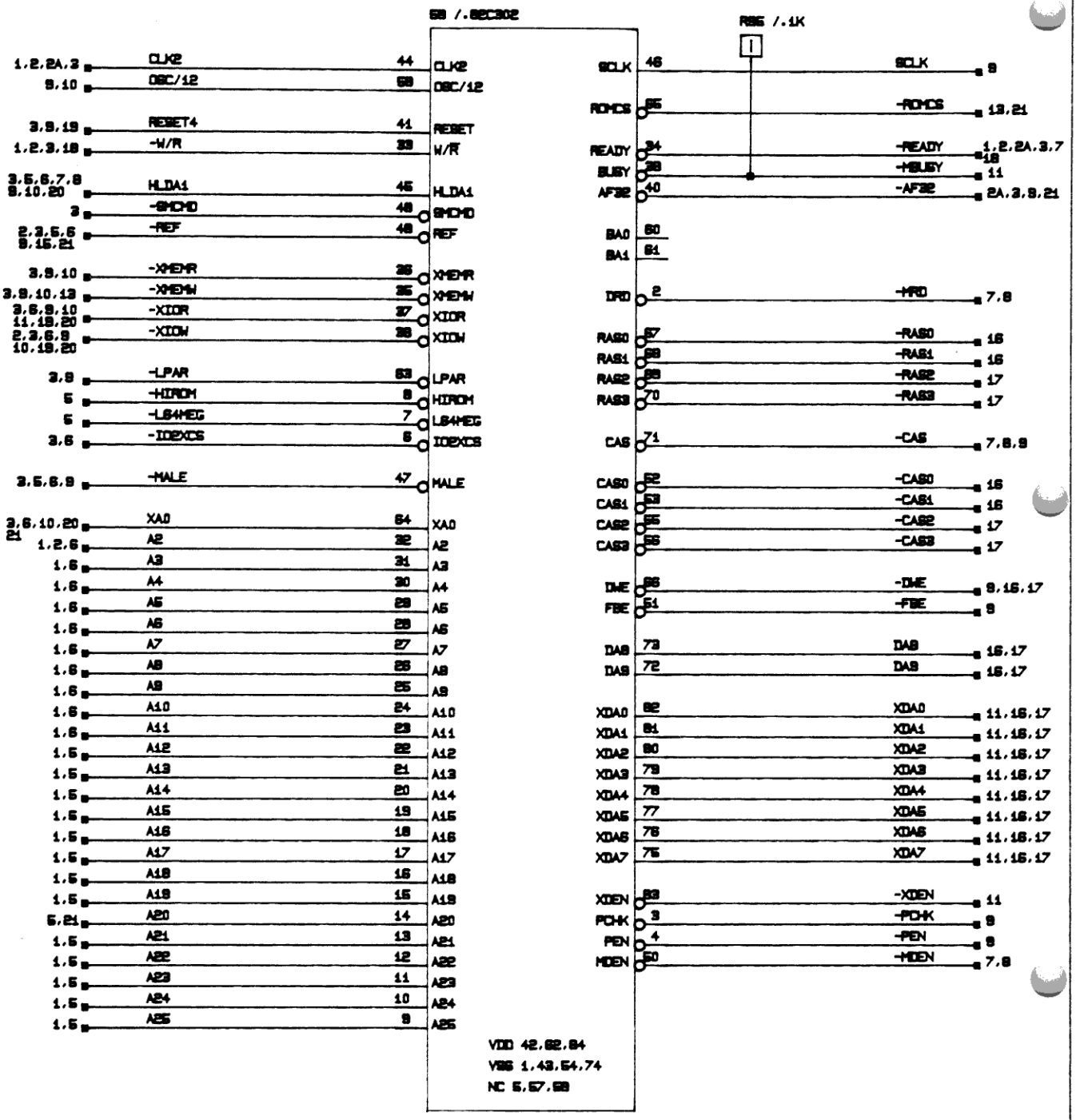
UNIT	DESIGN		
CPU451	PKA	NUMERICAL CO. PROCESSOR	2
DWG. NO.	DRAWN LIJ 880129		



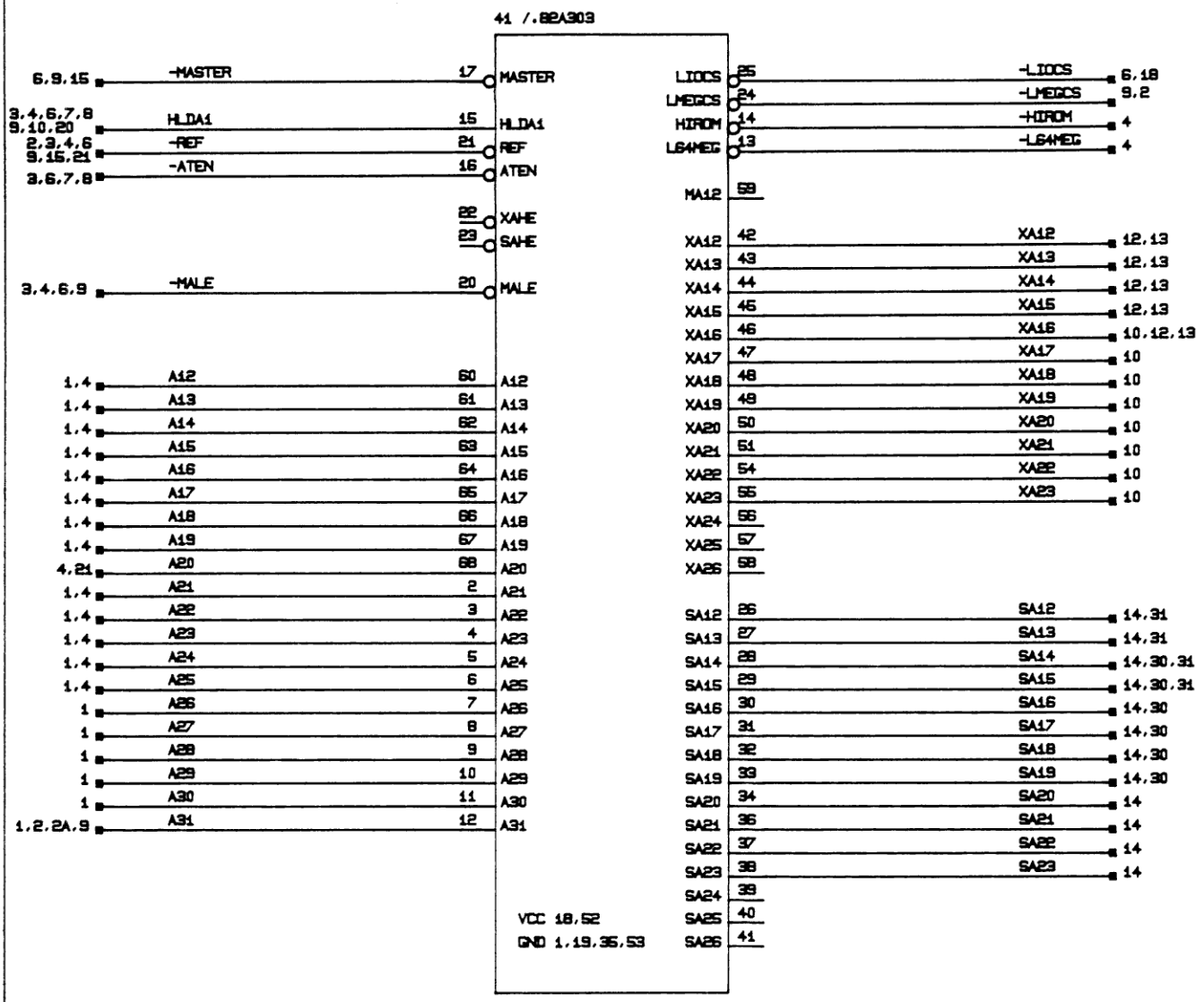
UNIT	DESIGN		
CPU451	PKA	NPX GLUE	2A
DWG. NO.	DRAWN LIJ 880125		



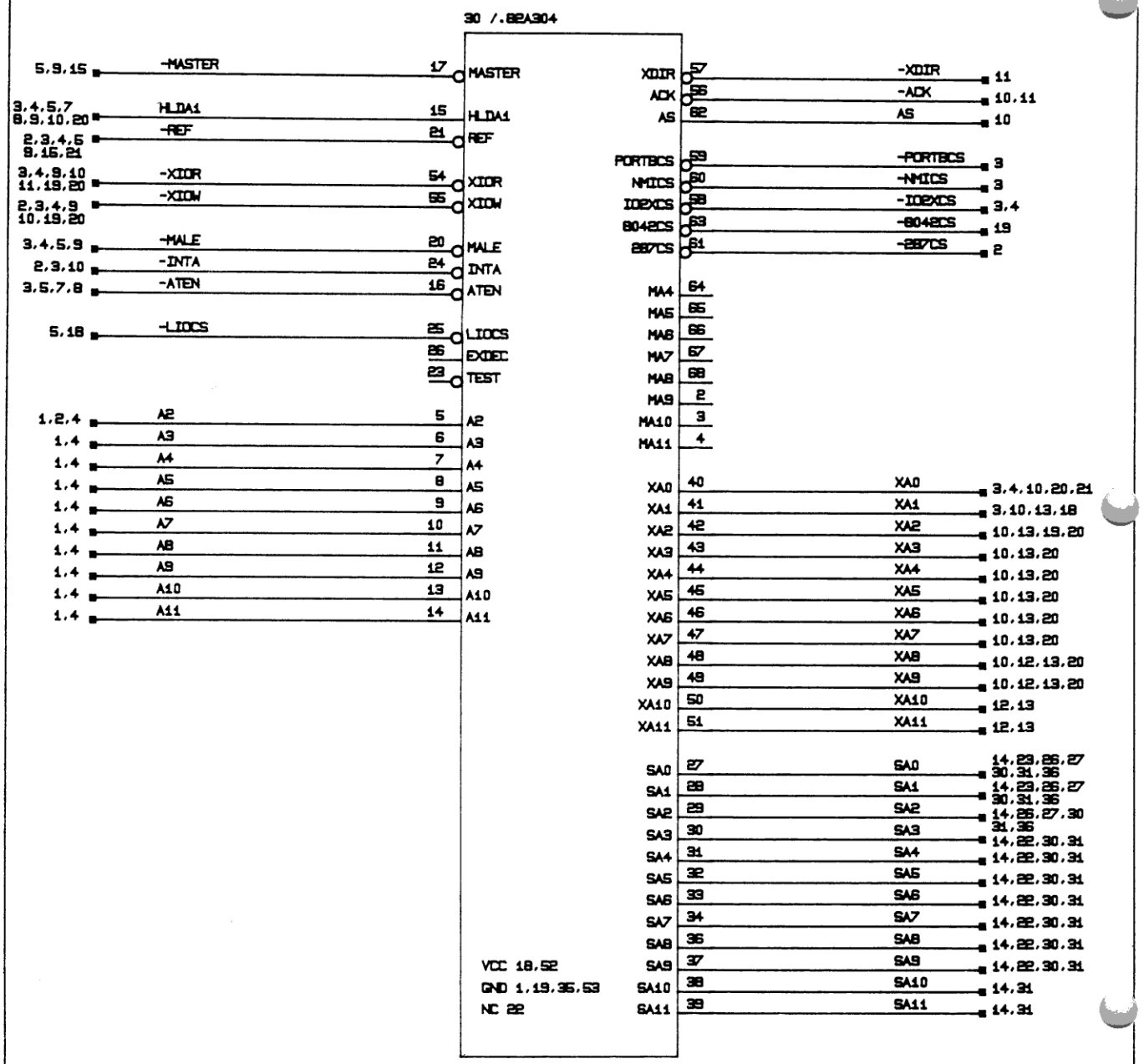
UNIT	DESIGN		
CPU451	PKA	BUS CONTROLLER	3
DWG. NO.	DRAWN LIJ 880129		



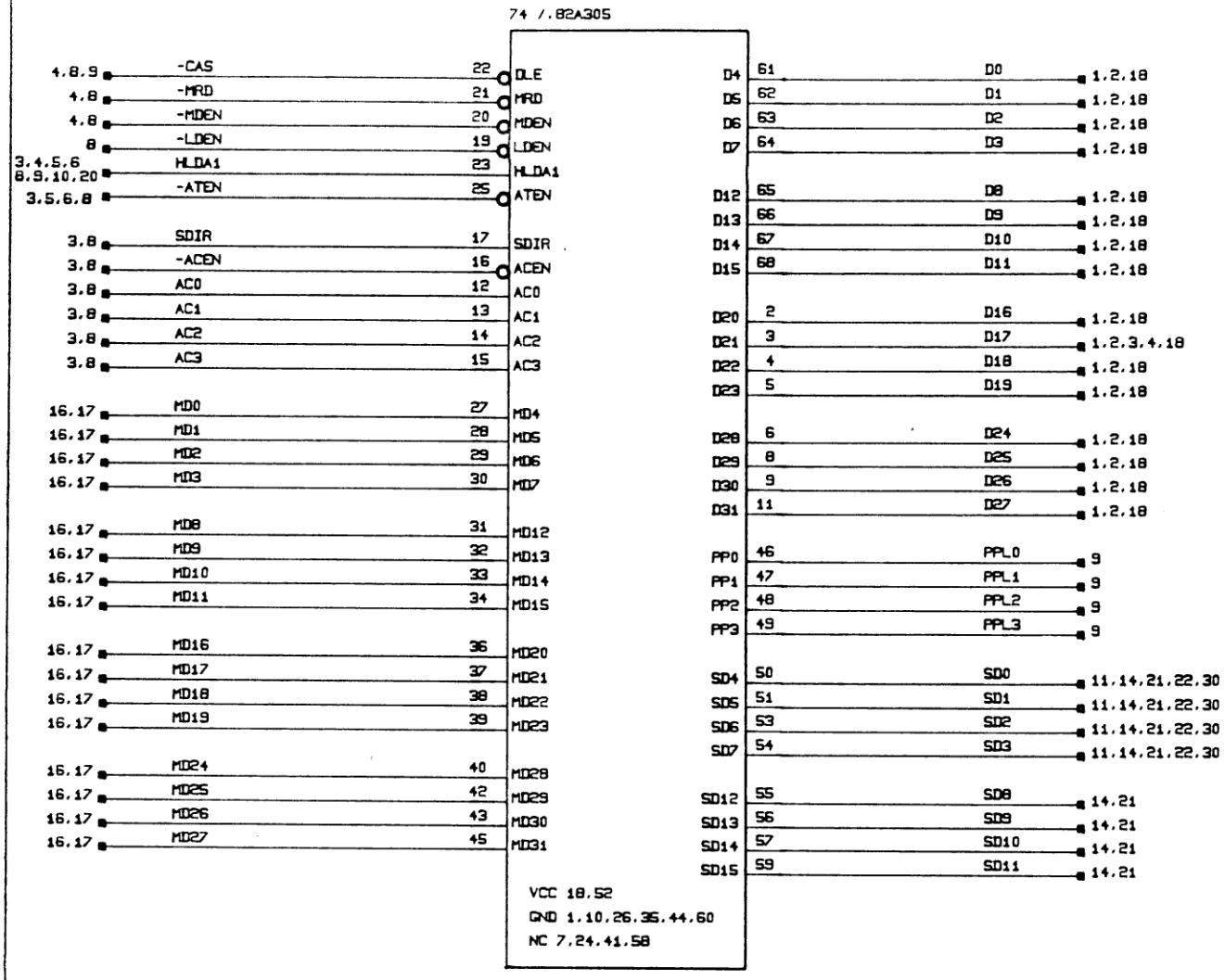
UNIT	DESIGN		
CPU451	PKA	PAGE INTERLEAVED MEMORY CONTROLLER	4
DWG. NO.	DRAWN LIJ 880107		



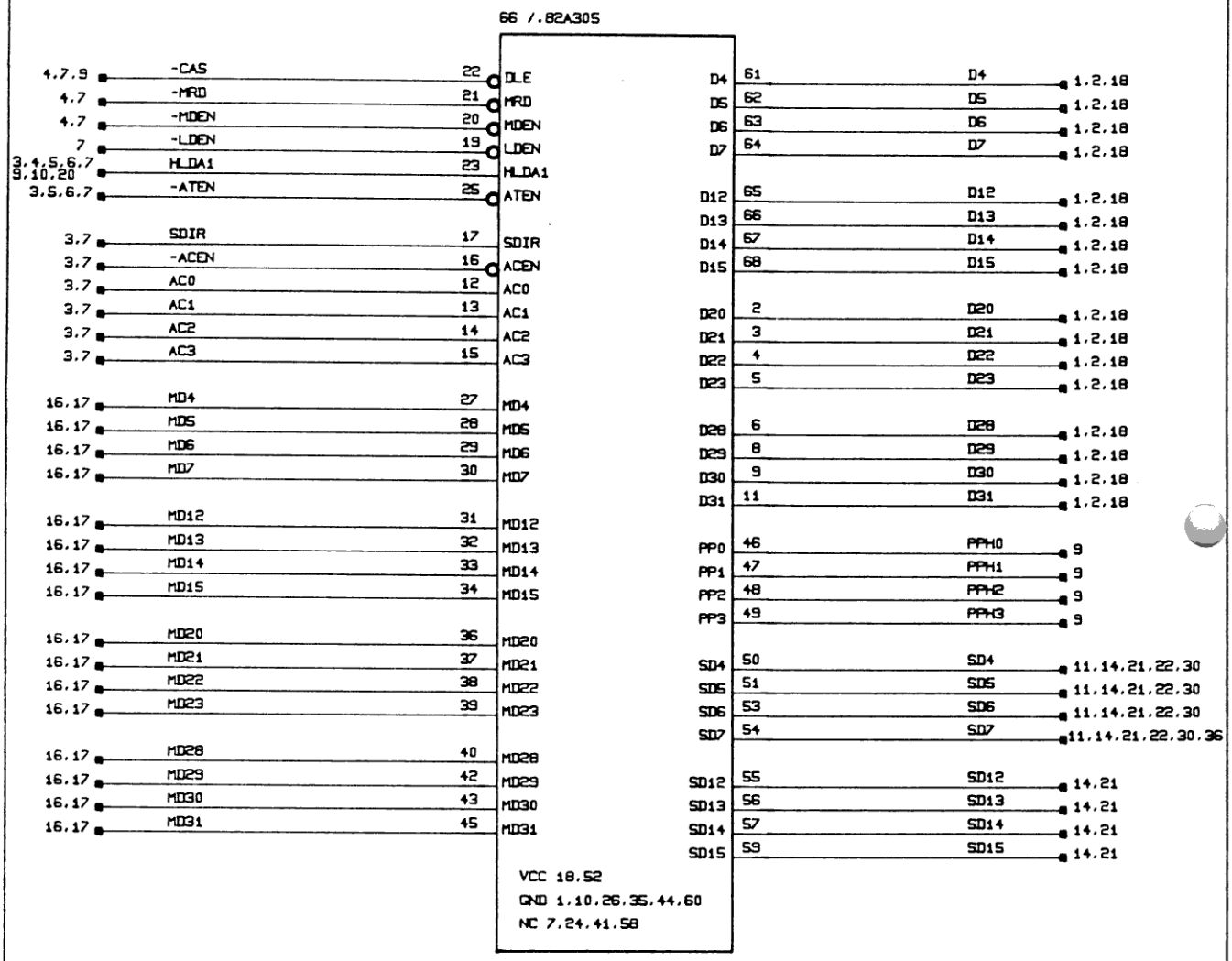
UNIT	DESIGN		
CPU451	PKA	ADDRESS HIGH BUFFER	5
DWG. NO.	DRAWN LJJ 880128		



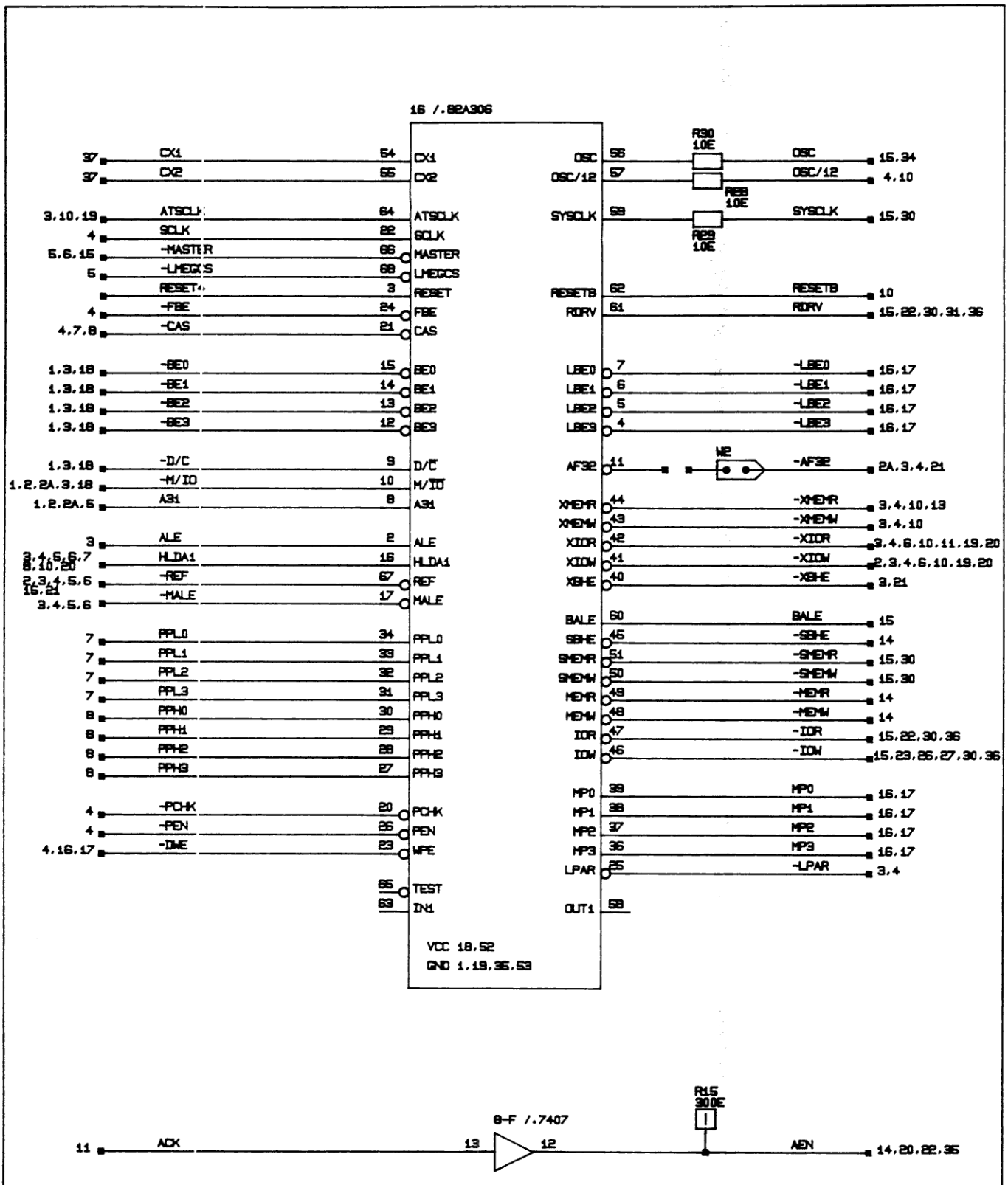
UNIT CPU451	DESIGN PKA	ADDRESSE LOW BUFFER	6
DWG. NO.	DRAWN LIJ 880129		



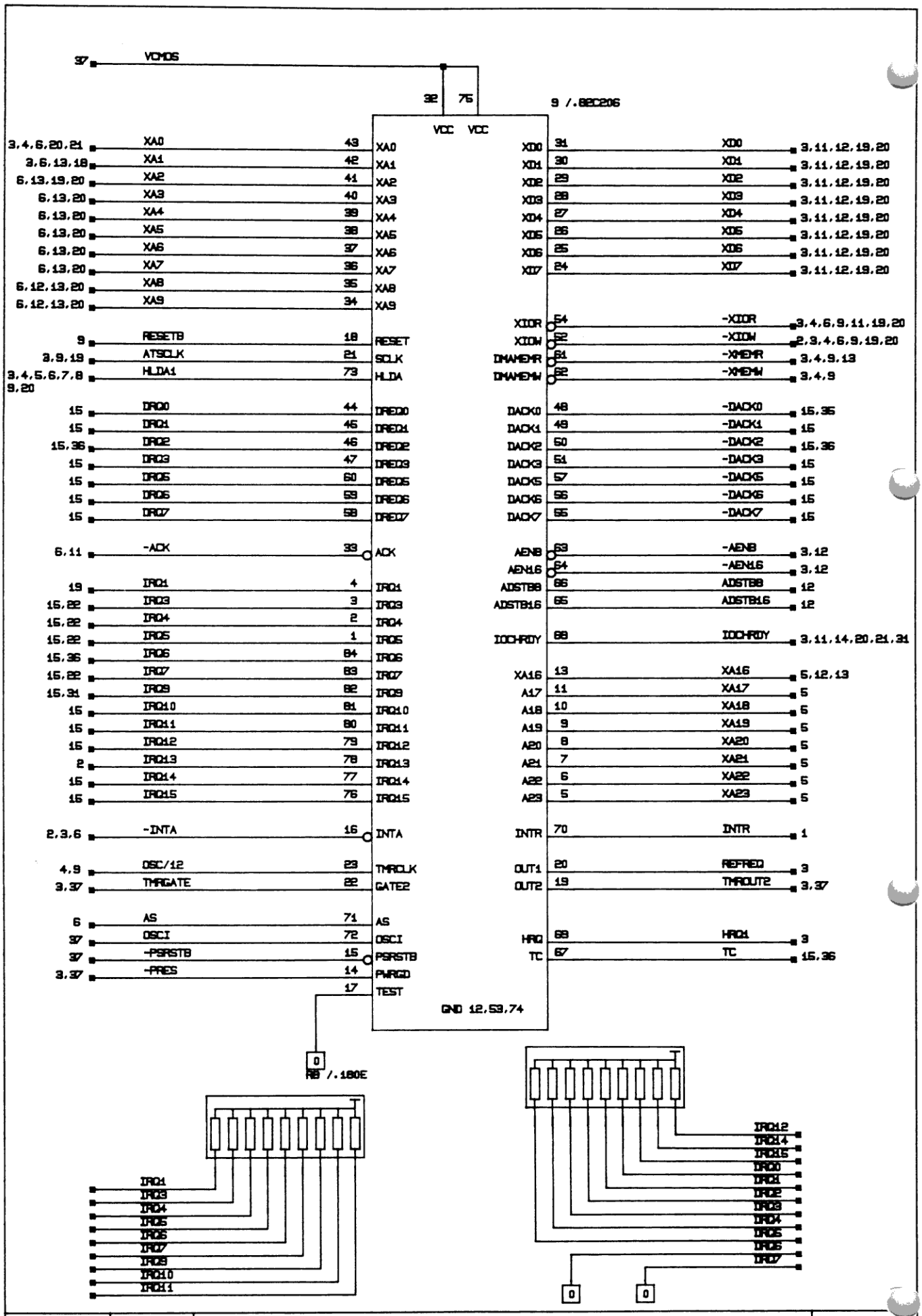
UNIT CPU451	DESIGN PKV.	MEMORY/AT DATA BUS BUFFER	7
DWG. NO.	DRAWN ACA 8/06/88		



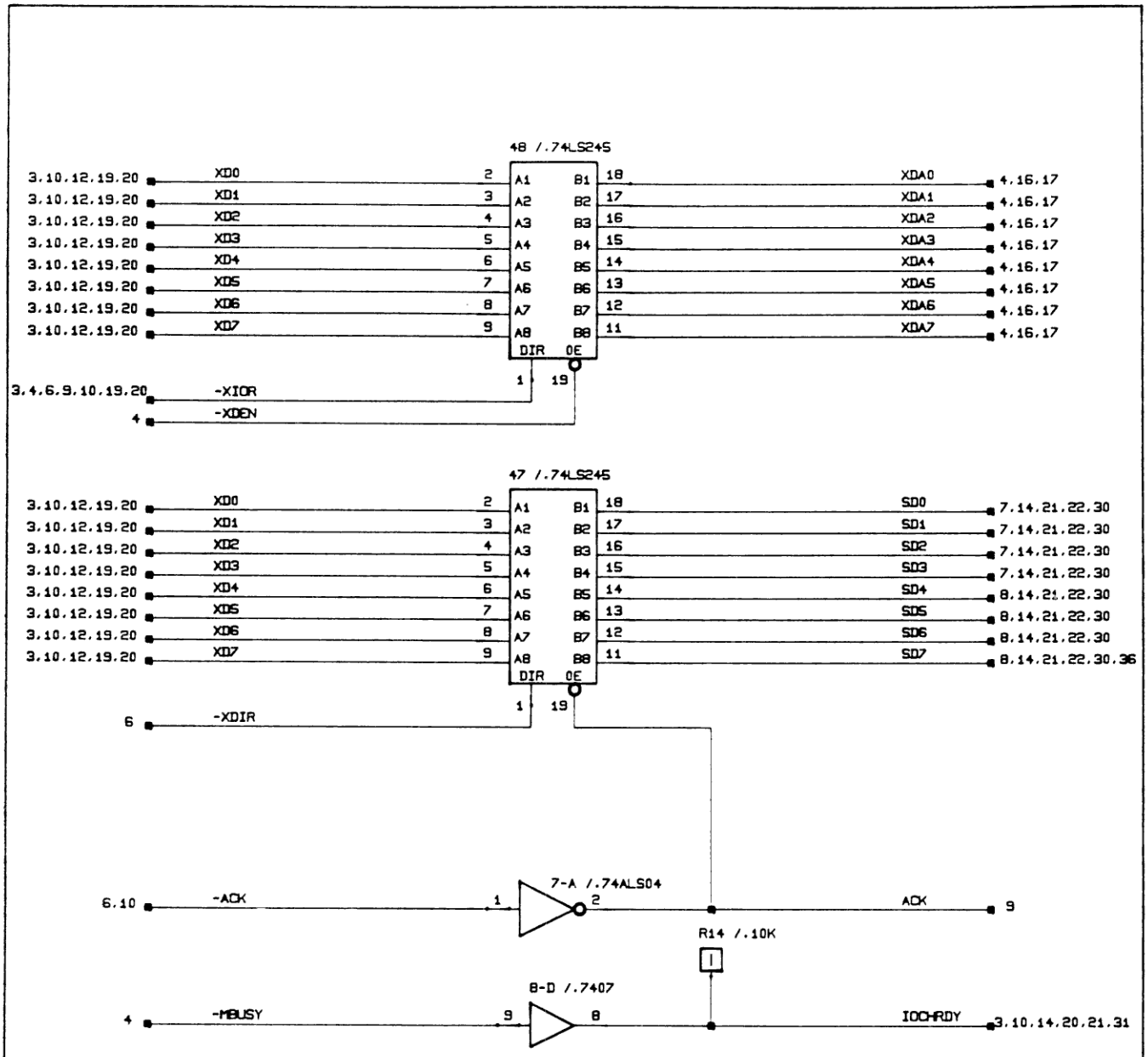
UNIT	DESIGN		
CPU451	PKA	MEMORY/X AT DATA BUS BUFFER	8
DWG. NO.	DRAWN AGA 870825		



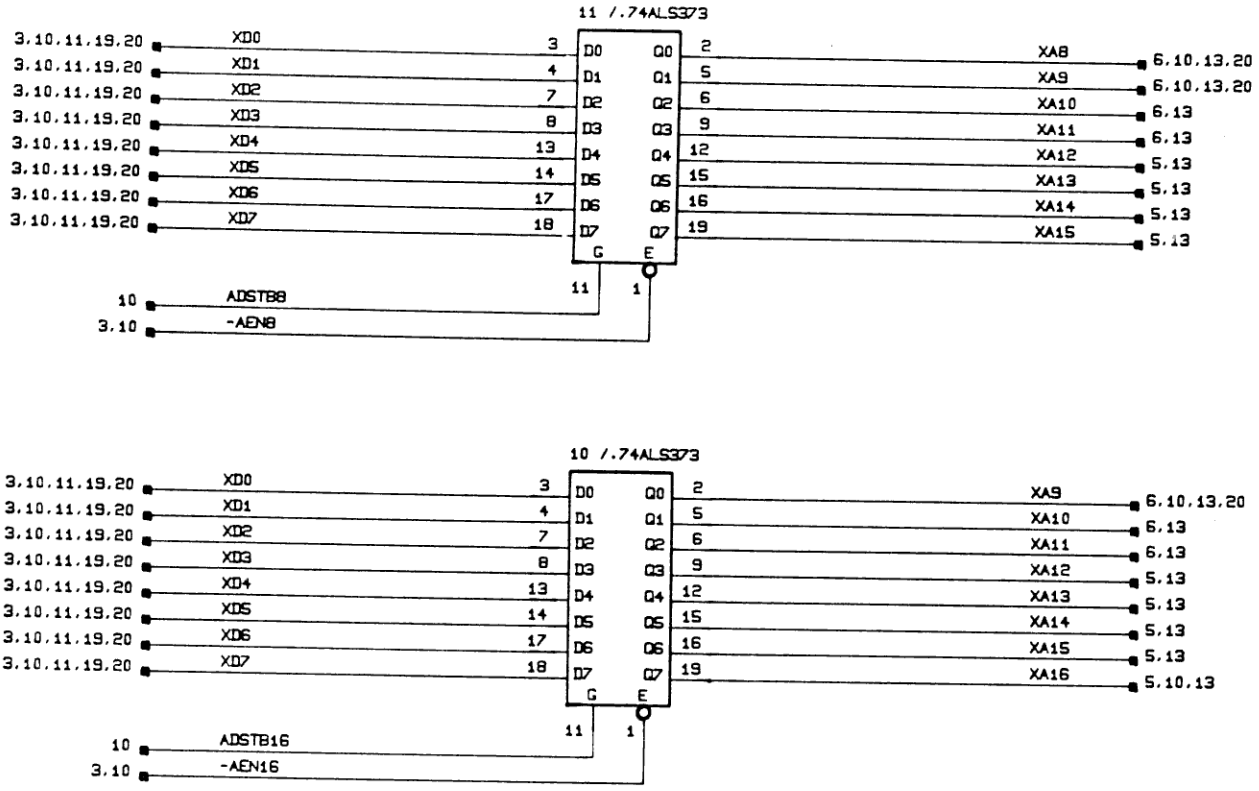
UNIT	DESIGN		
CPU451	PKA	CONTROL BUFFER	9
DWG. NO.	DRAWN LIJ 880129		



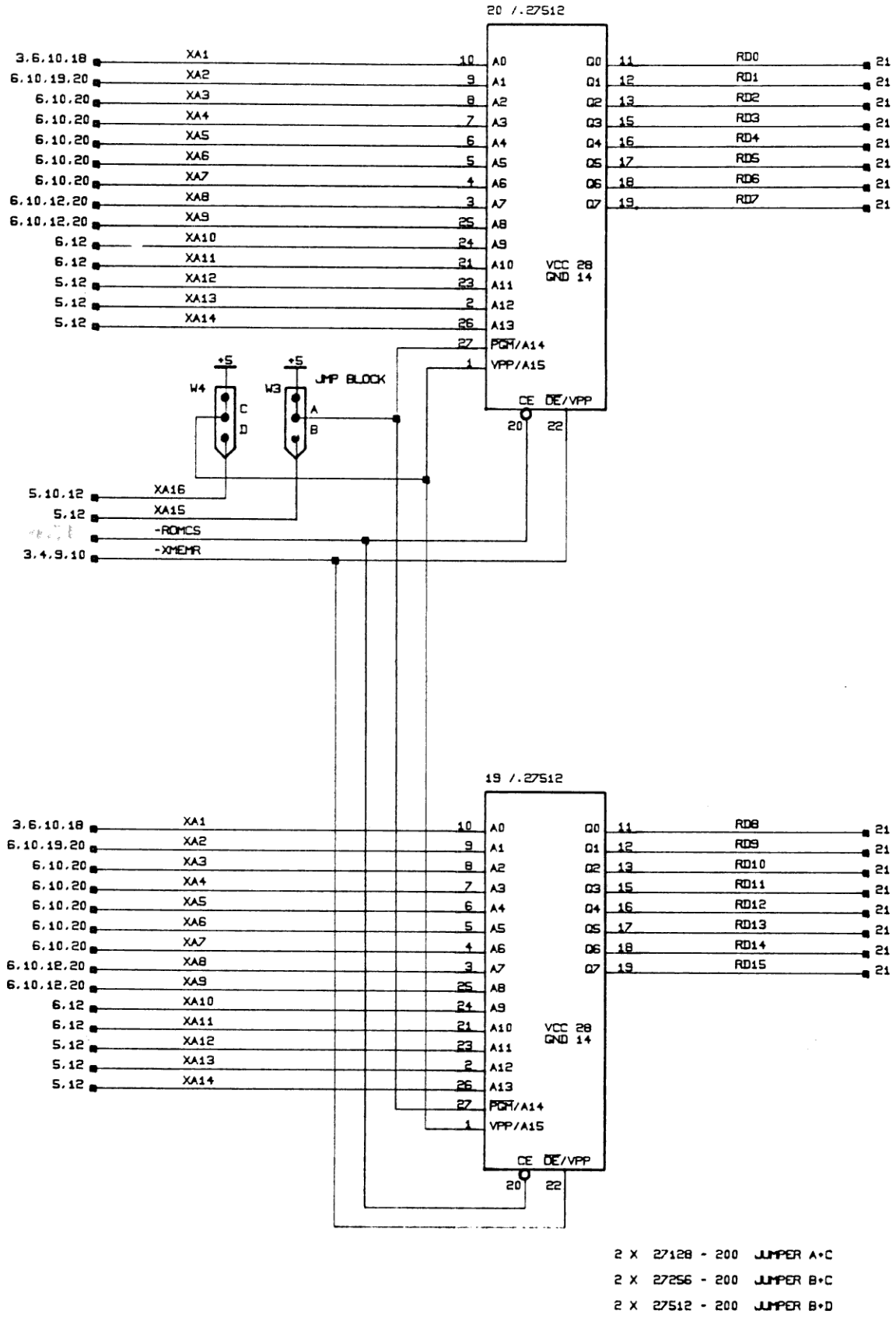
UNIT CPU451	DESIGN PKA	INTERGRATED PERIPHERALS CONTROLLER	10
DWG. NO.	DRAWN LIJ 880129		



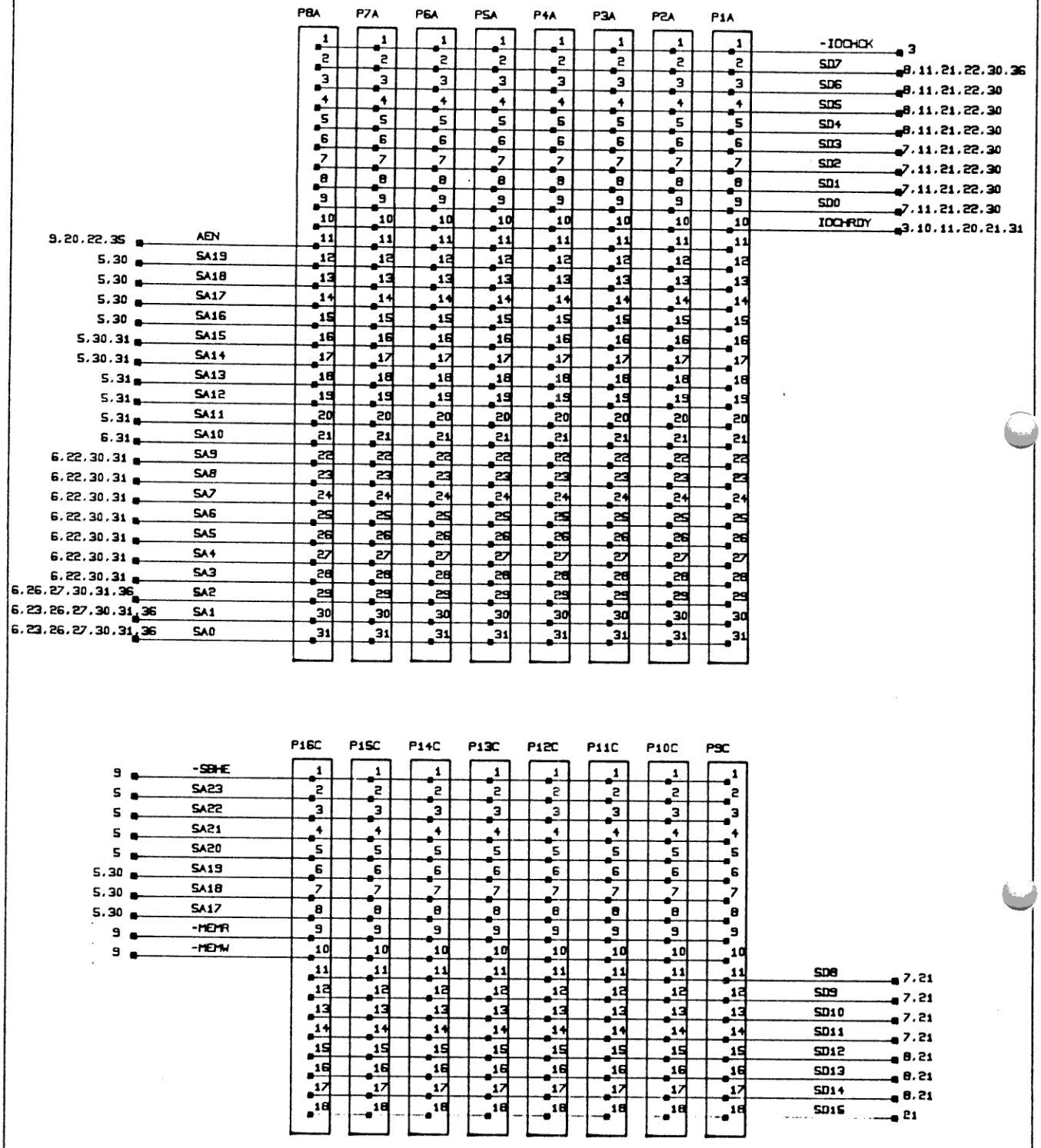
UNIT	DESIGN		
CPU451	PKA	DATABUFFERS, CLOCK GENERATOR	11
DWG. NO.	DRAWN AGA 870825		



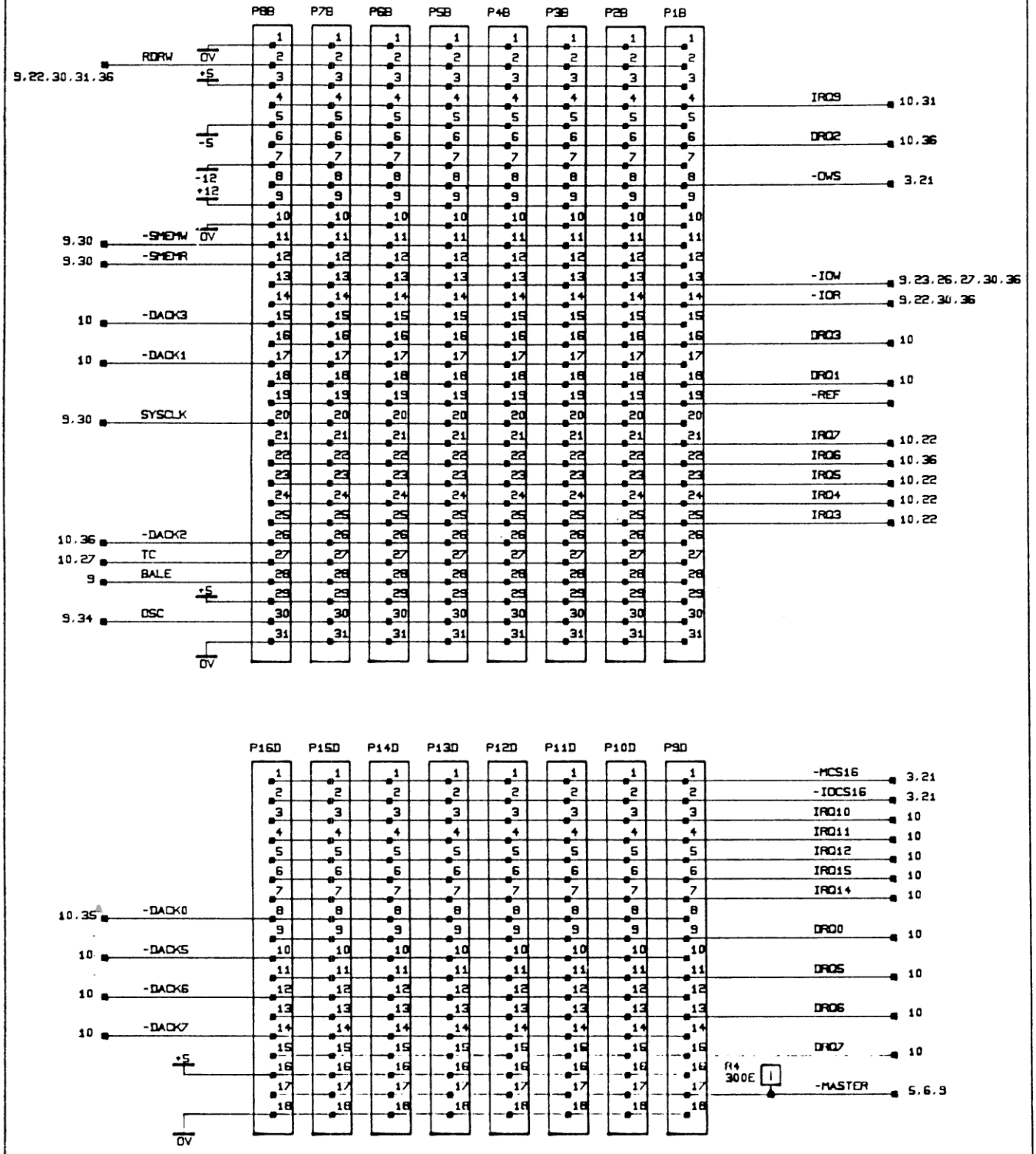
UNIT CPU451	DESIGN PKA	ADDRESS BUFFERS	12
DWG. NO.	DRAWN AGA 870825		



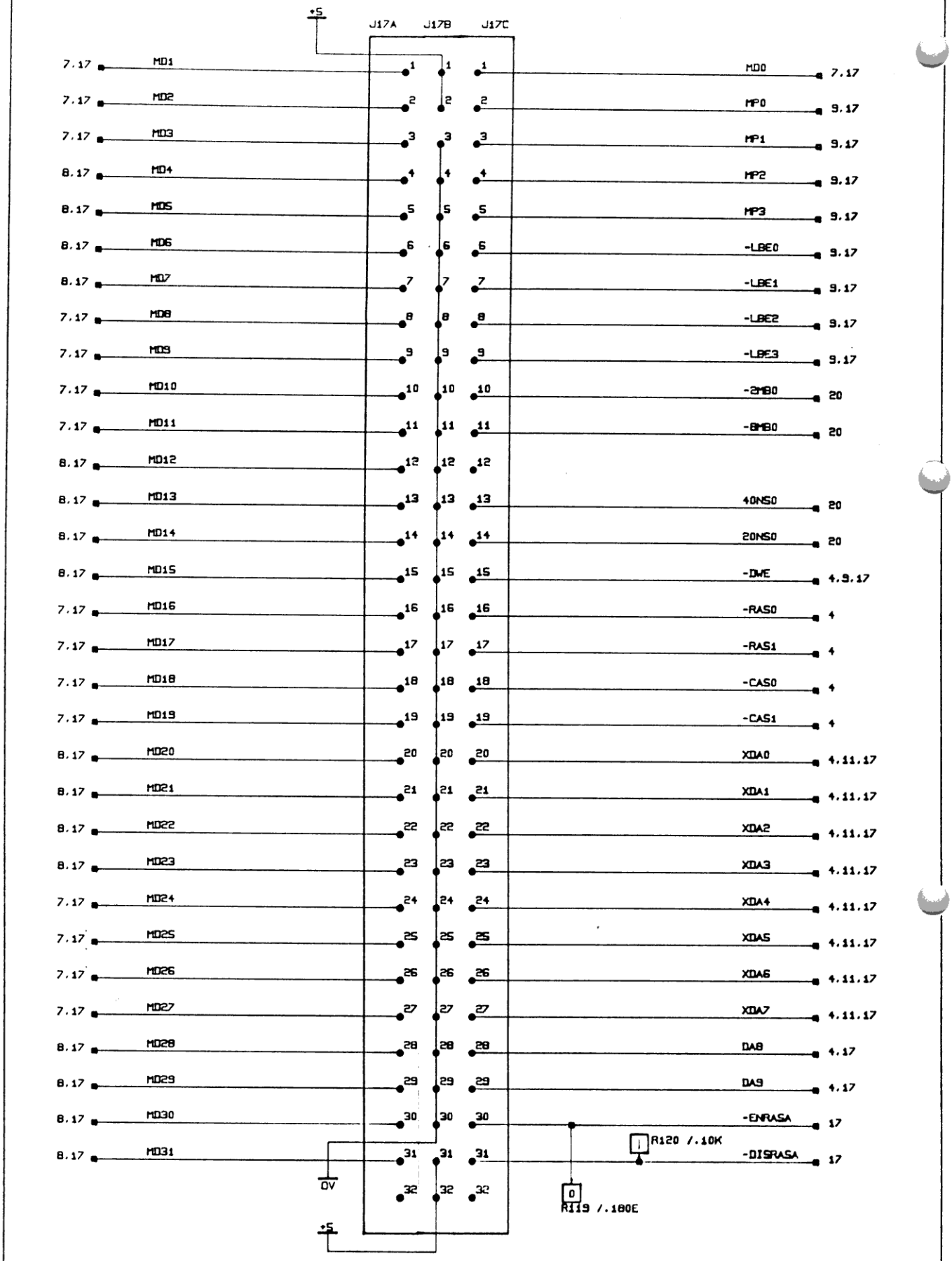
UNIT	DESIGN		
CPU451	PKA	BIOS ROMS	13
DWG. NO.	DRAWN AGA 870825		



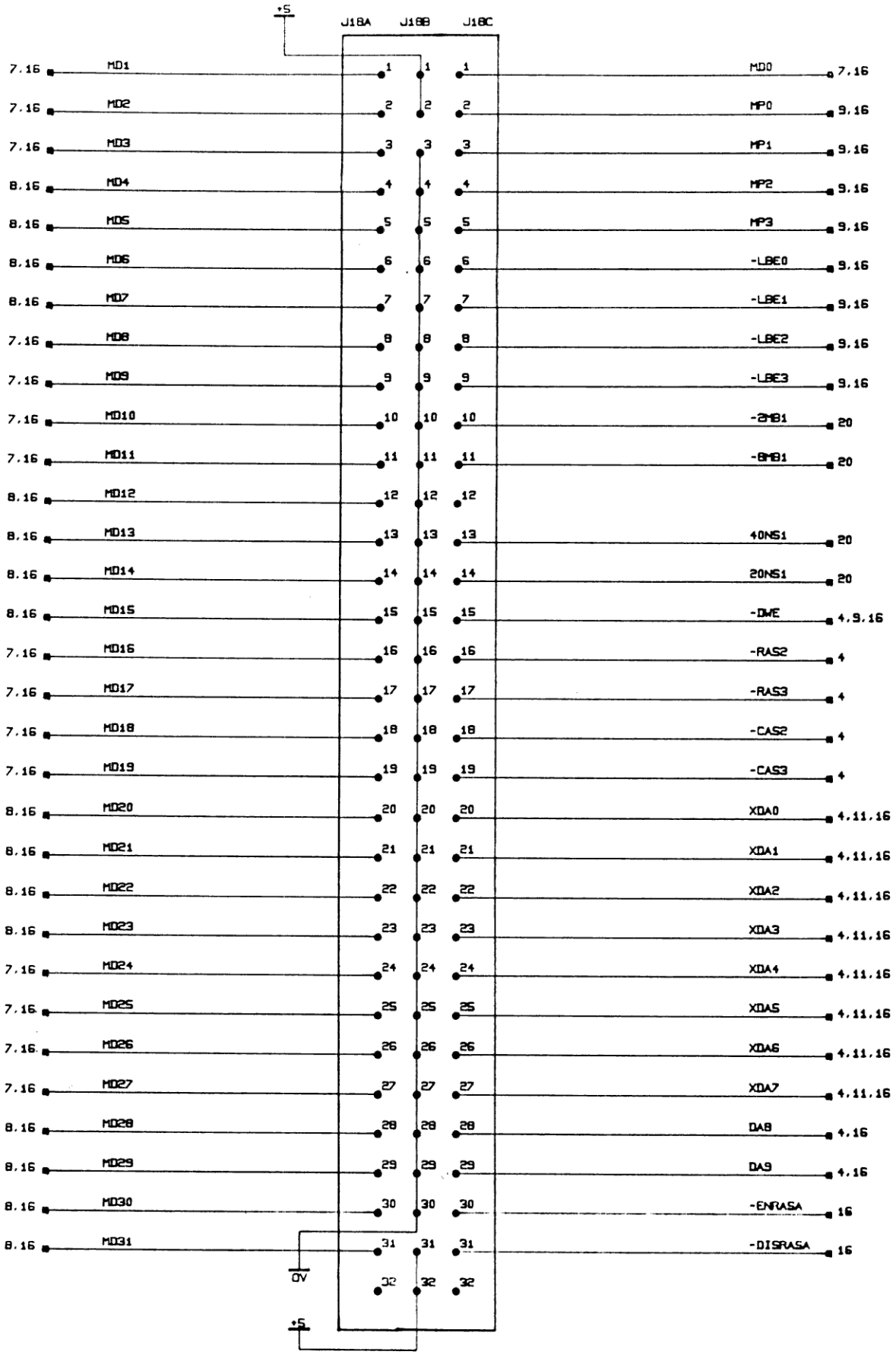
UNIT CPU451	DESIGN PKA	PC/AT BUS CONNECTORS	14
DWG. NO.	DRAWN AGA 870826		



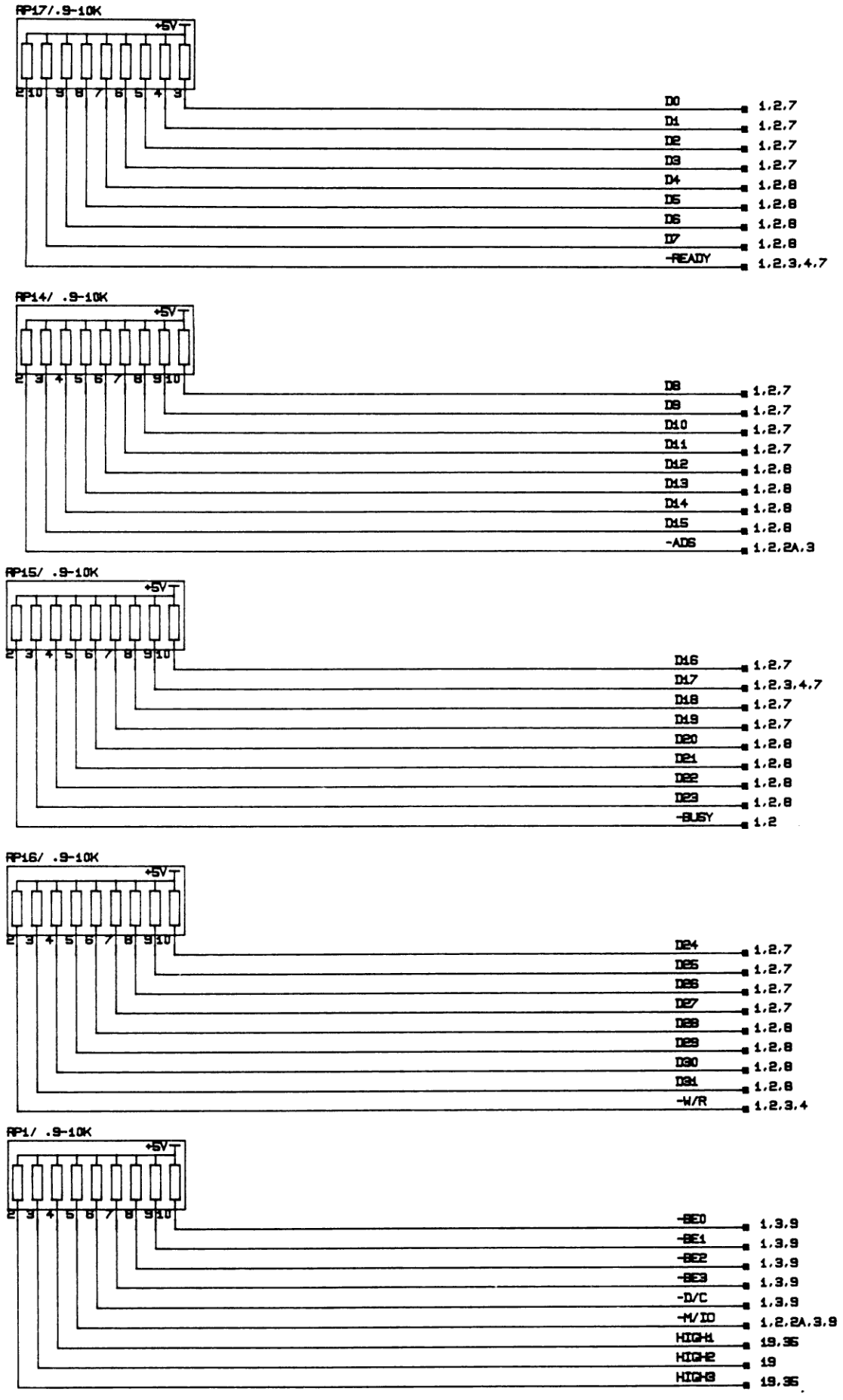
UNIT	DESIGN		
CPU451	PKA	PC/AT BUS CONNECTORS	15
DWG. NO.	DRAWN ACA 870826		



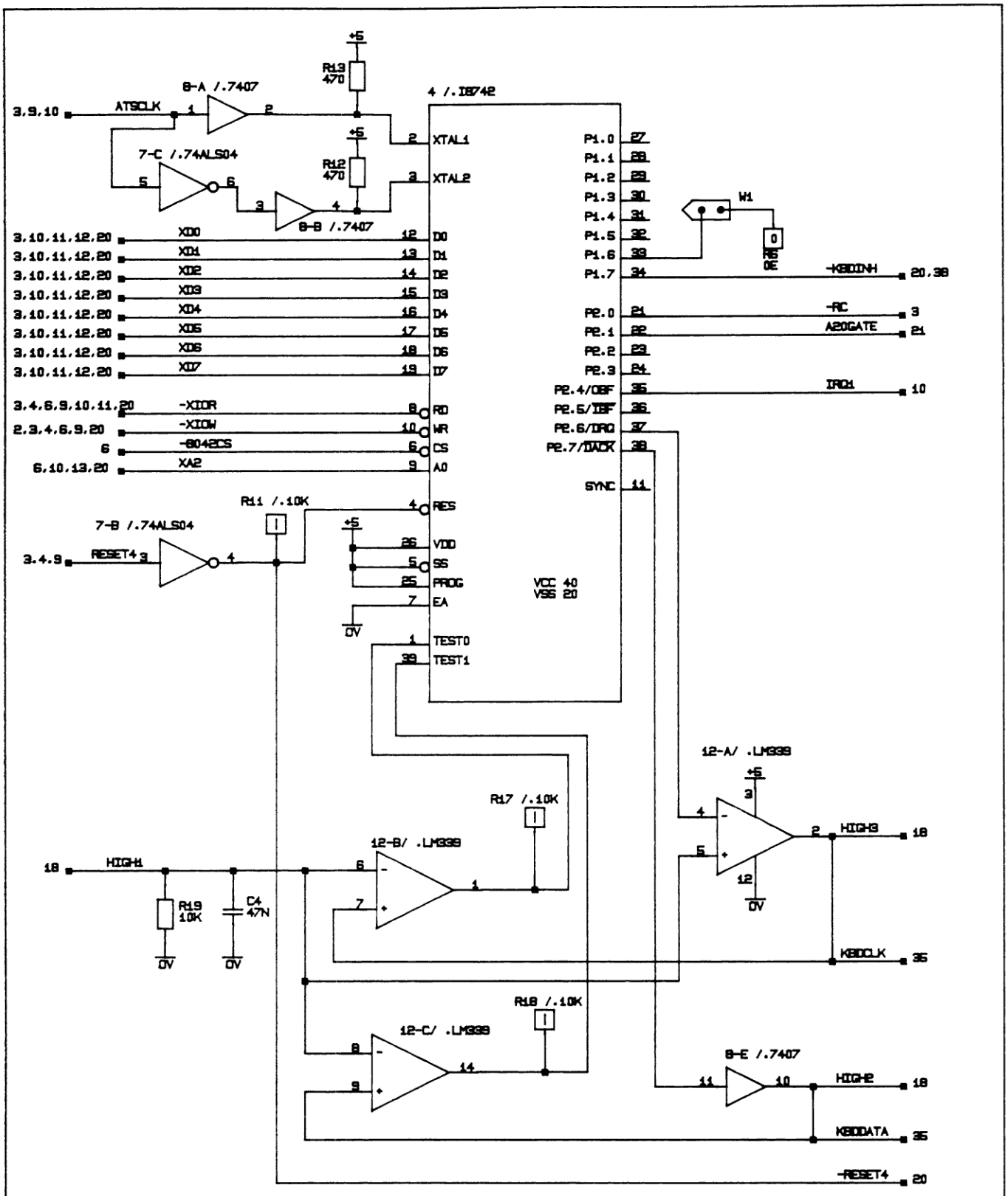
UNIT CPU451	DESIGN PKA	CONNECTOR FOR MEM BANK 0, 1	16
DWG. NO.	DRAWN AGA 870831		



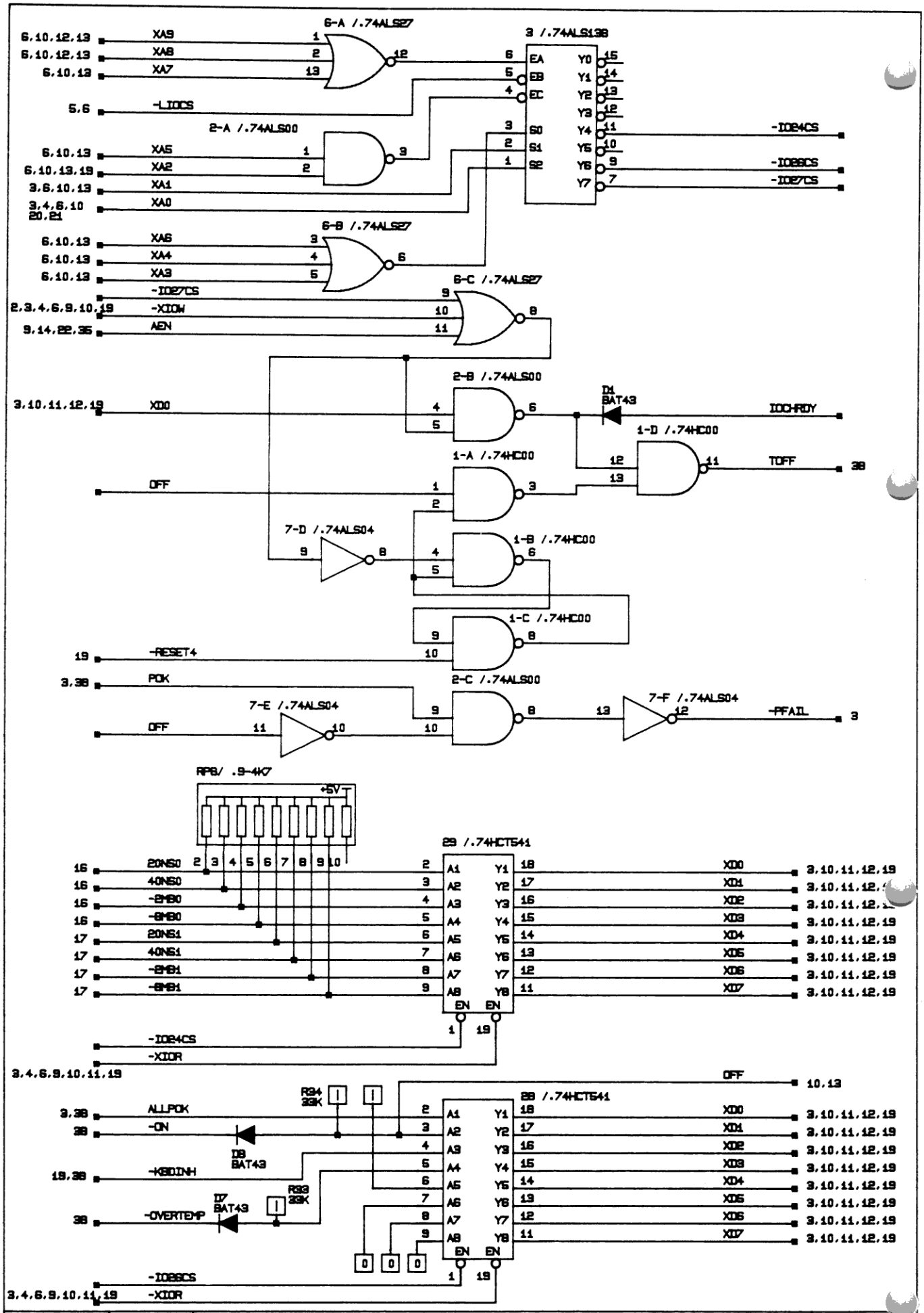
UNIT CPU451	DESIGN PKA	CONNECTOR FOR BANK 2, 3	17
DWG. NO.	DRAWN AGA 870831		



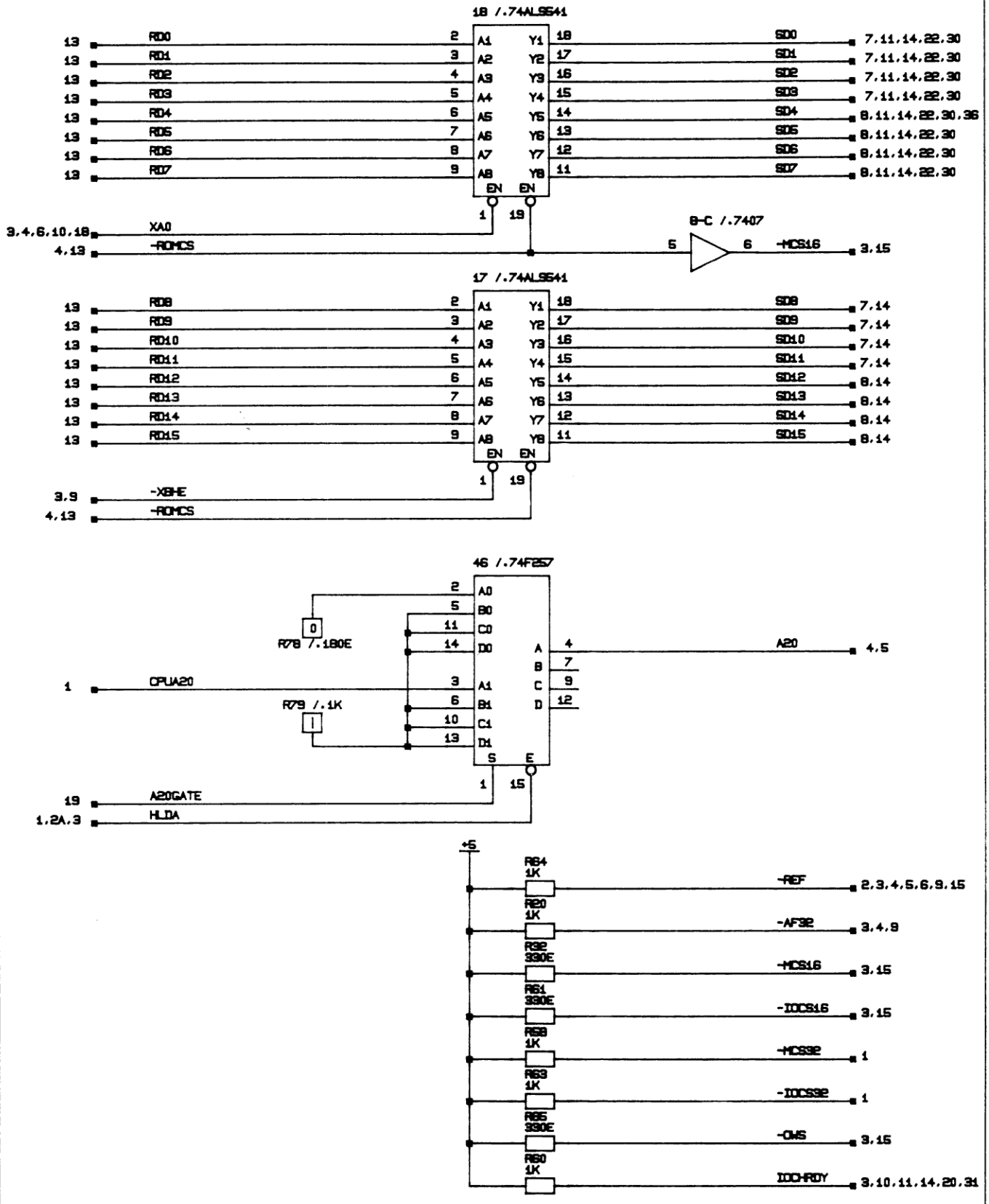
UNIT	DESIGN		
CPU451	PKA	PULL UP	18
DWG. NO.	DRAWN LIJ 880107		



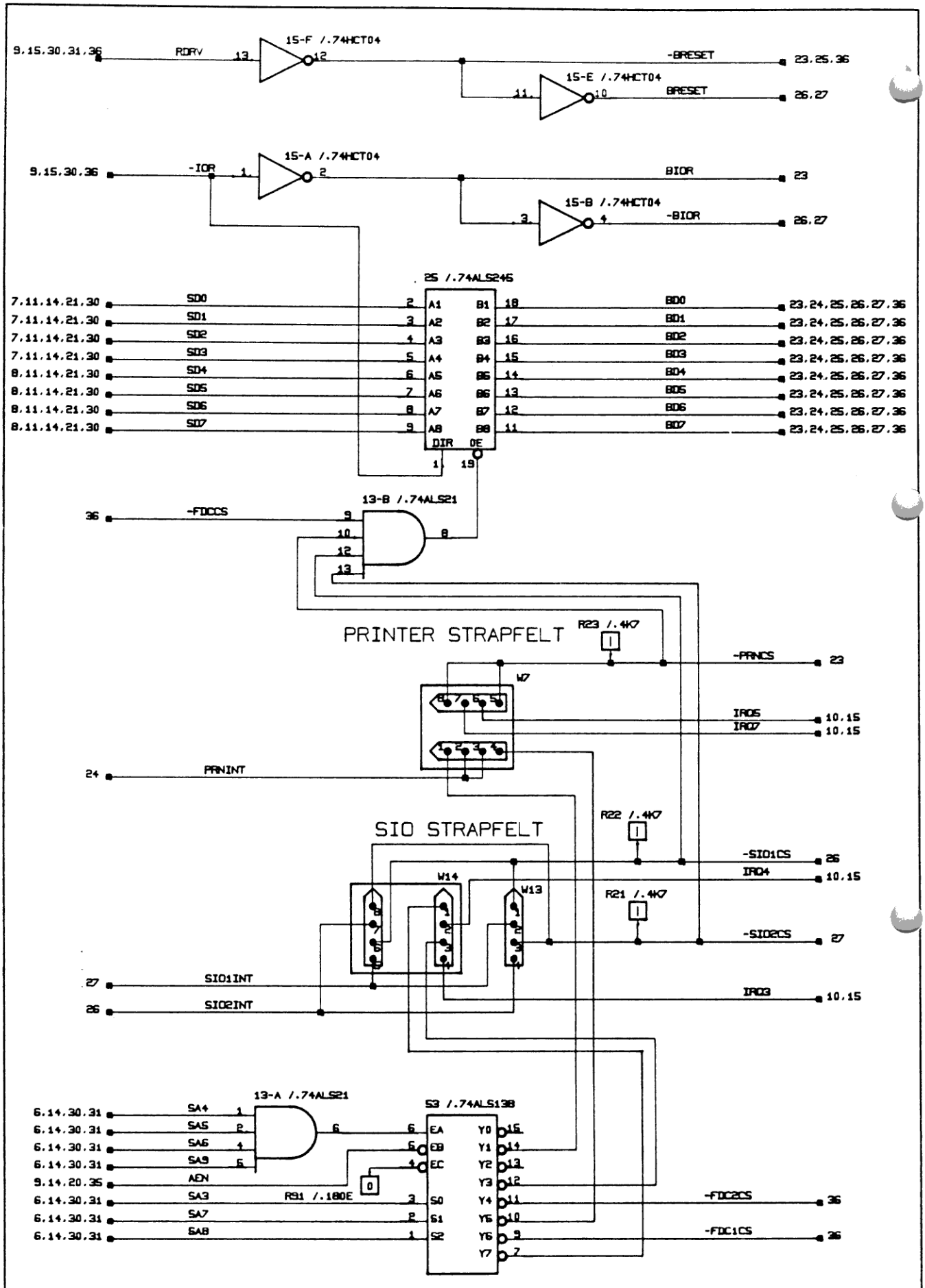
UNIT	DESIGN		
CPU451	PKA	KBD CONTROLLER	19
DWG. NO.	DRAWN LIJ 880129		



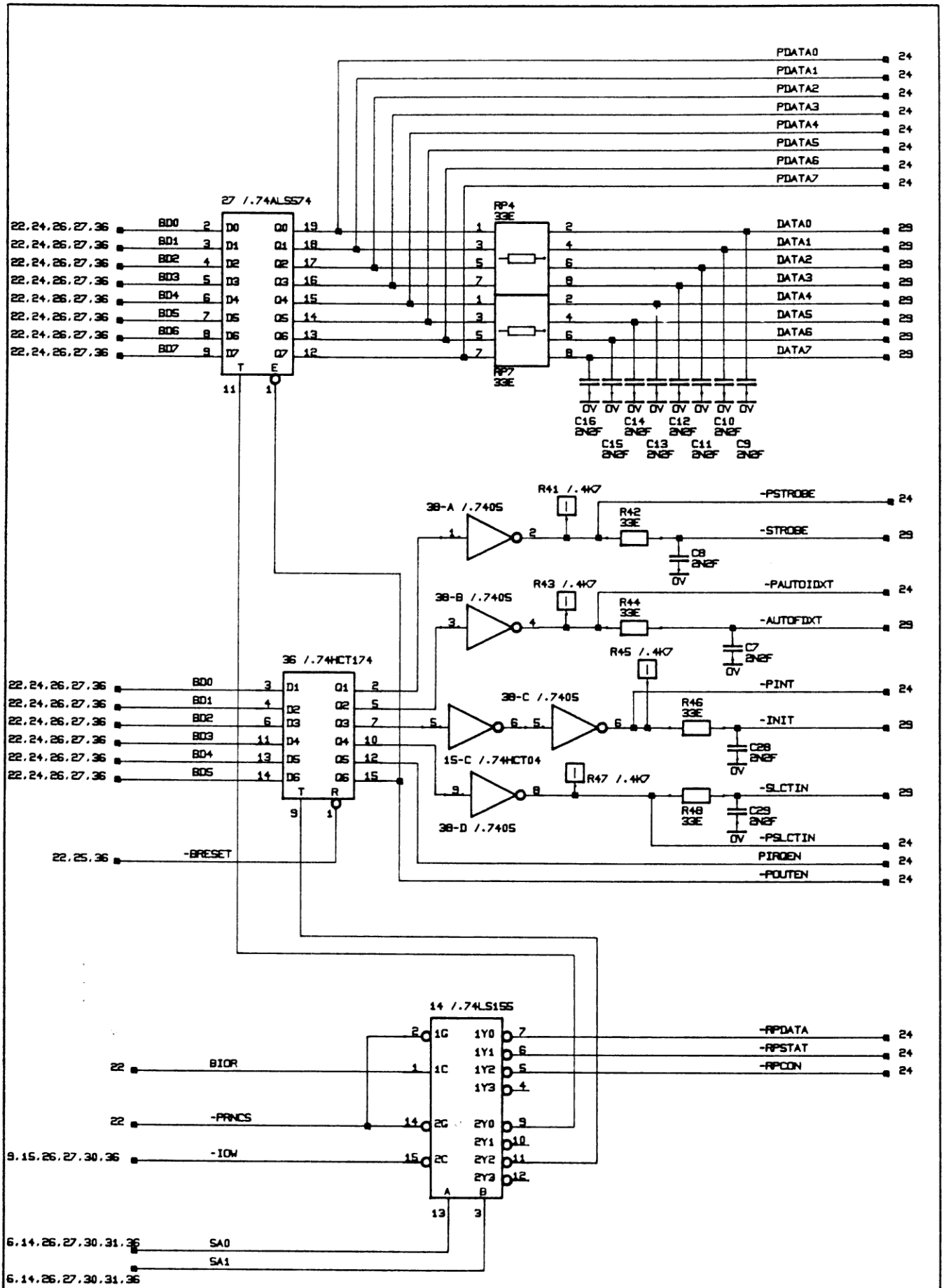
UNIT CPU451	DESIGN PKA	CONTROLS REGISTERS	20
DWG. NO.	DRAWN LIJ 880129		



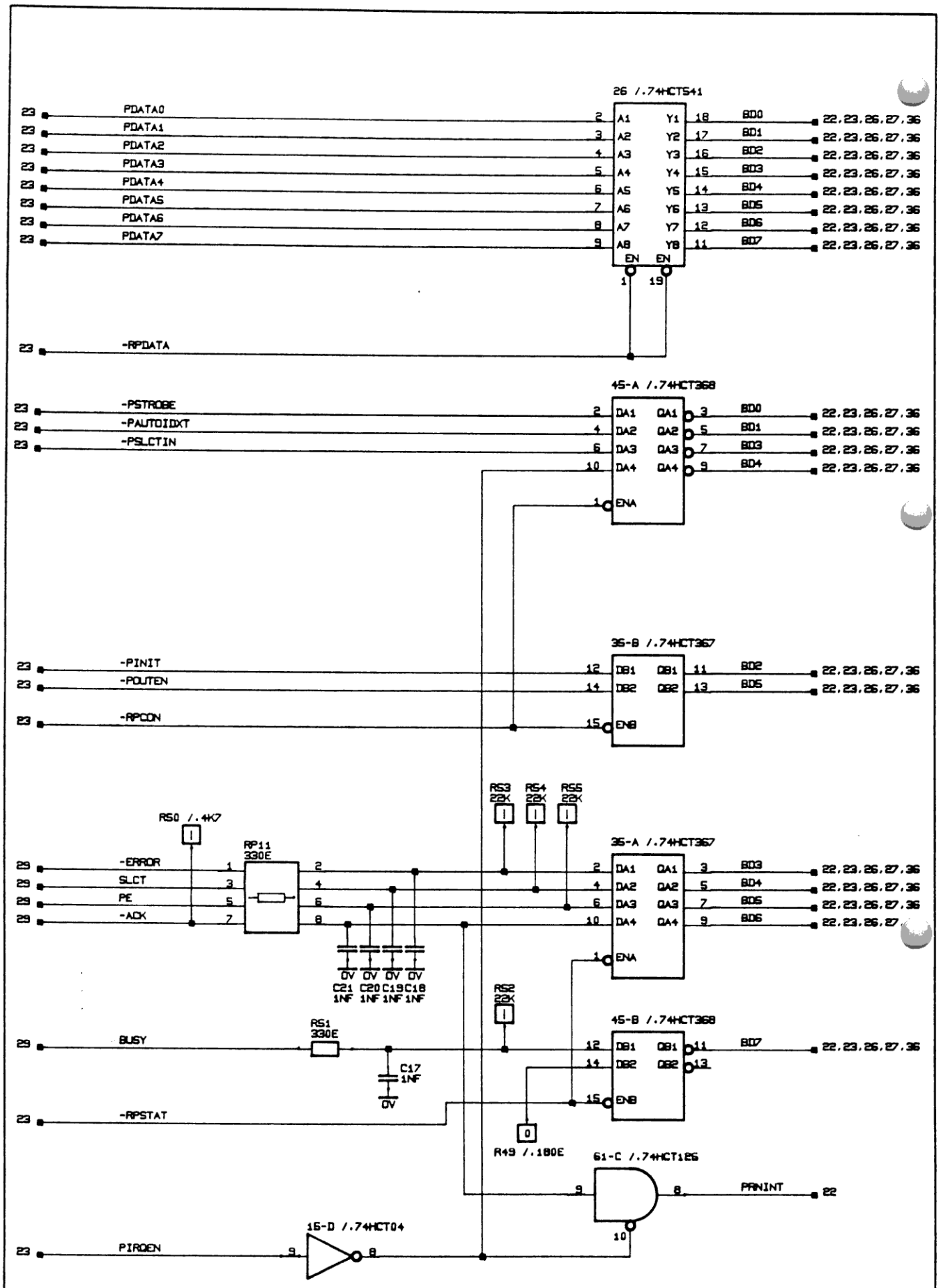
UNIT CPU451	DESIGN PKA	ROM BUFFERS	21
DWG. NO.	DRAWN LIJ 880107		



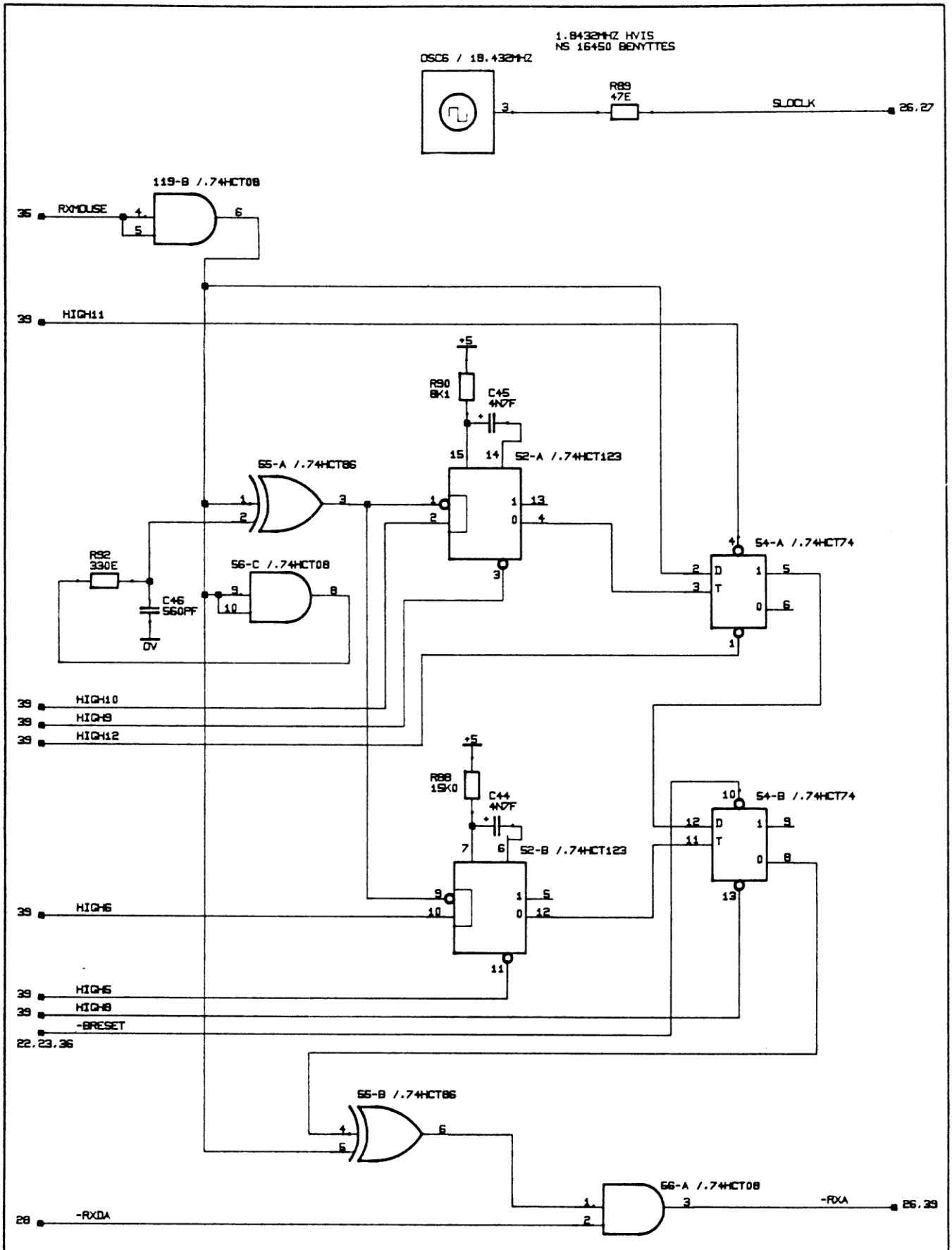
UNIT	DESIGN		
CPU451	MSJ	DATA BUS DRIVER & AT-BUS ADRESS DECODE	22
DWG. NO.	DRAWN AGA 870917		



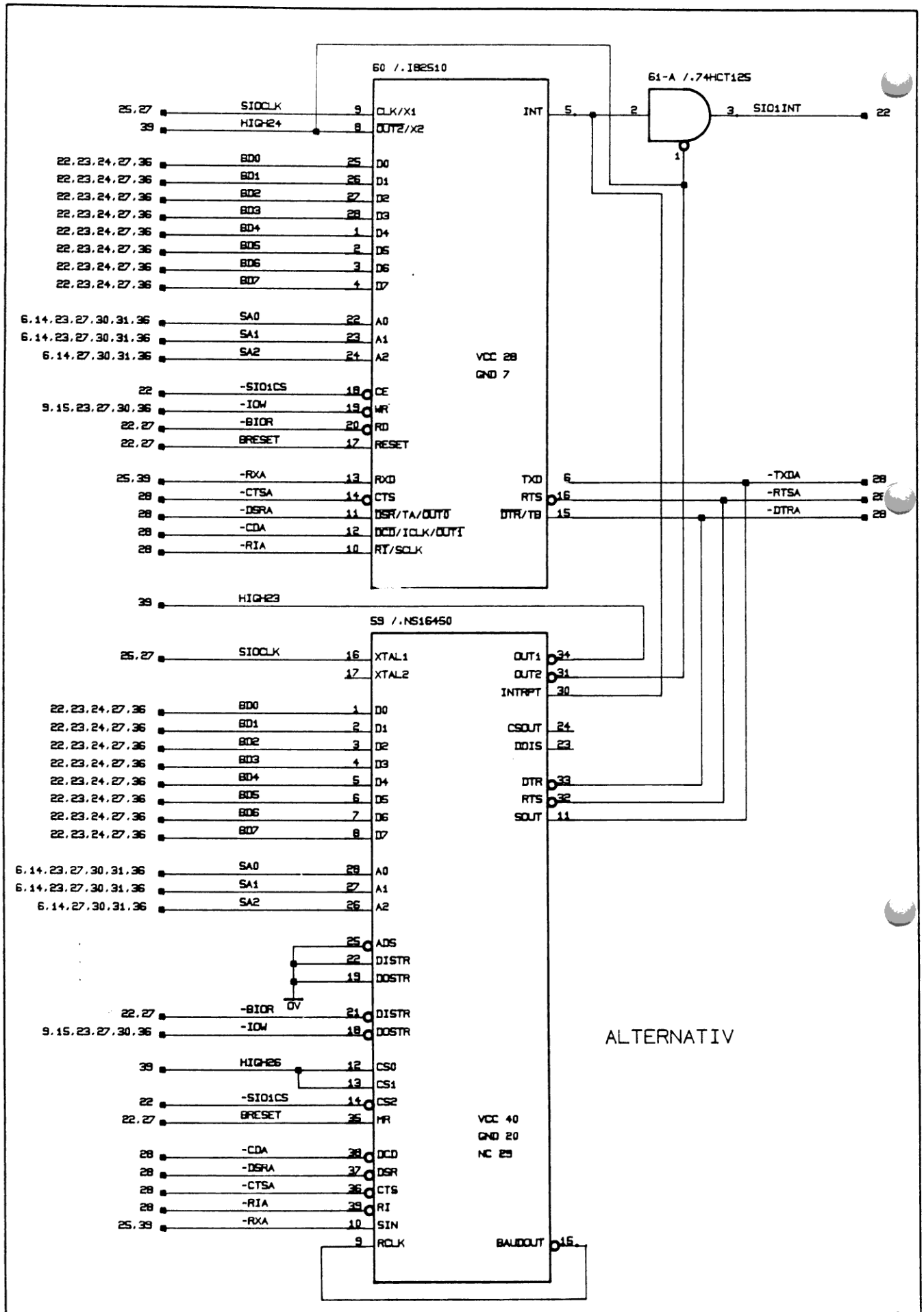
UNIT	DESIGN		
CPU451	WSJ	PRINTER WRITE LATCHES & ADDRESS DECODE	23
DWG. NO.	DRAWN AGA 870925		



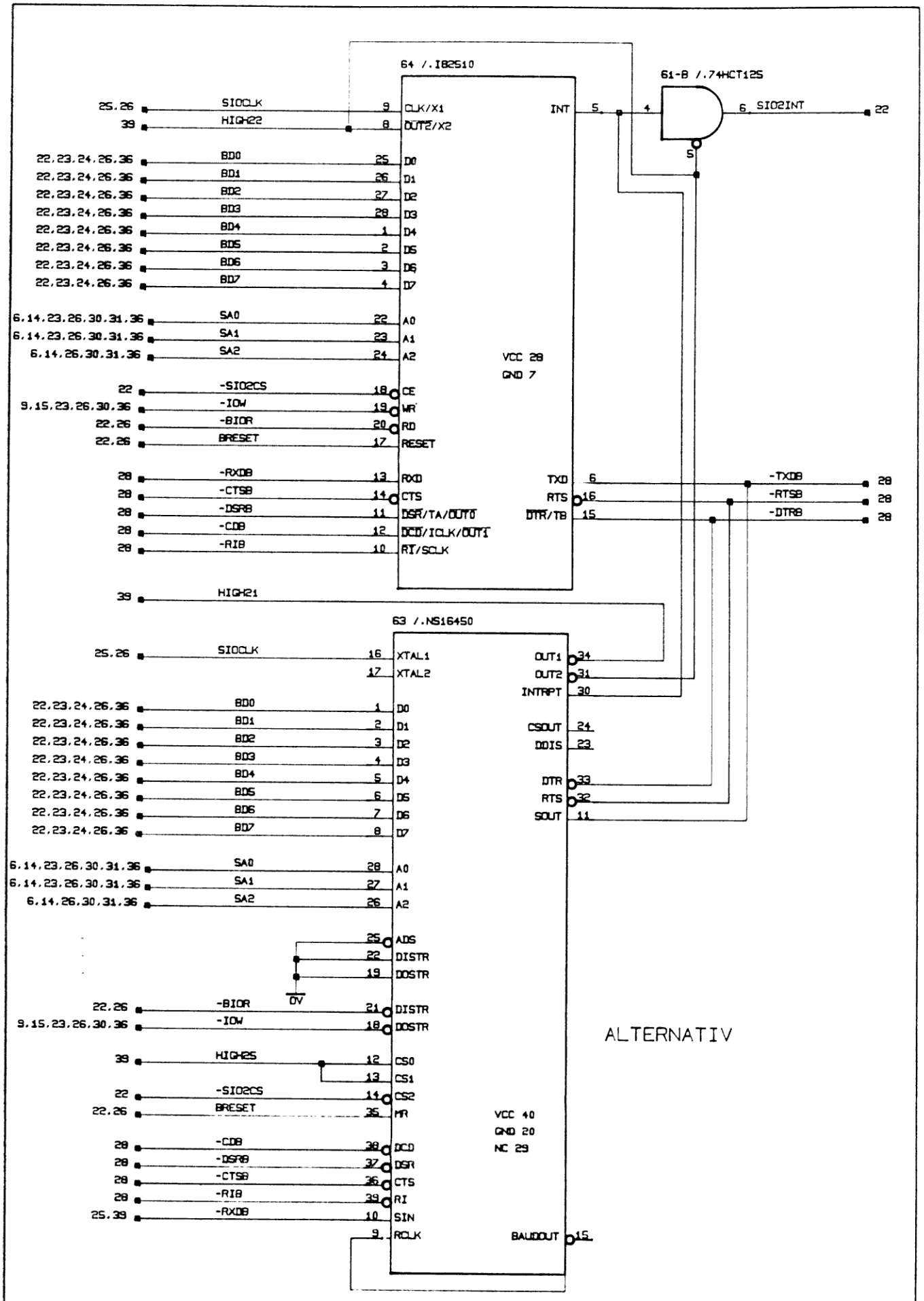
UNIT	DESIGN		
CPU451	WSJ	PRINTER READ-BUFFERE & INTERRUPT CONTROLE	24
DWG. NO.	DRAWN AGA 870928		



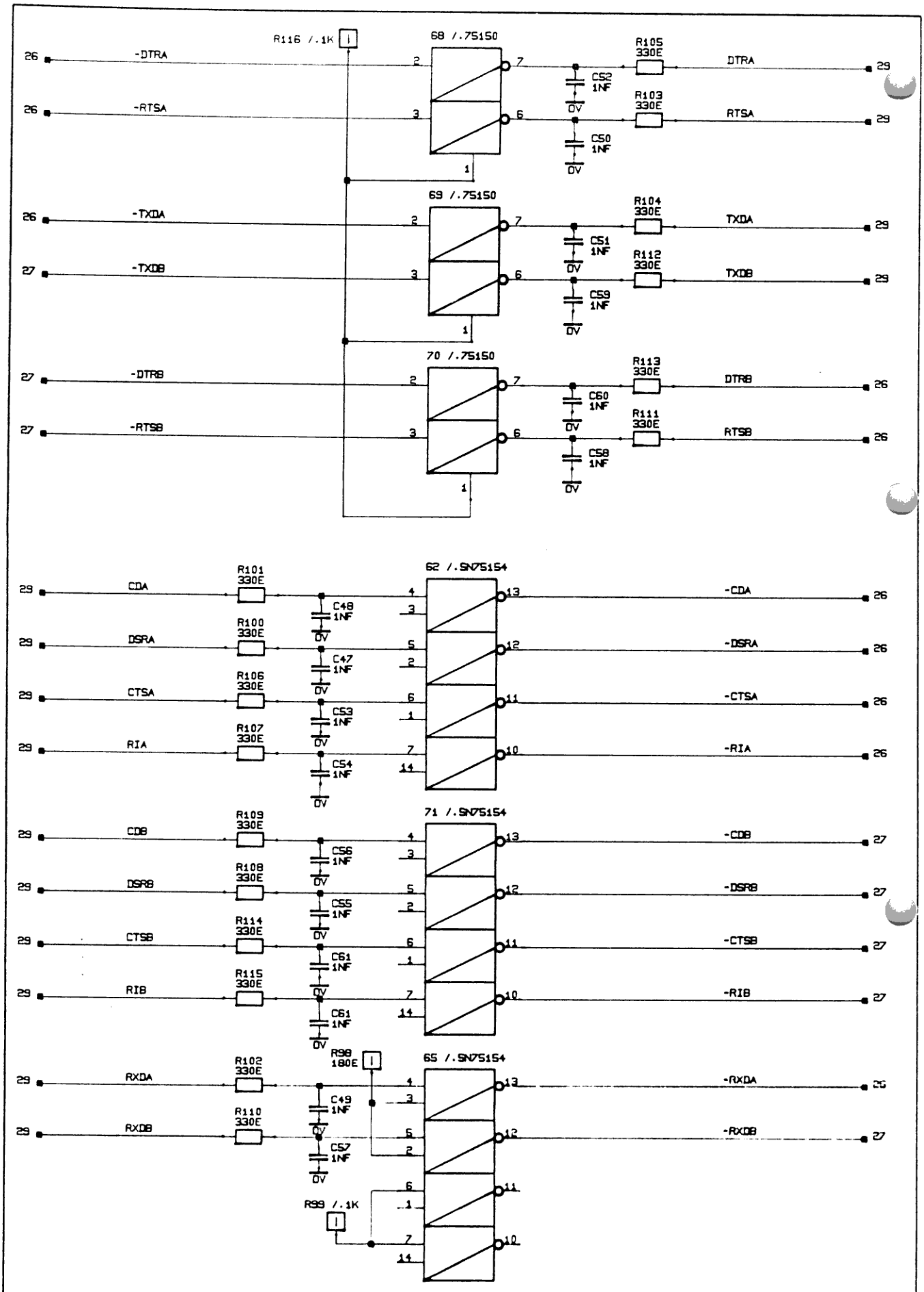
UNIT	DESIGN		
CPU451	MSJ	OSCILLATOR CIRCUIT & MOUSE POLARISATION DETERMIN	25
DWG. NO.	DRAWN ACA 870928		



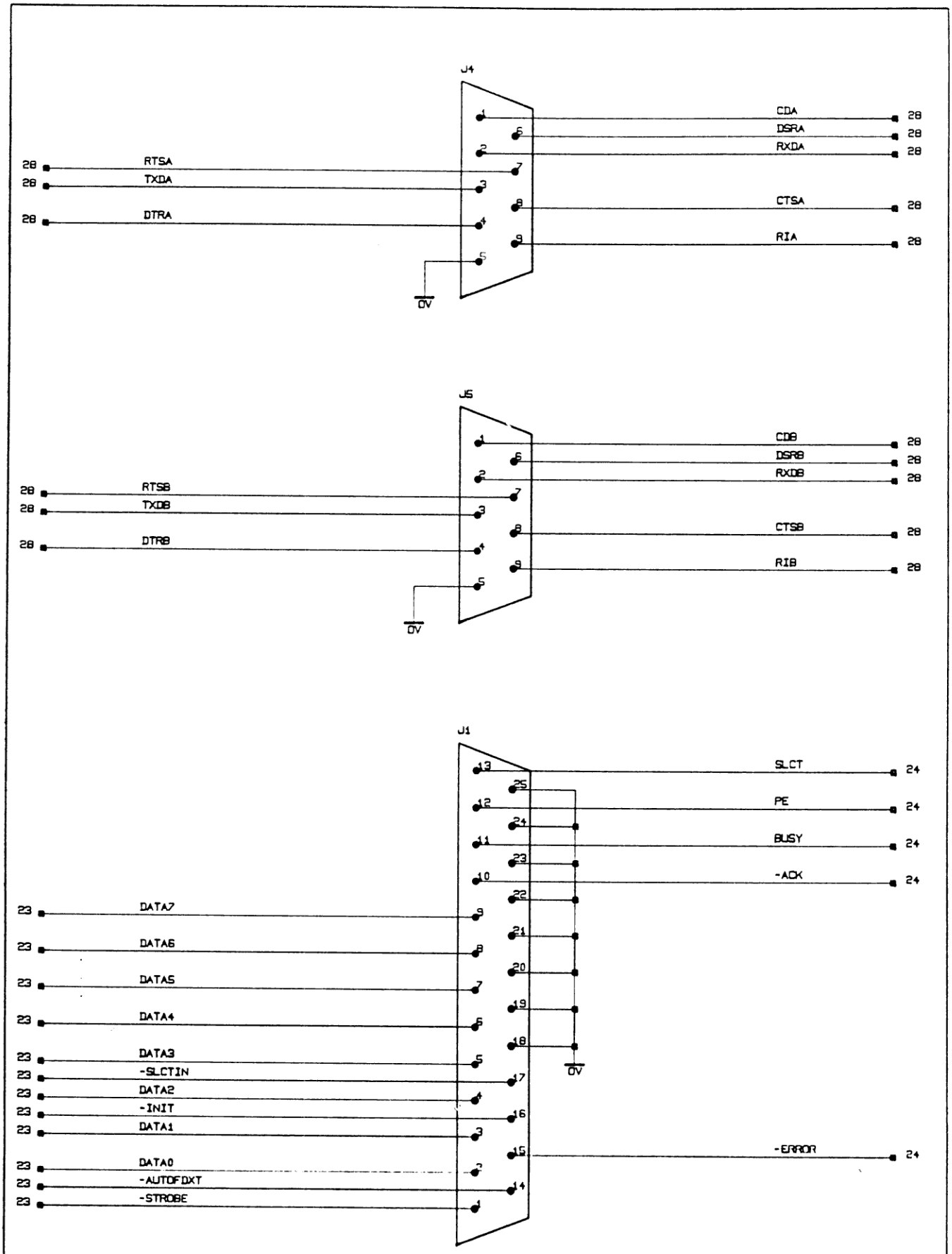
UNIT	DESIGN		
CPU451	WSJ	SIO1	26
DWG. NO.	DRAWN ACA 870928		



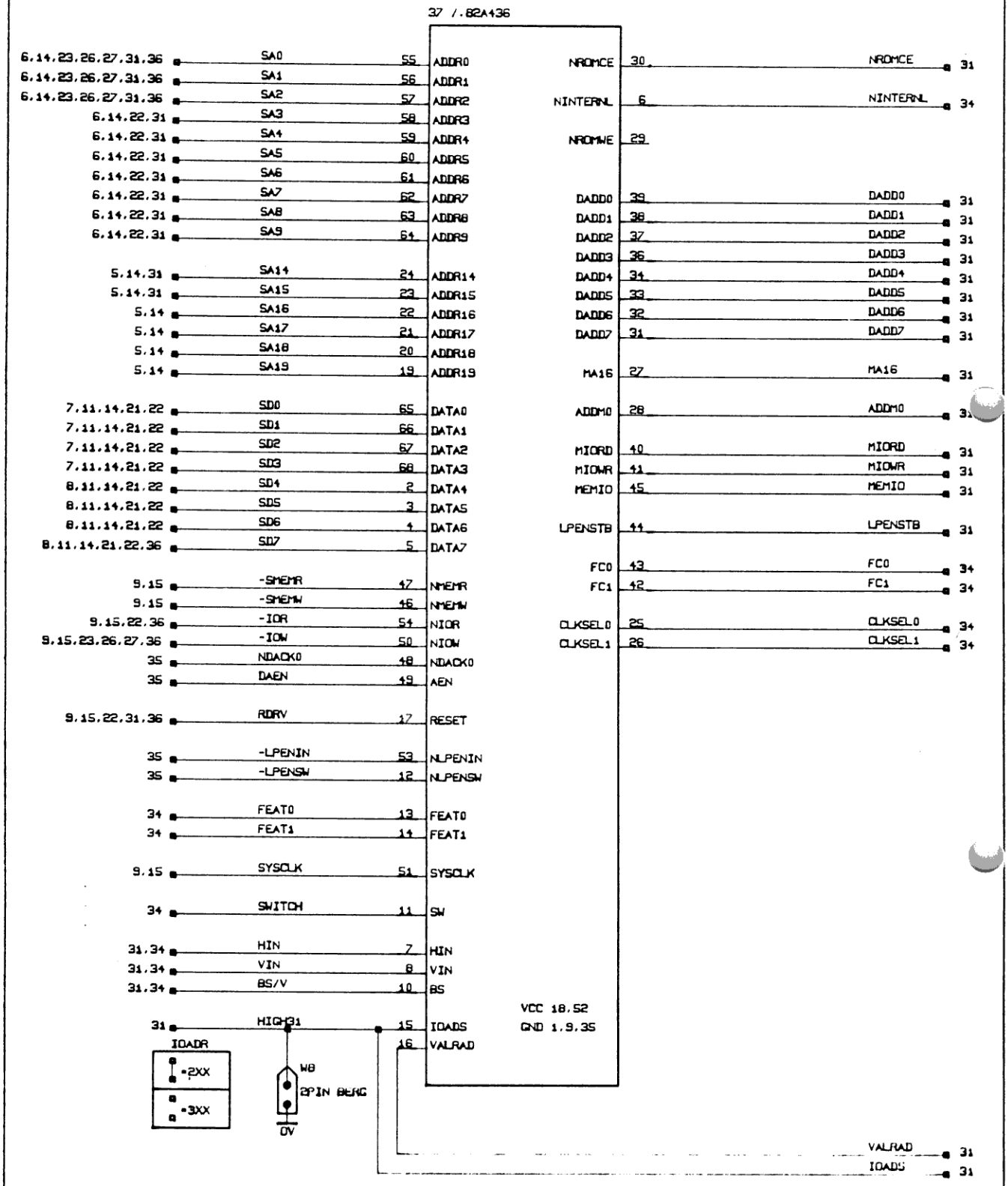
UNIT	DESIGN		
CPU451	WSJ	SIO2	27
DWG. NO.	DRAWN AGA 870930		



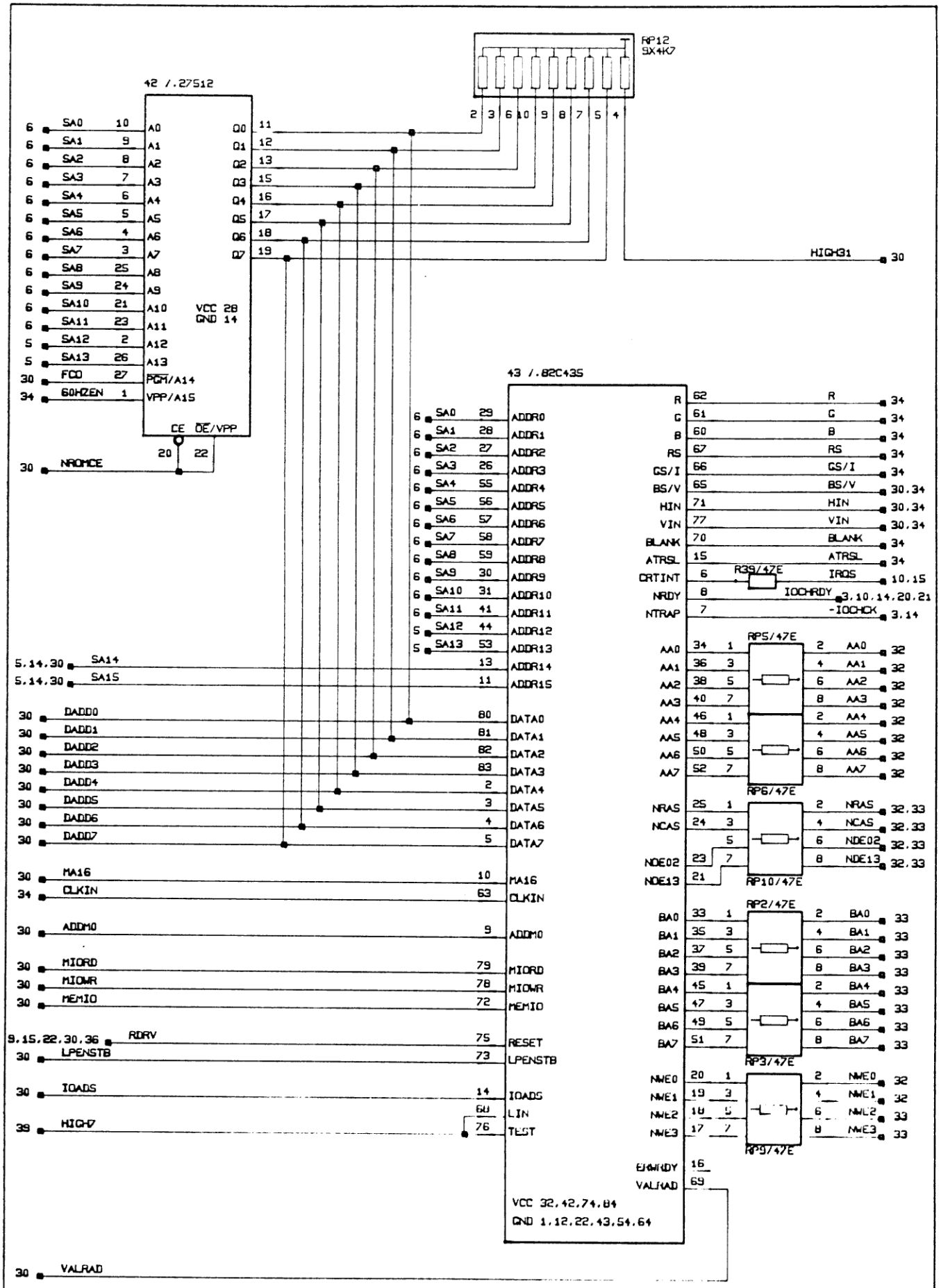
UNIT	DESIGN		
CPU451	WSJ	V24 INTERFACE	28
DWG. NO.	DRAWN AGA 870930		



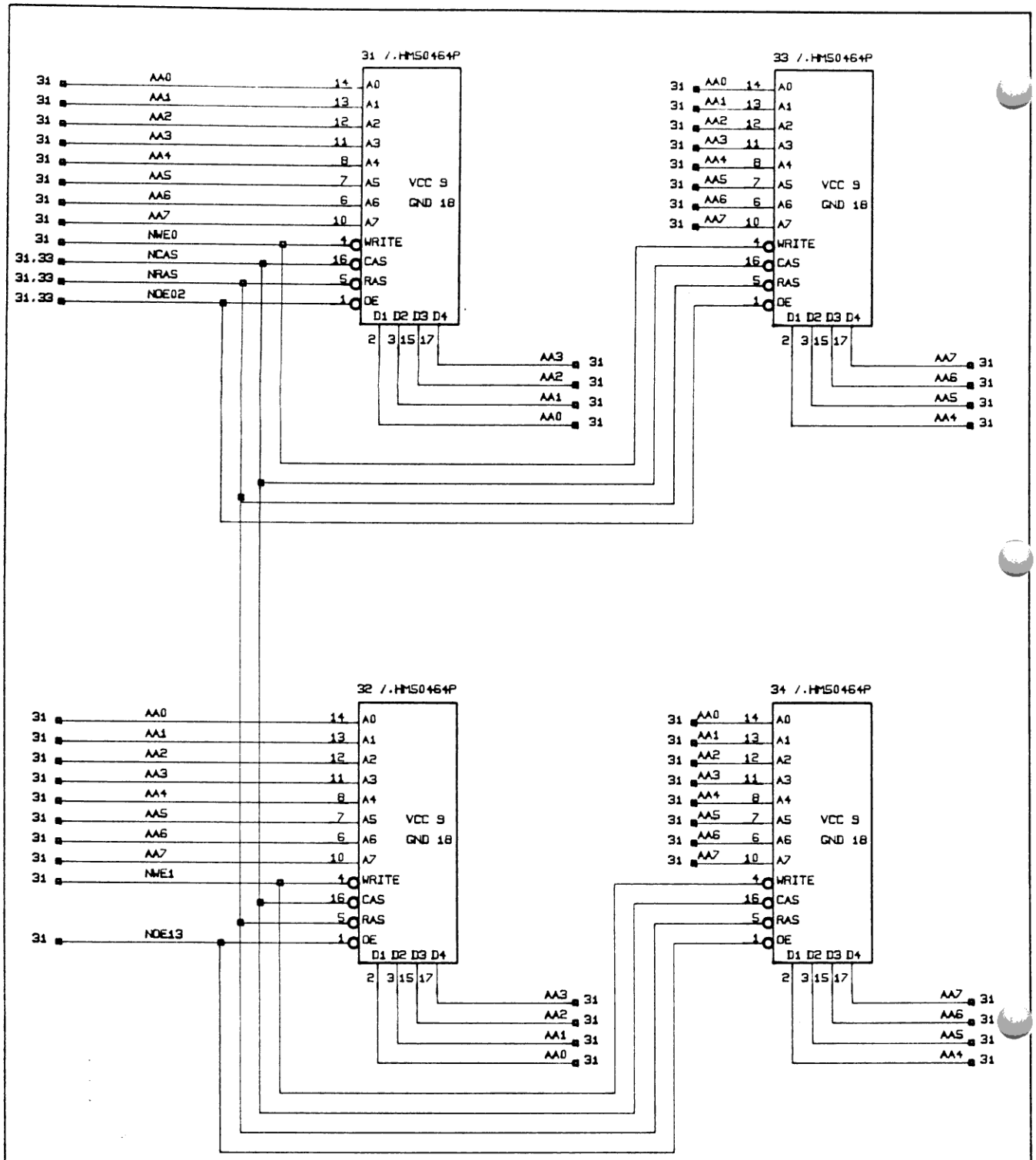
UNIT	DESIGN		
CPU451	WSJ	CONNECTORS	29
DWG. NO.	DRAWN AGA 870930		



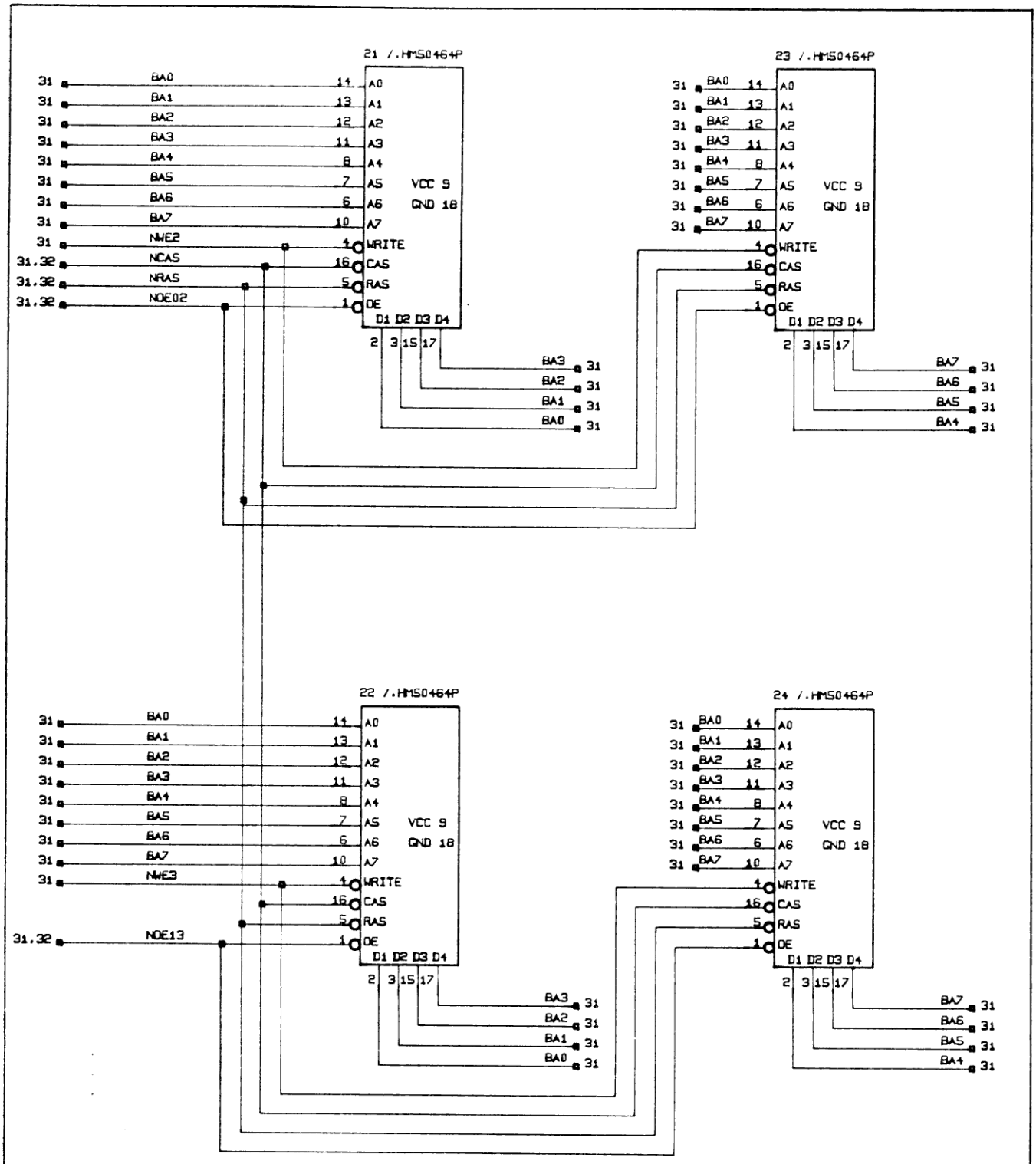
UNIT	DESIGN		
CPU451	JPJ	DISPLAY CONTROLLER BUS INTERFACE	30
DWG. NO.	DRAWN ACA 870930		



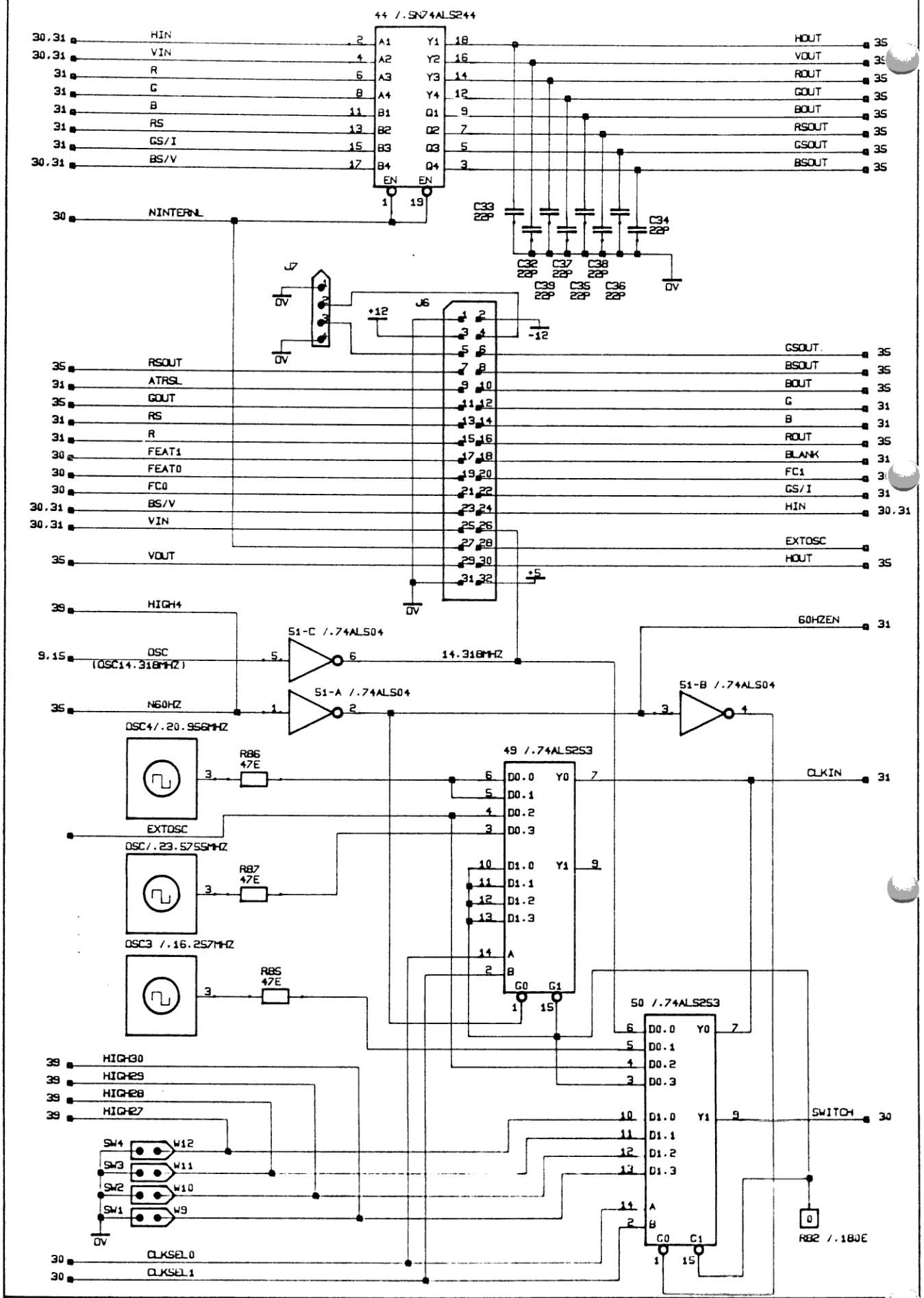
UNIT	DESIGN		
CPU451	JPJ	EGA BIOS PROM & DISPLAY CONTROLLER	31
DWG. NO.	DRAWN AGA 87/0930		



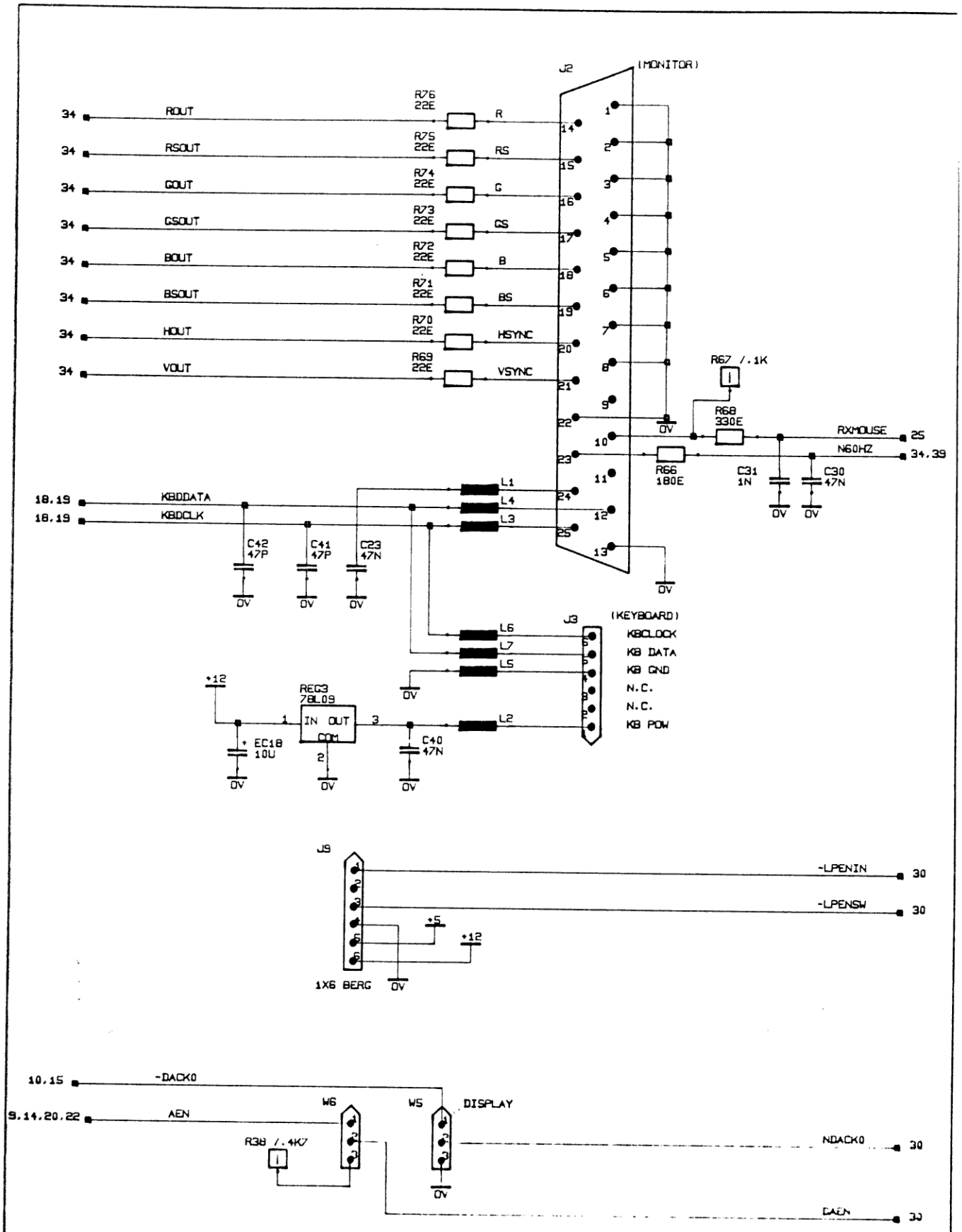
UNIT	DESIGN		
CPU451	JPJ	DISPLAY MEMORY 2 X 128KB	32
DWG. NO.	DRAWN ACA 871001		



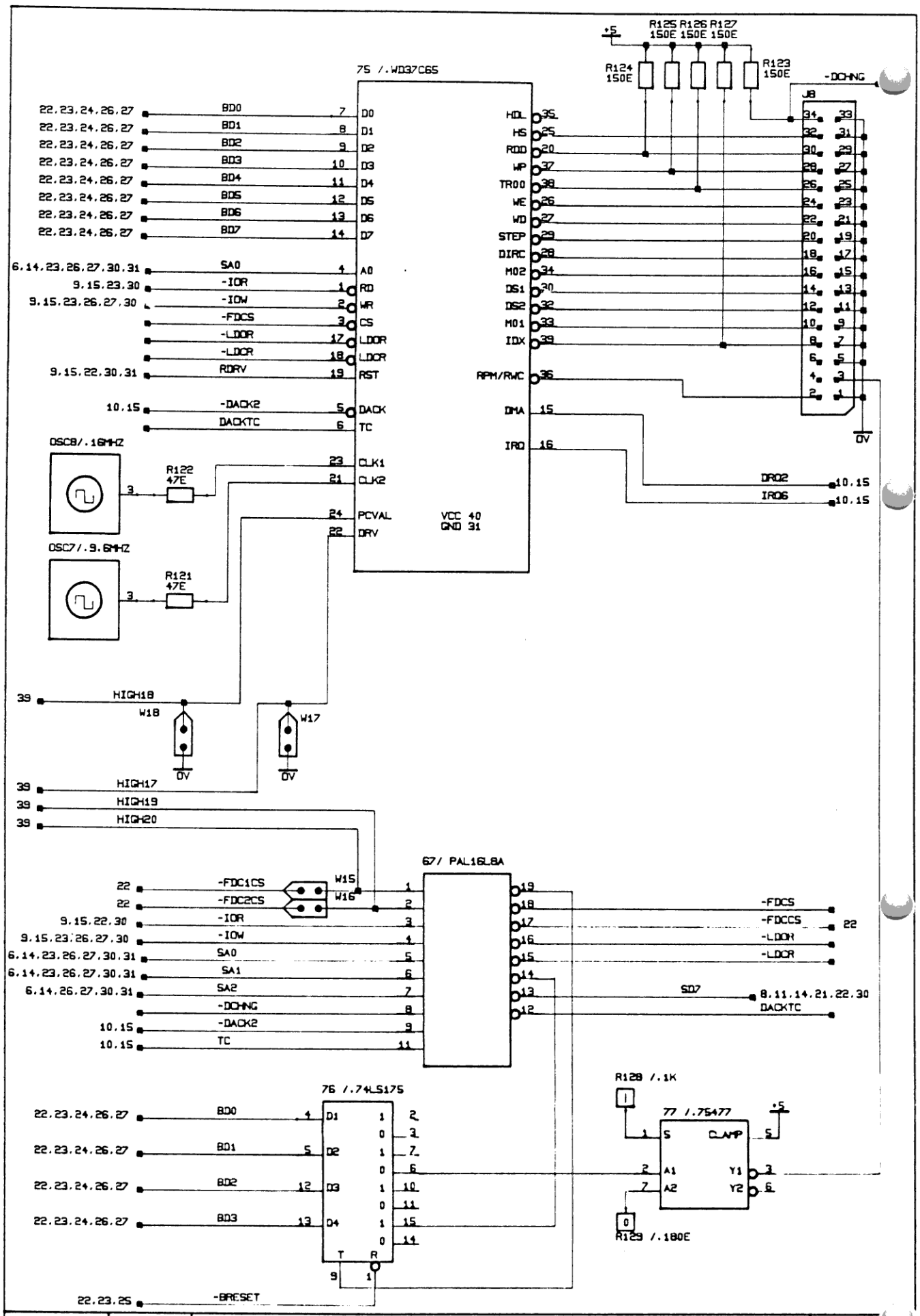
UNIT	DESIGN		
CPU451	JPJ	DISPLAY MEMORY 2 X 128KB	33
DWG. NO.	DRAWN AGA BZ1001		



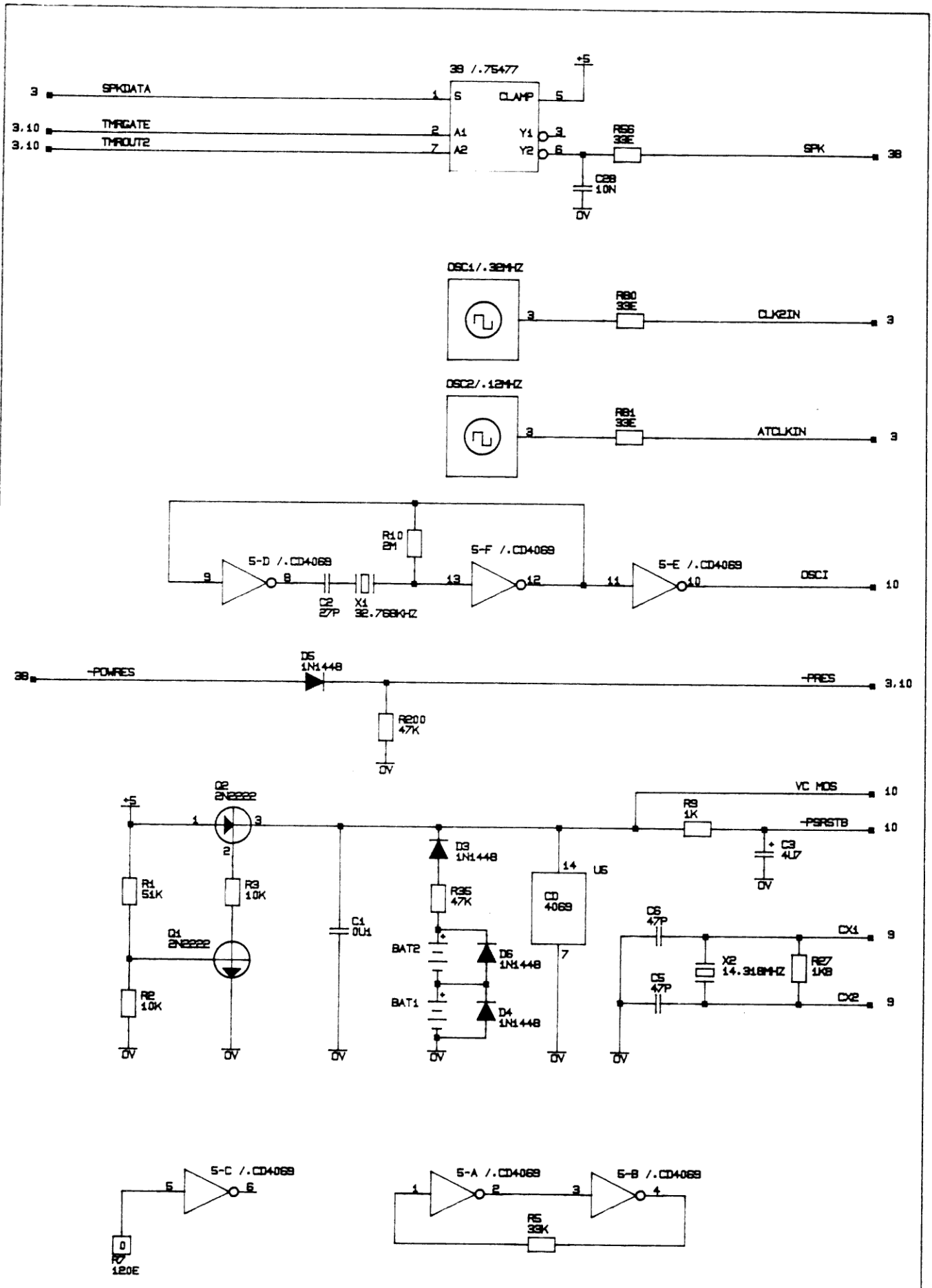
UNIT CPU451	DESIGN JPJ	DISPLAY CONTROLLER, OUTPUT BUFFER, FEATURE CONNECTOR CLOCK OSCILLATORS/SELECTOR	34
DWG. NO.	DRAWN AGA 871001		



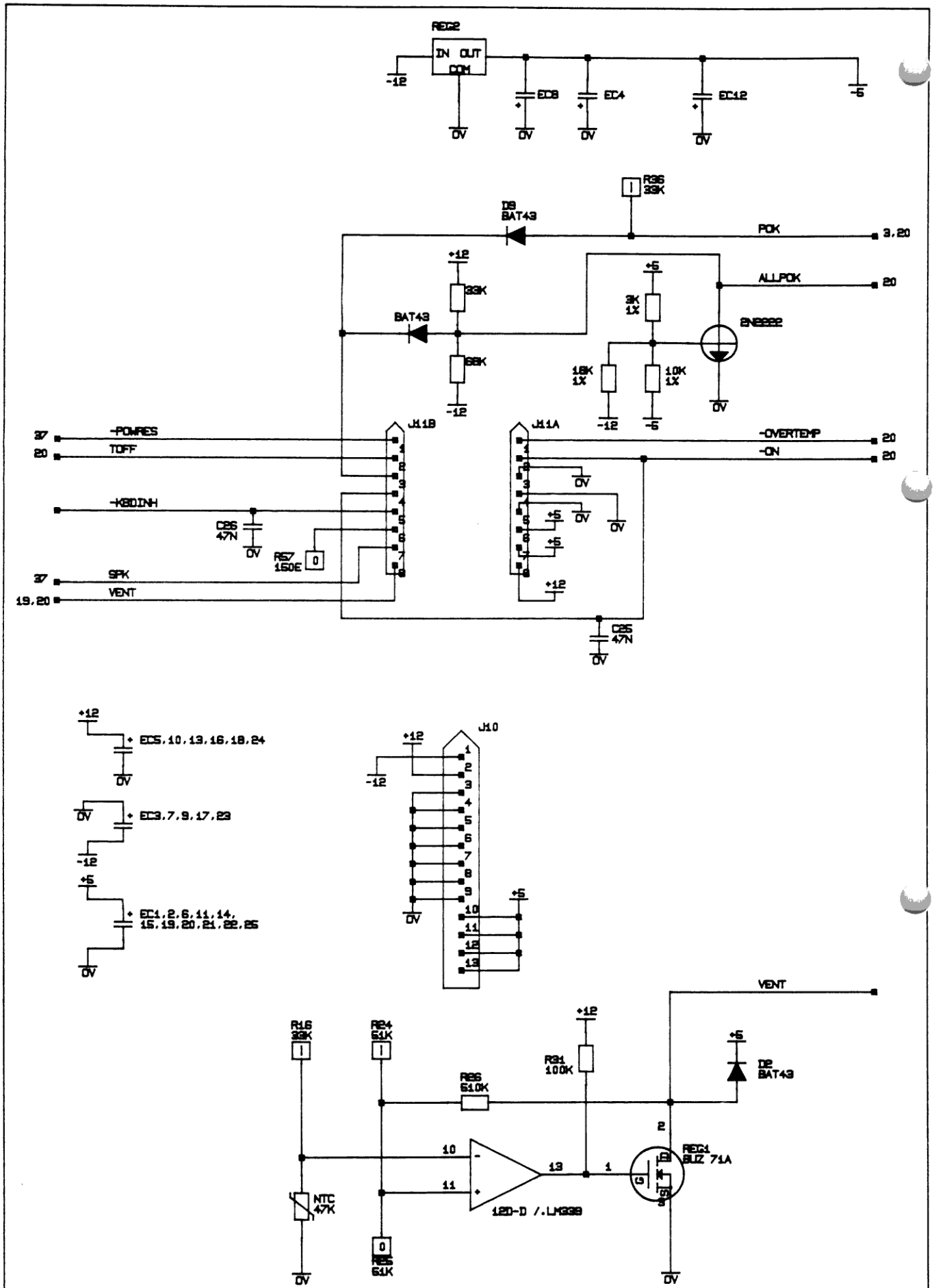
UNIT	DESIGN		
CPU451	JPJ	CONNECTORS FOR MONITOR, KEYBOARD	35
DWG. NO.	DRAWN AGA 871001		



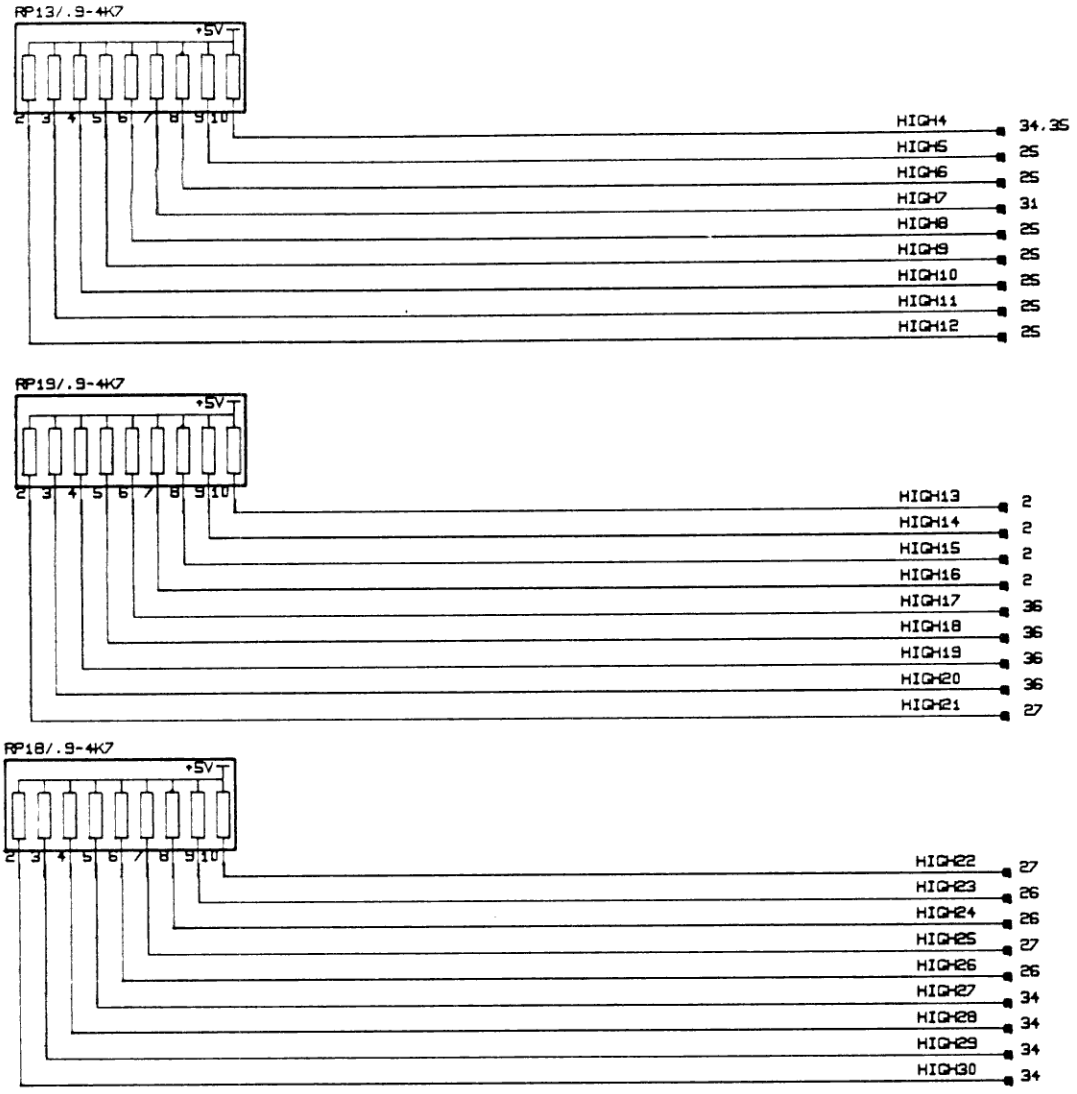
UNIT CPU451	DESIGN JPJ	FLOPPY DISC CONTROLLER	36
DWG. NO.	DRAWN AGA BZ1001		

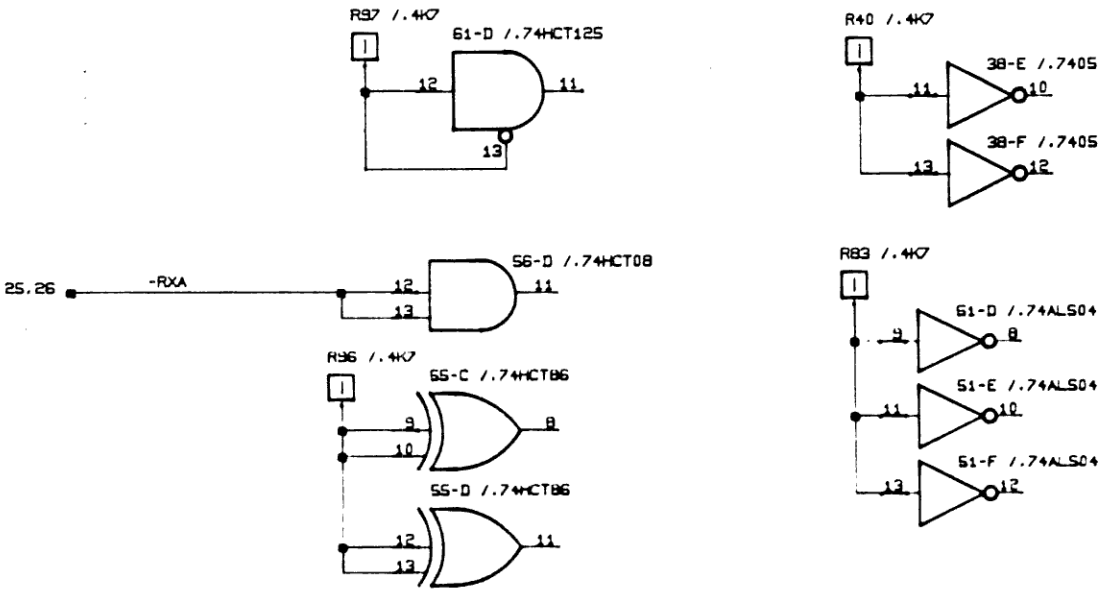


UNIT	DESIGN		
CPU451	PKA	OSCILLATORS, BATTERY	37
DWG. NO.	DRAWN AGA 87/1001		



UNIT	DESIGN		
CPU451	PKA	POWER CONTROL	38
DWG. NO.	DRAWN LIJ 880129		





UNIT	DESIGN		
CPU451	PKA	PULL UP & UNUSED GATES	39
DWG. NO.	DRAWN AGA 871001		

3.4 PAL descriptions

```
Module pal387
Title       'Glue-PAL for i80387 with AT -compability
                                  Author:  Peter Koch Andersson
                                  Edition: 24/9-1987
                                  Revision: 2
                                  A/S Regnecentralen.'

        PAT147 device 'P16L8';

        EMPTY   pin 14; " O   true after first 386-busaccess
                        "      if no i387 is mounted
        !ID     pin 12; " O   indicates the presence of i387 to
                        "      the CPU
        RESET   pin 1;  " I   common i387 and i386 reset
        !ADS    pin 2;  " I   ADdress Strobe from the CPU
        !COERR  pin 3;  " I   -ERROR output from i387
        IR13    pin 19; " O   interrupt request
        !IRinh  pin 13; " X   inhibition of IR13
        !BUSY   pin 17; " I/O i387 busy
        !BUSYen pin 15; " X   internal Busy enable
        PEREQ   pin 18; " I/O i387 data request
        STEN    pin 16; " O   Status enable, disables i387-
                        "      drivers when low.
        !CS287  pin 6;  " I   low when IO add.0E0-0FFH is
                        "      accessed.
        !INTA   pin 4;  " I   Interrupt ack.
        !XIOW   pin 5;  " I   IO write
        !REF    pin 7;  " I   Memory refresh
        !LMEGCS pin 9;  " I   Low, if A(20:31)=0
        true  = 1;
        false = 0;

Equations

        !EMPTY  = (IRinh & ADS) § (!EMPTY & !RESET);

        ID      = IRinh & EMPTY;

        IRinh   = IRinh & !RESET & (ADS § EMPTY)
                § IRinh & COERR
                § !EMPTY & LMEGCS & CS287 & XIOW & !INTA
                § COERR & RESET;

        !STEN   = COERR & BUSY & !IRinh & !RESET & !EMPTY
                § !STEN & BUSYen & !RESET & !EMPTY;

        !IR13   = STEN § EMPTY;

        !PEREQ  = false;
 enable PEREQ   = !STEN;

        BUSYen  = COERR & BUSY & !IRinh & !RESET
                § EMPTY  & !IRinh & !RESET
                § BUSYen & !IRinh & !RESET;
        BUSY    = !EMPTY § REF;
 enable BUSY    = BUSYen;

End
```

```
Module pal387
Title       'Adaptor for i80387 to C&T 386-chipset
                                Author:  Peter Koch Andersson
                                Edition: 14/9-1987
                                Revision:1
                                A/S Regnecentralen.'

        PAT190 device 'P16R6';

"       The adaptor-pal has two missions:
"
"               1: To insert one waitstate in nonpipelined
"                  387-buscycles to ensure fastest transition
"                  to pipelining (The C&T-chipset requires so).
"               2: To generate AF32 when buscycles are for 387.
"                  (AF32 indicates a local buscycle).

        RESET   pin 9;   " I   common i387 and i386 reset
        !ADS    pin 5;   " I   ADdress Strobe from the CPU
        !RDYO   pin 2;   " I   Low,when 80387 is ready for new
                         "     buscycel.
        !NPS1   pin 3;   " I   Num.processor select.
        NPS2    pin 4;   " I   Num.processor select.
        !RDY    pin 12;  " I/O Tristate connection to !Ready.
        !AF32   pin 19;  " O   Tristate connection to !AF32 on
                         "     the systemboard.
        SCLK    pin 14;  "     Phase counter syncronous with
                         "     Systemclk.
        !IDLE   pin 15;  "     Active when the 386bus is idle.
        !NPS    pin 16;  "     Active when the NP is selected
                         "     until rdy is active.
        !NPD    pin 17;  "     Active one SCLK after the activation
                         "     of NPS, until RDY inactive.
        !RDYFF  pin 18;  "     Used to gate RDY out.
        !AFG    pin 13;  "     Delayed NPD.
        true  = 1;
        false = 0;

Equations
        !SCLK   :=SCLK & !RESET;

        IDLE    :=RDY & !ADS & SCLK
                § IDLE & !ADS
                § IDLE & !SCLK
                § RESET;

        NPS     :=NPS1 & NPS2 & ADS & IDLE & SCLK
                § NPS1 & NPS2 & ADS &  RDY & SCLK
                § NPS & !RDYFF
                § NPS & !NPD;

        NPD     :=NPS & SCLK
                § NPD & NPS;

        AF32    = NPS & !AFG;
enable  AF32    = NPS;

        RDY     = RDYFF & NPD;
enable  RDY     = RDYFF;

        RDYFF   :=NPD & SCLK
                § NPD & RDYFF;

        AFG     :=NPD & NPS;
End
```

```
MODULE  PT118

TITLE   'CPU 451 ADDR DEKODER FOR WD37C65,
           JPJ , Regnecentralen A/S,Ballerup'

PAT118  DEVICE  'P16L8' ;

        nfdc1cs, nfdc2cs  PIN  1,2 ;
        nior, niow        PIN  3,4 ;
        sa0,sa1,sa2       PIN  5,6,7 ;
        ndchng,ndack2,tc  PIN  8,9,11 ;
        dacktc,sd7        PIN  12,13  ;
        dmaen,nwror       PIN  14,19  ;
        n1dor,n1dcr       PIN  16,15  ;
        nfdcs,nfdccs      PIN  18,17 ;

        H,L,X,C,Z         = 1,0,.x.,.c.,.z.;

        input   = Ænfdc1cs,nfdc2cs,sa2,sa1,sa0,
                  nior,niow,dmaen,ndchng,ndack2,tcÅ;
        output = Ænfdcs,nfdccs,n1dor,n1dcr,nwror,dacktc,sd7 Å ;

EQUATIONS

        ENABLE  nfdcs = H;
        ENABLE  nfdccs = H;
        ENABLE  n1dor = H;
        ENABLE  n1dcr = H;
        ENABLE  dmaen = L;
        ENABLE  nwror = H;
        ENABLE  dacktc = H;
        ENABLE  sd7    = !n1dcr & !nior ;


        sd7     = !ndchng ;
        !nfdcs  = (!nfdc1cs § !nfdc2cs) & sa2 & !sa1 ;
        !nfdccs = !nfdc1cs & !sa2 & sa1 & !sa0
                § !nfdc2cs & !sa2 & sa1 & !sa0
                § !nfdc1cs &  sa2 & !sa1
                § !nfdc2cs &  sa2 & !sa1
                § !nfdc1cs &  sa2 & sa1 & sa0 & !niow
                § !nfdc2cs &  sa2 & sa1 & sa0 & !niow
                § !ndack2  &  dmaen ;
        !n1dcr  = (!nfdc1cs § !nfdc2cs) & sa2 & sa1 & sa0 ;
        !n1dor  = (!nfdc1cs § !nfdc2cs) &!sa2 & sa1 &!sa0 ;
        !nwror  = (!nfdc1cs § !nfdc2cs) &!sa2 & sa1 &!sa0 &!niow;
        dacktc  = tc & !ndack2 ;
```

```
test_vectors in PAT118
    (Ænfdc1cs,nfdc2cs,nior,niow,sa0,sa1,sa2,
      ndchng,ndack2,tc,sd7,dmaenÅ ->
     Ædacktc,sd7,dmaen,n1dcr,n1dor,nfdccs,nfdcs,nwrorÅ)
Æ1,1,0,1,0,0,1,0,1,1,1,0Å -> Æ.X.,.X.,.X.,.X.,.X.,1,.X.,.X.Å;
Æ1,1,0,1,0,0,1,0,1,1,1,0Å -> Æ.X.,.X.,.X.,.X.,.X.,.X.,1,.X.Å;
Æ1,1,0,1,0,0,1,0,1,1,1,0Å -> Æ.X.,.X.,.X.,.X.,.X.,.X.,1,.X.Å;
Æ1,1,0,1,0,0,1,0,1,1,1,0Å -> Æ.X.,.X.,.X.,.X.,.X.,1,.X.,.X.Å;
Æ0,1,1,0,1,0,1,1,0,0,0,0Å -> Æ.X.,.X.,.X.,.X.,.X.,0,.X.,.X.Å;
Æ1,0,1,0,0,1,0,1,0,0,0,0Å -> Æ.X.,.X.,.X.,.X.,.X.,0,.X.,.X.Å;
Æ1,1,1,0,1,1,1,1,0,0,0,0Å -> Æ0,.X.,.X.,1,.X.,1,.X.,.X.Å;
Æ0,1,0,0,0,1,0,1,1,1,0,1Å -> Æ.X.,.X.,.X.,.X.,.X.,.X.,.X.,0Å;
Æ0,1,0,0,0,1,0,1,1,1,0,1Å -> Æ.X.,.X.,.X.,.X.,.X.,0,.X.,.X.Å;
Æ0,1,0,0,0,1,0,1,1,1,0,1Å -> Æ.X.,.X.,.X.,.X.,0,.X.,.X.,.X.Å;
Æ0,1,0,0,1,1,1,1,1,1,0,1Å -> Æ.X.,0,.X.,.X.,.X.,.X.,.X.,.X.Å;
Æ0,1,0,0,1,1,1,1,1,1,0,1Å -> Æ.X.,.X.,.X.,0,.X.,.X.,.X.,.X.Å;
Æ0,1,1,0,1,0,1,1,1,0,0,1Å -> Æ.X.,.X.,.X.,.X.,.X.,.X.,0,.X.Å;
Æ0,0,1,0,0,0,0,1,1,0,0,1Å -> Æ.X.,.X.,.X.,.X.,.X.,1,.X.,.X.Å;
Æ1,0,1,0,1,0,1,1,1,0,0,1Å -> Æ.X.,.X.,.X.,.X.,.X.,0,.X.,.X.Å;
Æ0,1,1,0,1,1,1,1,1,1,0,0,1Å -> Æ.X.,.X.,.X.,.X.,.X.,0,.X.,.X.Å;
Æ1,0,1,0,1,1,1,1,1,1,0,0,1Å -> Æ.X.,.X.,.X.,.X.,.X.,0,.X.,.X.Å;
Æ0,0,1,1,1,1,1,1,1,1,0,0,1Å -> Æ.X.,.X.,.X.,.X.,.X.,1,.X.,.X.Å;
Æ0,0,1,0,1,1,0,1,1,0,0,1Å -> Æ.X.,.X.,.X.,.X.,.X.,1,.X.,.X.Å;
Æ0,0,0,0,0,1,0,1,1,0,.X.,1Å -> Æ.X.,.Z.,.X.,.X.,.X.,.X.,.X.,.X.Å;
Æ1,0,0,0,0,1,0,1,0,1,1,1Å -> Æ.X.,.X.,.X.,.X.,.X.,.X.,.X.,0Å;
Æ1,0,0,0,1,0,1,1,0,1,1,1Å -> Æ.X.,.X.,.X.,.X.,.X.,.X.,0,.X.Å;
Æ0,0,0,0,0,0,0,1,0,1,1,1Å -> Æ.X.,.X.,.X.,.X.,1,0,1,1Å;
Æ0,1,0,0,1,0,1,1,0,1,1,1Å -> Æ.X.,.X.,.X.,1,.X.,.X.,.X.,.X.Å;
Æ1,0,0,0,1,0,1,1,0,1,1,1Å -> Æ.X.,.X.,.X.,1,.X.,.X.,.X.,.X.Å;
Æ1,0,0,0,0,1,0,1,0,1,1,1Å -> Æ.X.,.X.,.X.,.X.,0,.X.,.X.,.X.Å;
Æ1,0,0,0,1,0,1,1,1,0,1,0Å -> Æ.X.,0,.X.,0,.X.,.X.,.X.,.X.Å;
Æ0,0,0,0,1,1,0,1,0,1,1,1Å -> Æ.X.,.X.,.X.,1,1,.X.,.X.,1Å;
Æ0,0,0,1,0,1,0,1,1,1,1,1Å -> Æ0,.X.,.X.,.X.,.X.,.X.,.X.,1Å;
Æ1,1,0,0,0,1,0,1,1,0,1,1Å -> Æ.X.,.X.,.X.,.X.,1,1,.X.,1Å;
Æ0,0,0,0,0,1,1,1,1,0,1,1,0Å -> Æ.X.,.X.,.X.,1,1,1,1,1Å;
Æ1,0,1,0,1,1,1,1,1,0,1,.X.,1Å -> Æ.X.,.Z.,.X.,.X.,.X.,.X.,.X.,.X.Å;
Æ1,0,0,0,1,1,1,1,0,0,1,1,1Å -> Æ1,1,.X.,.X.,.X.,.X.,.X.,.X.Å;

END PT118
```

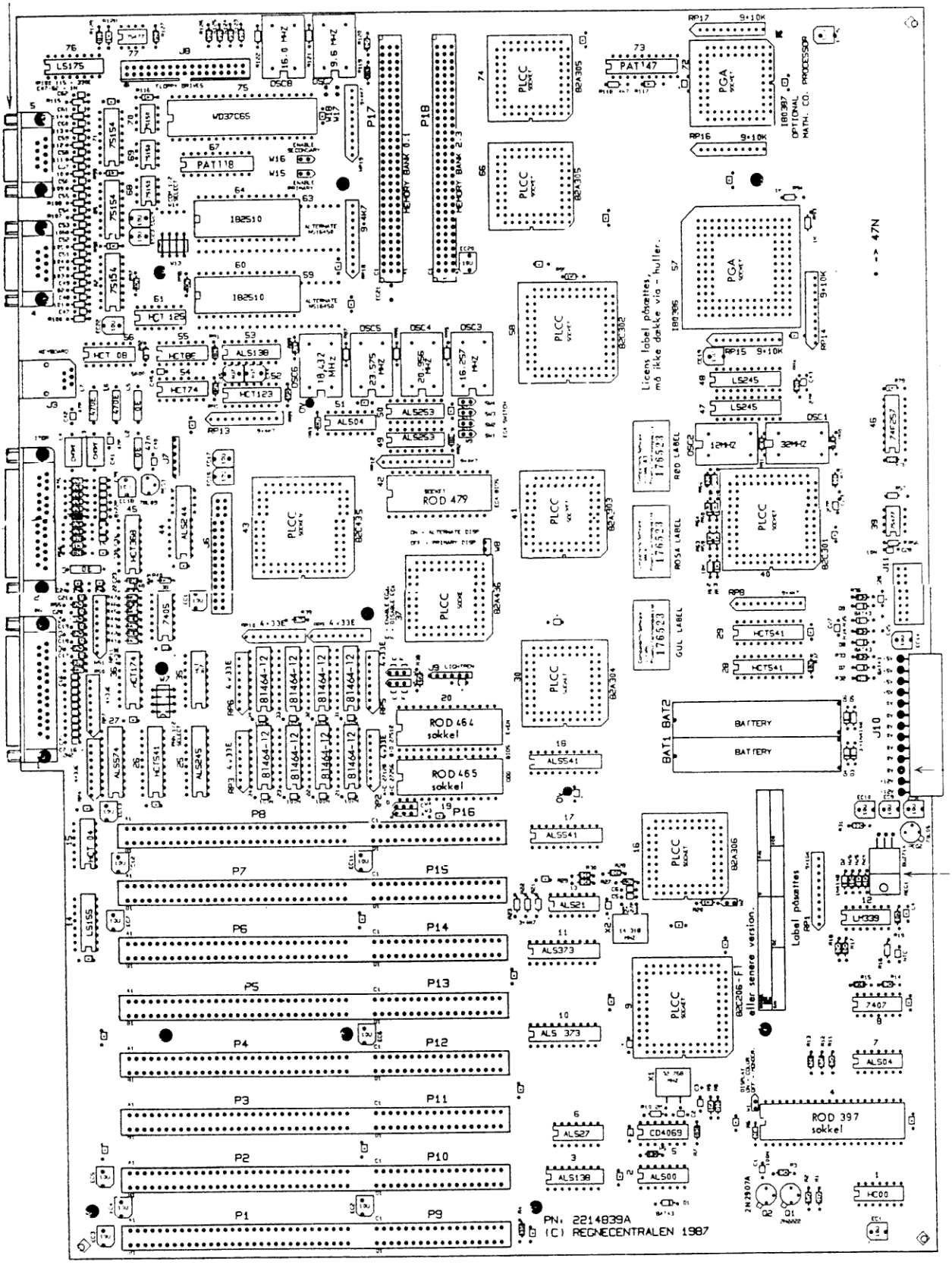
```
module PRQ;

title 'PEREQ gating for 80386 Paging/coproc. error
                Author  : Jens Peter Jakobsen
                Edition : 870921
                Revision: 0
                A/S Regnecentralen.'

PAT193 DEVICE 'P16R8';  " must be type 16R8B

"The adaptor pal monitors 80386 bus activity and
"ensures that the prefetch queue is full before
"a PEREQ is passed on to the 80386.
"The circuit assumes the prefetch queue is full
"when 8 idle bus cycles have been counted.

H,L,C,X = 1,0,.C.,.X.;

        GND     PIN 10;
        VCC     PIN 20;
        !OE     PIN 11;

        CLK2    PIN  1; "I 80386 CLK2
        RESET   PIN  4; "I HIGH DURING RESET
        !ADS    PIN  2; "I LOW TO BEGIN BUS CYCLES
        !READY  PIN  3; "I LOW TO END BUS CYCLES
        HLDA    PIN  8; "I HIGH DURING HOLD ACKNOWLEDGE
        PEREQ   PIN  5; "I HIGH DURING COPROC. OP. TRANSFERS
        NC1     PIN  6; "  UNUSED INPUT
        NC2     PIN  7; "  UNUSED INPUT
        NC3     PIN  9; "  UNUSED INPUT

        PEREQOUT        PIN 19; "O GATED PEREQ TO PROCESSOR
        NCOUT1  PIN 18; "O UNUSED
        SCLK    PIN 17; "O LOW DURING PHASE 1, HIGH DURING PH. 2
        NCOUT2  PIN 16; "O UNUSED
        !IDLE   PIN 15; "O LOW WHEN BUS ACTIVE
        ICNT0   PIN 14; "O IDLE COUNTER BIT 0
        ICNT1   PIN 13; "O IDLE COUNTER BIT 1
        ICNT2   PIN 12; "O IDLE COUNTER BIT 2

        INUSE   =Æ1,1,1Å;
        IDLE2   =Æ0,1,1Å;
        IDLE3   =Æ1,0,1Å;
        IDLE4   =Æ1,1,0Å;
        IDLE5   =Æ0,0,1Å;
        IDLE6   =Æ1,0,0Å;
        IDLE7   =Æ0,1,0Å;
        IDLE8   =Æ0,0,0Å;
```

```
EQUATIONS

        !SCLK    :=SCLK & !RESET;

        IDLE     := READY & !ADS & SCLK
                    §IDLE & !ADS
                    §IDLE & !SCLK
                    §RESET ;

" IDLE CYCLE COUNTER

STATE_DIAGRAM ÆICNT0,ICNT1,ICNT2Å

STATE INUSE:              "BUS IN USE, OR IDLE 1 CLOCK
        IF (IDLE & !ADS & !HLDA & SCLK) THEN IDLE2
        ELSE INUSE;

STATE IDLE2:              " 2 CLOCKS IDLE
        IF (IDLE & !ADS & !HLDA & SCLK) THEN IDLE3
        ELSE IF (SCLK) THEN INUSE
        ELSE IDLE2;

STATE IDLE3:              " 3 CLOCKS IDLE
        IF (IDLE & !ADS & !HLDA & SCLK) THEN IDLE4
        ELSE IF (SCLK) THEN INUSE
        ELSE IDLE3;

STATE IDLE4:              " 4 CLOCKS IDLE
        IF (IDLE & !ADS & !HLDA & SCLK) THEN IDLE5
        ELSE IF (SCLK) THEN INUSE
        ELSE IDLE4;

STATE IDLE5:              " 5 CLOCKS IDLE
        IF (IDLE & !ADS & !HLDA & SCLK) THEN IDLE6
        ELSE IF (SCLK) THEN INUSE
        ELSE IDLE5;

STATE IDLE6:              " 6 CLOCKS IDLE
        IF (IDLE & !ADS & !HLDA & SCLK) THEN IDLE7
        ELSE IF (SCLK) THEN INUSE
        ELSE IDLE6;

STATE IDLE7:              " 7 CLOCKS IDLE
        IF (IDLE & !ADS & !HLDA & SCLK) THEN IDLE8
        ELSE IF (SCLK) THEN INUSE
        ELSE IDLE7;
```

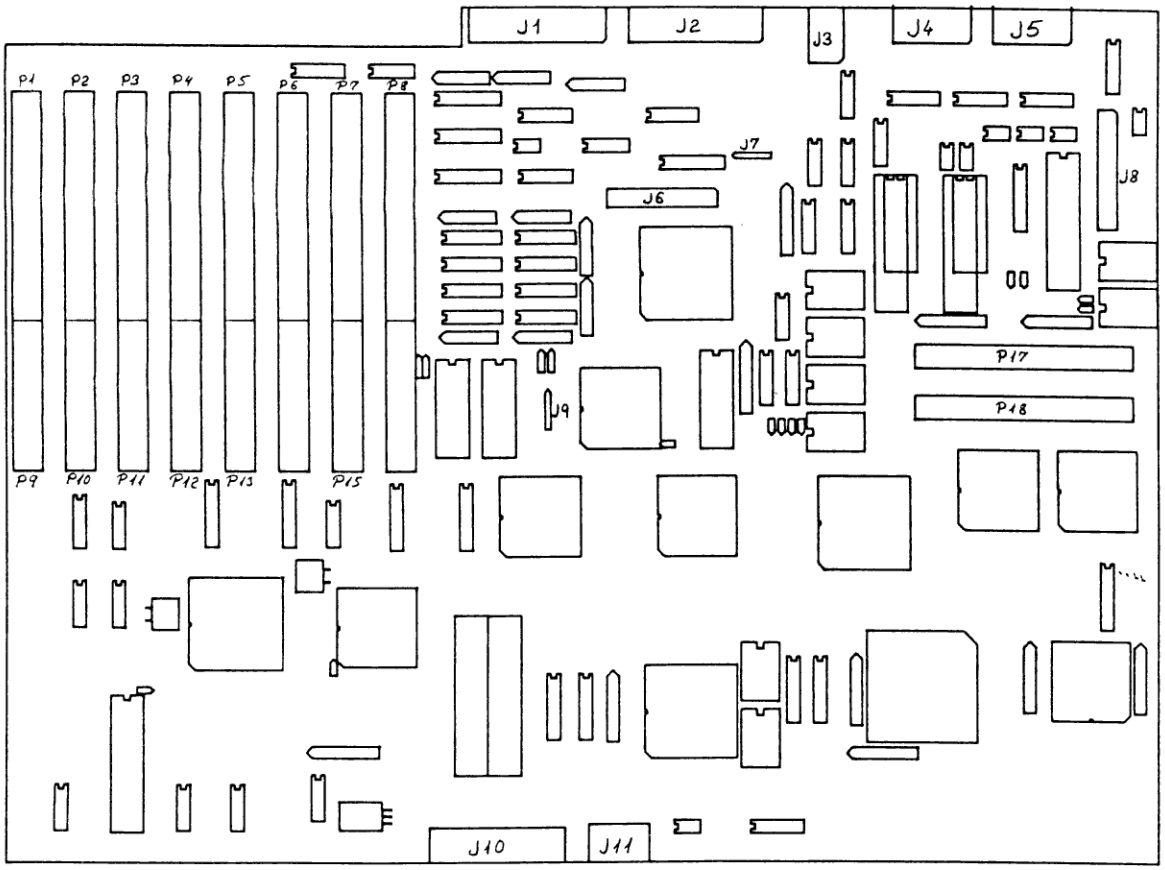
```
STATE IDLE8:              " 8 CLOCKS IDLE
        IF (IDLE & !ADS & !HLDA & SCLK) THEN IDLE8
        ELSE IF (SCLK) THEN INUSE
        ELSE IDLE8;

" COPROCESSOR OPERAND REQUEST

STATE_DIAGRAM ÆPEREQOUTÅ

STATE 0:                  " NO COPROCESSOR REQUEST
        IF (PEREQ & (ÆICNT0,ICNT1,ICNT2Å==IDLE8)
                                &!ADS &!HLDA &SCLK) THEN 1
        ELSE 0;

STATE 1:                  " COPROCESSOR REQUEST
        IF (!PEREQ & SCLK) THEN 0
        ELSE 1;
```

```
TEST_VECTORS (Æ CLK2,RESET,!ADS,!READY,HLDA,PEREQ,!OE Å ->
              Æ SCLK,PEREQOUT,IDLE Å)

        Æ C,H,H,H,L,L,L Å -> Æ X,X,X Å;
        Æ C,H,H,H,L,L,L Å -> Æ X,X,X Å;
        Æ C,L,H,H,L,L,L Å -> Æ L,L,H Å; " SYNCH. PHASE
        Æ C,L,H,H,L,L,L Å -> Æ H,L,H Å;
        Æ C,L,H,H,L,L,L Å -> Æ L,L,H Å;
        Æ C,L,H,H,L,L,L Å -> Æ H,L,H Å;
        Æ C,L,H,H,L,L,L Å -> Æ L,L,H Å;

        Æ C,L,L,H,L,L,L Å -> Æ H,L,H Å; " ADS ASSERTED
        Æ C,L,L,H,L,L,L Å -> Æ L,L,L Å;
        Æ C,L,H,H,L,L,L Å -> Æ H,L,L Å; " ONE WAIT-STATE
        Æ C,L,H,H,L,L,L Å -> Æ L,L,L Å;
        Æ C,L,H,L,L,H,L Å -> Æ H,L,L Å; " READY, PEREQ ASSERTED
        Æ C,L,H,L,L,H,L Å -> Æ L,L,H Å;

        Æ C,L,H,H,L,H,L Å -> Æ H,L,H Å; " 1 CLOCK IDLE
        Æ C,L,H,H,L,H,L Å -> Æ L,L,H Å;
        Æ C,L,H,H,L,H,L Å -> Æ H,L,H Å; " 2 CLOCKS IDLE
        Æ C,L,H,H,L,H,L Å -> Æ L,L,H Å;
        Æ C,L,H,H,L,H,L Å -> Æ H,L,H Å; " 3 CLOCKS IDLE
        Æ C,L,H,H,L,H,L Å -> Æ L,L,H Å;
        Æ C,L,H,H,L,H,L Å -> Æ H,L,H Å; " 4 CLOCKS IDLE
        Æ C,L,H,H,L,H,L Å -> Æ L,L,H Å;
        Æ C,L,H,H,L,H,L Å -> Æ H,L,H Å; " 5 CLOCKS IDLE
        Æ C,L,H,H,L,H,L Å -> Æ L,L,H Å;
        Æ C,L,H,H,L,H,L Å -> Æ H,L,H Å; " 6 CLOCKS IDLE
        Æ C,L,H,H,L,H,L Å -> Æ L,L,H Å;
        Æ C,L,H,H,L,H,L Å -> Æ H,L,H Å; " 7 CLOCKS IDLE
        Æ C,L,H,H,L,H,L Å -> Æ L,L,H Å;
        Æ C,L,H,H,L,H,L Å -> Æ H,L,H Å; " 8 CLOCKS IDLE
        Æ C,L,H,H,L,H,L Å -> Æ L,H,H Å;
        Æ C,L,H,H,L,H,L Å -> Æ H,H,H Å; " 9 CLOCKS IDLE,
                                        " PEREQOUT ASSERTED
        Æ C,L,H,H,L,H,L Å -> Æ L,H,H Å;

END PRQ
```

3.5 Assembly drawing



3.6 Connectors



Board layout showing the connectors on CPU451.

The system board has the following connectors:

Parallel printer connector	(J1)
Monitor connector	(J2)
Keyboard connector	(J3)
Serial communications connector COM1	(J4)
Serial communications connector COM2	(J5)
Feature connector	(J6)
Video connector	(J7)
Floppy drive connector	(J8)
Lightpen connector	(J9)
Power-supply connector	(J10)
System control connector	(J11)
I/O expansion slots	(P1 -P16)
Memory bank 0,1 connector	(P17)
Memory bank 2,3 connector	(P18)

The Pin assignments for the Parallel printer connector (J1) are as follows:

Pin	Function	Pin	Function
1	-STROBE	14	-AUTOFDXT
2	DATA0	15	-ERROR
3	DATA1	16	-INIT
4	DATA2	17	-SELECTIN
5	DATA3	18	0 Volt
6	DATA4	19	0 Volt
7	DATA5	20	0 Volt
8	DATA6	21	0 Volt
9	DATA7	22	0 Volt
10	-ACK	23	0 Volt
11	BUSY	24	0 Volt
12	PE	25	0 Volt
13	SELECT		

Parallel printer connector

The Pin assignments for the Monitor connector (J2) are as follows:

Pin	Function	Pin	Function
1	0 Volt	14	Red
2	0 Volt	15	Red Secondary
3	0 Volt	16	Green
4	0 Volt	17	Green Secondary
5	0 Volt	18	Blue
6	0 Volt	19	Blue Secondary
7	0 Volt	20	HSYNC
8	0 Volt	21	VSYNC
9	0 Volt	22	0 Volt
10	RxD (mouse)	23	N60Hz
11	Not connected	24	KeyBoarDPWR
12	KeyBoarDDATA	25	KeyBoarDCLK
13	0 Volt		

Monitor connector

The Pin assignments for the Keyboard connector (J3) are as follows:

Pin	Function
1	Keyboard Power (+9V)
2	Not Connected
3	Not Connected
4	Keyboard return
5	Keyboard Data
6	Keyboard Clock

Keyboard connector

The Pin assignments for the Serial communications connectors (J4 and J5) are as follows:

Pin	Function
1	Carrier Detect
2	Received Data
3	Transmitted Data
4	Data Terminal Ready
5	Ground
6	Data Set Ready
7	Request To Send
8	Clear To Send
9	Ringing Indicator

Serial communications connectors

The Pin assignments for the Feature connector (J6) are as follows:

Pin	Function	Pin	Function
1	0 Volt	2	-12 Volt
3	+12 Volt	4	J7 pin 4
5	J7 pin 3	6	GSOUT
7	RSOUT	8	BSOUT
9	ATRSL	10	BOUT
11	GOUT	12	G
13	RS	14	B
15	R	16	ROUT
17	FEAT1	18	BLANK
19	FEAT0	20	FC1
21	FC0	22	GS/I
23	BS/V	24	HIN
25	VIN	26	14.318 MHz
27	NINTERNL	28	EXTOSC
29	VOUT	30	HOUT
31	0 Volt	32	+5 Volt

Feature connector

The Pin assignments for the Video connector (J7) are as follows:

Pin	Function
1	0 Volt
2	J6 pin 4
3	J6 pin 5
4	0 Volt
5	Reserved
6	Reserved

Video connector

The Pin assignments for the Floppy Drive connector (J8) are as follows:

Pin	Function	Pin	Function
1	0 Volt	2	RMM/RWC
3	speedsel	4	
5	0 Volt	6	
7	0 Volt	8	IDX
9	0 Volt	10	M01
11	0 Volt	12	DS2
13	0 Volt	14	DS1
15	0 Volt	16	M02
17	0 Volt	18	DIRC
19	0 Volt	20	STEP
21	0 Volt	22	WD
23	0 Volt	24	WE
25	0 Volt	26	TR00
27	0 Volt	28	WP
29	0 Volt	30	RDD
31	0 Volt	32	HS
33	0 Volt	34	-DCHNG

Floppy Drive connector

The Pin assignments for the Lightpen connector (J9) are as follows:

Pin	Function
1	-LPENIN
2	Not connected
3	-LPENSW
4	0 Volt
5	+5 Volt
6	+12 Volt

Lightpen connector

The Pin assignments for the Power-supply connector (J10) are as follows:

Pin	Function
1	-12 volt
2	+12 volt
3	Key
4-9	Ground
10-13	+5 volt

Power-supply connector

The Pin assignments for the System control connector (J11) are as follows:

Pin	Function	Pin	Function
1A	-OVERTEMP	1B	-POWRESet
2A	-ON	2B	TurnOFF
3A	0 Volt	3B	Power OK
4A	-ON return	4B	-ON
5A	-KBDINH return	5B	-KBDINH
6A	+5V (LED pwr)	6B	LED pwr return
7A	+5V (SPKR pwr)	7B	SPK
8A	+12V(Vent pwr)	8B	VENT

System control connector

The Pin assignments for the I/O expansion connectors (P1 through P16) are as follows:

Pin	Function	Pin	Function
1A	-IOCHK	1B	0 Volt
2A	SD7	2B	RDRV
3A	SD6	3B	+5 Volt
4A	SD5	4B	IRQ9
5A	SD4	5B	-5 Volt
6A	SD3	6B	DRQ2
7A	SD2	7B	-12 Volt
8A	SD1	8B	-0WS
9A	SD0	9B	+12 Volt
10A	IOCHRDY	10B	0 Volt
11A	AEN	11B	-SMEMW
12A	SA19	12B	-SMEMR
13A	SA18	13B	-IOW
14A	SA17	14B	-IOR
15A	SA16	15B	-DACK3
16A	SA15	16B	DRQ3
17A	SA14	17B	-DACK1
18A	SA13	18B	DRQ1
19A	SA12	19B	-REF
20A	SA11	20B	SYSCLK
21A	SA10	21B	IRQ7
22A	SA9	22B	IRQ6
23A	SA8	23B	IRQ5
24A	SA7	24B	IRQ4
25A	SA6	25B	IRQ3
26A	SA5	26B	-DACK2
27A	SA4	27B	TC
28A	SA3	28B	BALE
29A	SA2	29B	+5 Volt
30A	SA1	30B	OSC
31A	SA0	31B	0 Volt

I/O expansion (PCbus-) connectors (P1 - P8)

Pin	Function	Pin	Function
1C	-SBHE	1D	-MCS16
2C	SA23	2D	-IOCS16
3C	SA22	3D	IRQ10
4C	SA21	4D	IRQ11
5C	SA20	5D	IRQ12
6C	SA19	6D	IRQ15
7C	SA18	7D	IRQ14
8C	SA17	8D	-DACK0
9C	-MEMR	9D	DRQ0
10C	-MEMW	10D	-DACK5
11C	SD8	11D	DRQ5
12C	SD9	12D	-DACK6
13C	SD10	13D	DRQ6
14C	SD11	14D	-DACK7
15C	SD12	15D	DRQ7
16C	SD13	16D	+5 Volt
17C	SD14	17D	-MASTER
18C	SD15	18D	0 Volt

I/O expansion (ATbus-) connectors (P9 - P16)

The Pin assignments for the Memory connectors (P17,P18) are as follows:

Pin	Function	Pin	Function	Pin	Function P17/P18
1A	MD1	1B	+5 Volt	1C	MD0
2A	MD2	2B	+5 Volt	2C	MP0
3A	MD3	3B	0 Volt	3C	MP1
4A	MD4	4B	0 Volt	4C	MP2
5A	MD5	5B	0 Volt	5C	MP3
6A	MD6	6B	0 Volt	6C	-LBE0
7A	MD7	7B	0 Volt	7C	-LBE1
8A	MD8	8B	0 Volt	8C	-LBE2
9A	MD9	9B	0 Volt	9C	-LBE3
10A	MD10	10B	0 Volt	10C	-2MB0/-2MB1
11A	MD11	11B	0 Volt	11C	-8MB0/-8MB1
12A	MD12	12B	0 Volt	12C	Reserved
13A	MD13	13B	0 Volt	13C	40NS0/40NS1
14A	MD14	14B	0 Volt	14C	20NS0/20NS1
15A	MD15	15B	0 Volt	15C	-DWE
16A	MD16	16B	0 Volt	16C	-RAS0/-RAS2
17A	MD17	17B	0 Volt	17C	-RAS1/-RAS3
18A	MD18	18B	0 Volt	18C	-CAS0/-CAS2
19A	MD19	19B	0 Volt	19C	-CAS1/-CAS3
20A	MD20	20B	0 Volt	20C	XDA0
21A	MD21	21B	0 Volt	21C	XDA1
22A	MD22	22B	0 Volt	22C	XDA2
23A	MD23	23B	0 Volt	23C	XDA3
24A	MD24	24B	0 Volt	24C	XDA4
25A	MD25	25B	0 Volt	25C	XDA5
26A	MD26	26B	0 Volt	26C	XDA6
27A	MD27	27B	0 Volt	27C	XDA7
28A	MD28	28B	0 Volt	28C	DA8
29A	MD29	29B	0 Volt	29C	DA9
30A	MD30	30B	0 Volt	30C	-ENRASA
31A	MD31	31B	+5 Volt	31C	-DISRASA
32A	Reserved	32B	+5 Volt	32C	Reserved

Memory connectors

References:

A: Intel 80386.

B: Intel 80387.

C: Chips & Technologies CS8230: AT/386 CHIPSet.

D: Chips & Technologies 82C206 Integrated Peripherals controller.

E: Chips & Technologies 82C435 Enhanced Graphics Controller 82A436 Bus Interface.

F: Western Digital WD37C65.