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2-11-82
Hans Juul-Olsen

MSM5832RS

MICROPROCESSOR REAL-TIME CLOCK/CALENDAR

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MSM5832 MICROPROCESSOR REAL-TIME CLOCK/CALENDAR

GENERAL DESCRIPTION

The MSM5832 is a monolithic, metal-gate CMOS integrated circuit that functions as a real time clock/calendar for use in bus-oriented microprocessor applications. The on-chip 32.768Hz crystal controlled oscillator time base is counted down to provide addressable 4-bit I/O data of SECONDS, MINUTES, HOURS, DAY-OF-WEEK, DATE, MONTH, and YEAR. Data access is controlled by 4-bit address, chip select, read, write and hold inputs. Other functions include 12H/24H format selection, leap year identification and manual ±30 second correction.

The MS5832 normally operates from a 5 volt ±5% supply. Battery back-up operation down to 2.2 volts allows continuation of time keeping when main power is off. One test input facilitates rapid testing of the time keeping operations. The MS5832 is offered in an 18-lead dual-in-line plastic (RS suffix) package.

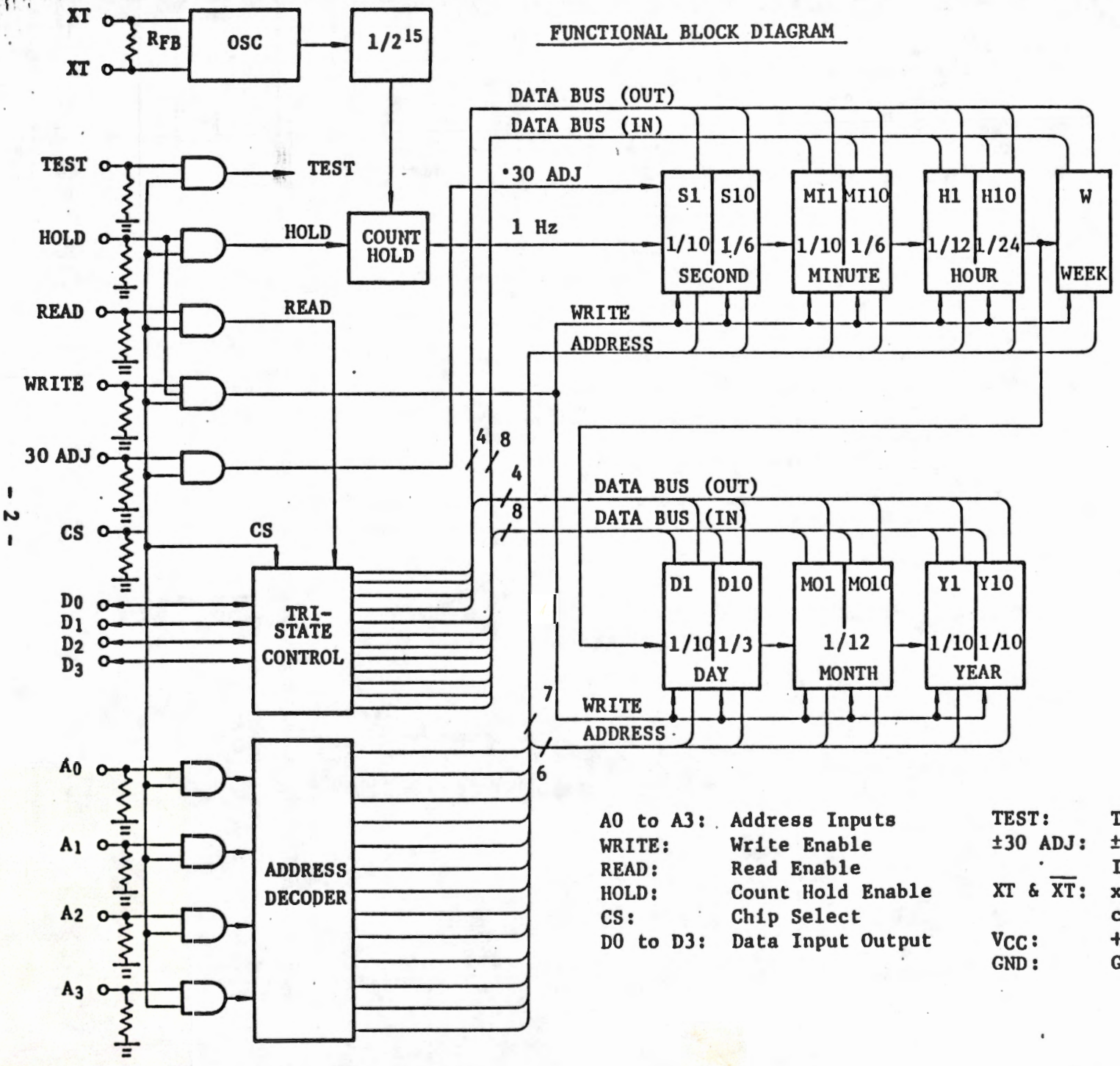
FEATURES

- Microprocessor bus-oriented
-

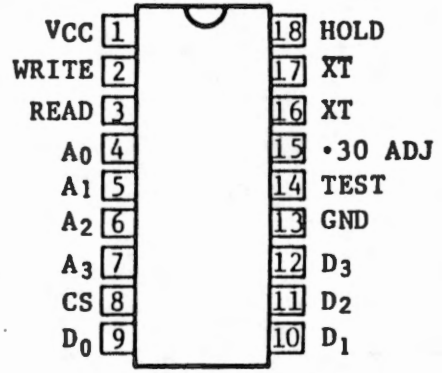
TIME	MONTH		DATE		YEAR		DAY OF WEEK
23:59:59	12	-	31	-	99	-	7

- 4-BIT DATA BUS
- 4-BIT ADDRESS
- Read, Write, Hold Chip select inputs
- Interrupt signal outputs -- 1024, 1, 1/60, 1/3600Hz
- 32.768kHz crystal controlled operation
- Leap year register bit
- 12 or 24 hour format
- ±30 second error correction
- Single 5 volt power supply
- Back-up battery operation to V_{cc} = 2.2V
- Low Power Dissipation

  90 µW Max. at V_{cc} = 3V
  2.5 mW Max. at V_{cc} = 5V
- High Density 300 mil 18-Pin Package



PIN CONFIGURATION



A0 to A3:	Address Inputs	TEST:	Test Input
WRITE:	Write Enable	±30 ADJ:	±30 Second Correction Input
READ:	Read Enable	XT & $\overline{XT}$:	xtal oscillator connections
HOLD:	Count Hold Enable	VCC:	+5V Supply
CS:	Chip Select	GND:	Ground
D0 to D3:	Data Input Output		

FUNCTION TABLE

FIGURE 1

ADDRESS INPUTS				INTERNAL COUNTER	DATA I/O				DATA LIMITS	NOTES
A_0	A_1	A_2	A_3		D_0	D_1	D_2	D_3		
0	0	0	0	S 1	*	*	*	*	0∿9	S1 or S10 are reset to zero irrrespective of input data D0∿D3 when write instruction is executed with address selection.
1	0	0	0	S 10	*	*	*		0∿5	
0	1	0	0	MI 1	*	*	*	*	0∿9	
1	1	0	0	MI 10	*	*	*		0∿5	
0	0	1	0	H 1	*	*	*	*	0∿9	
1	0	1	0	H 10	*	*	†	†	0∿1 / 0∿2	D2 = "1" for PM D3 = "1" for 24 hour format D2 = "0" for AM D3 = "0" for 12 hour format
0	1	1	0	W	*	*	*		0∿6	
1	1	1	0	D 1	*	*	*	*	0∿9	
0	0	0	1	D 10	*	*	†		0∿3	D2 = "1" for 29 days in month 2 D2 = "0" for 28 days in month 2 (2)
1	0	0	1	MO 1	*	*	*	*	0∿9	
0	1	0	1	MO 10	*				0∿1	
1	1	0	1	Y 1	*	*	*	*	0∿9	
0	0	1	1	Y 10	*	*	*	*	0∿9	

(1) * data valid as "0" or "1".

Blank does not exist (unrecognized during a write and held at "0" during a read)

† data bits used for AM/PM, 12/24 HOUR and leap year.

(2) If D2 previously set to "1", upon completion of month 2 day 29, D2 will be internally reset to "0".

TYPICAL CHARACTERISTICS — Oscillator Frequency Deviations

Frequency Deviation vs Temperature

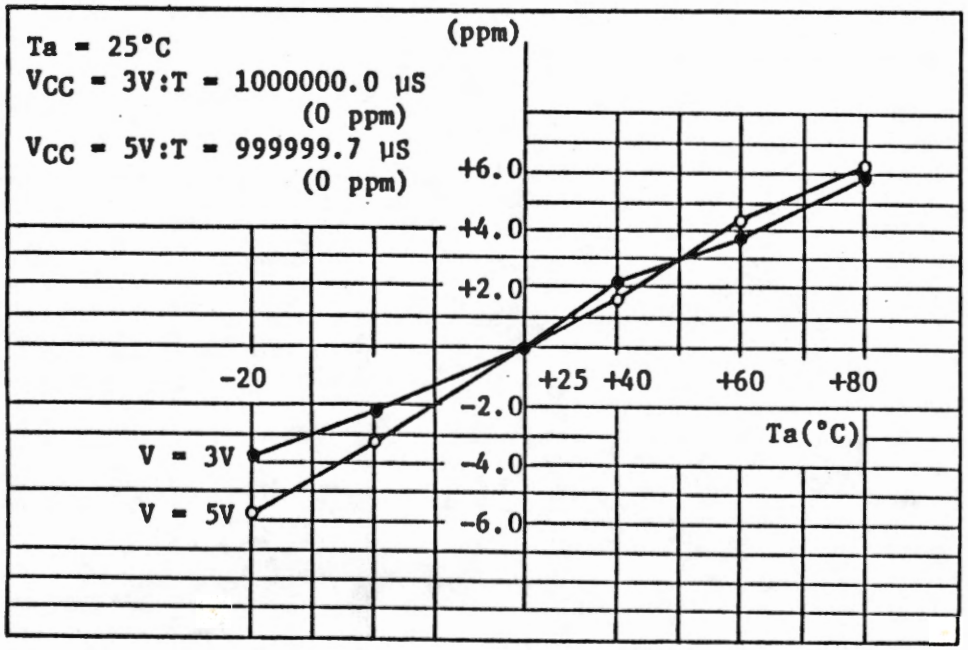


FIGURE 2

Frequency Deviation vs Supply Voltage

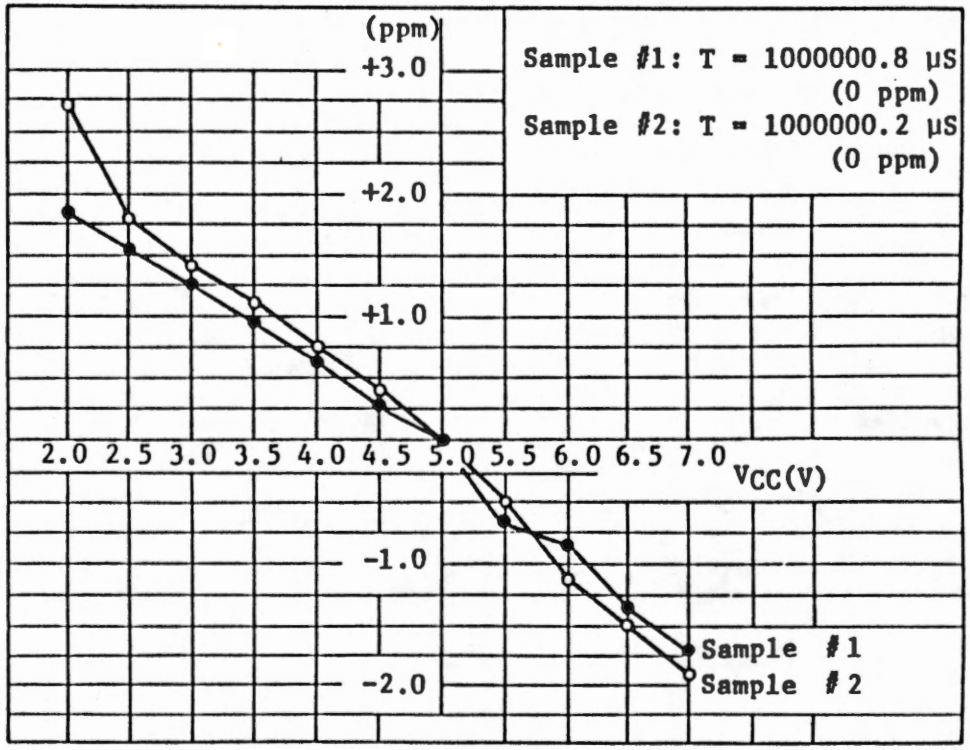


FIGURE 3

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	-0.3 ∿ 7.0	V
Input Voltage	V_{IN}	-0.3 ∿ V_{CC} +0.3	V
Data I/O Voltage	V_D	-0.3 ∿ V_{CC} +0.3	V
Storage Temperature	T_{stg}	-55 ∿ 150	°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.75	5	5.25	V	5V ±5%
Standby Supply Voltage	V_{CCS}	2.2	5	7	V	
Input Signal Level	V_{IH}	3.6	5	V_{CC}	V	V_{CC} = 5V ± 5% Respect to GND
	V_{IL}	-0.3	0	0.8	V	
Crystal Oscillator Freq.	f(XT)		32.768		kHz	
Operating Temperature	Ta	-30		+85	°C	

DC CHARACTERISTICS

(V_{CC} = 5V ± 5%; T_A = -30 to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input Current (1)	I_{TH}	10	25	50	μA	V_{IN} = 5V
	I_{IL}	-1		1	μA	V_{IN} = 0V
Data I/O Leakage Current	I_{LD}	-1		1	μA	$V_{I/O}$ = 0 to V_{CC}, CS = "0"
Output Low Voltage	V_{OL}			0.4	V	I_O = 1.6 ma, CS = "1", READ = "1"
Output Low Current	I_{OL}	1.6			mA	V_O = 0.4V, CS = "1", READ = "1"
Operating Supply Current	I_{CCS}			30	μA	V_{CC} = 3V, Ta = 25°C
	I_{CC}			500	μA	V_{CC} = 5V, Ta = 25°C

(1) XT, $\overline{XT}$ and $D_0 \sim D_3$ excluded.

AC CHARACTERISTICS

CAPACITANCE

T_A = 25°C, f = 1MHz

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			8	pF
Input Capacitance	C_{IN}			5	pF

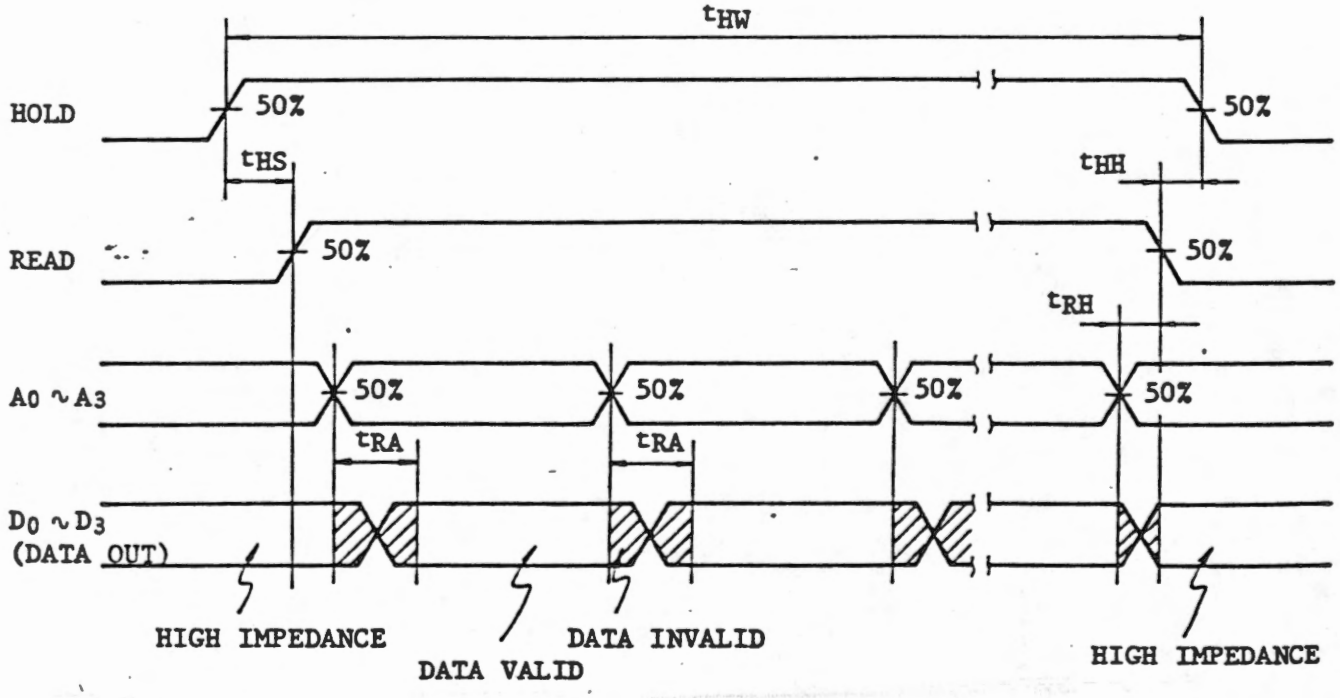
Note: This parameter is periodically sampled and not 100% tested.

READ CYCLE

(V_{CC} = 5V ± 5%; Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
HOLD Set-up Time	t_{HS}	150			µS
HOLD Hold Time	t_{HH}	0			µS
HOLD Pulse Width	t_{HW}			1	SEC
READ Hold Time	t_{RH}	0			µS
READ Access Time	t_{RA}			6	µS

READ CYCLE FIGURE 4



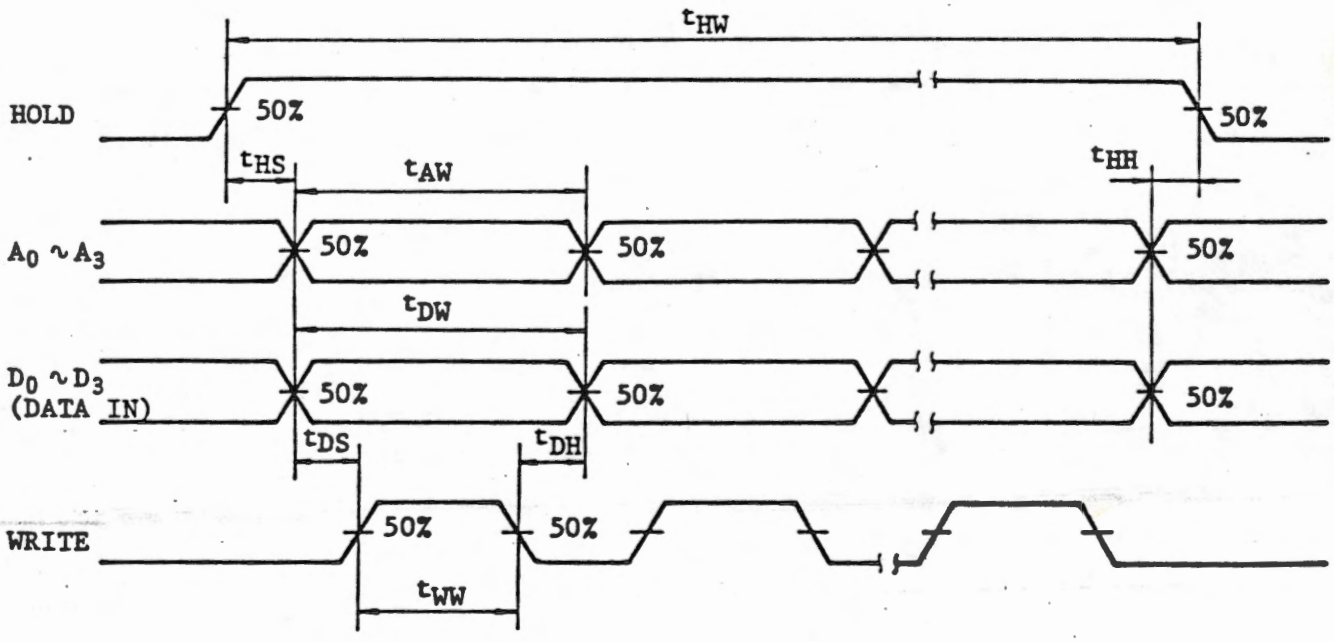
Notes:
1. A Read occurs during the overlap of a high CS and a high READ.
2. Output Load: 1 TTL Gate, C_L = 50 pf and R_L = 4.7kΩ
3. CS may be a permanent "1", or may be coincident with HOLD pulse.

WRITE CYCLE

(V_{CC} = 5V ± 5%; Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
HOLD Set-up Time	t_{HS}	150			µS
HOLD Hold Time	t_{HH}	0			µS
HOLD Pulse Width	t_{HW}			1	SEC
ADDRESS Pulse Width	t_{AW}	1.7			µS
DATA Pulse Width	t_{DW}	1.7			µS
DATA Set-up Time	t_{DS}	0.5			µS
DATA Hold Time	t_{DH}	0.2			µS
WRITE Pulse Width	t_{WW}	1.0			µS

WRITE CYCLE FIGURE 5



Notes: 1. A WRITE occurs during the overlap of a high CS, a high HOLD and a high WRITE.
2. CS may be permanent "1", or may be coincident with HOLD pulse.

FUNCTIONAL DESCRIPTION

A block diagram of the MSM5832 microprocessor real-time clock/calendar and a package connection diagram are shown on the first page. Figure 9 illustrates a method of interfacing between the clock/calendar circuit and a micro processor. Figures 9, 10 and 11 illustrate alternative standby power supply circuits. A function table listing relationships between address inputs, data input/output and internal counter selection is shown in Figure 1. Unless otherwise indicated, the following descriptions are based on the block diagram.

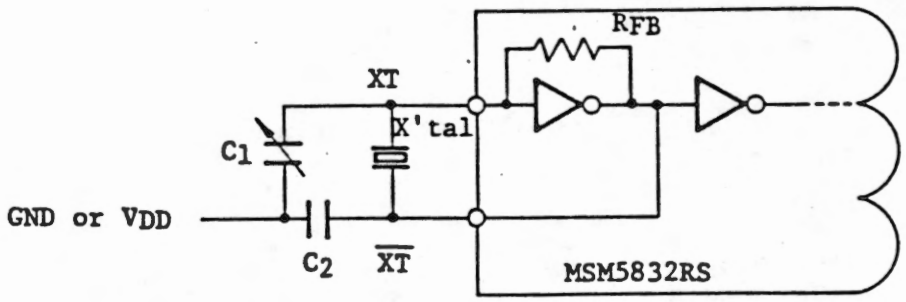
32.768kHz OSCILLATOR (pins 16 and 17): An internal inverting amplifier with feedback resistor, R_{FB}, is connected with a crystal and two capacitors as shown in Figure 6 to form a stable, accurate oscillator — which serves as the precision time base of the circuit. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal. Typical oscillator performance as a function of ambient temperature and supply voltage is shown in Figures 2 and 3 respectively.

$A_0 \sim A_3$ (pins 4 ~ 7): Address inputs, used to select internal counters for read/write operations (see function table — Figure 1). A "1" is defined as V_{CC}; a "0" is GND. Pull-down to GND is provided by internal resistors.

$D_0 \sim D_3$ (pins 9 ~ 12): Data Inputs/Outputs, two-way bus lines controlled by READ and WRITE inputs. As shown in Figure 7 external pull-up resistors of 4.7K or higher are required by the open-drain N-channel MOS outputs. D3 is the MSB; D_0 is the LSB.

TEST (pin 14): Normally this input is unconnected -- pull-down to GND is provided by an internal resistor -- or connected to GND. With CS at V_{CC}, pulses to V_{CC} on the TEST input will directly clock the S_1, MI_{10}, W, D_1 and Y_1 counters, depending on which counter is addressed (W and D_1 are select-d by D_1 address in this mode only). Roll-over to next counter is enabled in this mode.

OSCILLATOR CIRCUIT FIGURE 6



$C_1 \sim C_2 = 15 \sim 30pF$

CHIP SELECT (pin 8): Connecting CS input to V_{CC} enables all inputs and outputs. Unconnected -- pull-down to GND is provided by an internal resistor -- or connecting CS to GND will disable HOLD, WRITE, READ, ±30 ADJ, $D_0 \sim D_3$, $A_0 \sim D_3$ and TEST.

As shown in Figure 9 CS can be used to detect system power failure by connecting system power (+5V) to CS, so that when system power is on, all inputs and outputs will be enabled, and when system power is off, all inputs and outputs will be disabled. The threshold voltage of CS is higher than all other inputs to insure correct operation of this function.

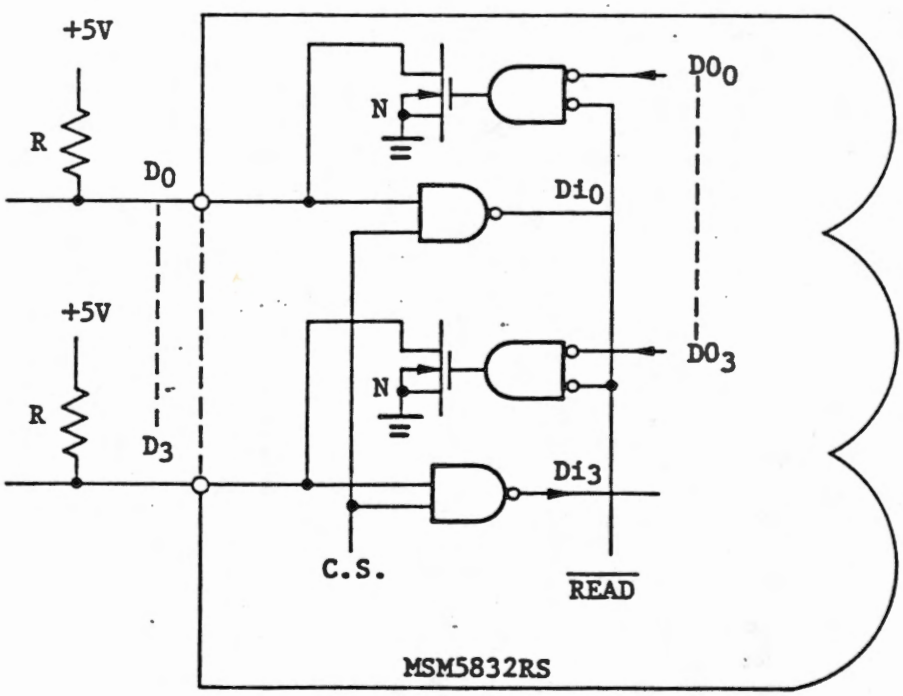
HOLD (pin 18): Switching this input to V_{CC} inhibits the internal 1Hz clock to the S1 counter. After the specified HOLD set-up time (150 µS), all counters will be in a static state, thus allowing error-free read or write operations. So long as the HOLD pulse width is less than 1 second, accuracy of the real time will be undisturbed. Pull-down to GND is provided by an internal resistor.

READ (pin 3): Read function as shown in Figure 4 is enabled when READ is switched to VCC. Pull-down to GND is provided by an internal resistor.

WRITE (pin 2): Write function as shown in Figure 5 is enabled when WRITE is switched to VCC. Pull-down to GND is provided by an internal resistor.

±30 ADJ (pin 15): Momentarily connecting this input to V_{CC} (>31.25 ms) will reset seconds (S1, S10 counters and $2^{11} \sim 2^{15}$ frequency dividers) to 00; if seconds were 30 or more, one minute is added to the minutes (MI 1 counter) and if seconds were less than 30, the minutes are unchanged. Pull-down to GND is provided by an internal resistor.

DATA I/O CIRCUIT FIGURE 7



REFERENCE SIGNAL OUTPUT

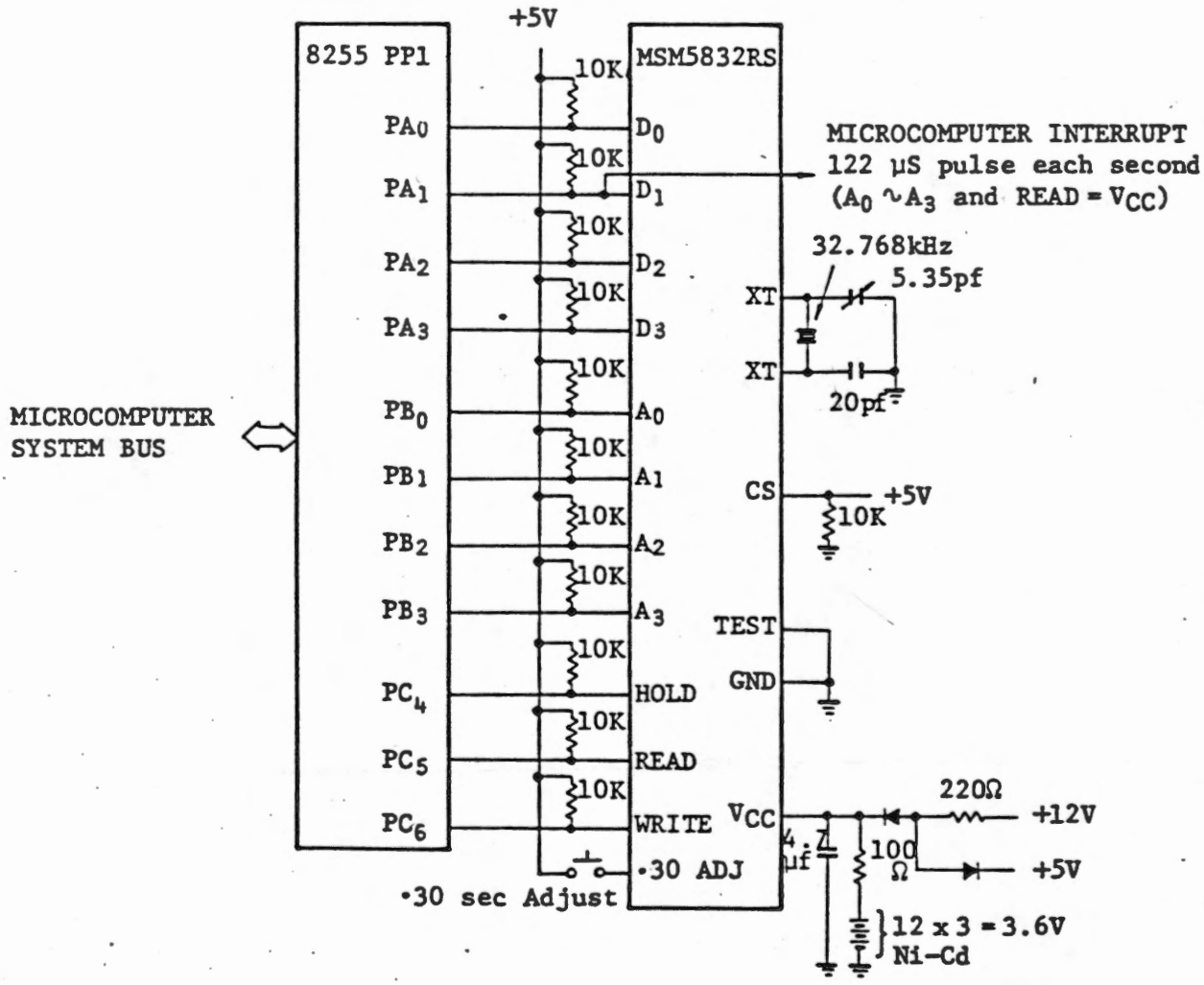
Reference signals are available as outputs on $D_0 \sim D_3$ if CS, READ and $A_0 \sim A_3$ are at VCC. Refer to Figure 8 for specifics. As shown in Figure 9 these signals may be used to generate interrupts for the microprocessor.

REFERENCE SIGNAL OUTPUTS — FIGURE 8

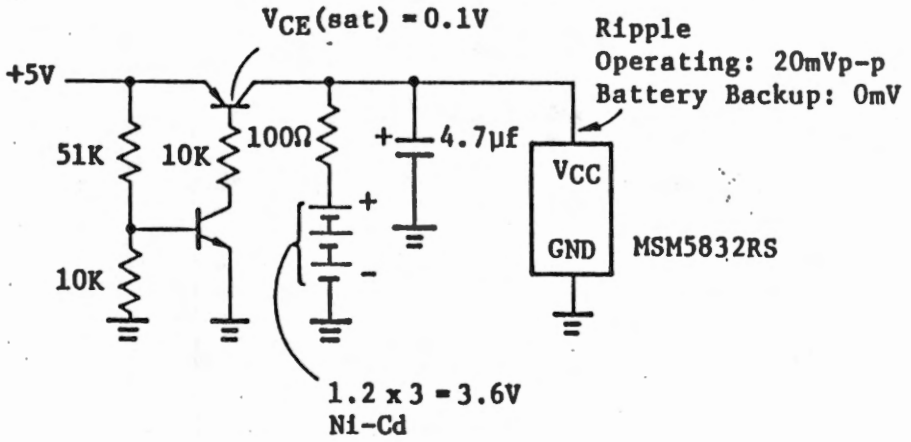
CONDITIONS	OUTPUT	REFERENCE FREQUENCY	PULSE WIDTH
HOLD = L	D_0(1)	1024 Hz	duty 50%
READ = H	D_1	1 Hz	122.1 µS
C.S. = H	D2	1/60 Hz	122.1 µS
$A_0 \sim A_3$ = H	D_3	1/3600 Hz	122.1 µS

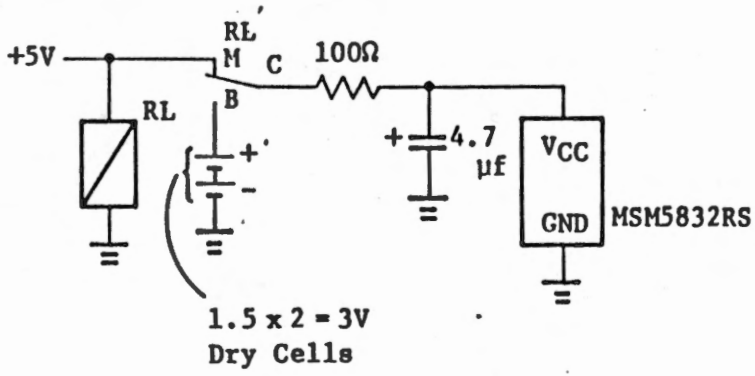
(1) 1024 Hz signal at D_0 not dependent on HOLD input level

TYPICAL APPLICATION — Use with Programmable Peripheral Interface (PPI) — FIGURE 9



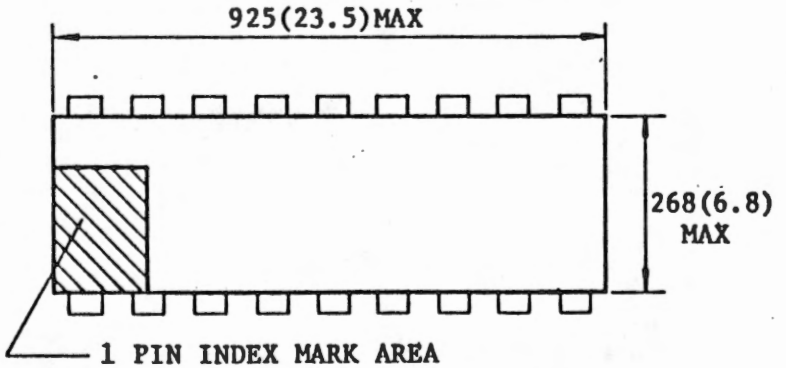
TYPICAL APPLICATIONS — Alternative Standby Power Supply Circuits

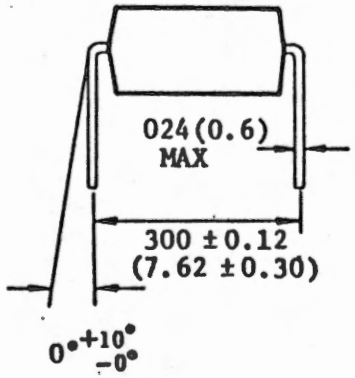


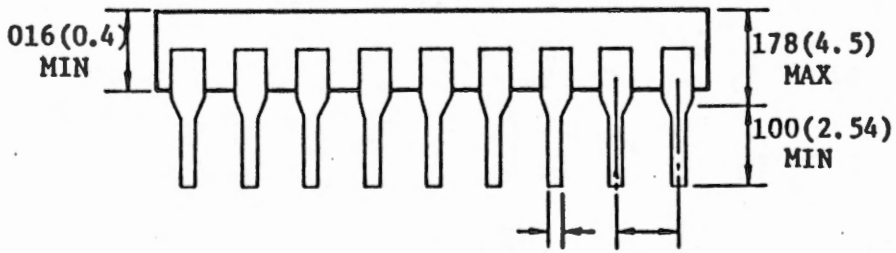


PACKAGE SPECIFICATIONS

18 LEAD PLASTIC (RS)







INCHES (MM)

SEMICONDUCTOR INTEGRATED CIRCUIT SPECIFICATIONS

MSM58321RS

Real Time Clock

The MSM58321RS is a real time clock with a battery backup function for a microcomputer timer unit.

The 4-bit bidirectional bus line method is used for the data I/O circuit; the clock is set, corrected, or read by accessing the memory.

The time is read with 4-bit DATA I/O, ADDRESS WRITE, READ, and $\overline{\text{BUSY}}$; it is written with 4-bit DATA I/O, ADDRESS WRITE, WRITE, and $\overline{\text{BUSY}}$.

The timer functions are: SECOND, MINUTE, HOUR, DAY-OF-WEEK, DATE, MONTH, YEAR, 12/24-hour timer conversion, automatic leap year setting and selection, start/stop, frequency divider 5-poststage reset, busy circuit reset, and reference signal output functions. The crystal oscillator outputs reference signals of 32.768 kHz.

o Model name : MSM58321RS

o Function : Real time clock

o Process : CMOS

o Circuit configuration: See Figure 1.

o Pin arrangement

(Top View) 16 Lead Plastic DIP

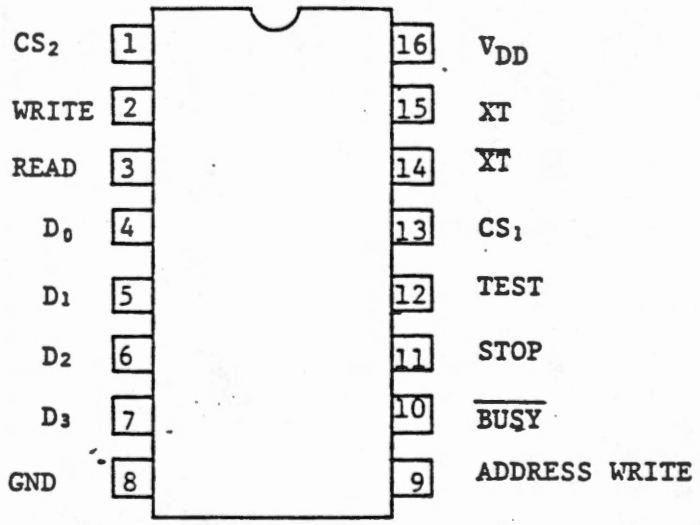
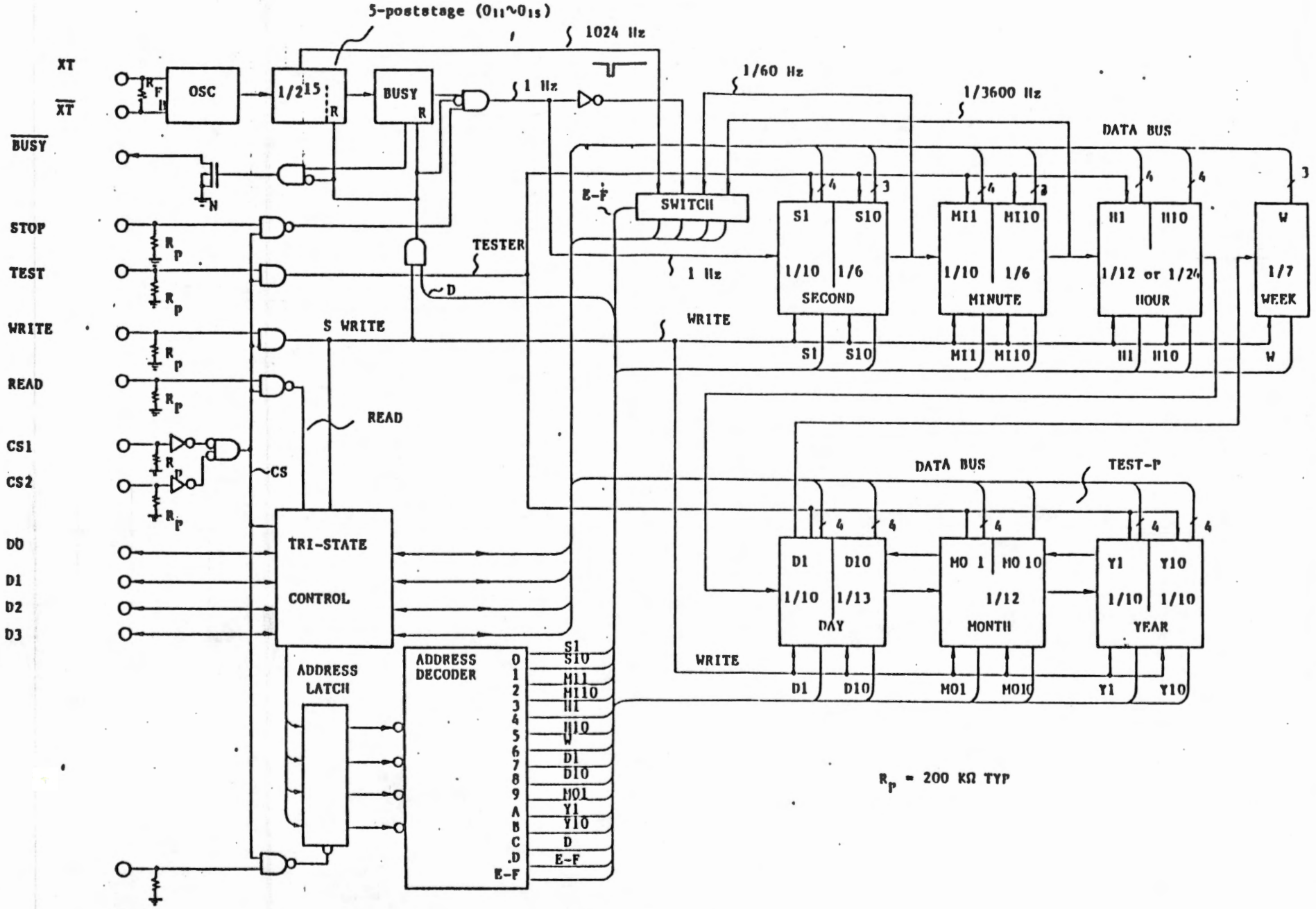


Fig. 1



o Function table

	Address input				Internal counter	Data input/output				Count value	Remarks
	D_0 (A_0)	D_1 (A_1)	D_2 (A_2)	D_3 (A_3)		D_0	D_1	D_2	D_3		
0	L	L	L	L	S 1	*	*	*	*	0 ∿ 9	
1	H	L	L	L	S 10	*	*	*		0 ∿ 5	
2	L	H	L	L	MI 1	*	*	*	*	0 ∿ 9	
3	H	H	L	L	MI 10	*	*	*		0 ∿ 5	
4	L	L	H	L	H 1	*	*	*	*	0 ∿ 9	
5	H	L	H	L	H 10	*	*	*	Ⓐ	0∿ 1/0 ∿2	D2 = H specifies PM, D2 = L specifies AM, D3 = H specifies 24-hour timer, and D3 = L specifies 12-hour timer. When D3 = H is written, the D2 bit is reset inside the IC by D3 = H.
6	L	H	H	L	W	*	*	*		0 ∿ 6	
7	H	H	H	L	D 1	*	*	*	*	0 ∿ 9	
8	L	L	L	H	D 10	*	*	Ⓐ*	Ⓐ*	0 ∿ 3	The D2 and D3 bits in D10 are used to select a leap year.
9	H	L	L	H	MO 1	*	*	*	*	0 ∿ 9	
A	L	H	L	H	MO 10	*				0 ∿ 1	
B	H	H	L	H	Y 1	*	*	*	*	0 ∿ 9	
C	L	L	H	H	Y 10	*	*	*	*	0 ∿ 9	
D	H	L	H	H							A selector to reset 5 poststages in the $1/2^{15}$ frequency divider and the BUSY circuit. They are reset when this code is latched with ADDRESS LATCH and the WRITE input goes to the H level.
E∿F	L/H	H	H	H							A selector to obtain reference signal output. Reference signals are output to D0 - D3 when this code is latched with ADDRESS LATCH and READ input goes to H.

Calendar	D_7	D_3	Remainder obtained by dividing the year number by 4
Gregorian calendar	L	L	0
Showa	H	L	3
	L	H	2
	H	H	

Notes: 1. There are no bits in blank fields for data input/output. L-level signals are output by reading and data is not stored by writing because there are no bits.

2. The bit with marked Ⓐ is used to select the 12/24-hour timer and the bits marked Ⓐ* are used to select a leap year. These three bits can be read or written.

3. When signals are input to bus lines D0 - D3 and ADDRESS WRITE goes to the H level for address input, ADDRESS information is latched with ADDRESS LATCH.

o Absolute maximum ratings

Item	Symbol	Conditions	Rated value	Unit
Power voltage	V_{DD}	Ta = 25°C	-0.3 ∿ 7	V
Input voltage	V_I	Ta = 25°C	GND-0.3 V_{DD}+0.3	V
Output voltage	V_O	Ta = 25°C	GND-0.3 V_{DD}+0.3	V
Storage temperature	Tstg	-	-55 ∿ +150	°C

o Operation range

Item	Symbol	Conditions	Rated value	Unit
Power voltage	V_{DD}	-	4.5 ∿ 7	V
Data hold voltage	V_{DH}	-	2.2 ∿ 7	V
Crystal frequency	$f_{(XT)}$	-	32.768	kHz
Operating temperature	Top	-	-30 ∿ +85	°C

Note: The data hold voltage guarantees the clock operations, though it does not guarantee operations outside the IC and data input/output.

o DC characteristics

(V_{DD} = 5 V ±5%, Ta = -30 ∿ +85°C)

Item	Symbol	Concitions	MIN	TYP	MAX	Unit
H input voltage	V_{IH}	-	3.6	-	-	V
L input voltage	V_{IL}	-	-	-	0.8	V
L output voltage	V_{OL}	I_O = 1.6 mA	-	-	0.4	V
L output current	I_{OL}	V_O = 0.4 V	1.6	-	-	mA
H input current[1]	I_{IH}	V_I = 5 V	10	25	50	µA
L input current[1]	I_{IL}	V_I = 0 V	-	-	-1	µA
Input capacity	C_I	f= 1 MHz	-	5	-	pF
Current consumption	I_{DD}	f=32.768 kHz V_{DD}=5V/V_{DD}=3V	-	100/15	500/30	µA

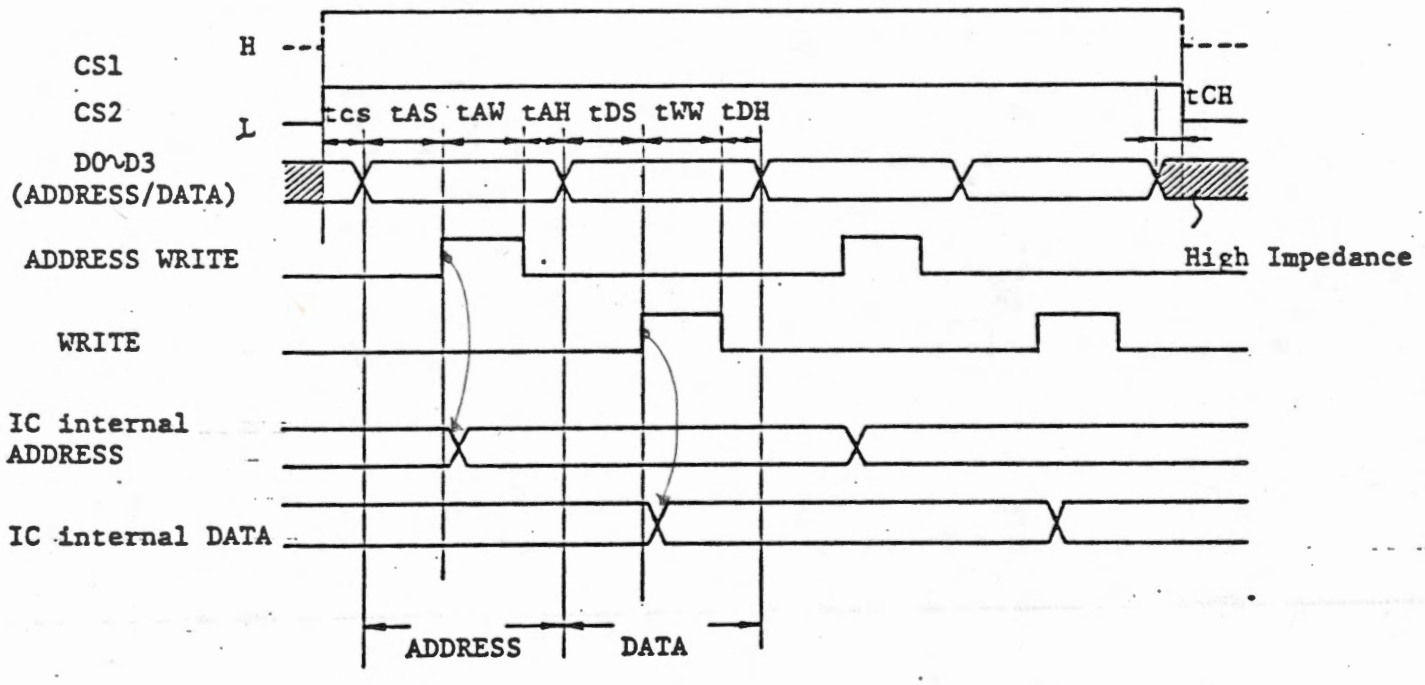
Note: 1. The XT, $\overline{XT}$, D0 - D3, and $\overline{BUSY}$ pins are not concerned.

o Switching characteristics

(1) WRITE mode

(V_{DD} = 5 V ±5%, Ta = 25°C)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
CS setup time	t_{CS}	-	0			µs
CS holding time	t_{CH}	-	0			µs
Address setup time	t_{AS}	-	0			µs
Address write pulse width	t_{AW}	-	0.5			µs
Address hold time	t_{AH}	-	0.1			µs
Data setup time	t_{DS}	-	0			µs
Write pulse width	t_{WW}	-	2			µs
Data hold time	t_{DH}	-	0			µs

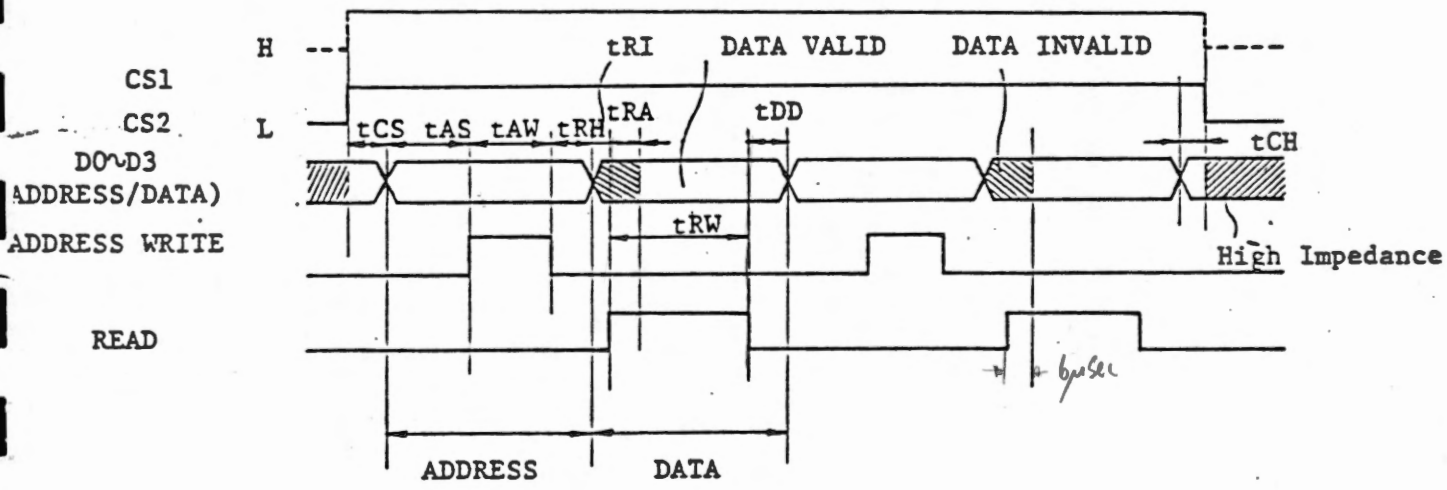


Note: ADDRESS WRITE and WRITE inputs are activated by the level, not by the edge.

(2) READ mode

(V_{DD} = 5 V ±5%, Ta = 25°C)

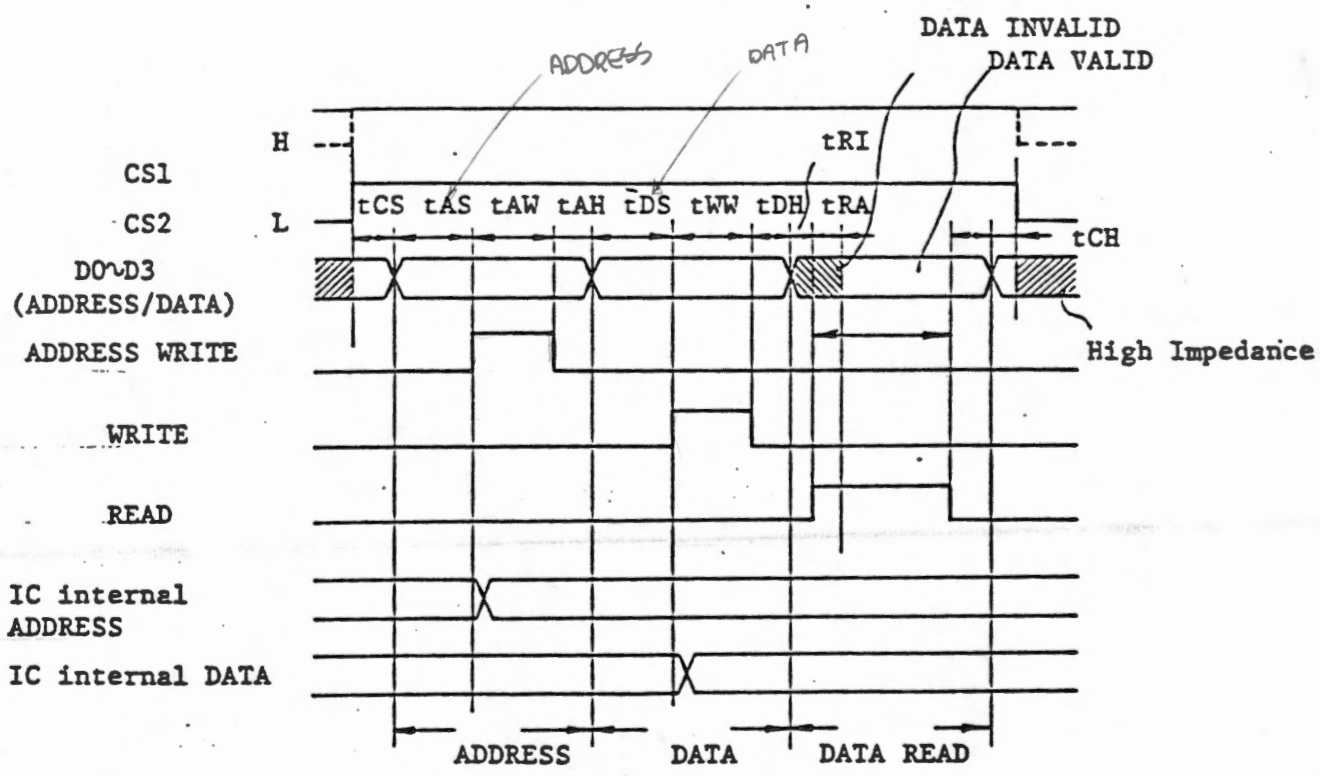
Item	Symbol	Conditions	MIN	TYP	MAX	Unit
CS setup time	t_{CS}	-	0			µs
CS holding time	t_{CH}	-	0			µs
Address setup time	t_{AS}	-	0			µs
Address write pulse width	t_{AW}	-	0.5			µs
Address hold time	t_{AH}	-	0.1			µs
Read access time	t_{RA}	-			6	µs
Read pulse width	t_{RW}	-	6			µs
Read delay time	t_{DD}	-			1	µs
Read inhibit time	t_{RI}	-	0			µs



Note: ADDRESS WRITE and READ inputs are activated by the level, not by the edge.

(3) WRITE & READ mode

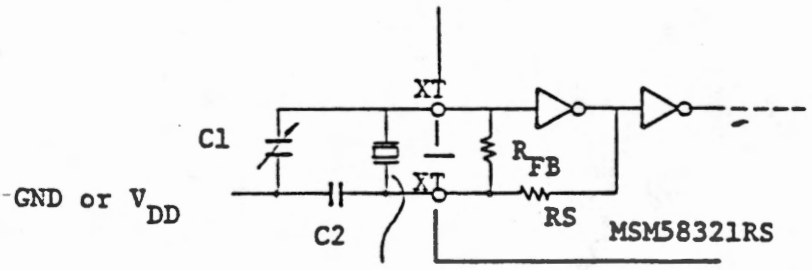
Item	Symbol	Conditions	MIN	TYP	MAX	Unit
CS setup time	t_{CS}	-	0			µs
CS hold time	t_{CH}	-	0			µs
Address setup time	t_{AS}	-	0			µs
Address write pulse width	t_{AW}	-	0.5			µs
Address hold time	t_{AH}	-	0.1			µs
Data setup time	t_{DS}	-	0			µs
Write pulse width	t_{WW}	-	2			µs
Data hold time	t_{DH}	-	0			µs
Read access time	t_{RA}	-			6	µs
Read pulse width	t_{RW}	-	6			µs
Read delay time	t_{DD}	-			1	µs
Read inhibit time	t_{RI}	-	0			µs



o Operations

(1) XT and $\overline{XT}$ pins

Crystal, capacitor, and trimmer capacitor for fine frequency adjustment are used in combination at the XT and $\overline{XT}$ pins.



R_{FB} = 10 MΩ typ
R_S = 200KΩ typ

X-TAL 32.768 kHz, The crystal impedance is 30 kΩ or less.

C1=C2=15∿30PF Fig. 2

See Figure 3 for inputting external clocks.
Input external clocks to the XT pin and open the $\overline{XT}$ pin.

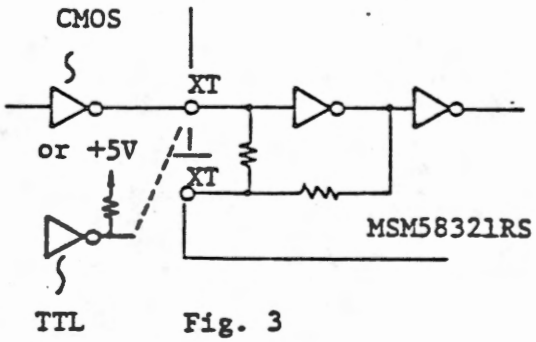


Fig. 3

(2) TEST pin

The TEST pin is used to measure this IC; if is normally open or connected to GND. It is recommended to connect it to GND to safe-guard against malfunctions from noise.

The TEST pulse can be input to the following nine digits:

S1, S10, MI1, MI10, H1, D1(W), MO1, Y1, and Y10

When a TEST pulse is input to the D1 digit, the W digit is also counted up simultaneously.

Input a TEST pulse as follows:

Set the address to either digit explained above, then input a pulse to the TEST pin while CS1 = CS2 = STOP = H and WRITE = L. The specified and succeeding digits are counted up. (See Figure 4.)

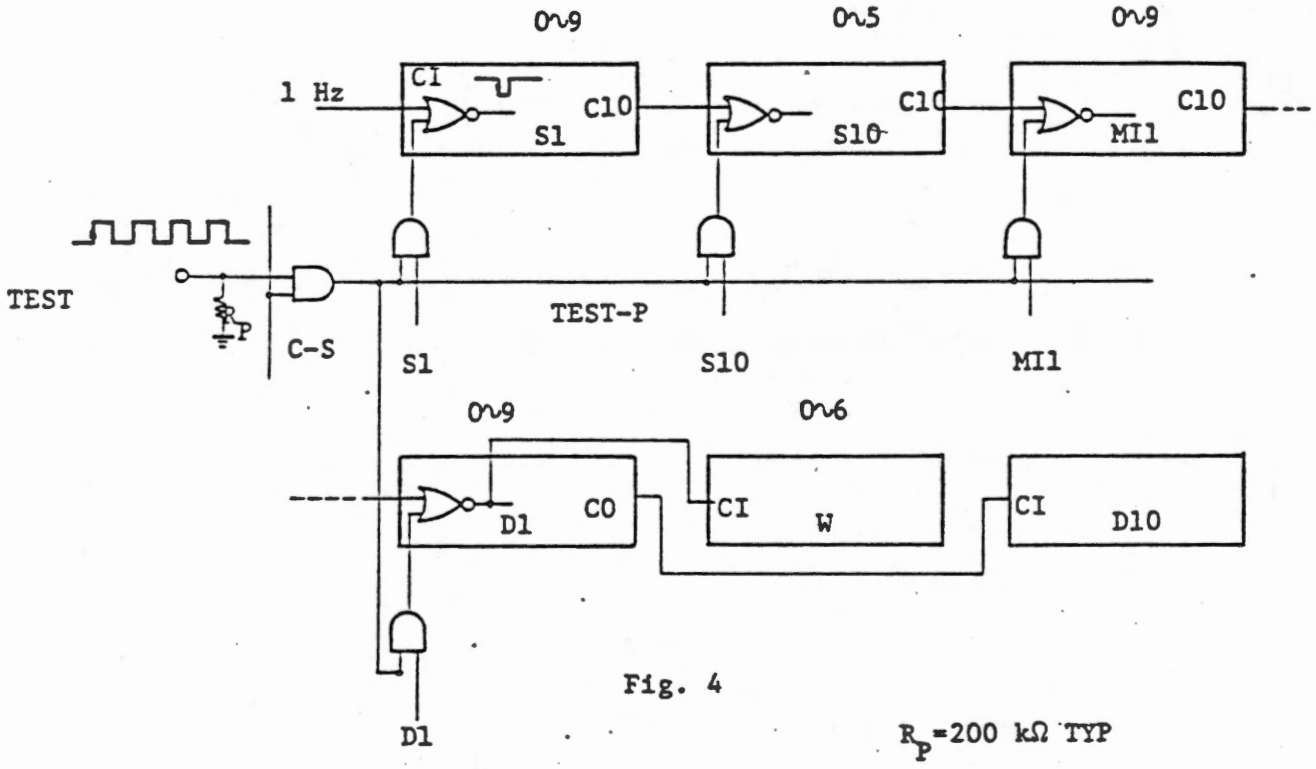
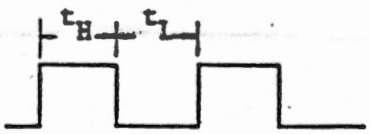


Fig. 4

R_P=200 kΩ TYP

A digit is counted up at the leading edge (changing point from L to H) of a TEST pin input pulse.

The pulse condition for TEST pin input at V_{DD} = 5 V ±5% is



t_H = 10μS MIN

t_L = 10μS MIN

(3) STOP pin AKTIV HØJ

The STOP pin is used to input on/off control for a 1 Hz signal. When this pin goes to the H level, 1 Hz signals are inhibited and counting for all digits succeeding the S1 digit is stopped. When this pin goes to the L level, normal operations are performed; the digits are counted up. This STOP input controls stopping digit counting. Writing of external data in digits can be assured by setting the STOP input to the H level to stop counting, then writing sequentially from the low-order digits.

(4) WRITE pin AKTIV HØJ

The WRITE pin is used to write data; it is activated when it is at the H level. Data bus data inside the IC is loaded to the object digit while this WRITE pin is at the H level, not at the WRITE input edge. (See Figure 5.)

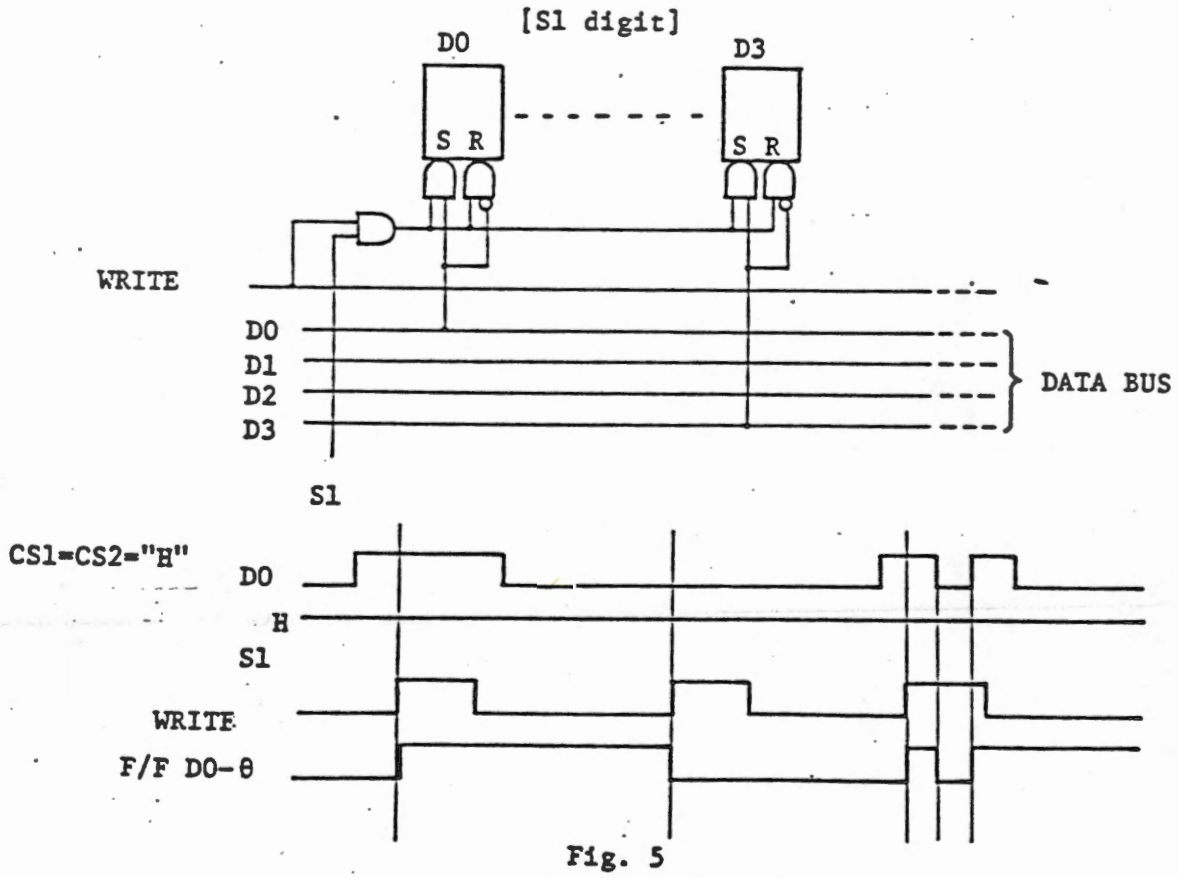
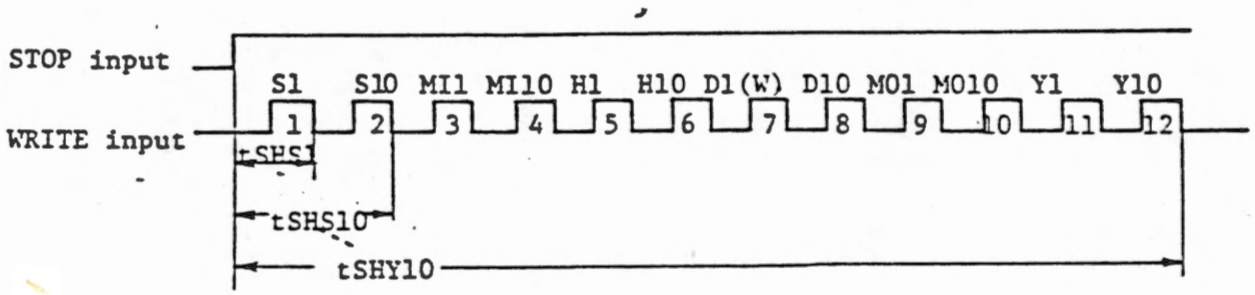


Fig. 5

Note that the timing relationships between the STOP and WRITE inputs vary by the related digit when counting is stopped by the STOP input to write data. The time (t_{SH}) between the STOP input leading edge and WRITE input trailing edge for each digit is limited to the minimum value. (See Figure 6.)



t_{SHS1} = 1 µs, t_{SHS10} = 2 µs, t_{SHMI1} = 3 µs, t_{SHMI10} = 4 µs, t_{SHH1} = 5 µs
t_{SHH10} = 6 µs, t_{SHD1} = 7 µs, t_{SHW} = 7 µs, t_{SHD10} = 8 µs, t_{SHMO1} = 9 µs
t_{SHMO10} = 10 µs, t_{SHY1} = 11 µs, t_{SHY10} = 12 µs.

If a count operation is continued by setting the STOP input to the level, write operation must be performed, in principle, while the $\overline{\text{BUSY}}$ output is at the H level. While the $\overline{\text{BUSY}}$ output is at the L level, count operations are performed by the digit counters and write operation is inhibited, but there is a marginal period of 244 µs from the $\overline{\text{BUSY}}$ output trailing edge. If the $\overline{\text{BUSY}}$ output goes to the L level during a write operation, the write operation is stopped temporarily within 244 µs and it is restarted when the $\overline{\text{BUSY}}$ output goes to the H level again. Figure 7 shows a time chart of $\overline{\text{BUSY}}$ output, 1 Hz signal inside the IC, and WRITE input.

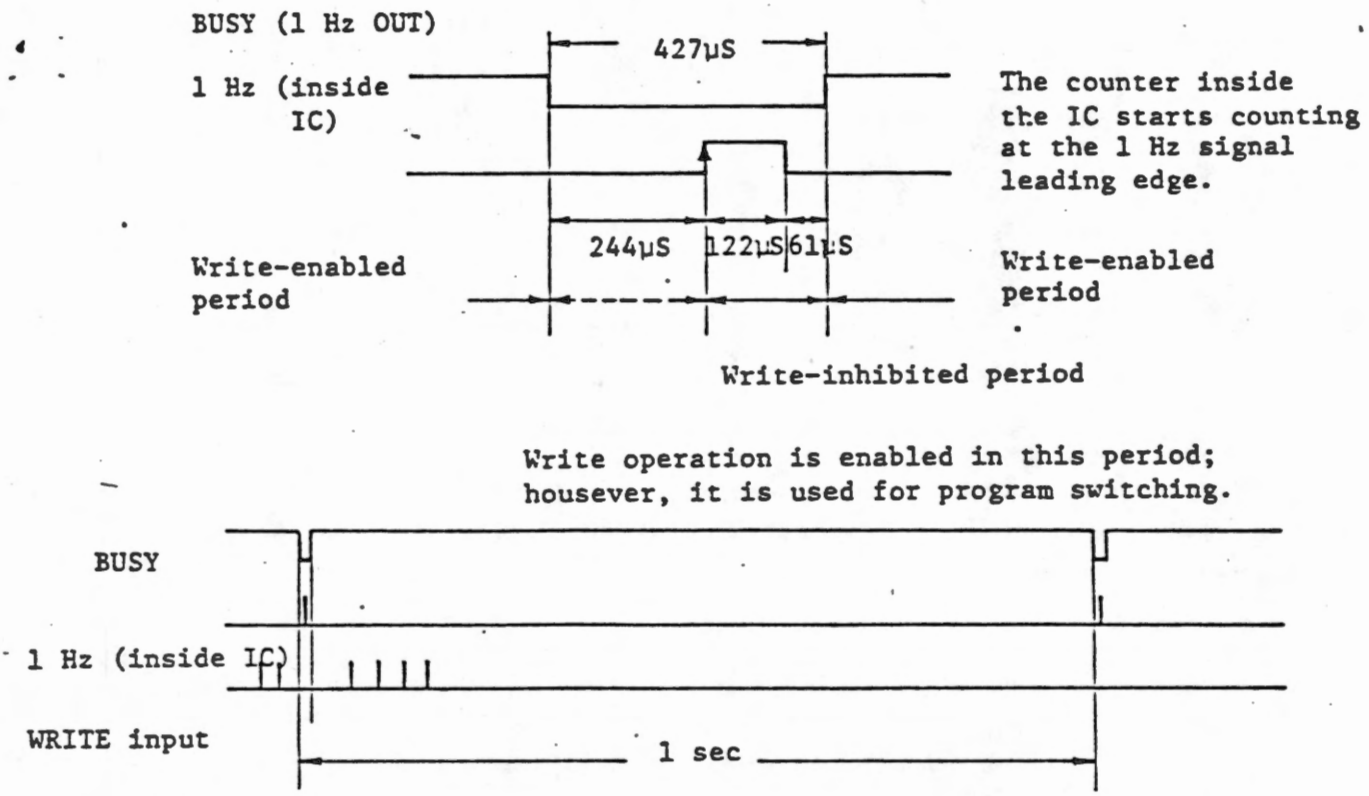


Fig. 7

If the WRITE and READ inputs go to the H level simultaneously, the WRITE input has priority.

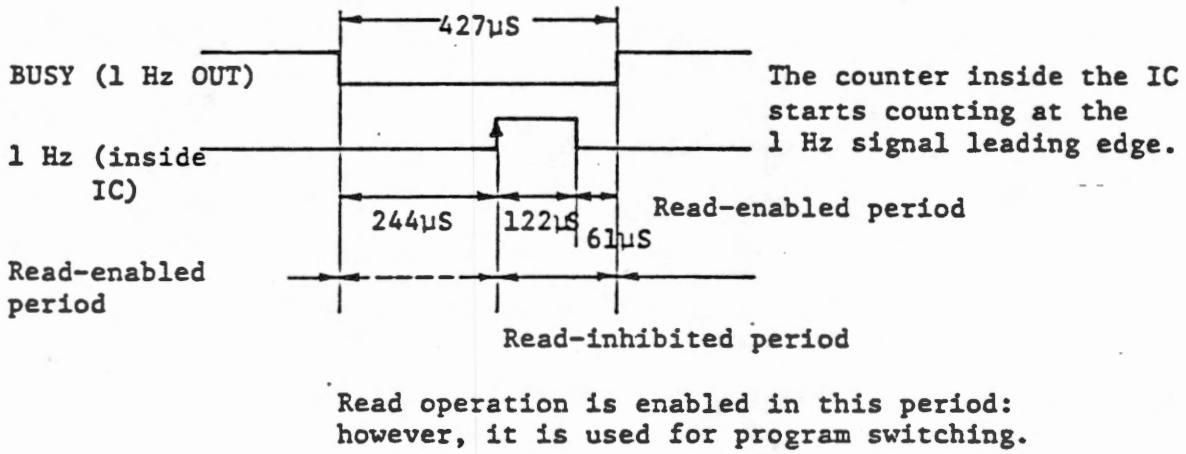
(5) READ pin AKTIV HIGH

The READ pin is used to read data; it is activated when it is at the H level. Address information is latched with ADDRESS LATCH inside the IC at the D0 - D3 and ADDRESS WRITE pins to select the object digit, then an H-level signal is input to the READ pin to read data.

If a count operation is continued by setting the STOP input to the L level, read operation must be performed, in principle, while the $\overline{\text{BUSY}}$ output is at the H level. While the $\overline{\text{BUSY}}$ output is at the L level, count operations are performed by digit counters and read data is not guaranteed, therefore, read operations are inhibited in this period. Figure 8 shows a time chart of the $\overline{\text{BUSY}}$ output, 1 Hz

signal inside the IC, and READ input.

A read operation is stopped temporarily within a period of 244 µs from the $\overline{\text{BUSY}}$ output trailing edge and it is restarted when the $\overline{\text{BUSY}}$ output goes to the H level again.



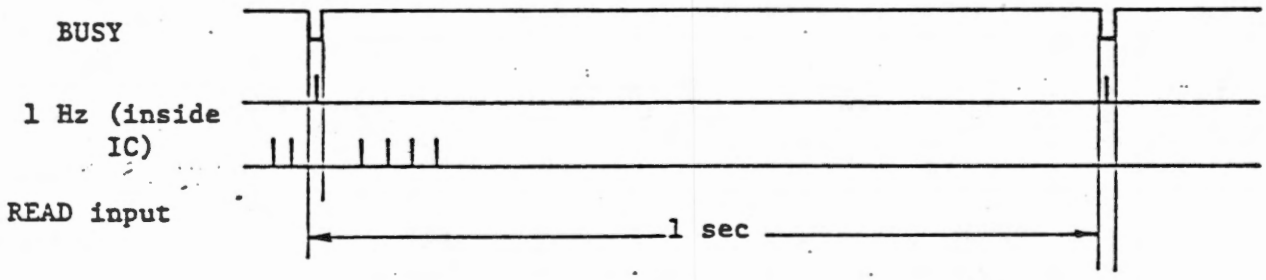


Fig. 8

If the counter operation is stopped by setting the STOP input to the H level, read operations are enabled regardless of the $\overline{\text{BUSY}}$ output.

A read operation is enabled by microcomputer software regardless of the $\overline{\text{BUSY}}$ output during the counter operation by setting the STOP input to the L level. In this method, read operations are performed two or more times continuously and data that matches twice is used as guaranteed data.

(6) CS1 and CS2 pins

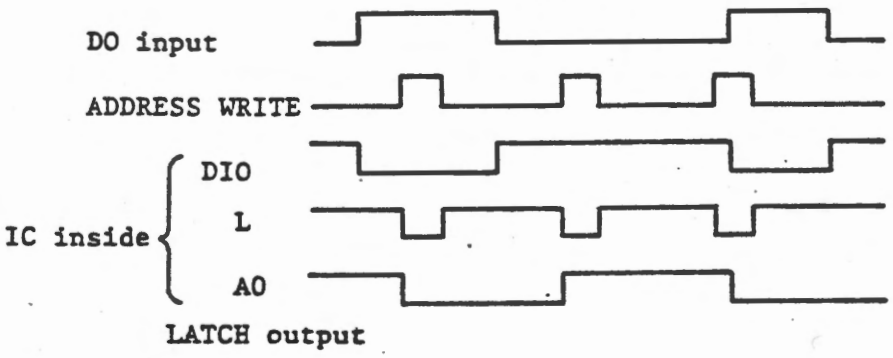
The CS1 and CS2 pins are used for external interfacing; they are activated when they are at the H level at the same time. If one of these pins goes to the L level, the STOP, TEST, WRITE, READ and ADDRESS WRITE input pins and D0 - D3 I/O bus pins are inactivated.

Since the threshold voltage V_T for the CS1 pin is higher than that for other input pins, it is connected to the peripheral circuit power drop detector and the CS2 pin is connected to a microcomputer.

(7) ADDRESS WRITE pin AKTIV HOJ

The ADDRESS WRITE pin is used to load address information from the D0 - D3 I/O bus pins to the ADDRESS LATCH inside the IC; it is activated when it is at the H level. This input is activated by the level, not by the edge. Figure 9 shows the relationships between the D0 address input, ADDRESS WRITE input, and ADDRESS LATCH input/output.

Fig. 9



(8) $\overline{\text{BUSY}}$ pin

The $\overline{\text{BUSY}}$ pin outputs the IC operation state. It is N-channel MOSFET open-drain output. An external pullup resistor of 4.7 kΩ or more must be connected (see Figure 10) to use the $\overline{\text{BUSY}}$ output. The signals are output in negative logics. If the oscillator oscillates at 32.768 kHz, the frequency is always 1 Hz

regardless of the CS1 and CS2 unless the D output of the ADDRESS DECODER inside the IC is H (CODE = H·L·H·H) and CS1 = CS2 = WRITE = H.

Figure 11 shows the $\overline{\text{BUSY}}$ output time chart.

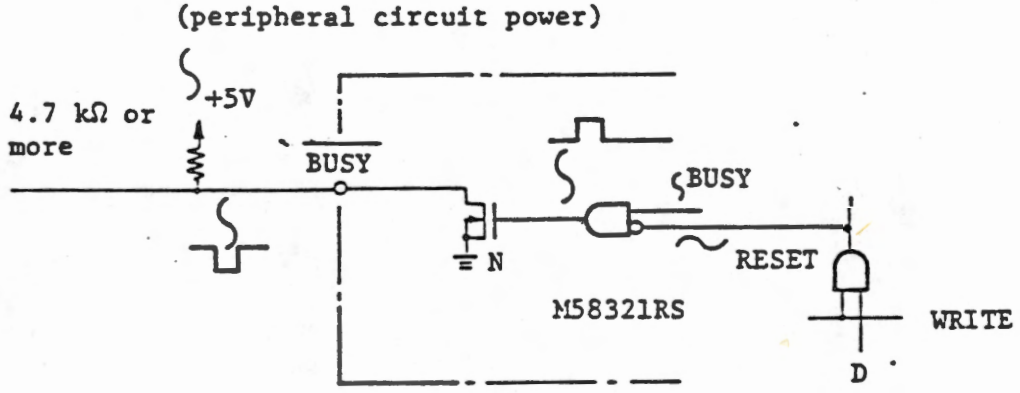
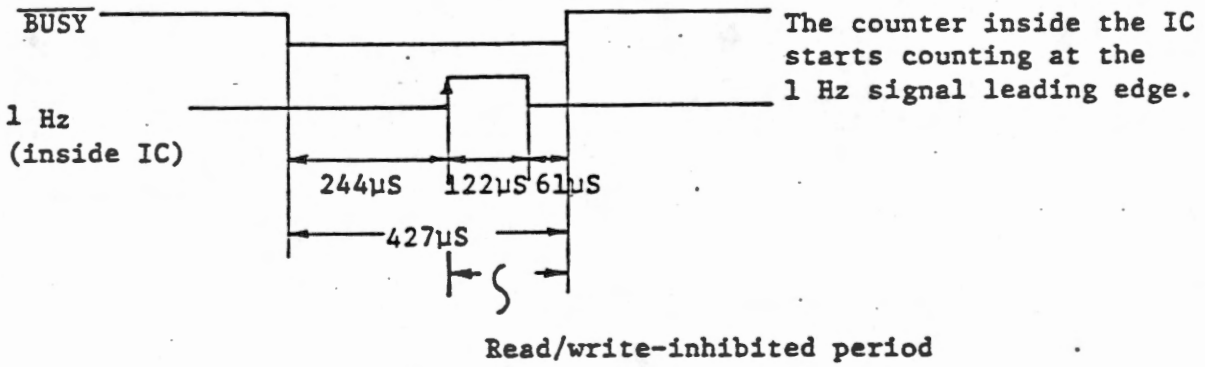


Fig. 10



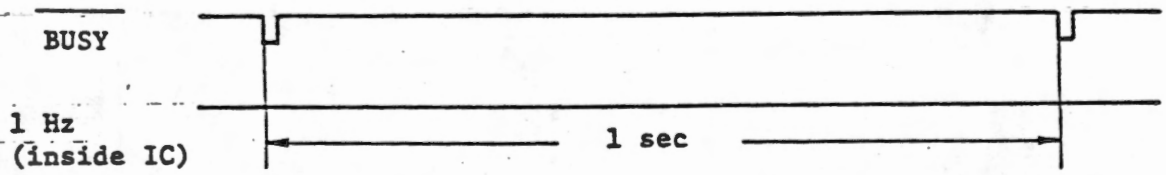


Fig. 11

(9) The D0-D3 pins are bidirectional buses for data input/output. See Figure 12.

o READ mode

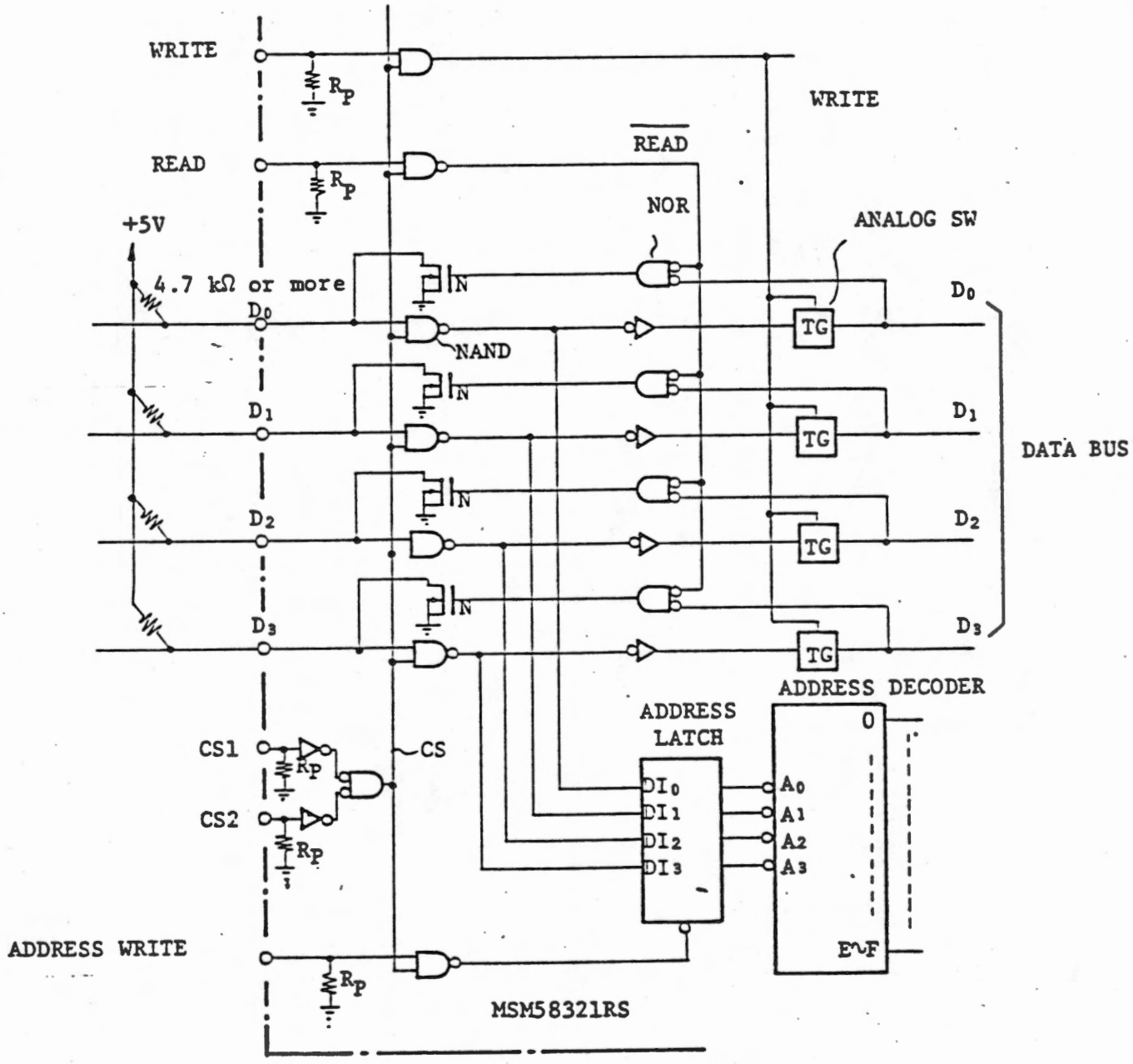
If CS1 = CS2 = H, WRITE = L, and READ = H, the ANALOG switch is in the OFF state. If data bus D0 is at the H level, the NOR gate output goes to L, N-channel MOSFET goes to OFF, and the D0 pin goes to the H level because it is pulled up to +5 V with the pull-up resistor; if it is at the L level, the NOR gate output goes to the H level, N-channel MOSFET goes to ON, therefore, the D0 pin goes to the L level. In the READ mode, four HAND gates connected to the D0-D3 pins are meaningless.

o WRITE mode

If CS1 = CS2 = H, READ = L, and WRITE = H, the output of four NOR gates connected to the data buses goes to the L level and N-channel MOSFET goes to OFF. The ANALOG switch goes to ON and data information from the D0-D3 pins appear at the data buses via the NAND gate, INV gate, and ANALOG switch.
In the WRITE mode, the N-channel MOSFETs connected to the D0-D3 pins are meaningless because they are set OFF.

o ADDRESS WRITE mode

If CS1 = CS2 = H, WRITE = READ = L, and ADDRESS WRITE = H, the N-channel MOSFETs connected to the D0-D3 pins and the ANALOG switch connected to the data buses are set OFF. Address information input to the D0-D3 pins is loaded to the ADDRESS LATCH via the NAND gate with an ADDRESS WRITE signal. The output of ADDRESS latch is connected to the input of ADDRESS DECODER; the ADDRESS DECODER output is decided by the ADDRESS LATCH output.



Note: Connect external pull-up resistors of 4.7 kΩ or more to the D0-D3 pins.

Fig. 12

(10) Reference signal output

Reference signals are output from the D0-D3 pins under the following conditions:

Conditions	Output pin	Reference signal frequency	Pulse width	Output logic
WRITE = L	D_0	1024 Hz	488.3 µs	Positive logic
READ = H	D_1	1 Hz	122.1 µs	Negative logic
CS1 = CS2 = H	D_2	1/60 Hz	122.1 µs	Negative logic
ADDRESS CODE (L·H·H·H or H·H·H·H)	D_3	1/3600 Hz	122.1 µs	Negative logic

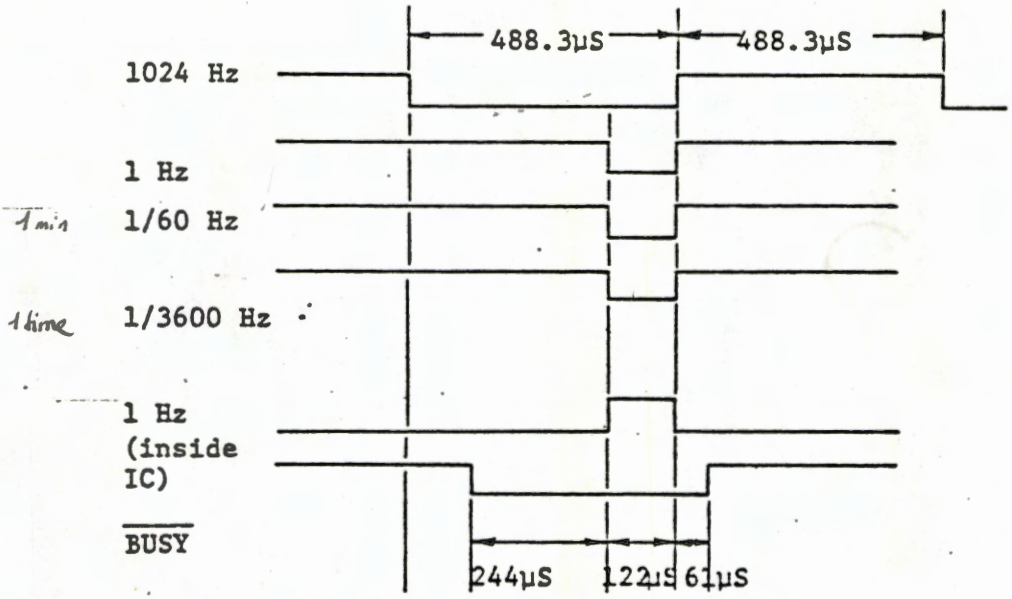


Fig. 13

$$122.1\mu S = \frac{10^{-3}}{32{,}768} \times 4$$

$$488.3\mu S = \frac{10^{-3}}{32{,}768} \times 16$$

(11) Frequency divider and $\overline{\text{BUSY}}$ circuit reset

If A0-A3 = H·L·H·H is input to ADDRESS DECODER, the DECODER output (D) goes to the H level. If CS1 = CS2 = H and WRITE = H in this state, the 5 poststages in the 15-stage frequency divider and the $\overline{\text{BUSY}}$ circuit are reset.

in this period, the $\overline{\text{BUSY}}$ output remains at the H level and the 1 Hz signal inside the IC remains at the L level, and counting is stopped. If this reset is inactivated while the oscillator operates, the $\overline{\text{BUSY}}$ output goes to the L level after 1000.1221 ±31.25 ms and the 1 Hz signal inside the IC goes to the H level after 1000.3663 ±31.25 ms. These times are not the same because the first ten stages in the 15-stage frequency divider are not reset. (See Figure 14.)

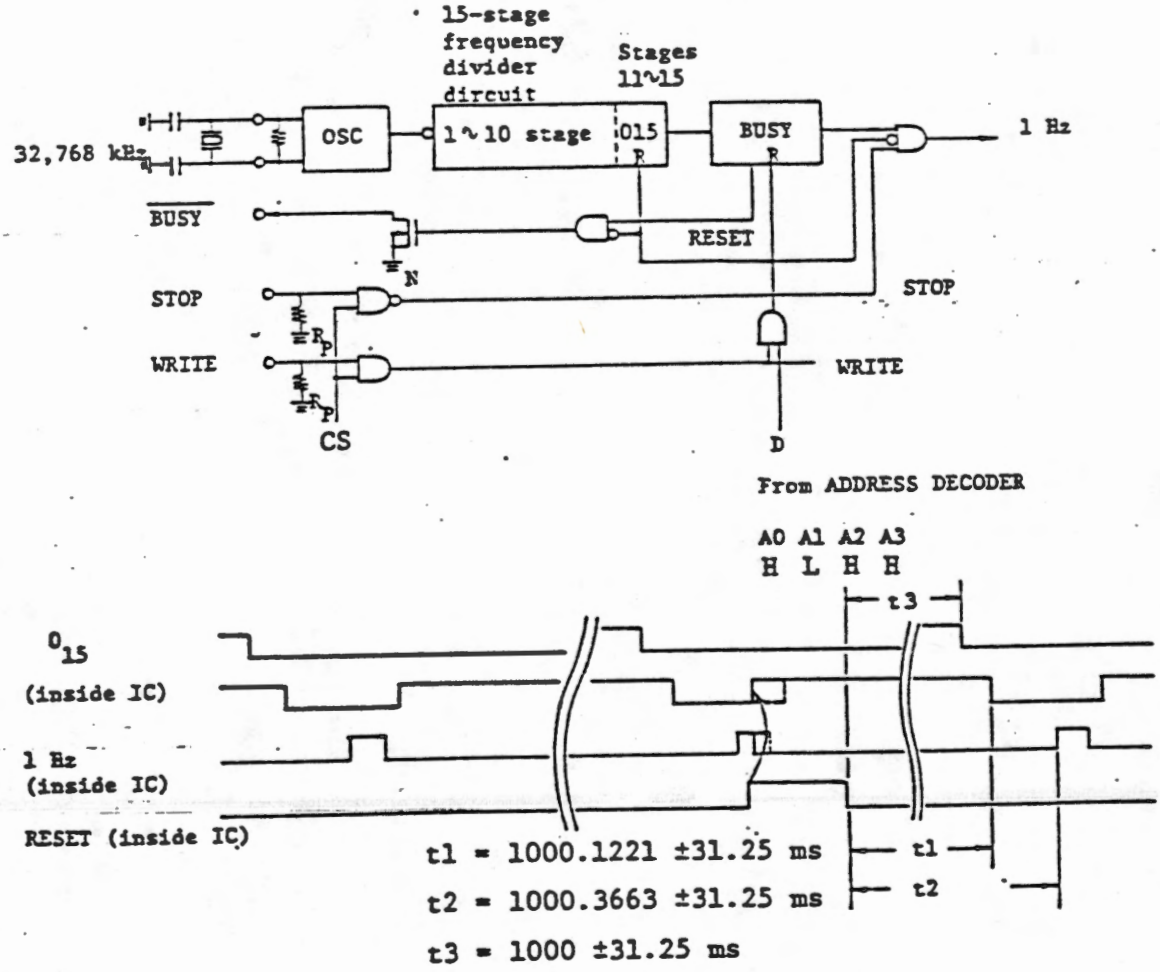


Fig. 14

(12) Leap year selection

This IC is designed to select leap year automatically.
Four types of leap years can be selected by writing a select signal in the D2 and D3 bits of the D10 digit (CODE = L·L·L·H). (See Table 1 for the functions.)

Gregorian calendar, Japanese Showa, or other calendars can be set arbitrarily in the Y1 and Y2 digits of this IC. There is a leap year every four years and the year number varies according to whether the Gregorian calendar or Showa is used. There are four combinations of year numbers and leap years. (See Table 1.)

No. 1: Gregorian calendar year. The remainder obtained by dividing the year number by 4 is 0.

No. 2: Showa year. The remainder obtained by dividing the year number by 4 is 3.

No. 3: The remainder obtained by dividing the year number by 4 is 2.

No. 4: The remainder obtained by dividing the year number by 4 is 1.

No. 1	Calendar	D10 digit		Remainder obtained by dividing the year number by 4	Leap years (examples)
		D2	D3		
1	Gregorian	L	L	0	1980, 1984, 1988, 1992, 1996, 2000, 2004
2	Showa	H	L	3	(83) (87) (91) (95) (99) 55, 59, 63 67, 71, 75, 79
3		L	H	2	82, 86, 90, 94, 98, 102, 106
4		H	H	1	81, 85, 89, 93, 97, 101, 105

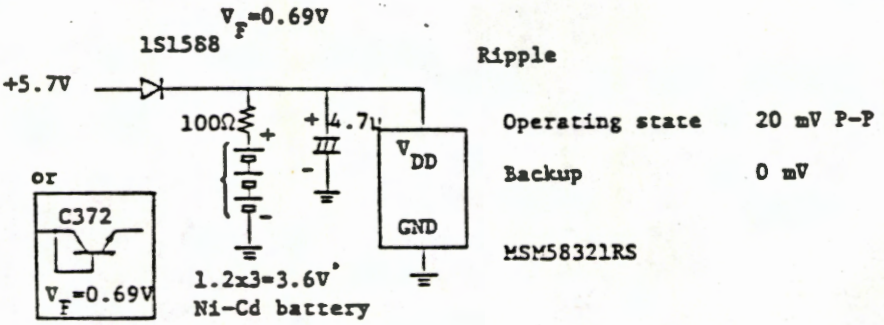
Table 1

(13) Handling of unused pins

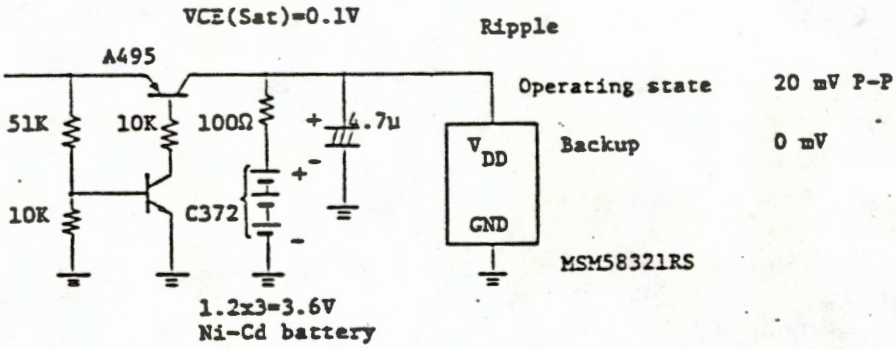
Open or ground unused pins (pins other than the XT, $\overline{XT}$, D0–D3, and $\overline{BUSY}$ pins).

MSM58321 RS power circuit examples

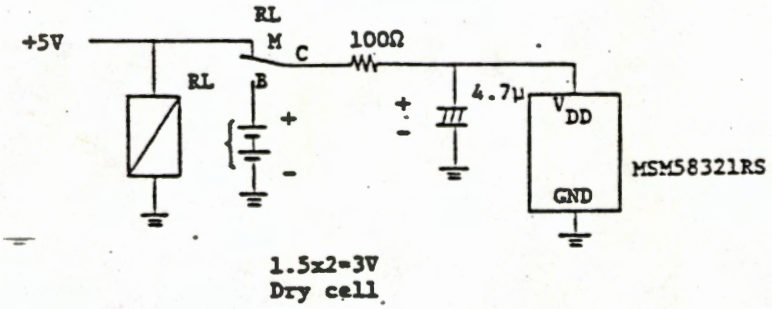
Example 1.



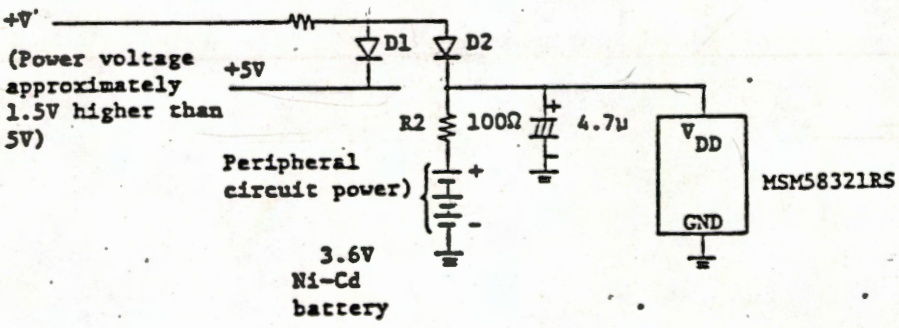
Example 2.



Example 3.



Example 4. (Recommended circuit)



Note: Use the same diodes for D1 and $\overline{D2}$ to reduce the level difference between +5V and V_{DD} of the MSM 58321RS.