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RC750, iAPX186, PC, Selftest Technical Guide

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Abstract:

This manual describes the RC750, iAPX186, PC, Selftest which contains a number of testprograms for power up testing and hardware maintenance of the RC750, a personal computer, based upon a 16 bit 80186 microprocessor.
The program performs the basic system hardware initialization. It also contains a hardware debugging program ("Snooper").
It is Prom resident and is an integrated part of the system bootloader.
This manual is directed toward technical personal.

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1. INTRODUCTION 1.

RC750 is a personal computer based upon the 16 bit microprocessor 80186 and the display controller 82730.

It is equipped with a power up selftest which is an integrated part of the system bootloader.

The RC750, PC, Selftest is both a power up test and a tool for hardware maintenance. To meet these two commands the test can run in two modes.

These will in the following be referred to as user mode (power up) and technical mode.

This manual will primarily concentrate on the technical mode.

Be aware that the RC750, PC, Selftest is a hardware debugging tool, and that it will support fault finding via a 2400 bps modem line connected to serial line B.

1.1 The Object of the Tests 1.1

It is the intention of the RC750, PC, Selftest to cover three in the nature different needs.

a) The RC750 is equipped with a power up selftest (user mode), consisting of a sequence of different test programs. These tests are organized with rising complexity, so that as far as possible no part of the hardware is used in the test, before it has been tested. This should ensure, when the selftest has passed, that the hardware of the RC750 is in a condition which enables system software to be loaded.

   It requires no interaction from the user, when the hardware is an error-free condition.

b) It gives the production department the possibility of using the selftest in technical mode as a burn in facility. In the technical mode it will be possible to run some additional tests which is not run at power up. This is uptained by the fact that the selftest can be stimulated from a connected keyboard, or alternatively from a console connected to the serial line B. The test programs in the RC750, PC, Selftest may either be run in loop mode, or sequencial (including all tests).

c) It gives the Technical Service department a diagnostic tool and a verification of the functionality of the hardware.

1.2 Automatic Hardware Configuration 1.2

The RC750, PC, Selftest has besides testing, the job of examining the hardware configuration of the system, in which it resides. The result of this configuration will be placed in a configuration record in address 0000:0050 and upwards. See fig. 1.

The configuration is used by the Selftest to determine the flow of some of the testprograms. It is also used by the bootloader as a basic hardware configuration description.

The configuration record will be updated at both "cold" and "warm-boot".

address	vector types
0000:0000	iAPX186 interrupt vectors
0000:0050	Configuration record
0000:0080	8259 interrupt vectors
0000:0100	8274 interrupt vectors

```
config_type:
   main_menu_size      DW  0,0
   total_menu_size     DW  0,0
   CRT_cmd_block       DW  0,0
   RTC_sec_source      DB  false
   net_state           DB  false
   aux3_state          DB  false
   aux2_state          DB  false
   aux1_state          DB  false
   aux0_state          DB  false
   colour_option       DB  false
   no_of_floppy        DB  0
   SCSI_vector         DB  0
   keyb_test_result    DB  0
   keyb_id             DB  0
   last_typed          DB  'A'
```

Figure 1: Configuration record.

The different fields in the record should be interpreted as follows:

main_mem_size: holds in a double word the size of the main memory. It is derived from bit 6 and 7 in input port 220H. This means that the memory can be of 4 different sizes 256K bytes, 512K bytes, 768K bytes or 1 M byte.

total_mem_size: holds in a double word the size of all CPU addressable RAM memory, incl. pizel memory. In this system main_mem_size + 32 K bytes.

CRT_cmd_block: Holds in a double word the real address of the 82730 Display controller command block. This information is necessary for a loaded display driver.

RTC_sec_source: This byte is set to true (0FFH), if a CDP1879 real time clock is installed instead of a MM58167. (Bit 5 in input port 220H).

net_state: This byte is set to true (0FFH), if the system is equipped with a net controller based on the 82586 chip.
(Bit 4 in input port 220H).

aux_state: The four bytes named aux0_state to aux3_state is set to true (0FFH), if any not predefined options is installed. The bytes will reflext to the state of bit 0-3 in input port 220H.

colour_option: This byte is set to true (0FFH), if a colour display is connected to the RC750.
(Bit 5 in the 8255 PPI port 72H).

no_of_floppy: This byte will contain the number of flexible diskette drives installed in the RC750 chassis.

SCSI_vector: Each bit in this byte, if set to "1", will indicate that a SCSI_controller is connected to that SCSI-bus address.

keyb_test_result: This byte holds the result of the keyboard selftest. The result will be zero, if no error occurred. The result is the first "character" send by the keyboard after power up.

keyb_id: This byte holds the nationality code of the keyboard. The nationality code is set in the switches on the keyboard. The nationality code is the second "character" send to the keyboard after power up.

last_typed: This byte holds the last typed character before either entering the bootloader or changing the mode of the selftest from user mode to technical mode. It will be used by the bootloader to decide the load medium.

On fig. 2 it is possible to locate the 8255 (port 72H) and the configuration port (port 220H).

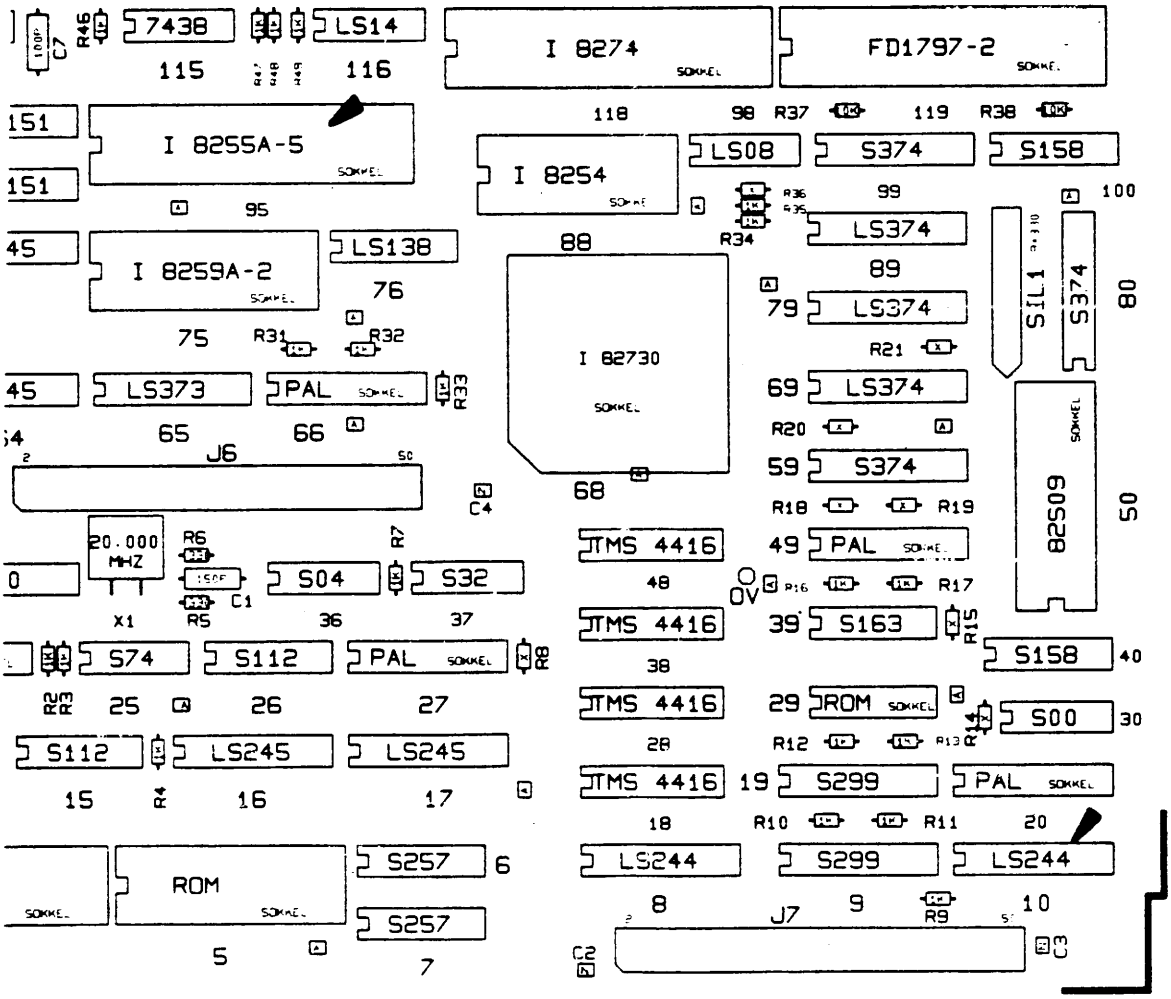


Figure 2: Locate the configuration port and the 8255.

1.3 Selftest Equipment

1.3

As the RC750, PC, Selftest is an integrated part of the bootload facility, it does not require installation. When run as a power up test, it does not require any special equipment either.

When run in the technical mode, the following is required:

KBL 580 : Test cable for the 8274 SIO test.

One or two formatted flexible diskettes for the Flexible disk test.

The RC750, PC, Selftest and Bootloader PROM's is installed in IC position 4 and 5.

See fig. 3 to locate the PROM positions.

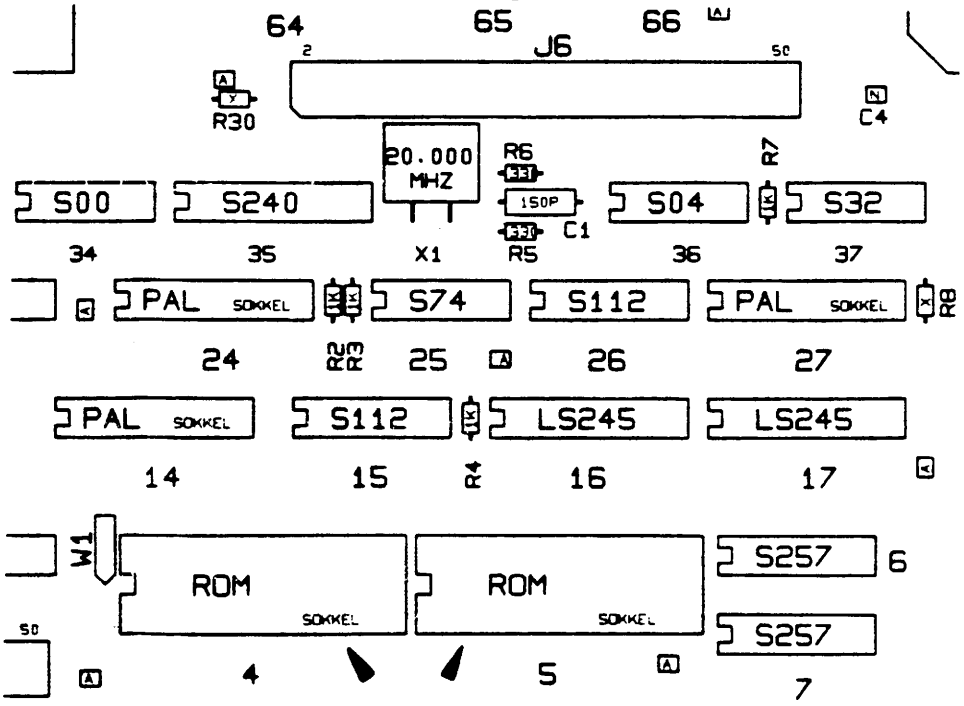


Figure 3: Locate the PROM's.

1.4 List of Included Tests

Besides the test programs, the RC750, PC, Selftest includes a test administrator and a library of some simple input and output routines.

The simple test administrator administers the mode in which a particular test is run. Different modes are determined by parameter settings. See chapter 2.

The test programs are as follows:

PROM checksum test - a simple PROM checksum is calculated. It is only executed once after each power up initialization.

RAM memory test - a modulus 3 pattern test of the pixel and the main RAM memory.

RAM refresh test - a test of the 82730 Display controllers capability of performing RAM memory refresh.

8255 PPI test - a simple test of the parallel port 8255 by shifting zeroes and ones through the port bits of port A.

Centronic Interface test - a test of the parallel Centronic Interface control and data signals using internal loop back.

Non Volatile Memory test - This test will calculate the checksum of all the nibbles in the NVM, seen as bytes. The checksum should be zero.

iAPX186 Timer test - a test of the on-chip timer1 and timer2 controllers of the iAPX186.

iAPX186 DMA test	- a test of both on-chip direct memory access controllers performing a memory to memory transport.
iAPX186 Interrupt test	- a test of the on-chip interrupt controller and its capability of generating interrupt from an on-chip timer.
8259 Interrupt test	- a test of the 8259 interrupt controller and its capability of generating interrupts from the 82730 display controller.
Keyboard test	- receive and check the result from the keyboard power up selftest.
8274 SIO test	- a test of the function of the 8274 serial interface controller and the connected interface. It includes X21 and V24 test as well as a data loop back test. Test cable KBL580 must be used.
Display Demo test	- This program will demonstrate some of the facilities of the 82730 display controller. It cannot detect any errors.
Flexible disk test	- a test of the FD1797-02 flexible disk controller and the drives that are ready. It will perform seeks and read sectors.
Winchester disk test	- a test of the SCSI-interface the disk controller (e.g. DTC510A) and a specific drive. It is only performing seeks and read blocks.

Messages from the test programs are explained along with the description of the individual programs. The message "END" is used by all test programs, and indicates that no error has been detected.

2. TESTADMINISTRATOR 2.

The RC750, PC, Selftest is equipped with a simple test administrator, that administers the mode in which a particular test is run.

By default all the tests are run sequential and the selftest is terminated by entering the bootloader. The main purpose of the test administrator is to compute the address of the next test in sequence and to generate errormessages to be written on the display (and obtional output via the SIO channel B).

Fig. 4 gives an overview of the RC750, PC, Selftest flow.

2.1 Selftest User Mode 2.1

When power is turned on (or the reset botton pushed), the RC750 will start with its selftest. It will initially be in its socalled "user mode".

The time consumed by the Selftest is proportional with the size of system main memory. For a minimum configuration (256 K bytes of main memory) the time is app. 8 seconds.

While the selftest is in progress the following will be seen on the first line of the display.

**** Rc750, TEST, V. 1.0 ****

The selftest consists of a set of test programs each testing its own limited part of the hardware. For every of these test programs an asterisk will be written on line 3 of the display.

When the selftest has passed without any error, the system bootloader will take over the control.

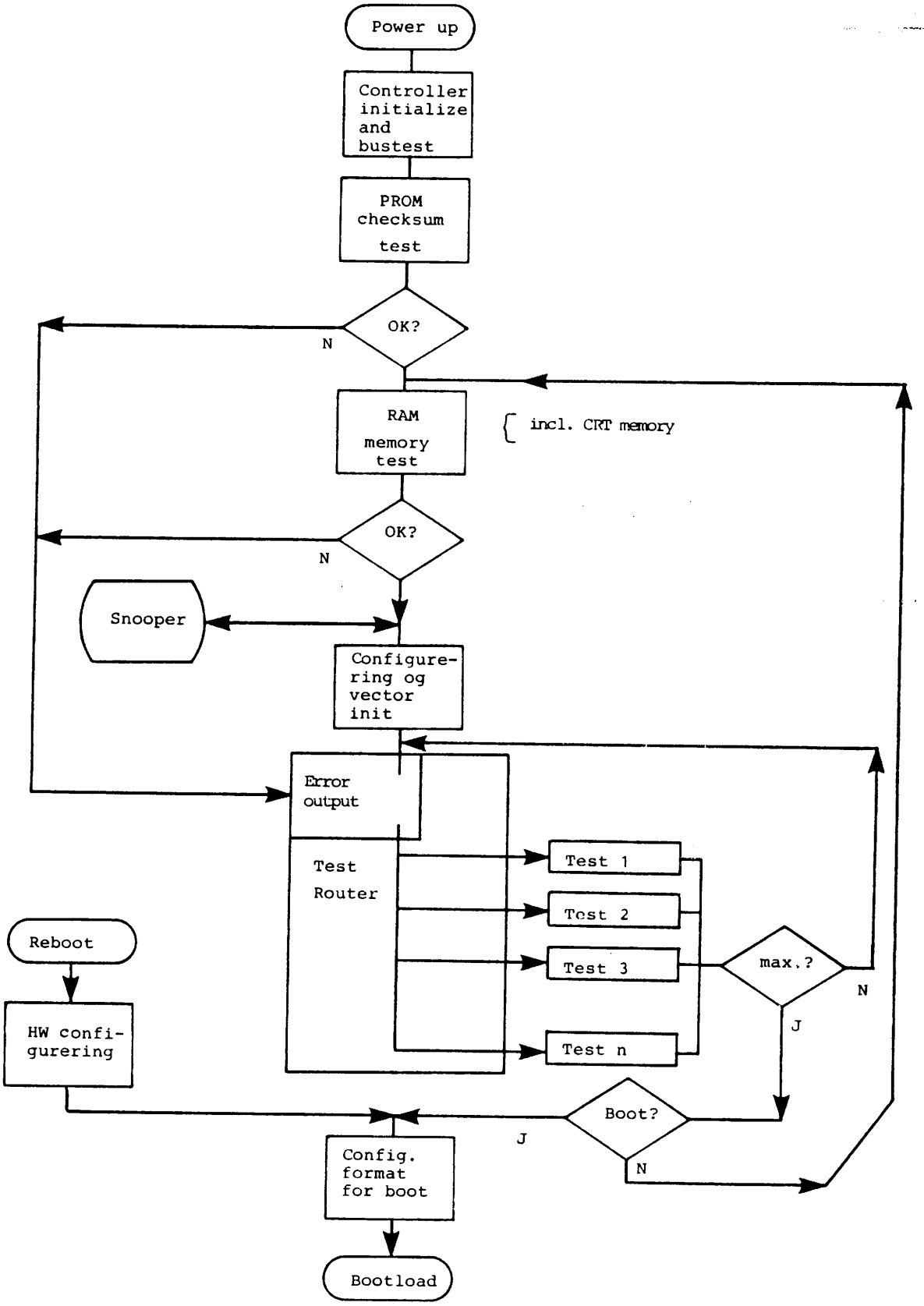


Figure 4: Test flow.

It should be noted, that the unit, flexible disk or Winchester disk, from which the system software should be loaded, has not been tested automatically by the power up selftest.

The 8274 serial interface, the flexible disk and the Winchester disk can be tested in the technical mode.

Should an error occur during the selftest, the following reaction could be observed:

The bottom line of the display, the socalled status line, will hold the text "ERROR xxxxx" in inverted writing, where "xxxxx" is a number which identifies the error occurred.

In conjunction to this, the loud speaker in the monitor will produce a number of sounds, which is equivalent to the above mentioned number. This means that the user has an audible feed back of the error number. The serie of sounds is devided into groups of 4, where every fourth sound is of a lower frequency than the three others.

The sound feed back can be useful, if an error in connection with the display has occurred.

A list of error numbers can be found in Appendix A.

2.2 Selftest Technical Mode 2.2

A change in the mode of the selftest from user mode to technical mode, may be performed after power up, when the following conditions are fullfilled.

The keyboard should have "clicked" it's three - OK clicks - and the memory test should be ended (seen by the appearance of the first asterisk on line 3 in the user picture).

It is also possible to make the change, when the selftest has discovered an error and stopped the execution.

Anyway the decision to change the mode must be taken before the bootloading is started, else the control can run out of hands.

The attention character that will change the mode of the selftest from user mode to technical mode is <space>.

When the space bar has been pressed the picture on the screen will be switched and the following menu will appear.

2.2.1 Menu 2.2.1

```
- - - - MENU - - - -
<0>: proceed test
<1>: list of tests
<2>: enter snooper
<3>: change parameters
<4>: show hardware configuration
SELECT FROM MENU:
```

Entry <0> is used, when a return to the testing phase is wanted.

Entry <1> will respond with a complete list of tests included in the RC750, PC, Selftest. The list shows a significant number for each test. This number is to be used when changing the parameters. See section 2.3 for a list of included tests.

Entry <2> will start a special hardware debugging program which enables the technician to manipulate with RAM data and input, output ports. See chapter 6 for a description of this program.

*** Note: That changing the content of RAM memory words or performing output to ports, may have some drastic effects to the selftest.

Entry <3> will enable the user to change the flow of the selftest (e.g. loop in a specific test). See subsection 2.2.3 for a description of how to change parameters.

Entry <4> will show the important part of the hardware configuration. See subsection 2.2.2.

When returning from one of the entries the main menu will be shown again.

2.2.2 Hardware Configuration 2.2.2

When entry <4> from the main menu is selected, a text like the following will be written:

```
RAM   size, NET, Diskettes, SCSI controller
-------------------------------------------
288   KB    NO   00001       0000
```

The field "RAM size" shows the size of the system RAM memory incl. the display pixel memory.

The field "NET" indicates, if the system is equipped with a micro net controller.

The field "Diskettes" shows the number of flexible disk drives installed in the system.

The field "SCSI controller" will show on which SCSI-bus address a controller is connected.

2.2.3 Parameters 2.2.3

The flow of the RC750, PC, Selftest is based upon the fact that each test program receives a set of parameters as input and delivers a buffer of error information as output.

The parameters are contained in a 16 bit word variable, a socalled switch variable, which survives the memory test in a CPU register. This variable contains the information necessary for the test administrator to manage the flow of the test programs. See fig. 5 for a description of this switch variable.

It is possible for the user to manipulate some of these parameters by using entry <3> from the menu. This will cause the questions as shown in fig. 6 to be asked. These questions must be answered one by one. the answers to the "<Y/N>" questions are "Y", "N" or carriage return (unchanged).

The answer to the "test no.:" question is a legal test number and/or carriage return.

name	initial value	comment
halt_bit	1	1: halts execution when an error is detected. 0: bypasses errors.
loop_bit	0	1: repeats the selection of the test specified. 0: sequential flow.
tech_bit	0	1: run test with display in technical mode. 0: run test with display in user mode.
boot_bit	1	1: enter bootloader when test number is bigger than the number of the last test in power up. 0: Stay in the selftest, and do not enter bootloader
status_bit	0	1: suppress status check. 0: perform status check.
data_bit	0	1: suppress data check. 0: perform data check.
warm_boot	0	1: bypass selftest when warm boot. 0: run selftest when cold boot.
not_used	0	
test_no	00	identification of test program.

Figure 5: Test parameter variable.

```
> PARAMETERS <

halt on error          ? <Y/N>, Y/
loop in test           ? <Y/N>, N/
boot after test        ? <Y/N>, Y/
suppress status check  ? <Y/N>, N/
suppress data check    ? <Y/N>, N/
test no.: 00000/
```

Figure 6: Parameter setting.

2.3 Test Numbers

2.3

The relationship between test numbers and actual test programs are as follows:

Test no	Test name
0	memory test
1	RAM refresh test
2	PPI 8255 test
3	Centronic Interface test
4	Non volatile memory test
5	iAPX186 Timer test
6	iAPX186 DMA test
7	iAPX186 interrupt test
8	8259 interrupt test
9	Keyboard selftest result
10	SIO 8274 test
11	Display test
12	Flexible test
13	Winchester disk test

The test numbers 10 to 13 is not run in the default power up sequence. They must be requested explicit in looping mode or the selftest must be run in the big sequencial loop with the "boot after test?" set to "N".

A list of test numbers can be seen, using the entry <1> in the main menu.

2.4 Output from a Test 2.4

Every test program will send some test information to an error buffer. At the end of every test program, the selftest will inform about its state, error or no error, to the user by writing on the display.

An error message will be written in two different places with the following formats:

On the status line an error message will have the format:

```
ERROR: xxxxx
```

where "xxxxx" is a unique number which identifies the error occurred.

When the display is in technical mode, an error message will also have the following format:

$$\{\langle\text{test name:}\rangle\}\ ,\left\{\begin{matrix}\{\langle\text{END}\rangle\}\\ \{\langle\text{error type}\rangle\}\end{matrix}\right.\ ,\ \{\langle\text{test}\rangle\langle\text{error data}\rangle\}_{0}^{N}\ \Bigg\}$$

<error type> is a primary errortext informing about the specific error. <text> is of the kind "addr:", "exp:" and the like.

2.5 Remote Hardware Debugging 2.5

The RC750, PC, Selftest is equipped with a facility for remote hardware debugging. This facility is implemented with the help of the 8274 Serial Input Output controller channel B.

It will be initialized to 7 bit, even parity, 2400 bps data transfer.

The remote hardware debugging feature enables the technicians to connect either a serial printer or a tty compatible terminal. It will also be possible to connect a 2400 bps modem to this port.

If a terminal is choosen, it will also be possible to send input to the selftest likewise the input from the keyboard.

When the parameter "HALT ON ERROR" is set to "N", only pass numbers and error messages will be written on the remote hardware debugging device.

To enable the remote hardware debugging the bit 7 of 8255 PPI part B (72H) must be strapped to zero (Pin 25 on the 8255), see fig. 7. Pin 11 in the SIO channel B interface plug is connected to this bit.

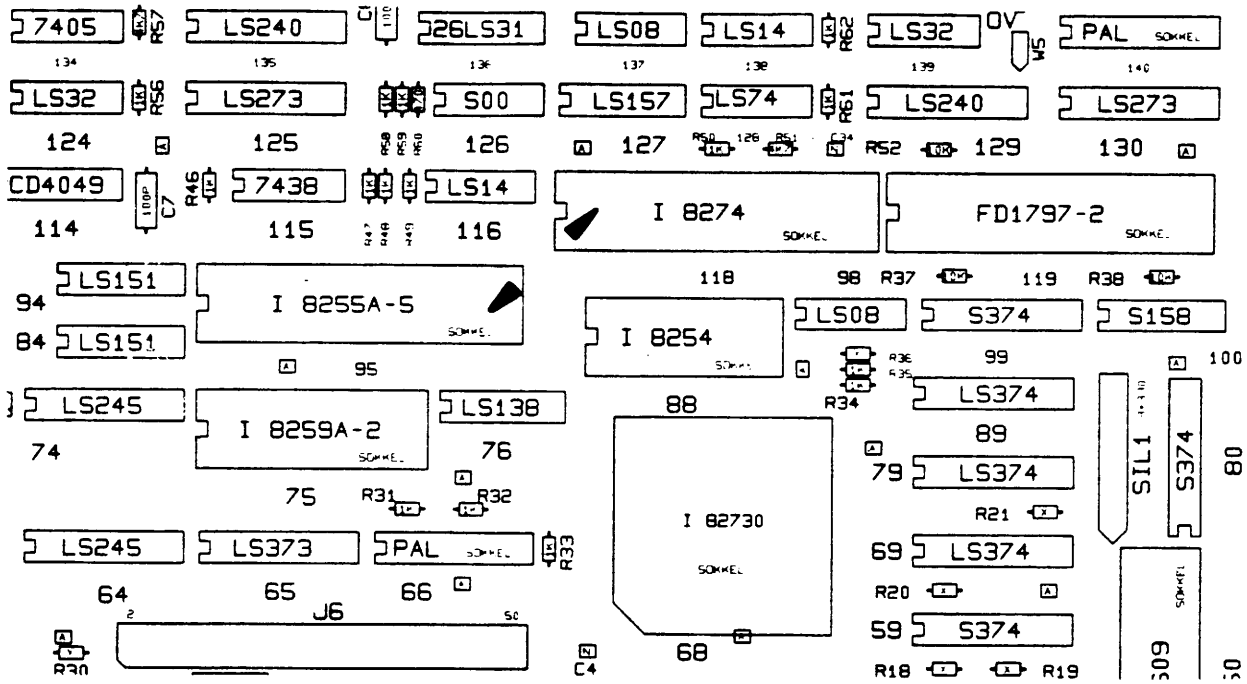


Figure 7: Locate the SIO and PPI.

2.6 Default Interrupt Handling

When the RC750, PC, Selftest has finished the memory test, a set of default interrupt vectors are placed in the memory. These vectors are primarily used to handle not wanted interrupts. There are two kinds of not wanted interrupts. One is handled by the interrupt procedure for internal iAPX186 instruction interrupts and the other is handled by the interrupt procedure for illegal device interrupts.

2.6.1 Instruction Exception

If an Instruction Exception interrupt occurs, it is likely to believe that this was caused by a malfunction of the iAPX186, because this interrupt is related to some of the CPU instructions.

If this error should occur, it will produce the following errortext:

">> instruction exception"

The related error number is 8.

2.6.2 Illegal Interrupt

Once after each test program the reception of interrupts are enabled. Only three types of interrupt are legal in the selftest, when not running a interrupt dependend test program. These are the keyboard interrupt, IR1, the 82730 Display controller interrupt, IR4 and the SIO (8274) channel B receive interrupt. All other interrupts requests received on the 8259 interrupt controller and on-chip iAPX186 interrupt controller will be decoded as illegal interrupts and will produce the following errortext:

"illegal interrupt"

followed by the information about which level was requesting the interrupt.

The related error number is 5.

Interrupt name	Vector type	Related instruction
Divide Error	0	DIV, IDIV
Single step	1	ALL
NMI	2	ALL
Breakpoint	3	INT
INTO Detected overflow	4	INTO
Array Bounds	5	BOUND
Unused Opcode	6	Undefined Opcodes
ESC Opcode	7	ESC opcodes

Interrupt name	Vector type	Related interrupt level
Timer 0 Interrupt	8	8
Reserved	9	-
DMA 0 Interrupt	10	10
DMA 1 Interrupt	11	11
INT0 Interrupt	12*	12
INT1 Interrupt	13**	13
INT2 Interrupt	14*	14
INT3 Interrupt	15**	15
Timer 1 Interrupt	18	8
Timer 2 Interrupt	19	8

Interrupt name	Vector type	Interrupt source
8259 IR0	20	Flexible disk
8259 IR1	21	Keyboard
8259 IR2	22	SASI bus
8259 IR3	23	RTC
8259 IR4	24	82730
8259 IR5	25	Net interrupt
8259 IR6	26	Centronic Interface
8259 IR7	27	I/O interrupt
8274 chB_TXBE	40	transmitter buffer empty
8274 chB_ESC	41	External/status change
8274 chB_RXCA	42	Receive character available
8274 chB_SPI	43	receive error
8274 chA_TXBE	44	transmitter buffer empty
8274 chA_ESC	45	External/status change
8274 chA_RXCA	46	receive character available
8274 chA_SPI	47	receive error

Figure 8: Interrupt Type Table.

* $\overline{\text{INT0}}$ and INT2 are used as $\overline{\text{INT0}}$ and $\overline{\text{INTA0}}$ for the 8259

** INT1 and int3 are used as INT1 and $\overline{\text{INTA1}}$ for the 8274.

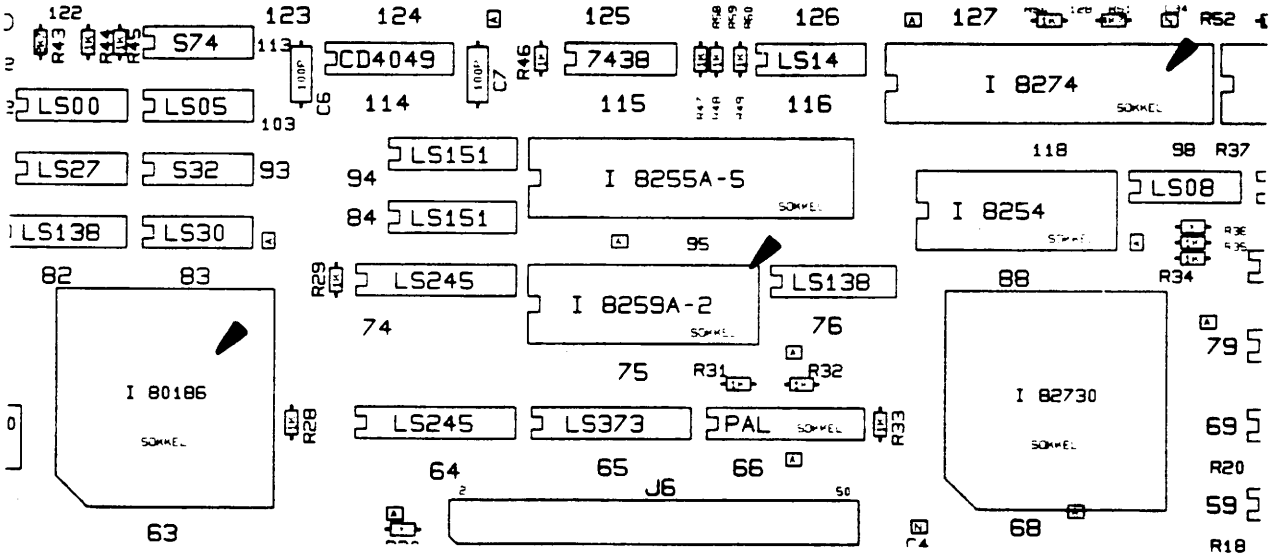


Figure 9: Locate Interrupt controllers.

3. I/O PROCEDURES AND TABLE INDEXING 3.

Included in the RC750, PC, Selftest is a rather simple handling of input and output. Furthermore it uses array tables to decide, which test is to be started next and which errortext is to be written.

3.1 Input 3.1

Input is handled in the most simple way possible. The selftest is working with a one character buffer which will receive characters from either the keyboard or alternatively from the remote hardware debugging device. See section 2.5. Characters will be received on interrupt. The character sequence <cntrl> <alt> <backspace> will force the test to hand over the control to the bootloader.

Note: That input may be delayed until a test is ended.

3.2 Output 3.2

Text output from the selftest is written in three different display buffers

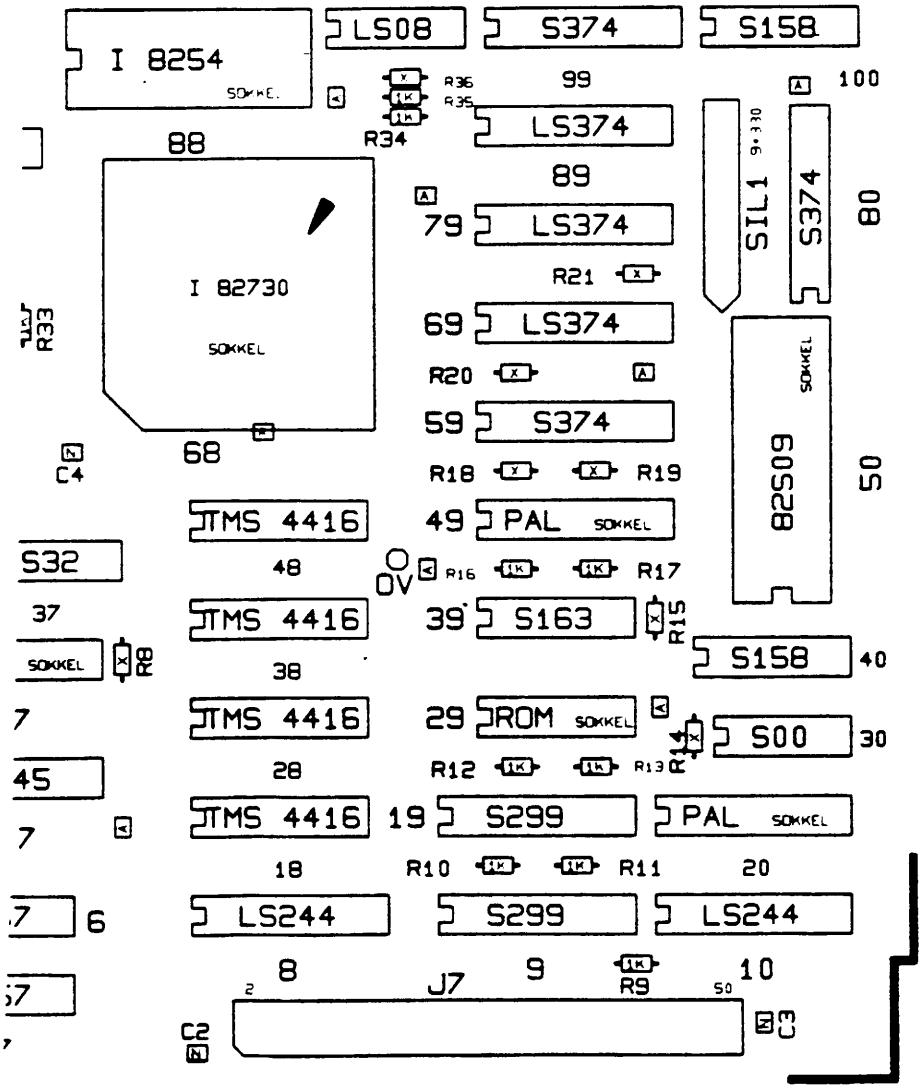
1: The user mode picture
   First memory address: 3000:3000
2: The technical mode picture
   First memory address: 3000:4000
3: The status line
   First memory address: 3000:5000

Character ascii values will be written in these buffers at the even bytes.

Both the user mode picture and the technical mode picture has 24 lines of 80 characters each.

Scrolling is performed as "hard scroll" by scrolling the content of the display buffer.

Output as written in the technical mode can be send to the remote hardware debugging device. See section 2.5.



Figur 10: Locate the display controller.

3.3 Test Selection 3.3

The test number field of the test parameter switch (see fig. 5) is used to select the next test to be run. This number is an index in an array, which for every test contains the offset to the introduction text and the test starting address.

The RC750, PC, Selftest will always write the test introduction text before the test is started.

3.4 Errornumber Decoding 3.4

At the end of every test program there is send an errornumber, and in some cases related informations, to the errorbuffer.

This errornumber is used by the testadministrator as an index in an array, which contains the offset and chainnumbers for every errortext in the selftest.

The chainnumber in connection with an errortext offset is used as index for writing address, received, expected and other values related to the error.

The errornumbers are listed in Appendix A.

4. RAM MEMORY CONFIGURATION 4.

The RC750, PC, Selftest contains a socalled Snooper facility (see chapter 6), by which it is possible to display and change the content of all CPU addressable memory cells, in the 1 M byte memory address space. Therefore this manual is equipped with a layout of the RAM memory configuration. This configuration is shown in fig. 11.

0000:0000	iAPX186 interrupt vectors
0000:0050	Configuration record (see section 1.2)
0000:0080	8259 interrupt vectors
0000:0100	8274 interrupt vectors
0000:0120	error buffer
0000:0120	err_no
0000:0121	adr_data
0000:0123	exp_data
0000:0125	rec_data
0000:0127	aux1_data
0000:0129	aux2_data
0000:012B	aux3_data
0000:012D	adm_switch
0000:012F	soft_count
0000:0130	pass_count
0000:0132	key_char_available
0000:0133	key_ascii
0000:0134	key_position_code
0000:0135	CRT frame_count
0000:0137	writing position
0000:0400	expected buffer
0000:2400	receive buffer
0000:4400	receive buffer
0000:6400	ascii convert buffer for snooper
0000:640A	interrupt level
0000:640C	8274 chA_xmt_pointer
0000:640E	8274 chA_rec_pointer
0000:6410	8274 chA_counter

0000:6412	floppy_0_ready
0000:6413	floppy_1_ready
0000:6414	4 Winchester status bytes
**** ****	*****
1000:0000	Selftest stack
1000:0320	stack top
****:****	*****
3000:2000	82730 Display controller command block
3000:2026	82730 Display mode block
3000:2054	Picture string pointers
3000:3000	User mode picture
3000:4000	Technical mode picture
3000:5000	Status line
****:****	*****
F000:0000	Display pixel character fond layout
F000:2000	Display command block and buffers, while running the memory test
F000:6000	Coprocessor intermidiate command block
FC00:0000	PROM with test programs and bootloader
FFFF:0000	Power up start address

Figure 11: Selftest RAM memory layout.

5. INITIALIZE 5.

After a power up/reset the RC750, PC, Selftest will perform some basic hardware initializations of the onboard controllers.

The initializations are common for the Selftest and the bootloader.

5.1 Wait States 5.1

The PROM and RAM memory will have 0 wait sates. Pheripherals will have 2 wait states. All I/O ports will be placed in the socalled I/O space.

5.2 iAPX186 Interrupt Controller 5.2

The interrupt vector for the iAPX186 controllers are tied to specific memory locations, equal to the location 20H for the first vector in the table. See section 2.6.

INT0/INT2:

Port: FF38H
Value: 003FH

These two pins of the iAPX186 are used for cascading with the extern interrupt controller 8259. See fig. 9.

INT1/INT3:

Port: FF3AH
Value: 003FH

These two pins of the iAPX186 are used for cascading with the extern interrupt source, the 8274 communication controller. See fig. 9.

Mask Register:

Port: FF28H
Value: CDH

Which will mask the following

```
I3  : 1 ; INT3
I2  : 1 ; INT2
I1  : 0 ; INT1, 8274 cascade
I0  : 0 ; INT0, 8259 cascade
D1  : 1 ; DMA 1
D0  : 1 ; DMA 0
TRM : 1 ; Timers
```

5.3 Programmable Interrupt Controller 8259 5.3

The hardware of the RC750 is configurated with keyboard interrupt connected to IR1 and 82730 Display controller interrupt connected to IR4.

8259 setup:

```
ICW 1 : 19H ; level triggered input
ICW 2 : 20H ; the interrupt vector table starts in 80H
ICW 3 : 00H ; no external slaves
ICW 4 : 1DH ; buffer mode/master, specific EOI and fully
              nested.
MASK  : EDH ; enable keyboard and CRT interrupts.
```

5.4 iAPX186 Timer 0 5.4

Timer 0 is initialized as a baudrate generator in alternating mode with even duty cycle. It is initialized to supply a baudrate clock for 2400 bps on the SIO 8274 channel B. See also section 2.5 about remote hardware debugging.

5.5 8254 Timer Initialize 5.5

Timer 0 and timer 1 are initialized as baudrate generators supplying a clock for a baudrate of 9600 bps on the SIO 8274 channel A. Timer 2 is initialized as a one shot supplying a delay of approximate 50 Msec for the flexible disk controller.

5.6 8274 Serial Communication Controller 5.6

Channel A

baudrate factor : X16
character length: 8 bit
parity : none
stop bits : 2
mode : asynchronous

Channel B

baudrate factor : X16
character length: 7 bit
parity : enabled/even
stop bits : 1
mode : asynchronous

5.7 82730 Display Controller 5.7

In the RC750, PC, Selftest, the 82730 Display controller will be initialized in a non interlaced mode with character fond formats of 7x9 bits.

A screen image will have 25 lines inclusive the status line. The selftest will show no cursor.

The selftest will be able to show two different pictures (character strings), one at a time, plus a status line. One picture is named the user mode picture and the other is named the technical mode picture.

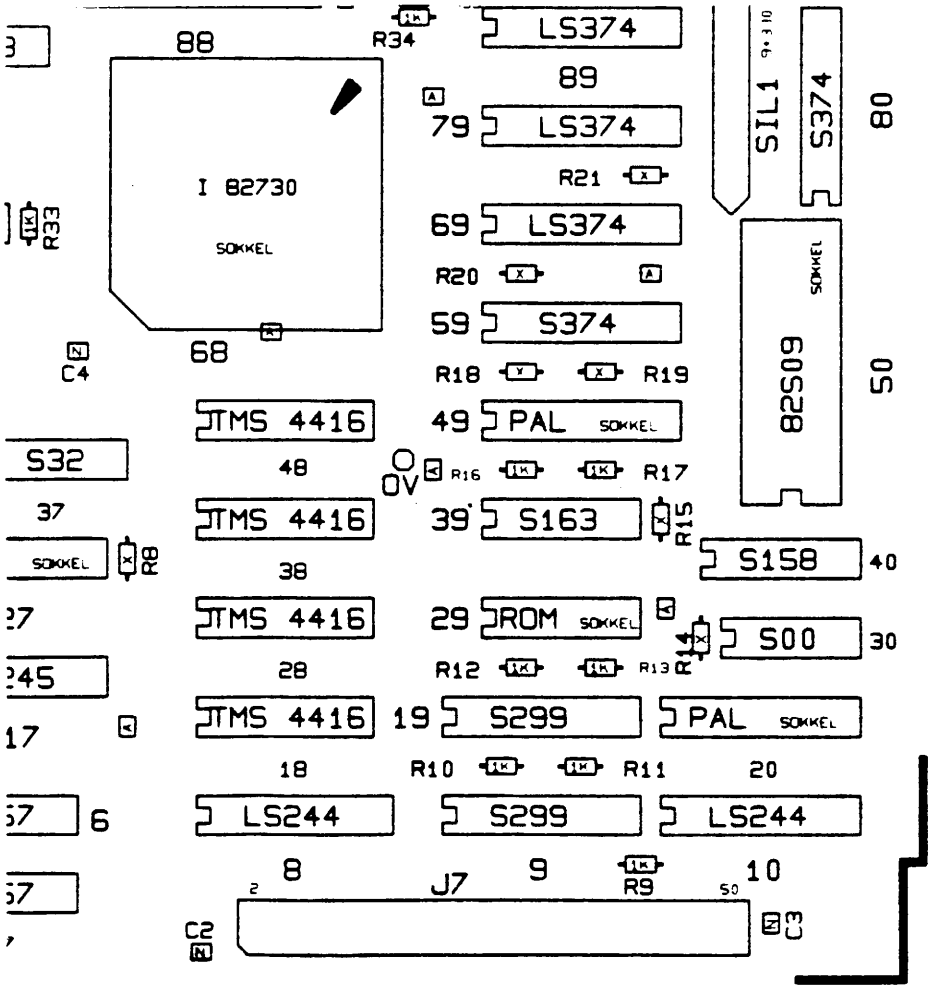


Figure 12: Locate the 82730 Display Controller.

6. SELFTEST SNOOPER 6.

The RC750, PC, Selftest is equipped with a socalled Snooper facility, which enables the user to manipulate with RAM data and input, output ports. It is enwoked by entering entry <2> in the main menu. See subsection 2.2.1.

The Snooper can be entered at the termination of any of the test programs.

When the Snooper is entered, it will respond with the following menu:

>> Snooper

<0>: output to port
<I>: input from port
<N>: substitute word
<M>: display memory
<,>: continue selected
<X>: exit from snooper

*** Note: That changing the content of RAM memory words or performing output to devices, may have some drastic effects to the Selftest.

When entering the character "X", the Snooper will return to the testadministrator, where a new entry in the main menu can be selected.

6.1 Press <M> 6.1

When the entry <M> has been selected, the following two questions concerning the address will be asked:

SEGM.: _ _ _ _ ADDR.: _ _ _ _

These questions must be answered with the address of the first memory word wanted to be displayed.

When the address has been typed, 100 - 16 bit words will be shown on the display. The format of the output is 20 lines each with the content of 5 words. It is shown in both hexadecimal and in ascii.

The following 100 words will be displayed, if the character "," is typed.

A new first address may be selected by reentering the character "M".

6.2 Press <N> 6.2

When the entry <N> has been selected, the following two questions concerning the address will be asked:

SEGM.: _ _ _ _ ADDR.: _ _ _ _

These questions must be answered with the address of the first memory word wanted to be changed.

When the address has been typed, the first word is displayed. Now there are two possibilities, either to fill in a new hexadecimal value or to type ",".

A new value may consist of from one up to four digits. If less than four digits is input, the number will be entered by typing <return>.

When a new value for a word has been entered, the value of the next word is shown.

If the character "," is entered, the memory word displayed is left unchanged, and the next word is displayed.

6.3 Press <I> 6.3

When the entry <I> has been selected, the Snooper will respond with the question:

PORT.: _ _ _ _

When a port number has been entered, the 16 bit word contained in this port is shown. If the port is an 8 bit type, it is the 8 LSB, that is significant.

6.4 Press <O> 6.4

When the entry <O> has been selected, the Snooper will respond with the questions:

PORT.: _ _ _ _ DATA: _ _ _ _

When a port number has been entered, the 16 bit word to be send, must be entered. If the port is an 8 bit type, it is the 8 LSB, that is significant.

7. BLOCK DIAGRAM 7.

Fig. 13 shows a block diagram of the RC750 Personal Computer.

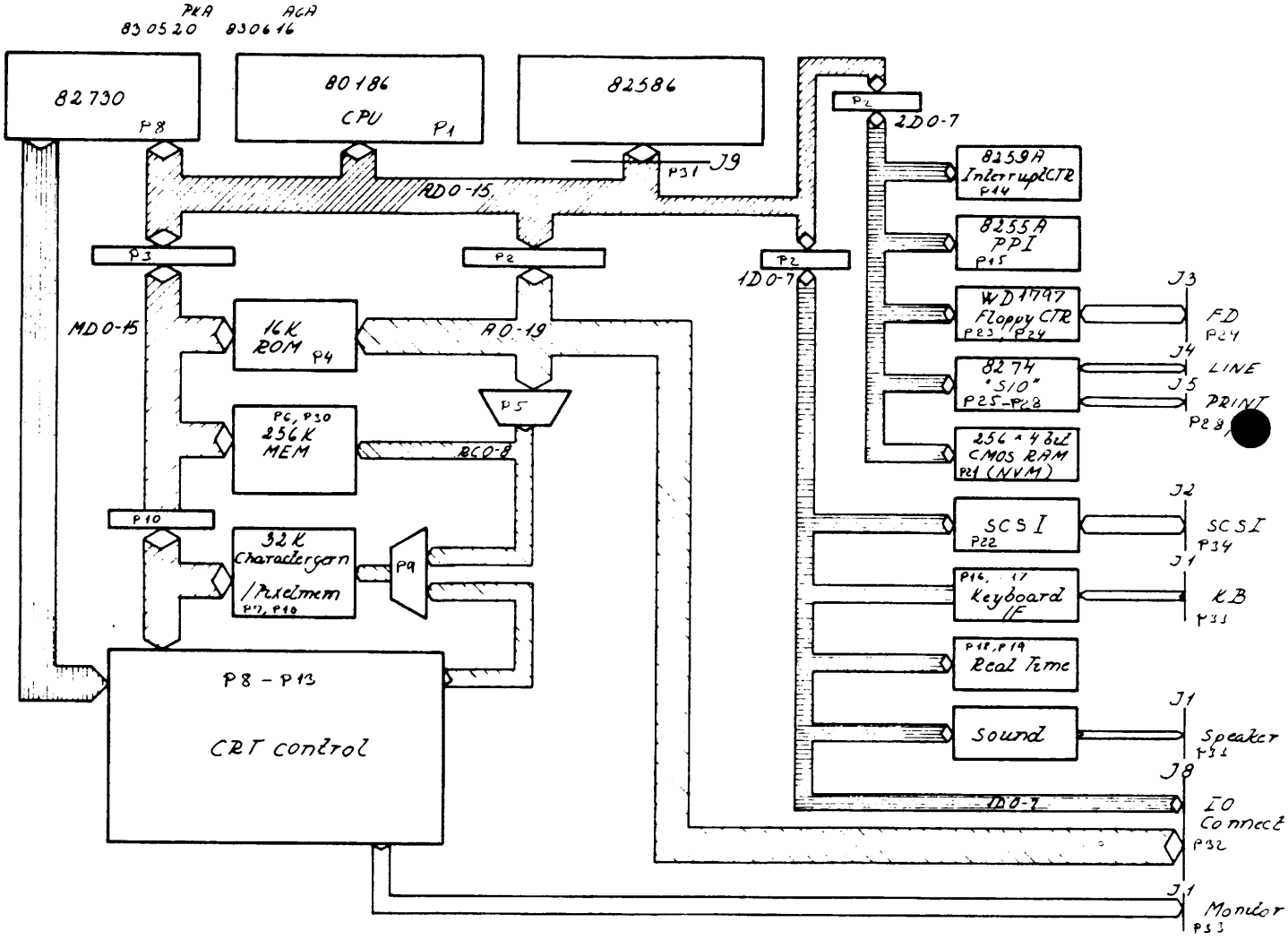


Figure 13: RC750 Block Diagram.

Refer to the hardware manual to get more detailed information about the hardware.

8. GENERAL SELFTEST ERRORS 8.

The RC750, PC, Selftest has four different types of errors, which might occur at any time during the selftest.

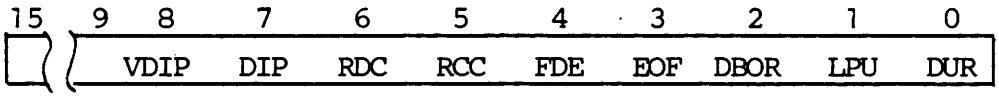
The type "Instruction Exception" is explained in subsection 2.6.1.

The related error number is 8.

The type "Illegal Interrupt" is explained in subsection 2.6.2

The related error number is 5.

The type "CRT status error" is caused by the 82730 display controller, when an incorrect status at interrupt is discovered. The status word layout is as shown.



82730 Status Word

VDIP: Virtual Display In Progress
DIP : Display In Progress
RCC : Reserved Channel Command
RDC : Reserved Datastream Command
FDE : Frame Data Error
EOF : End of nth Frame
DBOR: End of Row
LPU : Light Pen Update
DUR : Data Underrun

The "CRT status error" will be shown, if any of the bits RDC, RCC, DBOR, DUR is set during interrupt status read.

The related error number is 16.

The type "Incorrect SCSI state" can be set during hardware configuration of connected controllers to the SCSI bus, if this bus stays busy for an infinite period of time. See also chapter 22 conserning the Winchester test.

The related error number is 35.

9. MEMORY TEST 9.

The memory test of the RC750, PC, Selftest consists of three parts, a PROM checksum test, a CRT-pixel memory test and a main memory test. The PROM checksum test is only run once at power up, whereas the CRT-pixel and main memory test may be run several times, if requested.

9.1 PROM Checksum Test 9.1

The content of the two PROM's located in position 4 and 5, see fig. 14, are summarized independtly of each other. The summation for each PROM must result in a zero. For that reason each of the PROM's contains a compensation byte in the first byte of the PROM.

The PROM in position 4 contains all the even bytes, and the PROM in position 5 contains all the odd bytes.

If the summation is different from zero, the following will be output to SIO 8274 channel B, see section 2.5.

<00><EE> PROM checksum error

Where <00> is the 8 bit sum of the PROM containing the odd bytes, and <EE> is the 8 bit sum of the PROM containing the even bytes.

An atempt will also be made to start the display (82730) and write a normal errormessage there, see section 3.2, but this attempt might fail, because the RAM memory test will be bypassed, if there is an error in the boot and test PROM's.

This type of error means that the content of the program PROM's has not been maintained, and that the PROM's must be changed.

The error number of this kind of error is 1.

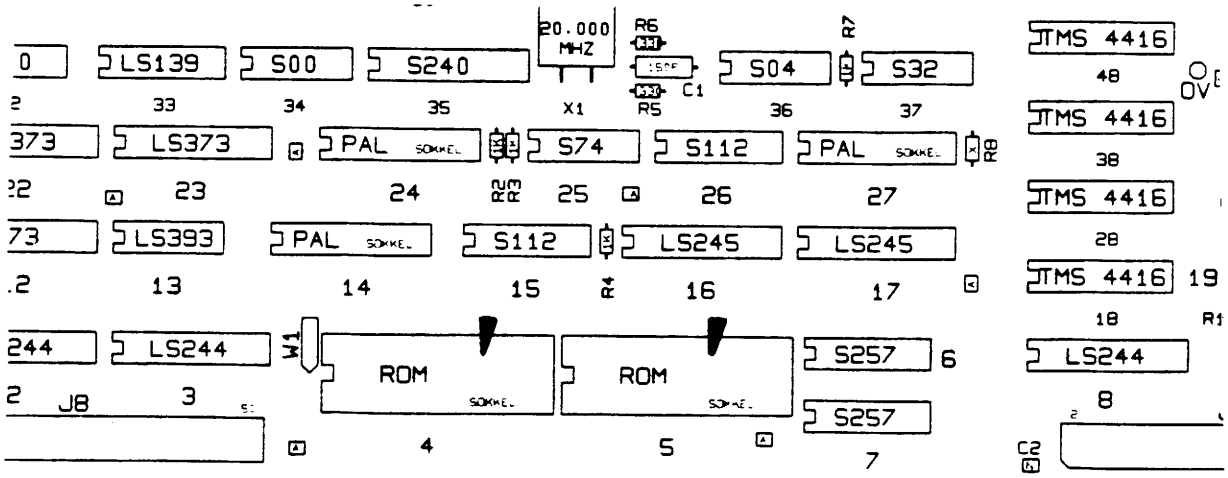


Figure 14: Locate the program PROM's.

9.2 CRT-pixel Memory Test

9.2

The CRT-pixel memory test of the RC750, PC, Selftest is testing the onboard pixel memory. See fig. 15.

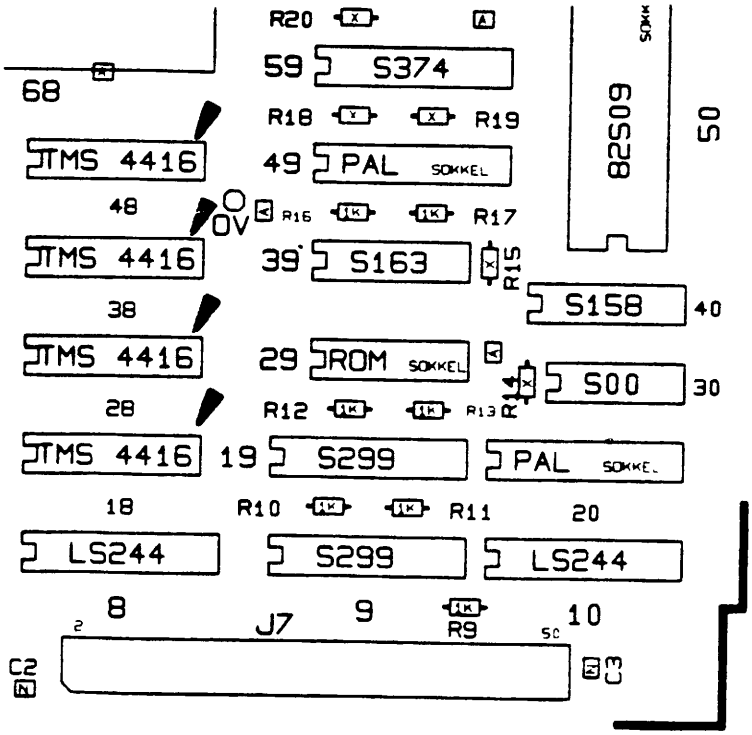


Figure 15: Locate the CRT-pixel memory.

The pixel memory is located from the physical address F000:0000, and has the size of 32 k bytes.

The display is turned of during this test. The test pattern is a modulus 3 pattern as explained in subsection 9.3.1.

This part of the memory test is a register based test not using memory variables at all, because of the fact that the main memory has not been tested yet.

This fact leaves only two registers for variables that can survive the memory test, a pass counter and the parameter word. It gives some of the explanation for the simple structure of the Selftest testadministrator.

Position 48: holds bit 0-3
Position 38: holds bit 4-7
Position 28: holds bit 8-11
Position 18: holds bit 12-15

At the end of a successful pixel memory test, the 82730 Display controller will be started and the following text will be written at the first line of the screen:

*** Rc750, TEST, V. 1.0 ***

Note, that during the main memory test this text will have a broad space between the letters (character fonds of 15x16 bit). At the end of the main memory test, the fonds will be narrowed to 9x16 bits.

As the function of the RC750, PC, Selftest is very much dependend of the function of the pixel memory and the 82730 Display controller, it is possible, if these elements should fail to function to get error information via the remote hardware debugging channel see chapter 2-5.

9.3 Main Memory Test

The main memory test, which will follow the CRT-pixel memory test sequencially, if no error was detected in the pixel memory, is able to test memory modules of different sizes.

The main memory can have one of four sizes 256 K bytes, 512 K bytes, 768 K bytes or 1 M byte.

The size of the memory is configurated in port 220 H bit 6 and 7 (position 10).

bit 7	bit 6	size
0	0	256 K
0	1	512 K
1	0	768 K
1	1	1 M

The memory test is using a modulus 3 pattern as explained in 9.3.1. Both the pixel and the main memory test starts in the highest address, and tests towards lower addresses.

See fig. 16 to locate a specific memory chip by a given error message.

9.3.1 Memory Test Pattern

The main memory of the RC750 consists of memory chips of 1 bit x 64 K. The memory test executes 4 passes through the memory, two times writing and two times reading.

The test pattern is the convinient modulus 3 pattern consisting of three times 55AA followed by three times AA55. The modulus of 3 will break the physical modulus 2 structure of the chips and the memory.

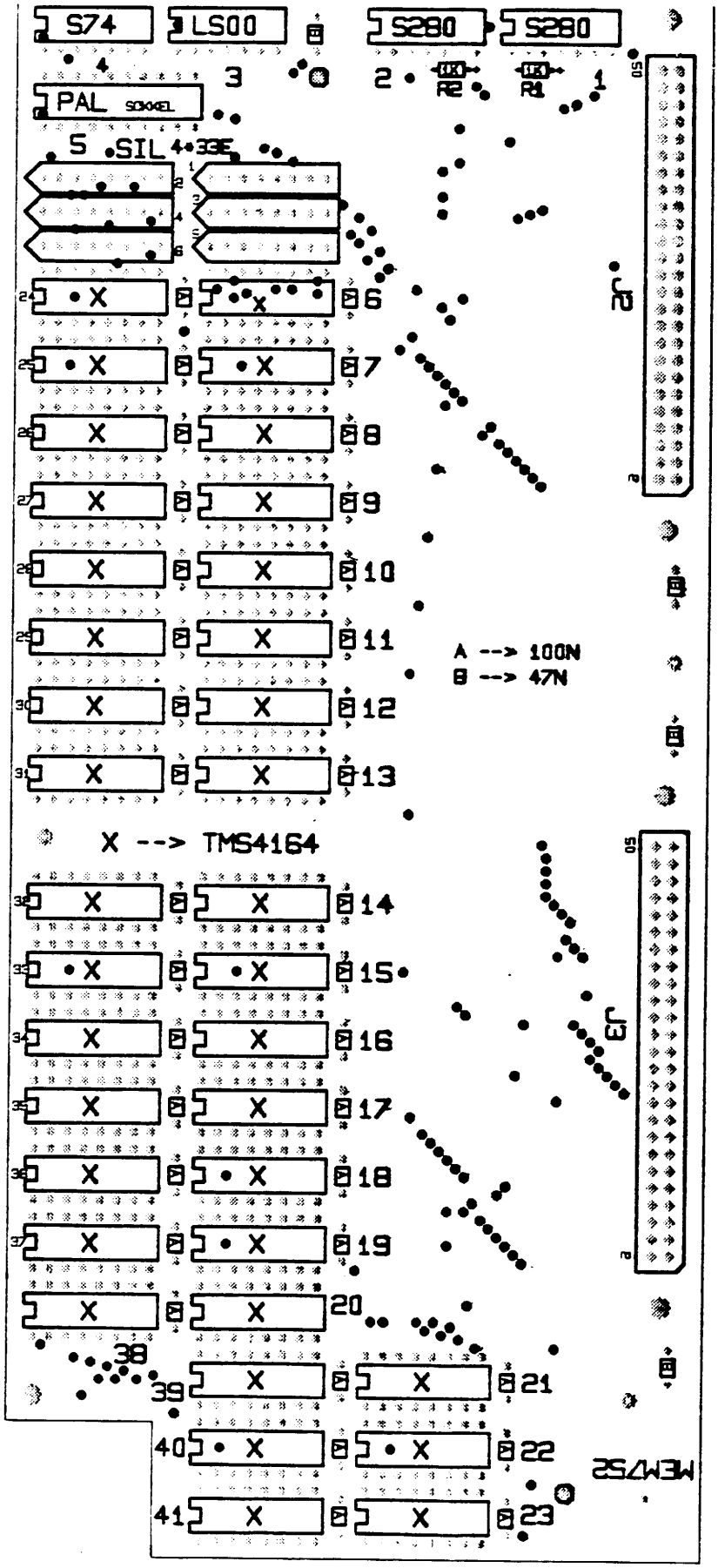


Figure 16: RAM memory module.

The test starts in the highest address, derived from the memory configuration bit 6 and 7 in port 220H, and inserts the pattern towards lower addresses.

When all memory words have been written and tested, they are tested again with the inversed pattern, this means that all bits are tested for "zero" and "one" insertion.

If an error occurs, a message will be written as follows:

Memory test: RAM memory error, segm.: <ssss>, addr.: <aaaa>, exp.: <eeee>, rec.: <rrrr>

Where

<ssss> is the segment address
<aaaa> is the offset address
<eeee> is the expected pattern
<rrrr> is the received pattern

The error number of this kind of error is 2.

The above mentioned informations can be used to find a defective RAM memory chip with the help of fig. 15 or fig. 16.
Say the error message was:

Memory test: RAM memory error, segm.: 1000, addr.: 0002, exp.: 55AA, rec.: 55AB.

This could indicate that the error was located in position 23 of the main memory module. Of course it could as well be an error in the surrounding logic. (Please consult the hardware manual).

After termination of the memory test the Selftest will enter the testadministrator, which controls the flow of the rest of the test program.

10. RAM REFRESH TEST 10.

The RAM refresh test of the RC750, PC, Selftest applies to verification of the function of the memory control logic and the refresh count generated with the 82730 Display controller as source. The main purpose of this test is to discover modification of data during a delay, due to malfunction of the memory control logic and/or the display controller.

The test pattern written is a counting pattern in the memory area called "expected buffer", see the RAM memory configuration in chapter 4. The size of the test buffer is 4K, 16 bit words.

When the pattern has been written the test program enters a waiting loop for approximate 1.0 seconds, in which the CPU will not access the RAM memory. After the delay, the buffer will be checked to discover any modification. The check-reading is performed 100 times to check that read memory does not modify the content of the words.

If any modification of data is discovered, a message as follows will be written:

RAM refresh test: not refreshed, addr.: <aaaa>, exp.: <eeee>,
rec.: <rrrr>

where

<aaaa> is the offset address relative to the start of the test buffer.
<eeee> is the pattern written in this word.
<rrrr> is the pattern read from this word.

The error number for this kind of error is 9.

11. 8255 PPI TEST 11.

The 8255 PPI test of the RC750, PC, Selftest applies to the verification of the function of the onboard programmable peripheral interface.

The 8255 PPI is only used for internal controlling purposes on the micro controller board.

The purpose of the test is to examine one of the ports on the controller. The testprogram tests the 8255 PPI port A, first by shifting ones though the bits and then zeroes. This shifting is performed from LSB towards MSB.

The original content of the port is restored at the end of the test.

If a bit in the port should fail to function, a message as follows will be written:

PPI 8255: port, bit error, exp.: <eeee>, rec.: <rrrr>

Where

<eeee>: is the pattern written in the port.

<rrrr>: is the pattern read from the port.

The errornumber of the 8255 PPI port error is 18.

See fig. 2 to locate the 8255 PPI.

12. CENTRONIC INTERFACE TEST 12.

The Centronic Interface Test of the RC750, PC, Selftest applies to the verification of the function of the internal loop back of the printer interface.

The test program is using the internal loop back facility to test the Centronic compatible parallel printer interface. It has no need of external equipment, because the internal loop back is used to check the data patterns send. The pattern send to the data port is rolling zeroes and ones.

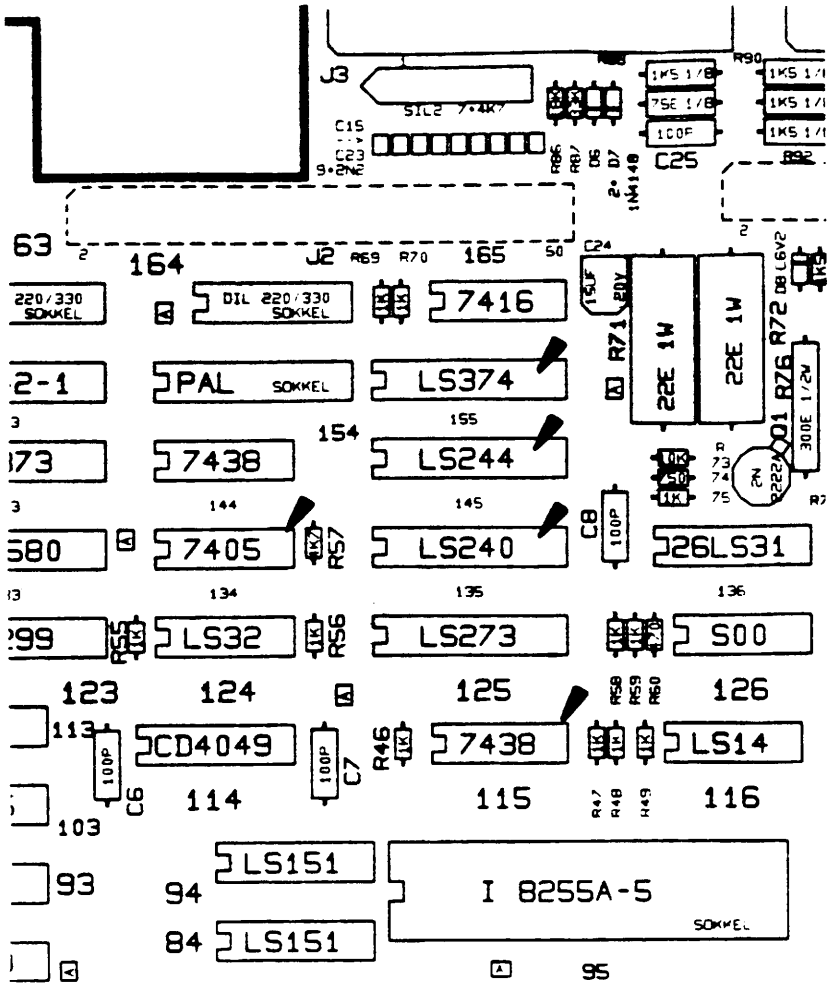


Figure 17: Locate the Centronic Interface.

The procedure of the test is first to check the function of the control signals and afterwards the data signals. The control signals are not tested in the default power up sequence.

The pattern send to the control signals are as follows:

INIT	STROBE	Port 260H
0	0	
1	0	
1	1	
0	0	

If an error should occur on these lines, a message as follows will be written:

Centronic Interface: control signals, exp.: <eeee>, rec.: <rrrr>

Where

<eeee> is the pattern written into the control port.

<rrrr> is the pattern read from the loop back of the port.

The data port test will shift first ones and then zero'es through the bits of the port (250 H).

If a bit should fail to function (internal loop back), a message as follows will be written:

Centronic Interface: data signals, exp.: <eeee>, rec.: <rrrr>

Where

<eeee> is the pattern written into the control port.

<rrrr> is the pattern read back from the loop back of the port

The errornumber of control signal error is 24.

The errornumber of data signal error is 25.

13. NON VOLATILE MEMORY TEST 13.

The Non Volatile Memory test of the RC750, PC, Selftest applies to the verification of the function of the MCM 14510101-1 non volatile memory.

The NVM is designated to contain system configuration parameters, which must survive power down.

The purpose of the test is to verify that the content has not changed since the RC750 was last configurated. This is done by calculating the checksum of all the nibbles in the NVM seen as bytes. The calculated checksum should be equal to AAH.

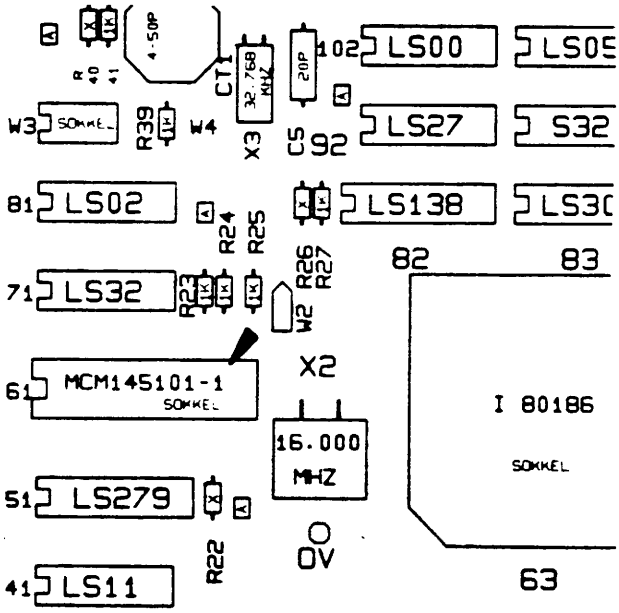


Figure 18: Locate the NVM.

If the test should calculate a checksum different from AAH, a message as follows will be written:

Non volatile memory: Incorrect checksum, rec.: <rrrr>

Where

<rrrr> is the sum of all the nibbles in the NVM seen as bytes.

The errornumber for this type of error is 19.

14. iAPX186 TIMER TEST 14.

The iAPX186 Timer Test of the RC750, PC, Selftest applies to the verification of the function of the on-chip iAPX186 timer.

The iAPX186 Timer consists of three integrated timers, Timer 0 is used as a baudrate generator, see chapter 5. Timer 1 is used as alternative sound generator, which is used by the Selftest to read out audio-error numbers.

The iAPX186 Timer Test will test the timers maximum count bit. It will first test timer 2, and then timer 1 prescaled by timer 2.

The procedure of the test is first to test that the timer's "MC" bit is not set before counting. Then to start the timer and wait for the "MC" bit to be set. The "MC" bit of the timer should be set before a programmed delay loop timeout.

The timer 2 count value equals 1000, and the initialization value of the mode/control register equals C000H. The timer 1 count value equals 5 prescaled by timer 2, and the initialization value of the mode/control register C008H.

15	14	13	12	11		5	4	3	2	1	0
EN	INH	INT	RIU	0	-	MC	RTG	P	EXT	ALT	CONT

Figure 19: Timer Mode/Control Register.

	Register address		
Register name	Tmr 0	Tmr 1	Tmr 2
Mode/control Word	FF56H	FF5EH	FF66H
Max Count B	FF54H	FF5CH	not present
Max Count A	FF52H	FF5AH	FF62H
Count Register	FF50H	FF58H	FF60H

Figure 20: Timer Control Block Format.

If the Maximum Count bit of one of the timers should fail to function, a message as follows will be written:

IAPX186 Timer test: counting error, reg.: <aaaa>, exp.: <eeee>,
rec.: <rrrr>

Where

<aaaa> is the related Timer Count Register.
<eeee> is the Timer count start value.
<rrrr> is the content of the Timer Count Register.

This error is due to an internal error of the iAPX186 chip.

The errornumber of the Timer counting error is 10.

15. iAPX186 DMA TEST 15.

The iAPX186 DMA Test of the RC750, PC, Selftest applies to the verification of the function of the two on-chip iAPX186 direct memory access controllers.

Both DMA channels are initialized to memory transports. Channel 0 will transfer to the lowest address of its receive buffer first, and channel 1 will transfer to the highest address of its receive buffer first.

Both channels are started and will transfer bytes simultaneously. The procedure of the test is to check that the transfer count reaches zero before a programmed delay loop timeout. The timeout is approximate 200 mS.

If both channels have transferred the test buffer of 8k bytes each without timeout, a datacheck of both receive buffers are performed. The data compare routine is based upon a string compare instruction.

If a difference between the transmit and receive buffers is discovered, the 16 bit word in question is fetched from memory and shown in an errormessage. In other words, the errorneous word is fetched in both the string compare instruction and for the errormessage. This could mean, that if the discovered error was due to a sporadic memory error, the shown expected and received values could turn out to be equal.

The control word of channel 0 is initialized to B606H and the control word of channel 1 is initialized to DA06H.

16. iAPX186 INTERRUPT TEST 16.

The iAPX186 Interrupt Test of the RC750, PC, Selftest applies to the verification of the function of a Timer generated interrupt from the on-chip iAPX186 Timer 2.

The procedure of the test is to start the internal timer 2 with a count value equal 1. It is tested that an interrupt is generated within a programmed delay loop timeout, and that the interrupt arrived on the expected level. The timeout value is approximate 40 mSec.

If no interrupt has arrived within the timeout, a message as follows will be written:

iAPX186 interrupt test: timeout.

If an interrupt has arrived, but on a not expected level, a message as follows will be written.

iAPX186 interrupt test: illegal level serviced, lev.: <aaaa>

Where

<aaaa> is the actual level that interrupted.

Both errors are due to an internal error of the iAPX186 chip.

The errornumber of "timeout" is 12.

The errornumber of "illegal level" is 13.

Register name	Register address ch. 0	ch. 1
Control word	FFCAH	FFDAH
Transfer Count	FFC8H	FFD8H
Destination Pointer (upper 4 bits)	FFC6H	FFD6H
Destination Pointer	FFC4H	FFD4H
Source Pointer (upper 4 bits)	FFC2H	FFD2H
Source Pointer	FFC0H	FFC0H

Figure 21: DMA Control Block Format.

If the Transfer Count of one of the channels does not reach zero before timeout, a message as follows will be written:

iAPX186 DMA test: transfer count error, reg.: <aaaa>,
exp.: <eeee>, rec.: <rrrr>.

Where

<aaaa> is the related Transfer Count Register.

<eeee> is the expected value, always zero.

<rrrr> is the content of the Transfer Count Register.

If a data error is discovered, a message as follows will be written:

iAPX186 DMA test: data error, addr.: <aaaa>, exp.: <eeee>,
rec.: <rrrr>.

Where

<aaaa> is the offset address in the receive buffer.

<eeee> is the 16 bit word in the transmit buffer.

<rrrr> is the 16 bit word in the received buffer.

Both errors could be due to an internal error of the iAPX186 chip.

The errornumber of the Transfer Count error is 4.

The errornumber of the data compare error is 3.

17. 8259 INTERRUPT CONTROLLER TEST 17.

The PIC (8259) Interrupt Test of the RC750, PC, Selftest applies to the verification of the function of a 82730 Display controller generated "end of frame" interrupt. This interrupt appears every 16 mSec.

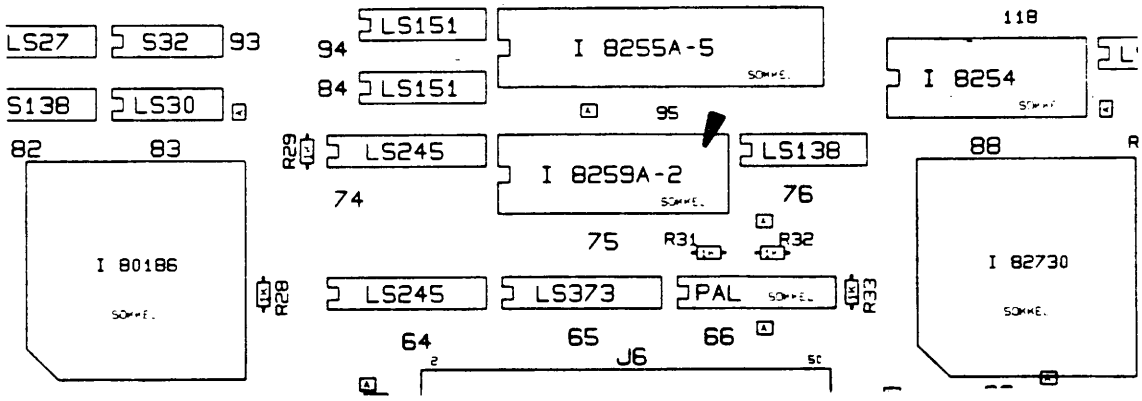


Figure 22: Locate the 8259 interrupt controller.

The procedure of the test is to wait for the appearance of an interrupt from the 82730 display controller. This controller will request an interrupt on the PIC level IR4. It is tested that an interrupt is generated within a programmed delay loop timeout, and that the interrupt arrived on the expected level.

If no interrupt has arrived within the timeout, a message as follows will be written:

8259 interrupt test: interrupt timeout.

If an interrupt has arrived, but on a not expected level, a message as follows will be written:

8259 interrupt test: illegal level serviced, lev.: <aaaa>

Where

<aaaa> is the actual level that interrupted

The errornumber of "timeout" is 6

The errornumber of "illegal interrupt" is 11.

18 KEYBOARD SELFTEST 18.

The Keyboard test of the RC750, PC, Selftest is only a routine to collect the result from the keyboard power up selftest.

The Keyboard test will receive the test result from the keyboard power up selftest, and check that the result from the test indicated, no errors found.

Of course, it will have no meaning to loop in this test, because the power up test result is only send once at power up.

If the keyboard is not connected, or if the RC750, PC, Selftest memory test has been run more than once, the following text will be written:

Keyboard: no result received.

If an error has been detected by the keyboard selftest and send to the RC750, PC, Selftest, a message as follows will be written:

Keyboard: Test result, rec.: <rrrr>

Where

<rrrr>: is the converted keyboard selftest errorcode.

The first character send by the keyboard after power up is the keyboard selftest errorcode. The errornumbers send from the keyboard is numbered 255, 254, 253 or 252. These numbers will be converted by the RC750, PC, Selftest to the numbers 0, 1, 2 or 3.

RC750 no.	Keyboard no.	Klick	Comment
0	255	3	No error
1	254	4	PROM checksum error
2	253	1	Port 1 error
3	252	2	Port 2 error

Figure 23: Keyboard error codes.

Note: 3 "klicks" from the keyboard indicates, that it is powered up and has not detected any internal errors.

The keyboard will repeat it's selftest, if the <T> key is pressed at power up. It is repeated until the key is released.

For further information about the keyboard selftest, refer to the Technical Manual.

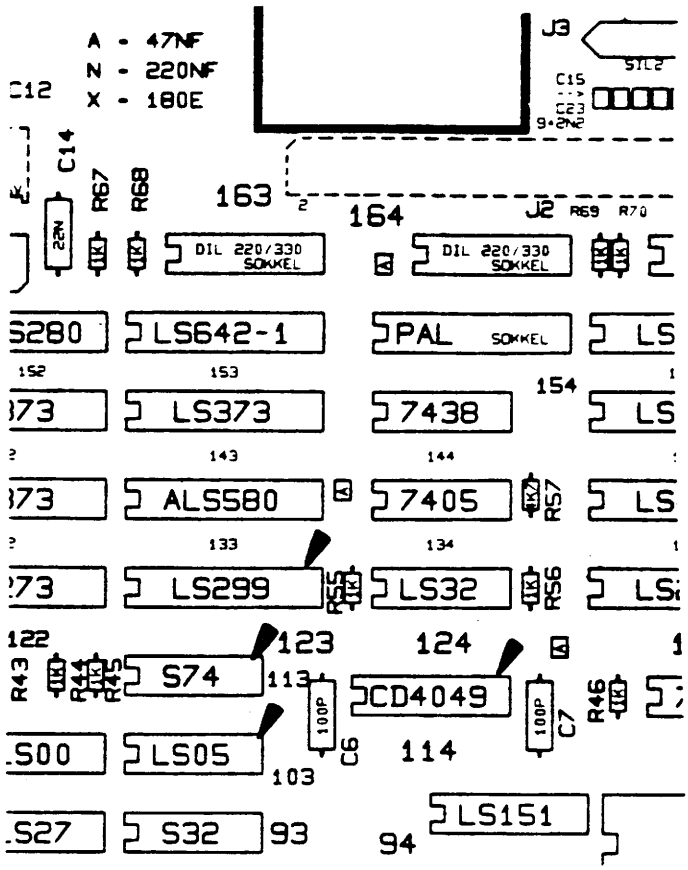


Figure 24: Locate the Keyboard Interface.

19. 8274 SIO TEST

The 8274 SIO Test of the RC750, PC, Selftest applies to the verification of the function of the 8274 channel A and the related interface for V.24 as well as X.21 connections.

This test is not included in the default power up sequence, but must be requested explicit either by setting the parameter "loop in test" to "Y", or the parameter "boot after test" to "N". See subsection 2.2.3.

The requirements for this test is the loop back cable called KBL580 see fig. 25. Should this cable not be installed at the start of the test, the following message will be written "Use testcable KBL580", and the test will be bypassed.

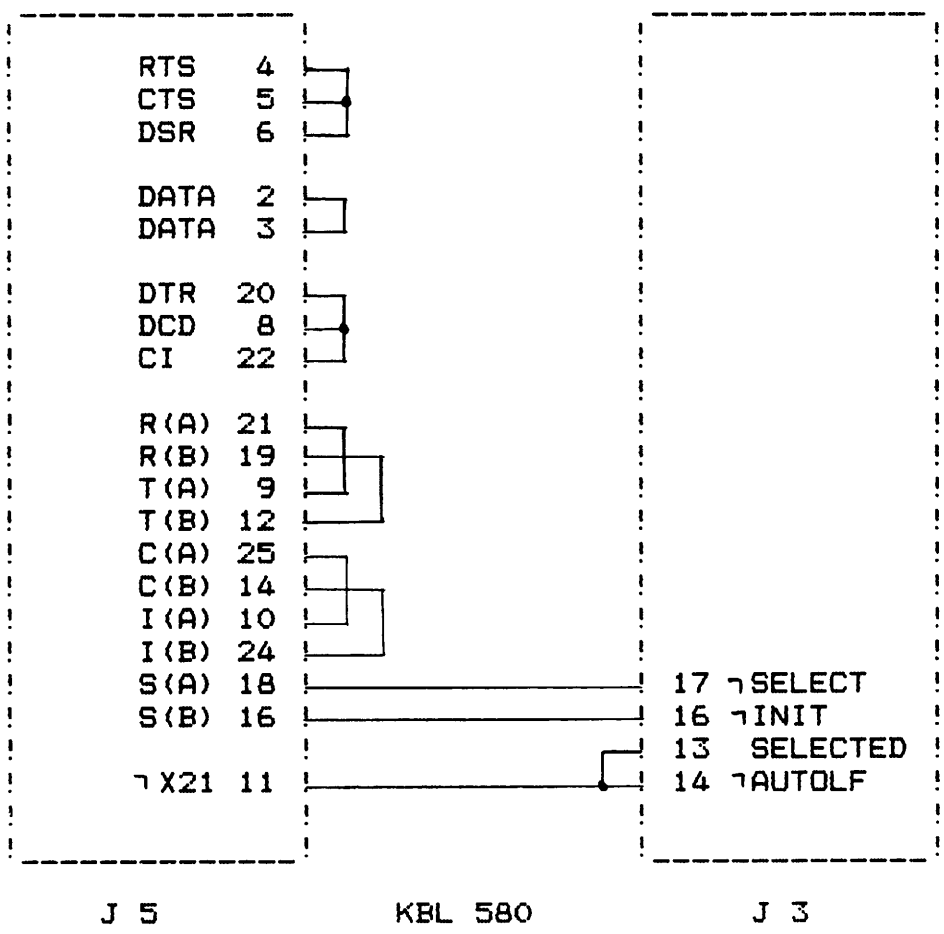


Figure 25: 8274-SIO-Test cable.

The 8274 SIO of the RC750 has two channels. Channel A is equipped with both V.24 and X.21 interface. Channel B is only equipped with V.24 interface.

Channel B is not tested in this test, because it is reserved, for remote hardware debugging, by the RC750, PC, Selftest, see section 2.5.

The initialization of both channels can be seen in chapter 5.

The testing of the 8274 SIO channel A is split into three parts. An X.21 interface test, a V.24 interface test, and a data loop back test.

19.1 X.21 Test

As it can be seen in fig. 25, the X.21 interface is turned active by the "AUTOLF" signal from the parallel printer port. The clocking of the X.21 interface is performed by the two signals "SELECT" and "INIT" at the parallel printer port. This clock is produced by a program-routine, which simmulates a balanced signal (when "SELECT" is true, then "INIT" will be false).

Step	Action	Result
1	8*clk, DTR, RTS	CTS, -,DCD, -,DATA
2	8*clk, -,DTR, RTS	-,CTS, -,DCD, DATA
3	16*clk, -,DTR, -,RTS	DCD

Figure 26: SIO Status Signals as result of X.21 test.

The X.21 test has a flow as can be seen in fig. 26. The notation in fig. 26 refer to the names of the status register bits in the 8274 SIO, rather than to the notation in the X.21 standard.

The relationship between the 8274 status register names CTS, DCD and receive data, and X.21 standard names S(A)/S(B), I(A)/I(B), C(A)/C(B), T(A)/T(B) and R(A)/R(B) can be found in the hardware manual.

7	6	5	4	3	2	1	0
		CTS		DCD			RX DATA

8274 SIO status register.

If an error should occur during the X.21 status signal test an errormessage as follows will be written:

SIO 8274: X.21 status error, reg.: <aaaa>, exp.: <eeee>,
rec.: <rrrr>

Where

<aaaa> is the address of the 8274 channel A status register (34H)

<eeee> is the expected value in the status register

<rrrr> is the actual value read from the status register

The errornumber of this type of error is 21.

19.2 V.24 Test

When the X.21 test is ended without any error discovered, the SIO test will proceed with V.24 test. This test will check the result on the status pins CTS, DSR, DCD and CI in respect to changes made on the RTS and DTR pins.

The relationship between the signals send and the status signals received is shown in fig. 27.

DTR	RTS	CTS	DCD	CI	DSR
0	0	0	0	0	0
0	1	1	0	0	1
1	1	1	1	1	1

Figure 27: V.24 status signals.

The two status signals not supplied by the 8274 SIO, CI and DSR are connected to port 210H bit 4 and 5.

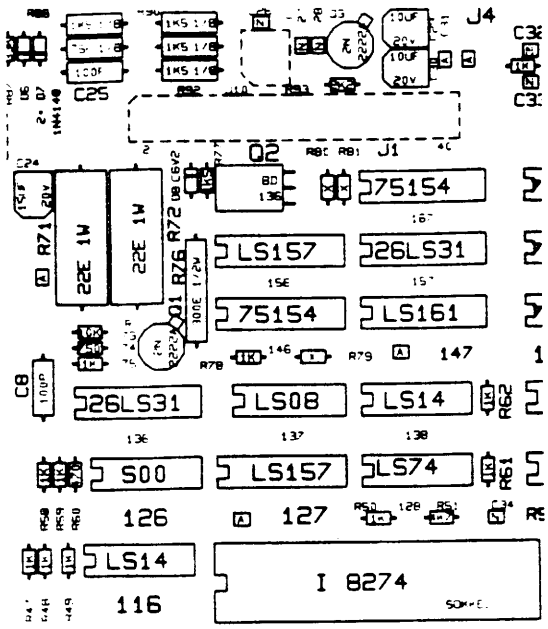


Figure 28: Locate the Serial Interface.

If an error should occur during the V.24 test a message as follows will be written:

SIO 8274: V.24 status error, reg.: <aaaa>, exp.: <eeee>,
rec.: <rrrr>

Where

<aaaa> is the port number of the 8274 SIO status register (34H) or the status port for the signals CI and DSR (210H) depending upon, where the error was discovered.

<eeee> is the expected value that should have been read from the port

<rrrr> is the actual value read from the port.

The errornumber related to this type of error is 22.

19.3 8274 SIO Data Test 19.3

When no errors has been discovered in either the X.21 or the V.24 status signal interface, the data loop back test is enterred.

The procedure of this test is to send a buffer of 8 k bytes of counting pattern. The pattern is counting on a word basis, so that the data send will look as follows: 0000 0001 0002 and so on.

Every time a byte has been send by the transmitter the test waits for an interrupt on the receiver. When one byte has been received a new byte is send. This is repeated until the whole buffer has been transferred. The transfer rate is 9600 bps.

As long as data is received, an asterix will be written every 1 sec.

During this test, it is checked that no data overrun, no parity error and no timeout has occurred.

If no data has been received within the last 1 sec., the following message will be written:

SIO 8274: timeout, lev.: <aaaa>

Where

<aaaa> is the expected receive interrupt level of channel A. (46H)

The errornumber of this type of error is 23.

If the parity error status is set during data transfer (not likely to happen, because the channel is initialized to 8 bit transfer), an errormessage as follows will be written:

SIO 8274: 8274 parity error, lev.: <aaaa>

Where

<aaaa> is the receive interrupt level of channel A (46H).

The errornumber of this type of error is 14.

If the receiver should set the overrun status, a message as follows will be written:

SIO 8274: 8274 overrun error, lev.: <aaaa>

Where

<aaaa> is the receive interrupt level of channel A (46H).

The errornumber of this type of error is 15.

When the 8k byte buffer has been transferred, the received data is checked against the data send. Should there be any difference, a message as follows will be written:

SIO 8274: Error in received data, addr.: <aaaa>, exp.: <eeee>,
rec.: <rrrr>.

Where

<aaaa> is the address of the first errornous word relative to the start of the buffer.

<eeee> is the value of the data send.

<rrrr> is the value of the data received.

The errornumber of this type of error is 20.

20. DISPLAY DEMO TEST 20.

The Display Test of the RC750, PC, Selftest is intended for visual inspection of some of the facilities of the 82730 Display controller and the CRT logic.

This test cannot detect any errors with the help of the CPU. It is not a part of the power up test, and must therefore be requested explicit. See subsection 2.2.3.

The display test is split into four major parts. These are:

1. Show the complete character set supplied for the RC750, PC, Selftest.

2. Show a screen filled with "H". This can be used for geometric adjustment.

3. Show the numbers (0-9) in different colours to test the palet logic. When shown on a monochrome monitor the colours will be seen as different intensities.

4. Show some pseudo graphics. Some characters are shown in graphic/bit mapped mode.

Each of these mentioned display features are shown for a short period of time before the picture is changed to show the next feature.

It is possible, by enterring the chracter <1>, to freeze the present picture. To continue press <return> or <space>. If <space> is pressed, the main menu will be shown at the end of the test.

20.1 Colour/Intensity Test 20.1

The numbers 0-9 are shown several times on the screen. 40 numbers are shown for each combination of fore- and background. Fig. 29 illustrates the realtionship between the palet initialization and the colours shown.

block	foreground	background	palet
0	white	black	F0
1	yellow	blue	E1
14	blue	yellow	1E
15	black	white	0F
16	black	black	00
17	white	blue	F1
30	green	yellow	2E
31	blue	white	1F

Figure 29: Palet initialization.

20.2 Pseudo Graphic 20.2

The pseudo graphic is obtained by changing the control bit 3 in the 8255 PPI to graphic mode, whereby the characters Rc750 is showed in bit mapped form.

The characters has normally the size of 9x14 bits, but in graphic mode the size is 16x16. Some vertical bars is placed in between the normal size characters. This will form a raftered pattern on the screen.

21. FLEXIBLE DISK TEST 21.

The Flexible Disk Test of the RC750, PC, Selftest applies to the verification of the FD1797-02 flexible disk controller and the drives installed in the system. This is done on a level of verifying the ability of loading system software.

This test is not included in the default power up sequence, but must be requested explicit by setting the parameter "loop in test" to "Y", or the parameter "boot after test" to "N". See subsection 2.2.3.

The requirements for this test is one or two diskettes, which must be formatted. The normal system disk can be used, because the test is non destructive to the data stored on the media.

The procedure of the test is to perform some seeks and read sectors. Fig. 30 shows a table of sectors read from the disk. The purpose of the test is to ensure that the flexible disk channel is in a state, from which it is able to load system software. More intensive disk testing is to be performed with the RC750, Reliability programs.

track	sector	side
0	0*	0
0	1	0
70	7	1
34	3	0
75	6	1
76	5	0
20	2	1
35	4	0
0	2	1
76	1	1

Figure 30: Disk position table.

The test will be performed on those drives that are ready at the beginning of the test. Drive "B", if ready, will be tested first.

The testing is performed on the basis of the bootloader disk routines. These routines will operate with 5 retries on seeks and 10 retries on read sectors. No errormessage will occur before the operation fails in all of the retries.

*) The first position read from the disk is the loader segment. If the door is opened during this operation the following message will be written in the status line:

INSERT DISKETTE

If an error occurs during the flexible disk test, one of the following errormessages will be written:

Flexible disk: Data lost, stat: <rrrr>

Where

<rrrr> is the returned value of the status information from disk routines. The same as the content of the controller status register.

This error refers to a DMA underrun condition, which might be caused by a not formatted diskette.

The errornumber of this type of error is 26.

Flexible disk: CRC error, stat: <rrrr>

This error is caused by data error on the diskette.

The errornumber of this type of error is 27.

Flexible disk: Record not found, stat: <rrrr>

This error appears when the controller cannot find the sector number held in the controller.

The errornumber of this type of error is 28.

Flexible disk: Seek error, stat: <rrrr>

This error is caused when the track cannot be found during a seek operation.

The errornumber of this type of error is 29.

Flexible disk: NOT READY, stat: <rrrr>

This error appears, when the state of the drive changes from ready to not ready during execution of the test.

The errornumber of this type of error is 30.

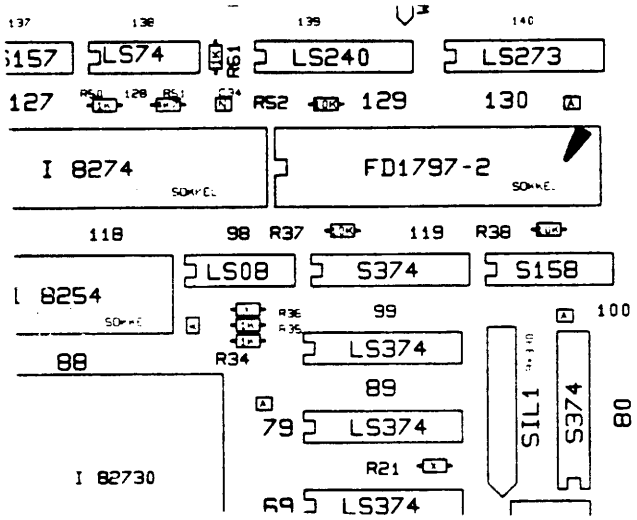


Figure 31: Locate the Flexible disk controller.

22. WINCHESTER DISK TEST 22.

The Winchester Disk Test of the RC750, PC, Selftest applies to the verification of the function of the SCSI interface, the disk controller (e.g. DTC510A) and a winchester drive. The testing is done on a level of verifying the ability of loading system software.

This test is not included in the default power up sequence, but must be requested explicit by setting the parameter "loop in test" to "Y", or the parameter "boot after test" to "N". See subsection 2.2.3.

The requirements for this test is a winchester disk, which must be formatted. The test is non destructive to the data stored on the media.

The procedure of the test is to perform some seeks and read blocks on the selected drive. The purpose of this test is to ensure that the Winchester disk channel and SCSI interface is in a state, from which it is able to load system software. More intensive disk testing is to be performed with the RC750, Reliability programs.

The first position read from the disk is the loader segment. Four other spots on the disk is read. These are the logical block numbers 10000, 2500, 7500, 5000. The block size read from the disk is 16x512 bytes.

If the test is run in not loop mode, the drive tested, will be the first unit number not being a flexible disk. When run in loop mode, it is possible to select an alternative medium to be tested. The test will ask the question "SELECT DRIVE" in the first pass of the test.

If an attempt is made to run the test on a non existing drive, a message as follows will be written:

Winchester disk: NON EXISTING MEDIUM.

The testing is performed on the basis of the bootloader winchester disk routines. The Winchester controller has the capability of performing retries, if errors are detected during seeks and read blocks. No error message will occur before the operation fails in all of the retries.

The DTC510A Winchester disk controller is equipped with some LED's for error indication, fig. 32 below lists the error indications as displayed by the controller.

Error Code (HEX, DS0 is LSB)	Interpretation
00	No Error
01	No Index from drive
02	No Track 00 from drive
03	Sector Address Out of Bounds
04	Drive not selected
05	No Seek Complete from Drive
06	No ID Address Mark
07	No Data Address Mark
08	Seek Error (Cylinder or Head not correct)
09	Sector not found
0A	ID ECC error
0B	No ACK from Host Adaptor
0C	Invalid Command
0D	Incorrect DATA MARK
0E	Incorrect ID MARK
0F	Incorrect cylinder address from drive
10	Incorrect sector address from drive
11	Incorrect head address from drive
12	Uncorrectable Data Error
13	Correctable Data Error
14	Drive not READY
15	Write fault
16	not used
17	Drive write protected
18	RAM diagnostic error
19 - 1E	not used
1F	Cannot read alternate track address.
20	Parity Error from host adaptor. If this error occurs, the host adaptor has a fault in the parity generation circuitry.
21	Bad Block detected from drive
22	Invalid function for this type
31	Attempted to directly access an alternate track.
32	Seek in Progress
33	Volume Overflow
81	Multiple Drives selected.
82	Sequencer time-out during a disk or a host transfer.

Figure 32: Winchester Controller errorcodes.

If an error should occur during the Winchester test, a message as one of the following will be written:

Winchester disk: drive status error, stat: <rrrr>

Where

<rrrr> is the SCSI error code from winchester sense command. See fig. 32.

This error refers to a type 0 error, which is drive related errors. See fig. 33.

The errornumber of this type of error is 31.

Winchester disk: Controller/data error, stat: <rrrr>

This error refers to a type 1 error, which is controller related. See fig. 33.

The errornumber of this type of error is 32.

Winchester disk: Command error, stat: <rrrr>

This error refers to a type 2 error. See fig. 33.

The errornumber of this type of error is 33.

Winchester disk: MISC error, stat: <rrrr>

This error refers to a type 3 error, which is related to a controller RAM error. See fig. 33.

The errornumber of this type of error is 34.

Winchester disk: Incorrect SCSI state.

This error will appear, when the SCSI-bus is in the busy state before the program accesses the interface.

The errornumber of this type of error is 35. See chapter 8.

Type_0_(Drive)_Error_codes.

0	No status
1	No Index signal.
2	No Seek Complete.
3	Write fault
4	Drive not ready
5	Drive not selected.
6	No Track00
7	Multiple drives selected.
D	Seek in progress.

Type_1_(Controller)_Error_codes.

0	ID read error. ECC error in the ID field.
1	Uncorrectable data error during a read.
2	ID Address Mark not found.
3	Data Address Mark not found.
4	Record not found. Found correct cylinder and head but not sector.
5	Seek error. R/W head positioned on a wrong cylinder and/or selected a wrong head.
6	Unused.
7	Write protected.
8	Correctable data field error.
9	Bad block found. Encountered a track with the Bad Track Flag set in the ID.
A	Format Error. The controller detected that during the Check Track command, the format on the drive was not expected.
C	Unable to read the Alternate Track address.
E	Attempted to directly access an alternate track.
F	Sequencer time-out error during a disk or a host transfer.

Type_2_(Command)_Error_codes.

0	Invalid Command received from the host.
1	Illegal disk address. Address is beyond the maximum address.
3	Volume overflow. Overflowed max address space while performing multiple blocks read/write operation.

Type_3_(Misc)_Error_codes.

0	RAM error. Data error detected during Sector buffer RAM diagnostic.

Figure 33: Winchester Error Code Description.

A. LIST OF ERROR NUMBERS A.

Error no.	Description
0	no error
1	PROM checksum error
2	RAM memory error (incl. pixel memory)
3	iAPX186 DMA data error
4	iAPX186 DMA count error
5	illegal interrupt
6	8259 timeout
7	test no. to big. Internal use only
8	CPU instruction exeption
9	RAM refresh error
10	iAPX186 timer error
11	8259 illegal interrupt level
12	iAPX186 interrupt timeout
13	iAPX186 illegal interrupt level
14	8274 parity error
15	8274 overrun
16	82730 CRT status error
17	Keyboard selftest error
18	PPI 8255 bit error
19	NVM checksum error
20	8274 SIO data error
21	X.21 status error
22	V.24 status error
23	8274 SIO timeout
24	Centronic control port error
25	Centronic data port error
26	Flexible disk data lost
27	Flexible disk CRC error
28	Flexible disk Record not found
29	Flexible disk Seek error
30	Flexible disk NOT READY
31	Winchester disk type 0
32	Winchester disk type 1
33	Winchester disk type 2
34	Winchester disk type 3
35	Incorrect SCSI state

RETURN LETTER

Title: RC750, iAPX186, PC Selftest Technical Guide

RCSL No.: 44RT 2102

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