Field Support Manual
System Controller P5020

Data
Systems

PHILIPS

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Great care has been taken to ensure that the information contained in this handbook is accurate and complete. Should any errors or omissions be discovered, however, or should any user wish to make a suggestion for improving this handbook, he is invited to send the relevant details to:

PHILIPS DATA SYSTEMS
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PUB. NO. 12th digit	UPDATE PACKAGE	SI. NO.	PAGES AFFECTED	DATE	REMARKS
1				8203	first issue
2	1		0-1 thr. 0-4 2-9 3-66 thr. 3-75 4-15 thr. 4-53 A-0 thr. A-14 B-0 thr. B-24 C-1 thr. C-20	8311	Added: - Version 'E' - Modification History - Drawings Config. Index Serial-to-Parallel Converter Shared Printer Controller Numeric Keypad

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LIST OF TABLES

2.3 DIFFERENCES BETWEEN VERSION C AND E

The functional differences between version C and E are:

- Version E can work directly with the control panel with reset.
- The protect attribute in version E is displayed as highlight instead of invert. This change is only affecting the Diagnostic program. See section 3.6.3.2 for detailed information.
- Version E is prepared for upgrading to a double character generator.
- The LED on version E is removed.

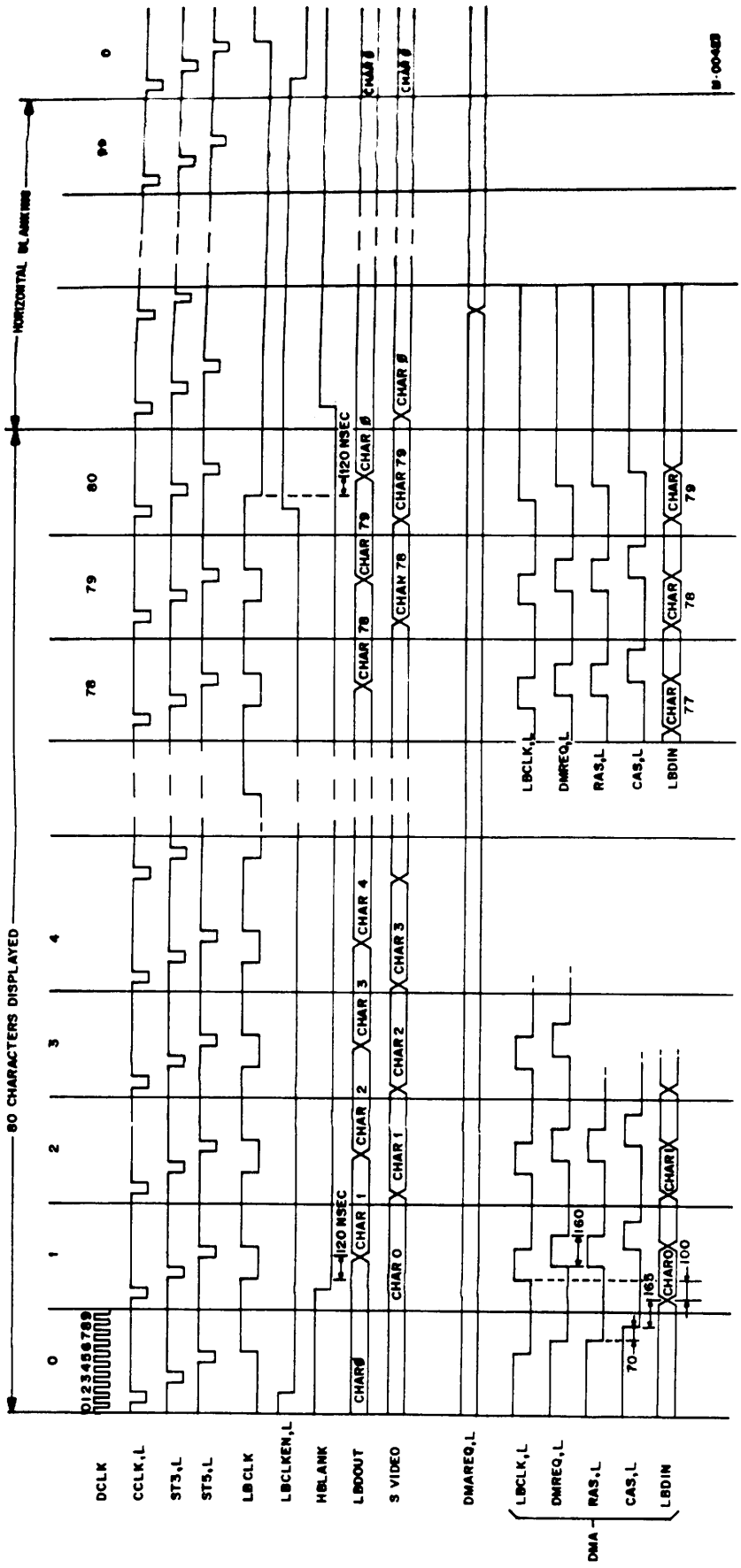


Figure 3-19 VIDEO TIMING (Sheet 2 of 2)

3.6 DETAILED DESCRIPTION OF DIFFERENCES BETWEEN VERSIONS C AND E (LEVELS 4 AND 6.4)

3.6.1 CPU PARTS

3.6.1.1 PRINTER INTERFACE

R 38 and C106 are added to RxD line.
R 33 is added to the BCTS line.
These modifications are installed to protect U23.

3.6.1.2 KEYBOARD INTERFACE

D-type FF U75 is dividing the BAUDCLK,L line by 2. The output of this FF is going to TxCA and RxCA of the DART and to the keyboard.
This modification results in a lower speed for keyboard communication and in an 50% duty cycle of the BAUDCLK,L.

3.6.1.3 I/O DECODING

The enabling of U78 is changed, but there are no functional difference.

3.6.1.4 RESET CIRCUITRY

RSET,L is going to connector J3, so that this PCB can be used in combination with the control panel PCB with reset.

3.6.2 MEMORY PART

The diodes on the RAS,L lines are removed.

3.6.3 VIDEO PART

3.6.3.1 CHARACTER GENERATOR

The character generator is prepared for upgrading to a double character generator. It is possible on this PCB to use either a row attribute (U81/pin2) or the character attribute protect (invert) for selecting one of the two sets of characters.
At present it is not used in any program.

3.6.3.2 ATTRIBUTE COMBINER

The attribute combiner is changed so that we have the following situation concerning the character attributes.

IBM,L active (normal WP programs):	UNDERLINE,L	displayed as UNDERLINE
	DPROTECT,L	displayed as HIGHLIGHT
IBM,L inactive :	UNDERLINE,L	displayed as BLANKING
	DPROTECT,L	displayed as HIGHLIGHT

NOTE: Blanking a certain character means this character is not displayed.
DPROTECT is called like that because in some application programs this attribute is used to indicate information which cannot be changed.

3.6.3.2 VIDEO OUTPUT STAGE

P1 is removed and fixed resistors are installed.

3.6.4 SLAVE CPU PART

3.6.4.1 ROM

This ROM is prepared for working with this level and is functional equal to ROM version 8.2 C. This ROM can not be interchanged with the ROM's of version C.

3.6.4.2 LED

The D-type FF for controlling the LED's is removed. Also the LED itself is removed. The LED on the control panel PCB is now controlled via U21.

3.6.4.3 MASTER-ON FF AND BOOT FF

These FF's are now controlled by the master CPU using the MSRQ and data lines MSD0 and MSD1.
The strap pins for strap W2 are removed. The slave CPU can still be started by shorting the two soldering points on the original position.

3.6.4.4 MASTER/SLAVE BUFFER CONTROL

Both control lines of U19 (CE,L and DIR,L) are now controlled via two D-types FF's (U66). This is done to extend a read or write cycle.

3.6.4.5 FLOPPY DISK CONTROLLER RESET

The reset line of the FDC is now direct controlled by a line coming from U21.

3.6.4.6 PHASE-LOCKED LOOP

The phase-locked loop consists of oscillator U1, comparator/ charge pump/ amplifier U5, counter U6 and part of U138 PAL. Figure 3.20 gives a block diagram of the phase-locked loop system.

The basic principle of the circuit is as follows:

U6 divides the 4MHz clock by 8 and feeds this as a reference signal to U5 comparator. This signal is compared with the output of oscillator U1. Time differences between the falling edges of REF and VAR cause a DC control signal, proportional to the error, to be generated. The error signal modifies the frequency of U1 until REF and VAR are synchronised. Granted Read Data (GRDAT-N) resets the counter when data is received. This synchronises REF, and thus VAR, to the read data.

Unfortunately, this simple method does not produce the best results in every case, therefore the circuit is modified in version "E". The PLL operates now in 3 modes:

STANDBY MODE

In this mode, which occurs before VCO SYNC goes high, the counter acts as a divider. It is not loaded or cleared by any other signal. Because VCO SYNC is low, DSYNC and GRDAT-N are both false, thus CNT RES (counter reset) and GRDAT-N cannot control U6. DSYNC low holds U138B reset, making FLOPUT (F/F output) true and gating VCOSC from U1 to the VAR input of U5. PLLVI (phase-locked loop, variable in) is in this case, an inversion of VCOSC. VCOSC is pulled into phase with REF (Q2).

LOCK-UP MODE

This mode, which occurs after VCO SYNC but before DSYNC, rapidly brings VCOSC into synchronisation with incoming data. VCO SYNC goes true during the VCO synchronisation bytes which occur after each gap. This action allows GRDAT-N to synchronise U6, and thus U1, to incoming data.

When RD DATA-N goes low, a positive pulse (less than 100 nanaseconds) is generated at U9 and U3. While GRDAT-N is low, U6 is loaded with decimal 12 and then counted on until the next read data pulse reloads the counter. Differences between falling edges of Q2 (REF) and PLLVI (VAR) bring VCOSC quickly into synchronisation.

Note that comparison between REF and VAR are made on every falling edge. The resulting control voltage brings OSC very quickly into synchronisation with the sync. bytes. However, in this mode the PLL is unable to follow large amounts of bit shift.

LOCK MODE

When LOCK-UP is achieved, the bit-shift handling capability can be improved by reducing the number of comparisons. This effectively reduces the control loop gain.

Approx. 70 microseconds after VCO SYNC, DSYNC goes high, thus releasing the reset of U138B and enabling 'AND' gates A and C. The delay is caused by R9 and C5. If Q3 is low and GRDAT-NN is high, counter U6 will be cleared and will remain cleared until the next read data pulse.
GRDAT-N true, removes CNTRES, loads U6 with 12 and sets U138B. FLOPUT goes low and PLLVI goes high.

U6 counts through 15 to zero, thus making CNTRES true once more. The counter will now be held cleared until the next GRDAT-N pulse. The first rising edge of VCOSC makes FLOPUT true and drives PLLVI low. This falling edge is compared to the falling edge of Q2.

From figure 3.21 is should be clear that in this mode, comparisons are only made when a RD DATA-N is received.

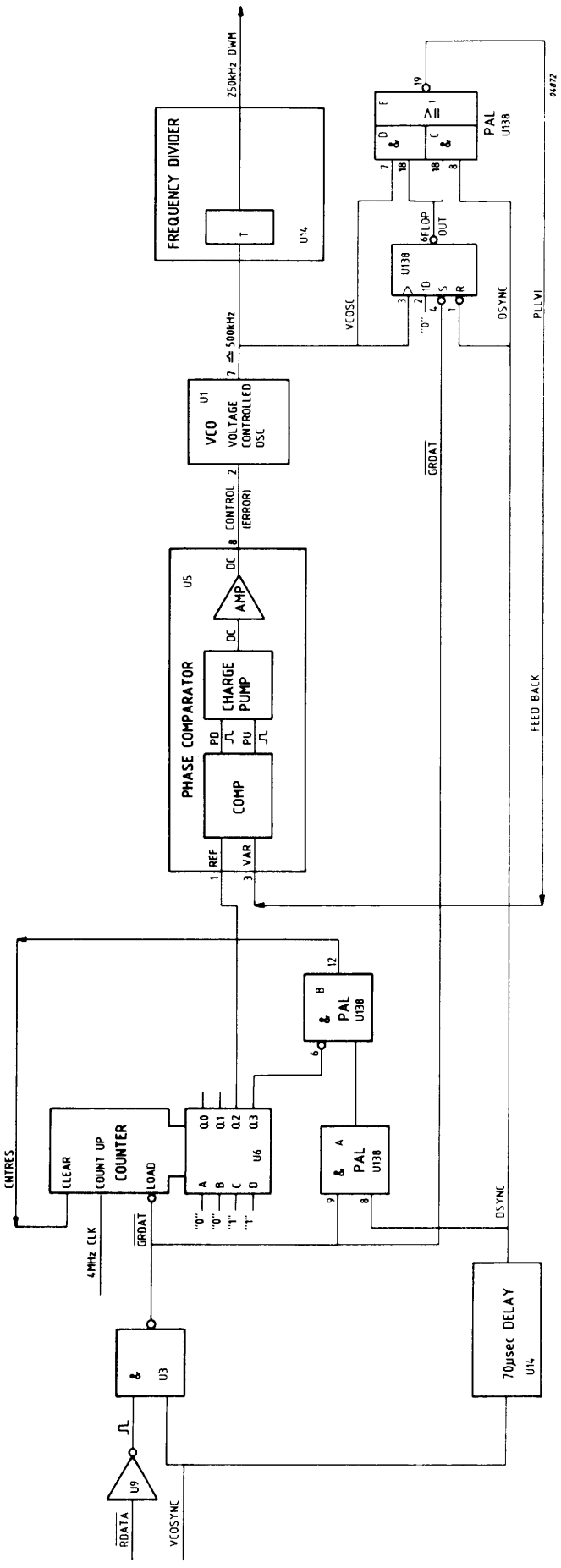


Figure 3.20 GENERATION OF DATA WINDOW

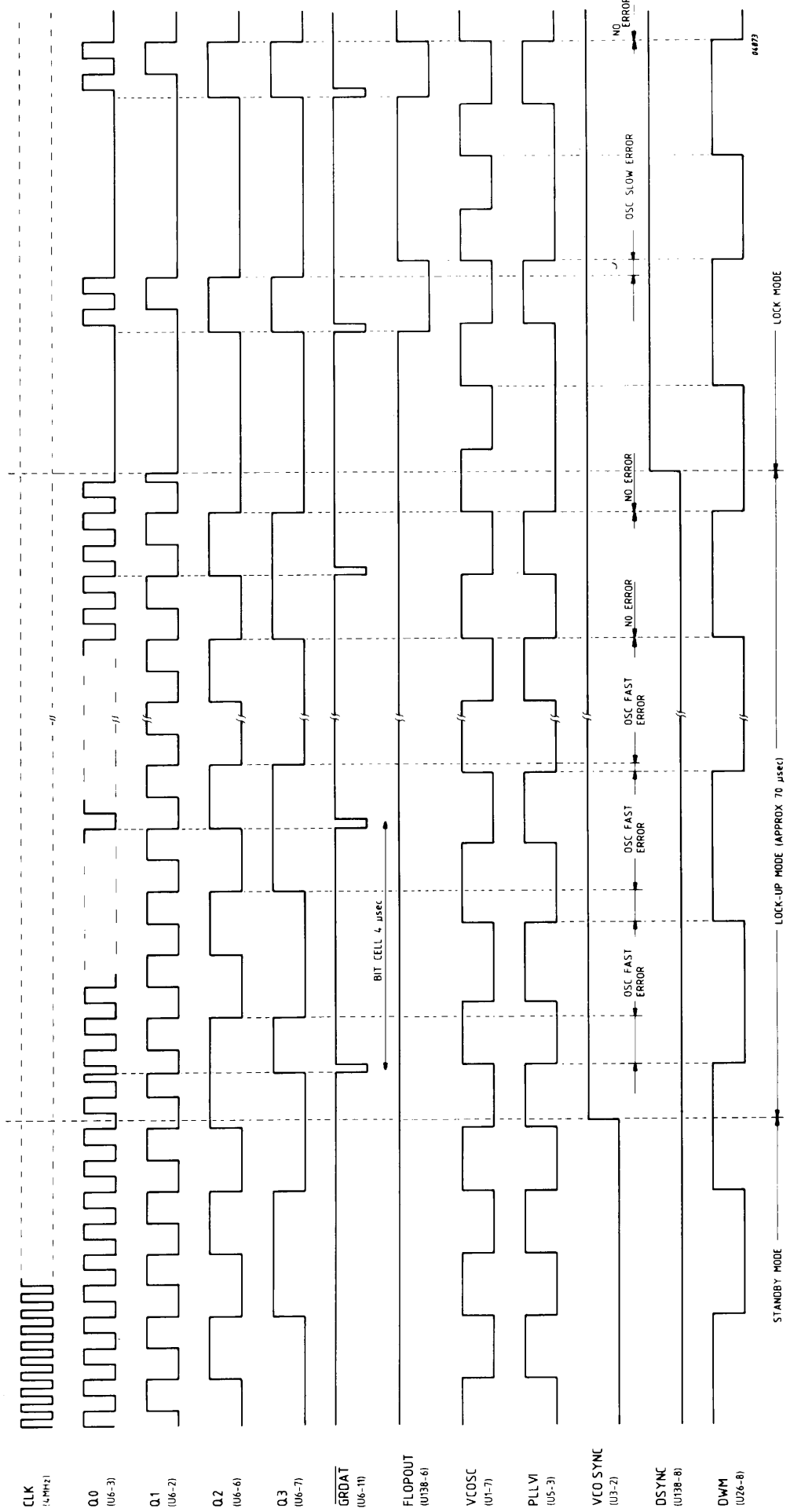


Figure 3.21 DATA WINDOW TIMING

3.6.4.7 DATA WINDOW GENERATION

The Read Data Window for MFM mode is produced by dividing VCOSC by 2. This produces a data window suitable for 4 microseconds (MFM) mode.

The waveforms of figure 3.21 represent the VCO synchronisation bytes and MFM mode. Note that the GRDAT-N pulses shown are all clock pulses. By recognising that clock pulses occur when DWM is high, the FDC can check for data pulses when DWM is low. This occurs in the middle of the bit cell. The window will be moved to accomodate disk speed variations or bit-shift.

3.6.4.8 PHASE-LOCKED LOOP COMPONENTS

The basic frequency range of U1 voltage controlled oscillator (VCO) is selected by the voltage at pin 3 and the capacity across pins 4 and 5. Therefore the uncontrolled frequency is selected by R3, R7 and C3. By applying a positive or negative voltage to pin 2, the output frequency can be increased or decreased around the selected frequency.

Phase-frequency detector IC5 is designed to control a VCO by detecting phase or frequency errors, and generating a DC voltage to bring the VCO into step with reference frequency.

The chip contains a detection, a charge pump and amplifier. The detector detects a difference between falling edge of the REF signal at pin 1 and VCO derived signal at pin 3, and generates PD (pump down) or PU (pump up) if the VAR frequency is too high or too low respectively.

PU or PD pulses feed a charge pump (integrator) which outputs a DC voltage at U5-5/10 to correct the error. U5-9 and 8 is an amplifier which controls U1 via the charge on C4.

3.7 DIFFERENCE BETWEEN HARDWARE LEVELS 6.4 AND 7

These differences are found in the video part of the PCB.

3.7.1 CHARACTER GENERATOR

The selection between the (optional) two character sets is changed. In level 7 the selection is done with FF U63/pin 5.
On all the old levels, this FF was used to generate the IBM signal (for changing the character attributes). The IBM signal in 7 is implemented as a row-attribute and is therefore coming from U81/pin 2.

3.7.2 CHARACTER ATTRIBUTES

The way character attributes are displayed on the screen is changed to the old (level 1-4) situation again.

IBM,L active (normal WP programs): UNDERLINE,L displayed as UNDERLINE
DPROTECT,L displayed as INVERT

IBM,L inactive : UNDERLINE,L displayed as BLANKING
DPROTECT,L displayed as HIGHLIGHT

3.8 DIFFERENCE BETWEEN HARDWARE LEVELS 7 AND 8

In hardware level 8 the master CPU is mounted on a piggyback. This piggyback contains also a buffer for the data bus. This buffer is required for future extensions.

3.9 MODIFICATION HISTORY

Refer to the P5020 SI's for modifications on the system.

P5020-001	P5020	Memory test EPROM	821014
P5020-002	P5020	P5020 Diagnostic Package	821221
P5020-003	P5020	Read problems on mini disk drives	821221
P5020-004	P5020	Wrong P5020 PCB support frame	821221
P5020-005	P5020/1	Possibility of trace shorting on control panel via E-Kote	821221
P5020-006	P5020	P5020 Diagnostic Package (revised)	830217
P5020-007	P5020	Memory test EPROM (revised)	830217
P5020-008	P5020	Modification PSU and main controller	830407
P5020-009	P5020	New level IPL PROM	830321
P5020-010	P5020	Problems with PAL	830322
P5020-011	P3000 P5000	Mini flexible disk doors	830606
P5020-012	P5020	Program laod programs	830616
P5020-013	P5020	Error messages	830616
P5020-014	P5020	Redesigned main controller	830729
P5020-015	P5020/3/4/5 P5020	Platen clutch parts	830624
P5020-016	P5350	Philips version "paper out" PCB for ASF 580 sheetfeeder	830803
P5020-017	P5020	No protected video E-SWIFT controller: 5107 299 91316.1.	830901
P5020-018	P5020	Redesigned control panel	
P5020-019	P5350/60	Installation hints for sheetfeeders	830829
P5020-020	P5130-09 P5131-03	Pagelength setting	830915
P5020-021	P5131-05	New firmware for the TEC printer	830927
P5020-022	P5331-03	Overprinting and skewed printout	831006

3.10 DRAWING CONFIGURATION INDEX

DRAWINGS 5107 299 9131X		HARDWARE LEVEL								
		C		E						
		2	4	6	6.1	6.2	6.3	6.4	7	8
Sheet 1	ISS	4	4	8	8	8	8	8	8	8
	Page	4-3	4-3	4-35	4-35	4-35	4-35	4-35	4-35	4-35
Sheet 2	ISS	4	4	8	8	8	8	8	8	8
	Page	4-5	4-5	4-37	4-37	4-37	4-37	4-37	4-37	4-37
Sheet 3	ISS	4	4	8	8	8	8	8	8	8
	Page	4-7	4-7	4-39	4-39	4-39	4-39	4-39	4-39	4-39
Sheet 4	ISS	4	4	8	8	8	8	8	8	8
	Page	4-9	4-9	4-41	4-41	4-41	4-41	4-41	4-41	4-41
Sheet 5	ISS	4	4	6.4	6.4	6.4	6.4	6.4	8	8
	Page	4-11	4-11	4-31	4-31	4-31	4-31	4-31	4-43	4-43
Sheet 6	ISS	4	4	6.4	6.4	6.4	6.4	6.4	8	8
	Page	4-13	4-13	4-33	4-33	4-33	4-33	4-33	4-45	4-45
Sheet 7	ISS	4	4	8	8	8	8	8	8	8
	Page	4-15	4-47	4-47	4-47	4-47	4-47	4-47	4-47	4-47

Note 1: Between most hardware levels there are only minor changes. Therefore only a selected set of drawings are supplied. Each time the highest levels are given.

Note 2: In version 8 the master CPU is mounted on a piggyback. The schematic of this piggyback is given on page 4-53.

DRAWING NO.
5107 299 91314

NOTES:

1 UNLESS OTHERWISE SPECIFIED
RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4W
CAPACITOR VALUES ARE IN MICROFARADS, ± 20%

2 COMPONENTS IN DOTTED LINES ARE MOUNTED ON RESPECTIVE BOARDS FOR PARTSLISTS REFER TO CORRESPONDING 12NC WITHIN DOTTED LIMITS

ISS	DESCRIPTION	DATE
2	DRAWING CREATED UNDER ECO 182	4 9 81
3	SCHEMATIC REVISED AS PER ECO 148	11 12 81
4	SCHEMATIC REVISED AS PER ECO 350	6 4 82

Figure 4.3
SYST. CNTR. SCHEM. (C/4) SH. 1 of 7

DRAWING NO
5107 299 91314

ISS	DESCRIPTION	DATE
2	DRAWING CREATED UNDER ECO 102	4-9-81
3	SCHEMATIC REVISED AS PER ECO 148	11-12-81
4	SCHEMATIC REVISED AS PER ECO 330	10-6-82

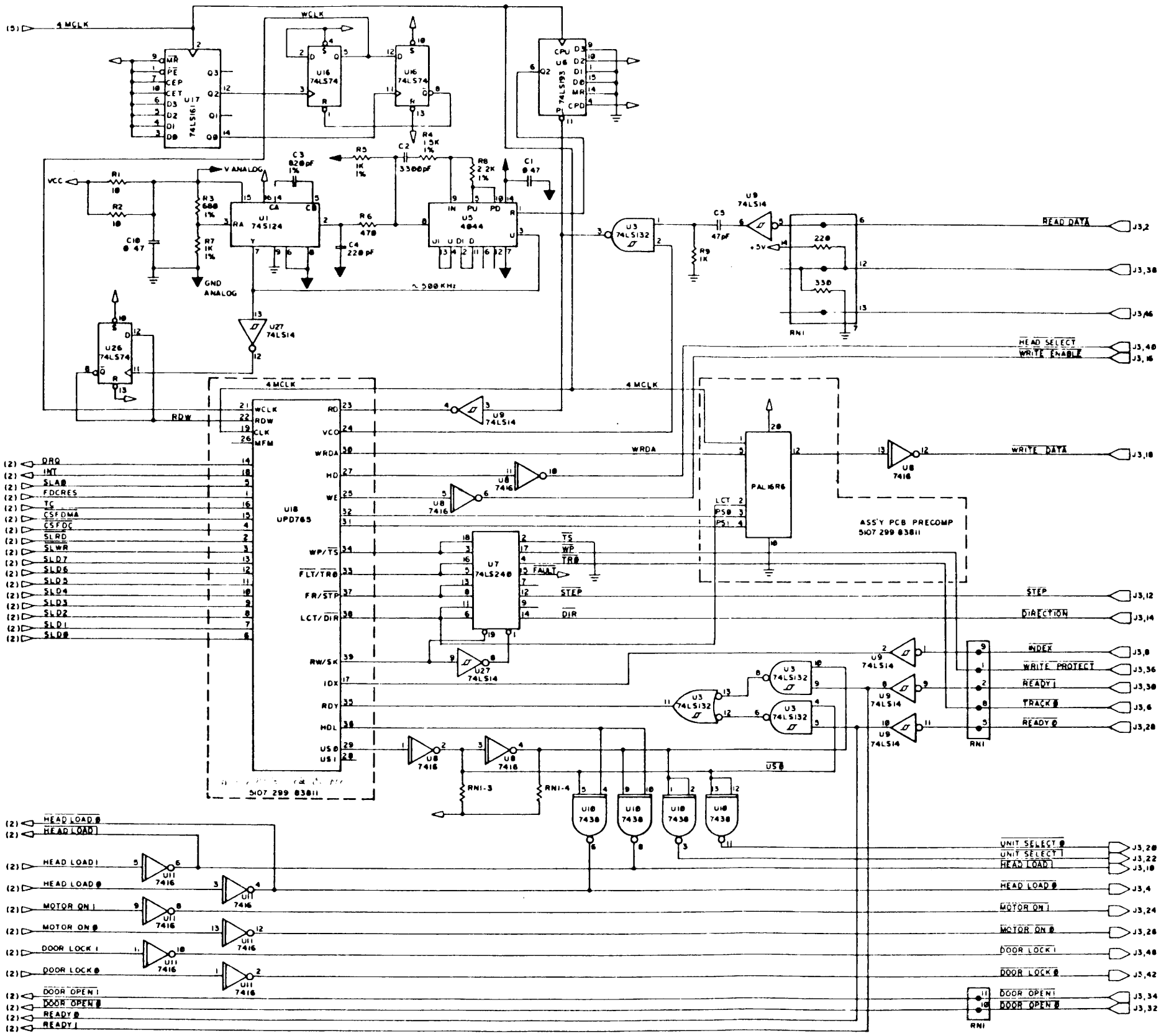
Figure 4.3
SYST. CNTR. SCHEM. (C/4) SH. 2 of 7

DRAWING NO
5107 299 91314

ISS	DESCRIPTION	DATE
2	DRAWING CREATED UNDER ECO 182	4-9-81
3	SCHEMATIC REVISED AS PER ECO 148	11-12-81
4	SCHEMATIC REVISED AS PER ECO 350	16-4-82

Figure 4.3
SYST. CNTR. SCHEM. (C/4) SH. 3 of 7

DRAWING NO
5107 299 91314



ISS	DESCRIPTION	DATE
2	DRAWING CREATED UNDER ECO 82	4 9 81
3	SCHEMATIC REVISED AS PER ECO 148	11-12-81
4	SCHEMATIC REVISED AS PER ECO 350	16 4 82

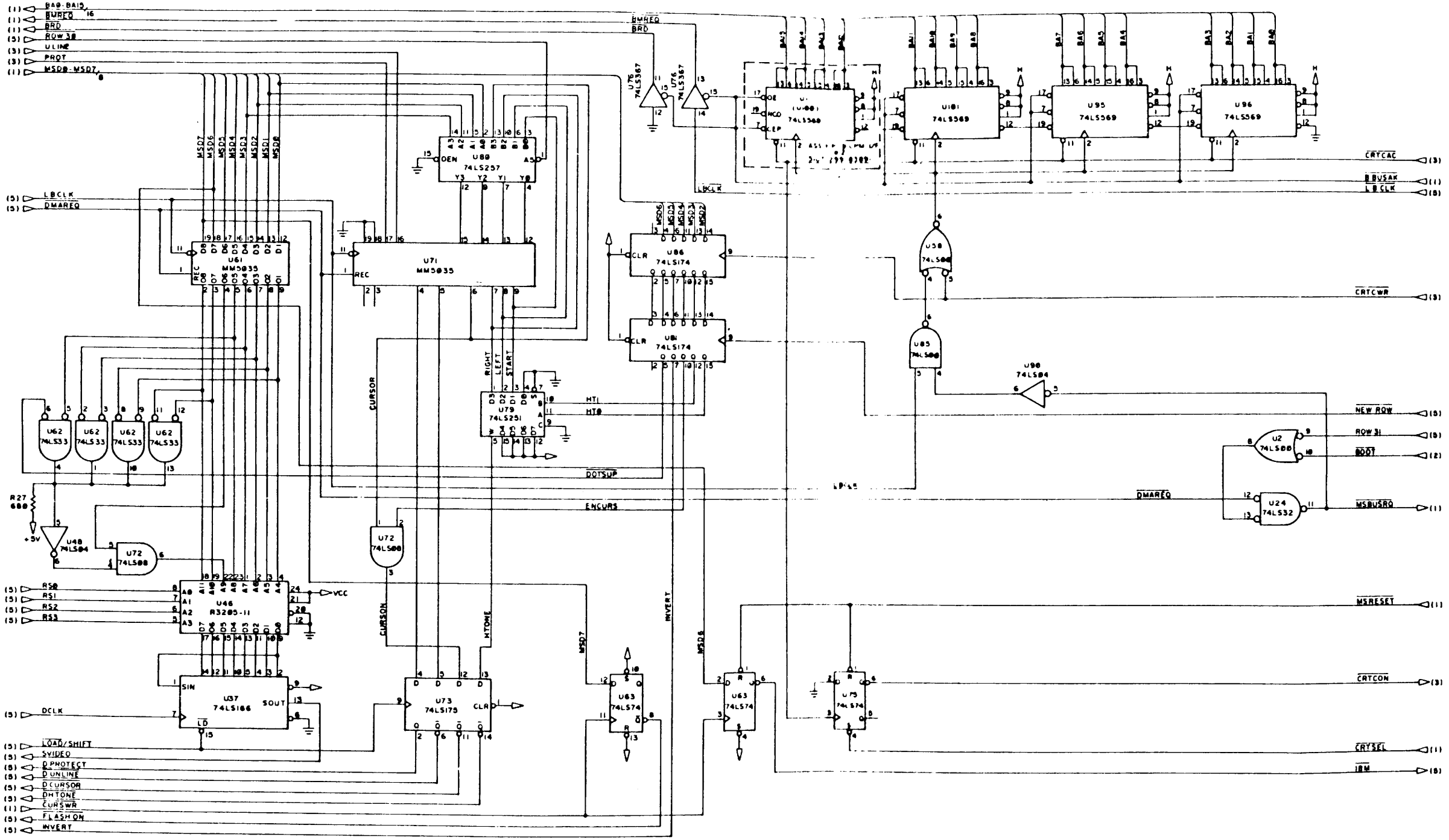
Figure 4.3
SYST. CNTR. SCHEM. (C/4) SH. 4 of 7

DRAWING NO
5107 299 91314

ISS	DESCRIPTION	DATE
2	DRAWING CREATED UNDER ECO 182	4-9-81
3	SCHEMATIC REVISED AS PER ECO 148	11-12-81
4	SCHEMATIC REVISED AS PER ECO 350	16-4-81

Figure 4.3
SYST. CNTR. SCHEM. (C/4) SH. 5 of 7

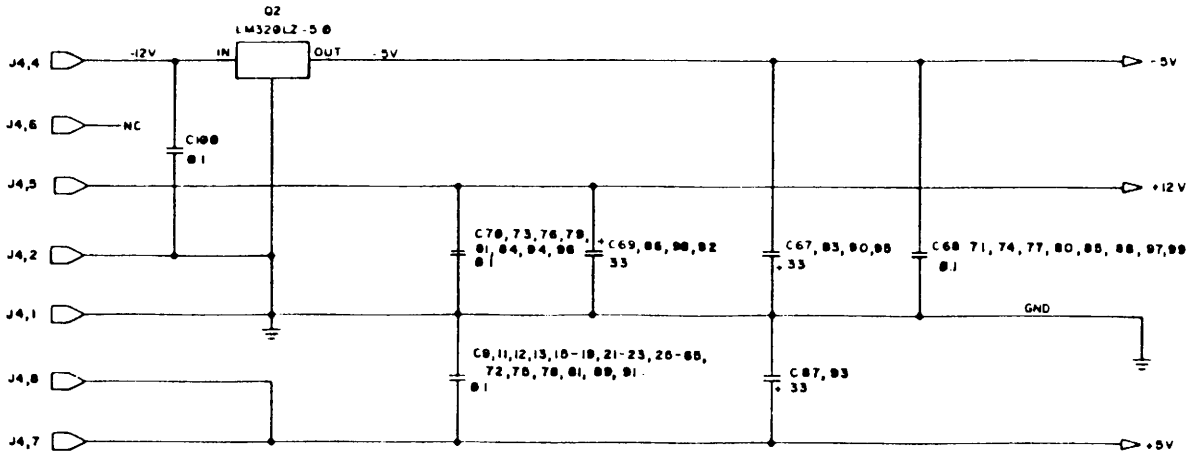
DRAWING NO
5107 299 91314

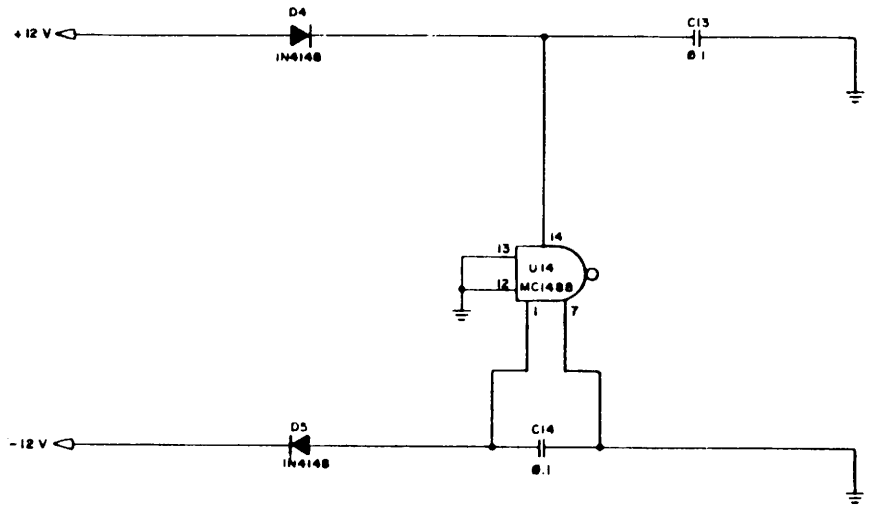


ISS	DESCRIPTION	DATE
2	DRAWING CREATED UNDER ECO 82	4-9-81
3	SCHEMATIC REVISED AS PER ECO 48	11-12-81
4	SCHEMATIC REVISED AS PER ECO 150	16-4-82

Figure 4.3
SYST. CNTR. SCHEM. (C/4) SH. 6 of 7

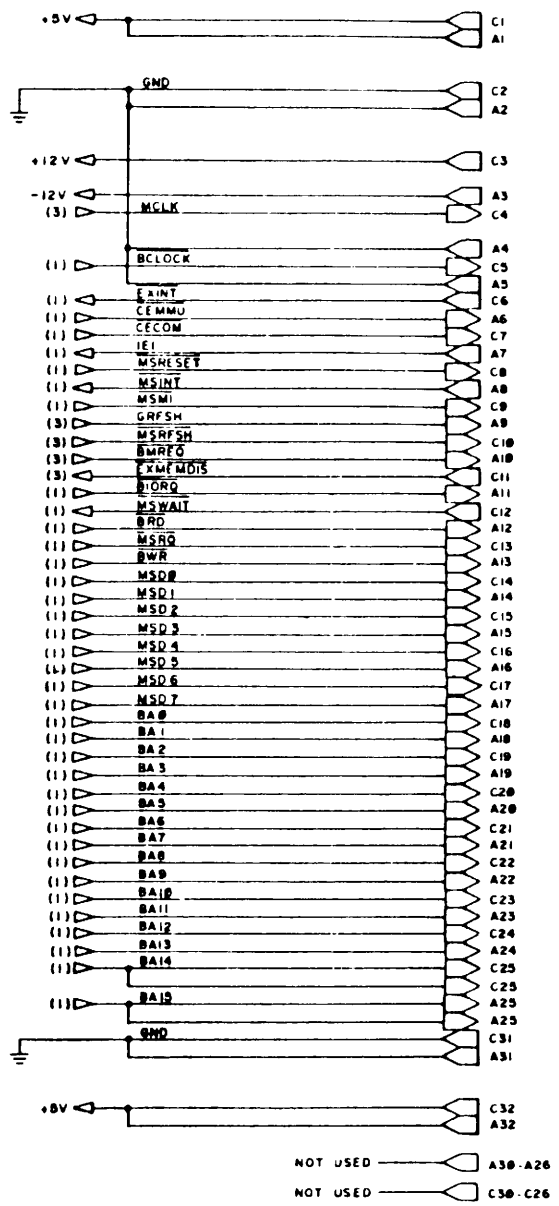
DRAWING NO
5107 299 91314





ECO	DESCRIPTION	DATE
2	DRAWING CREATED UNDER ECO 182	4-9-81
3	SCHEMATIC REVISED AS PER ECO 148	11-12-81
4	SCHEMATIC REVISED AS PER ECO 350	16-4-82

OPTION CONNECTORS (J1 & J2 IDENTICAL)

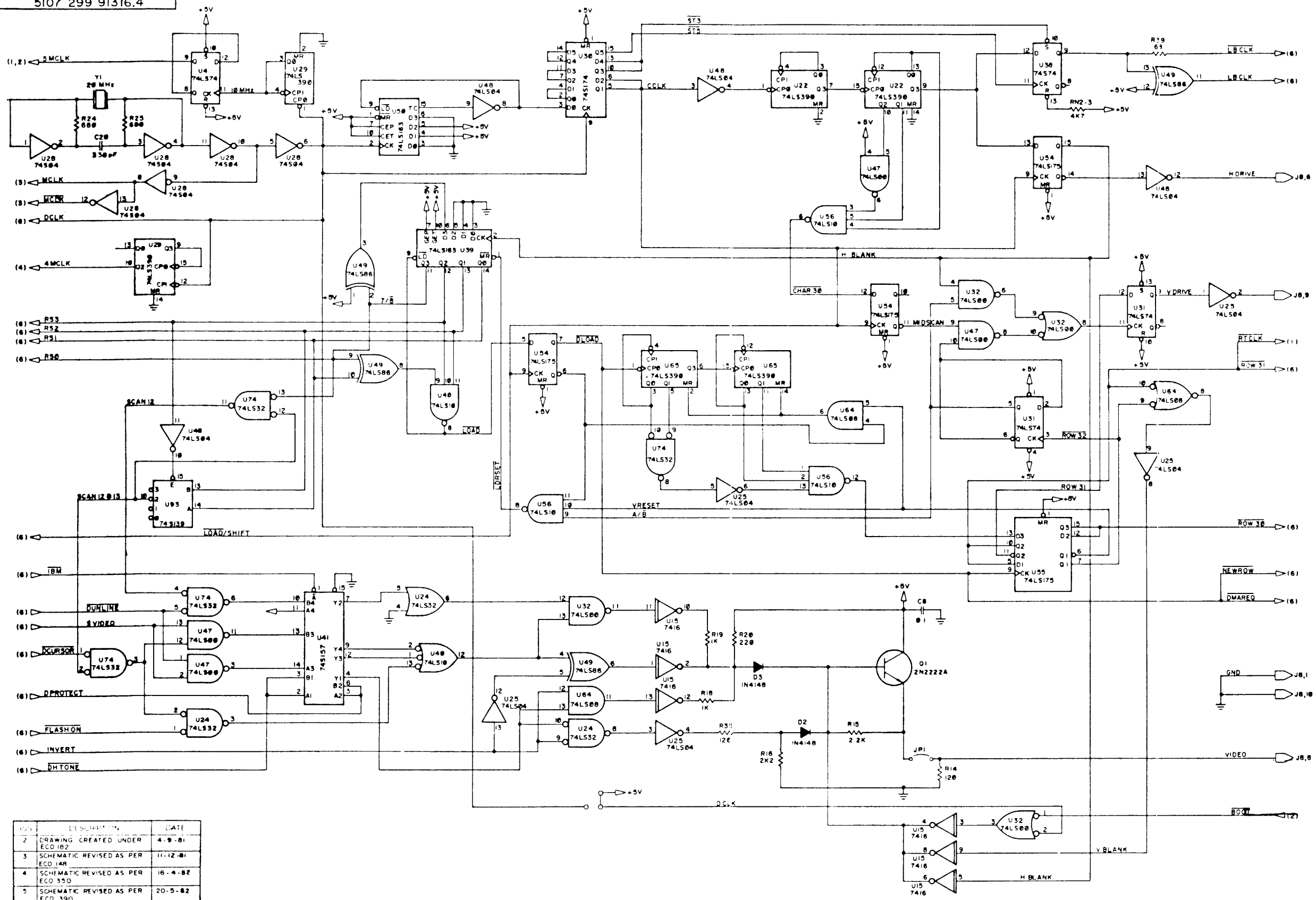


SPARE GATE TABLE

REF DESIGN	DESCRIPTION	PIN NOS	TOTAL GATES
U2	74LS00	11,12,13	3/4
U9	74LS14	12,13	5/6
U23	MC3486	5,6,7	3/4
U25	74LS04	10,11	5/6
U27	74LS14	10,11	5/6
U48	74LS18	3,4,5,6	2/3
U58	74LS08	11,12,13	3/4
U64	74LS08	1,2,3	3/4
U66	74S74	8,9,10,11,12,13	1/2
U72	74LS08	8,9,10,11,12,13	2/4
U85	74LS00	1,2,3	3/4
U92	74LS08	1,2,3	3/4
RN5	68	3,4	-

Figure 4.3
SYST. CNTR. SCHEM. (C/4) SH. 7 of 7

DRAWING NO
5107 299 91316.4



ISS	DESCRIPTION	DATE
2	DRAWING CREATED UNDER ECO 182	4-9-81
3	SCHEMATIC REVISED AS PER ECO 148	11-12-81
4	SCHEMATIC REVISED AS PER ECO 350	18-4-82
5	SCHEMATIC REVISED AS PER ECO 390	20-5-82
6	PARTS LIST UPDATE ONLY AS PER ECO-348	16-07-82
6.1	SCHEMATIC REVISED AS PER ECO 490	
6.2	NEW 12NC STICKER IMPLEMENTED AS PER ECO 486	1-11-82
6.3	SCHEMATIC REVISED AS PER ECO 548	19-11-82
6.4	SCHEMATIC REVISED AS PER ECO 680	

Figure 4.4
SYST. CNTR. SCHEM. (E/6.4) SH. 5 of 7

DRAWING NO
5107 299 91316.4

ISS	DESCRIPTION	DATE
2	DRAWING CREATED UNDER ECO 182	4-9-81
3	SCHEMATIC REVISED AS PER ECO 148	11-12-81
4	SCHEMATIC REVISED AS PER ECO 350	16-4-82
5	SCHEMATIC REVISED AS PER ECO 390	20-5-82
6	PARTS LIST UPDATE ONLY AS PER ECO-348	16-07-82
6.1	SCHEMATIC REVISED AS PER ECO 490	
6.2	NEW 12NC STICKER IMPLEMENTED AS PER ECO 486	1-11-82
6.3	SCHEMATIC REVISED AS PER ECO 558	1-07-83
6.4	SCHEMATIC REVISED AS PER ECO 660	

U46	N/A	5107 299 8495X	REGULAR CHAR GENERATOR
U46	EUR.	5107 299 8494X	REGULAR CHAR GENERATOR
U46	N/A	5107 299 8422X	CHAR GEN WITH GREEK SYM
U46	EUR	5107 299 8421X	CHAR GEN WITH GREEK SYM
X	COUNTRY	5107 299 XXXXX	DESCRIPTION

Figure 4.4
SYST. CNTR. SCHEM. (E/6.4) SH. 6 of 7

DRAWING NO
5107 299 91318

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4W
   CAPACITOR VALUES ARE IN MICROFARADS, ± 20%
2. COMPONENTS IN DOTTED LINES ARE MOUNTED ON RESPECTIVE BOARDS FOR PARTSLISTS REFER TO CONNECTIONING DRG WITHIN DOTTED LIMITS
3. IN PLACE OF U80 USE "ASS'Y PCB CPU PIGGY-BACK" 5107 265 088XX.

2	DRAWING CREATED UNDER ECO 182	4-9-81
3	SCHEMATIC REVISED AS PER ECO 148	11-12-81
4	SCHEMATIC REVISED AS PER ECO 350	16-4-82
5	SCHEMATIC REVISED AS PER ECO 390	20-5-82
6	PARTS LIST UPDATE ONLY AS PER ECO-348	16-07-82
6.1	SCHEMATIC REVISED AS PER ECO 490	
6.2	NEW I2NC STICKER IMPLEMENTED AS PER ECO 486	1-11-82
6.3	SCHEMATIC REVISED AS PER ECO 558	
6.4	SCHEMATIC REVISED AS PER ECO 660	
7	NEW ARTWORKS RELEASED AS PER ECO 641	
8	NOTE 3 ADDED AS PER ECO 676	

Figure 4.5
SYST. CNTR. SCHEM. (E/7) SH. 1 of 7

DRAWING NO:
5107 299 91318

2	DRAWING CREATED UNDER ECO 182	4-9-81
3	SCHEMATIC REVISED AS PER ECO 148	11-12-81
4	SCHEMATIC REVISED AS PER ECO 350	16-4-82
5	SCHEMATIC REVISED AS PER ECO 390	20-5-82
6	PARTS LIST UPDATE ONLY AS PER ECO-348	16-07-82
6.1	SCHEMATIC REVISED AS PER ECO 490	
6.2	NEW 12NC STICKER IMPLEMENTED AS PER ECO 486	1-11-82
6.3	SCHEMATIC REVISED AS PER ECO 558	
6.4	SCHEMATIC REVISED AS PER ECO 660	
7	NEW ARTWORKS RELEASED AS PER ECO 641	
8	NOTE 3 ADDED AS PER ECO 676	

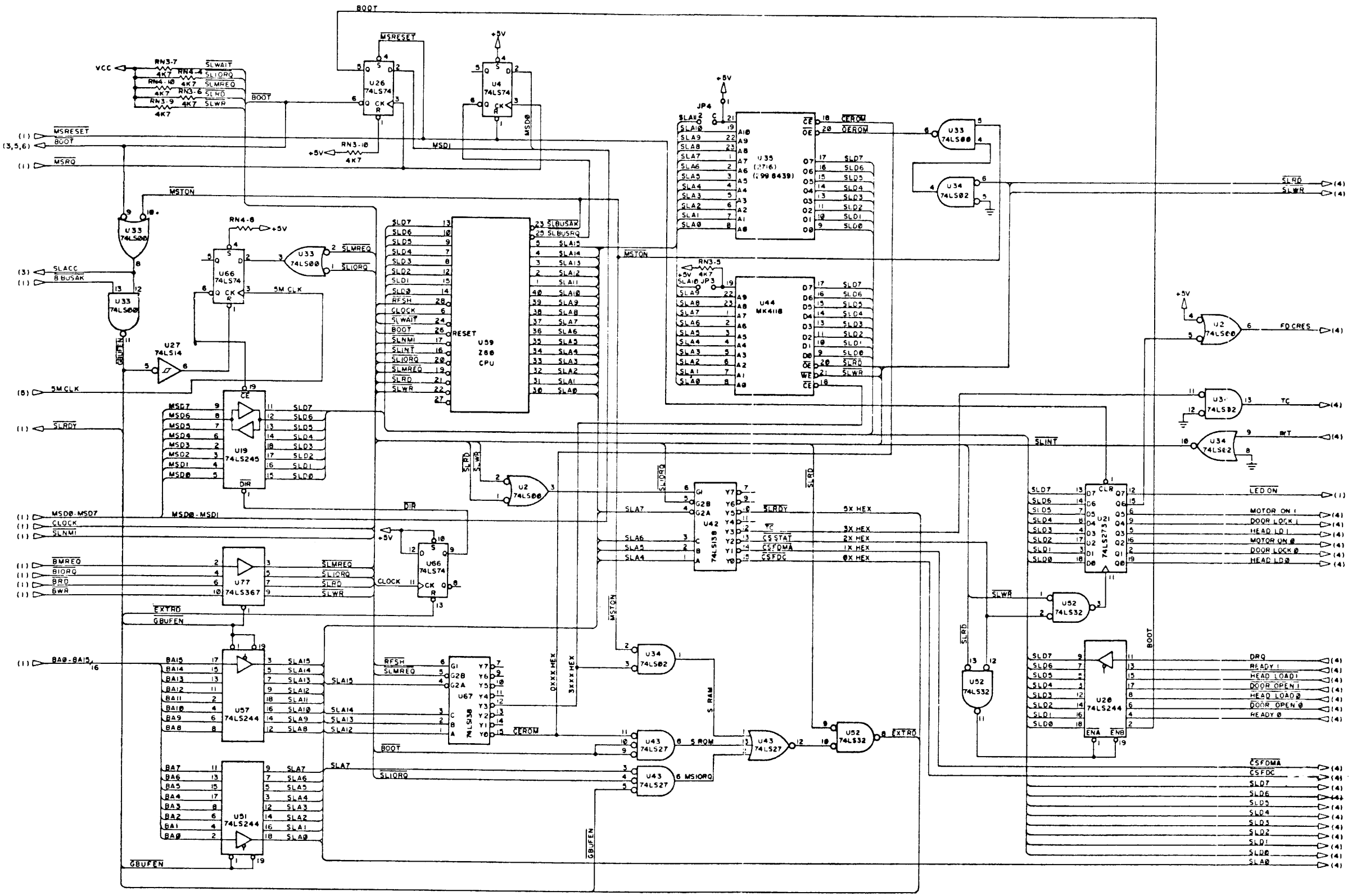


Figure 4.5
SYST. CNTR. SCHEM. (E/7) SH. 2 of 7

5107 299 91318

2	DRAWING CREATED UNDER ECO 182	4-9-81
3	SCHEMATIC REVISED AS PER ECO 148	11-12-81
4	SCHEMATIC REVISED AS PER ECO 350	16-4-82
5	SCHEMATIC REVISED AS PER ECO 390	20-5-82
6	PARTS LIST UPDATE ONLY AS PER ECO-348	16-07-82
6.1	SCHEMATIC REVISED AS PER ECO 490	
6.2	NEW 12NC STICKER IMPLEMENTED AS PER ECO 486	1-11-82
6.3	SCHEMATIC REVISED AS PER ECO 558	
6.4	SCHEMATIC REVISED AS PER ECO 660	
7	NEW ARTWORKS RELEASED AS PER ECO 641	
8	NOTE 3 ADDED AS PER ECO 676	

Figure 4.5
SYST. CNTR. SCHEM. (E/7) SH. 3 of 7

DRAWING NO
5107 299 91318

2	DRAWING CREATED UNDER ECO 182	4-9-81
3	SCHEMATIC REVISED AS PER ECO 148	11-12-81
4	SCHEMATIC REVISED AS PER ECO 350	16-4-82
5	SCHEMATIC REVISED AS PER ECO 390	20-5-82
6	PARTS LIST UPDATE ONLY AS PER ECO-348	16-07-82
6 1	SCHEMATIC REVISED AS PER ECO 390	
6 2	NEW TINC STICKER IMPLEMENTED AS PER ECO 486	1-11-82
6 3	SCHEMATIC REVISED AS PER ECO 558	8-03-83 1
6 4	SCHEMATIC REVISED AS PER ECO 660	
7	NEW ARTWORKS RELEASED AS PER ECO 641	17-06-83
8	NOTE 3 ADDED AS PER ECO 676	

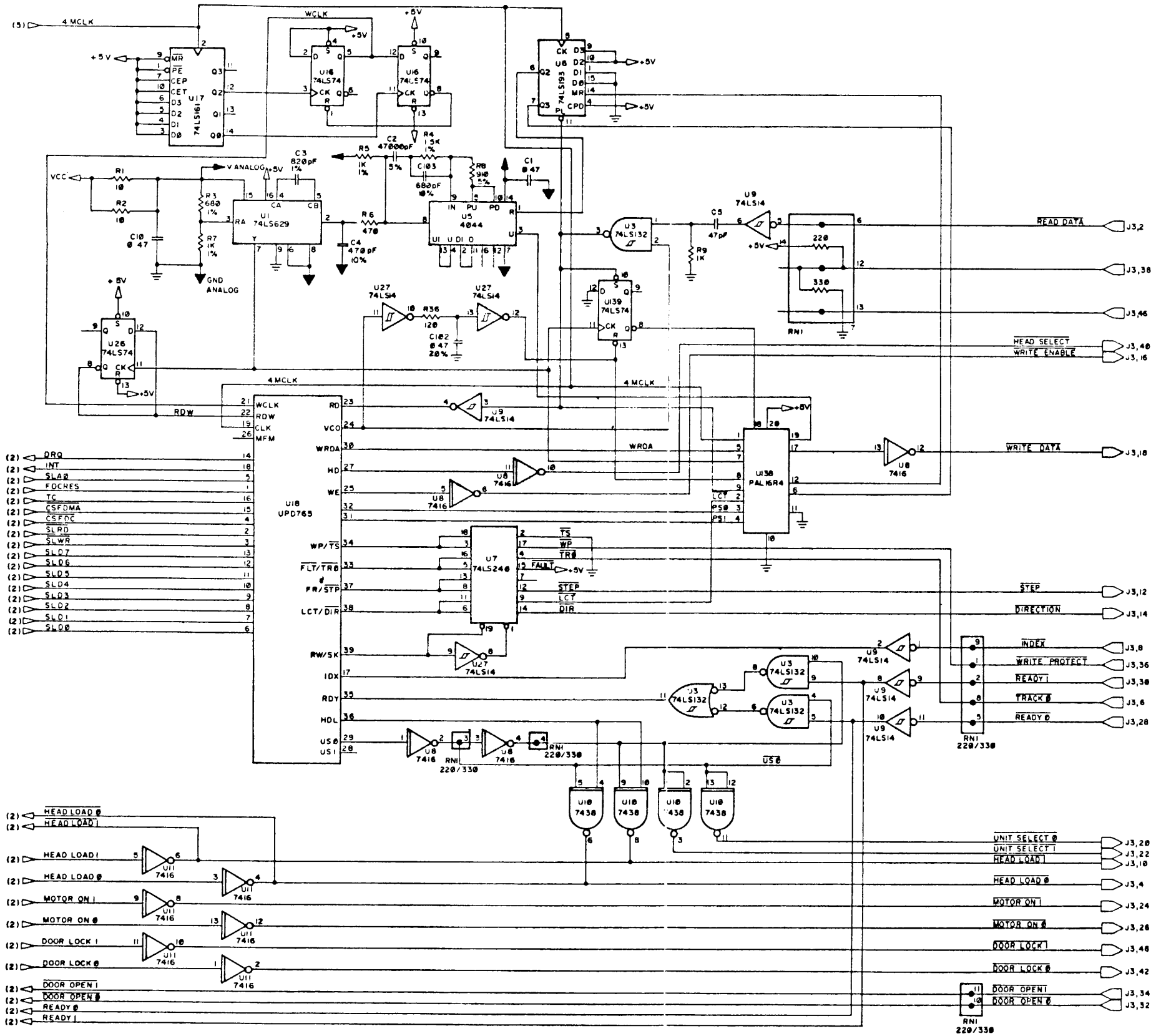


Figure 4.5
SYST. CNTR. SCHEM. (E/7) SH. 4 of 7

DRAWING NO
5107 299 91318

	DESCRIPTION	DATE
2	DRAWING CREATED UNDER ECO 182	4-9-81
3	SCHEMATIC REVISED AS PER ECO 184	11-2-81
4	SCHEMATIC REVISED AS PER ECO 350	16-4-82
5	SCHEMATIC REVISED AS PER ECO 390	20-5-82
6	PARTS LIST UPDATE ONLY AS PER ECO-348	16-07-82
6.1	SCHEMATIC REVISED AS PER ECO 490	
6.2	NEW 12NC STICKER IMPLEMENTED AS PER ECO 486	1-11-82
6.3	SCHEMATIC REVISED AS PER ECO 538	
6.4	SCHEMATIC REVISED AS PER ECO 660	
7	NEW ARTWORKS RELEASED AS PER ECO 641	
8	NOTE 3 ADDED AS PER ECO 676	

Figure 4.5
SYST. CNTR. SCHEM. (E/7) SH. 5 of 7

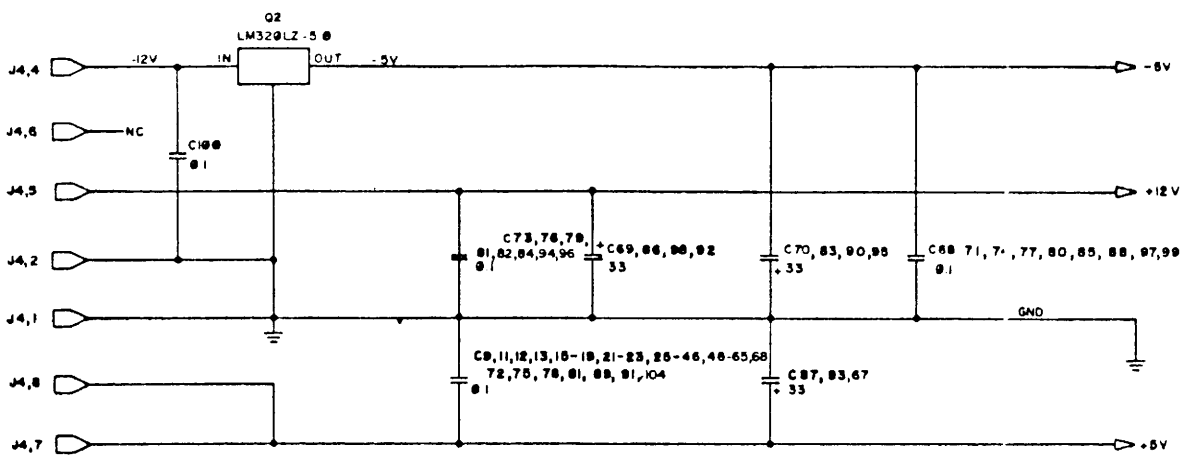
DRAWING NO
5107 299 91318

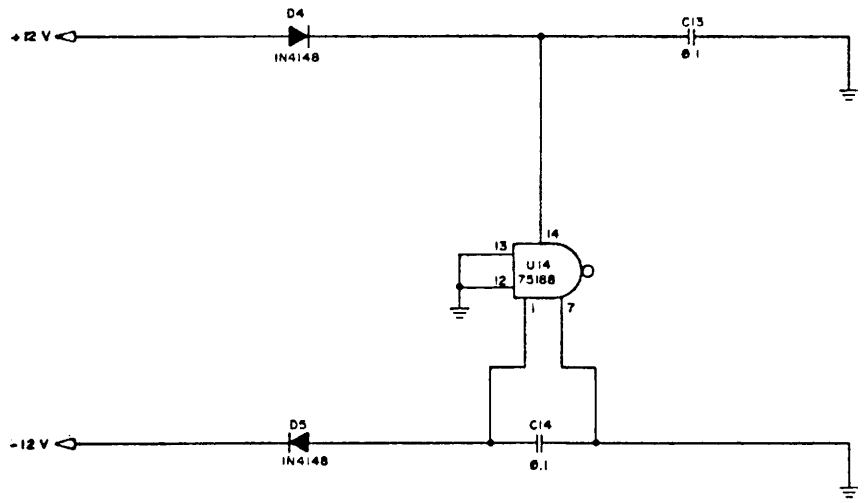
U46	N/A	5107 299 8495X	REGULAR CHAR GENERATOR
U46	EUR	5107 299 8494X	REGULAR CHAR GENERATOR
U46	N/A	5107 299 8422X	CHAR GEN WITH GREEK SYM
U46	EUR	5107 299 8421X	CHAR GEN WITH GREEK SYM
X	COUNTRY	5107 299 XXXXX	DESCRIPTION

2	DRAWING CREATED UNDER ECO [illegible]	4-9-81
3	SCHEMATIC REVISED AS PER ECO 148	11-12-81
4	SCHEMATIC REVISED AS PER ECO 350	16-4-82
5	SCHEMATIC REVISED AS PER ECO 390	20-5-82
6	PARTS LIST UPDATE ONLY AS PER ECO-348	16-07-82
6.1	SCHEMATIC REVISED AS PER ECO 490	
6.2	NEW I2NC STICKER IMPLEMENTED AS PER ECO 486	1-11-82
6.3	SCHEMATIC REVISED AS PER ECO 558	
6.4	SCHEMATIC REVISED AS PER ECO 660	
7	NEW ARTWORKS RELEASED AS PER ECO 641	
8	NOTE 3 ADDED AS PER ECO 676	

Figure 4.5
SYST. CNTR. SCHEM. (E/7) SH. 6 of 7

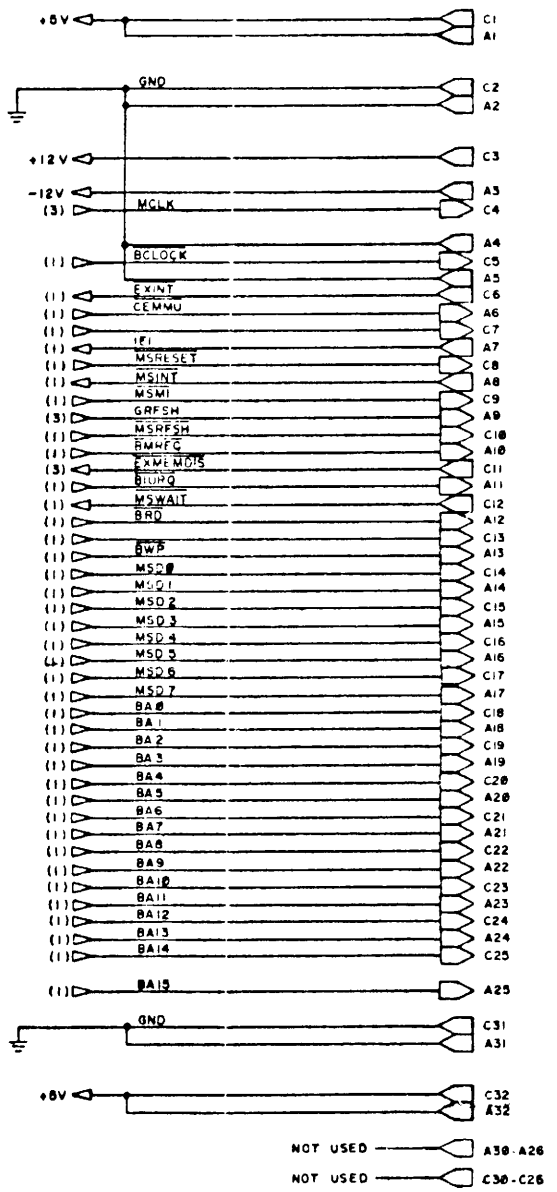
DRAWING NO
5107 299 91318





POS	DESCRIPTION	DATE
2	DRAWING CREATED UNDER ECO 182	4 [illegible] 81
3	SCHEMATIC REVISED AS PER ECO 148	11-12-81
4	SCHEMATIC REVISED AS PER ECO 350	16-4-82
5	SCHEMATIC REVISED AS PER ECO 390	20-5-82
6	PARTS LIST UPDATE ONLY AS PER ECO-348	16-07-82
6.1	SCHEMATIC REVISED AS PER ECO 490	
6.2	NEW 12NC STICKER IMPLEMENTED AS PER ECO 496	1-11-82
6.3	SCHEMATIC REVISED AS PER ECO 558	[illegible]
6.4	SCHEMATIC REVISED AS PER ECO 660	
7	NEW ARTWORKS RELEASED AS PER ECO 641	
8	NOTE 3 ADDED AS PER ECO 676	

OPTION CONNECTORS (J1 & J2 IDENTICAL)

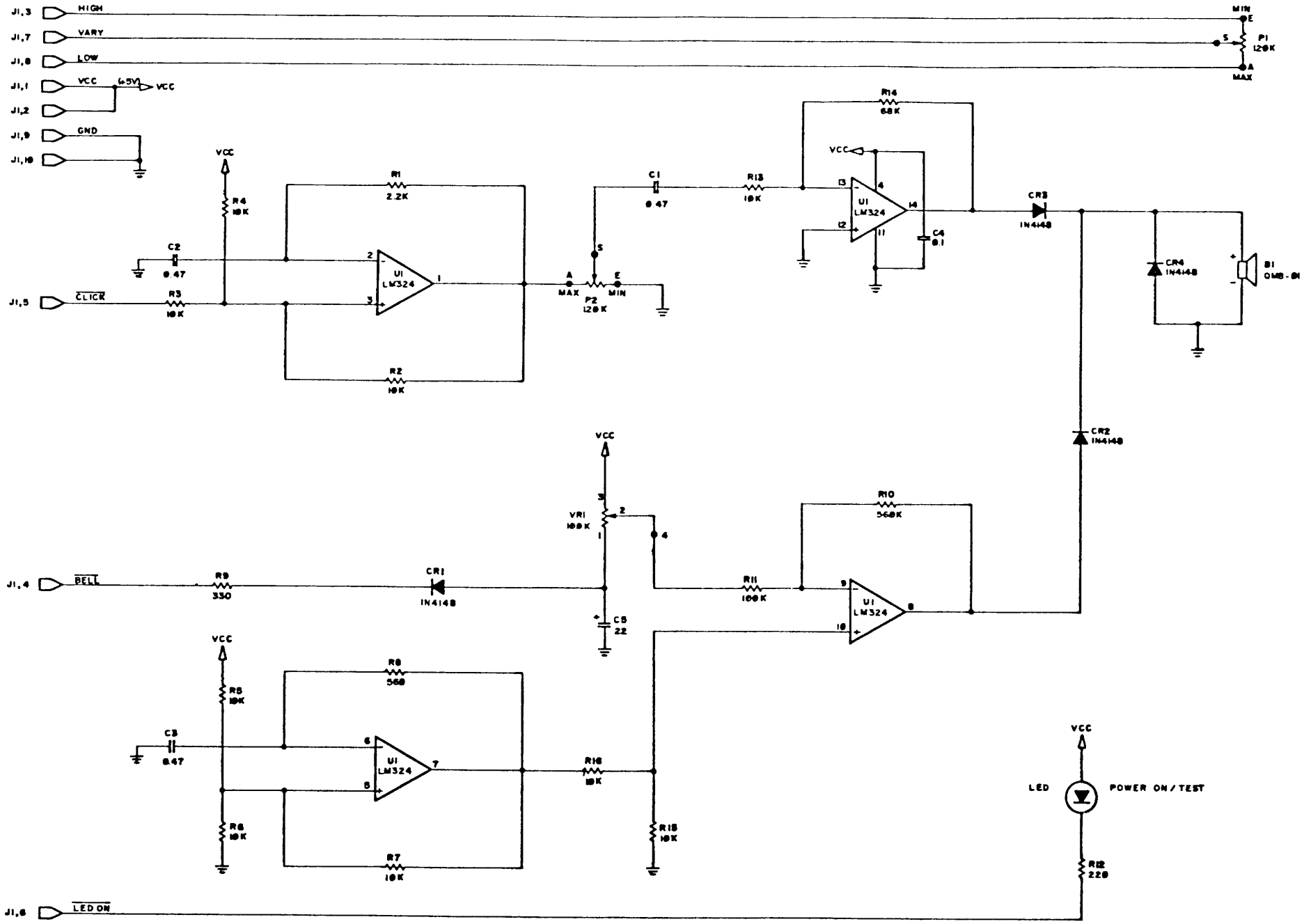


SPARE GATE TABLE

REF DESIGN	DESCRIPTION	PIN NOS	TOTAL GATES
U2	74LS00	11,12,13	3/4
U9	74LS14	12,13	5/6
U40	74LS10	3,4,5,6	2/3
RN6	68	1,2	-

Figure 4.5
SYST. CNTR. SCHEM. (E/7) SH. 7 of 7

DRAWING NO 5107 299 87723



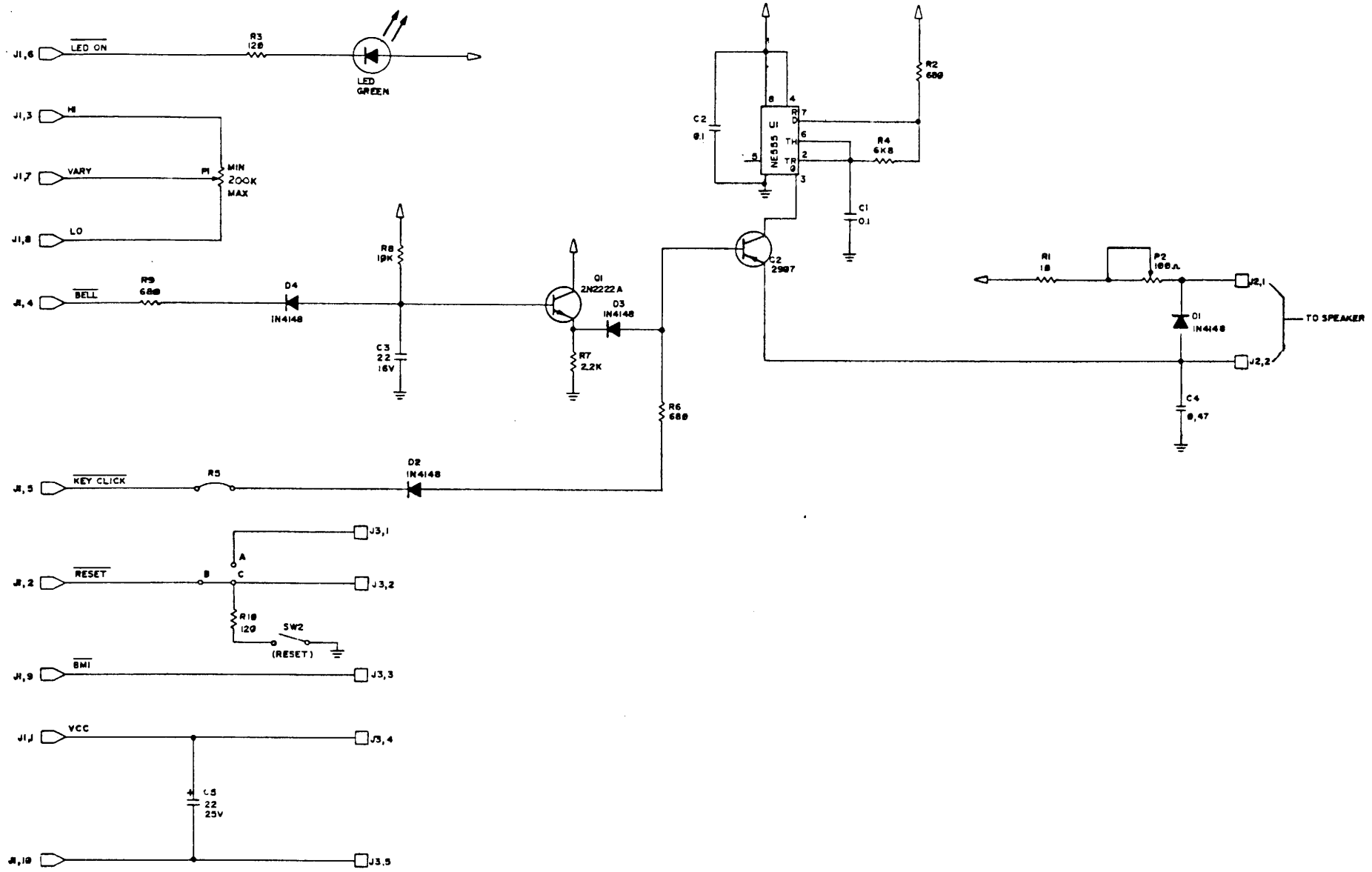
NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   RESISTOR VALUES ARE IN OHMS, ±5%, 1/4 W.
   CAPACITOR VALUES ARE IN MICROFARADS, ± 20%.

ISS	DESCRIPTION	DATE
2	SCHEMATIC REVISED AS PER ECO 242.	27-10-81
3	REF DESIGNATION CHANGED TO ALLOW FOR SWITCH RELOCATION AS PER ECO-289	27-01-82

Figure 4.6
CONTROL PANEL SCHEM. SH. 1 of 1

DRAWING NO
5107 ~~299~~ 80772



NOTES:

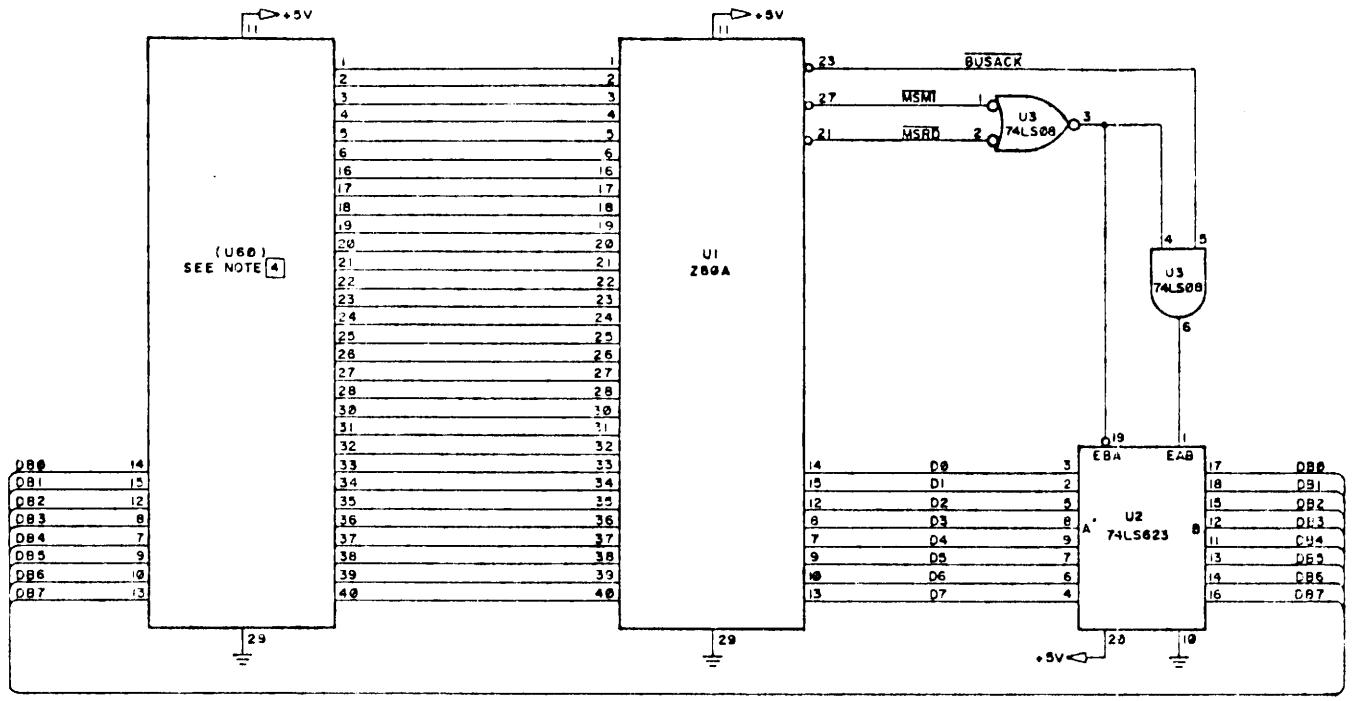
1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%. CAPACITOR VALUES ARE IN MICROFARADS, ±20%.
2. TRANSISTOR, DIODE & INTEGRATED CIRCUIT TYPE NUMBERS SHOWN ARE THOSE NORMALLY EQUIPPED. SUBSTITUTIONS OF EQUIVALENT TYPES MAY BE MADE AT TIME OF MANUFACTURE.
3. ON ALL INTEGRATED CIRCUITS THE NUMERICAL SEQUENCE IS COUNTER CLOCKWISE FROM PIN #1, (DIRECT VIEW COMPONENT SIDE), WHICH IS DESIGNATED BY A SQUARE PAD ON THE PRINTED CIRCUIT BOARD.

REVISIONS STATUS			
ISSUE	Description	APD'D BY DATE	REL'D BY DATE
1	FRN 075		12-11-82
2	R4 WAS 8.2K, P2 WAS 120K AS PER ECO 606		[illegible]

LAST REFERENCE DESIGNATION USED		
U1	J5	D3
Q2	R10	C5
SW2	P2	
REF. DESIGNATION NOT USED		

Figure 4.6
CONTROL PANEL SCHEM. SH. 1 of 1

DRAWING N°
5107 265 08811



NOTES:

1. UNLESS OTHERWISE SPECIFIED
   RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%
   CAPACITOR VALUES ARE IN MICROFARADS, ±20%.
2. TRANSISTOR, DIODE & INTEGRATED CIRCUIT TYPE NUMBERS SHOWN ARE THOSE NORMALLY EQUIPPED. SUBSTITUTIONS OF EQUIVALENT TYPES MAY BE MADE AT TIME OF MANUFACTURE
3. ON ALL INTEGRATED CIRCUITS THE NUMERICAL SEQUENCE IS COUNTER CLOCKWISE FROM PIN #1, (DIRECT VIEW COMPONENT SIDE), WHICH IS DESIGNATED BY A SQUARE PAD ON THE PRINTED CIRCUIT BOARD.

[4] THIS PCB REPLACES 'U60' ON "ASSY, PCB, SWIFT CONTROLLER", 5107 299 9131.

SPARE GATE TABLE			
REF DESIGN	DESCRIPTION	PIN NOS	TOTAL GATES
U3	74LS08	8,9,10;11,12,13	2/4

LAST REFERENCE DESIGNATION USED		
U3		
REF. DESIGNATION NOT USED		

Figure 4.7
CPU PIGGY BACK SCHEM. SH. 1 of 1

APPENDIX A: SERIAL-TO-PARALLEL CONVERTER

This appendix gives you information about the serial-to-parallel converter. Although it gives you detailed information, some important points are not mentioned:

These points are:

- The serial-to-parallel converter is shipped together with a 220V power supply for the Qume printer.

- At present, the power for the converter (+5V), is coming from the Qume printer. A connector simular to the connector on the Qume sheetfeeder has to be used.
  A definitive solution for a Qume printer with sheetfeeder and a serial-to parallel converter is not yet available.

If the serial-to-parallel converter is installed, in the profile has to be selected:"Qume".

- The internal printer cable in the console has to be connected to connector J7B of the System Controller PCB.

NOTE: In early versions of the converter, there are two wires instead of a connector for taking the supply from the Qume. These wires have to be connected to the Qume Power Supply.

A.1 INTRODUCTION

The Serial-to-Parallel Converter, shown in Figure A-1, interfaces an M3003 Word Processor console to a Qume printer. The main functions performed by the unit are to convert the serial data and control signal outputs of the console into the parallel format required by the Qume printer, to monitor the printer status signals, and to control the printer. The converter is a self-contained microcomputer-controlled unit which receives dc power (+5V) from the Qume printer, and which has baud rate select terminals that are set for the serial transmission rate used.

The converter is equipped with two captive screws, and J1 connects to the data interface connector at the rear of the Qume printer. Connector J3 connects to the cable to the Word Processor console, and P1 is for the power cable which connects to the adapter on the printer power connector. The converter measures .85 inches (123.2 mm) wide, 3.24 inches (82.2 mm) long, and 0.81 inch (20.6 mm) deep, and the power cable is 23.6 inches (600 mm) long.

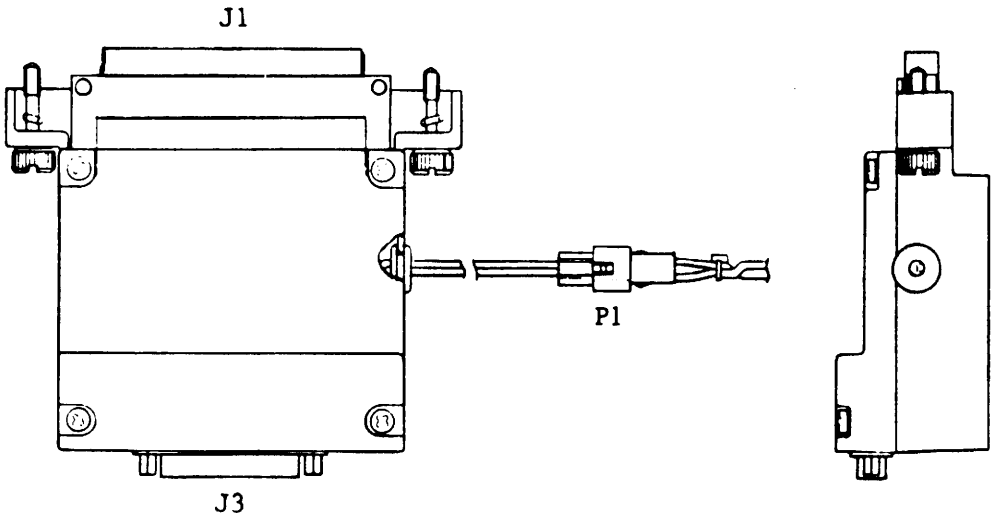


Figure A-1 SERIAL-TO-PARALLEL CONVERTER

A.2 THEORY OF OPERATION (Figure A-2)

All operations of the Converter are controlled by the MK38P73 microcomputer and its associated piggyback EPROM, which contains the program. Following is a brief description of the operation of the Converter. For a more detailed description of the microcomputer refer to paragraph A.2.1. Figure A-5 is a simplified flowchart of the software. Note that the flowchart does not show all operations, but illustrates the sequence of events.

The serial input data from the Word Processor console is applied to the serial input port of the microcomputer via J3 and the differential RS-422 line receiver of U5-3. The line receiver, which has a tri-state output, is held enabled by U5-4 being connected to +5V (the output at U5-3 is never put into the high impedance state). The serial data from the serial output port of the microcomputer and the DTR (data terminal ready) signal from P1-7 are routed to the Word Processor console via the RS-422 line drivers of U6, which have tri-state outputs. As the control input at U6-4 is held high by +5V, via RN2, the line driver outputs are held enabled. Balanced data outputs are provided at U6-5 and U6-6.

The microcomputer parallel ports connect to the Qume printer via J1, as follows:

- Port P0 is an input port which receives status signals from the printer.

- Port P1-6 provides the Printer Select signal to the printer, via line driver U6-11.

- Port P5 and half of port P4 provide the 13 data outputs to the printer, via the drivers.

- Three outputs of Port P4 and the strobe output of U4-7 provide the BCD input to decoder U3, which provides control signals to the printer, as shown below. Table A-1 defines the output signals.

INPUTS				OUTPUTS					
A	B	C	D	1	2	3	4	5	6
L	L	L	L	L	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H
L	H	L	L	H	H	L	H	H	H
H	H	L	L	H	H	H	L	H	H
L	L	H	L	H	H	H	H	L	H
H	L	H	L	H	H	H	H	H	L

Baud rate selection for the transmission rate is selected at strapping terminals W1 and W2, which connect to two inputs of port 1. Selections are:

BAUD RATE	W1	W2
1200	In	In
2400	Out	In
4800	In	Out
9600	Out	Out

The Reset input at U4-39 is used for the power-on start-up sequence. When power is first turned on the reset input is low and the microcomputer is reset. When C1 becomes charged via RN1-10 (after approximately 0.1 sec), the microcomputer begins program execution at location H000.

Crystal Y1 provides a 3.6864 MHz time base for the microcomputer, and the Test and Interrupt inputs are not used.

The +5V and Ground terminals connect, via the power cable, to the adapter on the Qume printer power connector.

A.2.1 **Microcomputer Description (Figure A-3)**

Microcomputer U4 is a complete 8-bit microcomputer with a 2K x 8 piggyback EPROM. The following is a brief description of the operation of the microcomputer. For a detailed description refer to the MOSTEK Data Book. The EPROM listing is provided in Table A.2.

The microcomputer has a 2048-byte piggyback EPROM, 64 bytes of scratchpad RAM, a programmable timer, a baud rate generator, 4 8-bit input/output ports, and serial input and output ports. An external 3.6864 MHz crystal provides a time base to control internal operations.

The memory address registers (program counter, stack pointer, data counter, auxiliary data counter) are used for addressing. When a memory access is required, the appropriate address register is gated onto the memory address bus and the memory output is gated onto the main data bus.

The instruction register (IR) receives the OP-code of the instruction to be executed via the main data bus. The main control logic decodes the instruction and provides the necessary gating signals to the rest of the circuitry. The indirect scratchpad RAM is used to address the 64 bytes of scratchpad RAM, which is used for temporary storage.

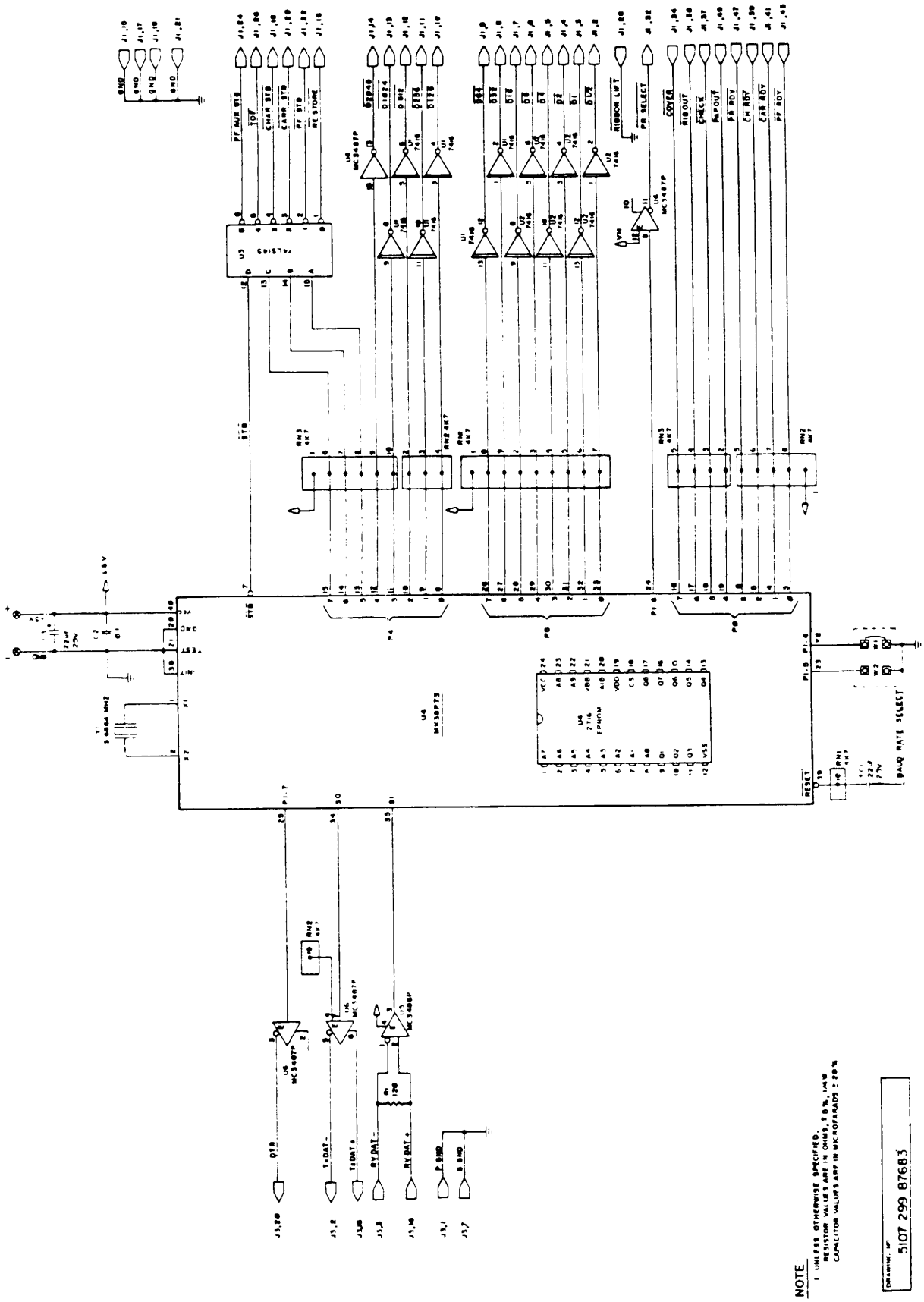


Figure A-2 SERIAL-TO-PARALLEL CONVERTER SCHEMATIC

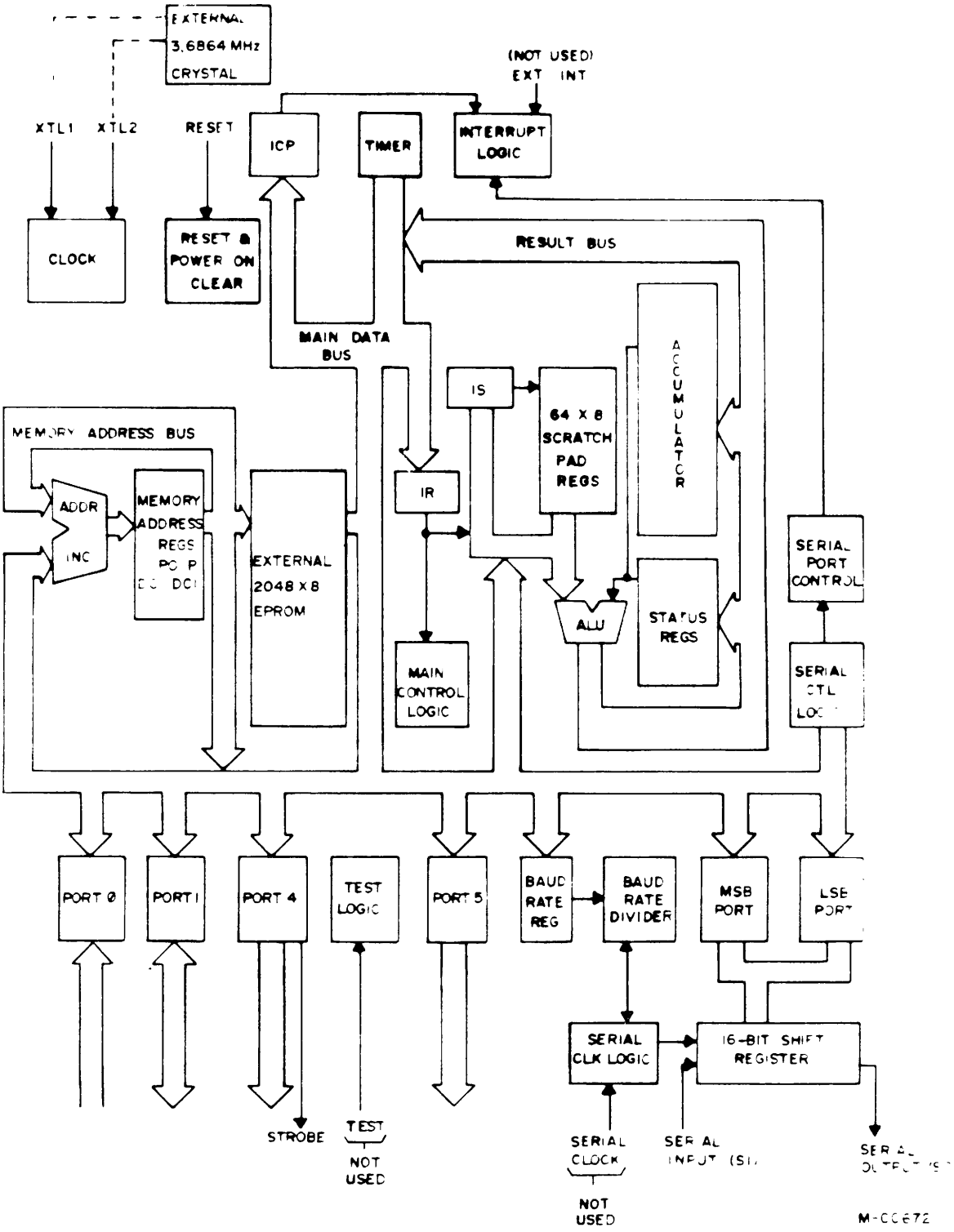


Figure A-3 MICROCOMPUTER BLOCK DIAGRAM

When the ALU receives commands from the main control logic it performs the required mathematical or logical operation on the data received on the two input buses and provides the result on the result bus. The status of the result (carry, overflow, etc.), is applied to the status registers. The status registers also hold other status flags, such as interrupt control, I/O ports control, etc. The accumulator is the main register for data manipulation, with the result of ALU operations stored there.

The timer is an 8-bit down counter which is a software programmable counter which can be used as an internal timer, pulse width timer or event counter.

There are 4 8-bit bidirectional ports. Port 0 is used as an input port, and is used to monitor printer status signals (see Table A.1). Ports 5 and 4 are output ports which provide the parallel data lines to the printer. Part of port 4, in conjunction with the strobe output at U4-7, provide the BCD input to decoder U3 which provides control signals to the printer. The strobe output is normally high and provides a single low pulse after valid data is present on the port 4 outputs during an output instruction. Table A.1 defines the printer signals. Port 1 is used as follows:

- P1-6 is an output, providing the Printer Select control signal.

- P1-7 is an output, providing the Data Terminal Ready (DTR) control signal to the Word Processor console.

- P1-4 and P1-5 are inputs, and are used for reading the setting of the baud rate select straps.

There are two serial ports, S1 and S0, which are the serial data links from and to the Word Processor. The serial port control logic controls the two ports to the 16-bit shift register. Each of the two ports is eight bits wide and has holding registers for data to/from the shift register (each port has a receive and transmit holding register). Data transfers between the holding registers and the shift register are performed at end-of-word time, under software control. Data transfer on the serial links consists of blocks of data with eight bits per character, two stop bits, with no parity (Figure A-4).

Data on the receive link from the console is conditioned by line receiver U5-3 before being applied to the microcomputer, and data from the microcomputer is conditioned by line transmitter U6 before being applied to the transmit link to the console.

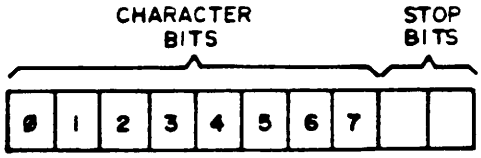


Figure A-4 SERIAL DATA LINKS FORMAT

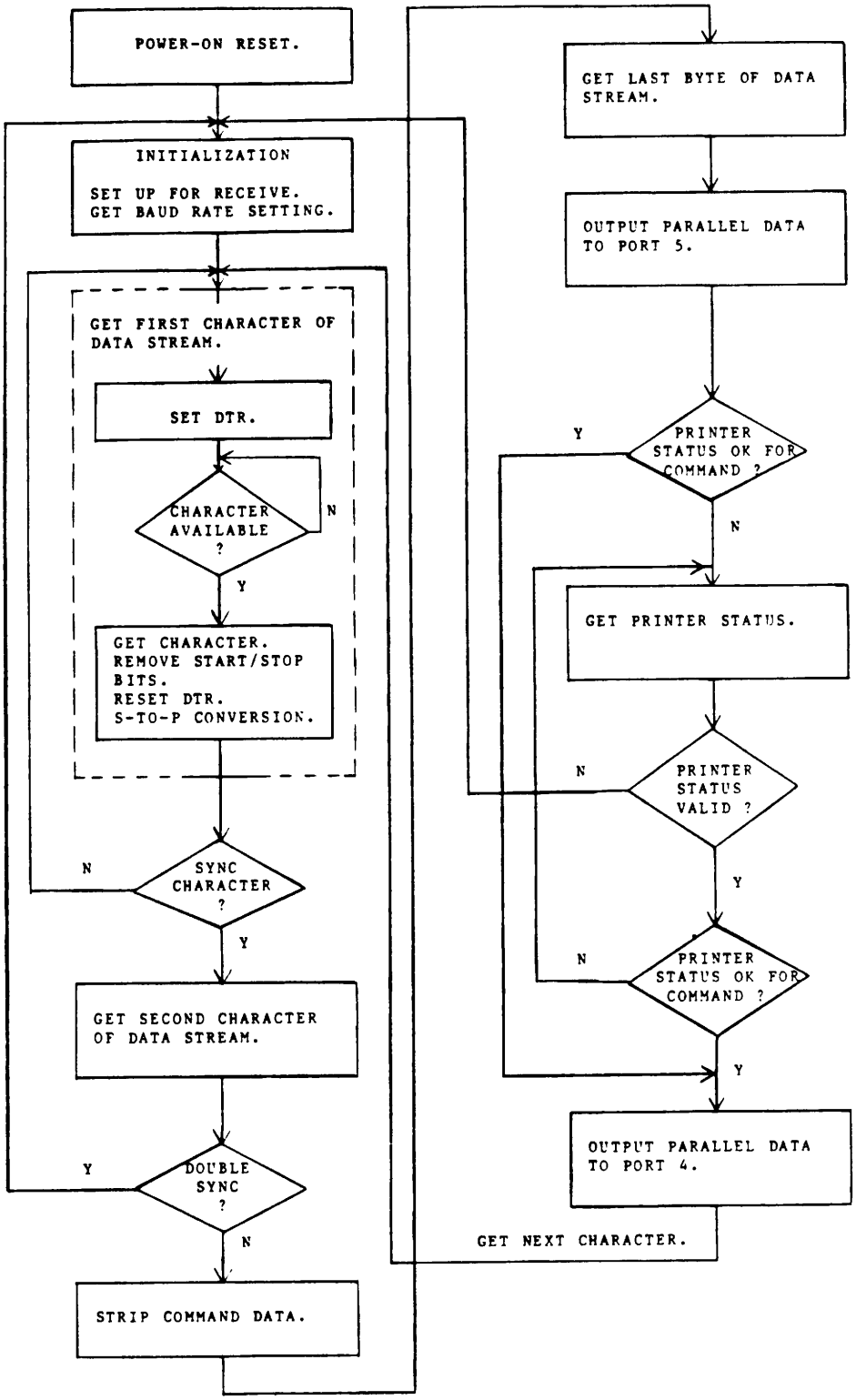


Figure A-5 SOFTWARE FLOWCHART

Table A.1 PRINTER LINES

SIGNAL	INPUT/ OUTPUT	DESCRIPTION
Paper Feed Auxiliary Strobe PF AUX STB, L	O	Normally not used by Qume printer.
Top of Form TOF, L	O	Advances paper to the beginning of the next form.
Character Strobe CHAR STB, L	O	Indicates valid character data is on the data lines.
Carriage Strobe CARR STB, L	O	Indicates data lines contain valid carriage movement data.
Paper Feed Strobe PF STB, L	O	Indicates data lines contain valid paper movement data.
RESTORE, L	O	Causes the printer to perform its restore (initialization) sequence.
13 Data Lines	O	Contains binary coded information representing an ASCII character, a carriage movement command, a paper feed command, or a top of form command.
RIBBON LIFT, L	O	Raises ribbon to the printing position.
Printer Select PR SELECT, L	O	Enables the printer.
COVER, L	I	Printer top cover is in place.
Ribbon Out RIBOUT, L	I	Printer is out of ribbon.
CHECK, L	I	A printer malfunction has occurred.
Paper Out PAOUT, L	I	Printer is out of paper.
Printer Ready PR RDY, L	I	Printer is ready to accept data and control inputs.
Character Ready CH RDY, L	I	Printer is ready to accept a character.
Carriage Ready CAR RDY, L	I	Printer is reay to accept a carriage movement command.
Paper Feed Ready PF RDY, L	I	Printer is ready to accept a paper feed command.

L = active low.

Table A.2 EPROM LISTING

ADDRESS	CODE	ADDRESS	CODE	ADDRESS	CODE	ADDRESS	CODE
0000	20B0	0051	50	00A0	70	00F1	AF
0002	BD	0052	2800FC	00A1	E1	00F2	14
0003	AE	0055	70	00A2	84BC	00F3	12
0004	70	0056	E1	00A4	2000	00F4	12
0005	B0	0057	84BC	00A6	B1	00F5	50
0006	2080	0059	2000	00A7	42	00F6	AE
0008	B1	005B	B1	00A8	211F	00F7	13
0009	A1	005C	42	00AA	54	00F8	13
000A	18	005D	18	00AB	E0	00F9	E0
000B	14	005E	B5	00AC	9404	00FA	52
000C	2103	005F	2080	00AE	290000	00FB	1C
000E	2A0123					00FC	20B0
		0061	B1	00B1	14	00FE	BD
0011	8E	0062	AD	00B2	12	00FF	40
0012	16	0063	2180	00B3	52		
0013	BC	0065	8406	00B4	2A0113	0100	C0
0014	2080	0067	2800F1	00B7	8E	0101	BF
0016	B1	006A	9039	00B8	16	0102	76
0017	AD	006C	A0	00B9	E4	0103	19
0018	2180	006D	21F8	00BA	54	0104	BE
001A	8406	006F	84EF	00BB	2A011B	0105	AE
001C	2800F1			00BE	42	0106	20A2
001F	9039	0071	56	00BF	8E	0108	BD
		0072	2000			0109	AD
0021	A0	0074	B1	00C0	16	010A	2140
0022	21F8	0075	70	00C1	57	010C	84FC
0024	84EF	0076	50	00C2	A0	010E	20B0
0026	56	0077	51	00C3	21F8		
0027	2000	0078	30	00C5	841A	0110	BD
0029	B1	0079	9405	00C7	50	0111	AE
002A	70	007B	31	00C8	56	0112	1C
002B	50	007C	70	00C9	2800FC	0113	C0
002C	51	007D	910A	00CC	A0	0114	60
002D	30	007F	AD	00CD	21F8	0115	40
002E	9405			00CF	94FC	0116	A0
		0080	2180			0117	20
0030	31	0082	84F5	00D1	50	0118	80
0031	70	0084	2800F1	00D2	30	0119	C0
0032	910A	0087	71	00D3	94FE	011A	00
0034	AD	0088	51	00D5	A0	011B	00
0035	2180	0089	46	00D6	21F8	011C	04
0037	84F5	008A	50	00D8	94F3	011D	02
0039	2800F1	008B	2800FC	00DA	50	011E	01
003C	71	008E	A0	00DB	2800FC	011F	01
003D	51	008F	21F8	00DE	90E3		
003E	46					0120	07
003F	50	0091	94FC	00E0	A0	0121	00
		0093	50	00E1	F7	0122	07
0040	2800FC	0094	30	00E2	8406	0123	08
0043	A0	0095	94FE	00E4	2000	0124	09
0044	21F8	0097	A0	00E6	B1	0125	0A
0046	94FC	0098	21F8	00E7	90DA	0126	0B
0048	50	009A	94F3	00E9	2080		
0049	30	009C	50	00EB	B1		
004A	94FE	009D	2800FC	00EC	18		
004C	A0			00ED	B4		
004D	21F8			00EE	290014		
004F	94F3						

A.3 INSTALLATION

The Serial-to-Parallel Converter Module connects directly to the rear of the Qume printer, to the data input/output connector.

- Secure the Converter to the printer using the two captive screws on the Converter.

- Connect the serial data cable from the Word Processor console to J3 of the Converter.

- Connect the power cable from the Converter to the adapter of the printer power connector (the Converter receives +5V from the printer).

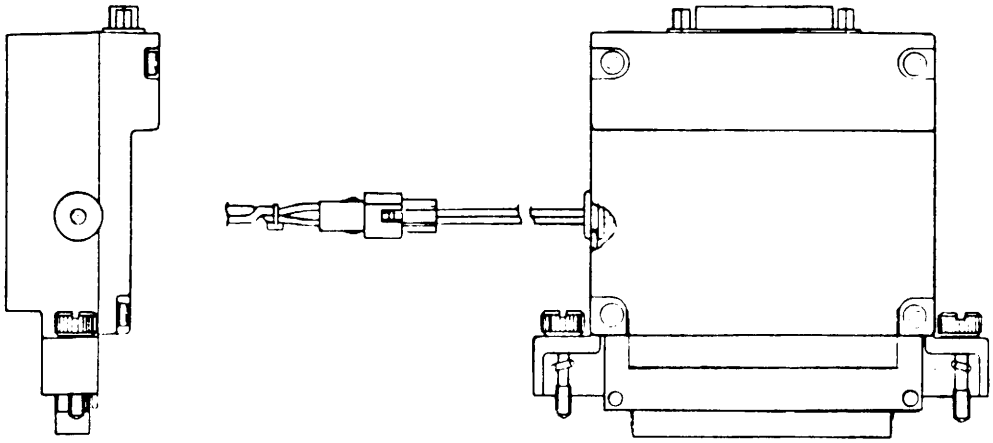
NOTE

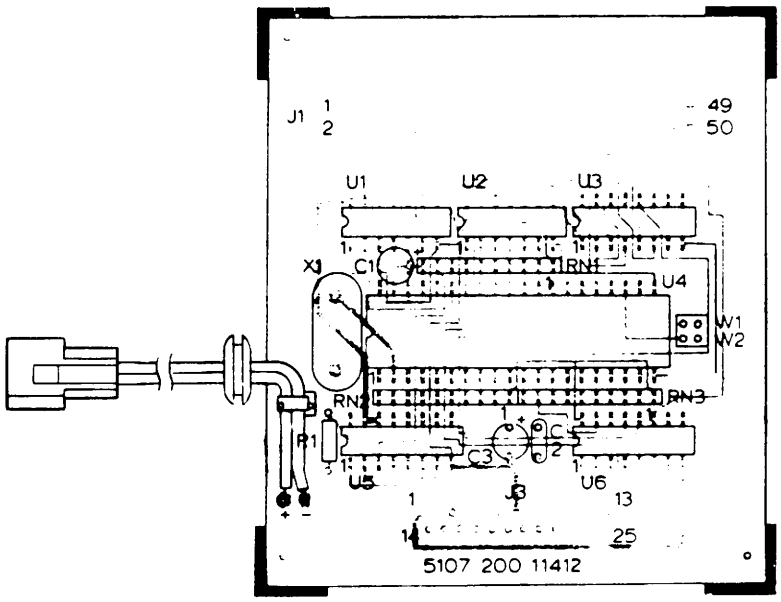
The Converter PCB is equipped with baud rate select terminals (W1 and W2) for selecting the transmission rate. Strapping options are:

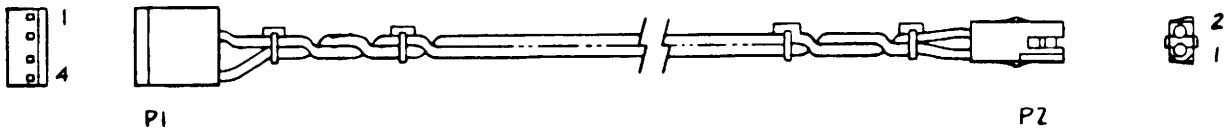
BAUD RATE	W1	W2
1200	In	In
2400	Out	In
4800	In	Out
9600	Out	Out

A.4 REPLACEABLE PARTS

Refer to Figure A-6 and Table A.3.







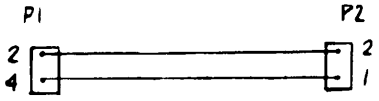


Figure A-6 SERIAL-TO-PARALLEL CONVERTER REPLACEABLE PARTS

Table A.3 SERIAL-TO-PARALLEL CONVERTER REPLACEABLE PARTS

ITEM	DESCRIPTION	12NC PART NUMBER
	Serial-to-Parallel Converter Module (complete)	5107 299 85521
	PCB (complete)	5107 299 87682
	Cover	5107 200 15591
	Base	5107 200 15601
	Captive Screw	5107 025 01501
	Screw, BHMS, M3x10	2522 004 02026
	Screw, BHMS, M3x18	2522 004 02029
	Washer, M3 (for M3x10 screw)	2522 600 16017
	O-Ring Seal (for captive screw)	5107 025 01491
	Grommet	5107 259 89161
	Jackpost Assembly (for J3)	5107 259 91481
C1	Capacitor, Tantalum, 22uF, 25V, ±20%	5107 259 95471
C2	Capacitor, Tantalum, 1uF, 50V, ±20%	5107 259 95402
C3	Capacitor, Tantalum, 22uF, 25V, ±20%	5107 259 95471
J1	Connector, 50-position	5107 259 90931
J3	Connector, 25-position	2422 025 01354
R1	Resistor, 120 ohm, 1/4W, ±5%	5107 259 98411
RN1	Resistor Network, 4K7	5107 259 97061
RN2	Resistor Network, 4K7	5107 259 97061
RN3	Resistor Network, 4K7	5107 259 97061
U1	IC, 7416	5107 259 93231
U2	IC, 7416	5107 259 93231
U3	IC, 74LS145	5107 259 92881
U4	IC, MK38P73	5107 259 92151
U5	IC, MC3486P	5107 259 94221
U6	IC, MC3487P	5107 259 94211
U7	IC, EPROM, 2716	5107 259 93271
W1	Jumper	5107 024 00651
W2	Jumper	5107 024 00651
XU4	IC Socket, 40-pin (for U4)	5107 259 99841
Y1	Crystal, 3.6864 MHz	5107 259 89871
	Cable Assembly (complete)	5107 299 81101
P1	Connector, 4-position	2422 025 01788
	Pin for P1	2422 034 11688
	Terminal Socket for P1	2422 034 01385
P2	Connector, 2-position	5107 259 86331
	Tie-wrap	5107 259 92101

APPENDIX B: SHARED PRINTER CONTROLLER

The following points are not mentioned in the rest of the manual:

- The supply voltages for the shared printer controller is coming from connector CN0-14 of the TEC printer. This connector must have -15V on pin 7. In some old TEC printers, this point is connected to an other, not used, line. If shared printer controller is used for these printers, the following modifications have to be done:
  - Cut the track to connector CN0-14 pin 7
  - Install a wire between -15V and connector CN0-14 pin 7 on the back of the mother board.

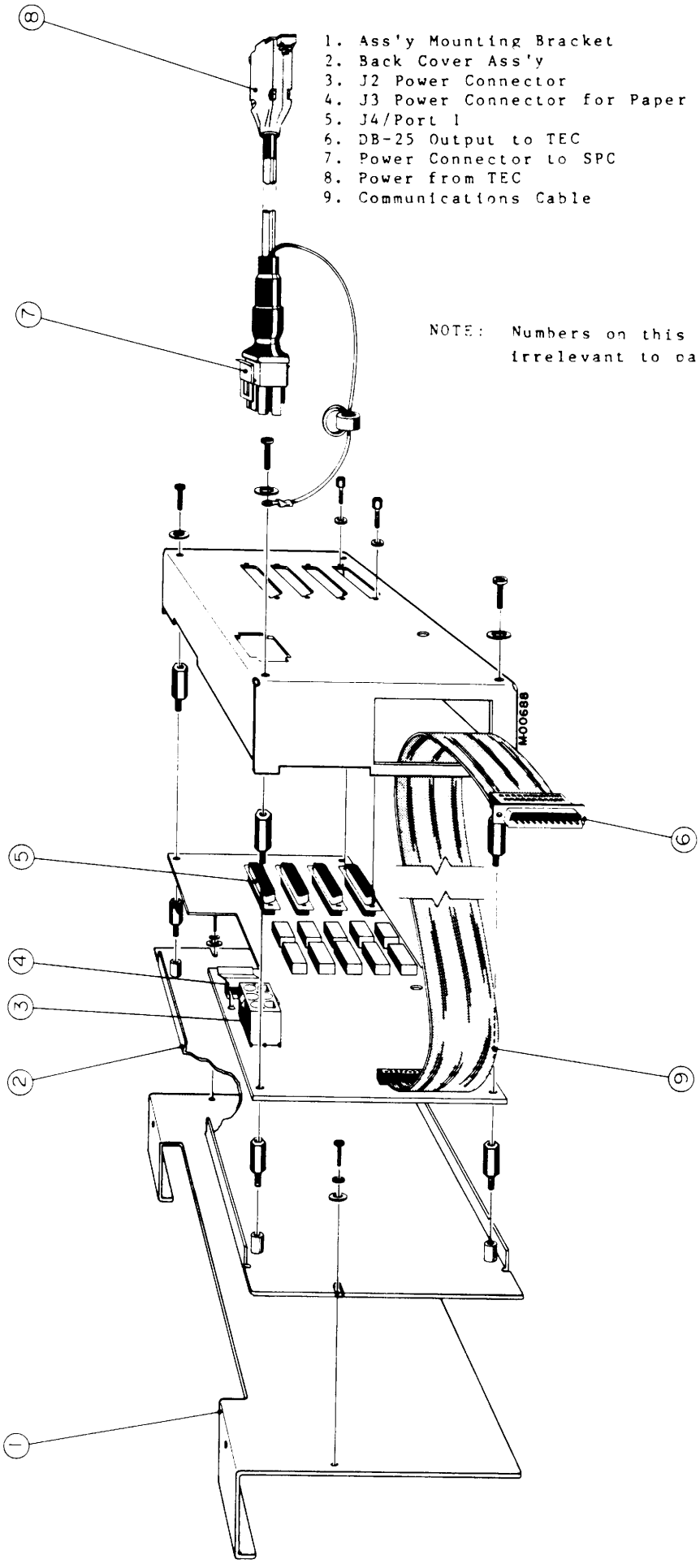
- Use connector J7A on the System Controller PCB.

- Select always: FILE OPTIONS SHARED PRINTER

- If for printing the option auto is not selected, the printing has to be started with the start/stop key.

- There is, at present, no definitive solution for a TEC printer together with sheetfeeder and shared printer controller (for connecting both power cables).

- For cable layouts see B24.


1. Ass'y Mounting Bracket
2. Back Cover Ass'y
3. J2 Power Connector
4. J3 Power Connector for Paper Processor
5. J4/Port 1
6. DB-25 Output to TEC
7. Power Connector to SPC
8. Power from TEC
9. Communications Cable
NOTE: Numbers on this page irrelevant to parts list.
M00688

B.1 INTRODUCTION

The Shared Printer Controller (SPC) allows four M3004 Systems to share a common TEC printer. The SPC has no intelligence of its own and is configured in a simple 4x1 arrangement. The SPC consists mainly of CMOS analog switches and some associated logic gates. It has no power supply so must receive power via the printer.

In the situation where requests do not happen concurrently, printing is executed as if each M3004 System had complete printer control. When arbitration is required, one M3004 System will have control while the others will have to time-out.

B.2 HARDWARE INTERFACE

Communication is done via one output port and four input ports. Inputs consist of four DB25 connections; for pin assignments see Table 1.1. The four input ports receive data from the M3004 Systems which then toggle for control of the printer. The four ports are in sequence from one to four (J4 being port 1, J5 being Port 2 and so on). When connecting the M3004 systems to the SPC, Port 1 must be connected first, then Port 2, Port 3 and finally Port 4. The cables used for transmission of data to the input ports are identical to regular printer cables; they are RS-232 and RS-422 compatible.

When one of the M3004 systems has taken control of the printer, commands are transmitted from the SPC via the output port. The output consists of one DB25 connection; pin assignments can be seen in Table B.2.

Table B.1 INPUT PORTS PIN ASSIGNMENTS

PIN	NAME	I/O
1	Prot Gnd	
2	TxD-	Output
3	RxD-	Input
6	REQ	Input
7	Gnd	
15	TxD	Output
16	RxD	Input
20	DTR	Output

TABLE B.2 OUTPUT PORT PIN ASSIGNMENTS

PIN	NAME	I/O
1	Prot Gnd	
2	RxD-	Input
3	TxD-	Output
7	Gnd	
15	RxD+	Input
16	TxD+	Output
20	DTR	Input

B.3 SOFTWARE INTERFACE

Since the SPC has no intelligence of its own, the four M3004 systems supply the intelligence to control the SPC. During initial power-up, a M3004 system must disable Data Terminal Ready (DTR) on the Printer Port (tied to REQ). For a M3004 system to access the the SPC, the four systems must toggle for control (see Table B.3).

Table B.3 SPC OPERATION

SWIFT 1 DTRB	SWIFT 2 DTRB	SWIFT 3 DTRB	SWIFT 4 DTRB	RESULT
0	0	0	0	The Printer line channel is toggled
0	0	0	1	The Printer is enabled for SW4
0	0	1	0	The Printer is enabled for SW3
0	1	0	0	The Printer is enabled for SW2
1	0	0	0	The Printer is enabled for SW1
1	1	0	0	Printer line status remains unchanged
0	1	1	0	Printer line status remains unchanged
1	1	1	0	Printer line status remains unchanged
1	0	1	0	Printer line status remains unchanged
1	1	1	1	Printer line status remains unchanged

0=inactive

1=active

From Table B.3 it can be seen that if all four M3004 Systems request the printer, the channel remains enabled and does not change state. The Systems will time-out if their channels are not enabled. In other words, if the Printer requests are not acknowledged the M3004 Systems will inform the users that the Printer is in use and to try again later. The M3004 request is acknowledged when the DTR (Printer Side) is active.

In the Shared Printer configuration, the printer driver performs a Printer Request and responds to a Printer Busy signal by timing-out. The M3004 makes a request for the printer by enabling DTR on Channel B of the DART. When the SPC enables the Clear to Send (CTS) (DTR printer side) line an acknowledgement is made. If the printer is busy the CTS channel will remain off, as if no printer was connected. Following this, the M3004 must time-out if CTS is not active by the time it normally takes the printer to empty some of its buffer (10 secs). The TxD line(s) from the printer are connected to all M3004 Systems. Receive character interrupts from the DART are only serviced by the System which has control of the print channel.

NOTE: The DTR CHANNEL B must be active for the entire print cycle. After printing the M3004 must disable its DTR line.

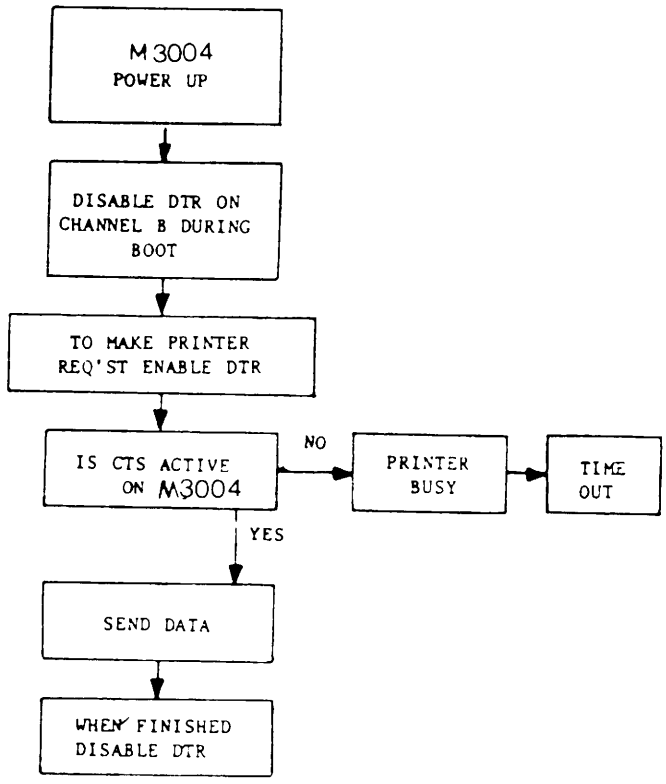


Figure B-2 SPC FLOWCHART OF OPERATION

B.4 ELECTRICAL INTERFACE

Power for the SPC is available from a number of sources depending on the user's facilities. When a TEC printer is being used, power will be tapped from a special connection located beside the DB25 connector. If a Paper Processor is used, then the SPC will be powered through the same connector as that used by the Paper Processor. The SPC will not affect operation of the Paper Processor. For a more indepth look at the electrical interfacing used; see Section on Installation.

B.5 MECHANICAL INTERFACE

The SPC is mounted in a small enclosure and placed at the rear of the printer via assembly brackets. If a Paper Processor is used, the SPC in its enclosure, will rest on the Paper Processor's controller housing. Indepth information on the mechanical interface of the SPC is contained in the Section on Installation.

B.6 TECHNICAL DATA

Physical

Length:	246.1mm/9.65"
Height:	127mm/5"

Electrical

All electronics are on a simple P.C.B. There is no power supply. Power will come from the TEC.

Voltage Requirements:	+15V (@ 30ma)
	-15V (@ 30ma)
	+5V (@ 1ma)
Power Consumption:	Less than 450mWatts

Environmental

Temperature:

Operating:	0 to 50°C
Non-operating:	-40 to 70°C

Humidity:

Operating:	20 to 80% R.H.
Non-operating:	10 to 90% R.H.

B.7.1 **INSTALLATION**

B.7.2 PREPARATION OF TEC PRINTER

Power for the Shared Printer Controller is taken from the TEC Printer via a DB-9 connector which will be located on the rear of the unit (see Figure B-7).

When preparing the TEC for the transfer of power, a modification must be made. A special cable assembly included in the SPC package must be installed. The cable has a DB-9 (with mounting hardware) on one end and on the other a female pin connector (see Figure B-3). To install the cable, the cover of the printer must first be removed (see section on TEC Cover Removal).

When the cover has been removed the installation of the cable can take place. The cable is connected to connector CN0-14 on the mother board of the printer by a simple plug in arrangement. This connector supplies the +15V, -15V and +5V needed for the SPC.

The DB-9 connector is mounted when the cover of the TEC is still off. A mounting bracket located next to the DB-25 connector (see Figure B-5) is provided. Before installing the cover back on the printer a plastic tab located next to the DB-25 connector must be broken off to allow access to the DB-9 (see Figure B-5).

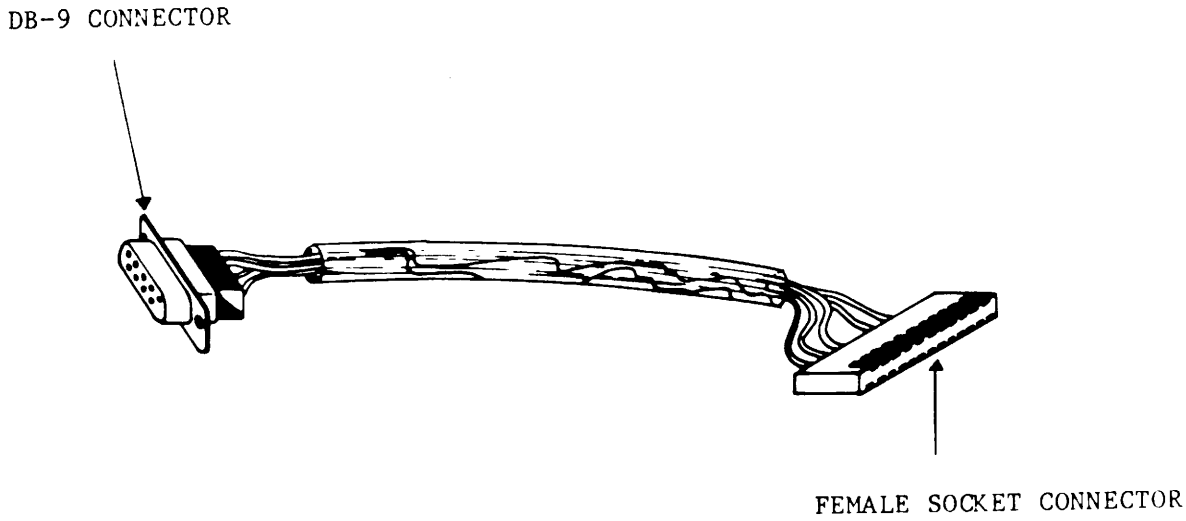


Figure B-3 TEC INTERNAL POWER CABLE ASSEMBLY

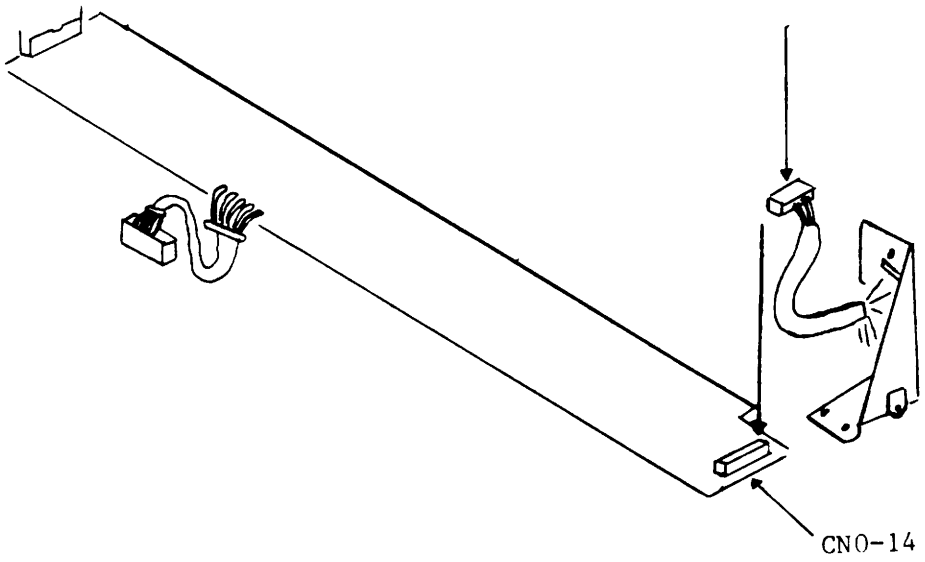


Figure B-4 TEC MOTHER BOARD

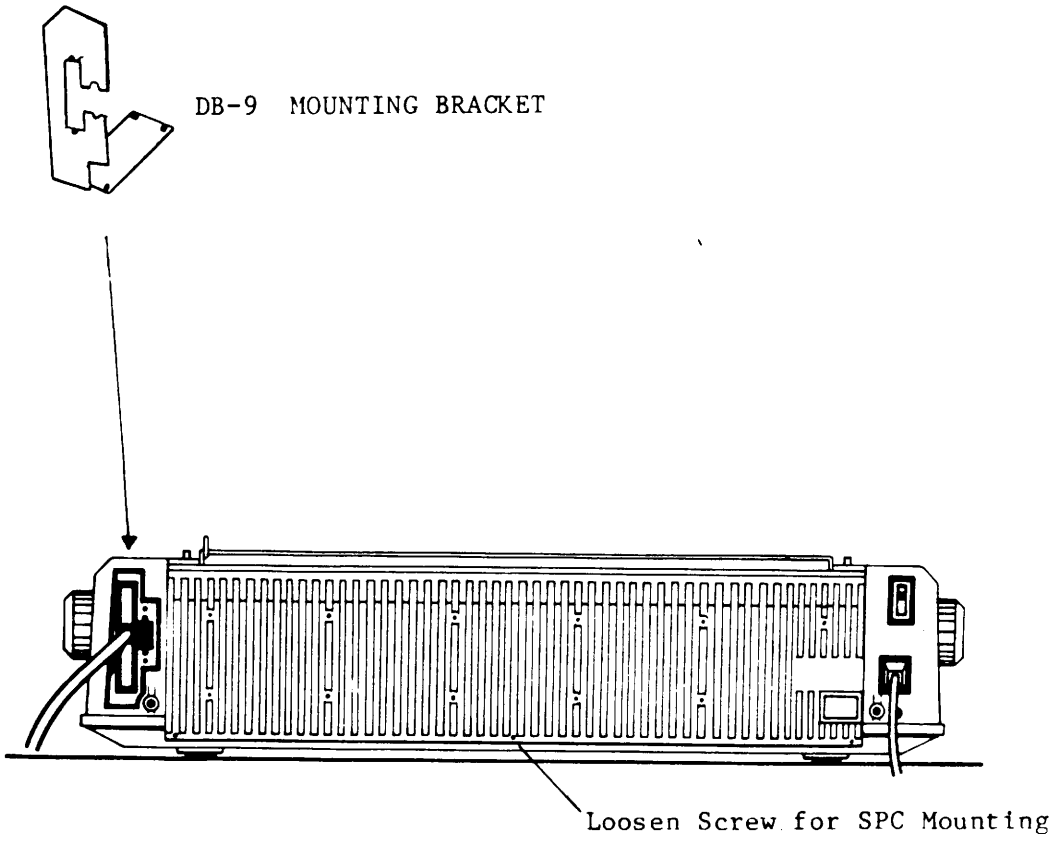


Figure B-5 TEC DB-9 LOCATION AND MOUNTING ASSEMBLY

B.7.3 TEC COVER INSTALLATION

B.7.3.1 COVER REMOVAL

Unplug the machine from the power source.

(1) Remove the front cover (2), platen cover L (3), platen cover R (4), and platen (1).

(2) Loosen the two screws (M4x10) fixing the panel switch board (10) and slide the panel switch board to the rear.

(3) Remove the three front screws (8) fixing the main cover (7) (these are captive screws, they do not drop out) and two rear screws (9).

(4) Check to ensure that the power switch is in the OFF position and after the hole for the power switch (7) is set away from the power switch, remove the cover upwards.

B.7.3.2 COVER INSTALLATION

(1) Check to ensure that the panel switchboard (10) is moved to the rear (platen direction) insert the main cover (7) from the front of the printer taking care that the power switch is correctly located in the hole in the rear of the main cover (7).

(2) After checking that the main cover (7) is placed in proper position and it does not affect other parts adversely, tighten three screws (8) and two screws (9).

(3) Move the panel switch board forward till it meets the main cover, and tighten screws.

(4) Install the platen (1), platen cover R (4), platen cover L (3), and front cover (2).

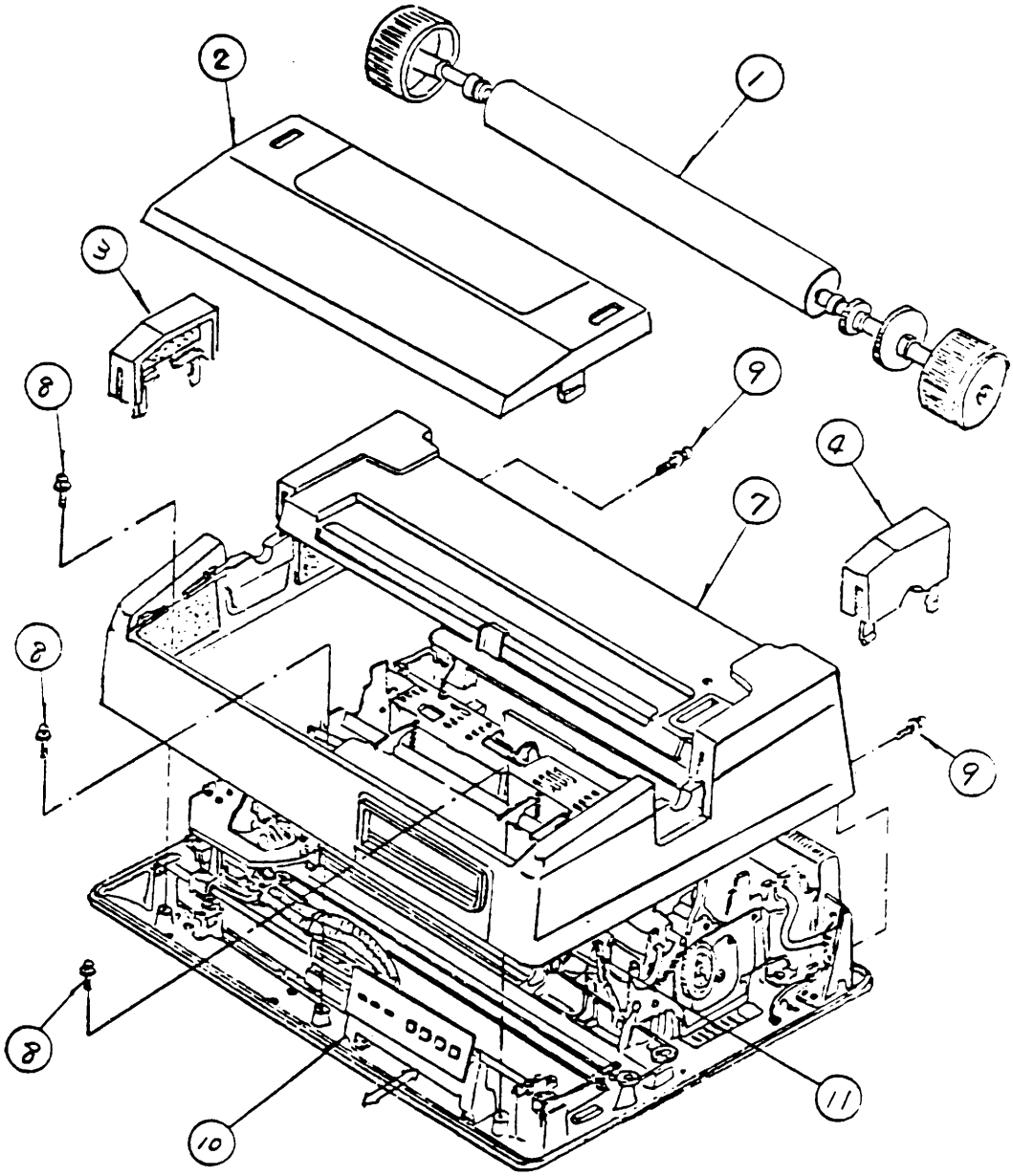


Figure B-6 TEC COVER REMOVAL AND INSTALLATION

B.7.4 MOUNTING SHARED PRINTER CONTROLLER

The SPC will be located at the rear of the TEC printer (see Figure B-7). It can be seen that the upper brackets of the mounting assembly reach over the the top of the heat sink and slip between the plastic cover and the heat sink. Firm pressure may be needed to insert the brackets. There is no mounting hardware necessary.

To mount the bottom bracket, first loosen the screw located at the bottom center of the heat sink (see Figure B-5). Slide the mounting assembly over until the mounting hoop at the bottom of the assembly bottoms with the screw. The screw can then be tightened through the hole in the assembly, thus securing the mounting bracket to the TEC.

Once the mounting assembly is on, then the bottom cover can be added to the assembly. Screw 1 and 2 are inserted and tightened to secure the back cover to the mounting assembly. Finally, stand-offs are inserted on the back cover assembly for the PCB placement.

The PCB is then mounted on the stand-offs and another set of stand-offs are provided for the cover assembly.

Finally, the cover slips over the entire assembly allowing access to the DB-25 input connectors and the power connector. The output DB-25 connector should be fitted through the hole provided in the side of the cover before it is secured (see Figure B-1).

B.7.4.1 MOUNTING WHEN A PAPER PROCESSOR IS USED

The mounting is basically the same when a Paper Processor is used with the exception of the logic and power arrangements. The PCB for the Paper Processor however, must be mounted between the base cover and the SPC PCB. This can be done in a simple stand-off arrangement (see Figure B-8). NOTE: When a Paper Processor is implemented, use the smaller stand-offs included in the Paper Processor package.

Logic and power cable arrangements are discussed futher in future Sections.

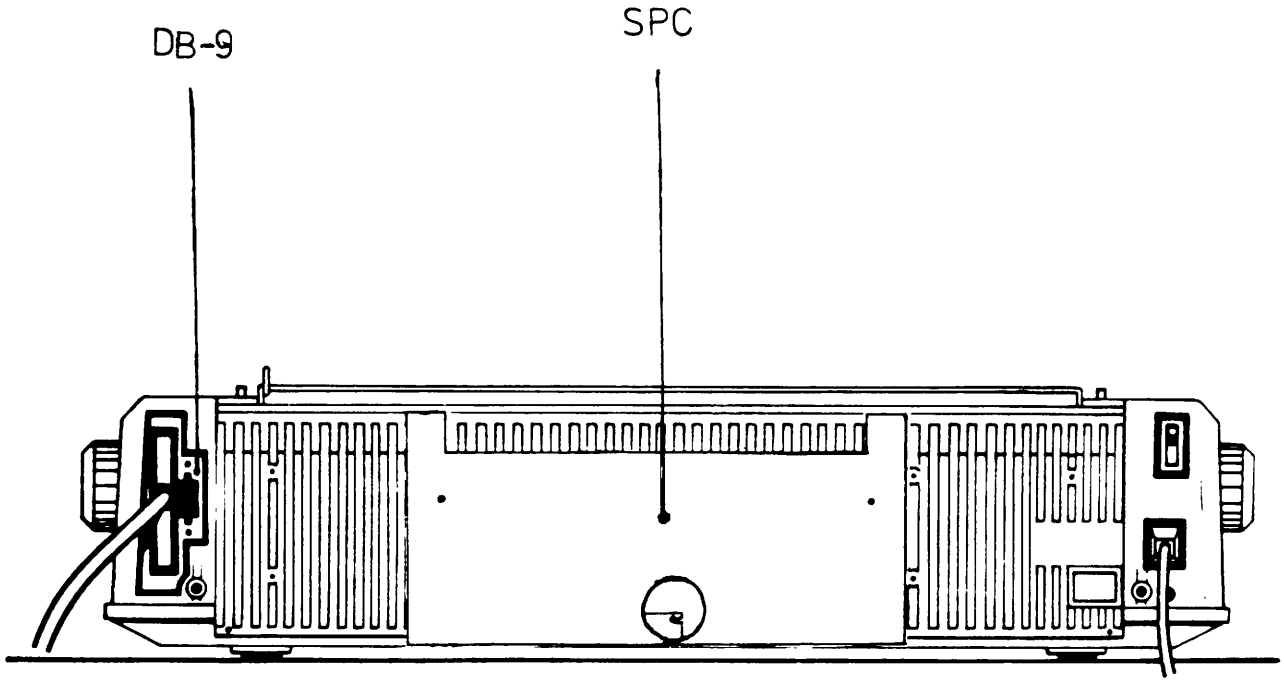


Figure B-7 ORIENTATION OF SHARED PRINTER CONTROLLER TO TEC

B.7.5 LOGIC CABLE ARRANGEMENT WITHOUT PAPER PROCESSOR

As stated earlier, the SPC has no intelligence of its own. Therefore, data and control information is supplied by the M3004 Systems being used. The outputs from each system go to a DB-25 connector located on the SPC. There are four DB-25 connectors in total and the M3004 Systems must toggle for control. When one M3004 System has accesed the SPC then it also has control over the TEC printer. Information is output from the SPC to the TEC via another DB-25 connector. The hook-up from the SPC to TEC is the same as that used when only one M3004 and no SPC is utilized.

The SPC receives its power from the TEC printers power supply. The +15v, -15V and +5Vs needed to power the SPC are tapped from a DB-9 connector located next to the DB-25 connector on the back of the TEC. Access to this connector is achieved by gently breaking off the tab over the connector (see Figure B-5).

B.7.5.1 LOGIC CABLE ARRANGEMENT WITH PAPER PROCESSOR

The logic cable arrangement used when a paper processor is incorporated is basically the same as that used without a paper processor. The data and control signals are still supplied to the SPC from the M3004 Systems but the output from the SPC (instead of going directly to the printer) goes to the paper processor via its connector J3. When the SPC is mounted on the paper processor this means a simple loop-back arrangement with the communications cable (see Figure B-8). Then connection from J1 of the paper processor is taken to the DB-25 of the printer.

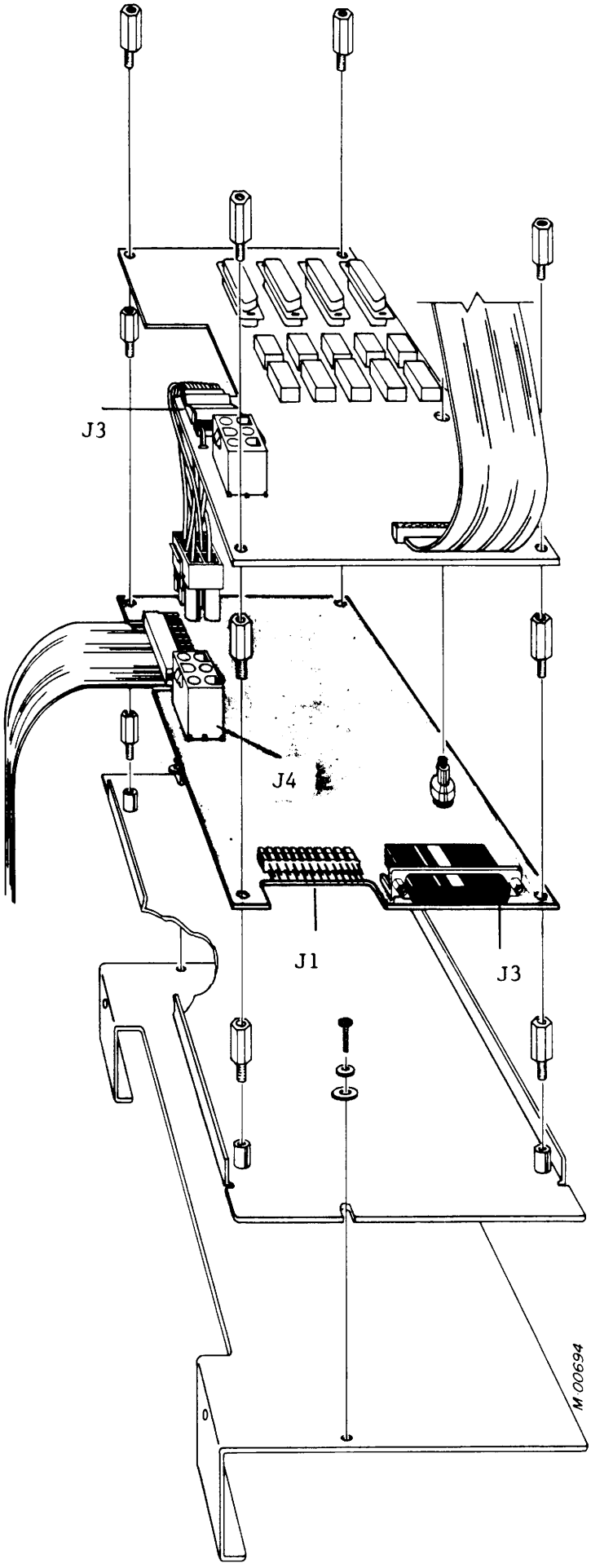


Figure B-8 EXPLODED VIEW OF SPC WITH PAPER PROCESSOR

B.7.6 POWER FOR THE SHARED PRINTER CONTROLLER

Power for the Shared Printer Controller is taken from the TEC Printer via a DB-9 connector located on the rear of the unit (see Figure B-5).

When preparing the TEC for the transfer of power, certain modifications must be made. These modifications have already been covered in the Installation Section. Once the modifications to the printer have been made then the SPC can be powered by the TEC by a simple cable connection. The Power Cable coming from J2 of the SPC is connected to the DB-9 of the TEC (see Figure B-1).

B.7.6.1 POWER FOR THE SHARED PRINTER CONTROLLER WITH PAPER PROCESSOR

When used with the Paper Processor the power arrangement for the SPC is the same. The Paper Processor, however, must get its power from the SPC. This is done through a simple loop-back arrangement from the SPC to the Paper Processor. A power cable loops from connector J3 on the SPC to connector J4 of the Paper Processor (see Figure B-8).

B.8 SPARE PARTS LIST

This section provides a list of all replacable parts for the Shared Printer Controller Assembly.

Table B.4 ASSEMBLY PCB SHARED PRINTER

REF DES	12NC PART NUMBER	DESCRIPTION
U1	5107 259 94221	INT. CKT. MC3486P
U2,4	5107 259 99331	INT. CKT. 74LS175
U3	5107 259 85351	INT. CKT. 63LS141
U5	5107 259 99191	INT. CKT. 74LS14
U6-10	5107 259 85391	INT. CKT. DG-201
R9	5107 259 85301	RES. CF. 570 OHM 1/4W ±5%
R1,4,6,8	5107 259 99661	RES. CF. 2K2 OHM 1/4W ±5%
R2,3,5,7	5107 259 99631	RES. CF. 4K7 OHM 1/4W ±5%
C1,3,5	5107 259 95471	CAP. TANT. 22uF 25V ±20%
C2,4,6,7-16	5107 259 95401	CAP. CER. 0.1uF 50V ±20%(.2SP)
RN1	5107 259 97451	RES. NTWK. 2K2 OHM
	5107 299 80101	ASSY, CABLE, SIG. SHARED PRNT
J2	2422 034 16853	HOUSING 6 POS.
J3	5107 259 85271	HEADER 6 POS. R.A.
J4-7	5107 259 85311	CONN. 25 POS.
	5107 200 19511	PCB SHARED PRINTER
	5107 259 84871	STANDOFF BUSHING
	5107 259 84861	SCREW 4-40 X 1/4

Table B.5 ASSEMBLY SHARED PRINTER W/O PAPER PROCESSOR

REF NO.	12NC PART NUMBER	DESCRIPTION	QTY
11	5107 025 00221	WSHR FLAT #6 .156x.375	2
09	5107 025 00561	SCR BHMS 6-32x3/8" PHILIPS DR	8
10	5107 025 00681	WSHR STAR INT #6	8
01	5107 200 36681	COVER SHARED PRINTER	1
07	5107 259 84851	STANDOFF	4
06	5107 259 85081	STANDOFF	4
08	5107 259 91481	ASSY POST JACK	4
13	5107 259 92161	CABLE MOUNT	1
14	5107 259 92171	TIE WRAP LOOSE	1
05	5107 299 80111	ASSY CBL PWR SHARED PRINTER	1
04	5107 299 80351	ASSY CBL PCB SHARED PRINTER	1
03	5107 299 81251	ASSY MOUNT PROCESSOR TEC	1
02	5107 299 81261	ASSY COVER BOTTOM SERIAL BOX	1

Table B.6 ASSEMBLY SHARED PRINTER FOR PAPER PROCESSOR

REF NO.	12NC PART NUMBER	DESCRIPTION	QTY
06	5107 025 00221	WHSR FLAT #6 .156x.375	4
04	5107 025 00241	NUT HEX #6-32 STD	4
07	5107 025 00561	SCR BHMS 6-32x3/8" PHILIPS DR	4
08	5107 025 00681	WHSR STAR INT #6	8
01	5107 200 36681	COVER SHARED PRINTER	1
03	5107 259 84851	STANDOFF	4
05	5107 259 91481	ASSY POST JACK	4
02	5107 299 80351	ASSY PCB PRINTER	1

Table B.7 ASSEMBLY CBL POWER PRINTER

REF NO.	12NC PART NUMBER	DESCRIPTION	QTY
04	2422 034 16267	TERMINAL	4
08	0722 183 00035	WIRE 18AWG BRN UL1007/CSA-TR64	8
07	0722 183 00036	WIRE STRAP 18AWG RED	7
06	0722 183 00038	WIRE 18AWG YEL UL1007/CSA-TR64	6
05	0722 183 00039	WIRE 18AWG GRN	5
01	5107 259 84931	CONNECTOR HOUSING 6 POS	1
02	5107 259 93071	TERMINAL CRIMP	2
03	5107 259 96811	HOUSING 6 POS	3

Table B.8 ASSEMBLY CBL SIGNAL

REF NO.	12NC PART NUMBER	DESCRIPTION	QTY
03	2422 025 02791	CONN 25 POS	1
01	0722 206 11005	FLT CBL 25 COND	.320
04	5107 259 84881	RETAINER KIT	2
02	5107 259 85291	CONN 26 POS D.R.	1

Table B.9 SHARED PRINTER W/O PAPER PROCESSOR

REF NO.	12NC PART NUMBER	DESCRIPTION	QTY
04	PRELIMINARY-1	ASSY PKG SHARED PRINTER	1
01	5107 299 80091	ASSY SHARED PRNTR W/O PAP PRO	1
03	5107 299 83672	ASSY CABLE PRNTR INT DC	1
02	5107 299 85001	ASSY CABLE ZIYAD EXT DC	1

Table B.9 SHARED PRINTER FOR PAPER PROCESSOR

REF NO.	12NC PART NUMBER	DESCRIPTION	QTY
03	PRELIMINARY-1	ASSY PKG SHARED PRINTER	1
01	5107 299 80081	ASSY SHARED PRNTR FOR PAP PRO	1
02	5107 299 80111	ASSY CBL PWR SHARED PRINTER	1

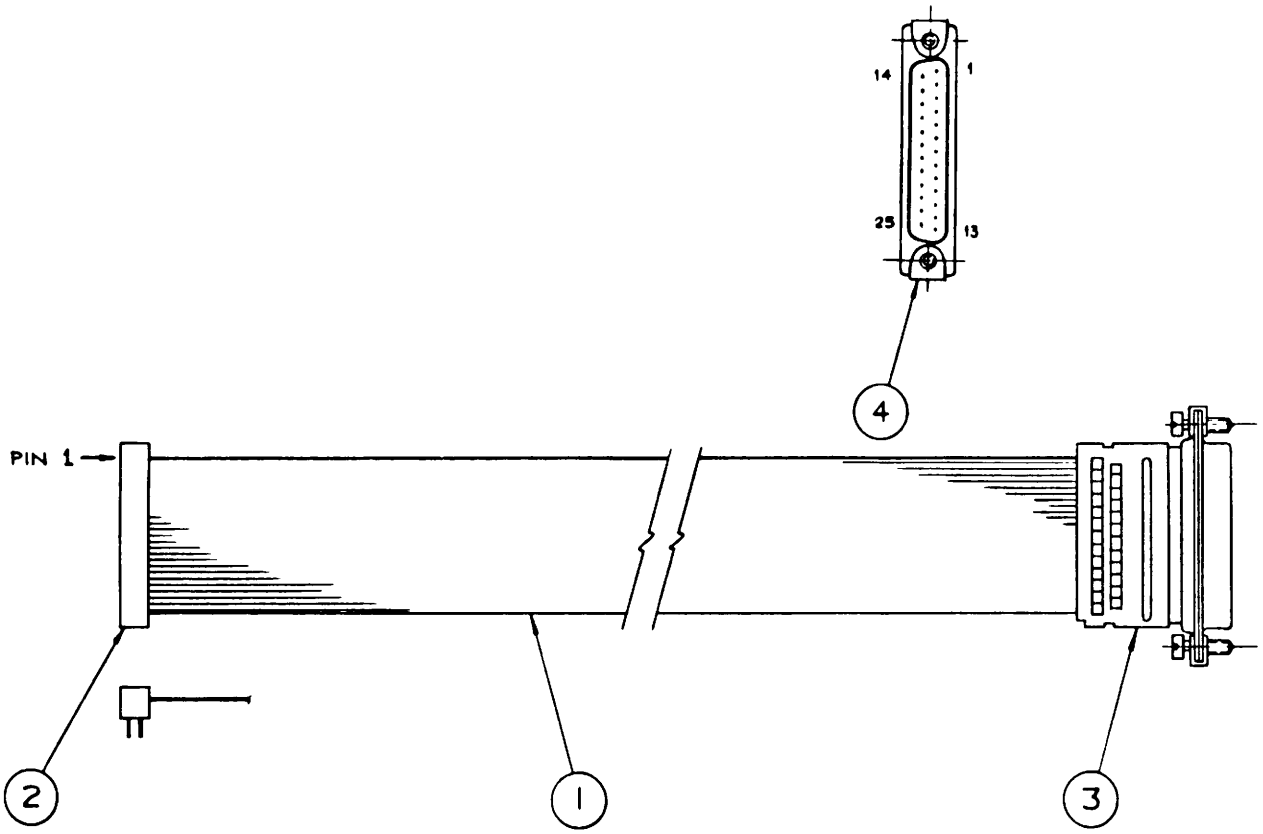


Figure B-9 ASSEMBLY SIGNAL CABLE

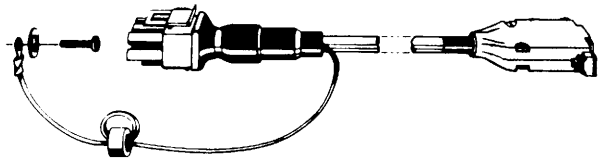


Figure B-10 ASSEMBLY POWER CABLE

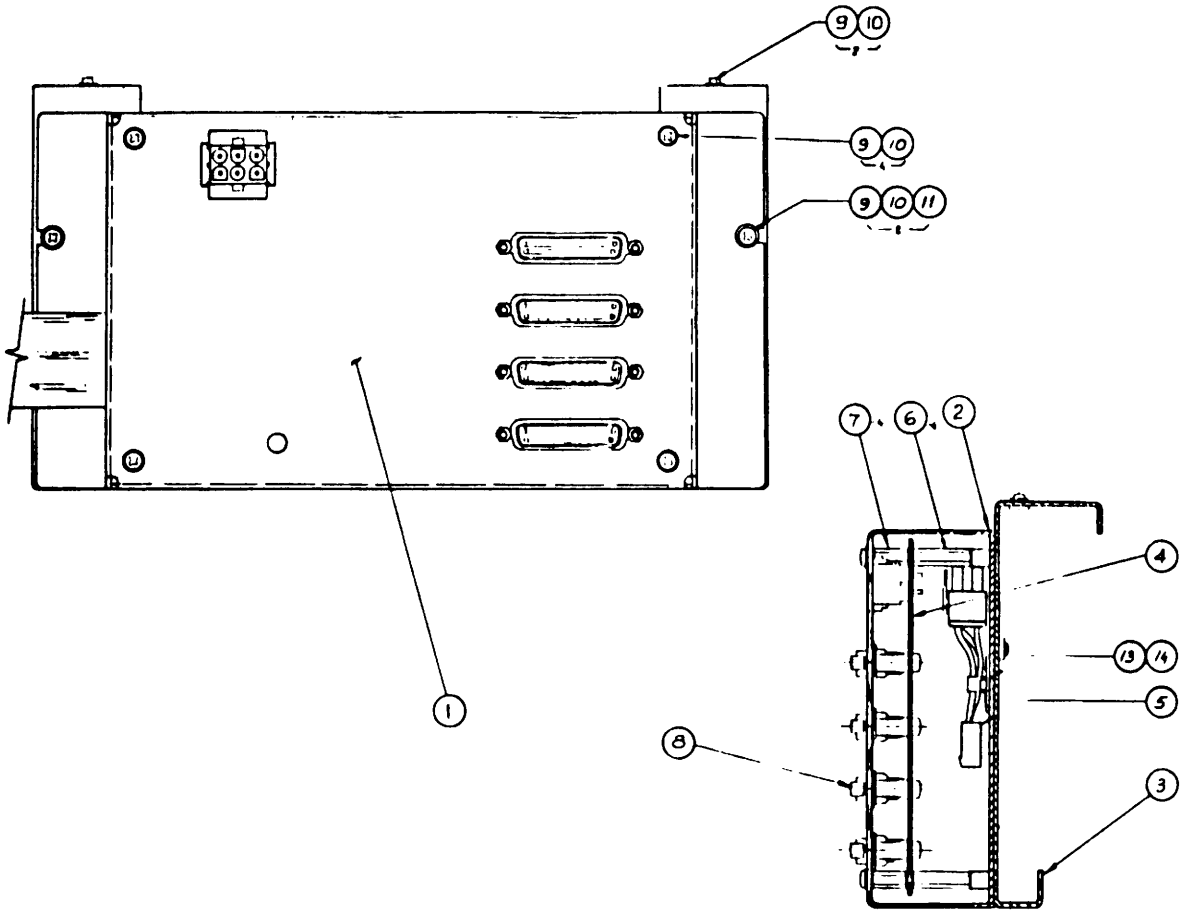


Figure B-11 ASSEMBLY SHARED PRINTER CONTROLLER W/O PAPER PROCESSOR

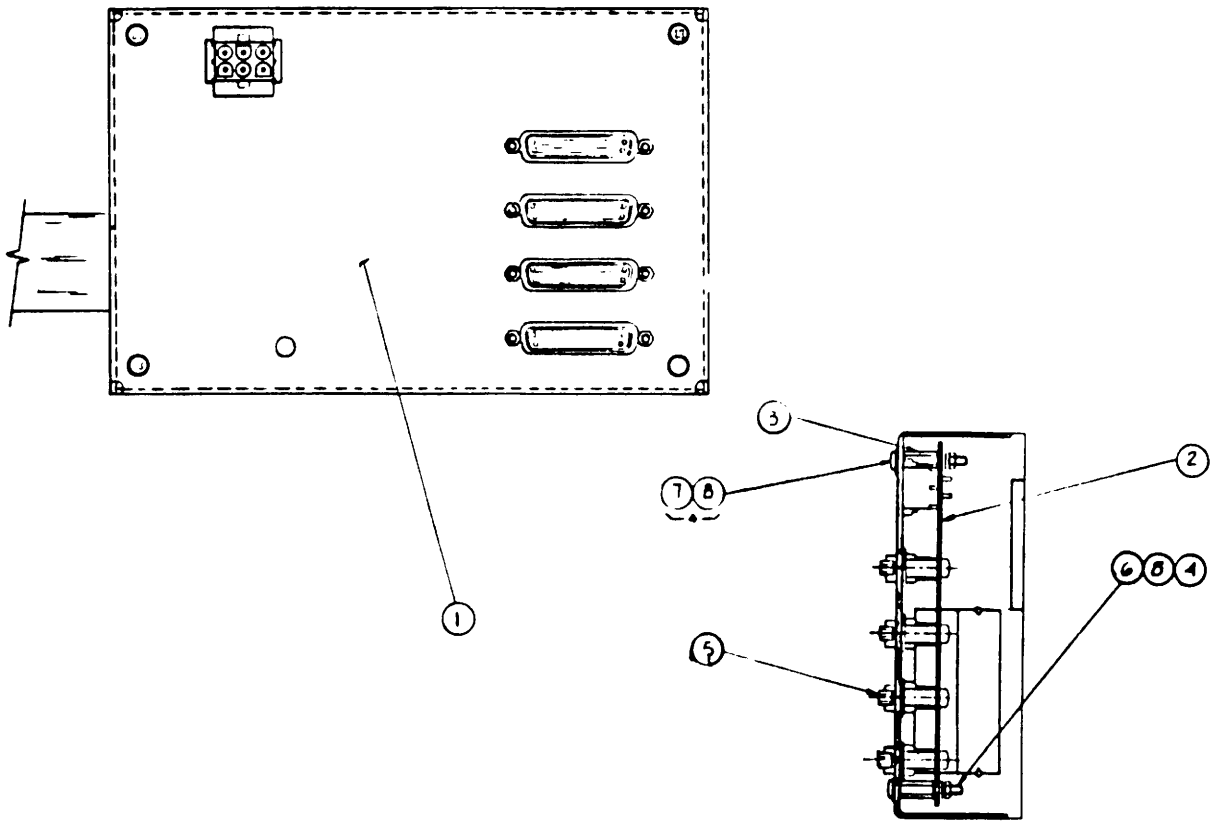
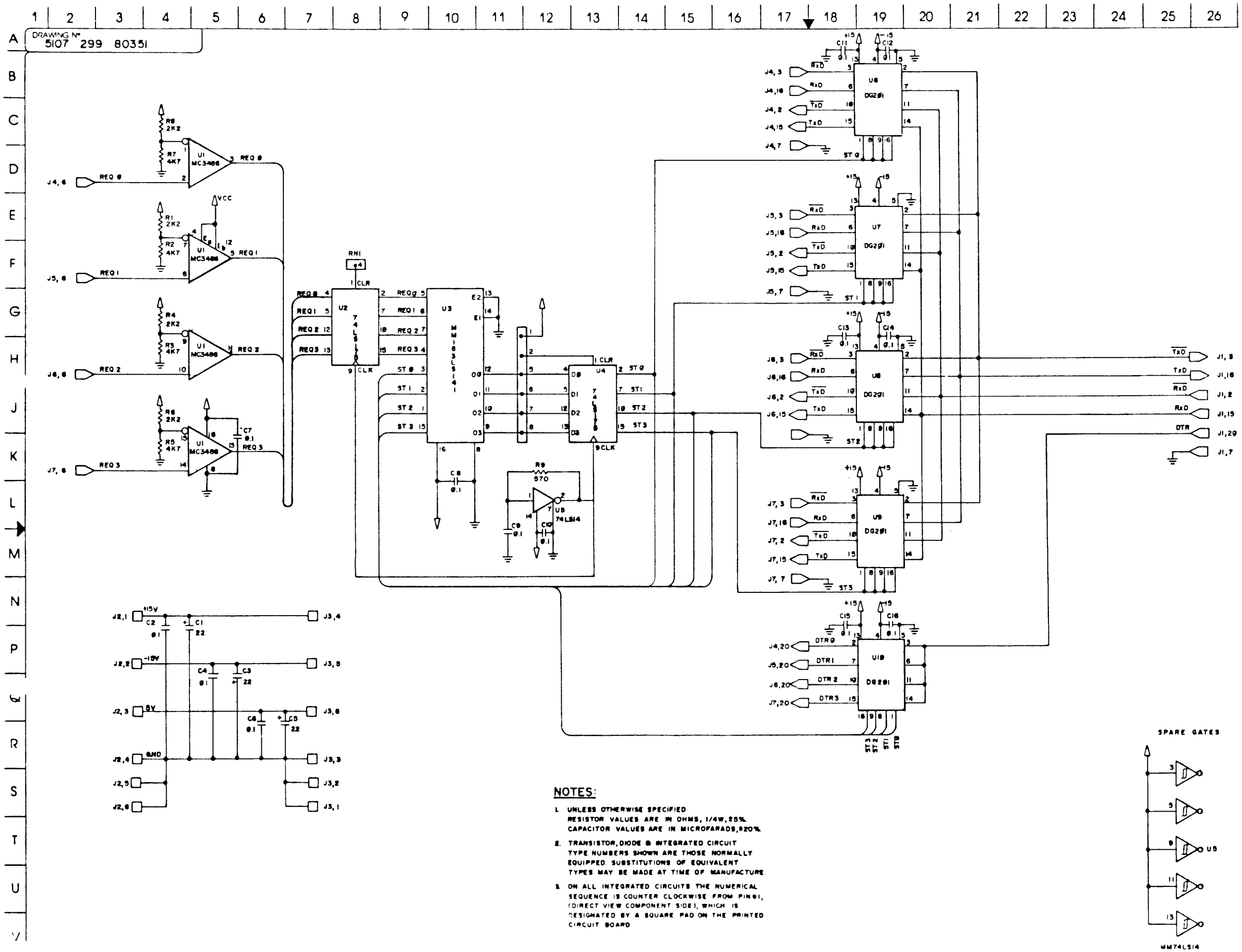


Figure B-12 ASSEMBLY SHARED PRINTER CONTROLLER WITH PAPER PROCESSOR



NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTOR VALUES ARE IN OHMS, 1/4W, 25% CAPACITOR VALUES ARE IN MICROFARADS, ±20%
2. TRANSISTOR, DIODE & INTEGRATED CIRCUIT TYPE NUMBERS SHOWN ARE THOSE NORMALLY EQUIPPED. SUBSTITUTIONS OF EQUIVALENT TYPES MAY BE MADE AT TIME OF MANUFACTURE
3. ON ALL INTEGRATED CIRCUITS THE NUMERICAL SEQUENCE IS COUNTER CLOCKWISE FROM PIN 01, (DIRECT VIEW COMPONENT SIDE), WHICH IS DESIGNATED BY A SQUARE PAD ON THE PRINTED CIRCUIT BOARD

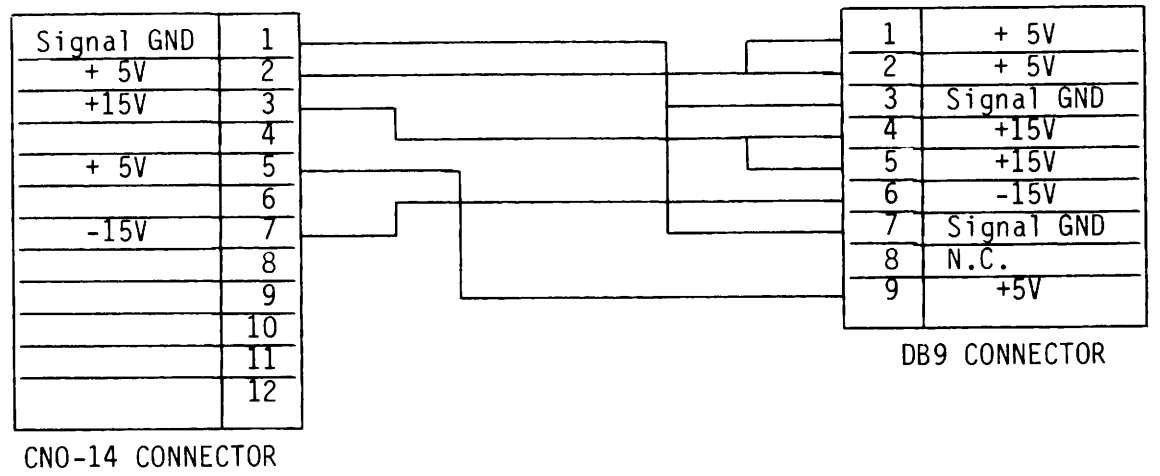


Figure B-14 INTERNAL TEC CABLE

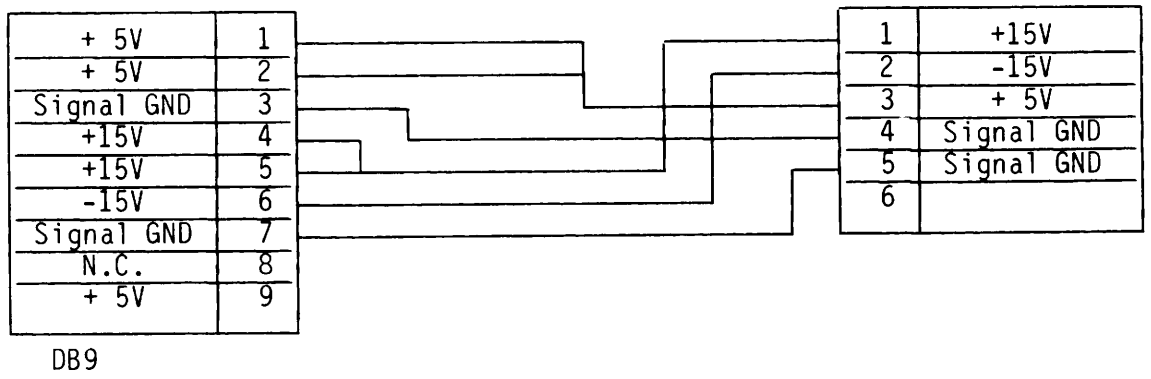


Figure B-15 EXTERNAL POWER CABLE FOR SHARED PRINTER

APPENDIX C: SWIFT NUMERIC KEYPAD

C.1 INTRODUCTION:

The Numeric keypad shown in figure C-1.1 is one of the several secondary keyboard that could be daisy chained to the main keyboard in a multiple keyboard support environment. The numeric keypad is an operator input device to the console, providing numeric, arithmetic and some special function codes to the M3003 word processing system. In addition, it echoes received serial data from the main keyboard as transmitted data to the console without examining it for self test directives.

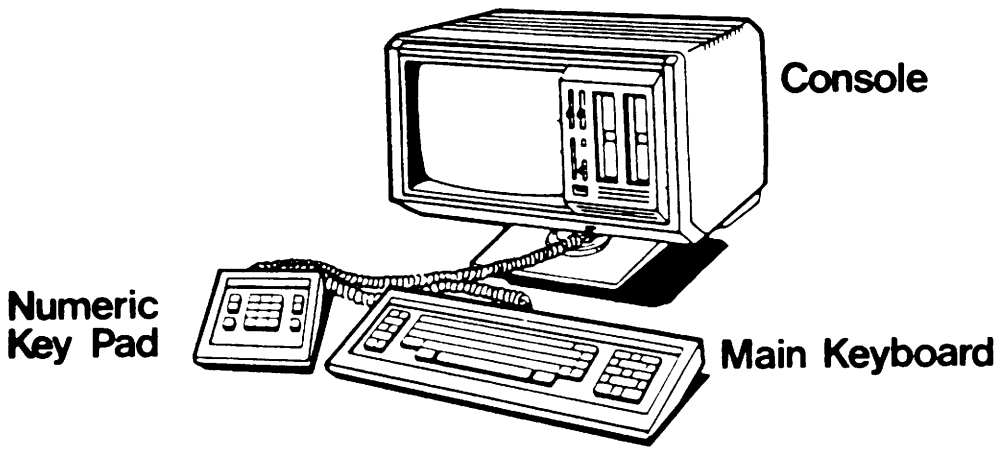


Figure C-1.1

The numeric keypad is a self-contained microcomputer controlled unit housed in a sand mould casting measuring 182x207x45 mm. The top cover and the base are secured together by four Phillps screws accessible from the bottom at the four extreme corners as shown in Fig.C-4.1. The keypad P.C.B. rests on the inside of the base and is secured to it by four Phillps screws at the inside corners, accessible from the bottom as shown in Fig.C-4.1. The keypad interfaces with the main keyboard and console via a connector and a connector-equipped telephone type cord, as shown in the Fig.C-3.1. The signals at the connector pinouts are indicated in TablesC-1.1, C-1.2 and in the schematic diagram (Fig.C-2.3).

There are two types of numeric keypads available to the user to facilitate different schools of thought. The main difference between the two is the placement of 1-2-3 and 7-8-9 numeric keycaps on the keypad. Fig.C-1.2 gives the settings of these keycaps indicating the names assigned to each type.

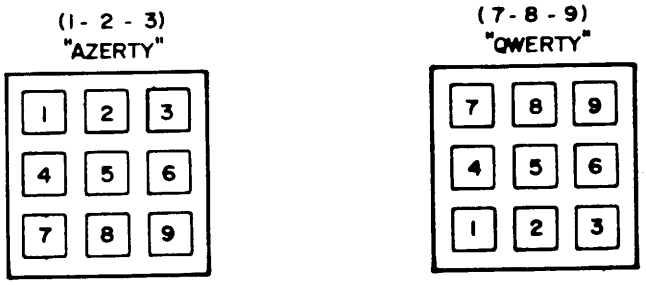


Figure C-1.2 NUMERIC KEYPAD TYPES

Table C-1.1 CONNECTOR PIN (P1) ASSIGNMENTS

PIN NUMBER	SIGNAL
A3	+5 Vdc
B2	Ground
A2	KEY
B1	NRV DATA
A1	16xCLK
B3	N/C

Table C-1.2 CONNECTOR PIN (P2) ASSIGNMENTS

PIN NUMBER	SIGNAL
A3	+5 Vdc
B2	Ground
A2	NTX DATA
B1	N/C
A1	16xCLK
B3	KEY

C2. THEORY OF OPERATION:

This section, divided into several subsections describes in detail the operation of the numeric keypad circuit, while discussing in brief the MK3873 microcomputer chip structure. For a detailed description of the microcomputer refer to the Mostek data book.

Refer to the following figures and Table where ever applicable:

- Block diagram (Fig.C-2.1).
- Schematic diagram (Fig.C-2.2)
- Keypad scanning diagram (Fig.C-2.3)
- MK3873 pin outs assignment (Table C-2.4).
- MK3873 internal structure diagram (Fig.C-2.4).

The following tasks are performed by the keypad:

- Identify depressed key.
- Generate secondary keyboard identification (escape) and character codes and transmit it to the console.
- Echo the serial data from the main key board to the console.
- Eliminate bouncing, rollover and static problems.

To accomplish these tasks the firmware uses the 2.5Mhz clock, 8x3 keyboard matrix and the MK3873 single chip microcomputer, which are the main components of the numeric keypad as shown in the block diagram (Fig.C-2.1).

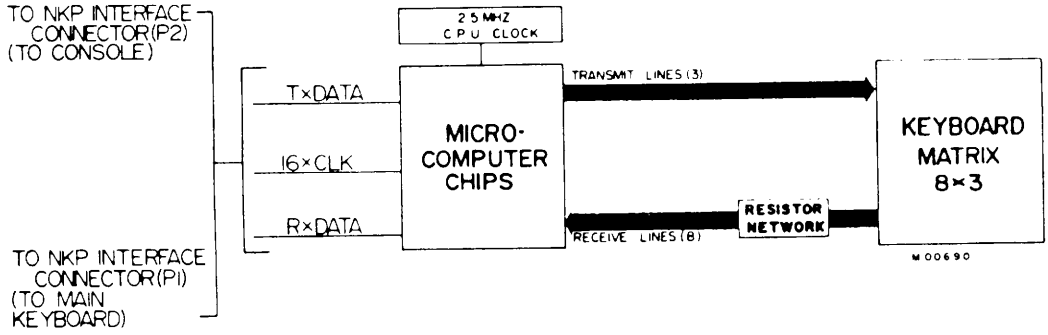


Figure C-2.1 NUMERIC KEYPAD BLOCK DIAGRAM

2.5Mhz Clock:

The C.P.U. clock is formed by the R.C. network (C4, R7&R8) and conditioned by the Schmitt triggered invertor (U2) before being applied to the external input (XTAL2, pin2) of the microcomputer, for it's internal operations.

Keyboard Matrix:

As shown in Figure C-2.3, each of the key switches installed in the 8x3 keyboard matrix are connected to their respective row lines via diodes, to eliminate roll over problem. Certain positions in the keypad matrix are not connected, since relative positions in the main keyboard matrix either have auto repeat keys or are not connected at all. Since the output lines (columns) of the matrix (inputs to the microcomputer;P0-P57) are normally open (keys off) a pull down resistor network RN1 is used. The character code generated for each depressed key is shown in Table C-2.3. Note that the character codes for similar keys on numeric keypad and main keyboard are different from one another.

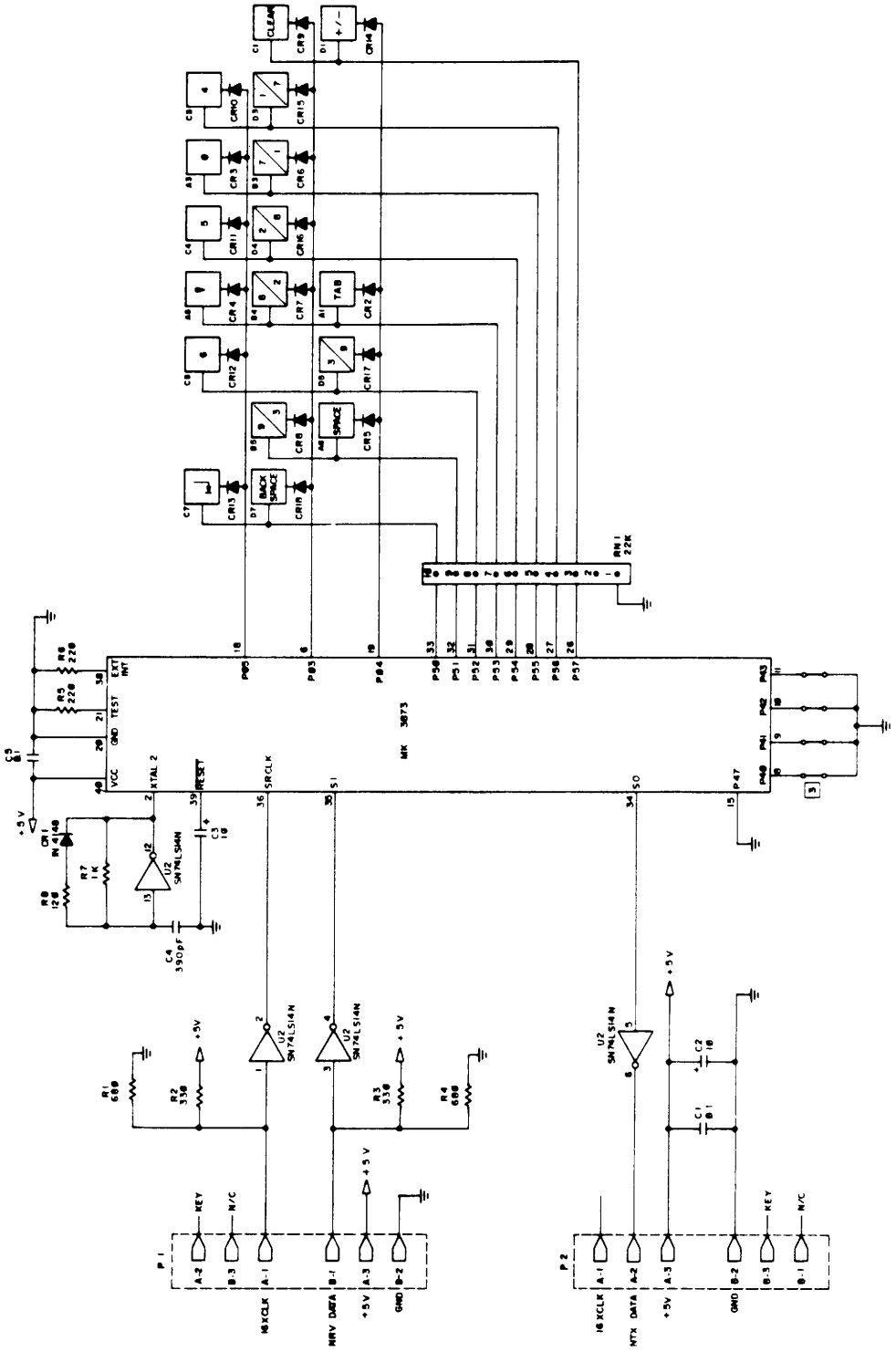


Figure C-2.2 NUMERIC KEYPAD SCHEMATIC

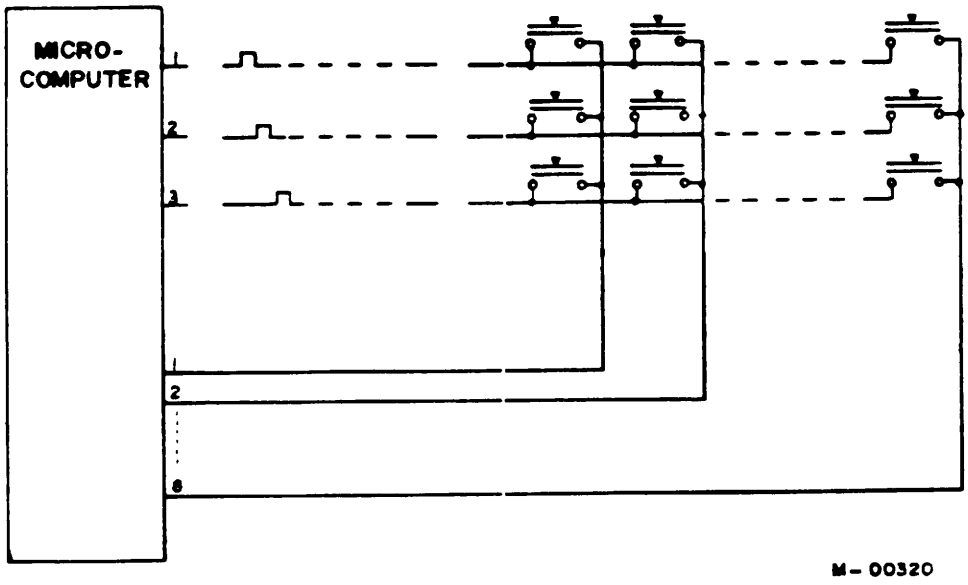


Figure C-2.3 KEYPAD SCANNING

Microcomputer:

The main component of the numeric keypad is the single chip MK3873 microcomputer chip, which performs the following functions.

- Scan the keyboard matrix to identify the depressed key.
- Convert the data, comprising of escape code (8 bits) and character code (8 data bits & 2 stop bits, with no (parity) and transmit it to the console.
- Receive serial data from the main keyboard and echo the same to the console.

The 8 bit microcomputer is equipped with 4 bidirectional ports (port 0, 1, 4, 5), three being 8 bits wide (port 0, 4, 5) and one 5 bits(port 1) as shown in Fig.C-2.5. The microcomputer, by applying strobes in sequence as shown in fig.C-2.2, to the input lines of the matrix (rows) through it's port 0 I/O lines (P0-3, P0-4 & P0-5, pins 6,19 &18 resp.) monitors the 8 output lines of the matrix (columns) going to port 5 I/O lines by reading the status of port 5 (P50-P57;pins 26-33). The output lines of the matrix are scanned every 6 msec. and whenever a key is depressed the scanning is repeated twice to ensure that bouncing effects have been eliminated.

When a key is depressed the console has to identify it's source (Main or Secondary keyboard). This is accomplished by reading the status of a single I/O line of port 4 (P47;pinl5). This pin is tied low for a secondary keyboard while pulled high for the main keyboard. The escape code generated by the secondary keyboard (numeric keypad) supplies this information to the console.

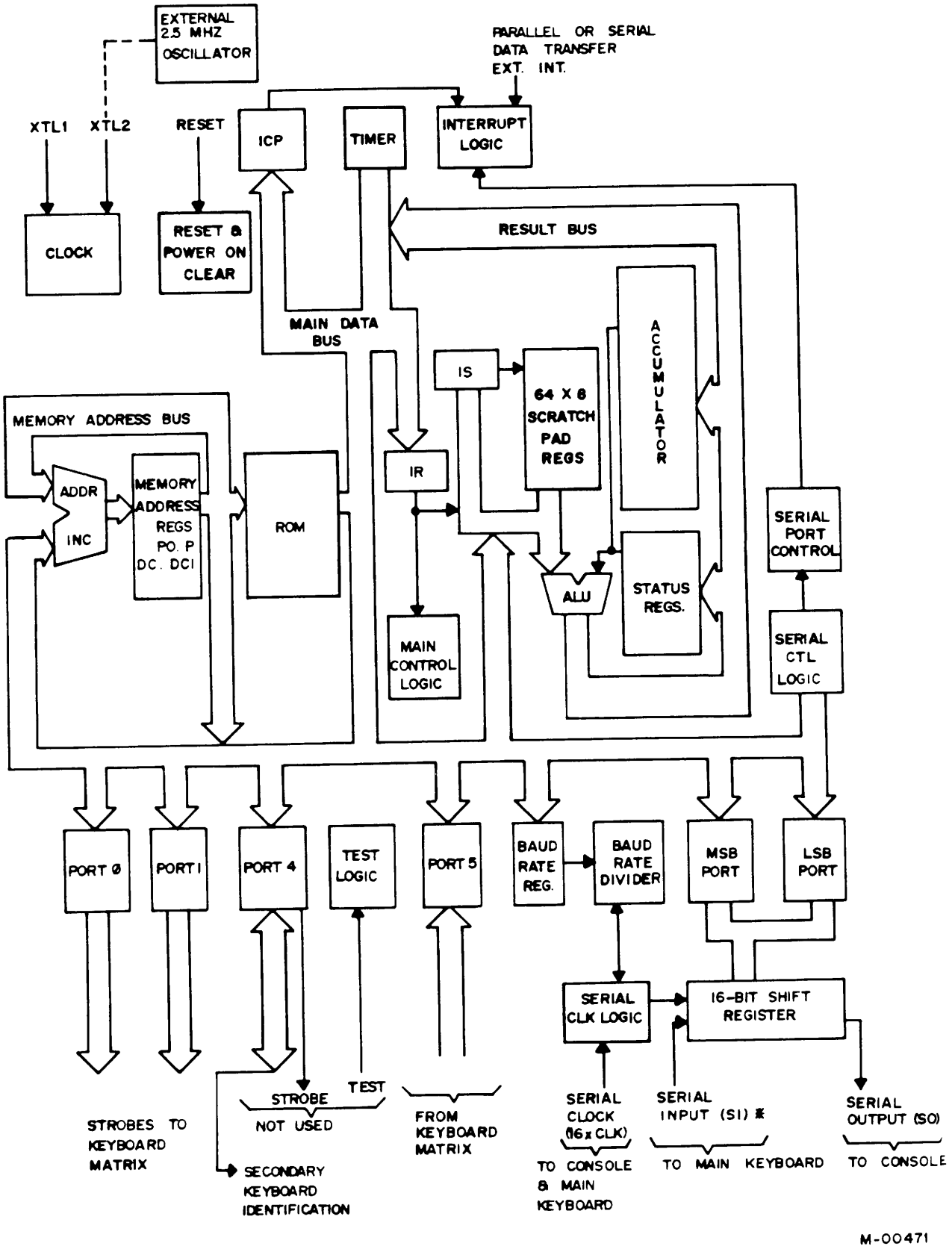


Figure C-2.4 MICROCOMPUTER ARCHITECTURE

In a multiple keyboard support environment it is possible that more than one secondary keyboard is daisy chained to the main keyboard or different types of secondary keyboards could be connected one at a time to the main keyboard. Therefore the console has to identify the type of secondary keyboard connected to the main keyboard. Port 4 I/O lines (P40,41,42,43;pins 8,9,10,11) are used for this purpose. All these pins are internally pulled high. However, as shown in the schematic (fig.C-2.3) by using programmable jumper configurations between pinouts and ground, any of these pins could be tied low externally. Since the status of 4 bits is read, 16 different configurations are possible. Table C-2.2 gives the escape code generated by the status of the four bits for different jumper configurations.

Since we have only two types of secondary keyboards i.e. Azerty and Qwerty, only the first two configurations are used. Fig.C-2.5 shows the jumper configurations and associated escape codes for these two types of keypads. The escape code contains the status of these pins, which is used by the console to identify the type of secondary keyboard.

The firmware, which directs the activities of the numeric keypad resides in the 1K bytes of ROM inside the microcomputer. The 64 bytes of scratchpad RAM is used for temporary storage, program execution, etc. Memory could be addressed via program counter, stack pointer, data counter, auxilliary data counter, which are the memory address registers in the microcomputer. When a memory access is required, the appropriate address register is gated onto the memory address bus and memory output is gated onto the main data bus. A flowchart indicating the sequence of operations is indicated in fig.C-2.6.

The instruction register (IR) receives the OP-code of the instruction to be executed via the main data bus. The main control logic decodes the instruction and provides the necessary gating signals to the rest of the circuitry. When the ALU receives commands from the main control logic, it performs the required mathematical or logical operation on the data received on the two input buses and provides the result on the result bus. The status of the result (carry, overflow, etc.), is applied to the status registers. The status registers also hold other status flags, such as interrupt control, I/O ports control, etc. The accumulator is the main register for data manipulation, with the result of ALU operations stored there.

The timer is an 8-bit down counter which is a software programmable counter which can be used as an internal timer, pulse width timer or event counter.

The 5V power supply is derived from the console via pin A-2 of connector P2 and is directed to the main keyboard as well via pin A-3 of connector P1.

The two serial IN and OUT ports (pins 35, 34) are serial data links between main keyboard and numeric keypad and between console and numeric keypad respectively. Associated with these serial ports is the serial clock input (6xClk;pin 36), which is derived from the console. This clock (Table C-2.1) sets the baud rate and synchronizes data transfer. The EXINT signal (pin 38) is used in this case to decide whether data transfer by the microcomputer is serial or parallel. In the numeric keypad this is tied low, meaning that data transfer is serial. The incoming (from main keyboard) and outgoing (to the console) data on the serial ports is conditioned by Schmitt triggered invertors U2.

The transfer of data through input and output ports is based on word length, which is pre defined (Escape code=8 bits; Character code=10 bits). The serial output port is used to transfer both numeric keypad and main keyboard data to the console. When ever data is present either on the input or the output port, internal interupts are generated and the requisite data transformation takes place. In the case of numeric keypad, the character code follows the escape code. The firmware at the console first checks whether the data it recieved contains the escape code or not. Presence of escape code indicates that data belongs to numeric keyboard, while it's absence indicates that data was from the main keyboard.

Table C-2.1 CLOCK FREQUENCIES AND BAUD RATES

CLOCK FREQUENCY	BAUD RATE
4.8 kHz	300
9.6	600
19.2	1200
28.8	1800
32.0	2000
38.4	2400
57.6	3600
76.8	4800
115.2	7200
153.6	9600

TABLE C-2.2 ESCAPE CODE

PIN	15	11	10	9	8	ESCAPE CODE
PORT	P4-7	P4-3	P4-2	P4-1	P4-0	
	0	0	0	0	0	07BH
	0	0	0	0	0	07CH
	0	0	0	1	0	07DH
	0	0	0	1	1	07EH
	0	0	1	0	0	07FH
	0	0	1	0	1	0FBH
	0	0	1	1	0	0FCH
	0	0	1	1	1	0FDH
	0	1	0	0	0	0FEH
	0	1	0	0	1	0FFH
	0	1	0	1	0	0FFH
	0	1	0	1	1	0FFH
	0	1	1	0	0	0FFH
	0	1	1	0	1	0FFH
	0	1	1	1	0	0FFH
	0	1	1	1	1	0FFH

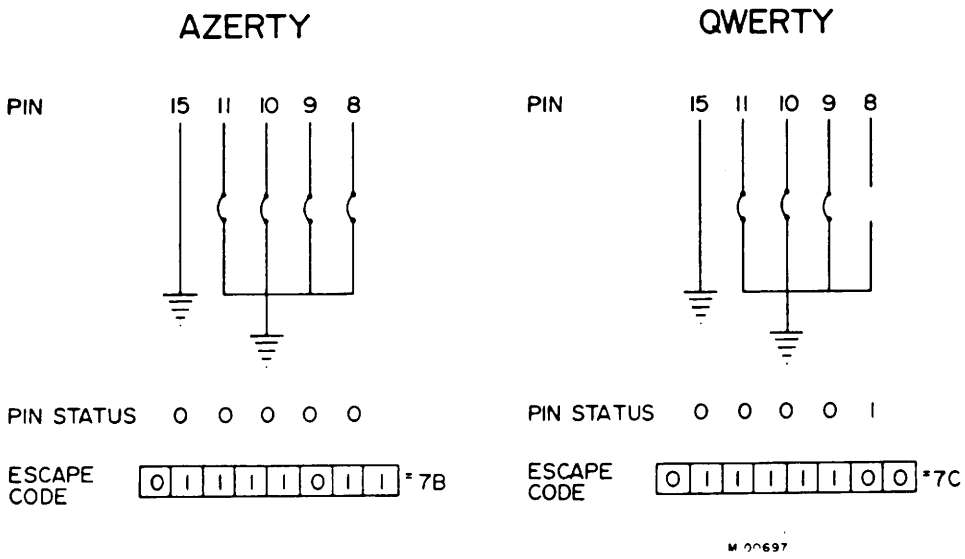


Figure C-2.5 AZERTY AND QWERTY JUMPER CONFIGURATIONS

Table C-2.3 CHARACTER CODES

REC/TRA→ ↓	P03		P04		P05	
	1-2-3	7-8-9	1-2-3	7-8-9	1-2-3	7-8-9
	CODE = 8C		CODE = B8		CODE = 9A	
P50	BACK/SP.	BACK/SP.	N/C	N/C	N/C	N/C
	CODE = 90		CODE = E9		CODE = 9E	
P51	9	3	SPACE	SPACE	N/C	N/C
	CODE = 9D		CODE = EB		CODE = 93	
P52	N/C	N/C	3	9	6	6
	CODE = 99		CODE = ED		CODE = 91	
P53	8	2	TAB	TAB	N/C	N/C
	CODE = FA		CODE = XX		CODE = 82	
P54	2	8	N/C	N/C	5	5
	CODE = E1		CODE = XX		CODE = 80	
P55	7	1	N/C	N/C	0	0
	CODE = F1		CODE = 04		CODE = 01	
P56	1	7	N/C	N/C	4	4
	CODE = B1		CODE = 8B		CODE = 84	
P57	CLEAR	CLEAR	+/-	+/-	N/C	N/C

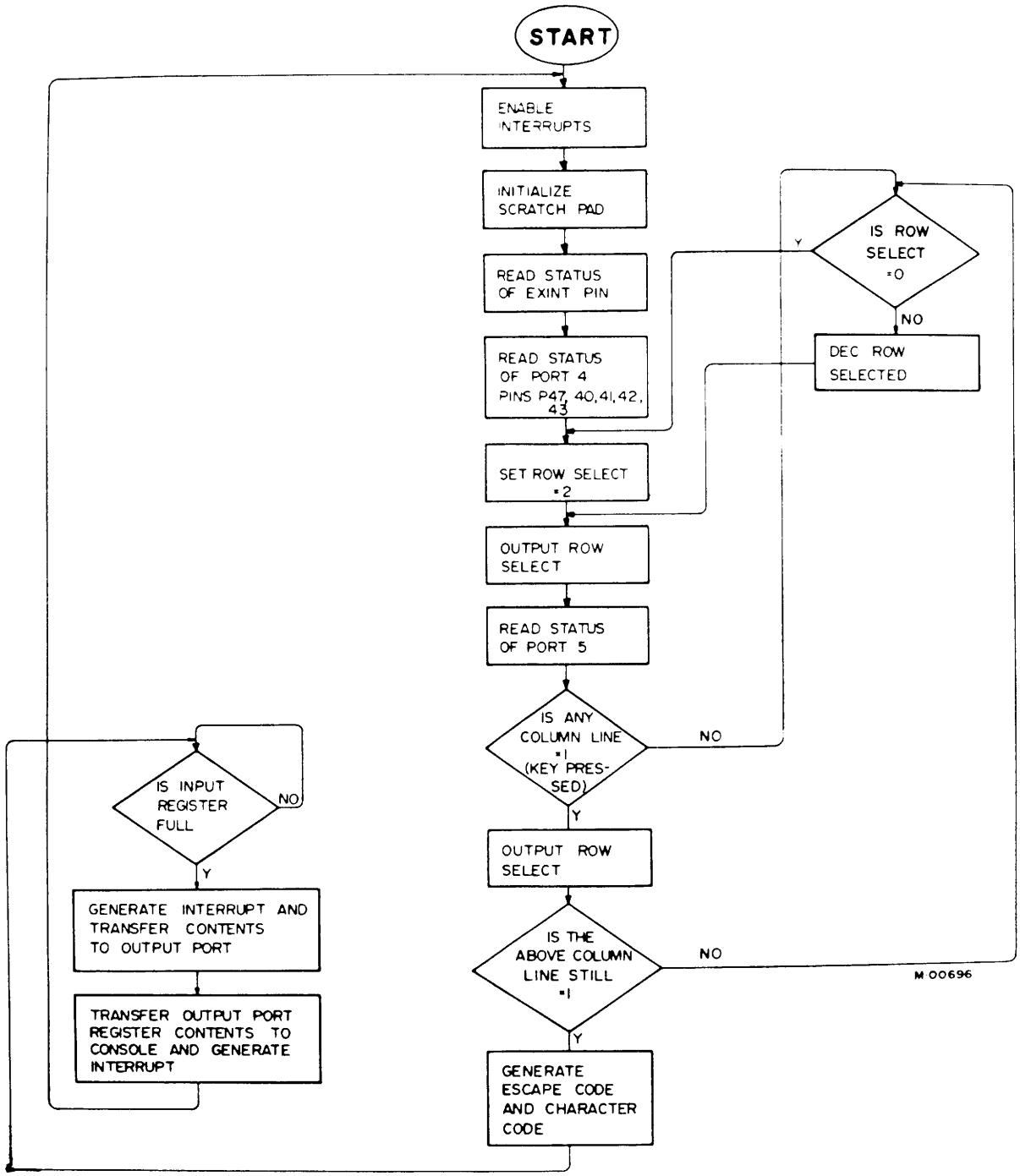
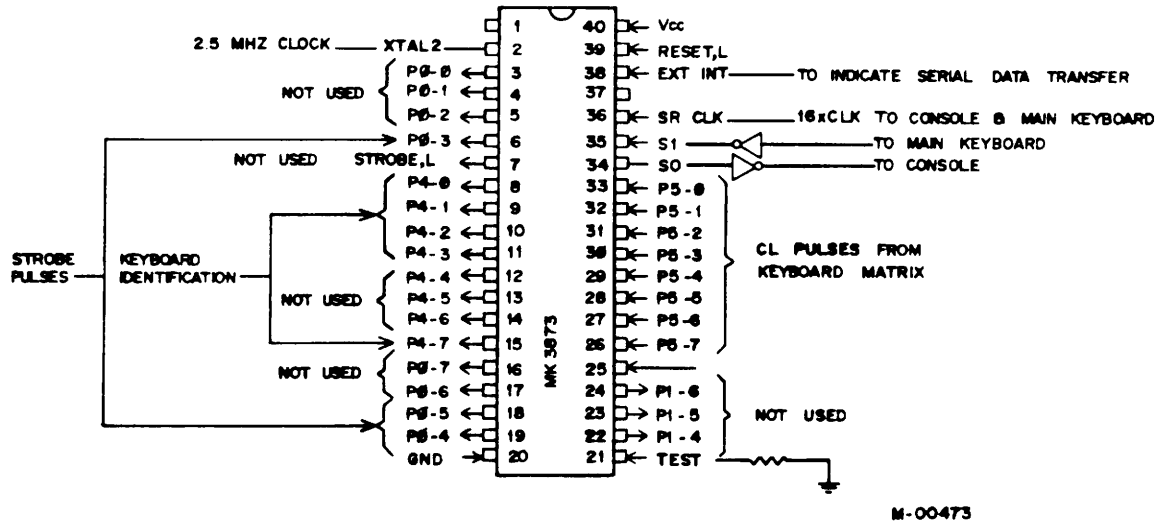


Figure C-2.6 SOFTWARE FLOWCHART

Table C-2.4 MICROCOMPUTER PIN OUT ASSIGNMENT



SIGNAL	DESCRIPTION
XTAL 2 (Crystal 2)	Input. A 2.5 MHz time base signal used to control some internal operations.
P0-3 to P0-5 (Port 0)	Output, active high. 3 strobe pulses to the keyboard matrix.
STROBE	Output, active low. Not used.
P4-0 to P4-3 (Port 4)	Input, programmable to be high or low to identify secondary keyboard.
P4-7 (Port 4)	Input, to identify source (Main or Secondary Keyboard).
GND (Ground)	Ground connection to chip.
Vcc	+5V connection to chip.
RESET,L	When pulled low the microcomputer will reset. When allowed to go high the microcomputer will begin program execution at 000H.

Table C-2.4 MICROCOMPUTER PINOUT ASSIGNMENT (Cont'd)

SIGNAL	DESCRIPTION
EXT INT (External Interrupt)	Input, tied low. To indicate data transfer is serial.
SRCLK (Serial Clock)	Input. Clock rate (16xCLK) which sets the baud rate. See Table C-2.1.
SI (Serial In)	Serial data from Main keyboard.
SO (Serial Out)	Serial data to console.
P5-0 to P5-7 (Port 5)	Input, active high. Clock pulses from keyboard matrix (when keys are operated).
P1-7,L (Port 1)	Output, active low. Not used.
TEST	Input. Not used in this application. Used for factory testing only.

Functional description of Numeric Keypad keys with respect to Main Keyboard keys.

Numeric Keypad	Main Keyboard
CLEAR	DELETE
BACK SPACE	BACK SPACE
SPACE	SPACE BAR
TAB	TAB
$\pm$	-
	.

C.3 INSTALLATION:

Refer to figure C-3.1

The numeric keypad is equipped with a connector equipped telephone type cord and a connector. The cord is connected to the console while the connector is connected to the main keyboard's cord.

The daisy chaining feature has been designed in such a way that main key board is always at the end. However, if only the main keyboard is to be used, then do the following:

- Unplug the numeric keypad telephone type cord from the console.
- Remove the main keyboard cord from the connector of numeric keypad and connect it to the console.

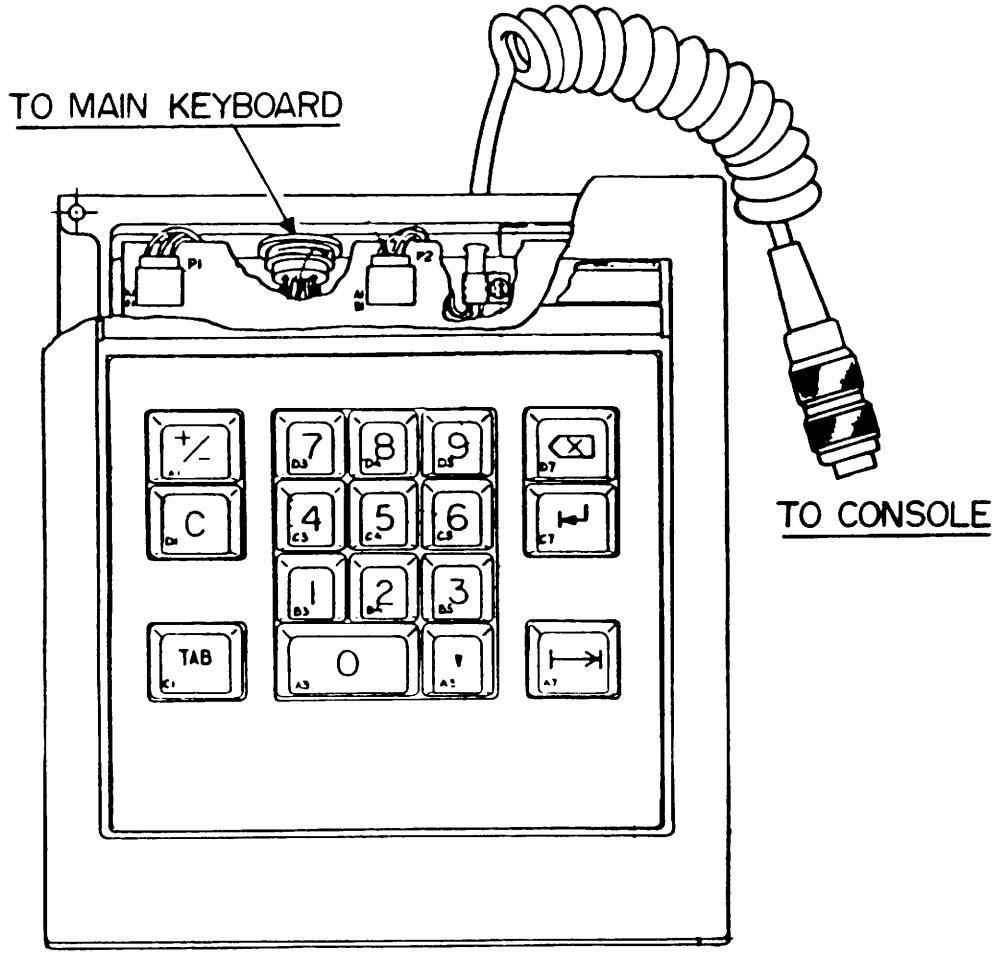


Figure C-3.1 NUMERIC KEYPAD CONNECTIONS TO CONSOLE AND MAIN KEYBOARD

C.4 REPLACABLE PARTS:

Refer to Table C-4.1, figure C-4.1, Figure C-4.2 and Figure C-4.3.

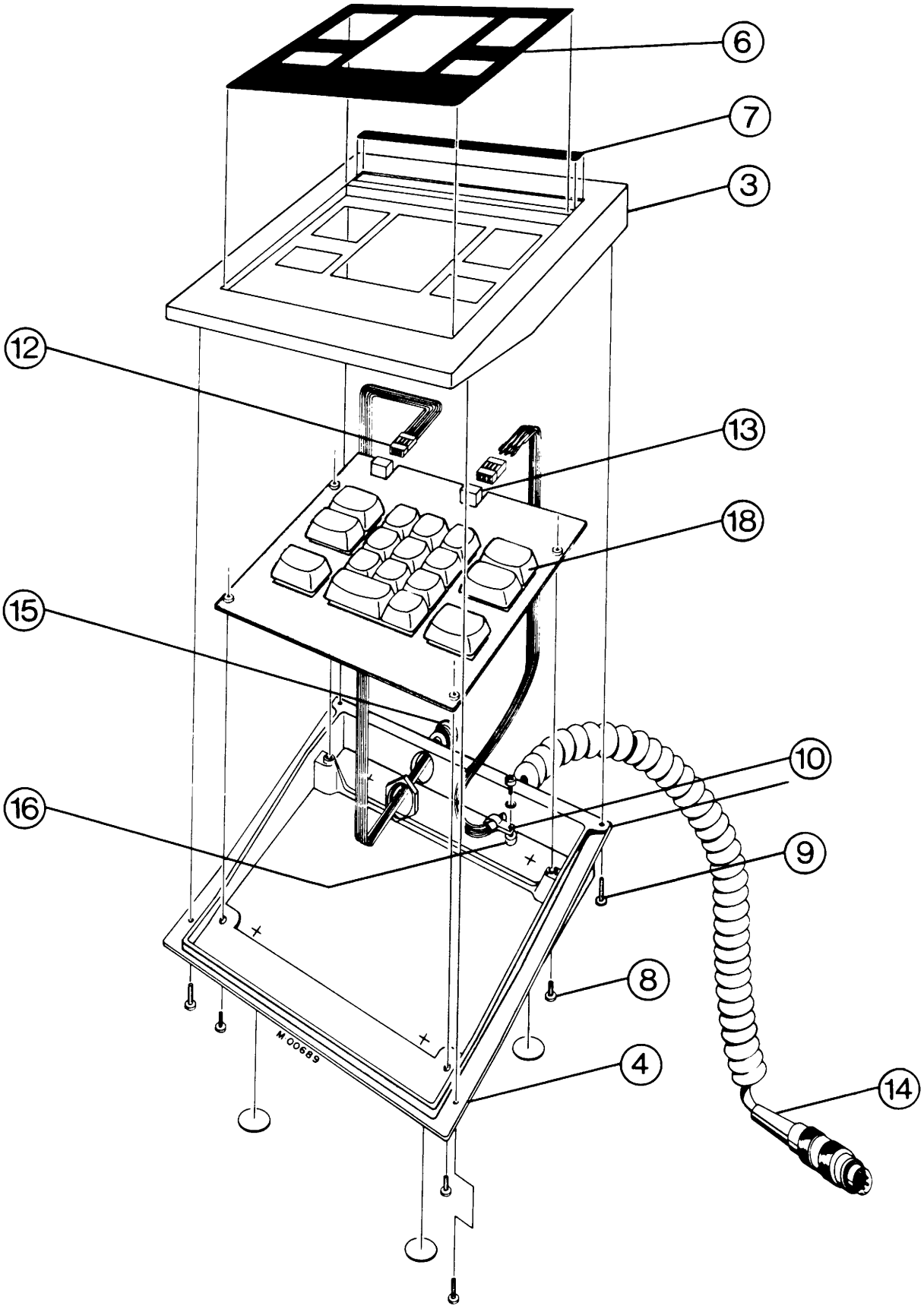
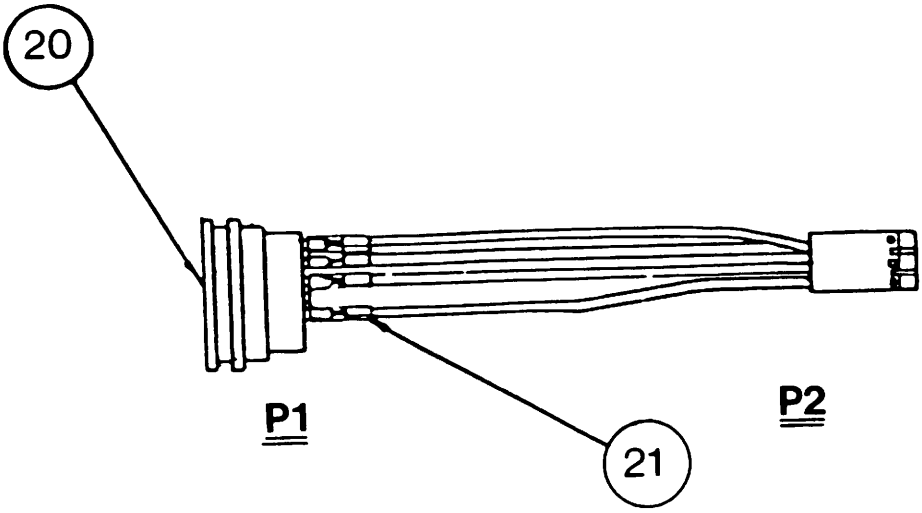


Figure C-4.1

TABLE C-4.1 REPLACABLE PARTS

ITEM	DESCRIPTION	12NC PART NUMBER
1	Numeric Keypad Module (complete)	5107 299 8440
2	P.C.B. (complete)	5107 200 81411
3	Top	5107 200 13492
4	Base	5107 200 13472
5	Sticker	5107 200 1966
6	Keypad Overlay	5107 200 13511
7	Logo Strip	5107 200 16131
8	Screw M3x8	5107 004 02025
9	Screw M3x22	5107 025 01630
10	Clamp	5107 025 01641
11	Polarizing Key BERG #65307-001	2422 034 10803
12	Connector 6 Position BERG #65351-034	5107 259 86921
13	Connector BERG #65625-106	2422 025 0416
14	Main Cable	5107 299 90254
15	Internal Cable	5107 299 81331
16	Lock Washer M3	2522 613 03005
17	Key Switches	5112 291 4329
18	Key Top Set	5112 291 76621
19	Terminal Socket	5107 259 94931
20	Connector Male 6 Position	5107 259 95051
21	Heat Shrink Tubing OD 1/8	5107 200 01311
22	Wire Strp 22AGW White	0722 183 00022
23	Wire 22 AGW Grey	0722 183 00021
24	Wire 22 AGW Yellow	0722 183 00016
25	Wire 22 AGW Red	0722 183 00014
CR1-18	Diode IN4148	5107 259 9905
C4	Cpacitor 390PF 200V ± 10%	5107 259 9562
C2, 3	Capacitor, Tantalum, 10UF 25V 20%	5107 259 9853
C1, 5	Capacitor 0.1UF (BLUE MAX) 50V ± (.1SP)	5107 259 8765
R7	Resistor CF 1KO 1/4W ± 5%	5107 259 9969
R8	Resistor CF 120 OHM 1/4W ± 5%	5107 259 9841
R5, 6	Resistor CF 220 OHM 1/4W ± 5%	5107 259 9959
R2, 3	Resistor CF 330 OHM 1/4W ± 5%	5107 259 9958
R1, 4	Resistor CF 680 OHM 1/4W ± 5%	5107 259 9964
RN1	Resistor Network 22KO BOURNS #4310R-101-223	2122 118 0031
U2	I.C. 74LS14	5107 259 9919
U1	I.C. MK3873	5107 259 9215



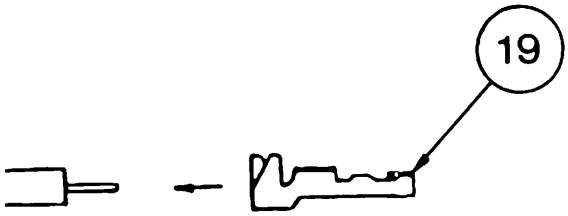


Figure C-4.3

IMPORTANT NOTE:

Modifications needed to Swift Numeric Keypad if 38P73 single chip microcomputer chip with piggy-back EPROM (2716) is used.

- Resistor Pack BOURNS 4310R-101-472 (4.7K)

Connect the Resistor Pack in the following manner:

- PIN 1 of Resistor Pack to PIN 40 of 3873.
- PIN 2 of Resistor Pack to PIN 39 of 3873.
- PINS 3-10 of RESISTOR PACK to PINS 15-8 of 3873 respectively.

Assemble the 2716 EPROM on MK3873 from PIN 3.