Data
Systems

PHILIPS

Field Support Manual
64Kb Memory PCB P5020

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Great care has been taken to ensure that the information contained in this handbook is accurate and complete. Should any errors or omissions be discovered, however, or should any user wish to make a suggestion for improving this handbook, he is invited to send the relevant details to:

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Chapter 1: GENERAL DESCRIPTION

1.1. INTRODUCTION

The 64k Memory PCB, shown in Figure 1-1, contains 64k bytes of dynamic RAM and the associated control logic. The memory is divided into four banks of 16k each, allowing memory mapping to be performed in blocks of 16k.

When this PCB is installed in an M3003 Word Processor System, system memory is expanded from 64k to 128k. Enabling, disabling and mapping functions of the expanded memory are controlled by the CPU located on the System Controller PCB of the word processor system.

1.2. PHYSICAL DESCRIPTION

The PCB measures 10.0 inches by 4.5 inches (254 mm x 114 mm) and has one connector which mates with J1 or J2 of the System Controller PCB. There are no strapping options or switches on the PCB.

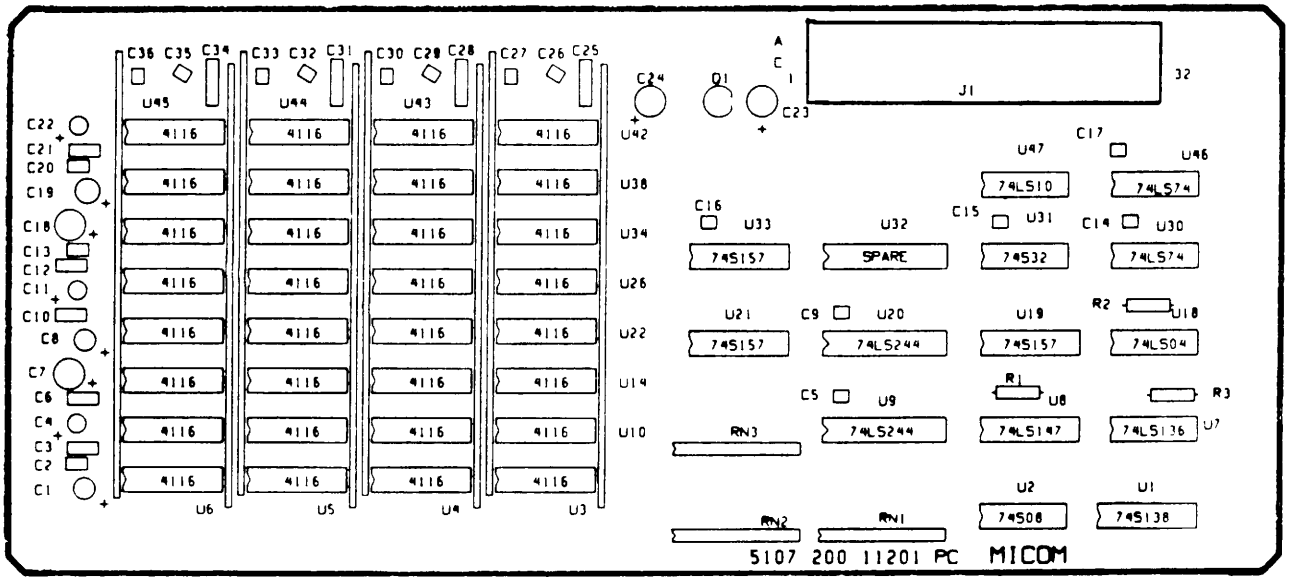


Figure 1-1 64K MEMORY PCB

1.3. TECHNICAL DATA

1.3.1. DIMENSIONS

Length:	10.0" (254 mm)
Width:	4.5" (114 mm)
Height:	0.5" (13 mm)

1.3.2. ELECTRICAL REQUIREMENTS

+5.0V ±10%
+12.0V ±10%
-12.0V ±10%

1.3.3. MEMORY CAPACITY

64k bytes of dynamic RAM divided into four pages of 16k bytes each.

1.3.4. ENVIRONMENTAL

Temperature	
Operating:	0 to +50°C
Non-operating:	-40 to +70°C
Humidity	
Operating:	20 to 80% R.H.
Non-operating:	10 to 90% R.H.

1.4. INTERFACES

The 64k Memory PCB interfaces with the System Controller PCB via J1, shown in Figure 1-1. Pin assignments for J1 are listed in Table 1-1.

Table 1.1 CONNECTOR J1 PIN ASSIGNMENTS

PIN NO.	SIGNAL	
	ROW A	ROW C
1	+5V	+5V
2	GND	GND
3	-12V	+12V
4	Not used	MCLK
5	Not used	Not used
6	CEMMU,L	Not used
7	IEI	Not used
8	Not Used	MSRESET,L
9	GRFSH	Not Used
10	BMREQ,L	MSRFSH,L
11	Not Used	EXMDIS,L
12	BRD,L	Not Used
13	BWR,L	Not Used
14	MSD1	MSD0
15	MSD3	MSD2
16	MSD5	MSD4
17	MSD7	MSD6
18	BA1	BA0
19	BA3	BA2
20	BA5	BA4
21	BA7	BA6
22	BA9	BA8
23	BA11	BA10
24	BA13	BA12
25	BA15	BA14
26	Not Used	Not Used
27	Not Used	Not Used
28	Not Used	Not Used
29	Not Used	Not Used
30	Not Used	Not Used
31	GND	GND
32	+5V	+5V

1.5. APPLICATION NOTES

The 64k Memory PCB is an option to the M3003 Word Processor System.

1.6. INSTALLATION DATA

There are no strapping options or switches on the PCB. Connector J1 of the PCB mates with J1 or J2 of the System Controller PCB. When installed, the PCB is supported by two card guides which are part of the card cage of the word processor system.

Chapter 2: DETAILED DESCRIPTION

2.1. INTRODUCTION

This chapter is divided into three subsections:

- Memory mapping concept;
- Block diagram description;
- Schematic diagram description.

In the following descriptions, the active state of a signal is indicated as follows:

- Active high, no suffix (e.g., INT);
- Active low, L suffix (e.g., INT,L).

2.2. MEMORY MAPPING (Figure 2-1)

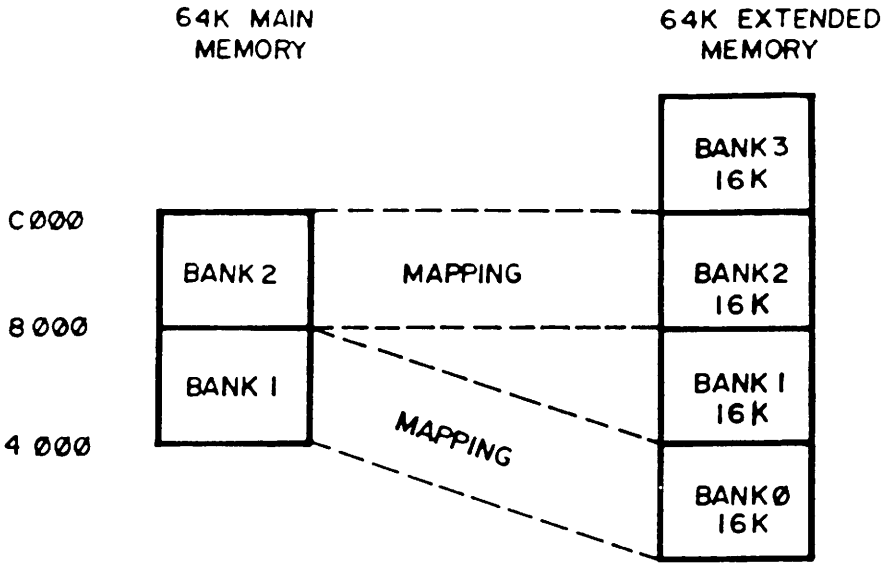
The memory on the 64k Memory PCB can be mapped into the main memory located on the System Controller PCB.

Memory mapping can be performed only on the middle 32k of main memory (banks 1 and 2). Any 16k bank of the extended memory can be mapped into banks 1 or 2 of main memory.

The extended memory is under control of the master CPU on the System Controller PCB, so enabling, disabling and mapping functions are performed by the master CPU. When the extended memory is enabled and accessed the main memory is disabled, and the extended memory only responds to the addressing.

Enabling and mapping is accomplished by a single byte written to I/O port A8H, enabling CEMMU,L. The bit description of the mapping control byte is shown in Figure 2-2. A mapping example is:

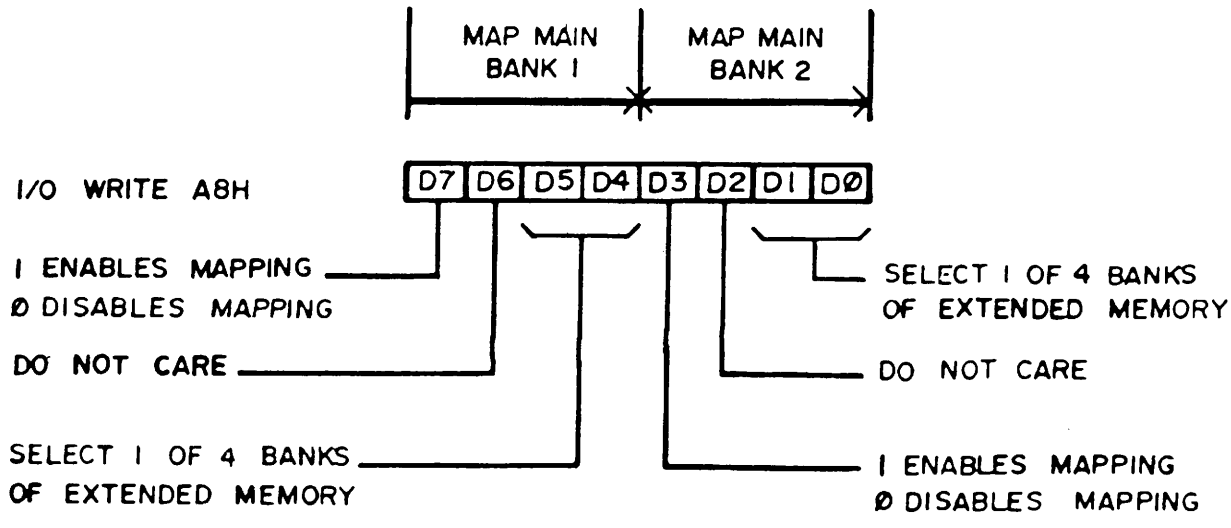
Memory Control Byte = 1001 1010 (9AH)
Result: Bank 2 of extended memory mapped into Bank 2.
Bank 1 of extended memory mapped into Bank 1.



NOTE: ANY BANK OF EXTENDED MEMORY CAN BE MAPPED INTO BANKS 1 OR 2 OF MAIN MEMORY.

M-00447

Figure 2-1 EXTENDED MEMORY MAPPING



M-00448

Figure 2-2 MEMORY CONTROL BYTE

2.3. BLOCK DIAGRAM DESCRIPTION (Figure 2-3)

2.3.1. POWER-ON RESET

When power is first applied to the system the MSRESET,L signal clears the latches, disabling the extended memory.

2.3.2. MEMORY ADDRESSING

The 64k block of memory is divided into four blocks of 16k, each 8 bits wide. To access any one of the 16,384 cells of a memory chip, three inputs to the chip are required:

- Seven address bits (MA0-MA6);
- Row address strobe (RSA0-RSA3) which latches the seven row address bits into the chip;
- Column address strobe (CAS) which latches the seven column address bits into the chip. The column address bits are latched after the row address bits.

To address the memory the CPU performs an I/O operation (CEMMU,L) and a write cycle (BWR,L). The states of MSD0-MSD7, which are used for memory mapping, are thus clocked into the latches. A high on the BA14 line selects the B inputs to the multiplexer (map into main memory bank 2) and a low on BA14 selects the A inputs (map into main memory bank 1). If mapping is enabled (D3 or D6 set), the ENBL signal, in conjunction with the Exclusive-OR of BA14 and BA15 (i.e., Bank 1 or 2), generates MSEL,L which:

- Provides one enable signal to the row address decoder, preparing it to decode D0 and D1 or D4 and D5;
- Enables EMDIS,L which disables the main memory on the System Controller PCB;
- Provides a high to the NAND gate, allowing the MREQ,L line to be activated by BMREQ,L.

With the multiplexer enable latch having been previously reset, the low on the MUX line selects the seven low-order bits on the address bus (BA0-BA6), which are applied to the memory chips on the address bus.

When the BMREQ,L line is activated, indicating that the address bus holds a valid address, the MREQ,L signal is activated and is clocked into the memory request latch by the first MCLK pulse (20 MHz). This provides the other enable signal for the row address decoder, allowing it to produce a row address strobe, which latches the row address bits into the correspo g row of memory chips.

The next MCLK pulse sets the multiplexer enable latch. The high on the MUX line causes the multiplexers to put the seven high-order bits (BA7-BA13) on the address bus to the memory chips. The next MCLK pulse resets the column address latch and the column address strobe latches the column address bits into the memory chips. With the row and column address bits now latched into memory, the particular row of cells (8) is accessed.

When the BMREQ,L signal goes high again, the memory request latch is set, the multiplexer enable latch is reset, and the column address latch is set.

2.3.3. DATA TRANSFER

For a data transfer operation to take place, the particular memory location must have been addressed, as described above.

For a write operation, the MUX,L signal and the BWR,L signal generate the WEN,L signal, which is the write line to the memory chips. Thus, the data on the data bus is written into the addressed memory location.

For a read operation, the MUX,L signal and the BRD,L signal generate the BUFEN,L signal, which enables the buffer drivers. Thus, the data from the addressed memory location is transferred to the MSD0-MSD7 lines.

2.3.4. MEMORY REFRESH

Clock states T3 and T4 of each fetch cycle are used for refreshing the dynamic memory. This is performed automatically by the CPU, by performing a memory cycle at each of the 128 row addresses ($2^6 = 128$).

A low on the MRFSH,L line disables the NAND gate, preventing the MREQ,L signal from being enabled. As the multiplexer enable latch was reset at the end of the last operation (by BMREQ,L), the low MUX signal routes the seven low-order address bits (BA0-BA6) through the multiplexers to the address ports of the memory chips. These seven bits are the row address. With the address bits

stablized, the low GRFSH,L signal to the row address strobe gates produces the four row address strobes (RAS0-RAS3). This refreshes the row that is addressed. Each row is refreshed, in sequence, during clock states T3 and T4 of the fetch cycles.

2.4. SCHEMATIC DIAGRAM DESCRIPTION

Refer to the schematic diagram provided in Chapter 3. Timing is shown in Figure 2-4.

2.4.1. MEMORY MAPPING

For a description of the memory mapping concept used refer to Paragraph 2.2.

2.4.2. POWER-ON RESET

When power is first applied to the system, the MSRESET,L signal clears the latches of U8, forcing the outputs low.

2.4.3. MEMORY ADDRESSING

The 64k of memory is divided into four banks of 16k, each 8 bits wide. To access any one of the 16,384 cells of a memory chip, three inputs to the chip are required:

- Seven address bits (MA0-MA6);
- Row address strobe (RAS0-RAS3) which latches the seven row address bits into the chip;
- Column address strobe (CAS) which latches the seven column address bits into the chip. The column address bits are latched after the row address bits.

To address the memory the CPU performs an I/O operation at A8H to activate CEMMU,L and performs a write cycle to activate BWR,L. This enables U31 which clocks the memory mapping bits into the latches of U8 (the memory mapping bits on the MSD0-MSD7 lines are routed to U8 via the line receivers of U9).

Multiplexer U19 selects either the A inputs or the B inputs, depending upon the state of BA14 (a low on BA14 selects the A inputs; a high selects the B inputs). On the inputs the B0 and B1 bits select one of four banks and the E

inputs are for enabling/disabling mapping, as shown in Figure 2-2. If mapping is enabled, the ENBL signal, in conjunction with the Exclusive-OR of BA14 and BA15 (i.e., Bank 1 or 2), generates MSEL,L which:

- Provides one enable input to decoder U1;
- Activates EMDIS,L which disables the main memory on the System Controller PCB;
- Provides a high to U47.

At this time, flip-flops U30-5 and U46-5 are set, and U30-9 is reset. Thus, the low on the MUX line selects the low-order bits (BA0-BA6 and VH) to multiplexers U21 and U33, and these bits are applied to the address inputs (MA0-MA7) of the memory chips. These bits are the row address.

When the BMREQ,L signal is activated, indicating that the address bus holds a valid address, the MREQ,L signal is activated and resets U30-5 on the first clock pulse. The low from U30-5 provides the second enable input to decoder U1 and the two bank select bits on the A and B inputs are decoded to produce a row address strobe (RAS0-RAS3). This strobe latches the row address bits into the corresponding row of memory chips.

The next MCLK pulse clocks the high from U30-6 into U30-12. This causes the MUX line to go high to select the high order address bits (BA7-BA13) at multiplexers U21 and U33, and these inputs are applied to the address inputs (MA0-MA7) of the memory chips. These bits are the column address.

The next MCLK pulse clocks the low from U30-8 into U46-2. This causes the RCAS,L line to go low, producing the low CAS,L signal, which is the column address strobe. This latches the column address bits into the memory chips. With the row and column address bits now latched into the memory chips, the appropriate row of cells (8) is accessed.

When the BMREQ,L line goes high again, U30-5 and U46-5 are set and U30-9 is reset.

2.4.4. DATA TRANSFER

For a data transfer operation to take place, the particular memory location must have been addressed as described above.

For a write operation, the data on the MSD0-MSD7 lines is applied, via U9, to the IN ports of the memory chips. A write cycle enables BWR,L which, in conjunction with the low MUX,L signal, causes write enable signal WEN,L to go low. Thus, the data is written into the eight memory cells that have been addressed.

For a read operation, the read cycle causes BRD,L to go low and, in conjunction with the low MUX,L signal, causes U31-6 to go low. The BUFEN,L signal enables data line driver U20, connecting the memory OUT ports to the MSD0-MSD7 lines. Thus, the data from the eight memory cells that have been addressed is read.

2.4.5. MEMORY REFRESH

Clock states T3 and T4 of each fetch cycle are used for refreshing dynamic memory. This is performed automatically by the CPU, by performing a memory cycle at each of the 128 row addresses (2^6 = 128).

A low on the MRFSH,L line disables gate U47-4. As flip-flop U30-9 was reset at the end of the previous operation, the low MUX signal routes the seven row address bits (BA0-BA6) through receivers U21 and U33 to the address lines of the memory chips (MA0-MA6). With the address bits stabilized, the GRFSH line goes high to produce a low GRFSH,L signal which, in turn, generates four row address strobes (RAS0-RAS3). This refreshes the row that is addressed (1 of 128). Each row is refreshed, in sequence, during clock states T3 and T4 of the fetch cycles.

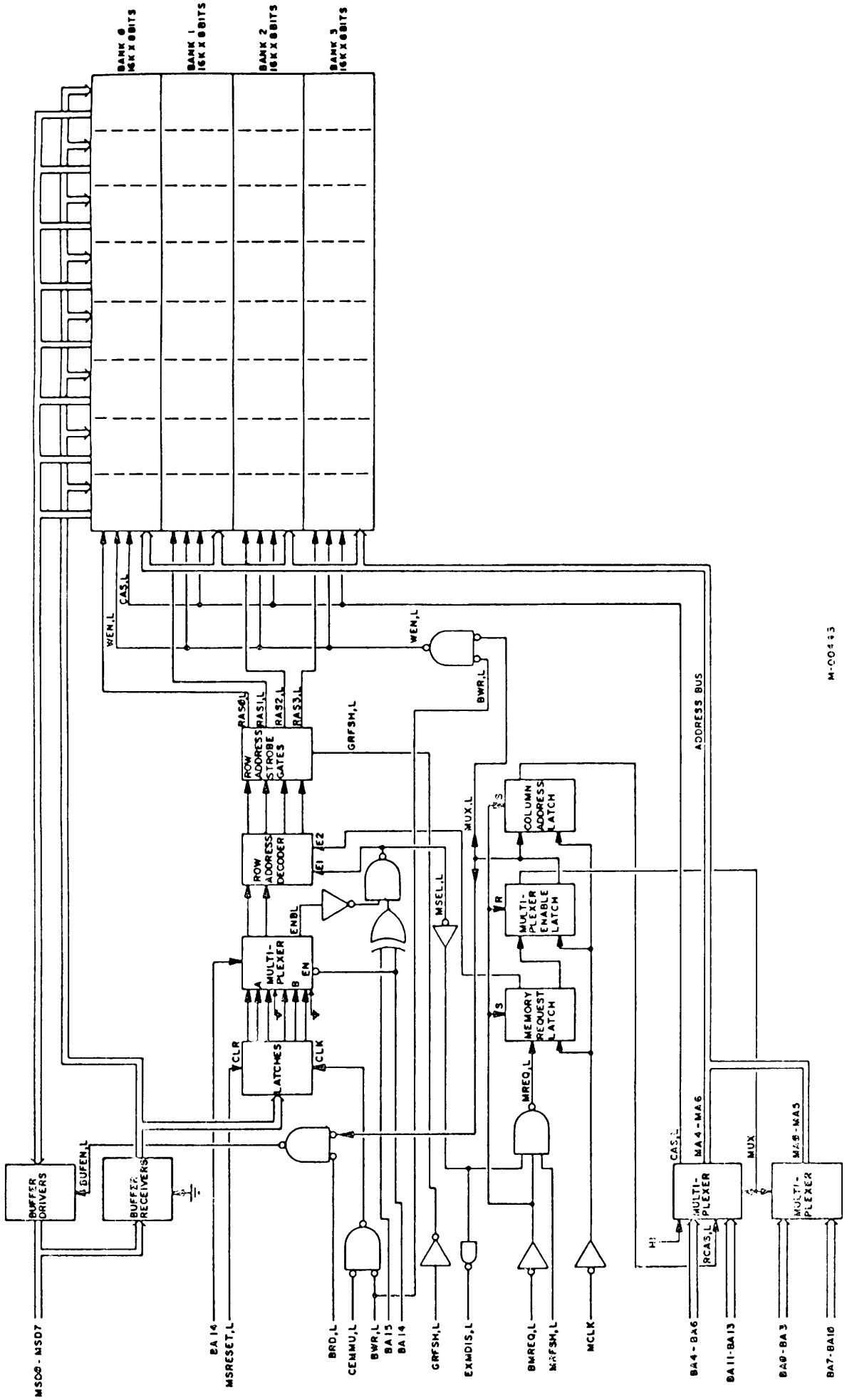


Figure 2-3 64K MEMORY PCB BLOCK DIAGRAM

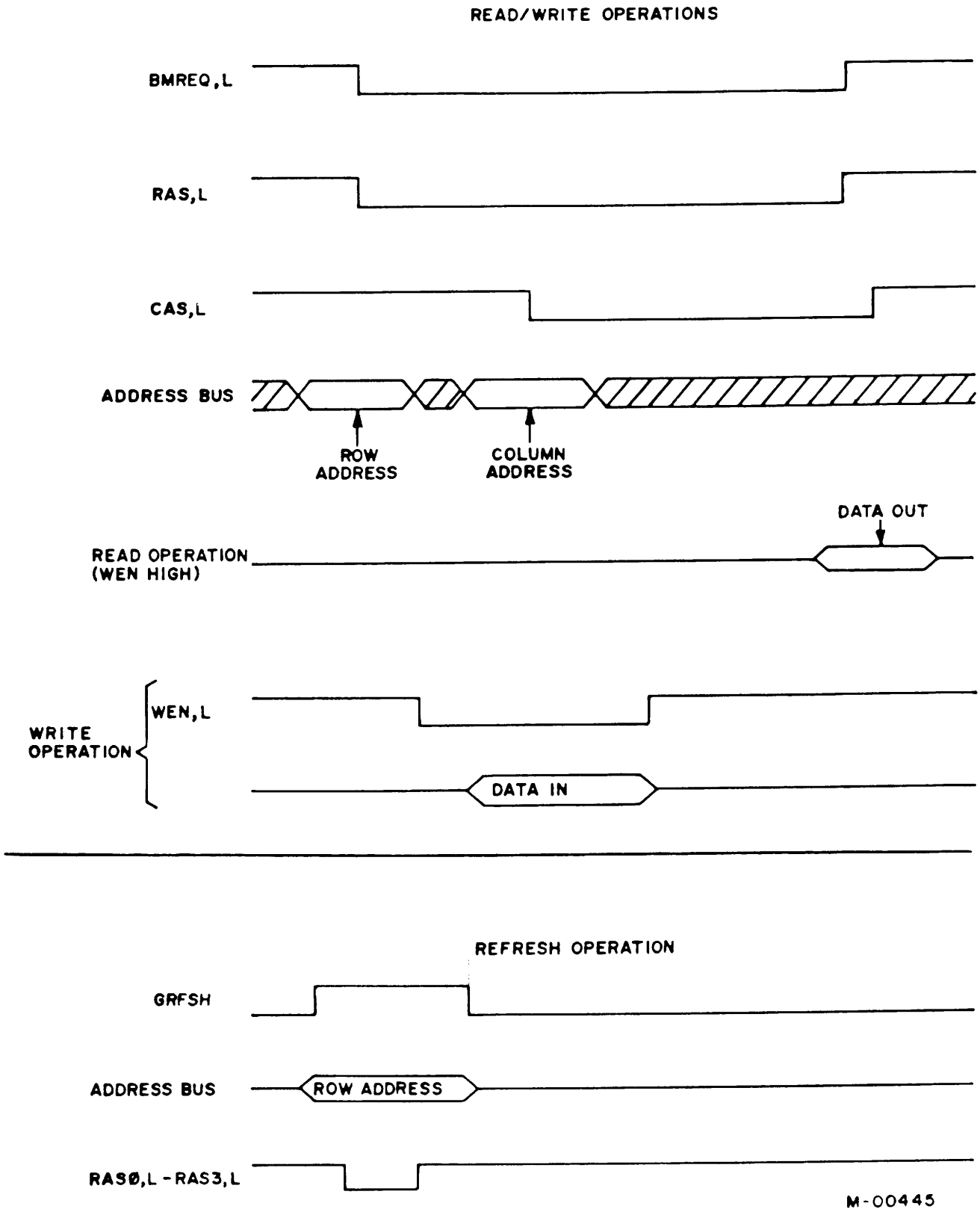


Figure 2-4 TYPICAL MEMORY TIMING

Chapter 3: DIAGRAMS

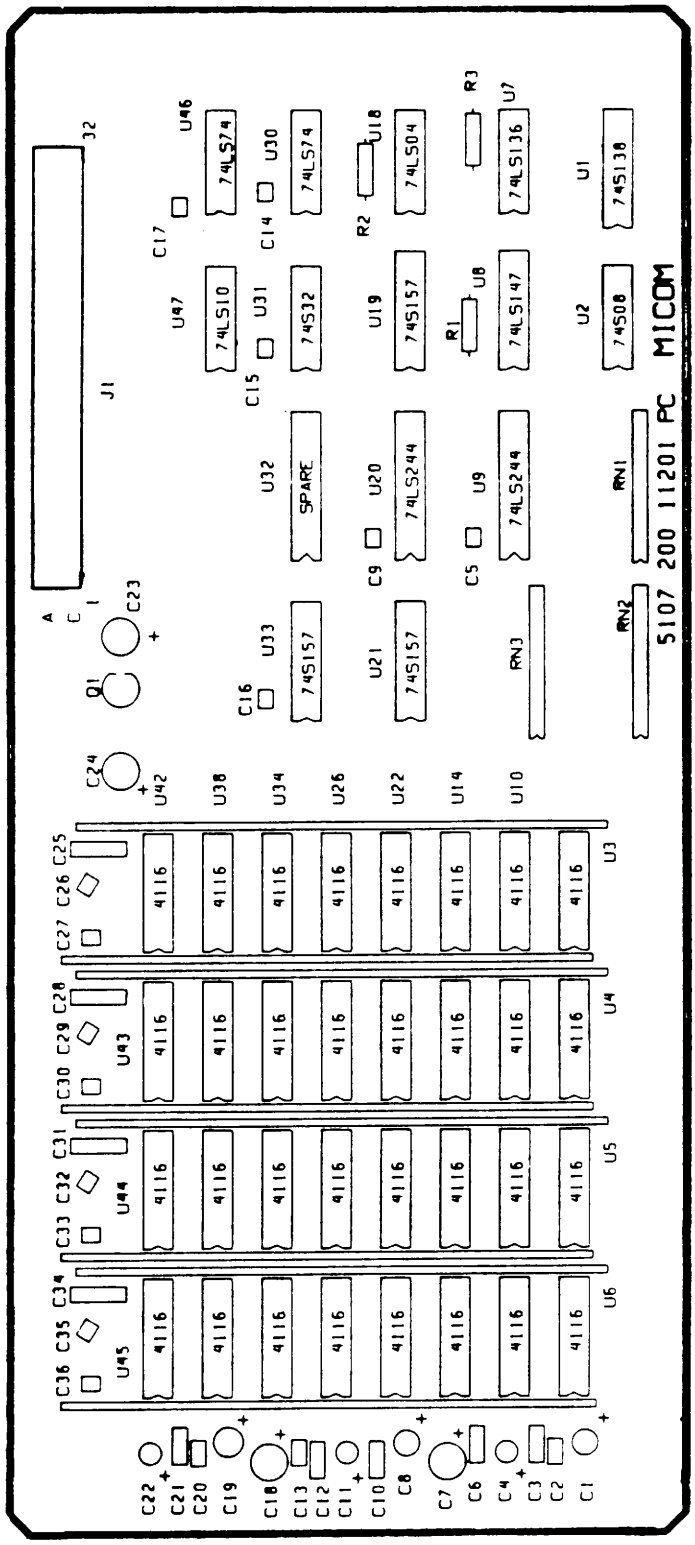
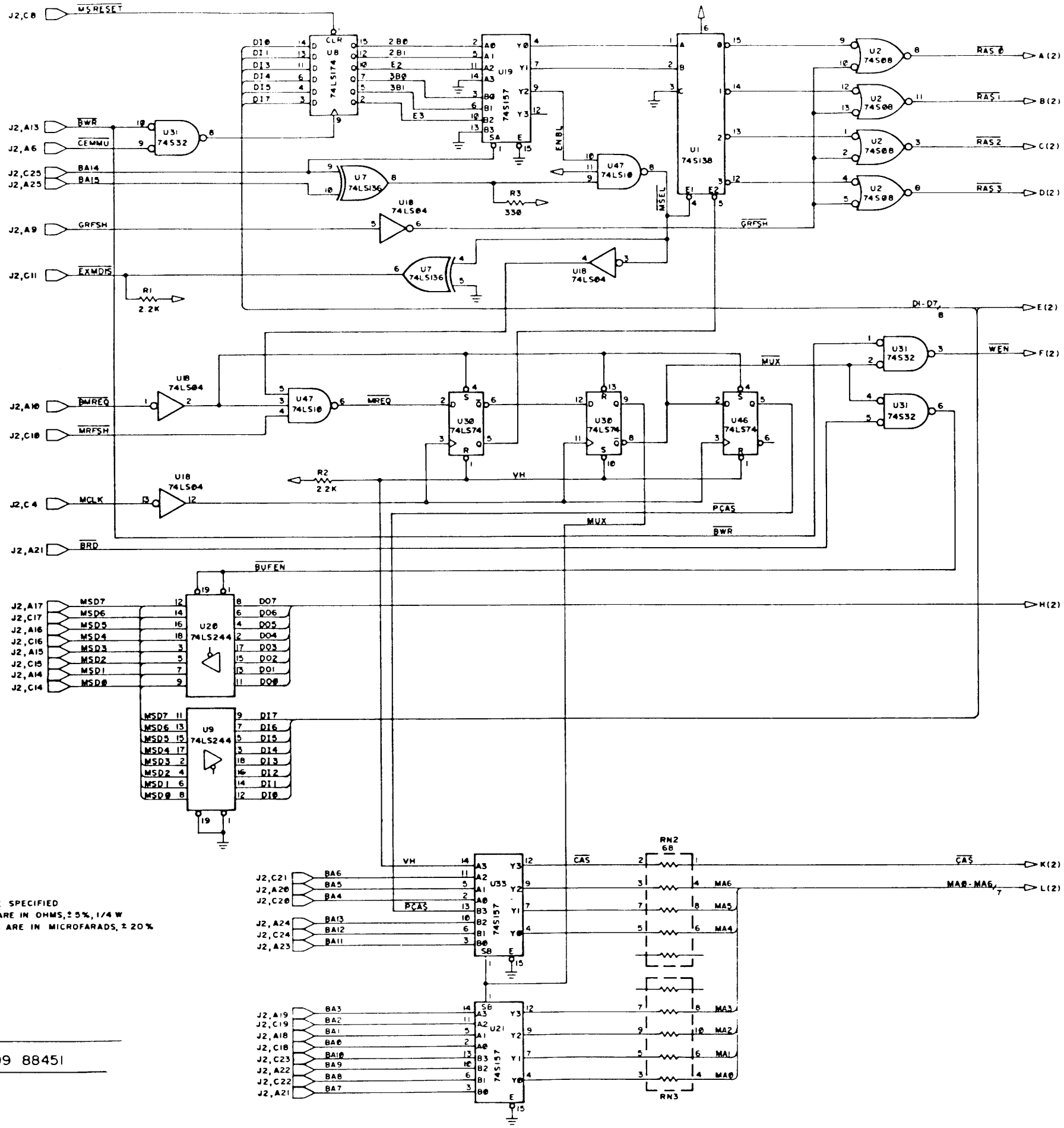


Figure 3-1 64K MEMORY PCB COMPONENT LAYOUT

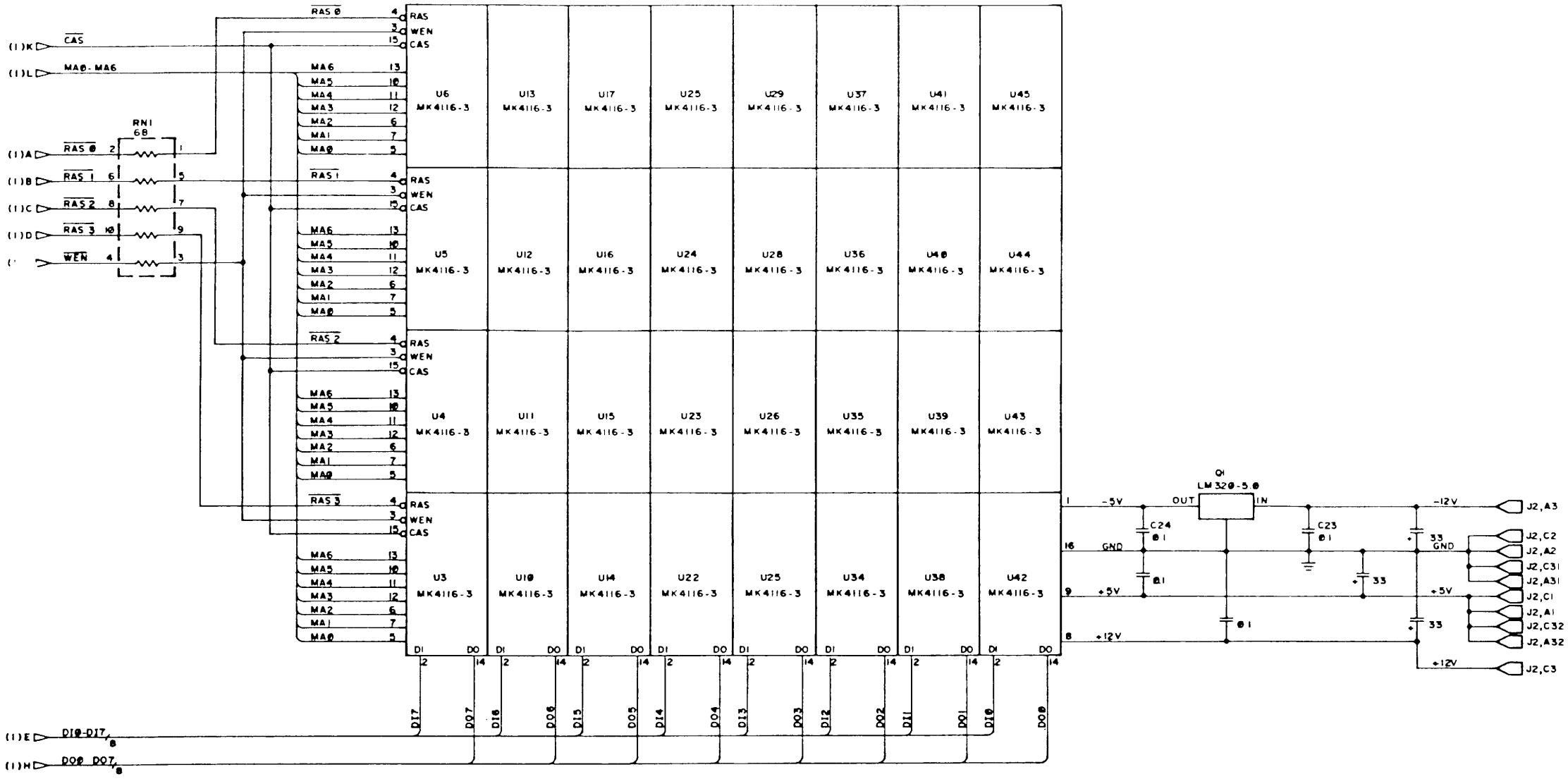


NOTES:

1 UNLESS OTHERWISE SPECIFIED
RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4 W
CAPACITOR VALUES ARE IN MICROFARADS, ± 20%

DRAWING NO
5107 299 88451

Figure 3-2 64K MEMORY PCB SCHEMATIC DIAGRAM (Sheet 1 of 2)



DRAW NO. MK
5107 299 88451

Figure 3-2 64K MEMORY PCB SCHEMATIC DIAGRAM (Sheet 2 of 2)

Chapter 4: PARTS LIST

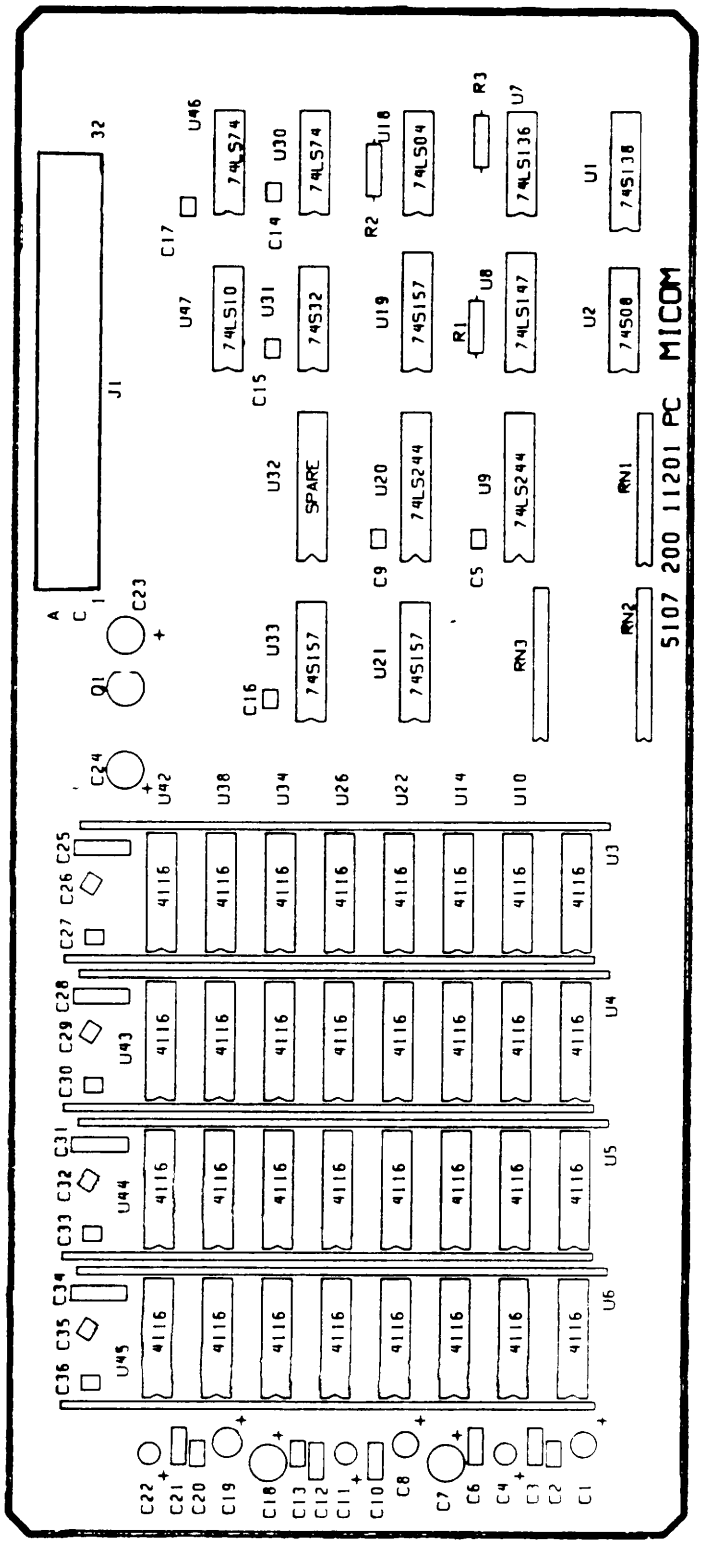


Figure 4-1 64K MEMORY PCB COMPONENT LAYOUT

4.1. GENERAL

This chapter provides a list of all replaceable parts for the 64k Memory PCB. For component locations refer to Figure 4-1.

Table 4.1 64K MEMORY PCB REPLACEABLE PARTS

REF DES	12NC PART NUMBER	DESCRIPTION
	5107 299 88451	64k Memory PCB (complete)
C1,C4,C7,C8, C11,C18,C19, C22,C23,C24.	5107 259 89991	Capacitor, Tantalum, 33 uF, 20V, ±20%.
C2,C3,C5,C6, C9,C10,C12-C17, C20,C21,C25-C36.	5107 259 95401	Capacitor, Ceramic, 0.1 uF, 50V, ±20%.
Q1	5107 259 94391	IC, Regulator, LM320L-5.0
R1	5107 259 99661	Resistor, 2.2K, 1/4W, ±5%
R2	5107 259 99661	Resistor, 2.2K, 1/4W, ±5%
R3	5107 259 99581	Resistor, 330 ohm, 1/4W, ±5%
RN1	5107 259 91121	Resistor Network, 68 ohm
RN2	5107 259 91121	Resistor Network, 68 ohm
RN3	5107 259 91121	Resistor Network, 68 ohm
U1	5107 259 93491	IC, 74S138
U2	5107 259 94541	IC, 74S08
U3-U6	5107 259 99901	IC, 4116-3 RAM, 200 nS
U7	5107 259 89391	IC, 74LS136
U8	5107 259 99101	IC, 74LS174
U9	5107 259 99321	IC, 74LS244
U10-U17	5107 259 99901	IC, 4116-3 RAM, 200 nS
U18	5107 259 99211	IC, 74LS04
U19	5107 259 96001	IC, 74S157
U20	5107 259 99321	IC, 74LS244
U21	5107 259 96001	IC, 74S157

Table 4.1 64K MEMORY PCB REPLACEABLE PARTS (Cont'd)

REF DES	12NC PART NUMBER	DESCRIPTION
U22-U29	5107 259 99901	IC, 4116-3 RAM, 200 nS
U30	5107 259 99411	IC, 74LS74
U31	5107 259 93321	IC, 74S32
U32		Not Used
U33	5107 259 96001	IC, 74S157
U34-U45	5107 259 99901	IC, 4116-3 RAM, 200 nS
U46	5107 259 99411	IC, 74LS74
U47	5107 259 98851	IC, 74LS10
J1	5107 259 93951	Connector, 64-pin

Chapter 5: TROUBLESHOOTING & REPAIR

5.1. GENERAL

This chapter provides troubleshooting and repair instructions for the 64k Memory PCB. The troubleshooting procedures apply when the PCB is installed in a console.

5.2. TOOLS AND MATERIAL REQUIRED

- Standard Tool Kit
- WP Diskette
- Functional Field Test Program Diskette
- Storage Oscilloscope (or dual-channel)

5.3. TROUBLESHOOTING

These procedures apply when the troubleshooting will be performed with the PCB installed in a console. All other assemblies of the console (power supply, System Controller PCB, etc.) must be fully operational.

Troubleshooting should be performed in the following sequence:

- Power check;
- Fault isolation to a particular circuit;
- Troubleshooting of the defective circuit.

Reference must be made to the assembly drawing and schematic diagram, which are located in Chapter 3.

5.3.1. POWER CHECK

The PCB receives external sources of +5V, +12V and -12V.

- The voltage at J1-A1 must be +5V ±10%.
- The voltage at J1-A3 must be -12V ±10%.
- The voltage at J1-C3 must be +12V ±10%.
- The voltage at Q1-OUT must be -5.0V ±10%.

5.3.2. FAULT ISOLATION

Faults are isolated using the memory test of the Functional Field Test Program, which is presently being developed. Details on how to use the memory test will be provided when the diskette is available.

When a fault has been isolated, troubleshoot the defective circuit as described in Paragraph 5.3.3.

5.3.3. CIRCUIT TROUBLESHOOTING

Once the fault has been isolated to a functional block of circuitry, the component at fault must be isolated using conventional troubleshooting methods. In order to troubleshoot individual circuits, Field Support Personnel must be completely familiar with the circuit theory described in Chapter 2. The PCB schematic diagram is included in Chapter 3 and pertinent waveforms are given in Chapter 2.

5.4. REPAIR

5.4.1. REPAIR PRECAUTIONS

When repairing the PCB the following precautions must be observed.

- Never repair the PCB with power applied.
- When soldering, use only a soldering iron which has a properly grounded soldering tip. A soldering iron which has AC on the soldering tip will cause extensive damage to IC's.
- Only use a low-wattage soldering iron.
- A soldering iron must not be held in contact with the PCB solder point any longer than necessary. Excess heat can damage the IC's. Use a "solder sucker" to remove melted solder.
- Perform a visual inspection of all repairs. After soldering, check for solder shorts between pins and tracks adjacent to the repair. Check for cold solder joints.

5.4.2. POST-REPAIR TESTING

After a PCB has been repaired, it should be checked for proper operation by running the memory test of the Functional Field Test Program and then by loading the WP Program and checking for correct operation.