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pp: 1 : 22
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RC 35-201
Interface between RC 3500 and RC 500 Paper Tape Reader
PTI 100-00,01
TECHNICAL MANUAL

Keywords: RC 3500 Interface, Paper Tape Reader, PTI 100-00,01,
Technical Manual.

Abstracts: This paper is a Technical Description of an interface
between RC 3500 and RC 500 Paper Tape Reader. General
Information RCSL: 52-AA070.

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GENERAL INFORMATION	RCSL: 52-AA070	
FUNCTIONAL DESCRIPTION		5
Line Receiver and Demodulator		5.1
Line Driver and Modulator		5.2
DATA OUT Register and HEADER Decoder		5.3
DATA IN/STATUS Register and Header Generator		5.4
CONTROL Logic to the Reader		5.5
INTERRUPT CIRCUIT		5.6
Clock Oscillator		5.7
JACK LIST J1	Dwg. No. A22837	6
Kabeltype CBL 10	Dwg. No. A22102	
TIMING CHARTS		7
TC 1	Dwg. No. A11957	
TC 2	Dwg. No. A11958	
CIRCUIT DIAGRAMS		8
PTR 1	Dwg. No. A11578	
PTR 2	Dwg. No. A11579	
PTR 3	Dwg. No. A11580	
PTR 4	Dwg. No. A11581	
Signal List		8.1
PTR 1	Dwg. No. A22838	
PTR 2	Dwg. No. A22839	
PTR 3	Dwg. No. A22840	
PTR 4	Dwg. No. A22841	

pp. 1 :

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CONTENTS

SHORT DESCRIPTION	1.0
GENERAL DESCRIPTION	2.0
Tape Loading Procedure	2.1
CONVENTIONS FOR TRANSMISSION BETWEEN RC 3500 AND RC 35-201	3.0
Write Control	3.1
Write Data	3.2
Read Data	3.3
Read Status	3.4
INSTALLATION	4.0
FIG. 1	A 11599

pp. 1 : 8

The RC 35-201 (Paper Tape Reader) interface is connected to one I/O channel on RC 3500.

The RC 35-201 interface covers interconnection requirements between RC 500 Paper Tape Reader and RC 3500.

The RC 500 is a photo-electric Reader developed to read 8-track paper tape with a nominal speed of 500 characters per second.

Physically the RC 35-201 interface is placed in the interface position inside the RC 500 cabinet and power supplied from the Reader.

For details about operation of RC 500 refer to the General Information for RC 500 (RCSL: 52-AA318).

For details refer to Block diagram Fig. 1.

The RC 35-201 interface sends a CHREQ (Character Request) signal when a character is wanted. During initializing the first CHREQ is set by operating the RESET button on the operator panel of the Reader.

The Reader responses a CHREQ signal with the signal CHR (Character Ready) when a character is ready in the output register of the Reader.

The signal CHR causes an interrupt to be sent to RC 3500. RC 3500 answers the interrupt with a READ DATA command to get the character in question. After this character is transmitted to RC 3500 a new CHREQ pulse is sent to the READER requesting a new character.

In the situation:

- (1) there is no paper tape in the reader (PTP = 0) and
- (2) the buffer in the Reader is empty (ZFB = 1)

The signal READER READY = 0 is generated to block interrupt transmission to RC 3500.

By means of WRITE CONTROL commands RC 3500 forces the interface to send an interrupt if READER READY = 1 and a character is ready from the Reader ($\bar{Z}$, CHR = 0).

Tape Loading Procedure.

2.1

1. Push RESET-button on the reader.
2. Set the STOP/RUN switch on the operator panel on RC 3500 in RUN-position.
3. Push READ-button on the Reader.

or:

1. Push RESET-button on the Reader.
2. Push READ-button on the Reader.
3. Set the STOP/RUN switch on the operator panel on RC 3500 in RUN-position.

CONVENTIONS FOR TRANSMISSION BETWEEN RC 3500 AND RC 35-201.

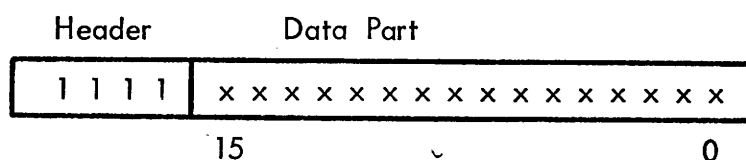
3.0

The RC 35-201 interface accepts all commands (WRITE CONTROL, WRITE DATA, READ DATA and READ STATUS) from RC 3500 but WRITE DATA has no effect on the operation of the RC 35-201 interface.

WRITE CONTROL

3.1

From RC 3500 to RC 35-201



bit 15 -: Not used.

bit 0

Decoding of a WRITE CONTROL header causes the RC 35-201 interface to send an interrupt to RC 3500 if READER READY = 1 (section 3.4) and a character is ready from the Reader.

WRITE DATA

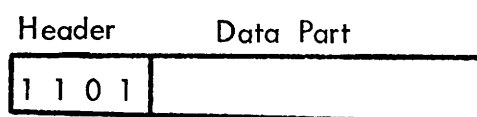
3.2

Not used in the RC 35-201 interface.

READ DATA

3.3

From RC 35-201 to RC 3500.



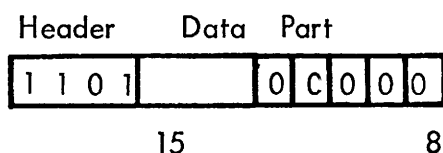
bit 15 -: Data Character.

bit 8 bit 15 - bit 8 corresponds to track 1-8 on the paper tape.
A hole on the paper tape results in a logic 1 in the Read Data Word.

READ STATUS

3.4

From RC 35-201 to RC 3500.



bit 15: Power OK.

bit 14: READER READY.

bit 14 = 1 if there is paper tape in the Reader
(PTP = 1) or
the buffer in the Reader is not empty (ZFB = 0).

bit 14 = 0 if PTP = 0 and ZFB = 1.

bit 13: EOI

bit 13 is set to logic 1 when bit 14 (READER READY)
shifts to logic 0.

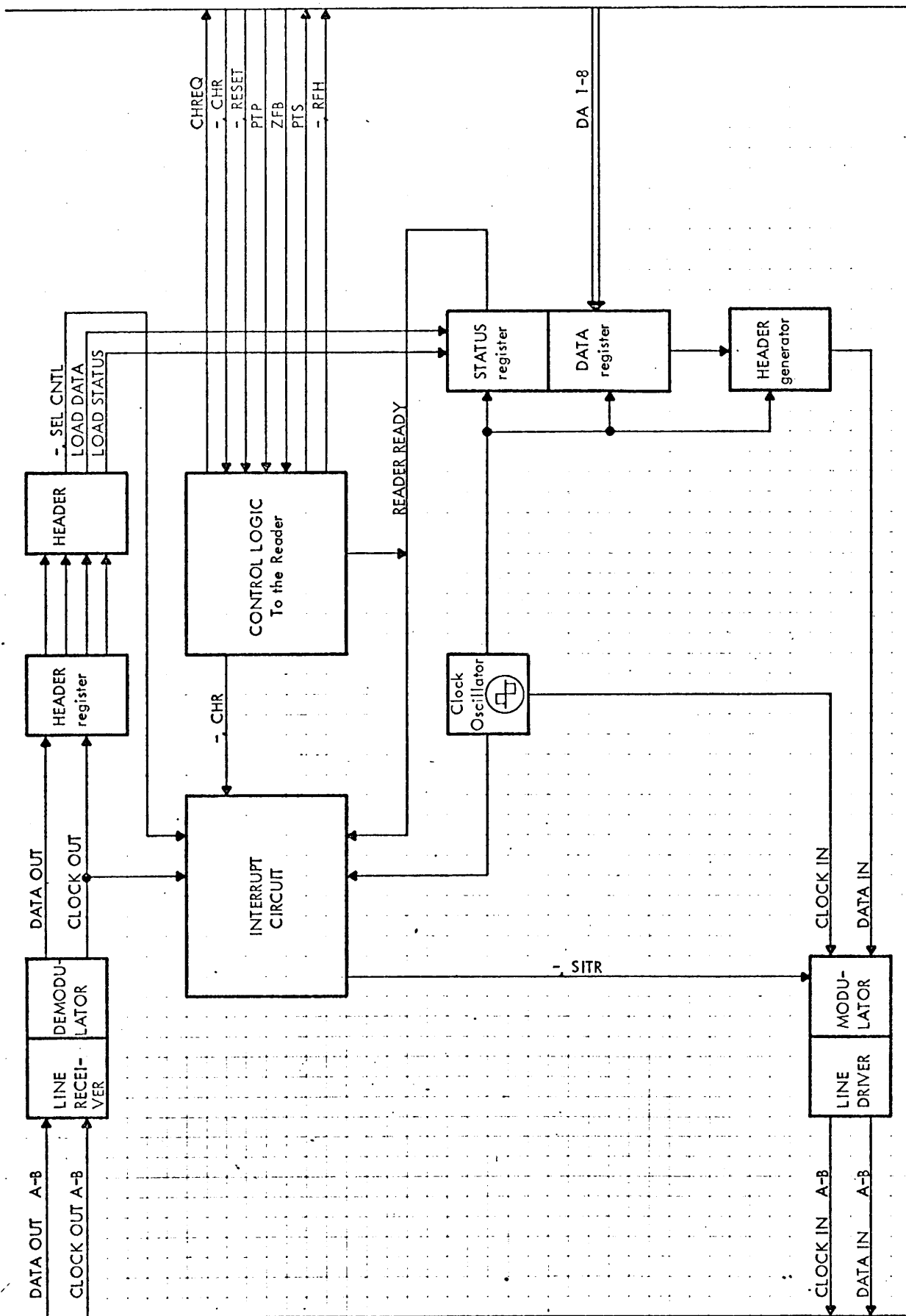
bit 13 is set to logic 0, when a Read Status
header is decoded in the interface.

bit 12 -

bit 8: logic 0.

Cable CBL 12 is used to connect the interface circuit board with the output connector internal in RC 500. The length of Cable CBL 12 is 0,20 m.

Cable CBL10 is used to connect RC 500 and RC 3500. The max. length of Cable CBL10 is 100 m.



For details refer to the block diagram, fig. 1.

Line Receiver and Demodulator.

5.1

For details refer to PTR 1.

Two balanced signals are received from RC 3500, serial data on DATA OUT A-B and clock on CLOCK OUT A-B.

By using transformer coupling, galvanic separation is obtained between RC 3500 and the PTI 100 interface.

In the demodulator the serial data stream is synchronized with the received clock, so a shift from logic 1 to logic 0 on DATA OUT corresponds to a trailing edge on CLOCK OUT.

Line Driver and Modulator.

5.2

For details refer to PTR 1.

In the modulator the serial data (DATA IN) and the interrupt signal are mixed, because an interrupt is sent as a logic 1 element on the data lines DATA IN A-B.

RC 3500 decodes a logic 1 on CH DAT A-B as an interrupt whether moment an input instruction (READ STATUS, READ DATA) is not in progress on the interrupt level in question.

The internal clock CLOCK IN is sent to RC 3500 on the lines CLOCK IN A-B.

DATA OUT Register and HEADER Decoder.

5.3

For details refer to PTR 2, TC 1 and TC 2.

The serial data received on DATA OUT is shifted into the DATA OUT register. The DATA OUT register is an 8-bit serial to parallel register.

When the first synchronization bit in the Header is recognized in the bottom of the register, the shift clock is stopped and the Header is decoded in accordance with the following table:

Command	Header				Strobe Pulse
	1	x_1	x_0	1	
WRITE CONTROL	1	1	1	1	$\overline{7}$ SEL CNTL
WRITE DATA	1	0	1	1	not used
READ DATA	1	0	0	1	$\overline{7}$ LOAD DATA
READ STATUS	1	1	0	1	LOAD STATUS

First bit on DATA OUT

The strobe pulses generated in accordance with the table above are 100 ns. pulses synchron with the internal clock CLOCK IN.

DATA IN/STATUS Register and Header Generator.

5.4

For details refer to PTR 3, TC 1, and TC 2.

This register is a 12-bit parallel to serial shift register (8 data bits + 4 header bits).

If a READ DATA header is decoded, the strobe pulse LOAD DATA (section 5.3) loads the register with the information on the parallel data inputs from the Reader (DA 1-8).

If a READ STATUS header is decoded, the strobe pulse LOAD STATUS (section 5.3) loads the register with status information (Power OK, READER READY). The header used to Read Data word and Read STATUS word is:

1 0 1 1 → Direction of Transmission.

The contents of the register + header generator are shifted serially to the modulator by CLOCK IN.

For details refer to PTR 4 and TC 1.

Before loading the Reader with a paper tape, the operator pushes the RESET button on the front panel of the Reader, generating the $\overline{\text{RESET}}$ signal. $\overline{\text{RESET}} = 0$ forces the CHREQ-FF to logic 1-state (CHREQ = 1).

Now the operator loads the Reader with a paper tape, indicated by PTP (Paper Tape Permit) = 1 causing the signal READER READY to switch to logic 1. When at least one character is read into the Reader-Buffer, the signal ZFB (Zero From Buffer) shifts to logic 0. When a character is ready from the Reader-Buffer to the RC 35-201 interface, the Reader shifts the signal $\overline{\text{CHR}}$ ($\overline{\text{CHR}}$, Character Ready) to logic 0. RC 3500 sends a READ DATA command to pick up the character in question.

When the Read Data header is decoded, the strobe pulse $\overline{\text{LOAD DATA}}$ clears the CHREQ-FF. About 4 μs . after the Read Data word is transmitted to RC 3500, the CHREQ-FF is set again to request a new character.

The signal $\overline{\text{RFH}}$ ($\overline{\text{RFH}}$, Read Feed Holes) is controlled by a switch on the interface printed circuit board.

In the ON-position ($\overline{\text{RFH}} = 0$) the Reader accepts the code with no holes in track 1-8 on the paper tape (only feed hole) as a character. In the OFF-position ($\overline{\text{RFH}} = 1$) the Reader only accepts codes on the paper tape with at least one hole in track 1-8.

When there is no more paper tape in the Reader (PTP = 0) and the Reader-Buffer is empty (ZFB = 1), the signal READER READY switches to logic 0.

INTERRUPT CIRCUIT.

5.6

For details refer to PTR 4, TC 1, and TC 2.

Whenever data is received from RC 3500 (CLOCK OUT) is pulsed a monostable circuit is started to block transmission of interrupts. This

monostable runs 7 μ S. after the last CLOCK OUT pulse to secure that the data word to RC 3500 as response to an input instruction (READ DATA or READ STATUS) is transmitted before enabling interrupt transmission.

The negative going edge of $\overline{\text{CHR}}$ will set the Dev Itr FF (ICB 17) if $\text{READER READY} = 1$; if the monostable circuit mentioned above is terminated, a 100 nS. pulse $\overline{\text{SITR}}$ is generated to the modulator.

If a WRITE CONTROL header is decoded, the signal $\overline{\text{SEL CNTL}}$ (section 5.3) will set the Dev. ITR FF (ICB 17), if $\text{READER READY} = 1$ and $\overline{\text{CHR}} = 0$, and the pulse $\overline{\text{SITR}}$ as mentioned above is generated again.

Clock Oscillator.

5.7

For details refer to PTR 2.

The clock oscillator delivers the internal clock signal, CLOCK IN (4.9152 MHZ).

J
ITT Cannon, type DEC - 95

PIN	GEN. ADR.	SIGNAL NAME
1		CLOCK IN A
2		CLOCK IN B
3		DATA IN A
4		DATA IN B
5		
6		CLOCK OUT A
7		CLOCK OUT B
8		DATA OUT A
9		DATA OUT B

DBSL: 062

PTI 100

A22837

Jack for Connection to RC 3500

Jacklist

J 1

Replaced by Dwg. No.

Due to EGN

Replaces Dwg. No.

Design Check

Dwg. Office Check

Drawn by

Designed by

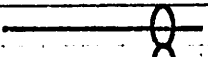
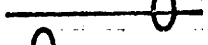
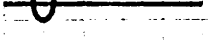
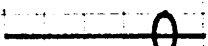
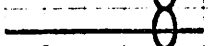
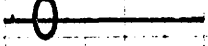
A/S REGJECENTRALEN

730907 KNEH 730910 IGH

CONNECTOR I : Canon Plug DE - 9 P

CONNECTOR II : Canon Plug DE - 9 P

CABLE : 6 x 2 x 0,25 mm² Datwyler 2783

I PIN	WIRE	II PIN
1	 blå	1
2	 hvid	2
3	 gul	3
4	 hvid	4
5		5
6	 brun	6
7	 hvid	7
8	 grå	8
9	 hvid	9
10		10
11		11
12		12
13		13
14		14
15		15
16		16
17		17
18		18
19		19
20		20
21		21
22		22
23		23
24		24
25		25

Unit

Dwg. No.

A22102

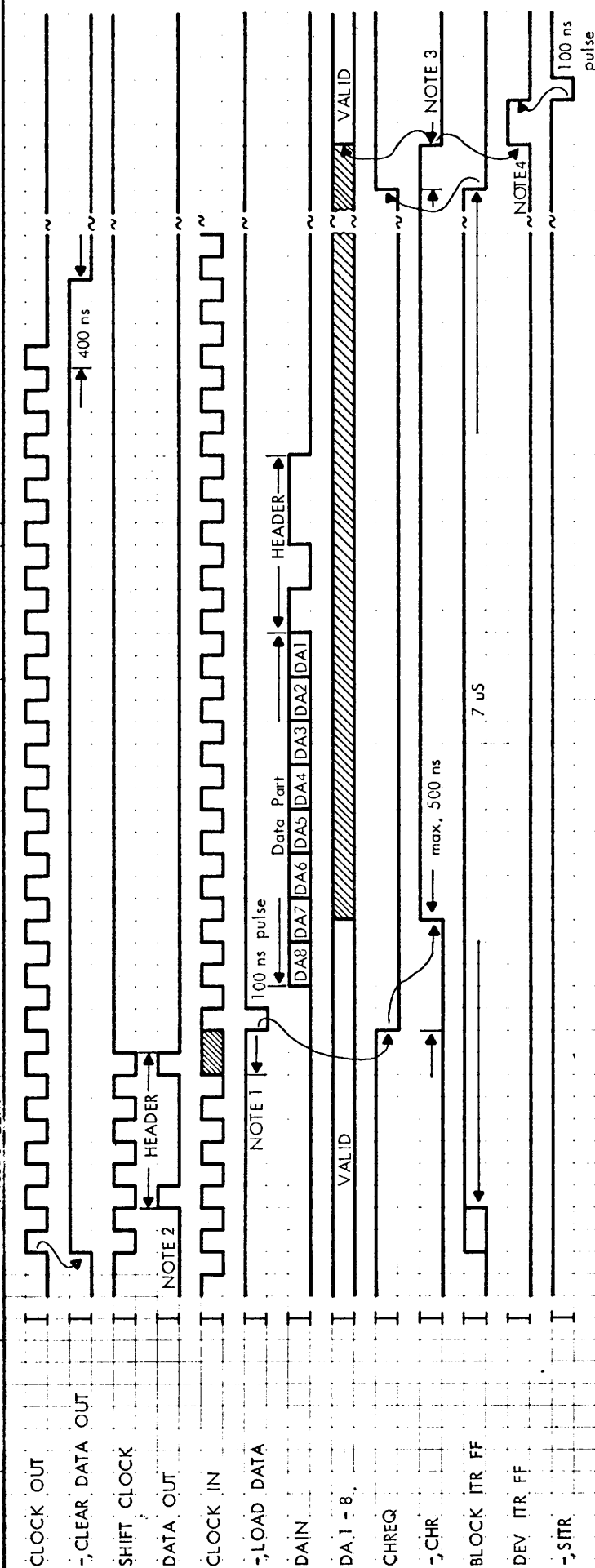
Kabeltype 10 / m
CBL 10

A/S REGNENTRALEN	Designed by 730306 KNEH	Drawn by 740517 AGS	Dwg. Check 740520 LLM	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.
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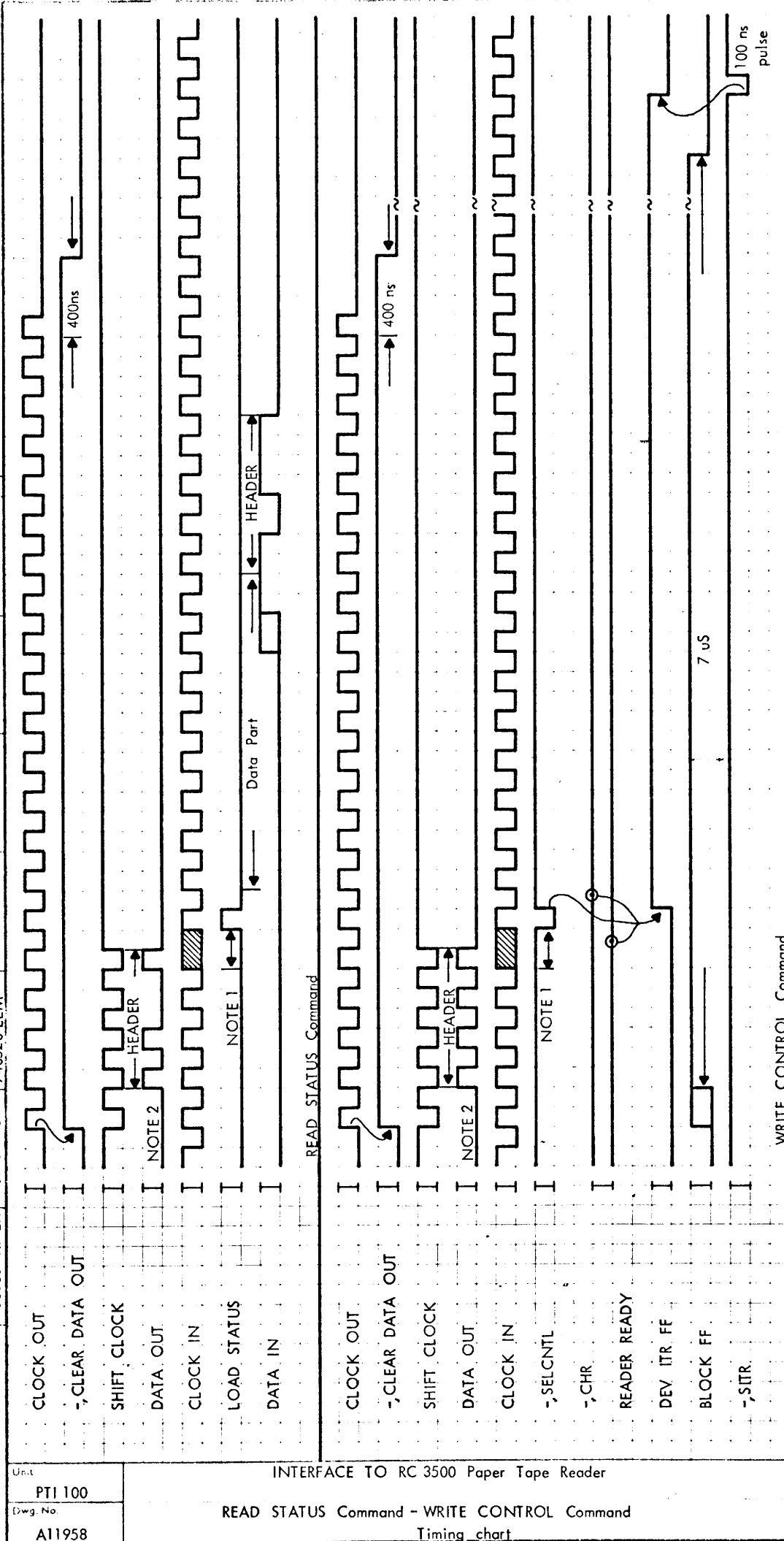
Unit	PTI 100
Dwg. No.	A11957

INTERFACE TO RC 500 Paper Tape Reader

READ DATA command
Timing Chart



A/S REGNECENTRALEN	Designed by 730306 KNEH	Drawn by 740516 AGS	Dwg. Check 740520 LLM	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.
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NOTE 1: max. 1 period of CLOCK IN (200ns) to synchronization of CLOCK OUT and CLOCK IN.

NOTE 2: One extra clock pulse on CLOCK OUT before data on DATA OUT.

Unit	PTI 100
Dwg. No.	A11958

INTERFACE TO RC 3500 Paper Tape Reader

READ STATUS Command - WRITE CONTROL Command
Timing chart

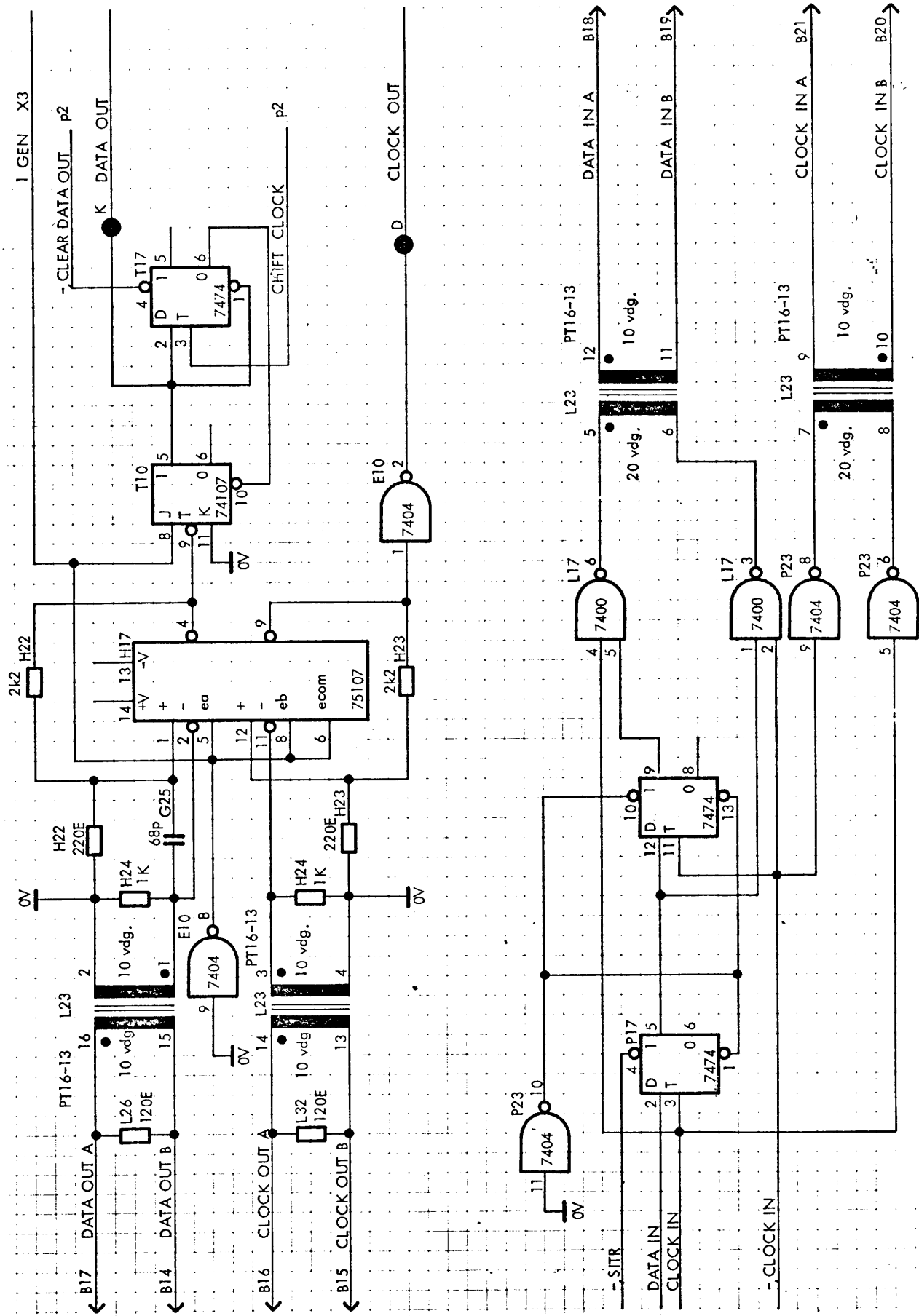
SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
7 CLEAR DATA OUT CLOCK IN 7 CLOCK IN CLOCK IN A CLOCK IN B CLOCK OUT CLOCK OUT A CLOCK OUT B DATA IN DATA IN A DATA IN B DATA OUT DATA OUT A DATA OUT B SHIFT CLOCK 7 SITR 1-GEN x3	PTR 2 PTR 2 PTR 2 J 1-6 J 1-7 PTR 3 J 1-8 J 1-9 PTR 2 PTR 4	J 1-1 J 1-2 PTR 2 PTR 4 J 1-3 J 1-4 PTR 2 PTR 2	7 CLEAR DATA OUT CLOCK IN 7 CLOCK IN CLOCK IN A CLOCK IN B CLOCK OUT CLOCK OUT A CLOCK OUT B DATA IN DATA IN A DATA IN B DATA OUT DATA OUT A DATA OUT B SHIFT CLOCK 7 Send InTeRrupt 1-GENerator x3

Unit PTI 100		PTR 1 RC 3239-1 Pos. 3 P. 1 of 4
Dwg. No. A22838		

A/S REGNECENTRALEN	Designed by	730306 KNEH	Drawn by	740517 AGS	Dwg. Office Check	740520 LLM	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.

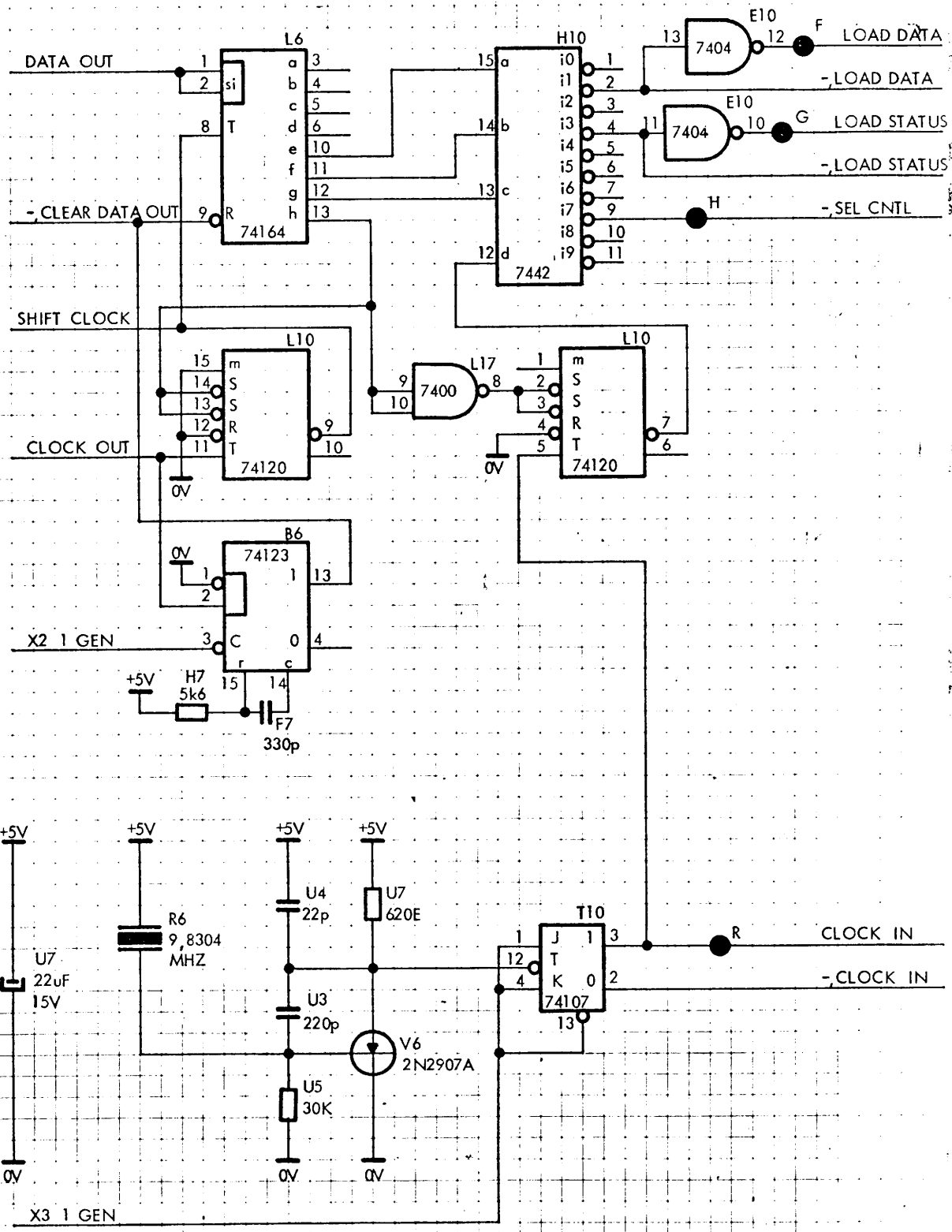
Unit	PTR 100
Dwg. No.	A11578

INTERFACE TO RC 500 Paper Tape Reader
DATA AND CLOCK RECEIVER
MODULATOR LINE DRIVER
Circuit Diagram



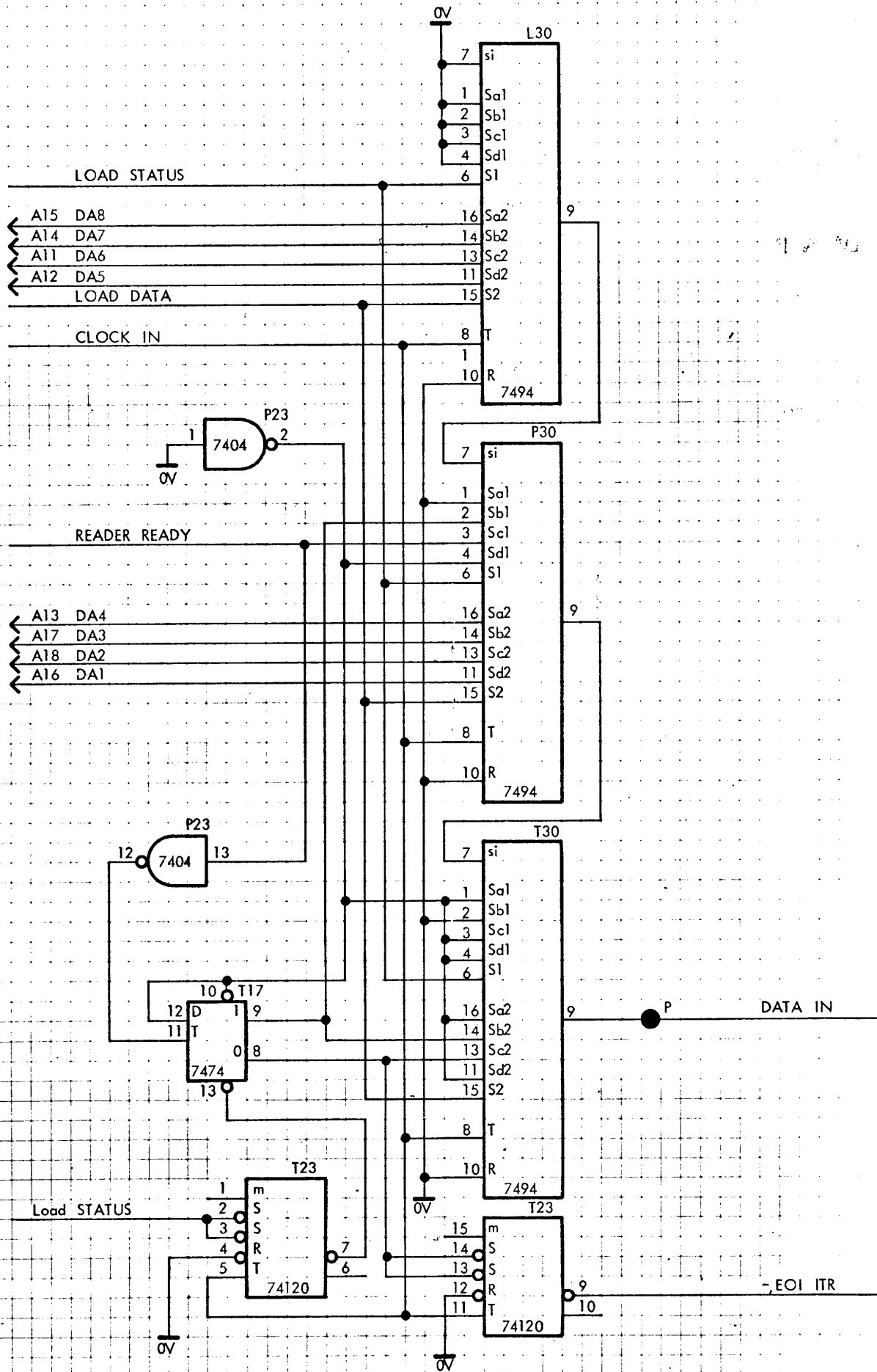
SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
7 CLEAR DATA OUT CLOCK IN 7 CLOCK IN CLOCK OUT DATA OUT LOAD DATA 7 LOAD DATA LOAD STATUS 7 SEL CNTL x2 1-GEN	 PTR 1 PTR 1 PTR 4	PTR 1 PTR 1 PTR 3 PTR 4 PTR 1 PTR 4 PTR 3 PTR 4 PTR 3 PTR 4	7 CLEAR DATA OUT CLOCK IN 7 CLOCK IN CLOCK OUT DATA OUT LOAD DATA 7 LOAD DATA LOAD STATUS 7 SElect CoNTroL x2 1-GENerator

A/S REGNECENTRALEN
 Designed by 730306 KNEH
 Drawn by 740516 AGS
 Dwg. Check 740520 LLM
 Design Check
 Replaces Dwg. No.
 due to ECN
 Replaced by Dwg. No.



SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
CLOCK IN	PTR 2		CLOCK IN
DA 1-8	RC 500		Data bit 1-8
DATA IN		PTR 1	DATA IN
7, EOI ITR		PTR 4	7, End Of Information InTeRrupt
LOAD DATA	PTR 2		LOAD DATA
LOAD STATUS	PTR 2		LOAD STATUS
READER READY	PTR 4		READER READY

Unit PTI 100		PTR 3
Dwg. No. A22840		RC 3239-1 Pos. 3 P. 3 of 4



Unit
PTI 100
Dwg. No.
A11580

INTERFACE TO RC 3500 Paper Tape Reader
DATA IN / STATUS Register - HEADER GENERATOR

Circuit Diagram

PTR 3
RC 3239-1
Pos. 3
P. 3 of 4

SIGNAL	ORIGIN	DESTINATION	DESCRIPTION
7 CHR	RC 500		7 CHaracter Ready
CHREQ		RC 500	CHaracter REQuest
CLOCK IN	PTR 2		CLOCK IN
7 CLOCK IN	PTR 2		7 CLOCK IN
CLOCK OUT	PTR 1		CLOCK IN
7 EOI ITR	PTR 3		7 End Of Information InTeRrupt
7 LOAD DATA	PTR 2		7 LOAD DATA
PTP	RC 500		Paper Tape Permit
PTS		RC 500	Paper Tape Select
READER READY		PTR 3	READER READY
RESET	RC 500		RESET
7 RHF		RC 500	7 Read Feed Hole
7 SEL CNTL	PTR 2		7 SEL CoNTroL
7 SITR		PTR 1	7 Send InTeRrupt
1 GEN x2		PTR 2	1 GENerator x2

Unit
PTI 100

Dwg. No.
A22841

PTR 4
RC 3239-1
Pos. 3
P. 4 of 4

A/S REGNENTRALEN
 Designed by 730305 KNEH 740516 AGS
 Drawn by 740520 LLM
 Design Check
 Replaces Dwg. No.
 due to ECN
 Replaced by Dwg. No.

