
Title:

RC 35-108

Block Synchronous communication controller

General Information

 **REGNECENTRALEN**

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RCSL No: 52-AA751

Edition: December 1974

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The RC 35-108 is a Block Synchronous Communication controller, hereafter called BSC 100, designed to connect a synchronous transmission equipment to RC 3500 via 2 or 3 I/O channels.

3 I/O channels are used in the FULL DUPLEX, simultaneous transmission mode. In this mode data can be received and transmitted simultaneously.

2 I/O channels are used in the FULL DUPLEX, alternate transmission mode.

The BSC 100 is designed to operate with following transmission rates:

48 - 200 kbps.

The transmission rate is determined by the clock, which must be supplied from the modem/modemsimulator.

Data/Clock lines between BSC 100 and modem comply with the CCITT V35 recommendation: "Transmission of 48 kbps using 60 - 108 KHz group baud circuits."

Control signals between BSC 100 and modem comply with the CCITT V24 recommendation: "Functions and Electrical Characteristics of circuits at the interface between data terminal and data communication equipment."

BSC 100 comply with following ISO recommendations:

- R 1745: Basic mode control procedures for data communication systems.
- R 1155: The use of longitudinal parity to detect errors in information messages.
- R 1177: Character structure for synchronous transmission.

The BSC 100 is constructed around a USRT circuit (COM 2601). The COM 2601 is a MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with synchronous data communication. For further information concerning COM 2601 refer section 4 "COM 2601 Description".

Some of the BSC 100 functions are made programmable using the BYM 100 byte-manipulator as a controller for the transfer of data between RC 3500 and the communication equipment.

Following functions are programmable by changing the contents of a Read Only Memory:

- a) Parity Mode.
Odd, even and no parity.
- b) Number of data bits/character. 5, 6, 7 or 8 bits, parity bit excl.
- c) The transmission control characters used.

The standard version of BSC 100 comply with ISO 1745. ISO code and 7 data bits/character - odd parity are used. The parity check/generation includes vertical parity check/generation and longitudinal redundancy check/generation.

The BSC 100 is operated by means of 3 RC 3500 I/O channels named:

- a) The WRITE CHANNEL
- b) The READ CHANNEL
- c) The CONTROL CHANNEL

The WRITE CHANNEL is only used during the simultaneous transmission mode to transmit characters to the communication equipment.

The CONTROL CHANNEL is used to start the transmitter.

Upon the reception of the start transmitter command the BSC 100 transmits 4 SYN characters, presupposed the modem returns READY FOR SENDING and DATA SET READY. Following the transmission of the SYN characters interrupts are sent to RC 3500 on the CONTROL and WRITE CHANNELS, indicating the end of the 4 syn-sequence and the request for data. Simultaneously the status bit READY TO TRANSMIT is set.

By means of the WRITE CHANNEL a write block of bytes command can now be used to transmit messages. Following the transmission of every characters to the modem the BSC 100 generates an interrupt to RC 3500 on the WRITE CHANNEL, indicating the request for a new character.

In the alternate transmission mode write data and write interrupts are transmitted via the READ CHANNEL.

Information messages

2.2.1

BSC 100 recognizes following control characters used as information framing characters:

SOH, STX, ETB and ETX.

By the appearance of either SOH or STX the summation to obtain the block check character (LRC) is started. The starting character is not included in the summation. All the characters transferred to BSC 100 from RC 3500, following the start of the block check summation are included in the summation, including the ETX or ETB control character, which causes the BSC 100 to transmit the LRC character to the modem.

The CONTROL CHANNEL is used to start synchronization.

Upon the reception of the start synchronization command the COM 2601 in the BSC 100 is set into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found.

A sync character is found, by definition, when the contents of the COM 2601 receiver sync register and the receiver shift register are identical. When this occurs the COM 2601 is set into the character mode. In this mode characters received are compared with the receiver sync register. If the character received after the shift to character mode is a sync character too, the BSC 100 is in character synchronization, and an interrupt is sent to RC 3500 on the CONTROL CHANNEL. Simultaneously the status bit READY TO RECEIVE is set, indicating that the BSC 100 is in character synchronization. If the character received after the shift to character mode is not a sync character, the COM 2601 is again set into the search mode, and the sequence described above is repeated.

Except for SYN characters every character received when BSC 100 is in character synchronization causes an interrupt to be sent to RC 3500 via the READ CHANNEL. Characters can be transferred to RC 3500 using the read block of bytes instruction.

Information Messages

2.3.1

BSC 100 recognizes following control characters used as information framing characters:

SOH, STX, ETB and ETX.

BSC 100 recognizes following control characters during supervisory sequences:

ACK, NACK, ENQ and EOT.

Character synchronization is established as described in section 2.3. Block check summation is not used in supervisory sequences, only vertical parity check is executed.

If the BSC 100 recognizes an ACK, NACK, ENQ or EOT control character in the data stream received, the RC 3500 is notified by means of a normal read data interrupt, and a read command will transfer the control character to RC 3500. However, upon the reception of the following character a read data interrupt and a control interrupt is send to RC 3500 indicating the end of receive condition. The character send to RC 3500 upon the following read command is a dummy character accompanied by End of Information.

Simultaneously with the interrupts status bit RECEIVE BLOCK END is set, status bit LRC PARITY ERROR cleared and status bit VERTICAL PARITY ERROR updated. The RECEIVE BLOCK END status causes the receiver to be reset. The receiver remains reset until the RECEIVE BLOCK END status is cleared upon the reception of the next start synchronization command.

The BSC 100 does not specify the type of the supervisory sequence, this must be done by the RC 3500 program.

CONTROL CHANNEL

3.1

The CONTROL CHANNEL is used during the simultaneously and alternate transmission modes to control the transmission i.e.:

- a) Initial start after power on dead start.
- b) Start/Stop of transmitter.
- c) Control of transmission mode.
- d) Transfer of status between RC 3500 and BSC 100/Communication equipment.

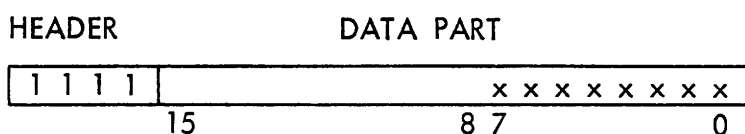
The above mentioned functions are made possible by means of the write control and read status instructions. The write data and read data instructions are not used in connection with the CONTROL CHANNEL.

Write Control

3.1.1

The transfer direction is from RC 3500 to BSC 100.

BSC 100 interprets the control word transferred as follows:



x = denotes unused bits.

bit 13: STOP TRANSMITTER

Bit 13 = "1" will cause the transmission line to the modem to change to idle level ("1"), and simultaneously the status bit 14: READY TO TRANSMIT is cleared. The stop transmitter command will also inhibit the write data interrupt until BSC 100 receives a start transmission command. An automatic stop of the transmitter is executed by BSC 100 if an ETX, ETB, ACK, NACK, ENQ or EOT character is recognized in the data stream from RC 3500. Refer to section 2.2.1 and 2.2.2.

A control word containing bit 14 and bit 13 equal logical one is interpreted as a stop transmitter command.

bit 12: START SYNCHRONIZATION

Bit 12 = "1" directs the BSC 100 to start synchronization i.e.:

1. The COM 2601 receiver circuits is set into the search mode (bit phase).
2. Status bit 13: READY TO RECEIVE is cleared.

In the search mode the serially received data bit stream is examined on a bit by bit basis until a SYN character is found. When this occurs the COM 2601 is set into character mode. In this mode the data stream is examined on a character by character basis. If the character received after the shift to character mode is a SYN character too, the BSC 100 is by definition in synchronization, and an interrupt is send to RC 3500 on the CONTROL CHANNEL. Besides the interrupt the status bit 13: READY TO RECEIVE is set.

bit 9: REQUEST TO SEND

This signal controls the transmit function of the modem. When the modem has received this signal and the modem status DATA SET READY is "1" the modem is conditioned to transmit data. This condition is indicated by the modem status signal READY FOR SENDING.

Since the BSC 100 operates with FULL DUPLEX transmission lines the REQUEST TO SEND signal can be permanently on.

Except for write control instructions with bit 8 = "1" the REQUEST TO SEND signal must be defined in every write control instruction send to RC 3500.

bit 8: REQUEST FOR CONTROL INTERRUPT.

Bit 8 = "1" directs the BSC 100 to send a control interrupt via the CONTROL CHANNEL, if a read status command has not been returned to BSC 100 as a response to a previous control interrupt. When bit 8 = "1" all of the other control bits are invalid.

bit 13: READY TO RECEIVE.

Bit 13 = "1" indicates to RC 3500 that BSC 100 is in character synchronization. Bit 13 is cleared by either:

1. A start synchronization command.
2. A dead start command.

Simultaneously with the set of status bit 13 a control interrupt is send to RC 3500 via the CONTROL CHANNEL.

bit 12: DATA SET READY.

Bit 12 is directly a modem status (CCITT circuit no. 107).
Bit 12 = "1" indicates that the modem is ready to exchange further control signals with BSC 100 i.e. the modem is not in TEST POSITION.

bit 11: READY FOR SENDING.

Bit 11 is directly a modem status (CCITT circuit no. 106).
Bit 11 = "1" indicates that the modem is conditioned to transmit data. Refer to section 3.1.1 REQUEST TO SEND.

bit 10: DATA CARRIER DETECTOR.

Bit 10 is directly a modem status (CCITT circuit no. 109).
Bit 10 = "1" indicates that the received signal is within appropriate limits.

bit 6: RECEIVE BLOCK END.

Bit 6 is set = "1" when the LRC character in an information message has been received, or when an ACK, NACK, ENQ or EOT control character in a supervisory sequence has been received.

Simultaneously with the set of bit 6 a control interrupt is send to RC 3500 and the receiver is reset. The receiver remains reset until bit 6 is cleared by either:

1. A dead start command.
2. A start synchronization command.

bit 5: OVERRUN.

If RC 3500 by some reason is unable to follow the receiving rate bit 5 is set to logical one, indicating that one or more of the received characters has been lost.

Bit 5 is updated simultaneously with the set of status bit 6: RECEIVE BLOCK END.

Bit 5 is cleared by either:

1. A dead start command.
2. A start synchronization command.

Control Interrupt Response

3.1.3

A control interrupt results when following status bits changes to logical one:

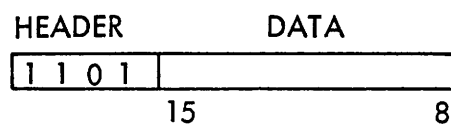
1. bit 15 : READY TO OPERATE
2. bit 14 : READY TO TRANSMIT
3. bit 13 : READY TO RECEIVE
4. bit 7 : TRANSMIT BLOCK END
5. bit 6 : RECEIVE BLOCK END

To specify the type of control interrupt the RC 3500 must read the status word.

This instruction is used during the FULL DUPLEX simultaneous transmission mode and during the FULL DUPLEX alternate transmission mode.

The instruction transfers characters, received on the transmission line, from BSC 100 to RC 3500.

The read data word shall be interpreted as follows:



Bit 15 - 8: DATA CHARACTER received.

Bit 15 is the least significant bit, and the first bit received from the communication equipment. Using ISO 7 bits code, the data bit 8 (parity bit) is always "0", since the COM 2601 circuit in BSC 100 suppresses the parity bit.

The last character send to RC 3500 during information messages should be the LRC character, but since the character is accompanied by End of Information the character will appear as all zeroes in RC 3500.

The last character send to RC 3500 during supervisory sequences is a dummy character (all zeroes) accompanied by End of Information.

Bit 15 - bit 8: DATA CHARACTER to transmit.

This character is transmitted from RC 3500 to the transmission line via the COM 2601 universal transmitter/receiver circuit in BSC 100.

Bit 15 is the least significant bit and the first bit transmitted to the communication equipment.

In the standard version of BSC 100 ISO 7 bits code is used, which makes bit 8 (parity bit) invalid, since the BSC 100 itself generates the parity bit.

Interrupt Response

3.3.1

Interrupt on the WRITE DATA CHANNEL notifies RC 3500 that a character is required for transmission to the communication equipment.

Full double buffering allows one full character time to load the character to be transmitted.

SYN characters are automatically inserted in the transmitted data stream if RC 3500 is unable to follow the transmission rate.

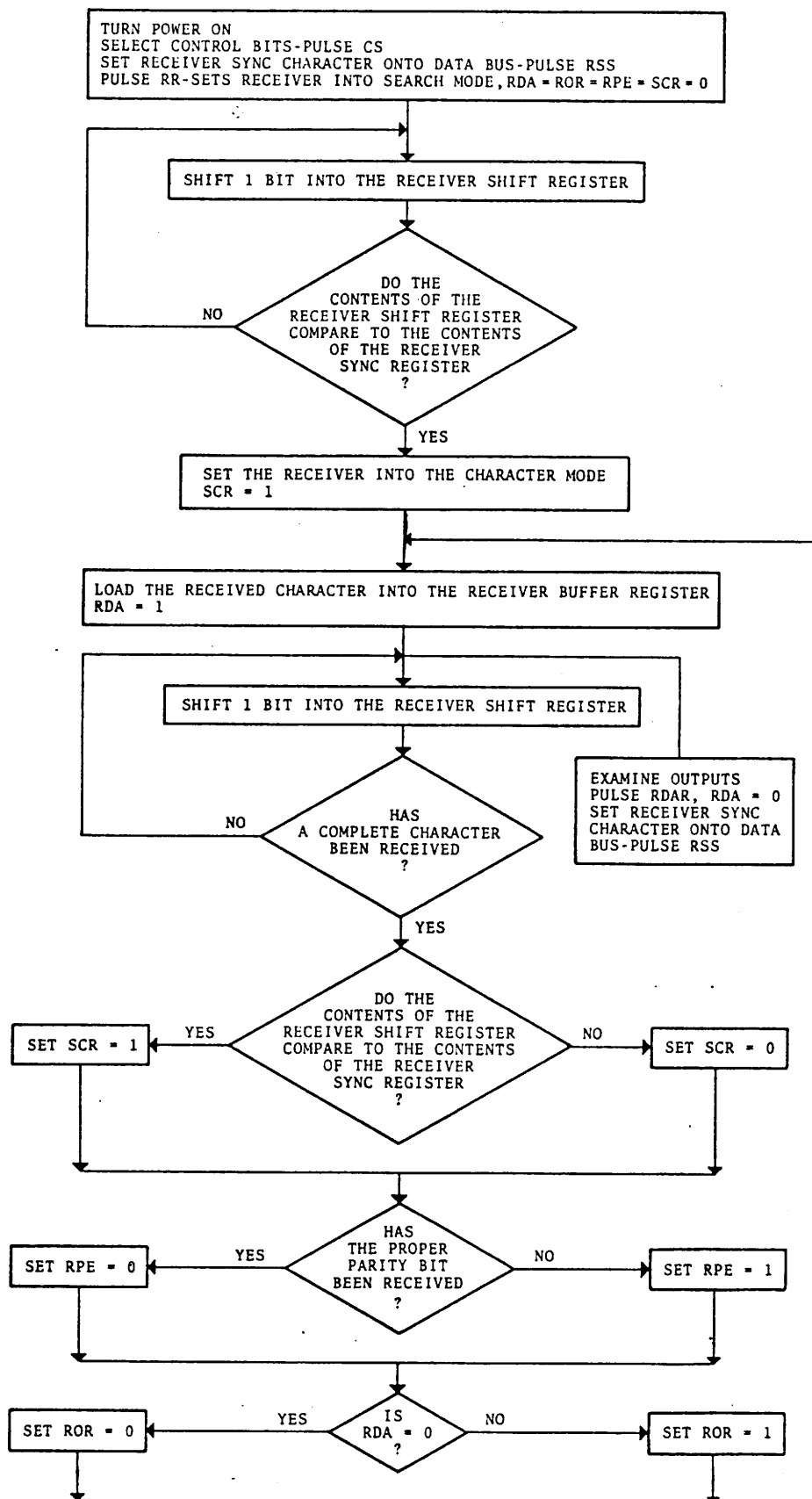
DESCRIPTION OF OPERATION - RECEIVER/TRANSMITTER

4.1

The input clock frequency for the receiver is set at the desired receiver baud rate and the desired receiver sync character (synchronous idle character) is loaded into the receiver sync register. When the Receiver Reset input transitions from a high-level to a low-level the receiver is set into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the Sync Character Received output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register. The receiver provides flags for Receiver Data Available, Receiver Over Run, Receiver Parity Error, and Sync Character Received. Full double buffering eliminates the need for precise external timing by allowing one full character time for received data to be read out.

The input clock frequency for the transmitter is set at the desired baud rate and the desired transmitter sync character is loaded into the transmitter sync register. Internal logic decides if the character to be transmitted out of the transmitter shift register is extracted from the transmitter data register or the transmitter sync register. The next character transmitted is extracted from the transmitter data register provided that a Transmitter Data Strobe pulse occurs during presently transmitted character.

FLOW CHART - RECEIVER



The interface between BSC 100 and the modem comply with the CCITT recommendations V24 and V35.

The signals used are listed below. The input/output jack for the modem is a CANNON JACK TYPE DB - 25 S (refer to fig. 3).

CIRCUIT NO. and NAME	DIRECTION	INTERFACE TYPE
103: TRANSMITTED DATA A - B	TO MODEM	V35
104: RECEIVED DATA A - B	FROM MODEM	V35
105: REQUEST TO SEND	TO MODEM	V24
106: READY FOR SENDING	FROM MODEM	V24
107: DATA SET READY	FROM MODEM	V24
109: DATA CARRIER DET.	FROM MODEM	V24
114: TRANSMITTER SIGNAL ELEMENT TIMING A - B	FROM MODEM	V35
115: RECEIVER SIGNAL ELEMENT TIMING A - B	FROM MODEM	V35

The BSC 100 is housed within 2 MKL 104 std module cassettes.

The POWER SUPPLY for BSC 100 is housed within a MKP 112 power supply cassette. The POWER SUPPLY is capable of delivering:

+ 5 VOLT/10 A

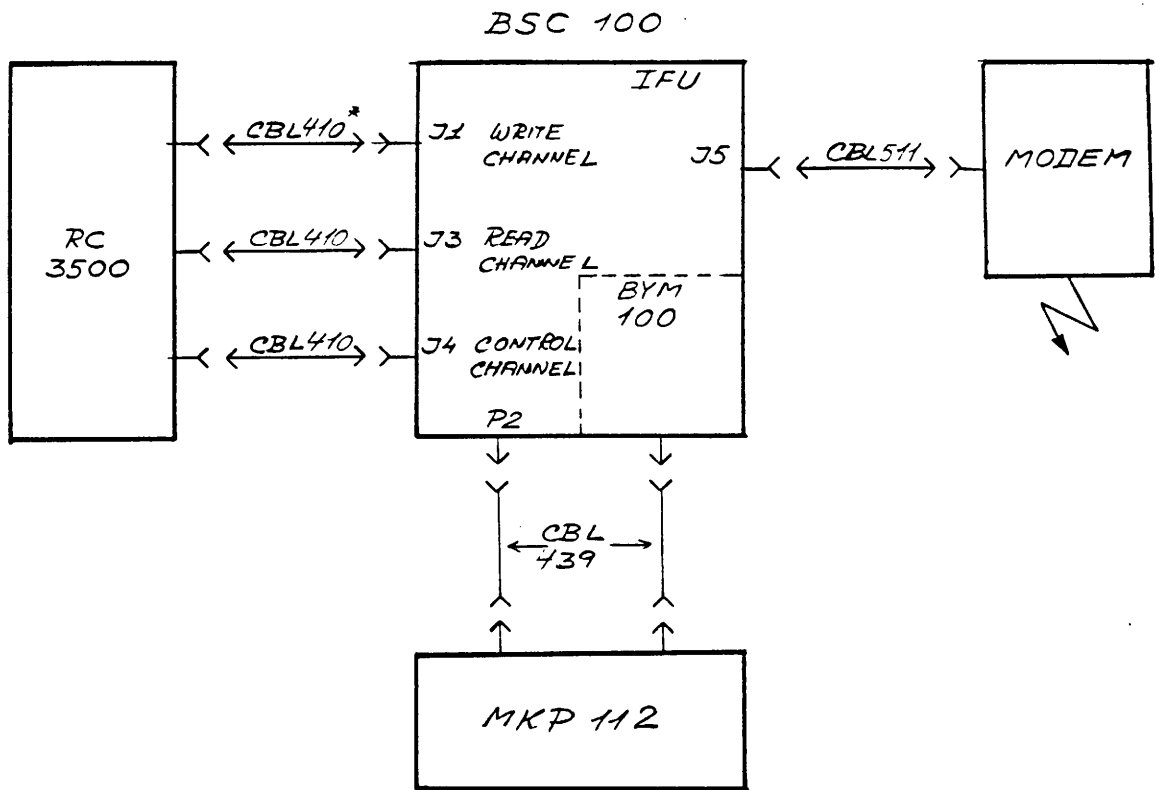
$\pm$ 12 VOLT/250 mA

To connect BSC 100 to the POWER SUPPLY 2 cables CBL 439 are required.

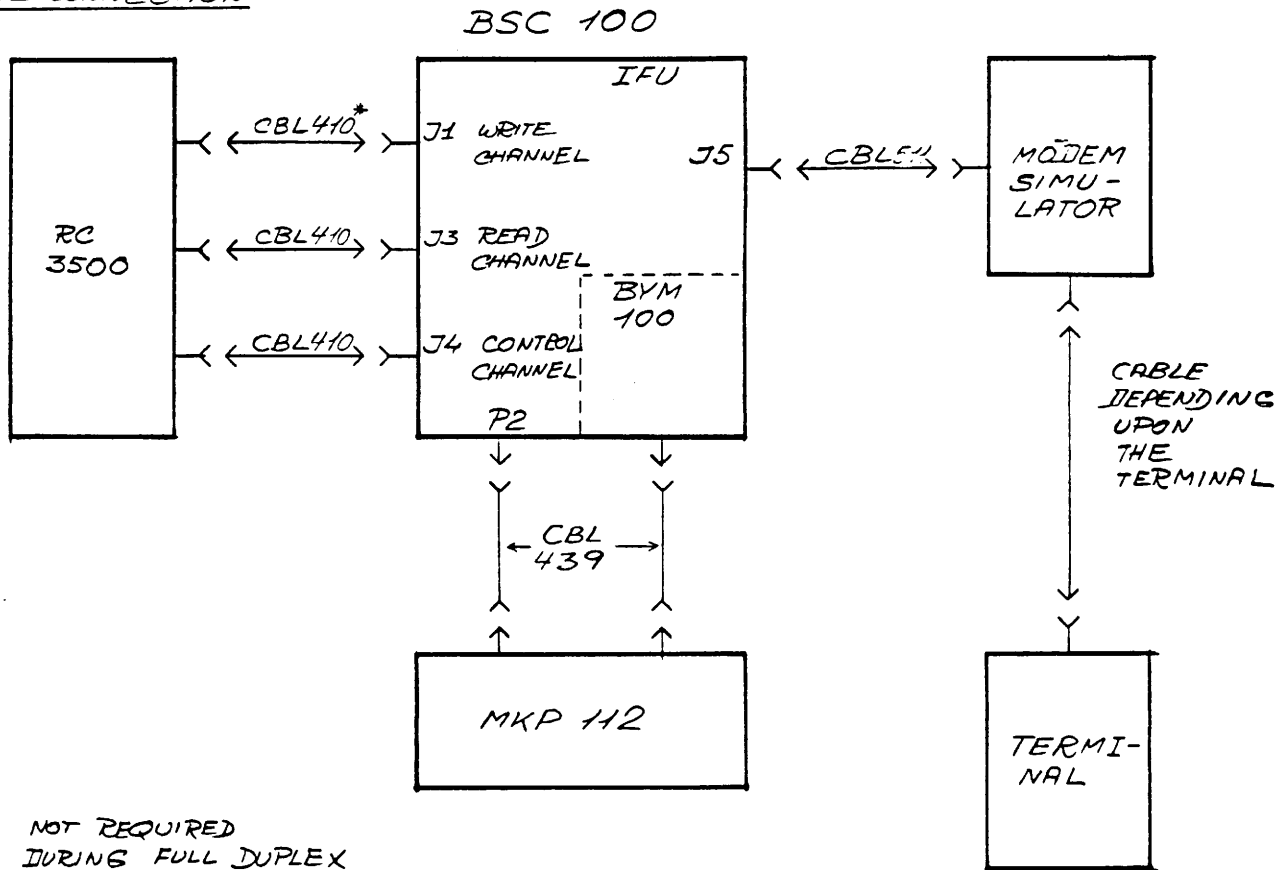
3 cables CBL410 are required to connect BSC 100 to RC 3500. Max length of CBL410 is 100 m.

Cable CBL511 is used to connect BSC 100 to the modem simulator/modem max. length of CBL 511 is 15 m. Refer to fig. 2 for LOCAL/REMOTE connection diagram.

REMOTE CONNECTION



LOCAL CONNECTION



* NOT REQUIRED
DURING FULL DUPLEX
ALTERNATE TRANSMISSION

Unit
BSC 100

Dwg. No.

A12172

LOCAL / REMOTE INTERCONNECTION

FIG. 2

A/S REGNECENTRALEN	Designed by	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.
	VH 741205						

J1, J3 and J4 to RC 3500
CANNON, type DEC 9-S

PIN	SIGNAL NAME
1	CLOCK IN A
2	CLOCK IN B
3	DATA IN A
4	DATA IN B
5	
6	CLOCK OUT A
7	CLOCK OUT B
8	DATA OUT A
9	DATA OUT B

Unit BSC 100
Dwg. No. A23318

STD. I/O JACKS FOR RC3500 FIG. 4