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General Information on RC 35-103/104

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(46 pages)

Abstract:

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CONTENTSPage

1.1.	Short description of signals	1
1.2.	Functional description	21
1.3.	Transmitter/Receiver unit	25
1.3.1.	Strobe multiplexors	25
1.3.2.	Holding register for clock select	25
1.3.3.	Clock selector	26
1.3.4.	Universal Asynchronous Receiver/Transmitter	26
1.4.	Modem Interface and status selectors	29
1.4.1.	Modem drivers and receivers	29
1.4.2.	Holding register for Modem control signals	29
1.4.3.	STATUS - selectors	30
1.4.4.	Blocking of TRM interrupts	30
1.4.5.	Interrupt generator	31
1.5.	Block diagrams 1 - 6	32
1.6.	Installation	38
1.7.	Power requirements	39

SHORT DESCRIPTION OF SIGNALS

In the LAM interface different signal levels are used. The normal signal levels will be the TTL standard levels:

HIGH $\geq 2,4$ V.

LOW $\leq 0,8$ V.

Other signal levels are listed below.

Note 1. Signal levels, RC 3500.

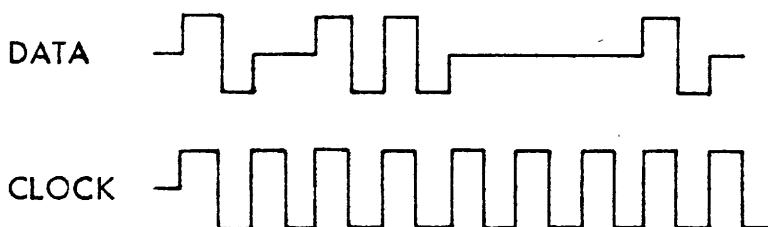
The signals between RC 3500 and the LAM interface are in balanced mode.

Voltage swing: $400 \text{ mV} < V < 3 \text{ V}$, depending on attenuation of the cable.

Cable impedance: 100 Ohms.

Waveform of the communication:

, 1 , 0 , 1 , 1 , 0 , 0 , 0 , 1 ,



Note 2. Signal levels, MODEM.

HIGH + 12 V nom.

LOW - 12 V nom.

when generated in LAM

Input from modem must apply to the following specification:

+ 3 V $\leq$ HIGH $\leq$ + 25 V.

- 3 V $\geq$ LOW $\geq$ - 25 V.

SIGNAL NAME	REFERENCE	DESCRIPTION
ADD IN 1-3	IOI 6	ADDress IN 1-3
	IOI 3	The three least significant
	TRU 2	bits in the scanner output.
	TRU 12	Used to address the U-ART
	MIS 5	circuits.
	MIS 6	
	MIS 7	
	MIS 12	
	MIS 13	
	MIS 14	
ADD IN 0	IOI 6	ADDress in 0.
	IOI 3	The most significant bit in the
	TRU 12	scanner output.
	MIS 12	
	MIS 13	
	MIS 14	
-, ADD IN 0	IOI 6	Same as above.
	TRU 2	
	MIS 5	
	MIS 6	
	MIS 7	

SIGNAL NAME	REFERENCE	DESCRIPTION
ADD OUT 1-3	IOI 2	ADDress OUT 1-3
	TRU 1	The three least significant bits in the multiplexer channel address send from RC 3500.
	TRU 2	
	TRU 11	
	TRU 12	
	MIS 5	
	MIS 6	
	MIS 7	
	MIS 12	
	MIS 13	
	MIS 14	
ADD OUT 0	IOI 2	ADDress OUT 0
	TRU 11	The most significant bit in the multiplexer channel address send from RC 3500.
	TRU 12	
	MIS 12	
	MIS 13	
	MIS 14	
7, ADD OUT 0	IOI 2	Same as above.
	TRU 1	This signal is used to select device 0-7.
	TRU 2	
	MIS 5	
	MIS 6	
	MIS 7	

SIGNAL NAME	REFERENCE	DESCRIPTION
7 CLEAR DATA OUT	IOI 2 IOI 1	Clear signal to the Data Out register 7 CLEAR DATA OUT = 1 from the leading edge of the first clock pulse on CLOCK OUT to about 650 ns after the last clock pulse.
CLOCK IN A-B	IOI 1 J 1	Clock output from LAM to RC 3500. NOTE 1.
CLOCK IN	IOI 7 IOI 1 IOI 2 IOI 3 IOI 4 IOI 5	Internal clock signal. 4,9152 MHZ. Used as clock output to RC 3500 and to shift serial data out to RC 3500.
7 CLOCK IN	IOI 7 IOI 1 IOI 5	Same as above.
CLOCK OUT A-B	J 1 IOI 1	Clock Output from RC 3500. NOTE 1.
CLOCK OUT	IOI 1 IOI 2 IOI 5	The clock signal from RC 3500 after receiver-circuit.
CLOCK SEL Ax-Bx	TRU 1, 11 TRU 3 - TRU 10 TRU 13- TRU 20	CLOCK SElect Ax-Bx Output signals from the holding register for CLOCK SElect. Input signals to the clock selector, one selector for each channel.

SIGNAL NAME	REFERENCE	DESCRIPTION
CNTL x	MIS 15, 12 MIS 1-4 MIS 8 - 11	CONnect TO Line x Output signal from the Holding register for Modem Control Signals. This signal is set and reset by bit 10 in a WRITE CON- TROL command. x corresponds to the binary value of ADD OUT 0-3. MASTER RESET = 1 clears this register.
CONTROL STROBE	IOI 8 TRU 1 TRU 12 TRU 11 TRU 12 MIS 5 MIS 12	Single pulse generated when a WRITE CONTROL with bit 15 = 0 is decoded. Used to load the CONTROL BITS REGISTER, in the device selected by ADD OUT 0-3. Pulselength is about 300 ns.
CONNECT TO LINE x	MIS 1-4, 8-11 J 2 - J 17	Control signal to the modem. This signal commands the modem to connect to the communication Line. NOTE 2.
CS x	TRU 2, 12 TRU 3 - TRU 10 TRU 13 - TRU 20	Control Strobe X. The same as the signal CONTROL STROBE; x corresponds to the binary value of ADD OUT 0-3.

SIGNAL NAME	REFERENCE	DESCRIPTION
DA	TRU 3 - TRU 10 TRU 13 - TRU 20 MIS 5 MIS 12	Data Available. Same as the signal 7, DATA AVAILABLE.
7, DACAR x	MIS 1 - 4 MIS 8 - 11 MIS 7 MIS 14	DAta CARrier x. Same as DATA CARRIER DETECTOR x after V 24 receivers.
7, DATA AVAILABLE	MIS 5, 12 IOI 5	Signal indicating that a whole character is ready from the U-ART circuit at which the SCANNER point. Used to set the INPUT ITR FF.
DATA CARRIER DETECTOR x	J 2 - J 17 MIS 1 - 4 MIS 8 - 11	Output signal from the modem. This signal indicates that the received carrier from the remote station is within appropriate limits as specified in the rele- vant Recommendation equipment.
DATA IN A - B	IOI 1 J 1	Serial data from LAM to RC 3500. NOTE 1.
DATA IN	IOI 4 IOI 1	Serial data from the DATA IN register to the modulator shifted by CLOCK IN.

SIGNAL NAME	REFERENCE	DESCRIPTION
DATA OUT A-B	J 1 IOI 1	Serial data from RC 3500 to LAM NOTE 1.
DATA OUT	IOI 1 IOI 2	Serial data to the DATA OUT register from the demodulator. The trailing edge of DATA OUT corresponds to the trailing edge of CLOCK OUT.
DATA SET READY x	J 2 - J 17 MIS 1 - 4 MIS 8 - 11	Output signal from the modem. This signal indicates that the modem power is switched on and the modem is not in test mode. NOTE 2.
DATA STROBE	IOI 8 TRU 2 TRU 12	Single pulse generated when a WRITE DATA header is decoded. Used to load the Data Bits Hol- ding Register in the channel selected by ADD OUT 0-3. Pulse length is about 250 ns.
DB 1 - 8	TRU 1, 11 TRU 3 - TRU 10 TRU 13 - TRU 20	Data Bit 1 - 8 Same as DOUT 7-0

SIGNAL NAME	REFERENCE	DESCRIPTION
7, DCD	MIS 7, 14 IOI 3	7, Data Carrier Detector. status from the modem selected by ADD OUT 0-3. 7, DCD is sent as bit 10 in the STATUS WORD to RC 3500.
DOUT 15	IOI 2	Output from the DATA OUT register. Corresponds to bit 15 in the command word from RC 3500. In a WRITE CONTROL word DOUT15 means START SCANNER. DOUT15 in a WRITE CONTROL starts the scanner; if DOUT15 = 0 DOUT10-0 are disabled. In the other command words DOUT 15 has no function.
7, DOUT 15	IOI 2 IOI 6 IOI 8	Same as above.
DOUT 10	IOI 2 MIS 5 MIS 12	Output from the DATA OUT register. Corresponds to bit 10 in the command word from RC 3500. In a WRITE CONTROL word DOUT10 = 1 means CONNECT TO LINE. In the other command words DOUT10 has no function.

SIGNAL NAME	REFERENCE	DESCRIPTION
DOUT 9	IOI 2 MIS 5 MIS 12	Output from the DATA OUT register. Corresponds to bit 9 in the command word from RC 3500. In a WRITE CONTROL WORD DOUT 9 = 1 means REQUEST TO SEND. In the other command words DOUT 9 has no function.
DOUT 8	IOI 2 IOI 8	Output from the DATA OUT register. Corresponds to bit 8 in the command word from RC 3500. In a WRITE CONTROL word DOUT 8 = 0 means MASTER RESET. In the other command words DOUT 8 has no function.
DOUT 7	IOI 2 TRU 1 TRU 11	Output from the DATA OUT register. Corresponds to bit 7 in the command word from RC 3500. In a WRITE CONTROL word DOUT 7 = 1 means NO PARITY. In a WRITE DATA word DOUT 7 = 0 corresponds to bit 7 - 0 in the command word contain a data character.
DOUT 6	IOI 2 TRU 1 TRU 11	Output from the DATA OUT register. Corresponds to bit 6 in the command word from RC 3500. In a WRITE CONTROL word DOUT 6 means PARITY mode. For the WRITE DATA word see DOUT 7

SIGNAL NAME	REFERENCE	DESCRIPTION
DOUT 5	IOI 2 TRU 1 TRU 11	Output from the DATA OUT register. Corresponds to bit 5 in the command word from RC 3500. In a WRITE CONTROL word DOUT 5 means Number of STOP-elements. For the WRITE DATA word see DOUT 7
DOUT 4 - 3	IOI 2 TRU 1 TRU 11	Output from the DATA OUT register. Corresponds to bit 4 - 3 in the command word from RC 3500. In a WRITE CONTROL word DOUT 4 - 3 means Number of Data bits/char. For the WRITE DATA word see DOUT 7
DOUT 2 - 1	IOI 2 TRU 1 TRU 11	Output from the DATA OUT register. Corresponds to bit 2 - 1 in the command word from RC 3500. In a WRITE CONTROL word DOUT 2 - 1 means Transmission Speed Select. For the WRITE DATA word see DOUT 7
DOUT 0	IOI 2 TRU 1 TRU 11	Output from the DATA OUT register. Corresponds to bit 0 in the command word from RC 3500. No function in WRITE CONTROL. For the WRITE DATA word see DOUT 7

SIGNAL NAME	REFERENCE	DESCRIPTION
$\neg$ DS x	TRU 2, 12 TRU 3 - TRU 10 TRU 13-TRU 20	$\neg$ Data Strobe x. The same as the signal DATA STROBE, x corresponds to the binare value of ADD OUT 0 - 3.
$\neg$ DSR	MIS 7, 14 IOI 3	$\neg$ Data Set Ready. status from the modem selected by ADD OUT 0 - 3. $\neg$ DSR is sent as bit 12 in the STATUS word to RC 3500.
$\neg$ DSRDY x	MIS 1 - 4 MIS 8 - 11 MIS 7 MIS 14	$\neg$ Data Set ReaDY. x same as the signal DATA SET READY x after V 24 receivers.
$\neg$ EITR	MIS 5, 12 IOI 5	$\neg$ Enable InTeRrupt. $\neg$ EITR = 0 if the device x addressed by the SCANNER is ready to receive a new character from RC 3500 (TBMT = 1 $\wedge$ $\neg$ RDYFSX = 0 $\wedge$ OPEN TRM ITR = 1) or a whole character is ready to RC 3500 (DA = 1). If $\neg$ EITR = 0 the SCANNER is stopped and interrupt is sent to RC 3500.

SIGNAL NAME	REFERENCE	DESCRIPTION
FE	TRU 3 - TRU 10	Framing Error.
	TRU 13- TRU 20	Indicates that the device at which the
	IOI 3	SCANNER point has received a character with no valid STOP-element. Is sent as bit 14 in the STATUS word to RC 3500. If FE = 1 the ERROR bit in the READ DATA word is logic 1.
INPUT ITR	IOI 5	INPUT InTeRrupt.
	IOI 3	Output from INPUT ITR FF.
	MIS 6	This FF is set if the SCANNER points
	MIS 13	at a channel with $\neg$ DATA AVAILABLE = 0; this FF is reset by either $\neg$ MASTER RESET = 0 or $\neg$ RESET ITR = 0. The signal INPUT ITR is sent to RC 3500 in the READ DATA word as bit 15.
ITR CLOCK	IOI 6	InTeRrupt CLOCK.
	IOI 5	Clock signal from the Stop Scanner circuit. The trailing edge of ITR CLOCK is used to step the SCANNER. The leading edge as trigger input to the STOP SCAN FF and the INPUT ITR FF. Frequency = 0,3 MHZ.
LOAD DATA	IOI 2	Single pulse generated when a READ DATA
	IOI 3	header is decoded.
	IOI 4	Used to load the DATA IN register. Pulselength about 100 ns.

SIGNAL NAME	REFERENCE	DESCRIPTION
LOAD DATA	IOI 2	Same as above.
	IOI 3	Used to start the RESET ITR pulse;
	IOI 8	and to set the FF addressed by
	MIS 6	ADD IN 0-3 in the BLOCKING OF
	MIS 13	TRM ITR circuit if INPUT ITR = 0.
LOAD STATUS	IOI 2	Single pulse generated when a READ
	IOI 3	STATUS header is decoded.
	IOI 4	Used to load the STATUS register. Pulselenght about 100 ns.
MASTER RESET	IOI 8	Single pulse generated when a
	TRU 3 - 10 TRU 13- TRU 20	WRITE CONTROL with bit 8 = 0 is received. This clear-pulse is used to Clear all registers in the U-ART circuits. Pulselength is about 1 uS.
MASTER RESET	IOI 8	Same as above.
	IOI 5	This clear pulse is used to
	IOI 6	a) disconnect all communication lines
	MIS 5	(RLINE = 1).
	MIS 12	b) Stopping the SCANNER. c) Resetting the STOP SCAN FF and the INPUT ITR FF.

SIGNAL NAME	REFERENCE	DESCRIPTION
-, MODEM ERROR	MIS 7, 14 IOI 3	-, MODEM ERROR = 0 if DATA CARRIER DETECTOR = 0 for the channel at which the SCANNER points. If -, MODEM ERROR = 0 the ERROR bit in the READ DATA word is logic 1.
OPEN TRM ITR	MIS 13, 6 MIS 12, 5	OPEN TRAnsmit InTeRrupt. Output from the BLOCKING OF TRM ITR circuit. OPEN TRM ITR = 1 if the FF in this circuit corresponding to the channel at which the Scanner point is set. The set condition of this FF indicates that a Transmit Interrupt is earlier sent to RC 3500; but not answered with a WRITE DATA to this channel.
OR	TRU 3 - TRU 10 TRU 13-TRU 20 IOI 3	OverRun. Indicates that the device at which the SCANNER point has received a new character before the previously received character is transferred to RC 3500. The signal OR is sent as bit 15 in the STATUS word to RC 3500. If OR = 1 the ERROR bit in the READ DATA word is logic 1.

SIGNAL NAME	REFERENCE	DESCRIPTION
PE	TRU 3 - TRU 10	Parity Error.
	TRU 13- TRU 20	Indicates that the channel at which the
	IOI 3	SCANNER point has received a character with a parity bit which does not agree with the parity mode selected by bit 6 in the WRITE CONTROL word.
		The signal PE is sent as bit 13 in the STATUS word to RC 3500.
		If PE = 1 the ERROR bit in the READ DATA word is logic 1.
RD 1 - 8	TRU 3 - TRU 10	Read Data bit 1 - 8.
	TRU 13- TRU 20	RD 1 - 8 contain a data character
	IOI 3	from the channel at which the SCANNER points.
		RD 1 - 8 are sent as bit 7 - 0 in the READ DATA word to RC 3500.
		RD 1 is the data bit received immediately after the START-element on the communication line.
7 RDAX	TRU 2, 12	7, Reset Data Available x.
	TRU 3 - 10	Same as 7, RESET ITR; x corresponds
	TRU 13 - TRU 20	to the channel number at which the SCANNER points.

SIGNAL NAME	REFERENCE	DESCRIPTION
⌋ RDYFS	MIS 7, 14 IOI 3	⌋ ReaDY For Sending. Status from the modem selected by ADD OUT 0-3. ⌋ RDYFS is sent as bit 11 in the STATUS word to RC 3500.
⌋ RDYFS X	MIS 1 - 4 MIS 8 - 11 MIS 5, 12 MIS 7, 14	⌋ ReaDY For Sending x. Same as the signal READY FOR SENDING x after V 24 receivers.
READY FOR SENDING	J 2 - J 17 MIS 1 - 4 MIS 8 - 11	Output signal from the modem. This signal indicates that the modem is ready to transmit data. NOTE 2.
RECEIVED DATA x	J 2 - J 17 TRU 3 - TRU 10 TRU 13-TRU 20	Serial data from the modem. HIGH Level corresponds to logic 0. NOTE 2.
RESET ITR	IOI 8 TRU 2 TRU 12	RESET InTeRrupt. Single pulse generated by ⌋ LOAD DATA. Pulselength is about 1 uS. Used to clear the DA (Data Available) FF in the U-ART circuit at which the SCANNER points.
⌋ RESET ITR	IOI 8 IOI 5	Same as above. Used to clear the INPUT ITR FF.

SIGNAL NAME	REFERENCE	DESCRIPTION
R _W NE	MIS 5 , 12 MIS 6, 13	Reset LINE. Single pulse started by MASTER RESET. Pulselength is about 1 mS. Used to disconnect the communication lines.
$\overline{r}$, RLINE	MIS 5, 12 MIS 1 - 4 MIS 8 - 11	Same as above.
REQTS X	MIS 5, 12 MIS 6, 13 MIS 1 - 4 MIS 8 - 11	REQ <u>U</u> est To Send x. Output signal from the Holding Register for Modem Control Signals. This signal is set and reset by bit 9 in a WRITE CONTROL command; x corresponds to the binare value of ADD OUT 0 - 3. MASTER RESET clears this register.
REQUEST TO SEND X	MIS 1 - 4 MIS 8 - 11 J 2 - J 17	Control signal to the modem. This signal commands the modem to transmit carrier to the remote station. NOTE 2.
$\overline{r}$, SEL CNTL	IOI 2 IOI 6 IOI 8	$\overline{r}$, SE <u>L</u> ect Co <u>N</u> Trol. Single pulse generated when a WRITE CONTROL header is decoded. Used to start the CONTROL STROBE pulse if bit 15 = 0 in the WRITE CONTROL word. Pulselength is about 100 nS.

SIGNAL NAME	REFERENCE	DESCRIPTION
SEL CNTL	IOI 8	Same as above.
	IOI 8	Used to start the SCANNER if bit 15 = 1 in the WRITE CONTROL word, to start the MASTER RESET pulse if bit 8 = 0.
7 SEL DA REG	IOI 1	7 SElect DAte REGister.
	IOI 8	Single pulse generated when a WRITE DATA header is decoded. Used to start the DATA STROBE pulse. Pulselength is about 100 nS.
SEL DA REG	IOI 8	Same as above.
	MIS 6	Used to reset the FF, in the BLOCKING OF TRM ITR circuit,
	MIS 13	selected by ADD OUT 0-3.
7 SELECT x	TRU 2, 12	This signal places the received data
	TRU 3 - TRU 10	character from device x onto the
	TRU 13- TRU 20	output lines (RD 1 - 8) and the status word bits onto the output lines (PE, FE, OR, DA, TBMT). x is the device at which the SCANNER points.
SHIFT CLOCK	IOI 2	Shift clock to the DATA OUT
	IOI 1	register.
SHIFT IN	IOI 3	Serial data from the DATA IN/STATUS
	IOI 4	register to the Header Generator.

SIGNAL NAME	REFERENCE	DESCRIPTION
¬, SITR	IOI 5	¬, Send InTeRrupt.
	IOI 1	Signal to the modulator, when the LAM wants to send an interrupt to RC 3500, causing a logic 1 to be sent on the data lines DATA IN A-B.
¬, STOP SCAN	IOI 5	¬, STOP SCANner.
	IOI 6	Output from the STOP SCAN FF. This FF is set by the leading edge of ITR CLOCK if ¬, EITR = 0. This FF is reset by ¬, SITR = 0. ¬, STOP SCAN = 0 is used to stop the SCANNER.
TBMT	TRU 3 - TRU 10	Transmitter Buffer eMpTy.
	TRU 13-TRU 20	TBMT = 1 indicates that the data
	MIS 5	bits holding register at which the
	MIS 12	SCANNER points may be loaded with another character from RC 3500.
TRANSMITTED DATA x	TRU 3 - TRU 10	Serial output data to the modem.
	TRU 13- TRU 20	HIGH level corresponds to logic 0.
	J 2 - J 17	NOTE 2.

SIGNAL NAME	REFERENCE	DESCRIPTION
110 bps	IOI 7 TRU 3 - TRU 10 TRU 13 - TRU 20	Clock signal. Frequency 16 x 110 HZ.
300 bps	IOI 7 TRU 3 - TRU 10 TRU 13- TRU 20	Clock signal. Frequency 16 x 300 HZ.
600 bps	IOI 7 TRU 3 - TRU 10 TRU 13- TRU 20	Clock signal. Frequency 16 x 600 HZ.
1200 bps	IOI 7 TRU 3 - TRU 10 TRU 13- TRU 20	Clock signal. Frequency 16 x 1200 HZ.
0,3072 MHZ	IOI 7 IOI 6	Clock Signal. Used to step the SCANNER.

Logical the LAM interface is divided into three parts:

1. I/O Interface (IOI).
2. Transmitter/Receiver Unit (TRU).
3. Modem interface and Status Selectors (MIS).

In the following each unit is further described.

I/O Interface.

The IOI takes care of the communication between RC 3500 and the LAM. For details refer to blockdiagram fig. 3.

Line Receiver and Demodulator.

For details refer to IOI 1.

Two balanced signals are received from RC 3500, serial data on DATA OUT A-B and clock on CLOCK OUT A-B.

By using transformer coupling galvanic separation is obtained between RC 3500 and the LAM interface

In the demodulator the serial data stream is synchronized with the received clock so that a negative shift on DATA OUT corresponds to a trailing edge on CLOCK OUT.

Line Driver and Modulator.

For details refer to IOI 1.

In the modulator the serial data (DATA IN) and the interrupt signal ($\neg$ SITR) are mixed, because an interrupt is sent as a logic 1 element on the data lines DATA IN A-B. RC 3500 decodes a logic 1 on DATA IN A-B as an interrupt whatever moment an input instruction (Read Data, Read Status) is not in progress on the I/O channel in question.

DATA OUT Register and HEADER DECODER.

For details refer to IOI 2 and TC 1.

The serial data received on DATA OUT is shifted into the DATA OUT register. The received word contains 20 bits, 16 data bits and 4 header bits. When the first synchronization bit in the Header is recognized in the bottom of the register, the SHIFT CLOCK is stopped and the header is decoded in accordance with the following table.

Command	Header				Strobe pulse
	1	x ₁	x ₂	1	
WRITE CONTROL	1	1	1	1	SEL CNTL
WRITE DATA	1	0	1	1	SEL DA REG
READ DATA	1	0	0	1	LOAD DATA
READ STATUS	1	1	0	1	LOAD STATUS

↑
First bit on DATA OUT

The strobe pulses are delayed min. 1 period of the internal clock CLOCK IN to secure that the selectors and decoders driven by ADD OUT 0-3 are calmed down before strobing.

DATA IN/STATUS Register and Header Generator.

For details refer to IOI 3 and IOI 4.

This is a 20 bits parallel to serial shift register.

If a READ DATA Header is decoded, the strobe pulse LOAD DATA loads the register with the Read Data word; and the contents of the register is shifted serial to the demodulator (section 7.1.3) by CLOCK IN. The Read Data word is 16 bits.

If a READ STATUS Header is decoded, the strobe pulse LOAD STATUS loads the register with the Status word; and the contents of the register is shifted serial to the modulator (section 7.1.3) by CLOCK IN. The Status word is 8 bits.

The Header contains the following information:

Command	Header			
	1	x ₁	x ₀	1
READ DATA	1	0	0	1
READ STATUS	1	0	0	1


 The first bit sends on
DATA IN

The SCANNER.

For details refer to IOI 6 and TC 2.

The SCANNER is a 4 bits counter. The outputs from the SCANNER is used to address the U-ART circuits. The SCANNER is stopped by simply blocking the clock input to the counter.

The SCANNER is stopped by $\neg$ MASTER RESET = 0 (section 7.1.7) or $\neg$ STOP SCAN = 0 (section 7.1.6).

The SCANNER is started again by a WRITE CONTROL command with bit 15 = 1 ($\neg$ DOUT 15 = 0).

The SCANNER is stopped on the trailing edge of ITR CLOCK.

INTERRUPT CIRCUIT.

For details refer to IOI 5 and TC 2.

Whenever data is received from RC 3500 (CLOCK OUT is pulsed) a monostable is started to block transmission of interrupts. The monostable runs 6 μ S after the last CLOCK OUT pulse, to secure that the data word as response to a READ DATA command is transmitted to RC 3500 before enabling interrupt transmission.

If the SCANNER selects a device ready to receive a character from RC 3500 or with a character ready to RC 3500 $\neg$ EITR shifts low.

On the leading edge of ITR CLOCK the $\neg$ STOP SCAN FF is triggered ($\neg$ STOP SCAN = 0) causing the SCANNER to stop and an interrupt to be sent to RC 3500 ($\neg$ SITR).

If it was a device with a character ready to RC 3500 ($\neg$ DATA AVAILABLE = 0) the INPUT ITR FF is triggered too on the leading edge of ITR CLOCK (INPUT ITR = 1). The INPUT ITR FF is reset by $\neg$ MASTER RESET = 0 (section 7.1.7) or $\neg$ RESET ITR = 0 (section 7.1.7). The INPUT ITR signal is sent to RC 3500 as bit 15 in the Read Data word as information about what kind of interrupt it was.

STROBE GENERATOR.

For details refer to IOI 8 and TC 1.

If a WRITE CONTROL command with bit 8 = 0 (DOUT 8 = 0) is received a 1 μ S MASTER RESET pulse is generated.

If a WRITE CONTROL command with bit 15 = 0 ($\neg$ DOUT15 = 1) is received a 300 nS CONTROL STROBE pulse is generated.

If a READ DATA command is received as response at a character ready interrupt (INPUT ITR = 1) a 1 μ S RESET ITR pulse is generated.

If a WRITE DATA command is received a 300 nS DATA STROBE pulse is generated.

CLOCK OSCILLATOR AND FREQUENCY DIVIDER.

For details refer to IOI 7.

The clock generator delivers the shift frequency to the DATA IN/STATUS register (CLOCK IN), the step-frequency to the SCANNER (0,3072 MHZ) and the clock signals to the Transmitter/Receiver Unit (110 bps - 300 bps - 600 bps - 1200 bps).

TRANSMITTER/RECEIVER Unit.

3.0

For details refer to Blockdiagram fig. 4.

The TRU unit accepts parallel data information from the IOI and transmits this information serial to the communication line selected by RC 3500. On the other side the TRU unit accepts serial input from the communication lines and when a whole character is received this character, together with information about which communication line the character comes from, is ready for the IOI interface.

STROBE MULTIPLEXERS

3.1

For details refer to TRU 2, TRU 12 and TC 1.

The signal DATA STROBE (section 7.1.7) and the signal CONTROL STROBE (section 7.1.7) are multiplexed to the channel x as the signals $\neg DS\ x$ and $CS\ x$; where x is the binary value of ADD OUT 0-3.

The signal RESET ITR (section 7.1.7) is multiplexed to the channel x , at which the SCANNER points (ADD IN 0-3), as the signal $\neg RDA\ x$. In a BCD to decimal decoder the value of the outputs from the SCANNER-counter (ADD IN 0-3) is decoded to a single signal to each U-ART circuit, $\neg SELECT\ x$.

HOLDING REGISTER FOR CLOCK SELECT.

3.2

For details refer to TRU 1, TRU 11.

This is a 16 bits memory, 2 bits for each device.

By means of CONTROL STROBE (section 7.1.7) the contents of bit 1-2 (DOUT 1 - 2) in the WRITE CONTROL word is loaded into the memory cells addressed by ADD OUT 0-3.

The output signals CLOCK SEL Ax and CLOCK SEL Bx are used to select the transmission speed for device x .

CLOCK SELECTOR

3.3

For details refer to TRU 3, TRU 13 - TRU 20.

There is one selector for each device. By means of the signals CLOCK SEL Ax and CLOCK SEL Bx (section 7.2.2.) the selectors can select between 4 possible transmission speeds (110 bps - 300 bps - 600 bps - 1200 bps).

Universal Asynchronous Receiver/Transmitter (U-ART)

3.4

The Universal Asynchronous Receiver/Transmitter is an LSI subsystem which accepts binary characters from either a terminal device or the I/O interface and receives/transmits this character with appended control and error detecting bits. All character contain a start bit, 5 to 8 data bits, one or two stop bits, and either odd/even parity or no parity. The number of data bits/char, parity mode and the number of stop bits are externally selectable. For details refer to Blockdiagram fig. 5 and TRU 3 - TRU 10, TRU 13 - TRU 20.

Transmitter Operation.

3.4.1

Power is applied, external reset is enabled by a WRITE CONTROL command and clock pulse is applied having a frequency of 16 times the desired baud rate. The above conditions will set TBMT, EOC (End of Character) and SO (serial output) to logic 1 (line is marking).

After initializing is completed the control Bits Holding Register is loaded with information about number of data bits/char, parity mode and the number of stop bits (DB1 - 5) by the signal CSx (section 7.2.1).

The Data Bits Holding Register is loaded with a data character (DB 1 - 8) by pulsing DSx (section 7.2.1). Once DSx is pulsed the TBMT signal will change from logic 1 to a logic 0 indicating that the Data Bits Holding Register is filled with a previous character and is unable to receive new data bits, and Transmitter Shift Register is transmitting

previously loaded data. When Transmitter Shift register is empty, data bits in the holding register are immediately loaded into the Transmitter Shift Register for transmission. The shifting of information from the holding register to the Transmitter Shift Register will be followed by SO and EOC going to a logic 0, and TBMT will also go to a logic 1 indicating that the shifting operation is completed and that the Data Bits Holding Register is ready to accept new data. It should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering, (separate Data Bits Holding Register and Transmitter Shift Register).

Data Transmission is initiated with transmission of a start bit, data bits, parity bit (if desired) and stop bit (s). When the last stop bit has been on line for one bit time, EOC will go to logic 1 indication that new character can be transmitted. This new character will be transmitted only if TBMT is a logic 0 as was previously discussed.

The signal TBMT is gated out of the U-ART circuit by $\neg$ SELECT x (section 7.2.1).

Receiver Operation.

3.4.2.

Power is applied, external reset is enabled by a WRITE CONTROL command and Clock pulse is applied having a frequency of 16 times the desired baud rate. The previous condition will set DA (Data Available) to a logic 0.

After initializing is completed, the user should note that one set of control bits will be used for both receiver and transmitter making individual control bit setting unnecessary. Data reception starts when serial input signal changes from logic 1 (marking) to logic 0 (spacing) which initiates a start bit. The start bit is valid if, after transition from logic 1

to logic 0, the SI line continues to be at logic 0, when carrier sampled, 8 clock pulses later. If, however, line is at logic 1 when center sampling occurs the start bit verification process will be reset. If the serial input line transitions from a logic 1 to a logic 0 (marking to spacing) when the 16 x clock is in a logic 1 state, the bit time, for center sampling will begin when the clock line transitions from a logic 1 to a logic 0 state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit (s) reception proceeds in an orderly manner.

While receiving parity and stop bit (s) the receiver will compare transmitted parity and stop bit (s) with control data bits (parity mode and number of stop bits) previously set and indicate an error by changing the parity error FF and/or the framing error FF to a logic 1. It should be noted that if the no parity mode is selected the PE (parity error) will be unconditioned set to a logic 0.

Once a full character is received, internal logic looks at the data available (DA) to determine if data has been read out. If the DA signal is at a logic 1 the receiver will assume data has not been read out and the overrun FF of the status word holding register will be set to a logic 1. If the DA signal is at a logic 0 the receiver will assume that data has been read out. After DA goes to a logic 1 the Receiver Shift Register is now ready to accept the next character and RC 3500 has one full character time to remove the received character.

The contents of the Data Bits Holding Register is strobed onto the output line (RD 1 - 8) by the signal $\overline{\text{SELECT}}$.

The contents of the Status Bits Holding Register is strobed onto the output lines (DA, FE, PE, TBMT) by same signal $\overline{\text{SELECT}}$ (section 7.2.1). The data available FF is reset by the signal $\overline{\text{RDA}}$ x (section 7.2.1).

Modem Interface and Status Selectors.

4.0

This unit takes care of setting the correct control signals to the modems and select status from the modem requested from the IOI unit.

For details refer to Blockdiagram fig. 6.

Modem Drivers and Receivers.

4.1

For details refer to MIS 1-4, MIS 8-11.

There are drivers for the modem control signals CONNECT TO LINE and REQUEST TO SEND; receivers for DATA SET READY, READY FOR SENDING and DATA CARRIER DETECTOR.

CONNECT TO LINE $x = 1$ (CNTL $x = 1$) commands the modem x to connect to the communication line; if the modem power is switched on and the modem is not in a test mode, the modem will answer with DATA SET READY $x = 1$ ($\neg$ DSRDY $x = 0$).

REQUEST TO SEND $x = 1$ (REQTS $x = 1$) commands the modem x to transmit carrier to the remote station, the modem answers with READY FOR SENDING $x = 1$ ($\neg$ RDYFS $x = 0$) when it is ready to transmit data (max. delay 200 mS).

DATA CARRIER DETECTOR $x = 1$ ($\neg$ DACAR $x = 0$) when the modem x receives carrier from the remote station within appropriate limits.

Holding Register for Modem Control Signals.

4.2

For details refer to MIS 5 and MIS 12.

This logic unit contains two 8 bit adressable latches which store single line data in the addressed latch. There is one latch for the signal CNTL x (section 7.3.1) and another for the signal REQTS x (section 7.3.1).

The latches addressed by ADD OUT 0-3 is loaded with bit 9-10 (DOUT9-10) in the WRITE CONTROL word by the signal CONTROL STROBE (section 7.1.7).

All latches are cleared (CNTL x = 0 and REQTS x = 0) by

-, MASTER RESET = 0 (section 7.1.7).

-, MASTER RESET = 0 starts a 1 mS pulse RLINE (Reset line).

This pulse is used to secure that the modems really removes the carrier in the situation: The program sends a WRITE CONTROL with bit 8 = 0 (MASTER RESET = 1) and immediately in the next instruction sends a WRITE CONTROL with bit 10 = 1 (CONNECTION TO LINE = 1) and bit 9 = 1 (REQUEST TO SEND x = 1).

STATUS - Selectors.

4.3

For details refer to MIS 7 and MIS 14.

There is three STATUS - Selector one for each of the modem signals

-, DSRDY x, -, RDYFS x and -, DACAR x (section 7.3.1). These selectors are controlled by ADD OUT 0-3.

There is a selector more for the -, MODEM ERROR signal. This selector is controlled by the output signals (ADD IN 0-3) from the SCANNER-counter. If the SCANNER stops at a channel address, where -, DACAR x = 1 the signal -, MODEM ERROR switches to logic 0, setting the ERROR - bit in the READ DATA word.

Blocking of TRM Interrupts.

4.4

For details refer to MIS 6, MIS 13 and TC 2.

The function of this unit is blocking of TBMT = 1 interrupts from devices to which RC 3500 at the moment has no information, without breaking down the communication lines.

This circuit consists of 8 FF's with individually set and reset.

Whenever RC 3500 answers a TBMT = 1 interrupt (INPUT ITR = 0) with a READ DATA command the FF corresponding to the channel at which the SCANNER is stopped (the binary value of ADD IN 0-3) is set by the signal -, LOADDATA (section 7.1.3) on the assumption that -, REQTS x = 0.

If RC 3500 at the moment has not a new character to the channel x in question a WRITE CONTROL with bit 15 = 1 (START SCANNER) is sent to LAM interface causing the SCANNER to step forward again; when the SCANNER reaches the channel mentioned above again the signal OPEN TRM ITR = 0 will cause the SCANNER not to stop and no interrupt is sent to RC 3500.

When RC 3500 at later moment has a character ready to the channel x mentioned above, a WRITE DATA command with ADD OUT 0-3 = x is sent to the LAM causing the FF in question in the Blocking of TRM ITR circuit to be reset.

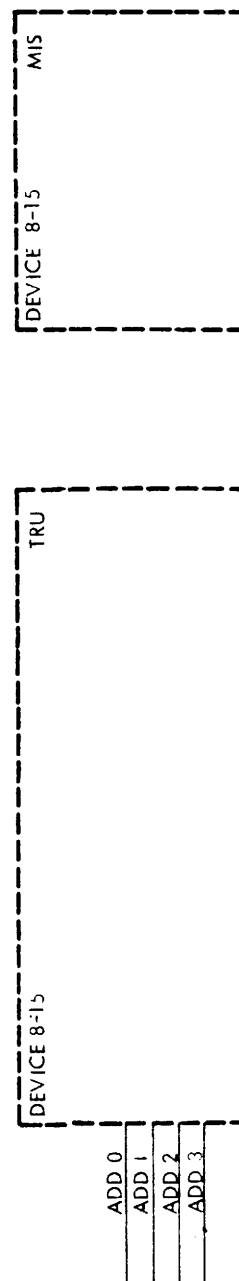
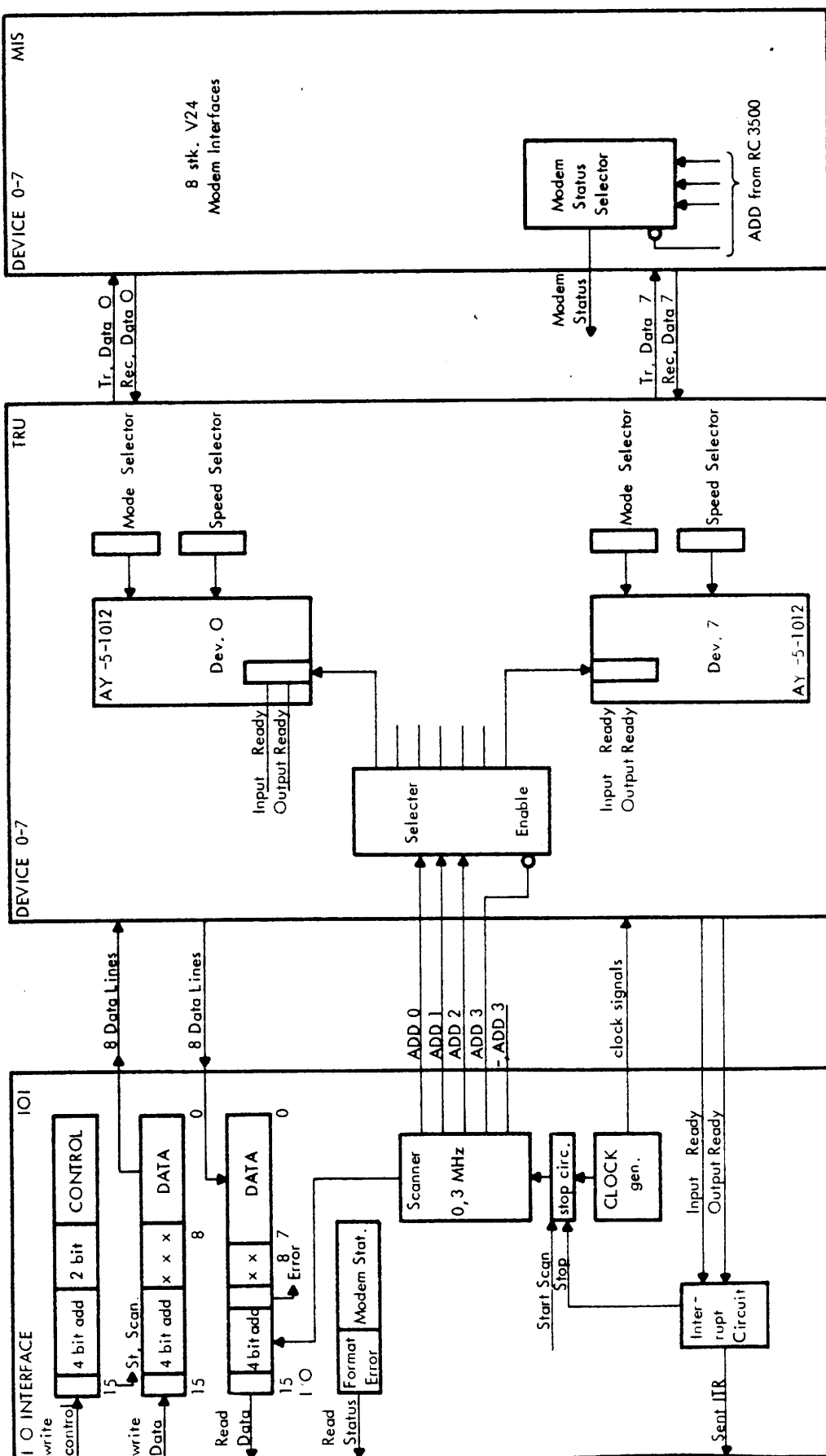
Interrupt Generator.

4.5

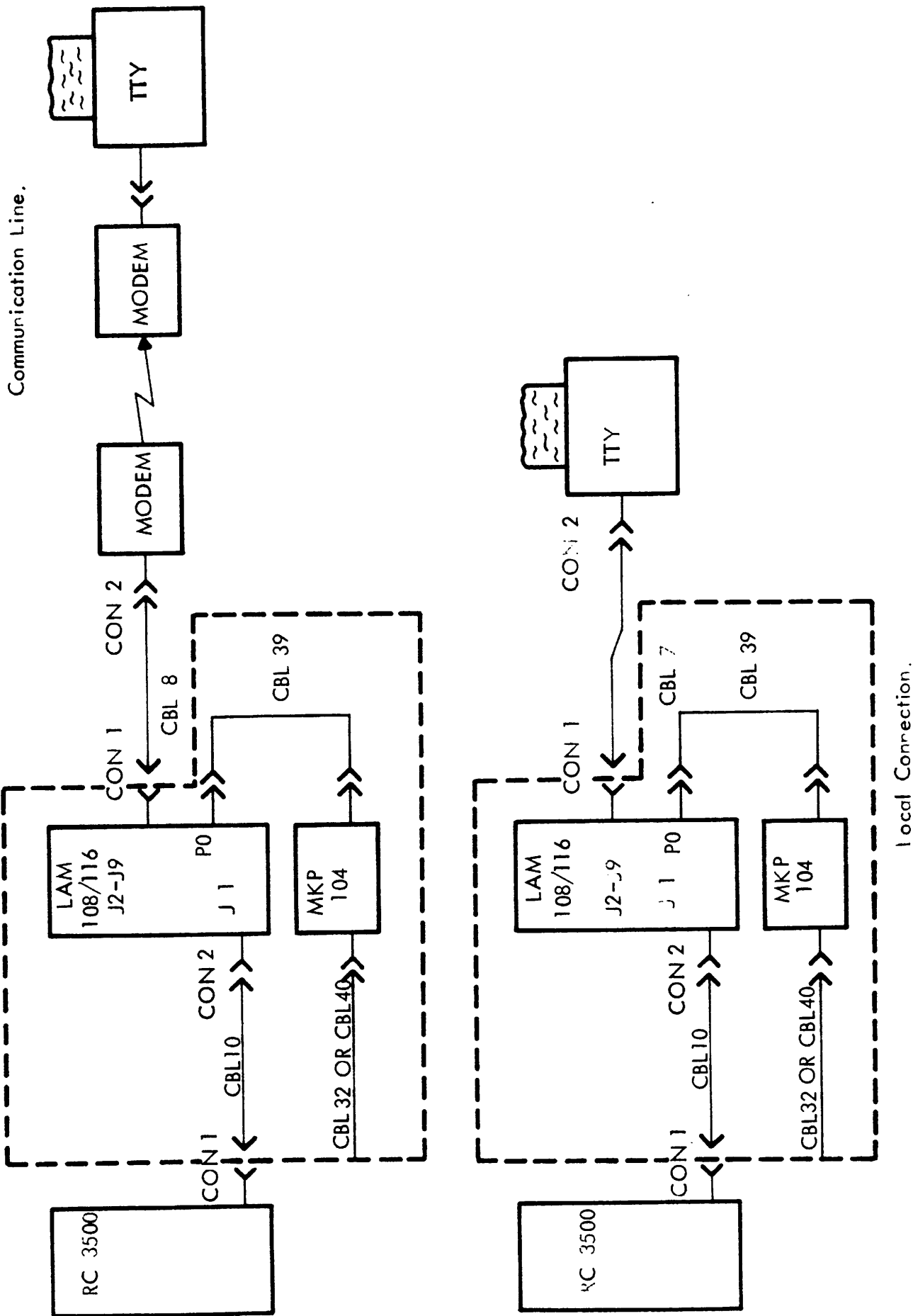
For details refer to MIS 5, MIS 12 and TC 2.

If DA = 1 (Data Available) the two signals $\neg$ EIR (Enable Interrupt) and $\neg$ DATA AVAILABLE switches to logic 0 giving set conditions to the STOP SCAN FF and the INPUT ITR FF (section 7.1.6)

If the SCANNER reaches a channel x (ADD IN 0-3) where DA = 0, TBMT = 1, OPEN TRM ITR = 1 and $\neg$ RDY FS x = 0 only the signal $\neg$ EITR switches to logic 0 giving set condition to the STOP SCAN FF but not to the INPUT ITR FF.



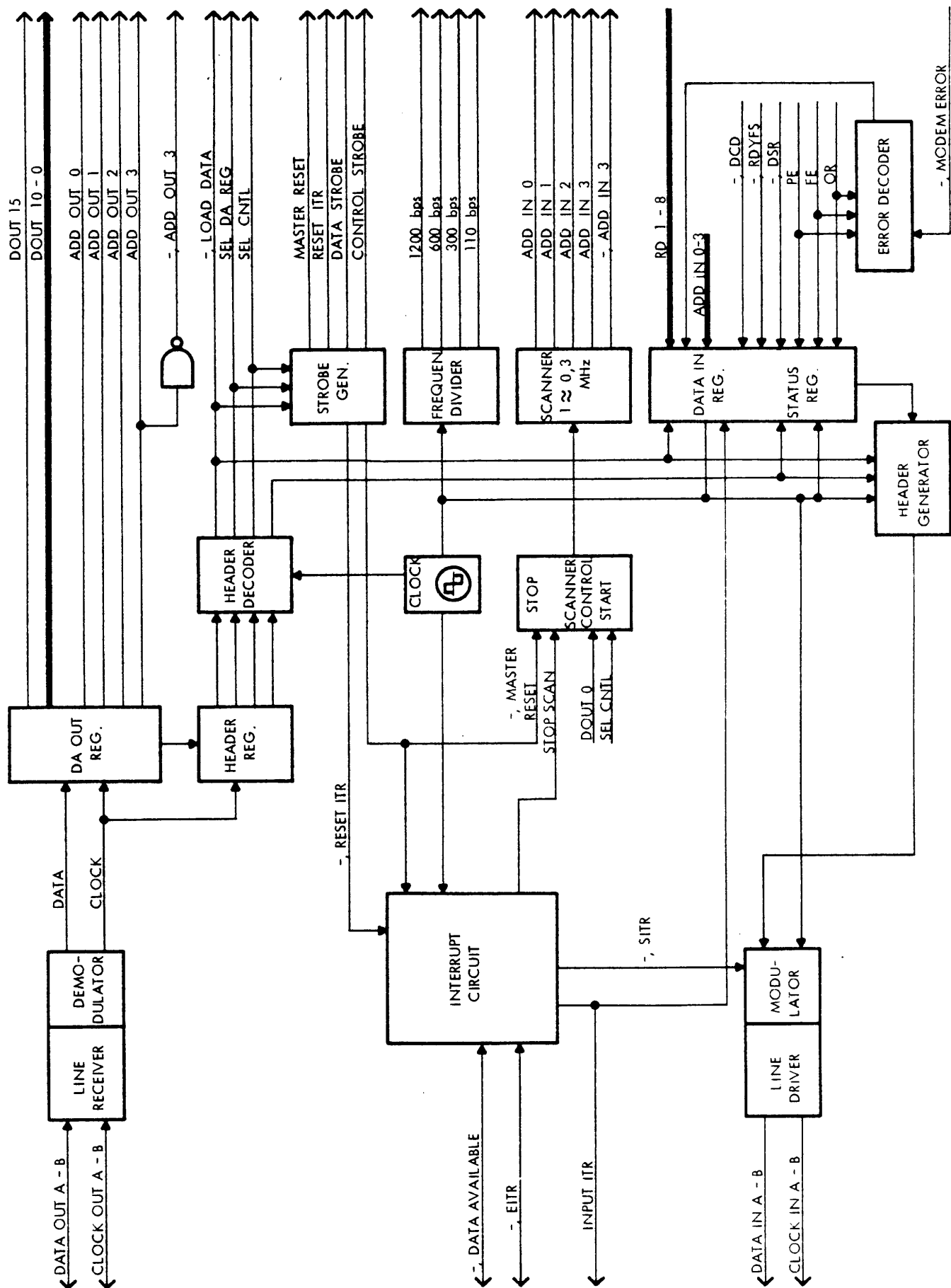
730302 KNEH 730508 AGS

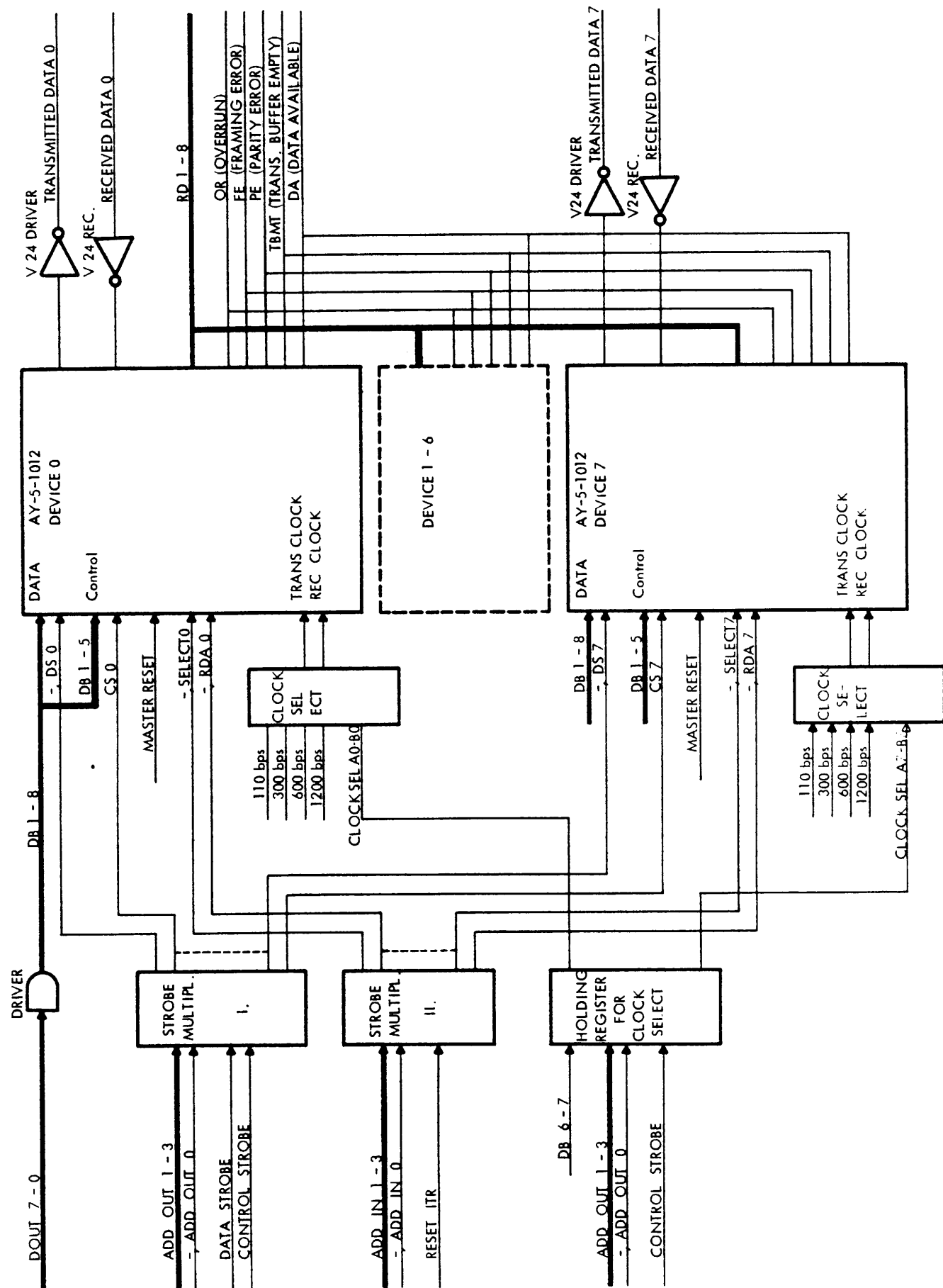


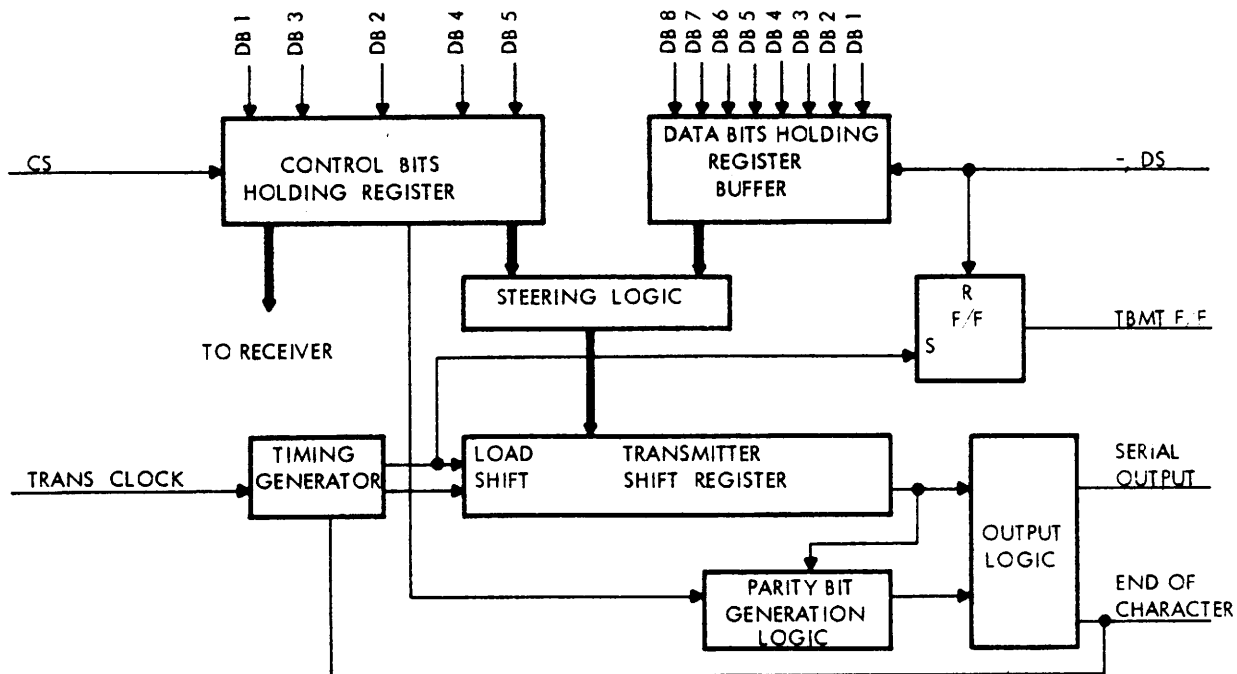
LAM108/116

A2211+

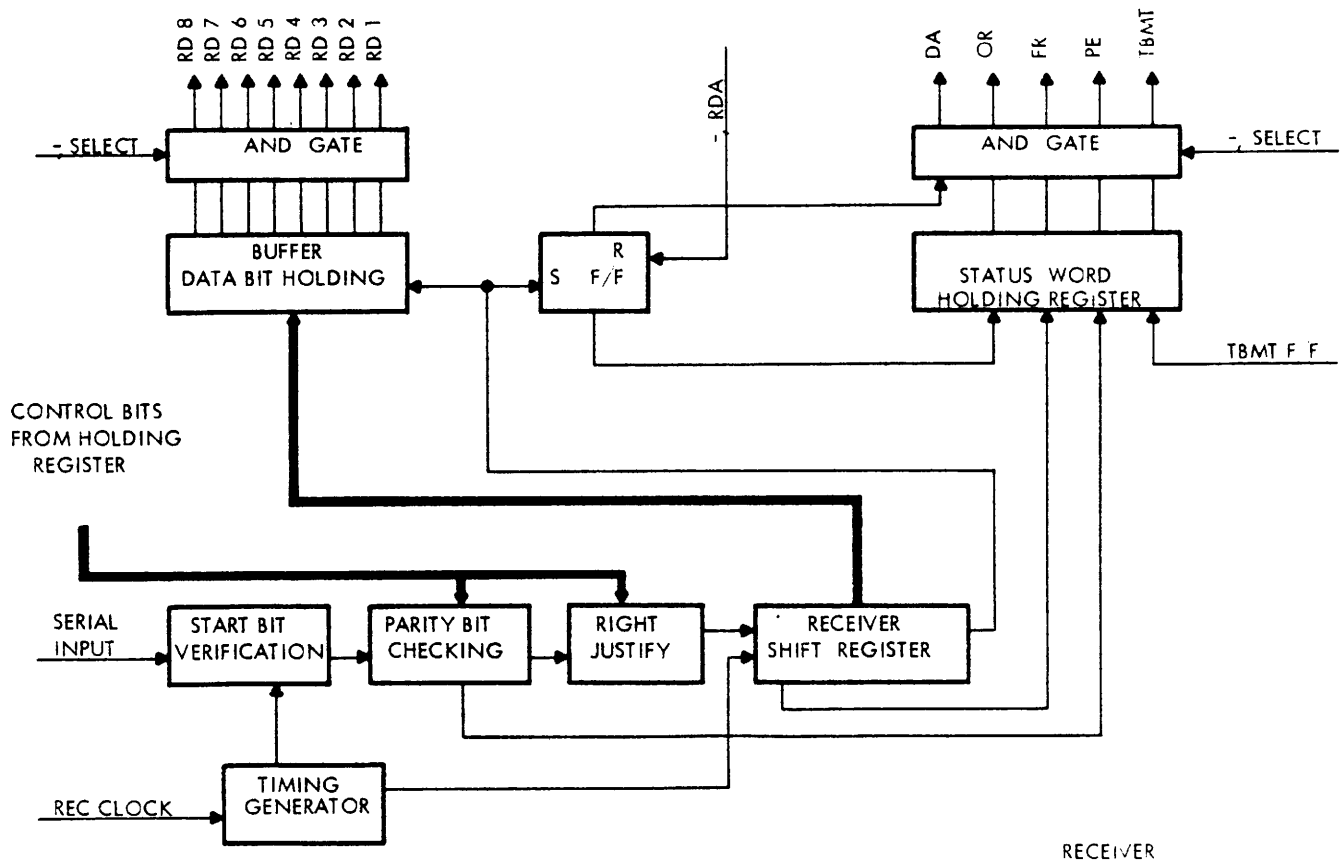
SYSTEM OUTLINE
BLOCK DIAGRAM
Figure



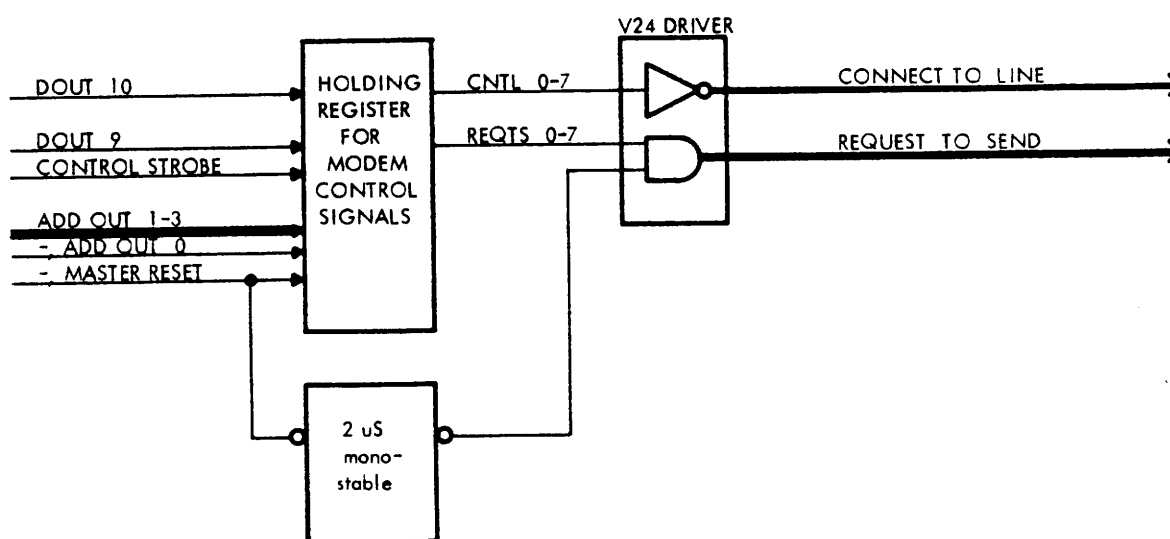
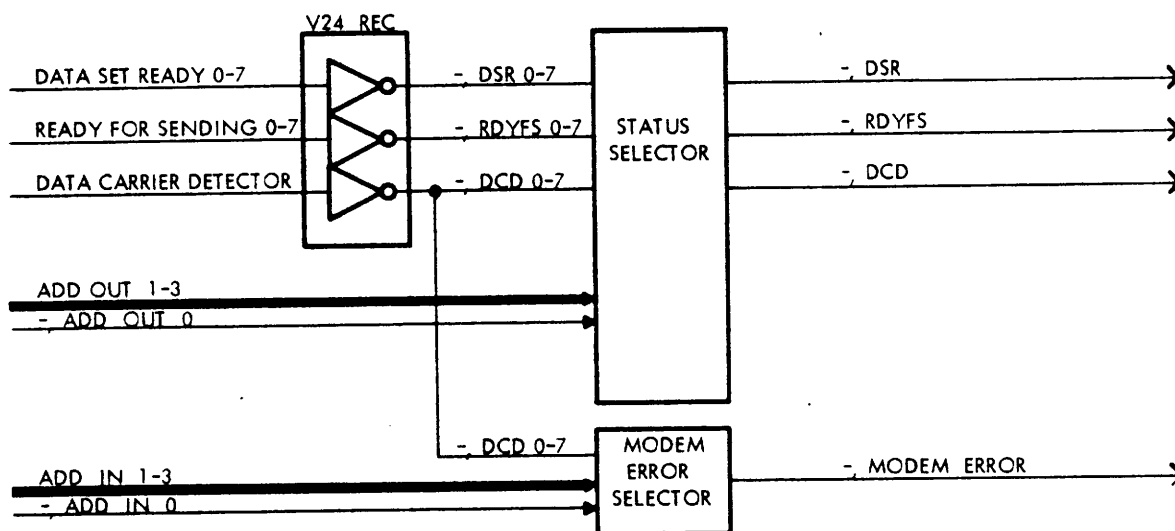
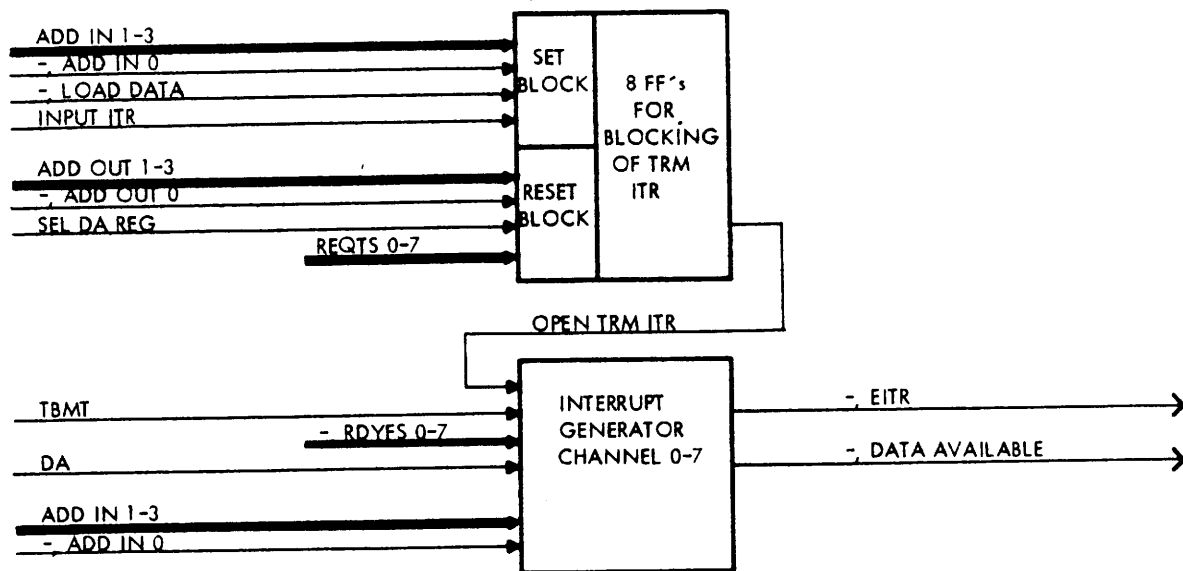




TRANSMITTER



RECEIVER



730227 KNEH 730831 IGH

For details refer to fig. 2.

Remote Connection.

Cable CBL 10 is used to connect RC 3500 and the LAM interface;
cable CBL 8 is used to connect the modem and the LAM interface.

NOTICE: From factory the modem signal FREQUENCY SELECT is strapped to low level in CON2 of cable CBL8(pin 10 to pin 11);
i.e. in the remote modem the same signal must be strapped to HIGH level (pin 11 to pin 12).

max. length of CABLE CBL 10 is 100 m.

max. length of CABLE CBL 8 is 15 m.

Local Connection.

Cable CBL 10 is used to connect RC 3500 and the LAM interface;
cable CBL 7 is used to connect the terminal in question directly to the LAM interface.

max. length of cable CBL 7 is 1000 m (if the transmission speed is not more than 110 bps).

8 channel version.

+ 5V $\pm$ 5%	2,6A
+ 12V $\pm$ 5%	120 mA
- 12V $\pm$ 5%	270 mA

16 channel version.

+ 5V $\pm$ 5%	4,1A
+ 12V $\pm$ 5%	200 mA
- 12V $\pm$ 5%	450 mA

RETURN LETTER

Title: General Information on
RC 35-103/104

RCSL No.: 52-AA663

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