
Title:

RC 8401

GENERAL INFORMATION

Keywords:

RC 8401, RC 8000, Peripheral Device,
FPA 801, Front-end Processor Adapter,
General Information.

Abstract:

This paper is a general information for
the RC 8401 front-end processor adapter.

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GENERAL INFORMATION

1

GENERAL DESCRIPTION

1.1

FPA 801 is an asynchronous communication controller intended for use as interconnecting medium between the RC 8000 computer and the RC 3600/RC 3500 computer.

FPA 801 contains two sub-devices, called the TRANSMITTER and the RECEIVER.

Normally, the transmitter part of FPA 801 is used to transmit a data block to the front end processor, and to receive a single status character as a respond to the transmitted block.

The receiver part is used to receive a data block, and to transmit a single status character as a respond to the received data block.

The communication with the front-end utilizes the asynchronous, fully interlocked technique. Each request signal from FPA 801 to front-end must be acknowledged by the front-end to complete the transfer.

When FPA 801 wants to transmit a character, the character is placed on the data lines and the request signal is raised. When the front-end has stored the character, it responds to the request signal by raising the request acknowledge signal, indicating the reception of the character. Upon the reception of the acknowledge signal, FPA 801 lowers the request signal, which causes the front-end to lower the acknowledge signal thus completing the transfer of the character.

The communication with RC 8000 CPU takes place via a unified bus.

Operations are started by means of an output operation, which starts the receiver or the transmitter. Hereafter the communication takes place via a channel program stored in the memory, which is also connected to the unified bus.

Once started FPA 801 fetches its commands in the channel program and executes these commands without the engagement of the CPU.

SPECIFICATIONS

1.2

Performance Specifications

1.2.1

Transmission rate:

Max 600,000 chars / sec.

Transmission mode:

Asynchronous on character by character basis,
fully interlocked.

Transmission Line:

A set of input lines and a set of output lines. The output and input lines are completely symmetrical, each set consisting of:

9 data lines incl. a parity line

7 control lines

Signals to/from Front-End:

- | | |
|--------------------------|---|
| Data lines 0:7 | : Data line 0 is MSB.
Data line 7 is LSB. |
| Parity line | : Odd parity is used |
| Last char line | : This line points out the last character in a block. |
| Data request | : Indicates to the receiving unit that a data character is ready on the data lines. |
| Status request | : Indicates to the receiving unit that a status character is ready on the data lines. |
| Request acknowledge line | : Indicates to the transmitting unit that |

the receiving unit has stored the transmitted character. This allows the transmitting unit to transmit the next character.

- Reset line : Areset signal is send to the opposite controller when the transmitter is reset.
- Connected line : This signal indicates to the opposite controller that power is on.
- Autoload line : This signal is used to initiate an autoload sequence in the opposite computer and visa versa.

Channel commands:

The transmitter part of FPA 801 as well as the receiver part is able to execute following channel commands:

- READ : receive characters from the opposite controller.
- Write : transmit characters to the opposite controller.
- Sense : transfer status to RC 8000 memory.
- Control : transmitter part: send autoload signal
receiver part: transmit an all zero status character.
- Wait : wait for an attention event or a new start.
- Stop : stop channel program.

Electrical specifications

1.2.2

Supply voltage:

$$5\text{vdc} \pm 5\%/6\text{A}$$

Bus towards CPU:

1. Bus characteristic

Bidirectional, open collector, separate data and address bus.

2. Signal representation

Logical 1 = low voltage

$$0\text{V} \leq V_{\text{out}_L} < 0\text{V}_{45}$$

Logical 0 = high voltage

$$4\text{V}_3 \leq V_{\text{out}_H}$$

3. Transceivers

Texas instrument SN75138

4. Cable

Characteristic impedance

$$120\Omega \pm 20\% \text{ unbalanced.}$$

Communication line towards Front-end:

1. Characteristic

Differential in and outputs $\pm 15\text{V}$ common mode input voltage range.

2. Signal representation

Logical 1 = line A positive relative to B

Logical 0 = line A negative relative to B

Line A or B high level min. 1V8

Line A or B low level max 0V4

3. Drivers/Receivers

Texas 75183 line drivers/Texas 75182 line receivers are used for control signals.

Fairchild 9612E line drivers / Fairchild 9613 line receivers are used for data out/in signals.

4. Cable

Characteristic impedance
app. 120E balanced.

Environmental Specifications

1.2.3

Ambient temperature : 10 - 40° C

Relative humidity : 20 - 80 % (no condensation)

Physical Specifications

1.2.4

FPA 801 logic is mounted on a standard RC 2301 PCB, which occupies one slot in a standard CHS 802 cassette.

IDENTIFICATION OF ITEMS

1.3

FPA 801 : Front-end processor adapter

CBL 803 : Autoload Cable

INSTALLATION

1.4

This section explains how the FPA 801 is installed in the CHS 802 cassette, and how to connect FPA 801 to the surrounding equipment. Strapping possibilities and adjustment of main device number selector is also explained.

Installation of controller

1.4.1

The FPA 801 PCB may be inserted in any position of the CHS 802 cassette.

PCB plug 1001 and 1002 connects FPA 801 to the RC 8000 bus.

PCB plug 1003 is not used.

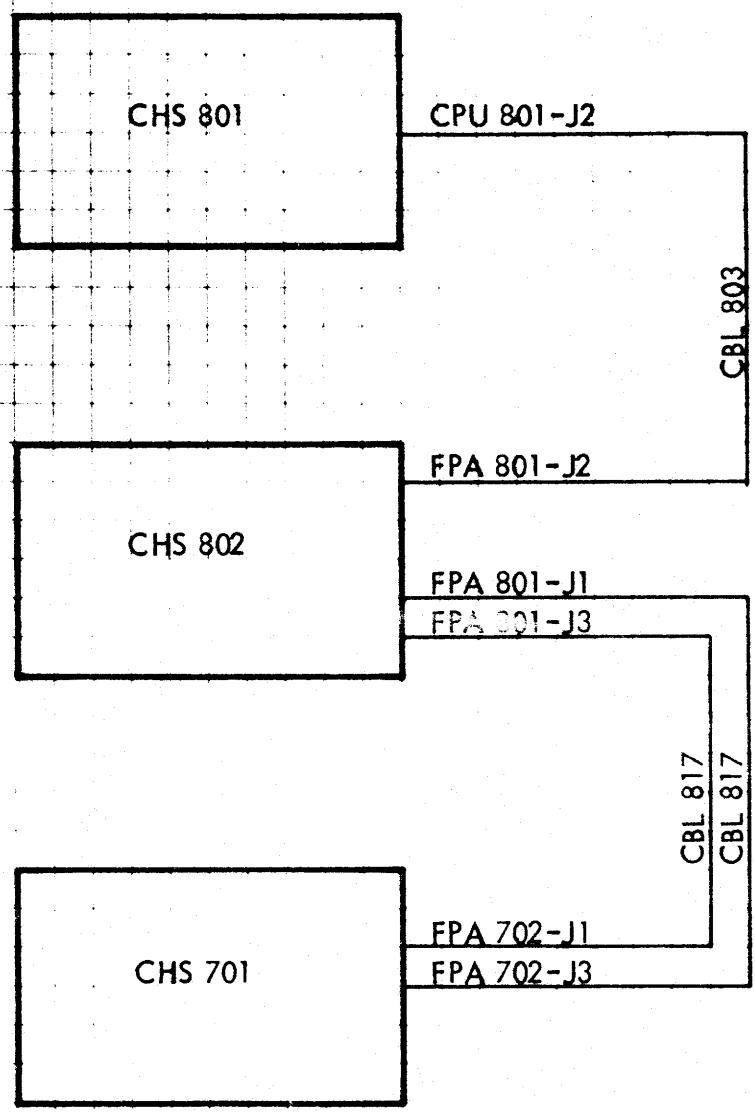
Via PCB plug 1005 characters are received from the front-end, and via PCB plug 1004 characters are transmitted to the front-end.

Rev. 10-1-76

Due to ECH

Ref. 10-1-76

760519 VH 761215 IGH



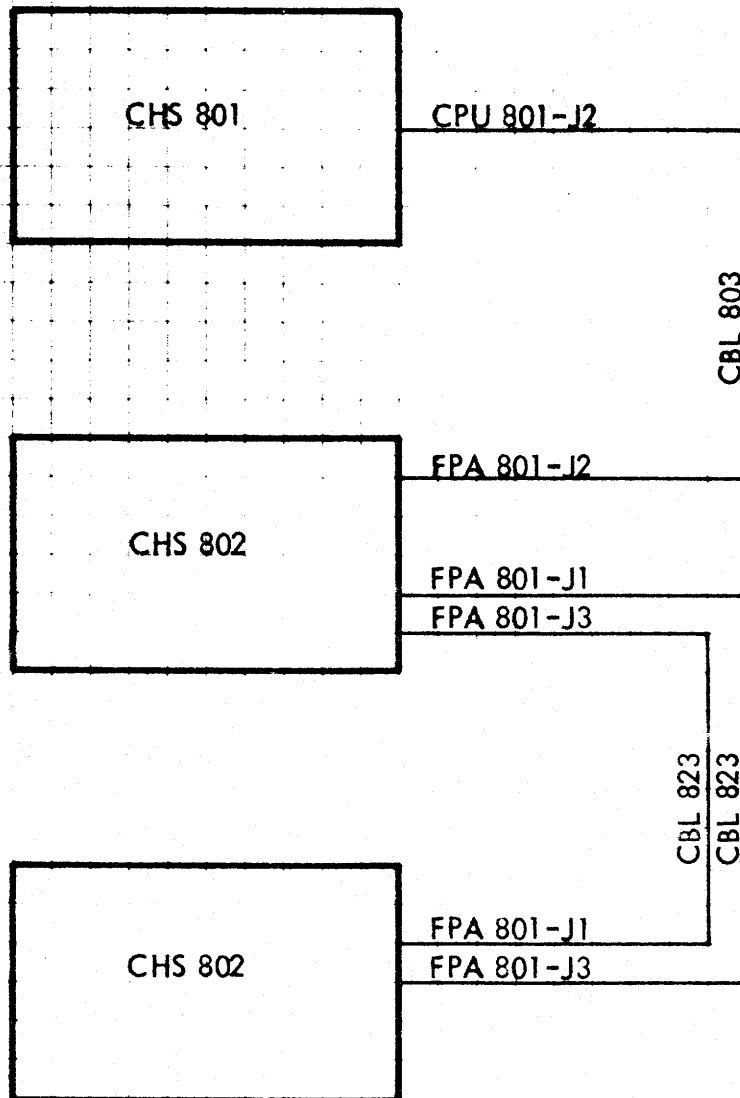
FPA 801

A24700

FPA 801 RC 8000 connected to FPA 702 RC 3600

Interconnection Diagram

760519 VH 761215 IGH



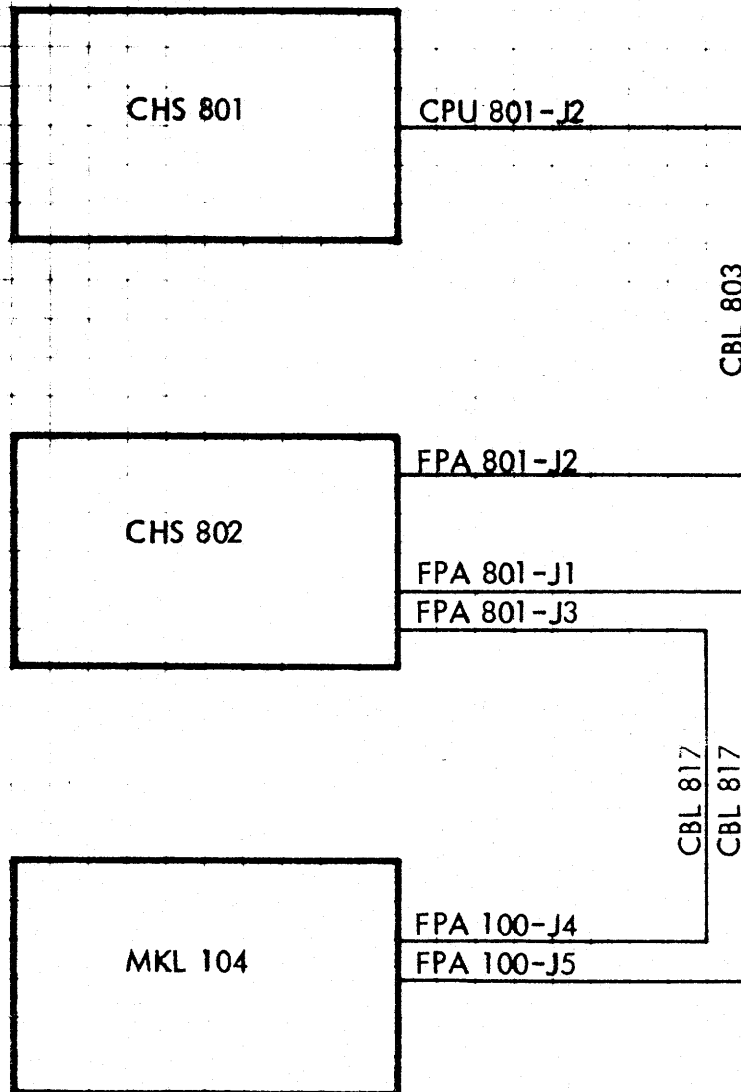
FPA 801

VR NG
A24701

FPA 801 RC 8000 connected to FPA 801 RC 8000

Interconnection Diagram

760512 VH 761215 JGH



FPA 801

Rev No
A24702

FPA 801 RC 8000 Connected to FPA 100 RC 3500

Interconnection Diagram

NOTE

The PCB board should not be removed from or inserted in the cassette while dc-power is present.

Concerning interconnections to the opposite controller refer to interconnection diagrams Dwg. no. A24700, A24701, and A24702.

Strapping Possibilities

1.4.2

Main device number switches

The main device number switches are located in position 72, and consists of 8 switches used to set the main device number and 1 switch used to make the parity of the main device number and the parity control switch even. The switches are shown in fig. 1.4.1

Position 72

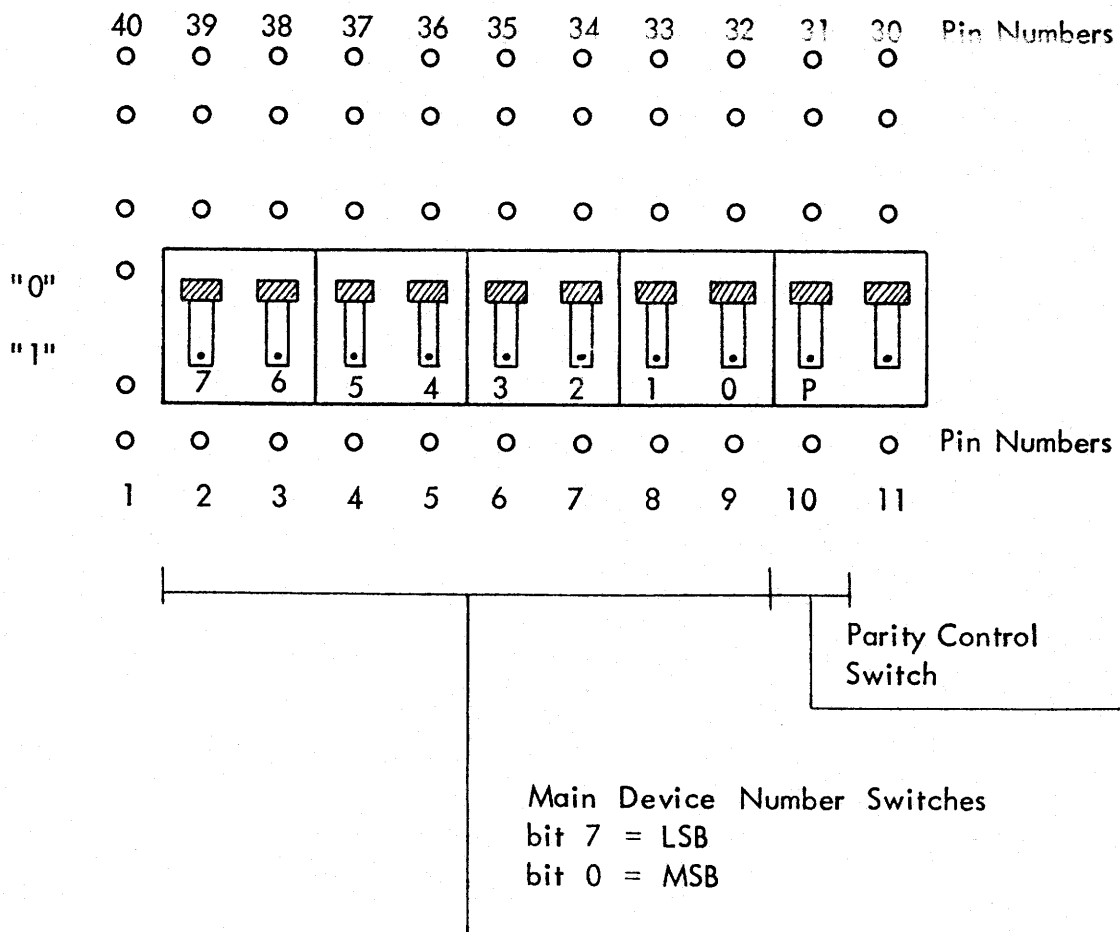


fig. 1.4.1

Strapping platform

In KT 525 Pos. 80 is included a strapping platform. When this platform is removed, the RUN/STOP and SINGLE STEP switches may be inserted. Refer to section 3 Diagram 1.

Front Panel

1.4.3

On the FPA 801 frontpanel is located one switch and two indicators. The switch is named "AUTOLOAD ENABLE / DISABLE", and is used to enable/disable the autoload signal relayed to the RC 8000 CPU.

The indicators are named "TRANSMIT" and "RECEIVE". The transmit indicator is switched on for app. 100 ms every time the data request signal to the opposite controller changes from false to true, thus indicating when data characters is being transmitted.

The receive indicator is switched on for app. 100 ms every time a data request from the opposite controller is acknowledged by FPA 801, thus indicating when data characters is being received.

Concerning logic mounted on the frontpanel PCB refer to section 3 Diagram 32. The frontpanel indicators are connected to the FPA 801 PCB via a dip-plug, which is inserted in dip-position 28.