
Title:

TECHNICAL MANUAL for
FPA 801, Front-end Processor Adapter.

Keywords:

RC 8401, RC 8000, Peripheral Device
FPA 801, Front-end Processor Adapter,
Technical Manual.

Abstract:

This publication is a Technical description of the front-end processor adaptor - FPA 801 - designed to connect the RC 8000 computer to the RC 3600 or RC 3500 computer.

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Internal receiver cable CBL 814 with signal names ..	Dwg.no. A12889
CBL 817 with signal names	Dwg.no. A12890

The FPA 801 is an asynchronous controller intended for use as interconnecting medium between the RC 8000 computer and the RC 3600 / RC 3500 computer.

FPA 801 contains two sub-devices, called the TRANSMITTER and the RECEIVER.

Although transmission cannot take place in both directions simultaneously, the FPA 801 acts from a programmers point of view as two independent devices, each running their own program simultaneously.

FPA 801 is constructed around a 24 bits wide tree-state bus (refer to BLOCK-DIAGRAM SECTION 3.1.2)

Sources to the bus are:

1. Register ALU (MMI 6701)
2. Data Selector, which gates following registers to the internal bus:
 - a.) Device selector switch
 - b.) I/O DATA-IN register
 - c.) Constant Proms
 - d.) Receiver Character register

Destinations on the bus are:

1. Register ALU (MMI 6701)
2. Data selector, which routes data to the transmitter character register
3. I/O DATA-OUT Register
4. I/O ADDRESS Register
5. Parity checker / generator

Transfer of data between registers on the bus is under control of the microprogram, which executes following macroinstructions under control of the RC 8000 computer:

- | | |
|-----------|---|
| a.) Read | receive characters from the opposite controller |
| b.) Write | transmit characters to the opposite controller |
| c.) Sense | transfer status to RC 8000 memory |

- d.) Control send autoloader signal or transmit an all zero character
- e.) Wait wait for an attention event or a new start
- f.) Stop stop channel program

The Register ALU holds the following 16 registers, of which 8 are assigned to the transmitter and 8 are assigned to the receiver :

- 0. Description Address
- 1. Channel Program Address
- 2. First Word Address
- 3. Character Counter
- 4. Buffer
- 5. Remaining Char. Count
- 6. Event status
- 7. Command register

The transmitter and receiver register names are identical.

Besides the above mentioned registers the Register ALU contain an arithmetic logic unit, which is used when counters and address registers has to be incremented / decremented and when status bits in the status register is set and cleared.

I/O DATA register and I/O ADDRESS register are via TEXAS 75138 transceivers connected to the RC 8000 standard bus. When I/O DATA register and I/O ADDRESS register data are present on the internal bus the parity is generated / checked by the Parity checker / generator.

Communication with RC 8000 takes place via the standard unified bus. Operations are initiated by means of an output operation, which addresses the receiver or the transmitter. Hereafter the communication takes place via a channel program stored in the memory. Once started FPA 801 fetches its commands in the channel program and executes the commands without the engagement of the CPU. Data to be written or read from front end are transferred directly between FPA 801 and memory.

When the channel program has been executed, it is normally terminated with a STOP command which transfers status to memory and interrupts the CPU.

The communication with the opposite controller takes place via a set of output and a set of input lines. The output lines and input lines are completely symmetrical, each set consisting of:

9 data lines incl. a parity line

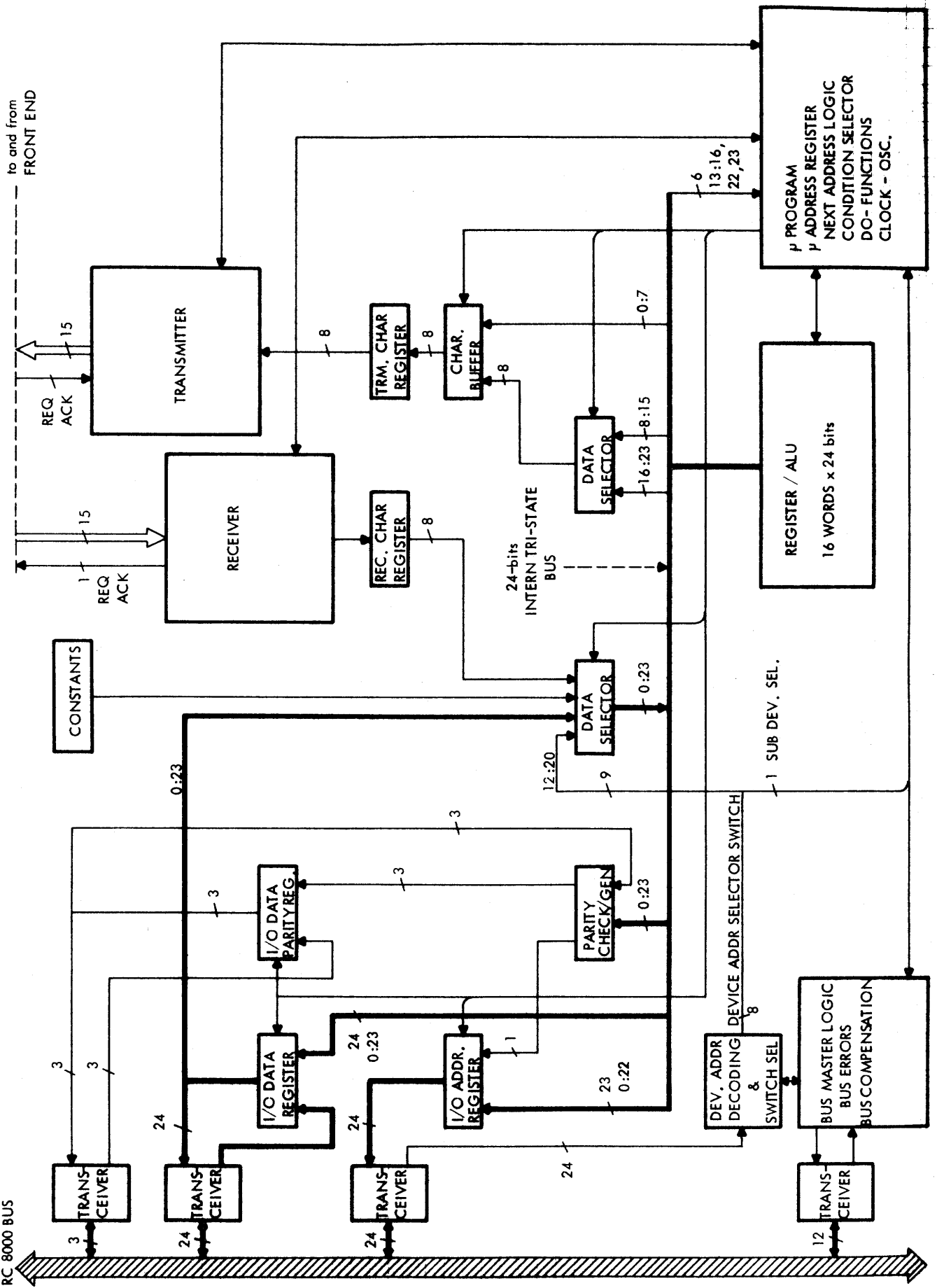
7 control lines

Included in the control lines is an autoloading request line, which is necessary to be able to initiate an autoloading procedure in the opposite controller under RC 8000 program control and vice versa. The communication is asynchronous on character basis.

RC 8000 BUS

FPA 801

A12899



Block Diagram

CP 2

μ ADDRESS REG

NEXT ADDRESS PROMS

EKS. 1

- BUS RDY
- BUS ERROR
- CONDITION 0

- CONDITION 1

EKS. 2 (WORST CASE)

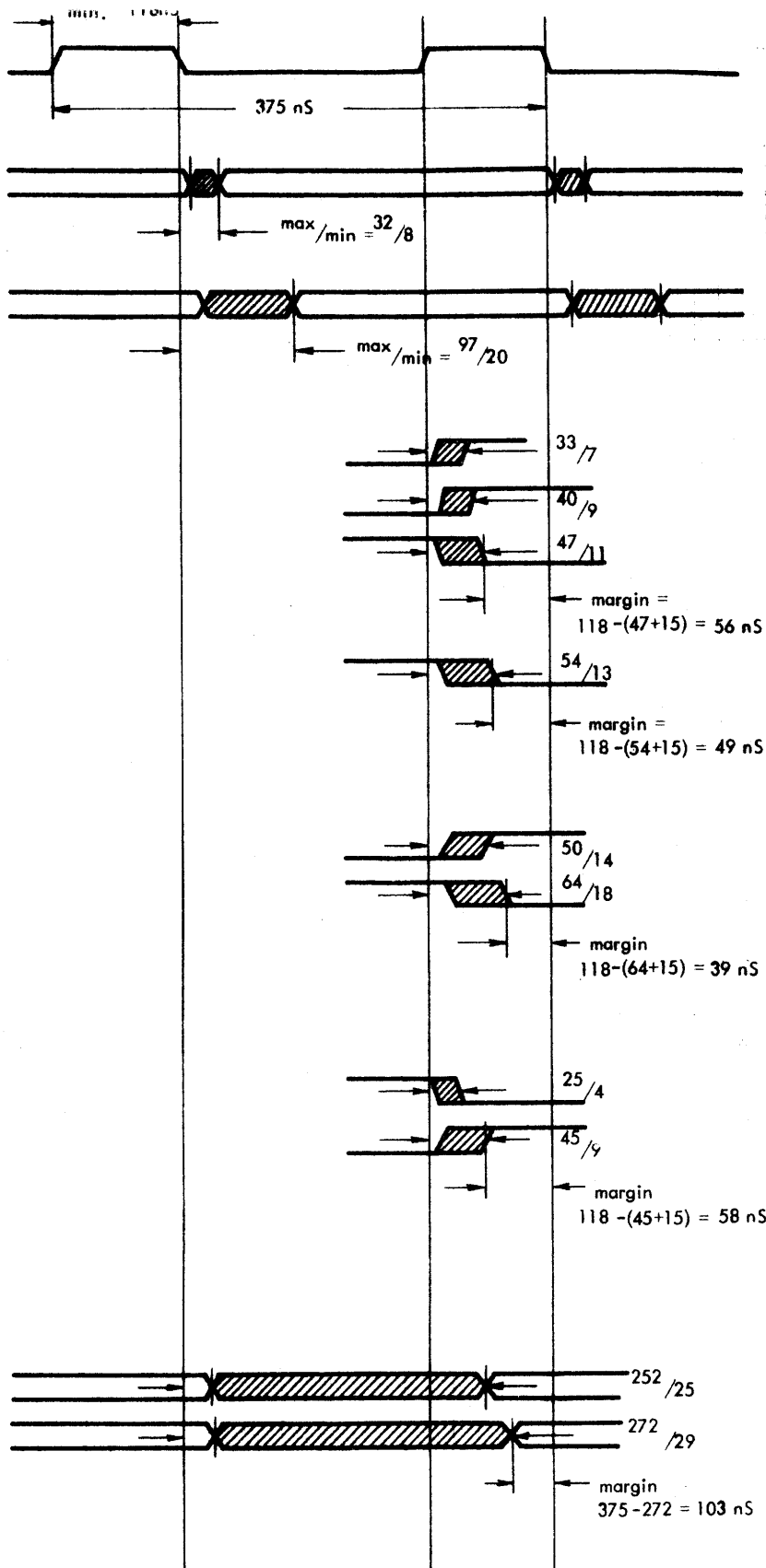
- TRANSMITTER DONE
- CONDITION 0

EKS. 3

- REC DONE
- CONDITION 0

EKS. 4

- CONDITIONS FROM RALU
(INTERN BUS 22, 23)
- CONDITION 0 or 1



SHADED AREAS = UNDEFINED STATE

CP 2

INTERNAL BUS
(DATA FROM REGISTER
ALU)

The min value is composed
of :

CP 2 → μ ADDR. REG.	8
μ ADDR. REG. → SOURCE ADDR 12	
SOURCE ADDR → BUS	5
	~ 25 nS

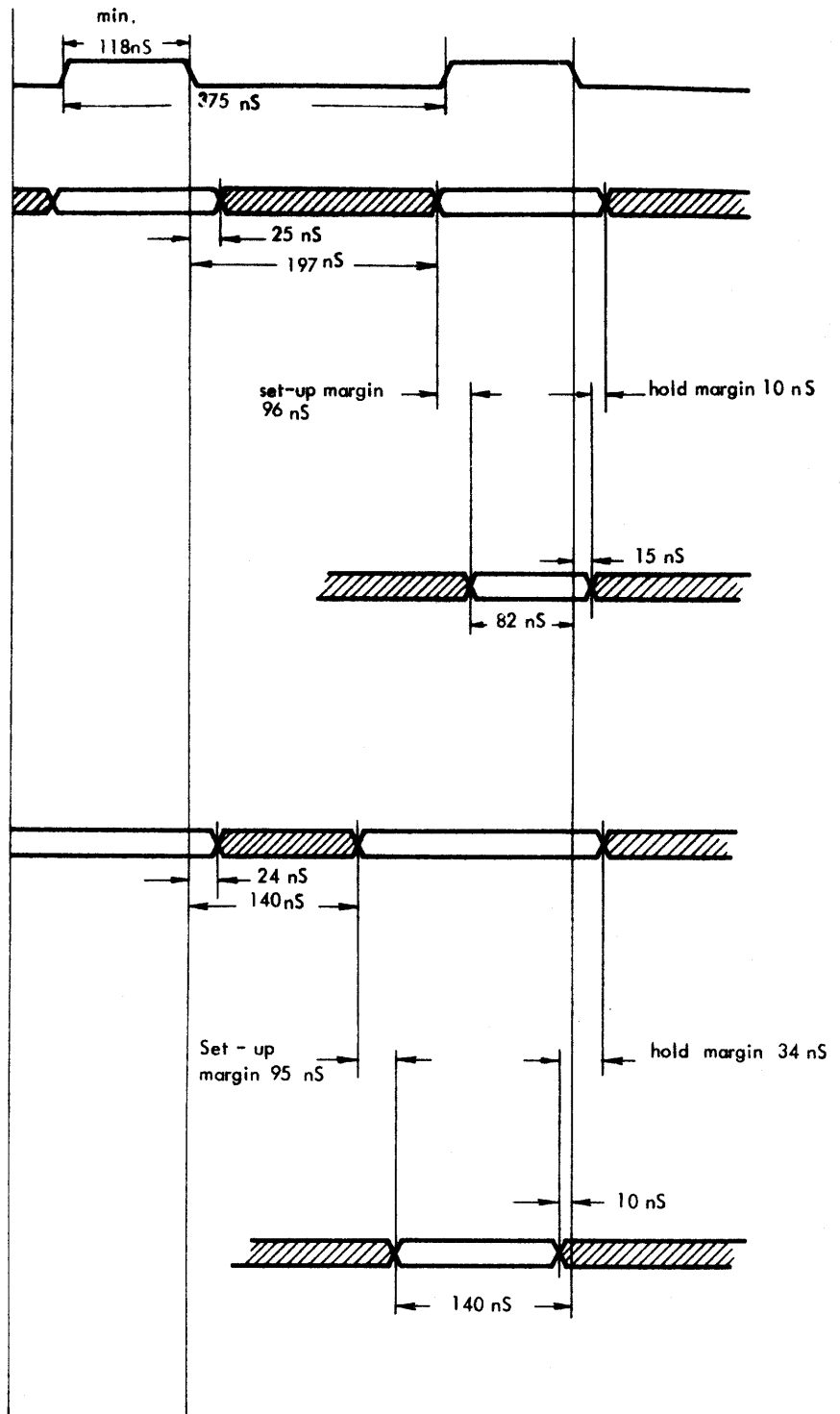
The RALU sends data to
TRANSMITTER BUFFER or
I/O DATA REGISTER or
I/O ADDRESS REGISTER, These
REGISTERS demands the INTERNAL
BUS to be defined as follows :

INTERNAL BUS
(DATA FROM BUS DATA
SELECTOR)

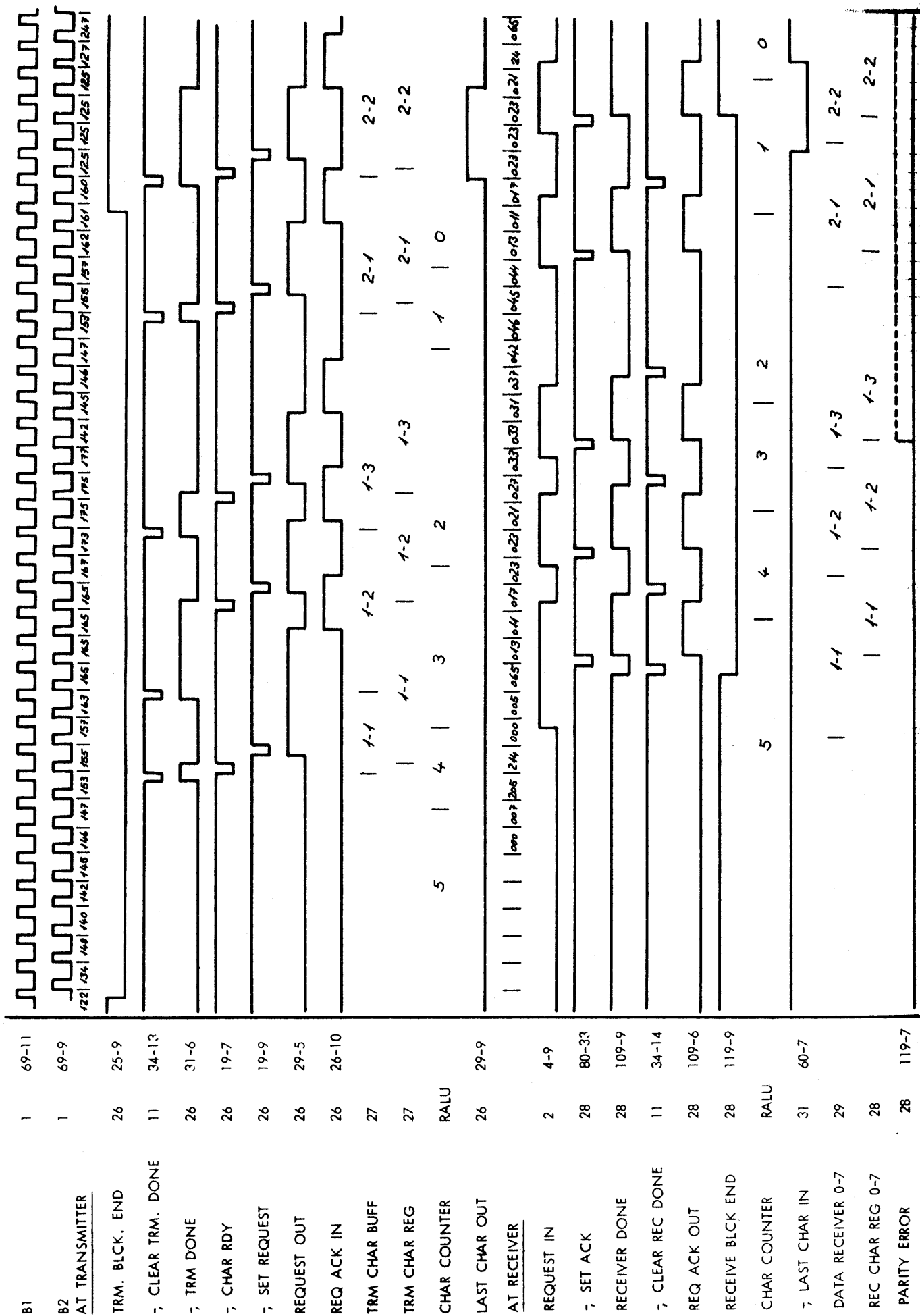
The max. value is composed
of :

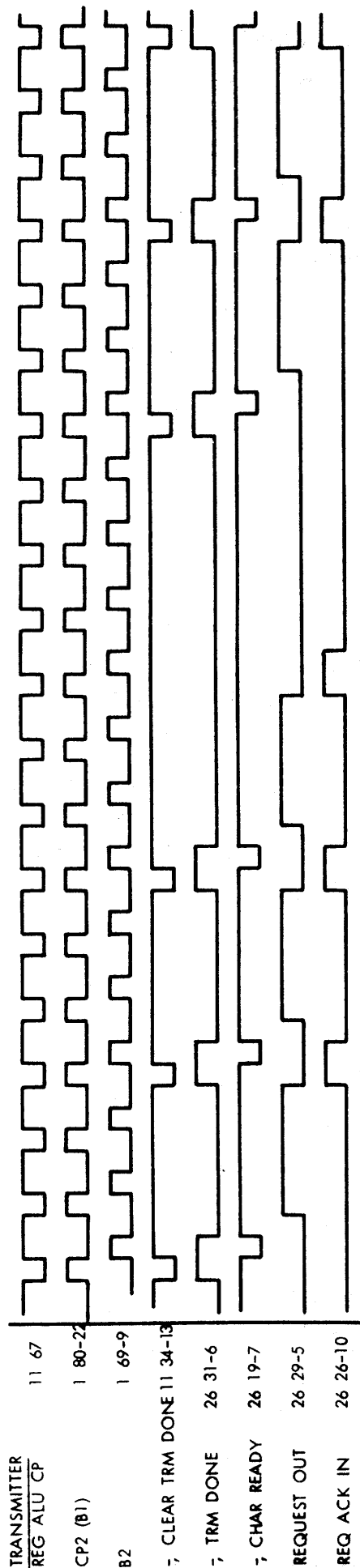
CP 2 → μ ADDR. REG	32 nS
μ ADDR. REG →	
SOURCE ADDRESS	87 nS
SOURCE ADDR → BUS	21 nS
	~ 140 nS

Data from data selector
are send to the RALU
via the bus. The RALU
demands the bus to be
defined as follows :



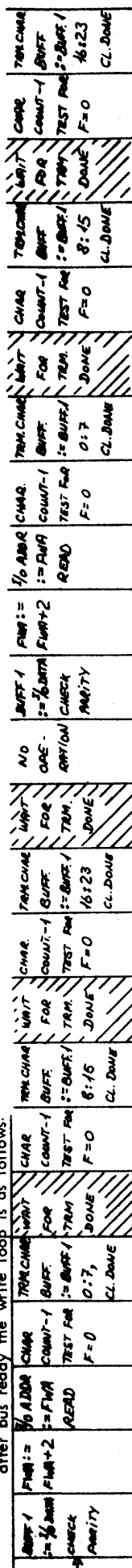
TRANSMIT/RECEIVE TIMING
(Transmit and Receive 5 characters)
Timing Chart



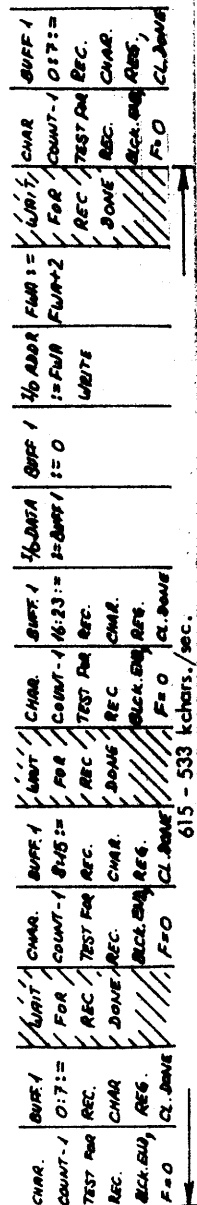


INSTRUCTION SEQUENCE:

Write of characters is initiated with I/O ADDR:=FWA, read-and after bus ready the write loop is as follows:



INSTRUCTION SEQUENCE:



SIGNAL	DESTINATION	DESCRIPTION
B1	11 26-3	Clock Pulse ~ 3,278 Mhz.
CP 1	26 19-5 26 19-11 28 80-11	Clock Pulse ~ 4,915 Mhz. This CP is used by the receiver and transmitter logic.
CP 2	2 80-5 2 15-1 3 64-23 3 66-23 4 15-13 11 67-2 11 67-5 11 67-10 11 34-6	Clock Pulse ~ 3,278 Mhz. Period 305 ns, duty cycle 33 %. This CP is used by the μ - address register. Clock Pulses to RALU is derived from this pulse.
CP 3	4 18-2	Clock Pulse ~ 3,278 Mhz Period 305 nS, duty cycle 16.6 %. This clock pulse strobes the write signal to the μ - address store.
END	2 5-5 2 5-2 11 33-13 26 22-6 28 22-11	END signals the end of a channel program. The signal is also high during the Power Reset condition.
$\neg$, POWER RESET A	4 18-4 23 1-5 25 1-13 25 23-4 25 13-16 26 25-15	
$\neg$, POWER RESET B	2 80-1 2 80-2 2 6-1	
POWER OK	18 16-5 21 5-13	This signal together with MASTER and DATA OUT strobes DATA and ADDRESS to RC 8000 BUS.
$\neg$, POWER OK	23 141-12 23 142-12 30 137-5 30 137-9	

Unit	CLOCK OSC & POWER RESET	
FPA 801		
Dwg. No.		
A24712		1

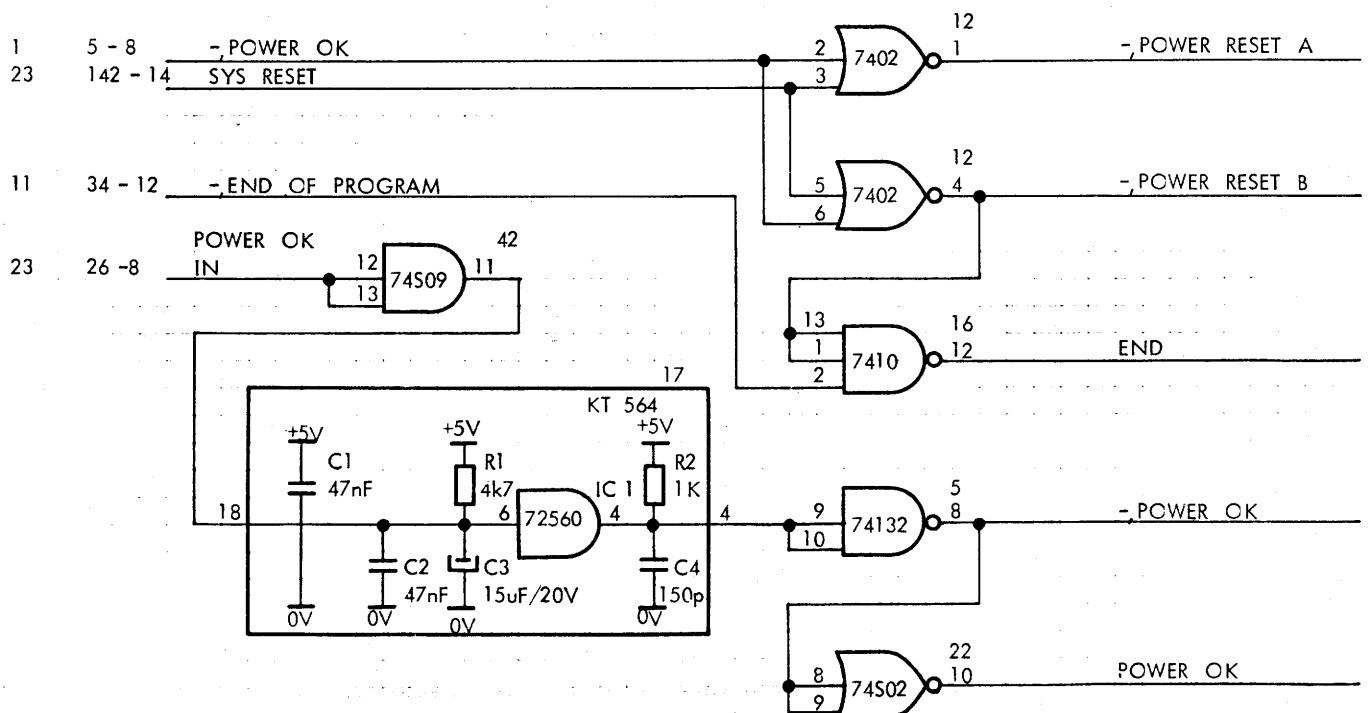
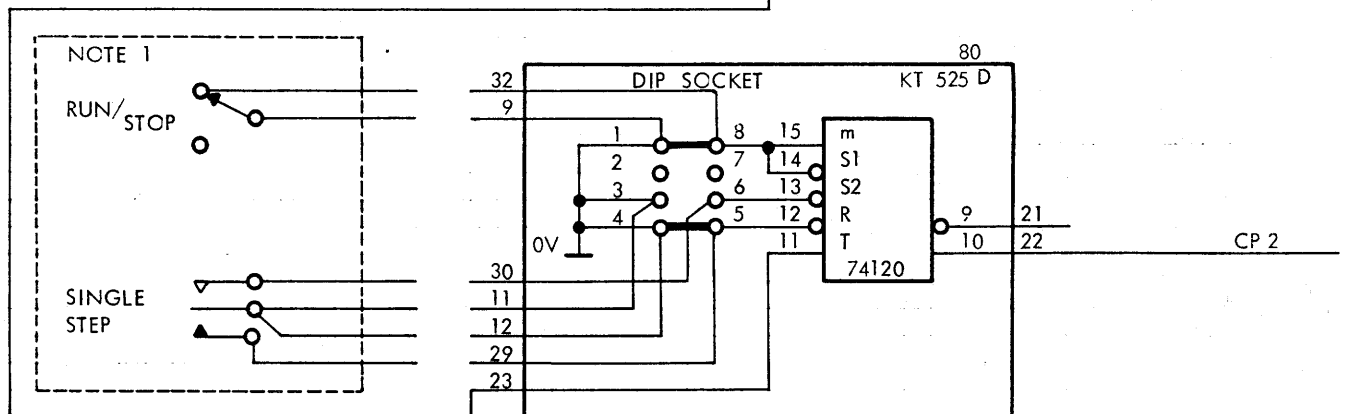
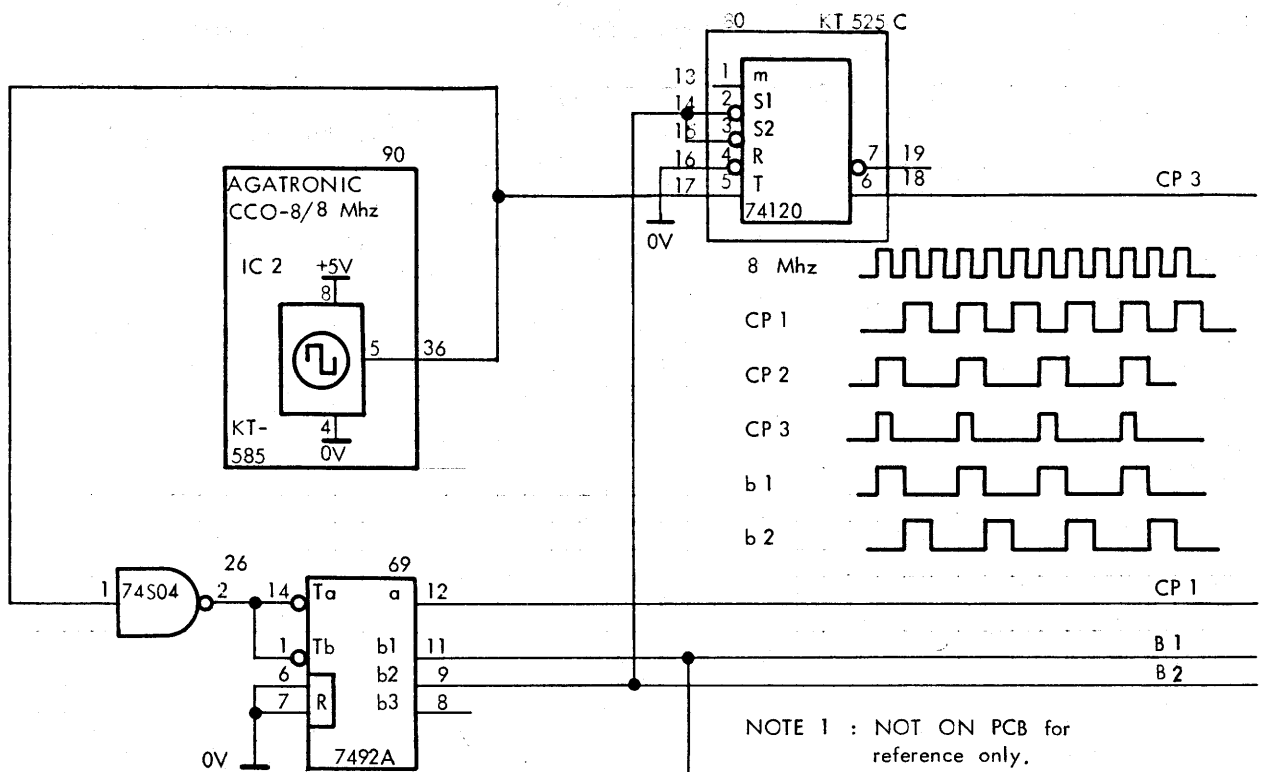
18-014, 018

770406 VH.

770330 LLM

770329 OKJ

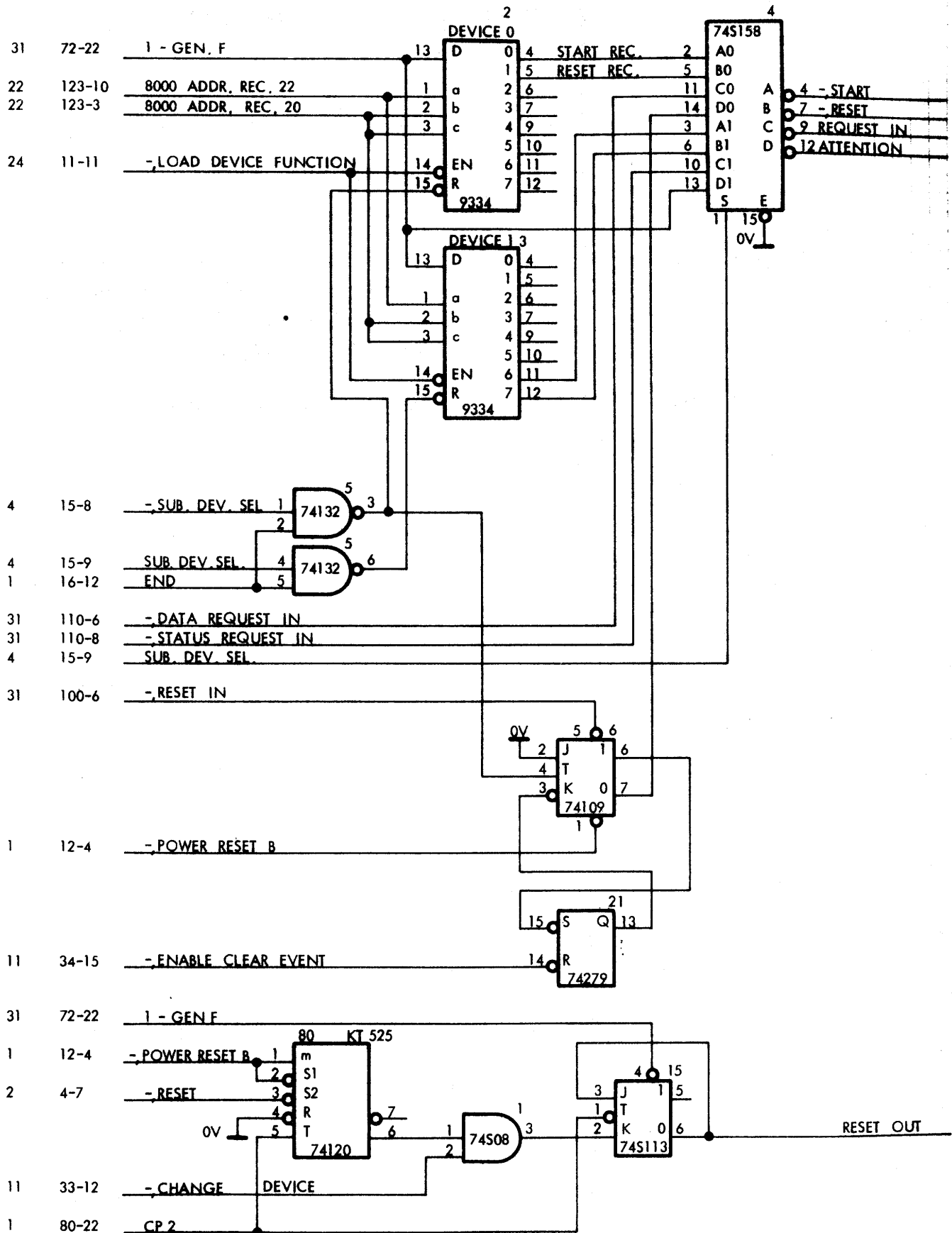
770206 VH



SIGNAL	DESTINATION	DESCRIPTION
ATTENTION	5 70-5	Reset signal received from opposite controller.
- , RESET	5 70-1	Device function "Reset unit."
RESET OUT	3 64-38 3 66-38 5 68-9 5 70-9 11 33-14 30 30-1	Reset signal to opposite controller. The signal is also used to initiate the μ - address logic
REQUEST IN	5 68-5 28 16-10 28 109-4	Data or status Request from opposite controller
- , START	5 68-2	Device function "Start Channel Program."

Unit	DEVICE FUNCTIONS START & RESET	
FPA 801		
Dwg. No.		
A24714		2

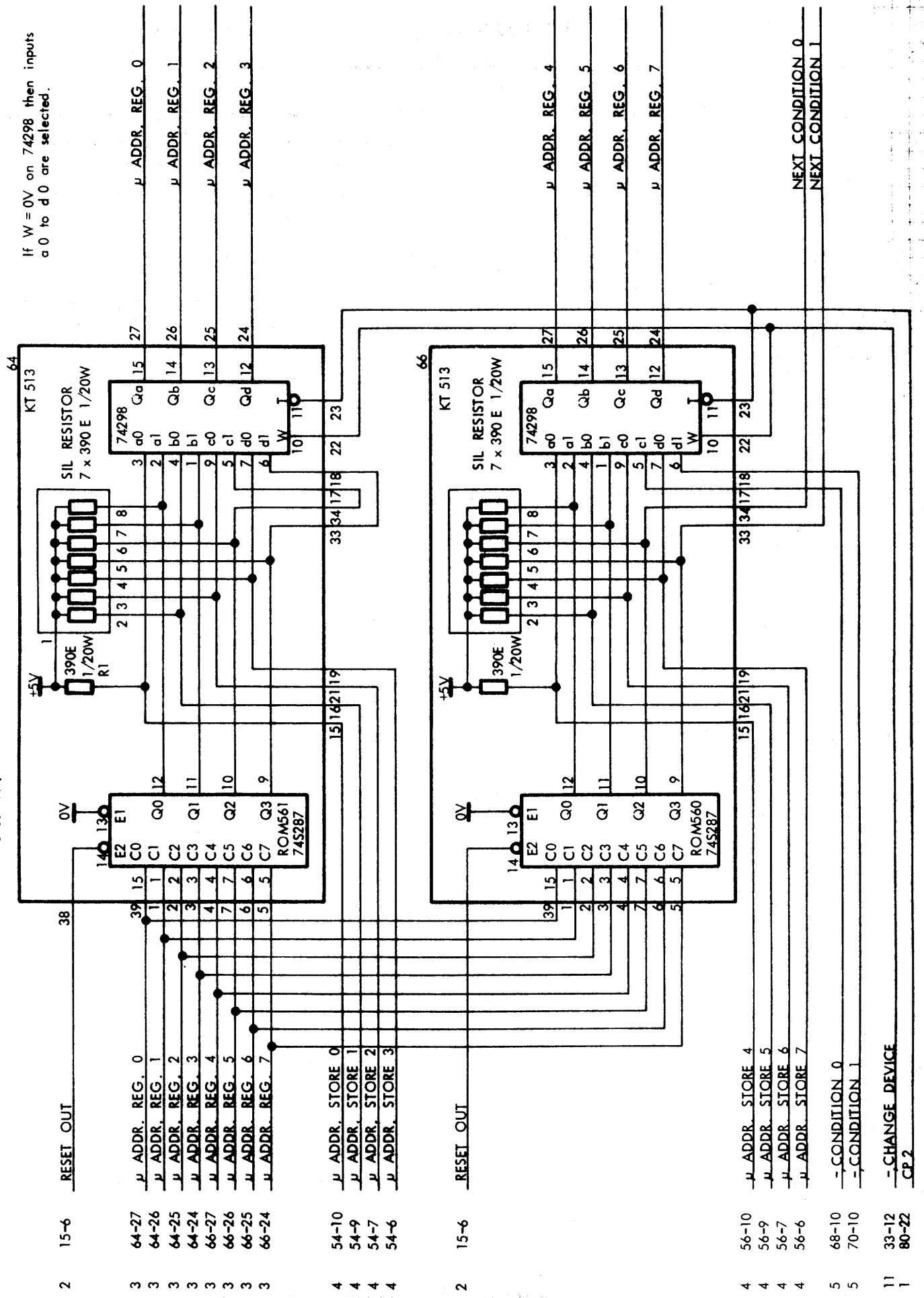
750929 VH. 770307 AMS. 770330 LLM. 770406 VH.



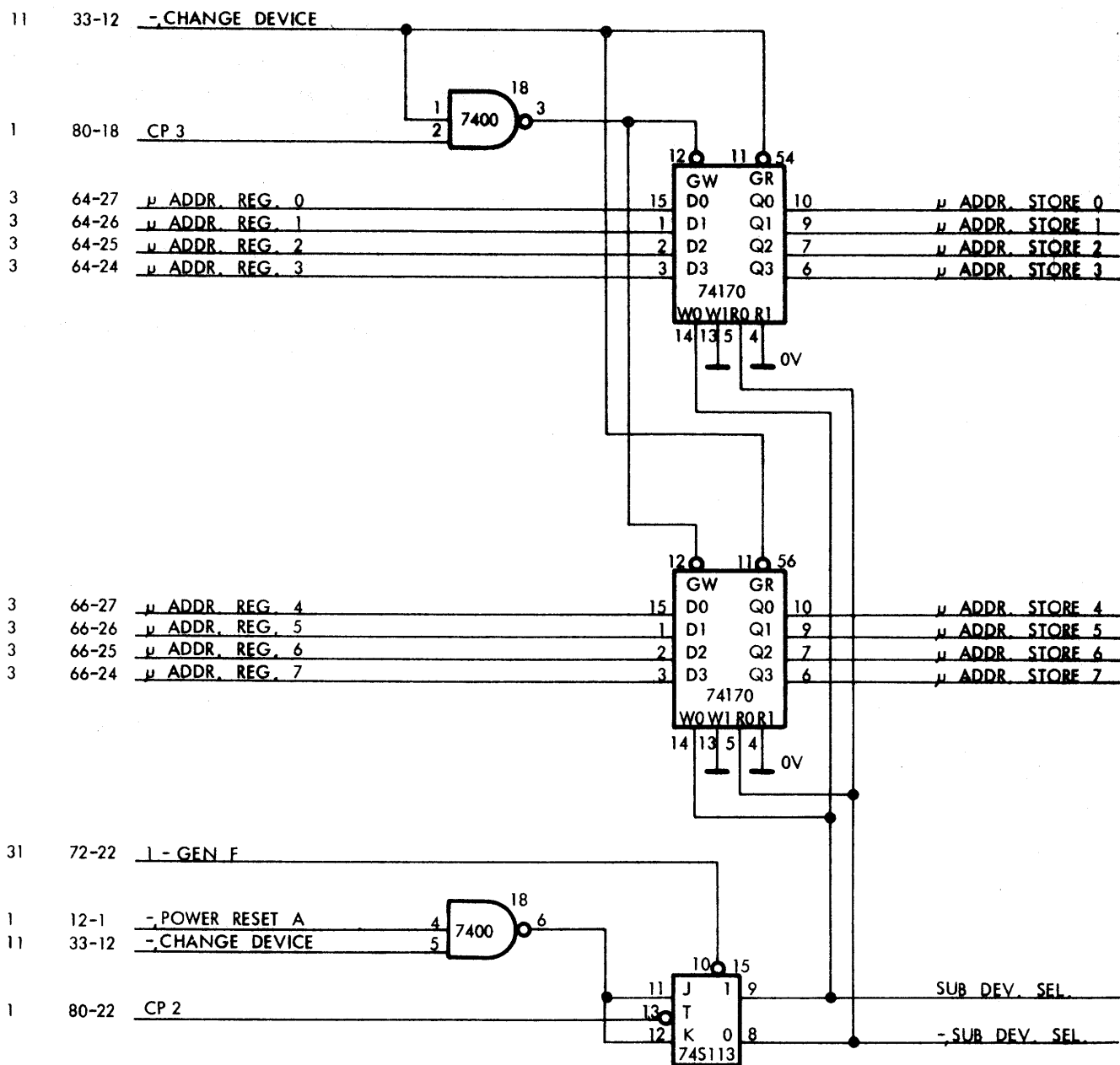
SIGNAL	DESTINATION	DESCRIPTION
μ ADDR. REG 0-7	4 5 10 11 12	μ Address Register is used as address to the micro program PROM'S.
NEXT CONDITION 0	5 70-16	Next Condition 0 and 1 is generated by the micro program and may be used as the two least significant bits of the next micro address.
NEXT CONDITION 1	5 68-16	Refer to next Condition 0

Unit	μ ADDRESS REGISTER	
FPA 801		
Dwg. No.		
A24715		3

If W = 0V on 74298 then inputs a0 to d0 are selected.



SIGNAL	DESTINATION	DESCRIPTION
μ ADDR STORE 0-7	3	The μ Address Store consists of two words, one word for the RECEIVER part of FPA 801 and one word for the TRANSMITTER. The store holds the micro address of the subdevice not currently running.
SUB. DEV. SEL	2 4-1 2 5-4 5 70-23 6 74-2 6 74-11 6 84-2 6 84-11 7 76-2 7 76-11 7 86-2 7 86-11 8 78-2 8 78-11 8 88-2 8 88-11 12 27-10 15 107-5	The Sub Device Selector FF indicates which sub device is current currently running.
- , SUB. DEV. SEL	2 5-1 2 5-10 26 90-28 30 40-11 30 137-1	
Unit	μ ADDRESS STORE	
FPA 801		
Dwg. No.		4
A24716		



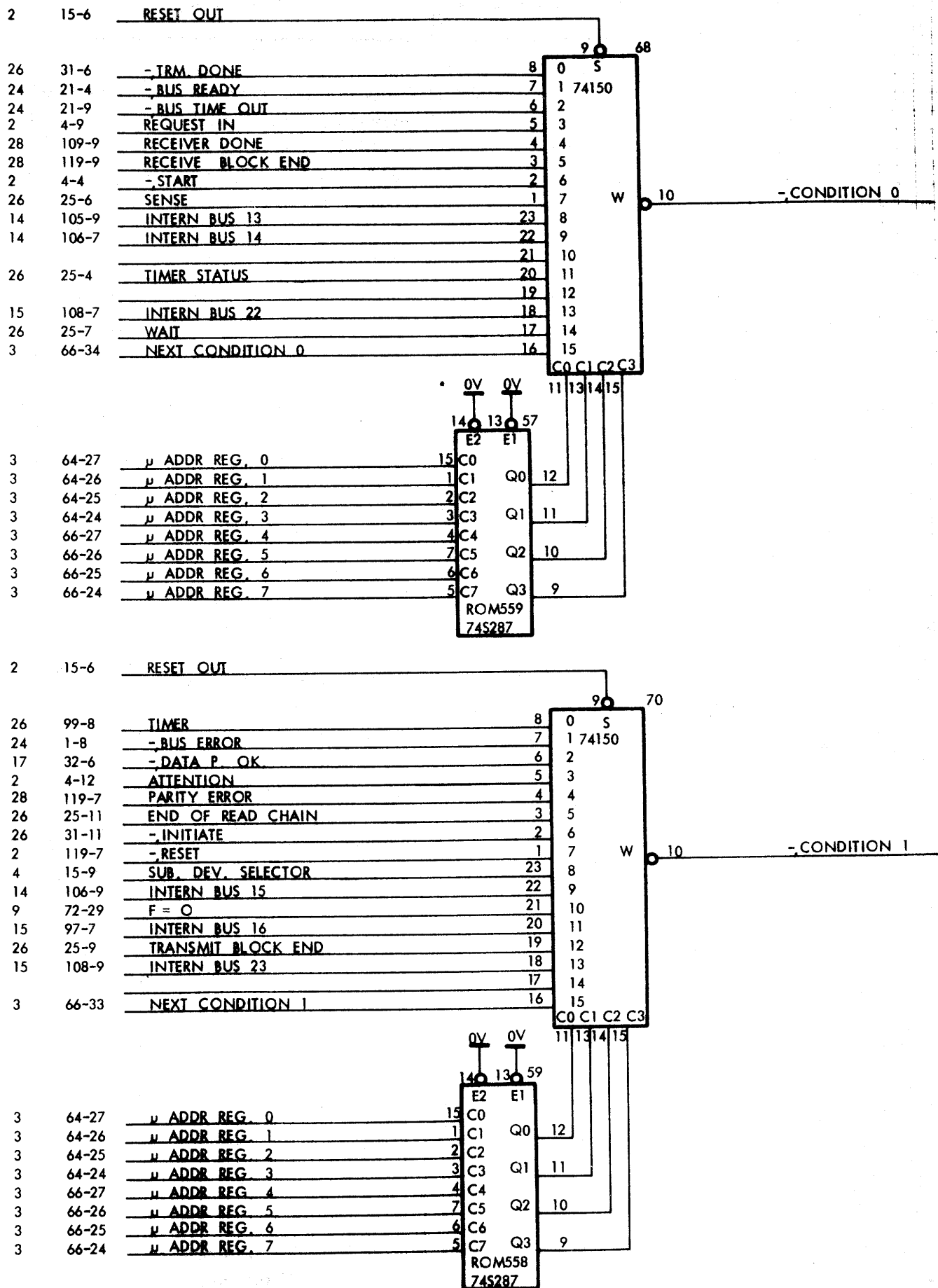
ADDRESS 1 0

WORD 0	0	0	RECEIVER μ ADDR. STORE
WORD 1	0	1	TRANSMITTER μ ADDR. STORE
WORD 2	1	0	NOT USED
WORD 3	1	1	NOT USED

SUB. DEV. SEL = "1" TRANSMITTER
SUB. DEV. SEL = "0" RECEIVER

SIGNAL	DESTINATION	DESCRIPTION
- ,CONDITION 0	3 66-17	The two outputs from the condition selector is always used as the two least significant bits of the micro address. Condition 1 is the least significant bit. By means of this selector two conditions can be selected at a time, thus making it possible to, jump to 4 different micro addresses. The 2 x 15 conditions is selected by the micro program via the PROM'S IC 57 and IC 59.
- ,CONDITION 1	3 66-18	
Unit		
FPA 801		
Dwg. No.		
A24717		
CONDITION SELECTOR		
		5

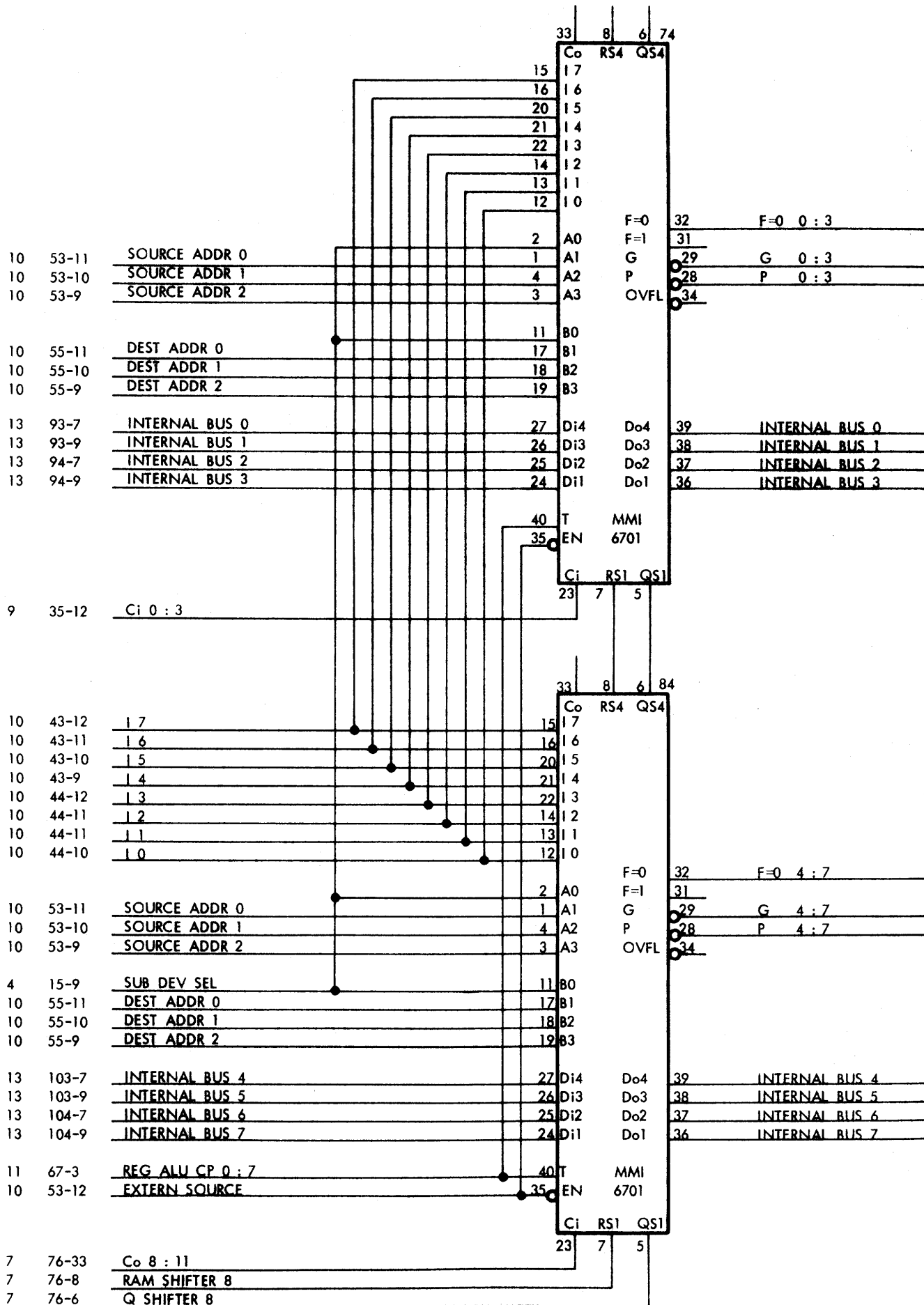
750929 VH. 770307 AMS, 770401 LLM, 770406 VH.



SIGNAL	DESTINATION	DESCRIPTION
F = 0 0 : 3	9 72-29	Diagrams 6,7 and 8 shows the Register - Arithmetic - logic - unit (RALU) used in FPA 801. The RALU performs via a micro-program all of the functions associated with the communication. The data outputs and inputs of the RALU are connected to the FPA 801 internal bus. The RALU contains 16 directly addressable, two port, general purpose registers, and one separate Q - register. The Q register is not utilized in FPA 801. 8 of the general purpose registers are assigned to the receiver part of FPA 801 and 8 are assigned to the transmitter part. The registers, which has the same meaning in both sub devices, holds the following information: 0: Description Address 1: Channel Program Address 2: First Word Address 3: Character Counter 4: Data Buffer 5: Remaining Char. Count 6: Event Status 7: Command Register The registers are addressed via the micro - program by means of the Source and Destination addresses 0 - 2. Continued on Diagram 7
F = 0 4 : 7	9 72-29	
G 0 : 3	9 35-1	
G 4 : 7	9 35-3	
INTERN BUS 0 - 7	13	
P 0 : 3	9 35-2	
P 4 : 7	9 35-4	

Unit	μ CONTROLLER 0 : 7	
FPA 801		
Dwg. No.		
A24718		6

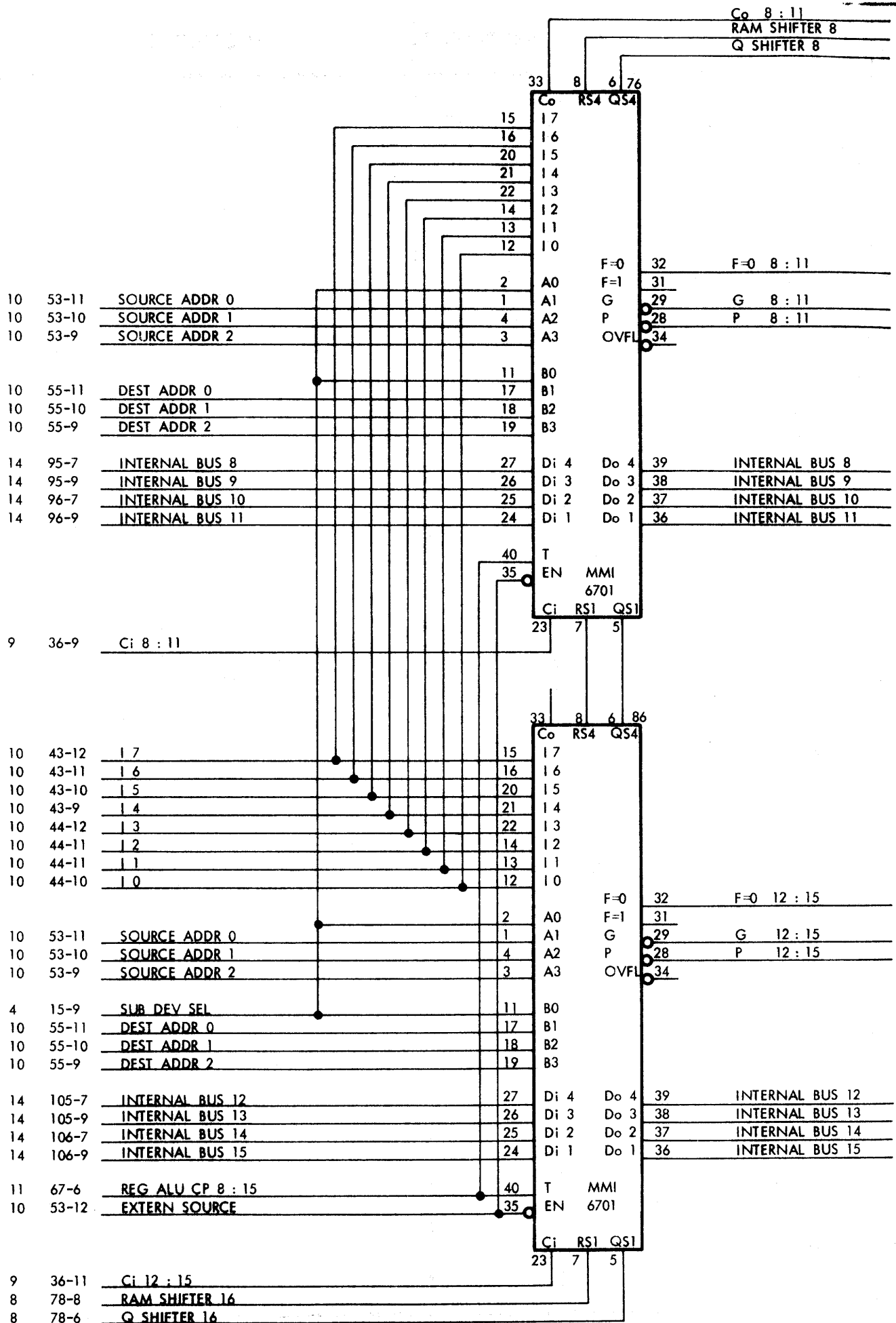
750924 VH 770310 OKJ 770401 LLM. 770406 VH.



SIGNAL	DESTINATION	DESCRIPTION
Co 8 : 11	6 84-23	Continued from Diagram 6 The RALU function to be exuted is under control of the instruction bits 0 - 7, which are generated by the microprogram. The FPA 801 RALU is connected to utilize the carry look-ahead technigue, which makes a cycle time of 215 nS possible, however, additional time is requiered for the micro Address Register and the RALU address/function PROM'S to settle so the total cycle time becomes 305 nS. G and P outputs are the conuentional carry generate and carry propagate signals assosiated with the look ahead technique. The F=0 outputs indicates that the output of the alu is all zeroes. These outputs are all wired together and used as a condition in the microprogram.
F = 0 8 : 11	9 35-13	
F = 0 12 : 15	9 72-29	
G 8 : 11	9 36-5	
INTERN BUS 8 : 15	13	
P 8 : 11	9 36-6	
P 12 : 15	9 36-15	
Q SHIFTER 8	6 84-5	
RAM SHIFTER 8	6 84-7	

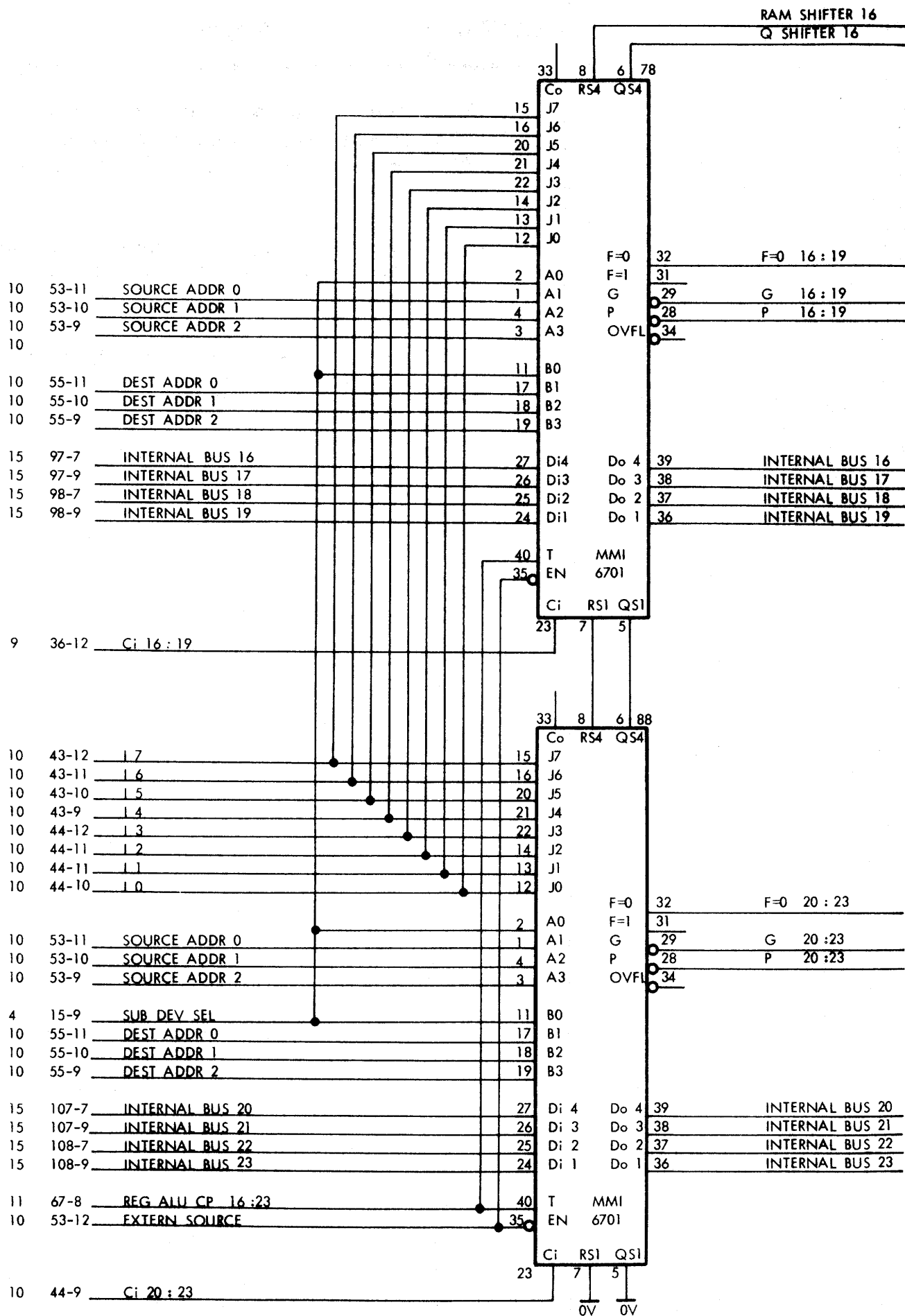
Unit	FPA 801 μ CONTROLLER 8 : 15	
Dwg. No.		
A24719		
		7

750924 VH 770310 OKJ 770401 LLM. 770406 VH.



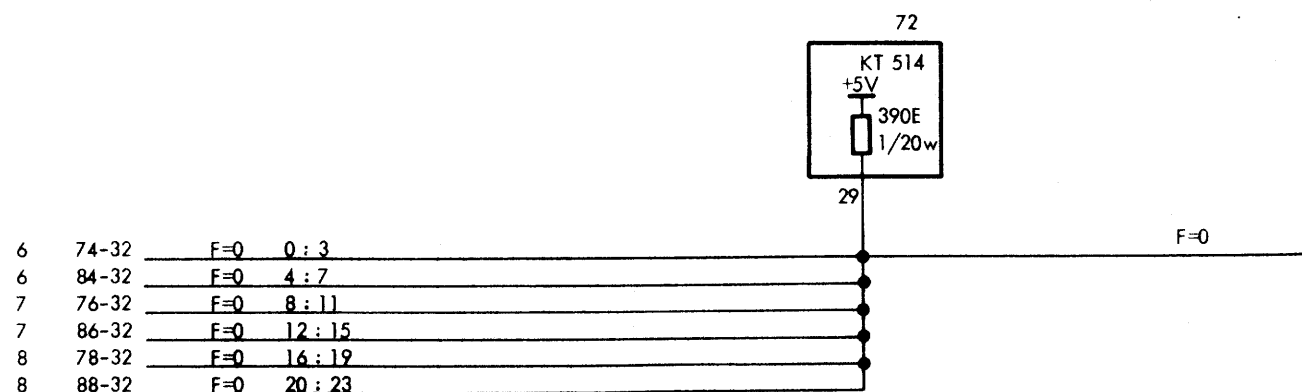
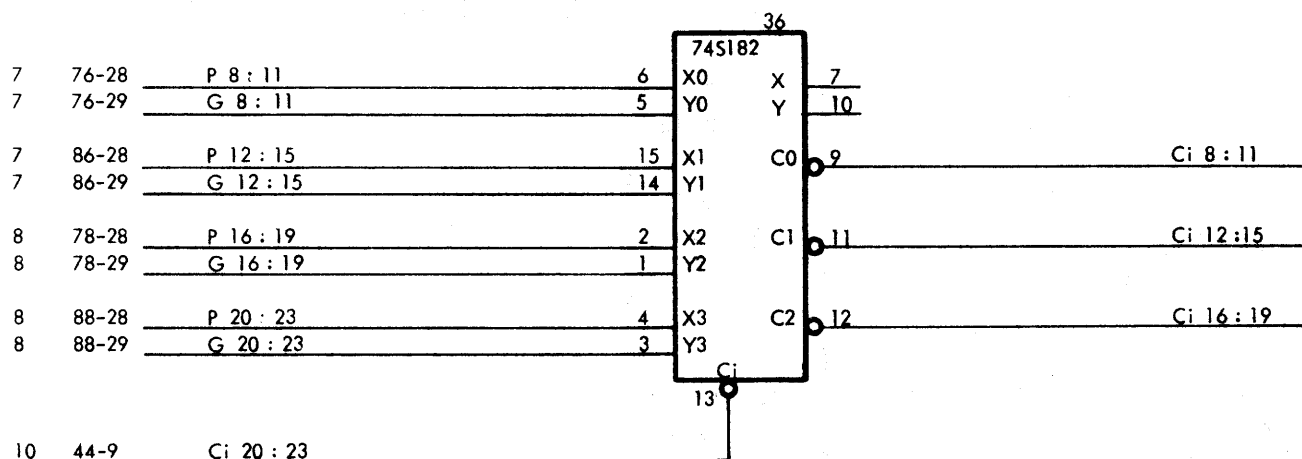
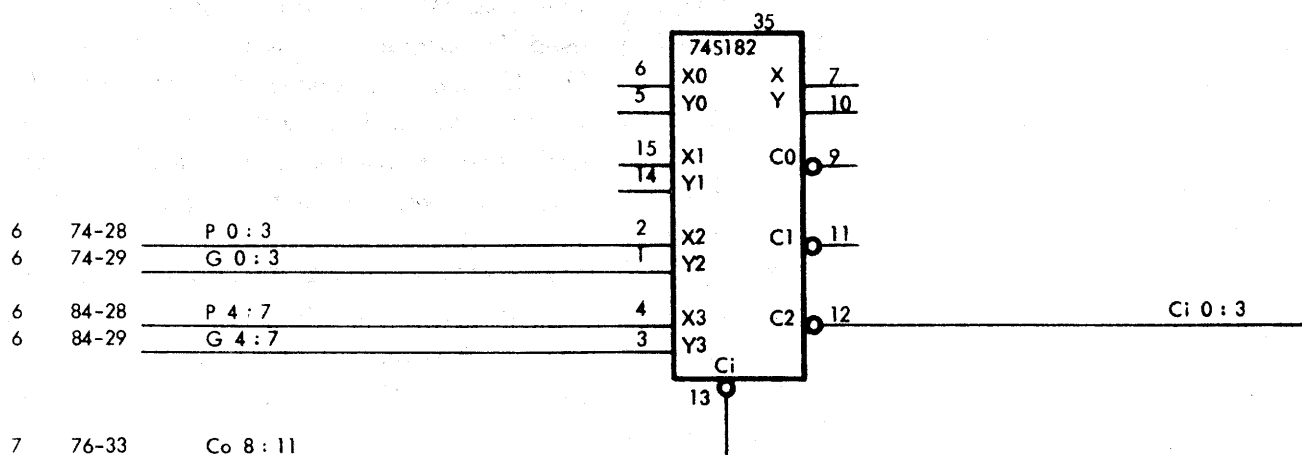
SIGNAL	DESTINATION	DESCRIPTION
F = 0 16:19	9 72-29	
F = 0 20:23	9 72-29	
G 16:19	9 36-1	
G 20:23	9 36-3	
INTERN BUS 16:23	13	
P 16:19	9 36-2	
P 20:23	9 36-4	
Q SHIFTER 16	7 86-7	
RAM SHIFTER 16	7 85-5	
Unit FPA 801 Dwg. No. A24720 μ CONTROLLER 16:23 8		

750923 VH 770309 OKJ 770406 VH.



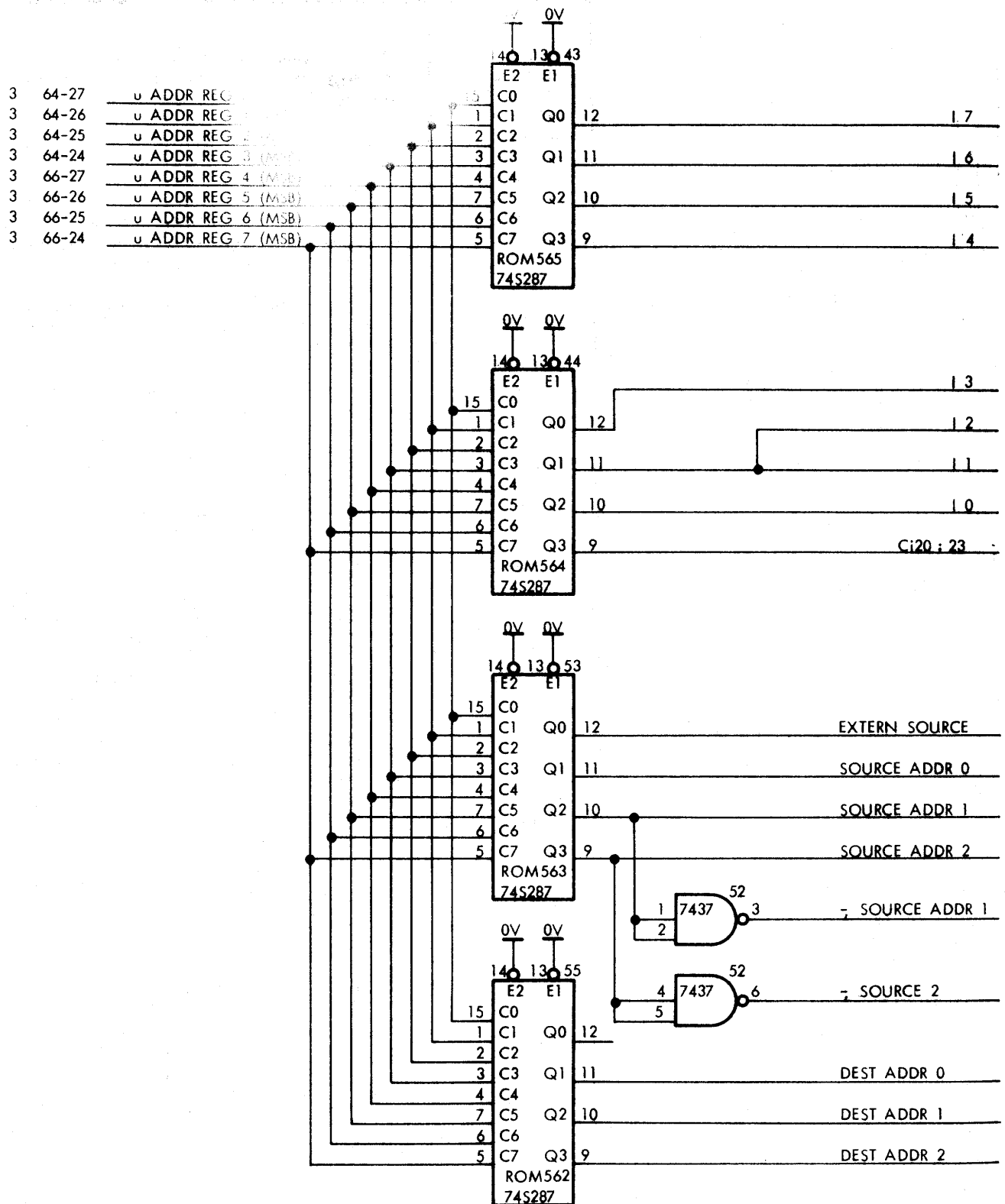
SIGNAL	DESTINATION	DESCRIPTION
Ci 0 : 3 Ci 8 : 11 Ci 12:15 Ci 16:19 F = 0	6 74-23 7 76-23 7 86-23 8 78-23 5 70-21	This diagram shows the carry look ahead circuits. The generated Ci outputs are lead to the carry inputs of the respective RALU sections. The F = 0 output is a wired - or result of the F = 0 outputs from the different RALU sections. The output is terminated with a 390 E resistor since the F = 0 outputs from RALU sections are open - collectors.
Unit FPA 801 Dwg. No. A24721	CARRY LOOK AHEAD & F = 0.	
		9

750925 VH 770310 OKJ 770401 LLM 770406 VH.



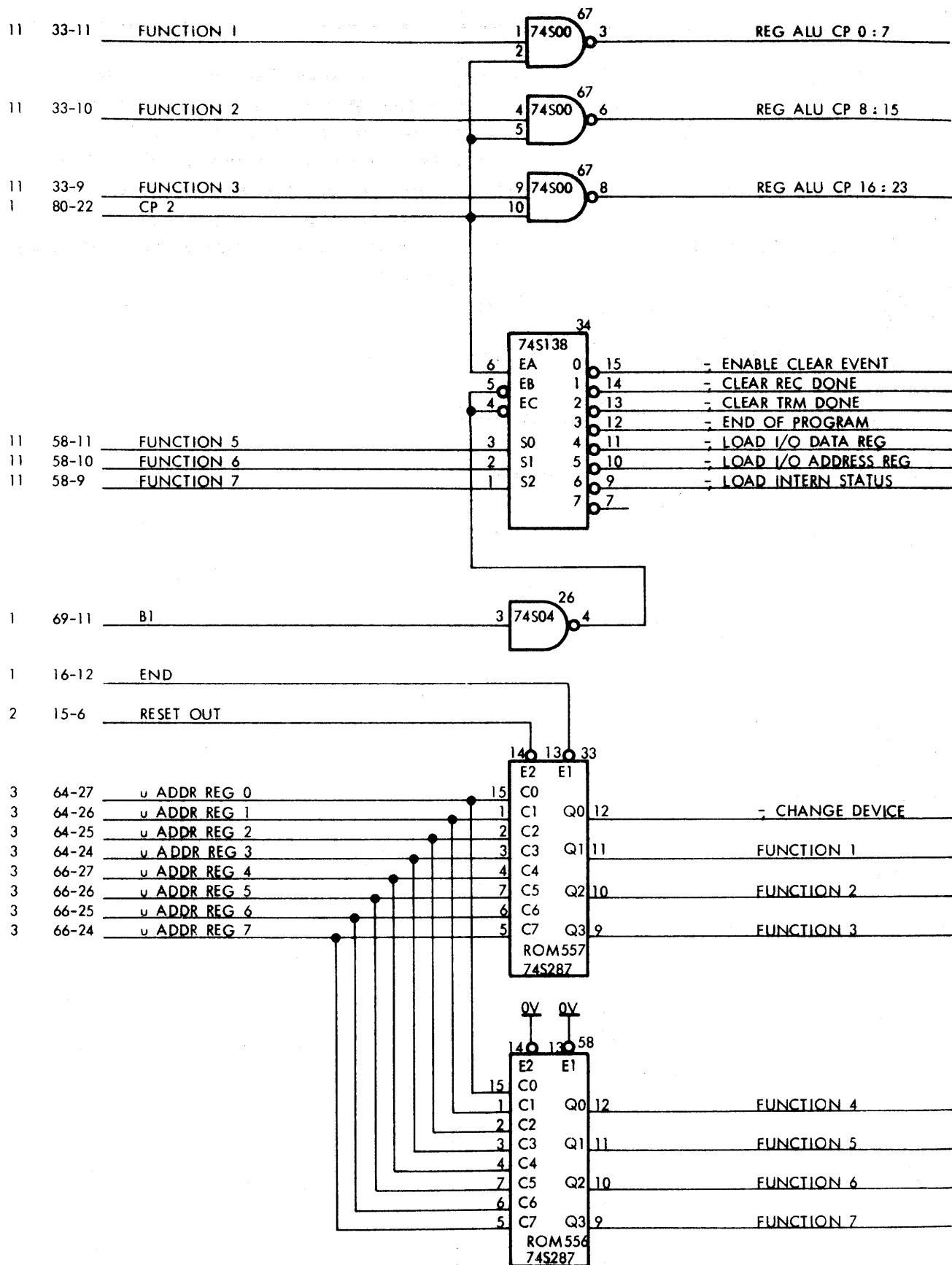
SIGNAL	DESTINATION	DESCRIPTION
Ci 20 : 23 DEST ADDR 0-2 EXTERN SOURCE I0 - I7 SOURCE ADDR 0 - 2 -,SOURCE ADDR 1 -,SOURCE ADDR 2	8 88-23 9 36-13 6,7,8, 26,27 6 74-35 6 84-35 7 76-35 7 86-35 8 78-35 8 88-35 13 52-9 13 52-10 14 52-12 14 52-13 6,7,8 6,7,8,12 13 93-2 13 94-2 13 103-2 13 104-2 13 93-14 13 94-14 13 103-14 13 104-14 14 95-14 14 96-14 14 105-14 14 106-14 15 97-14 15 98-14 15 107-14 15 108-14	The PROM'S on this diagram is primary used in connection with the RALU. I3 - I7 are the instruction bits and I0 - I2 are instruction modifiers. The Source and Dest Addresses 0 - 2 are used by the RALU as well as some registers outside the RALU. The EXTERN SOURCE signal when logical 1 will gate data from the Data selector to the FPA 801 internal bus, while a logical 0 will gate data from the RALU to the internal bus. Ci 20 : 23 signal is the carry input to the least significant bit of the RALU.
Unit	PROM'S for μ CONTROLLER	
Dwg. No.	A24722	
		10

750916 VH 770309 OKJ 770401 LLM 770406 VH.



SIGNAL	DESTINATION	DESCRIPTION
-CHANGE DEWICE	2 1-2 3 64-22 3 66-22 4 18-1 4 18-5 4 54-11 4 56-11	This signal when low causes the Sub Device Selector to change state i.e. the other sub device becomes selected.
-,CLEAR REC. DONE	28 109-13 28 119-11	This signal starts the receiver and causes a Request Ack signal to be send to the opposite controller provided a Request in signal is present.
-,CLEAR TRM. DONE	26 6-11 26 26-13	This signal starts the transmitter, loads the transmitter buffer and causes a Request signal to be send to the opposite controller.
-,ENABLE CLEAR EVENT	2 21-14	This signal enables clear of the Reset in FF, which holds the reset received information from the opposite controller.
-,END OF PROGRAM	1 16-2	Indicates the end of a channel program.
FUNCTION 1,2,3	This diag.	These bits controls the clock pulses to the RALU, and makes it possible to transfer 8-bits characters to the RALU.
FUNCTION 4	23 41-12 26 25-13	This parameter is used to control the Data Out Out FF, and in conjunction with the Load Intern Status signal to set/clear the internal status FF 'S.
FUNCTION 5,6,7	This diag.	These signals are via a 3 to 8 decoder converted to 7 do-functions.
-,LOAD I/O ADDRESS REGISTER.	21 134-11 21 135-11 21 136-11 23 22-2 23 22-3 23 41-3 24 21-2 24 21-3 24 21-6 24 21-11 24 21-12	This signal loads the I/O Address Register from the internal FPA 801 bus, and simultaneously a RC 8000 bus transfer is requested.
-,LOAD I/O DATA REG.	18 67-12 23 41-13	This signal loads the I/O Data Register from the internal FPA 801 bus.
-,LOAD INTERN STATUS	This diag.	Refer to the function 4 signal.
REG ALU CP 0:7	6 74-40 6 84-40	Clock pulse to the RALU.
REG ALU CP 8:15	7 76-40 7 86-40	Clock pulse to the RALU.
REG ALU CP 16-23	8 78-40 8 88-40	Clock pulse to the RALU.
Unit FPA 801	DO- FUNCTIONS	
Dwg. No. A12957	11	

750930 VH 770310 OKJ 770401 LLM 770406 VH.



SIGNAL	DESTINATION	DESCRIPTION
CONSTANT PROM BIT 0	This diag.	Outputs from the constants circuits are wired to the data selector from which the constants can be send to the internal bus, when the constant PROM'S are selected as source. The constants are used when counters or registers has to incremented or decremented, and when status bits are set.
CONSTANT PROM BIT 1	This diag.	
CONSTANT PROM BIT 2	13 94-4	
CONSTANT PROM BIT 4	13 103-4	
CONSTANT PROM BIT 20	15 107-4	
CONSTANT PROM BIT 21	This diag.	
CONSTANT PROM BIT 22	15 108-4	
CONSTANT PROM BIT 23	This diag.	
CONSTANT BIT 0	13 93-4	
CONSTANT BIT 1	13 93-12	
CONSTANT BIT 21	15 107-12	
CONSTANT BIT 23	15 108-12	

Unit

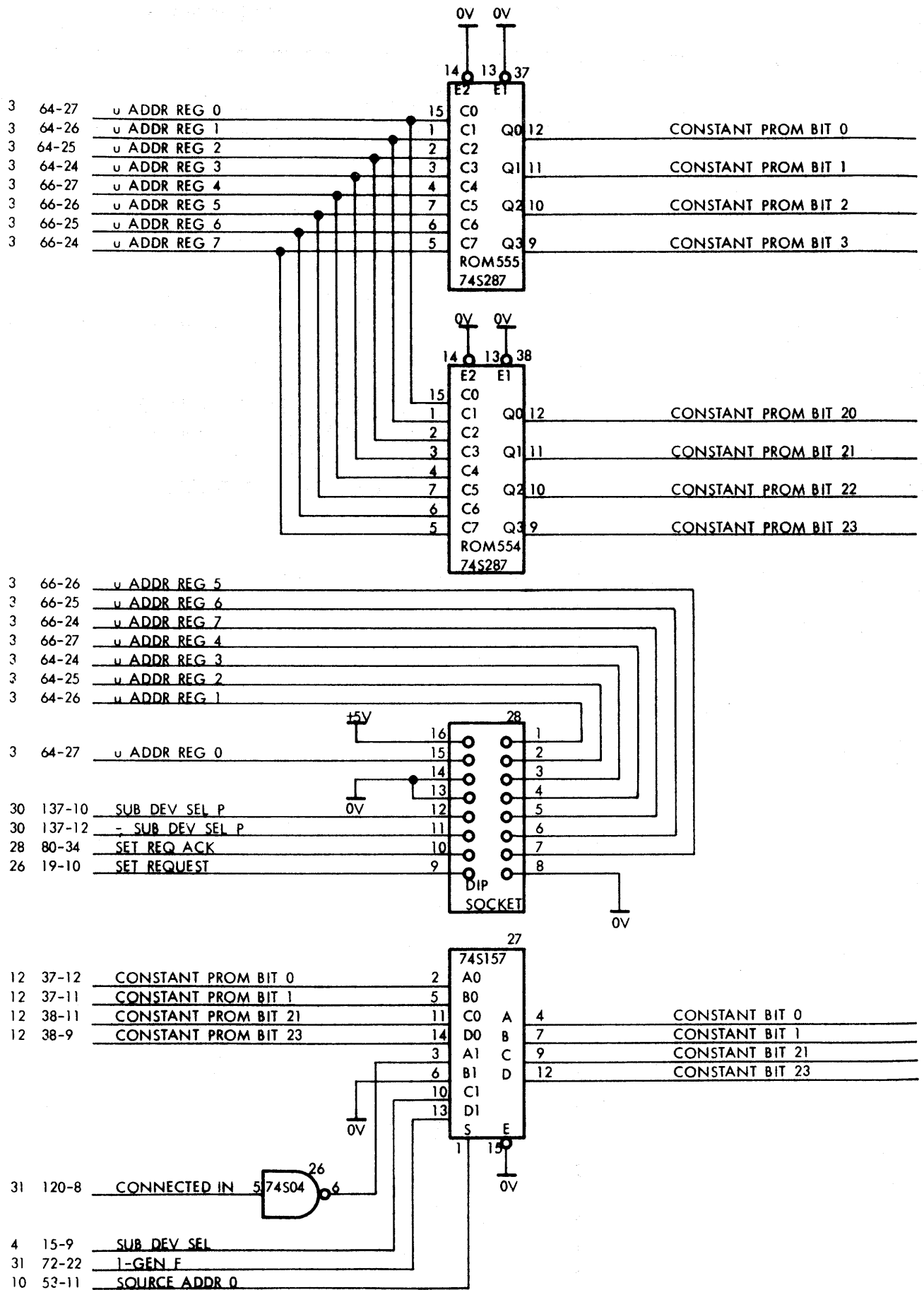
FPA 801

Dwg. No.

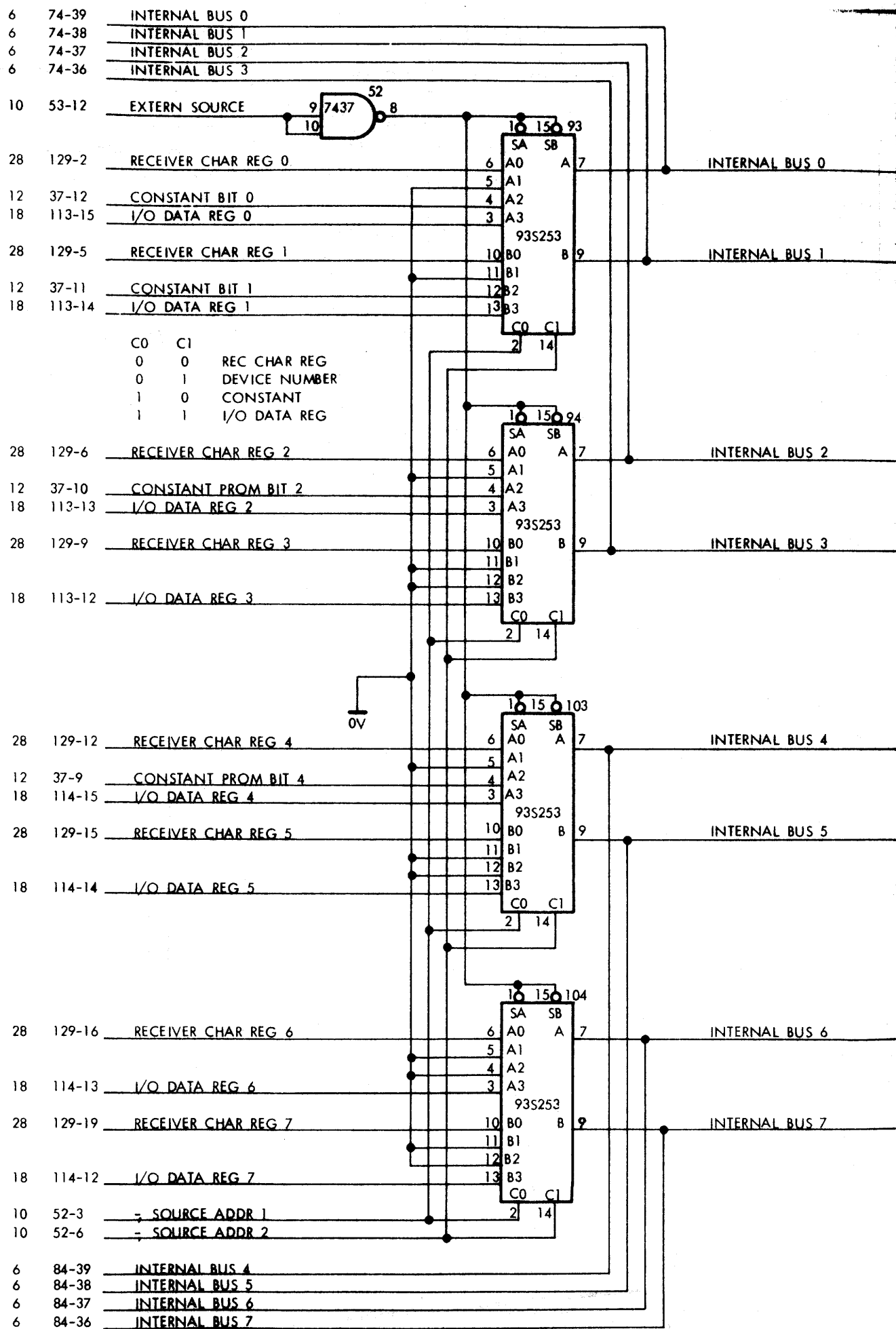
A24725

PROM'S for CONSTANTS

12

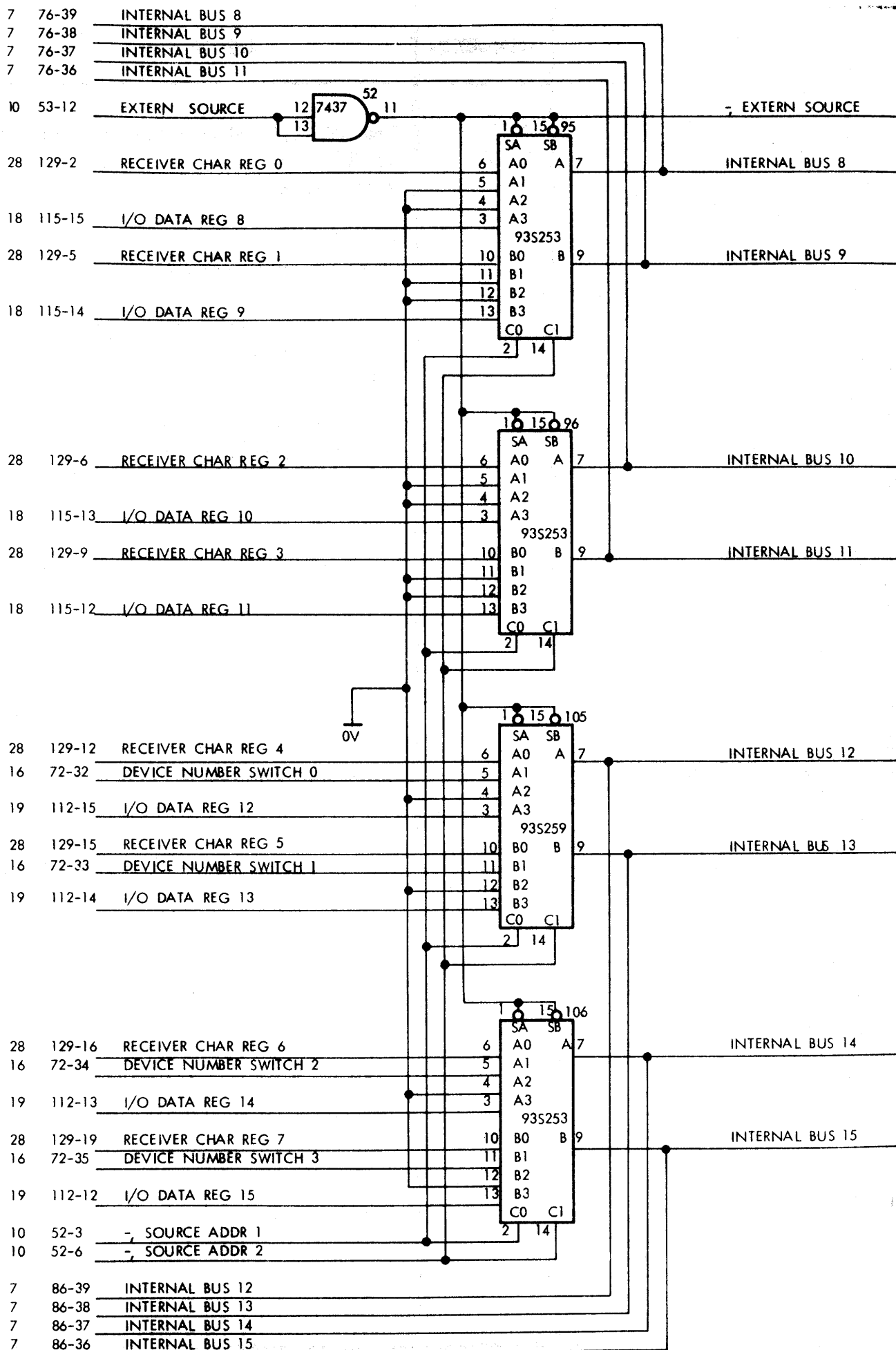


SIGNAL	DESTINATION	DESCRIPTION
INTERNAL BUS 0-23	6,17,18 21,27	The FPA 801 internal bus is a tri-state bus 24 - bits wide. The internal bus has two main sources: 1. The RALU 2. The data selector. By means of the data selector 4 different data sources can be gated to the internal bus: 1. RECEIVER CHARACTER REG 2. DEVICE NUMBER SWITCH 3. CONSTANTS 4. I/O DATA REGISTER
Unit FPA 801	DATA SELECTOR 0 : 7 TO INTERNAL BUS	
Dwg. No. A24726	DATA SELECTOR 8 : 15 TO INTERNAL BUS	
	DATA SELECTOR 16 : 23 TO INTERNAL BUS	
		13,14 & 15



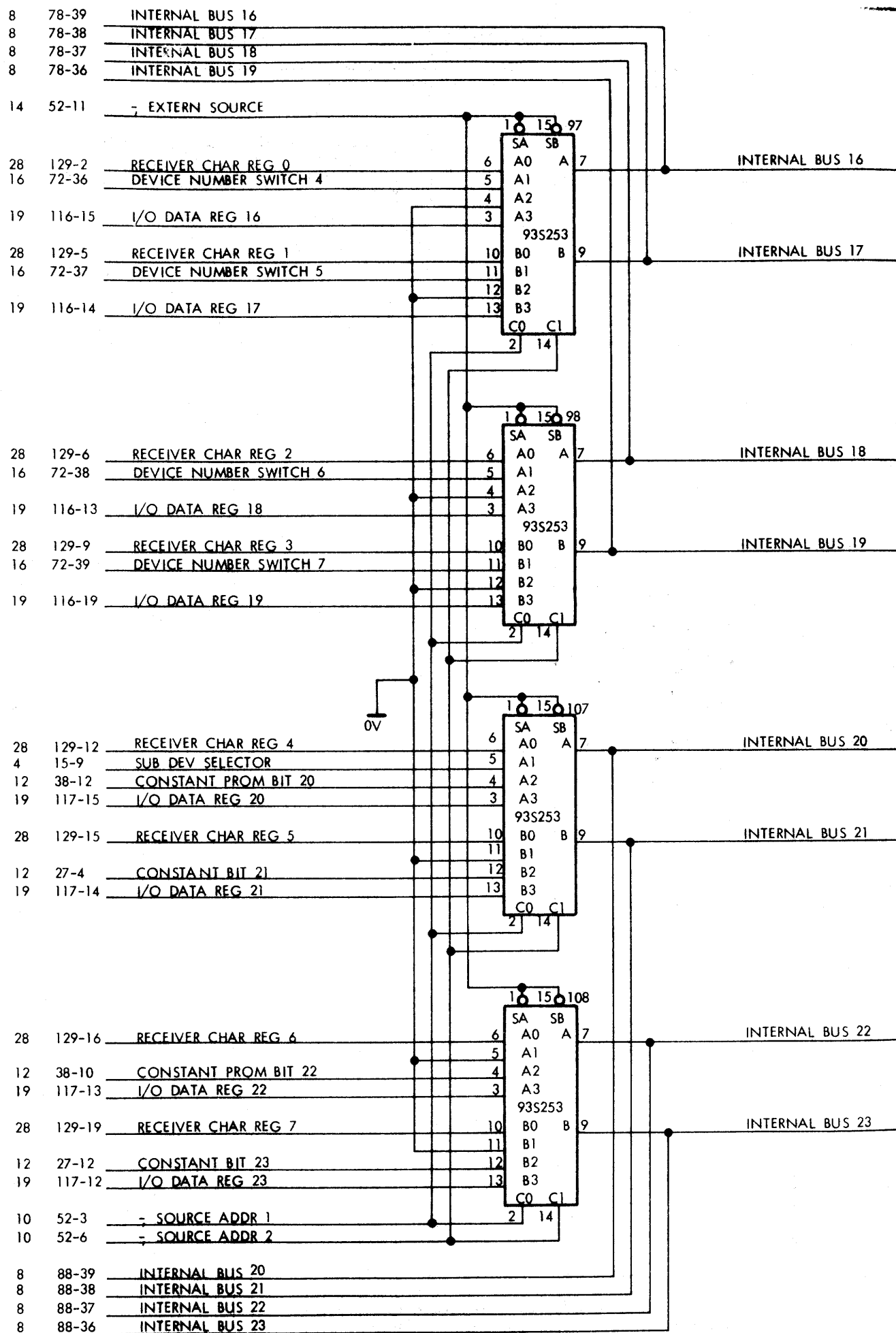
SIGNAL	DESTINATION	DESCRIPTION
INTERNAL BUS 0-23	6,17,18 21,27	The FPA 801 internal bus is a tri-state bus 24 - bits wide. The internal bus has two main sources: 1. The RALU 2. The data selector. By means of the data selector 4 different data sources can be gated to the internal bus: 1. RECEIVER CHARACTER REG 2. DEVICE NUMBER SWITCH 3. CONSTANTS 4. I/O DATA REGISTER
Unit FPA 801	DATA SELECTOR 0 : 7 TO INTERNAL BUS	
Dwg. No. A24726	DATA SELECTOR 8 : 15 TO INTERNAL BUS	
	DATA SELECTOR 16 : 23 TO INTERNAL BUS	
		13,14 & 15

750924 VH. 770311 OKJ 770401 LLM 770406 VH.



SIGNAL	DESTINATION	DESCRIPTION
INTERNAL BUS 0-23	6,17,18 21,27	The FPA 801 internal bus is a tri-state bus 24 - bits wide. The internal bus has two main sources: 1. The RALU 2. The data selector. By means of the data selector 4 different data sources can be gated to the internal bus: 1. RECEIVER CHARACTER REG 2. DEVICE NUMBER SWITCH 3. CONSTANTS 4. I/O DATA REGISTER
Unit FPA 801 Dwg. No. A24726	DATA SELECTOR 0 : 7 TO INTERNAL BUS DATA SELECTOR 8 : 15 TO INTERNAL BUS DATA SELECTOR 16 : 23 TO INTERNAL BUS	 13,14 & 15

750924 VH
770311 OKJ
770401 LLM
770406 VH.



SIGNAL	DESTINATION	DESCRIPTION
DEVICE NUMBER SWITCH 0 - 7 (bit 7 = LSB) -,SELECTED	15 24 12-12	By means of the device number switch it is possible to change the device number of FPA 801. The device number switch is continuously compared with the RC 8000 address bus bits 12 - 19 (bit 20 equal sub-device number). The selected signal is generated when all of the following conditions are fulfilled: 1. Device number coincidence 2. Address bus bits 1-11 = "0" 3. Address bus bits 0 = "1" 4. Parity of address bus = odd When the selected signal becomes logical 1 in a data out instruction to FPA 801, the device function registers are loaded (diagram 2).

Unit

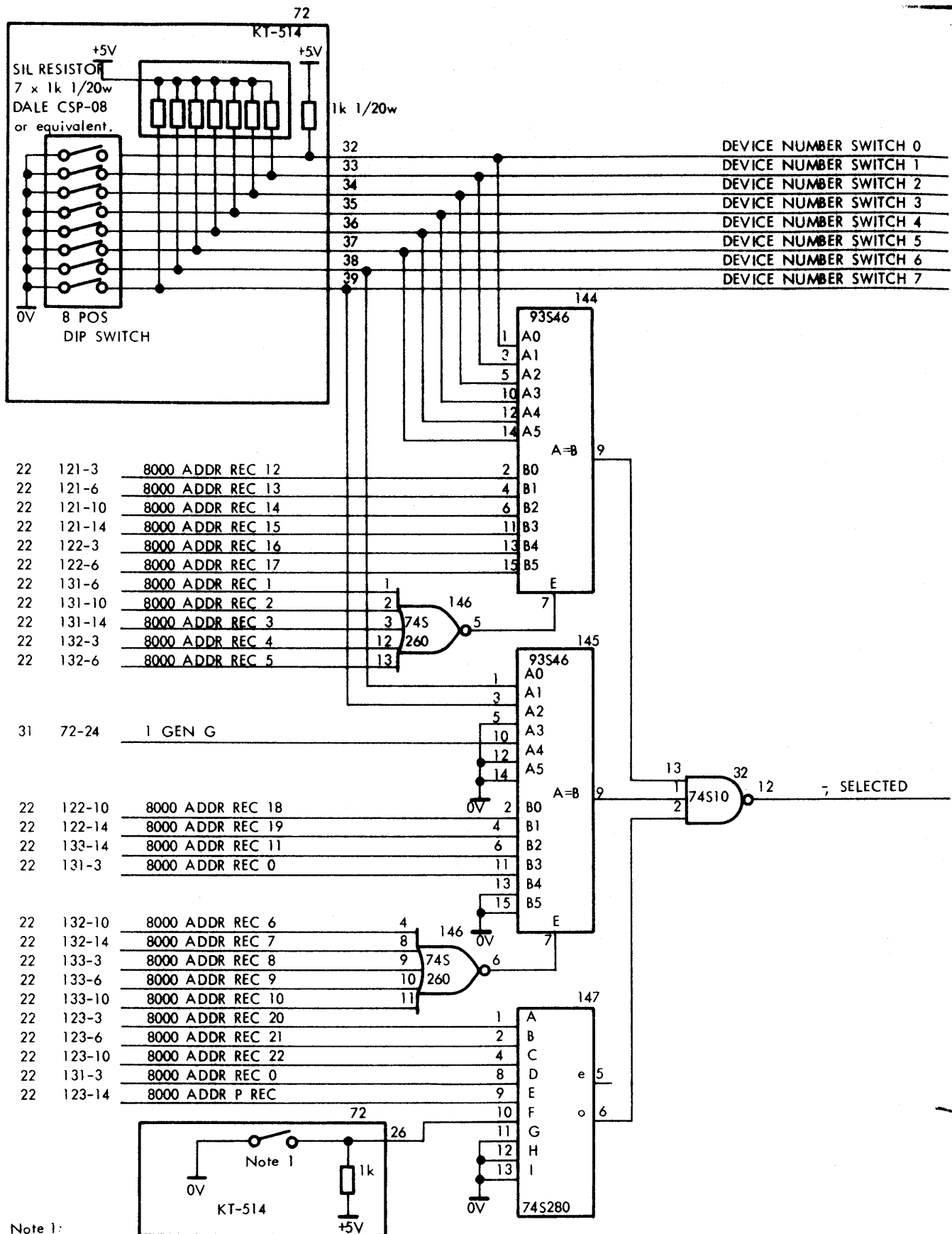
FPA 801

Dwg. No.

A24727

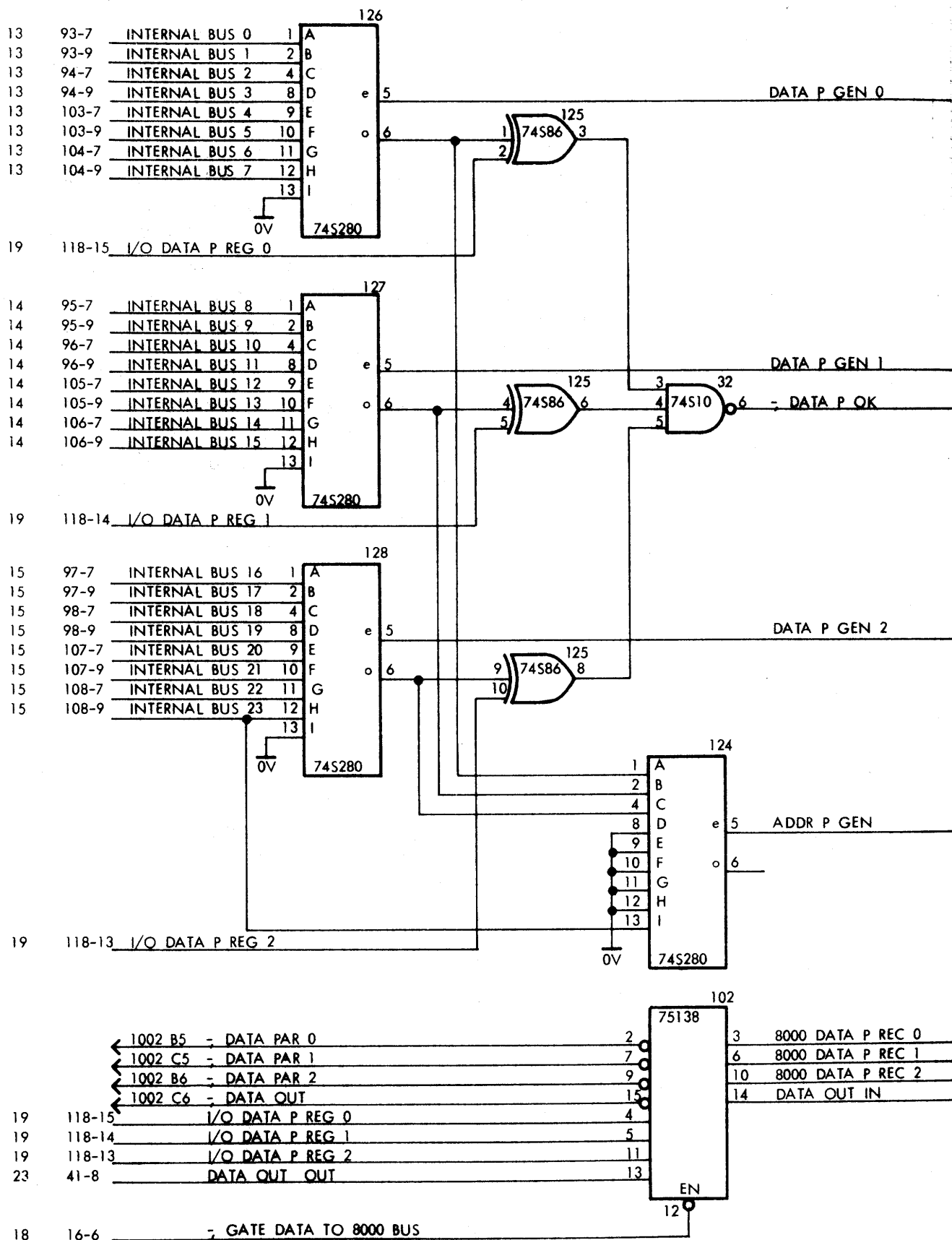
DEVICE ADDRESS DECODING

16



74S280		OUTPUT	
Numbers of inputs A-I that are high		e	o
0 - 2 - 4 - 6 - 8		H	L
1 - 3 - 5 - 7 - 9		L	H

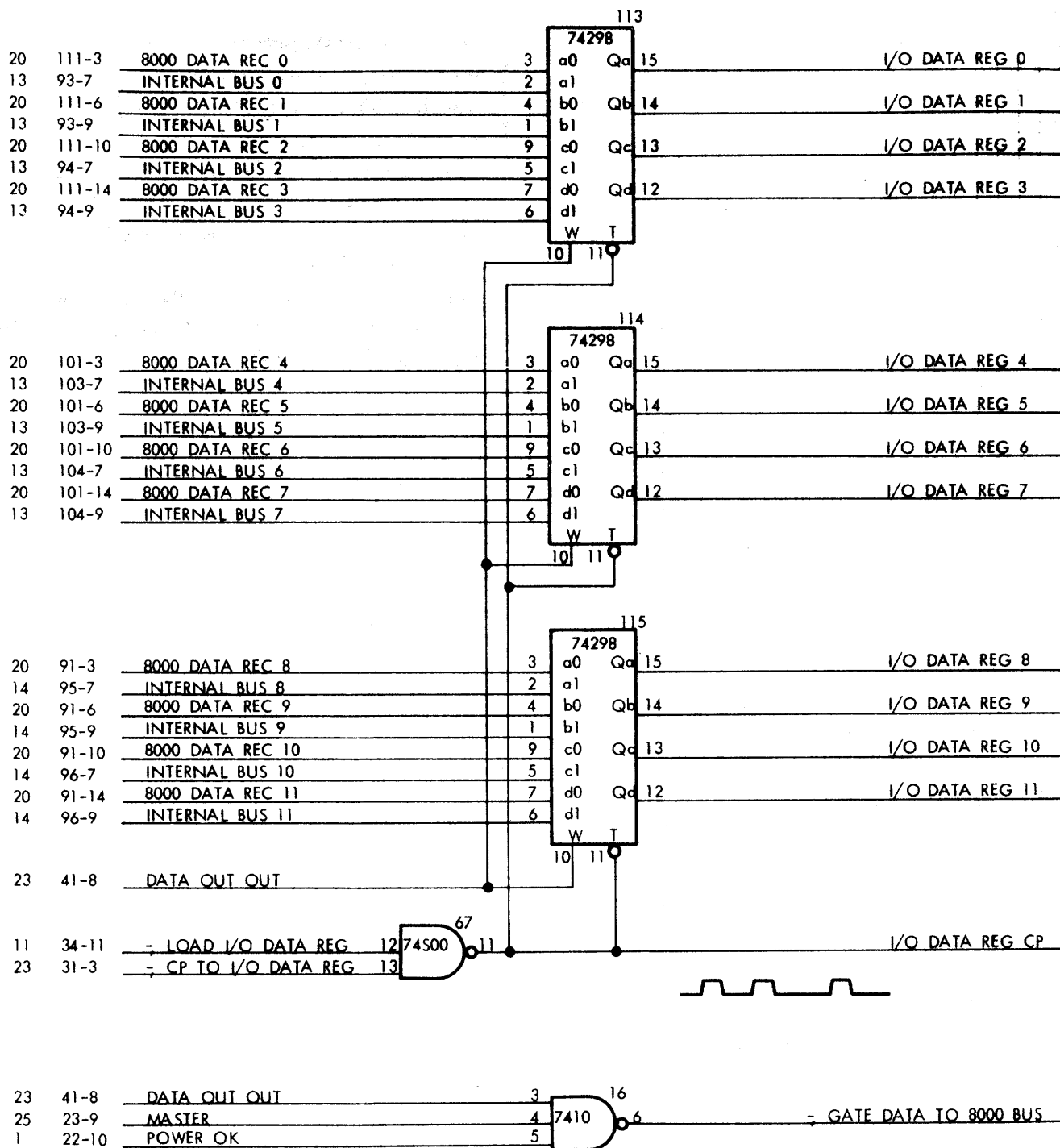
SIGNAL	DESTINATION	DESCRIPTION
ADDR. P. GEN DATA P. GEN 0 DATA P. GEN 1 DATA P. GEN 2 -,DATA P. GEN OK DATA OUT IN	21 136-18 19 118-2 19 118-1 19 118-5 5 70-6 24 31-8 24 31-9	Data parity is checked/generated and address parity generated by means of 4 parity chekers/generators connected to the FPA 801 internal bus. Data parity involves 3 parity bits, which makes the parity of the 3 characters of the RC 8000 word odd: Data parity 0 valid for 0:7 Data parity 1 valid for 8:15 Data parity 2 valid for 16:23 The parity bit of the address is bit 23, which makes the parity of the address bits 0 : 23 odd. The data parity ok signal is connected to the condition selector to be used by the microprogram.
8000 DATA P REC. 0	19 118-3	
8000 DATA P REC. 1	19 118-4	
8000 DATA P REC. 2	19 118-9	
Unit FPA 801	PARITY CHECKER & GENERATOR	
Dwg. No. A24728		17



SIGNAL	DESTINATION	DESCRIPTION
I/O DATA REG 0 : 7	13,20	The FPA 801 input/output register has two input ports of which one is connected to the internal bus and one to the RC 8000 data receivers. The output of the I/O data register is connected to the RC 8000 data transmitters and to the FPA 801 data selector. All data transfer between FPA 801 and RC 8000 bus takes place via this register. In case of data-out transfer the I/O data register and the I/O address register is loaded from the internal bus. Simultaneously with load of the I/O address register a bus cycle is requested. When FPA 801 becomes busmaster the I/O data register is gated to the RC 8000 data bus and the I/O address register to the RC 8000 address bus. In case of data-in transfer the I/O address register is loaded from the internal bus and a bus cycle is requested. When FPA 801 becomes bus master the I/O address register is gated to the RC 8000 data bus. When the addressed slave places data on the RC 8000 data bus the data bus lines is deskewed and the I/O data register is loaded with data from the data bus. In both cases a bus ready signal notifies the microprogram when the bus transfer is complete.
I/O DATA REG 8 : 11	14,20	
I/O DATA REG CP	19 112-11	
	19 116-11	
	19 117-11	
	19 118-11	
-GATA DATA TO 8000 BUS	17 102-12	
	20 81-12	
	20 82-12	
	20 91-12	
	20 92-12	
	20 101-12	
	20 111-12	

Unit	I/O DATA REGISTER 0 : 11	
FPA 801		
Dwg. No.		
A24729		18

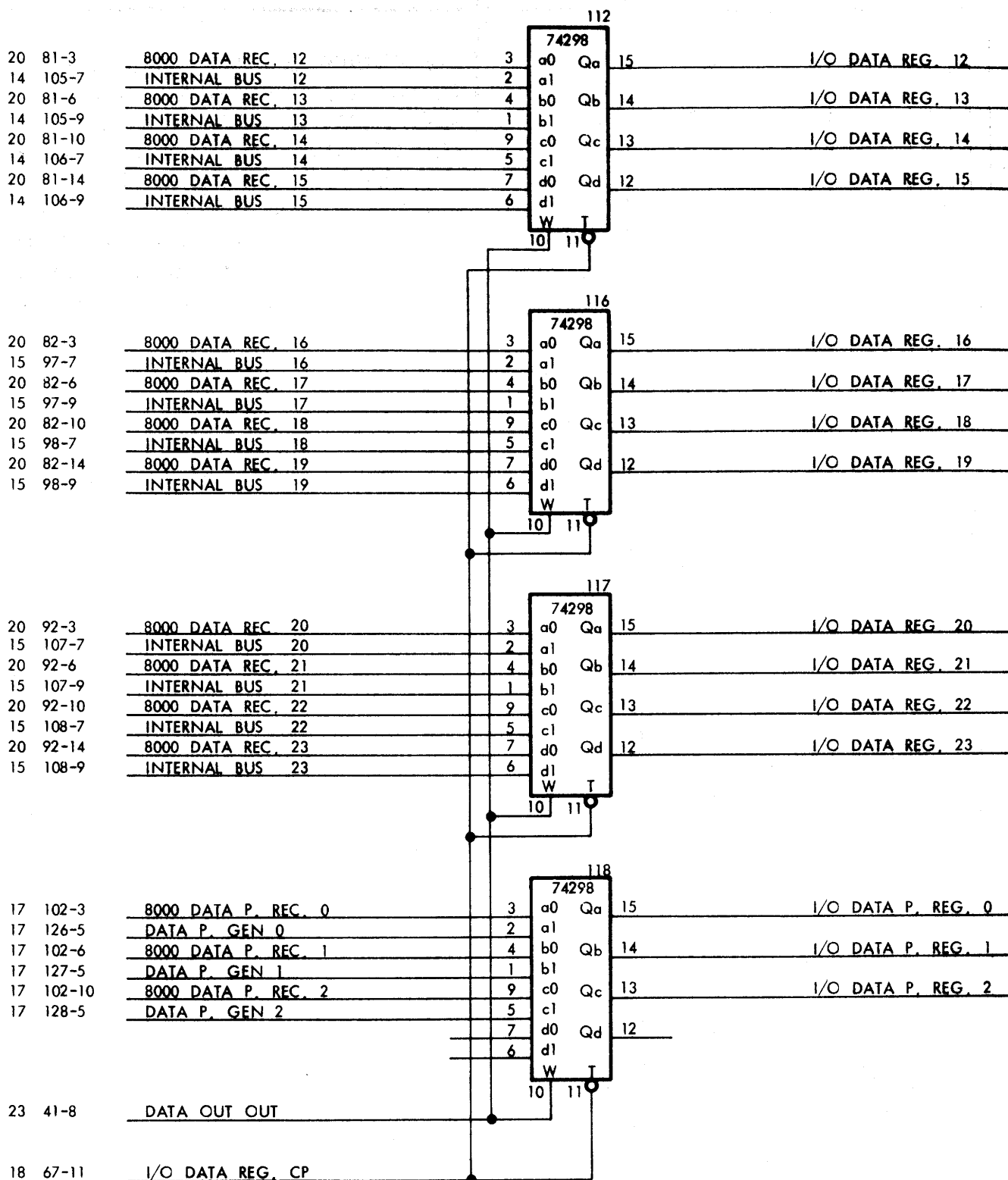
750927 VH
770317 OKJ
770401 LLM 770406 VH.



SIGNAL	DESTINATION	DESCRIPTION
I/O DATA REG. 12 : 15	14,20	The I/O data parity register has two input ports. One port is connected to the RC 8000 data parity receivers and the other to the data parity generator. Output of the I/O data parity register is connected to the data parity checker and to the RC 8000 data parity transmitters (refer to diagram 17). The I/O data parity register serves as buffer for the parity bits received/generated from/to the RC 8000 bus.
I/O DATA REG. 16 : 23	15,20	
I/O DATA P. REG. 0 : 2	17	

Unit		
FPA 801	I/O DATA REGISTER 12 : 23 &	
Dwg. No.	I/O DATA P. REG. 0 : 2	
A24730		19

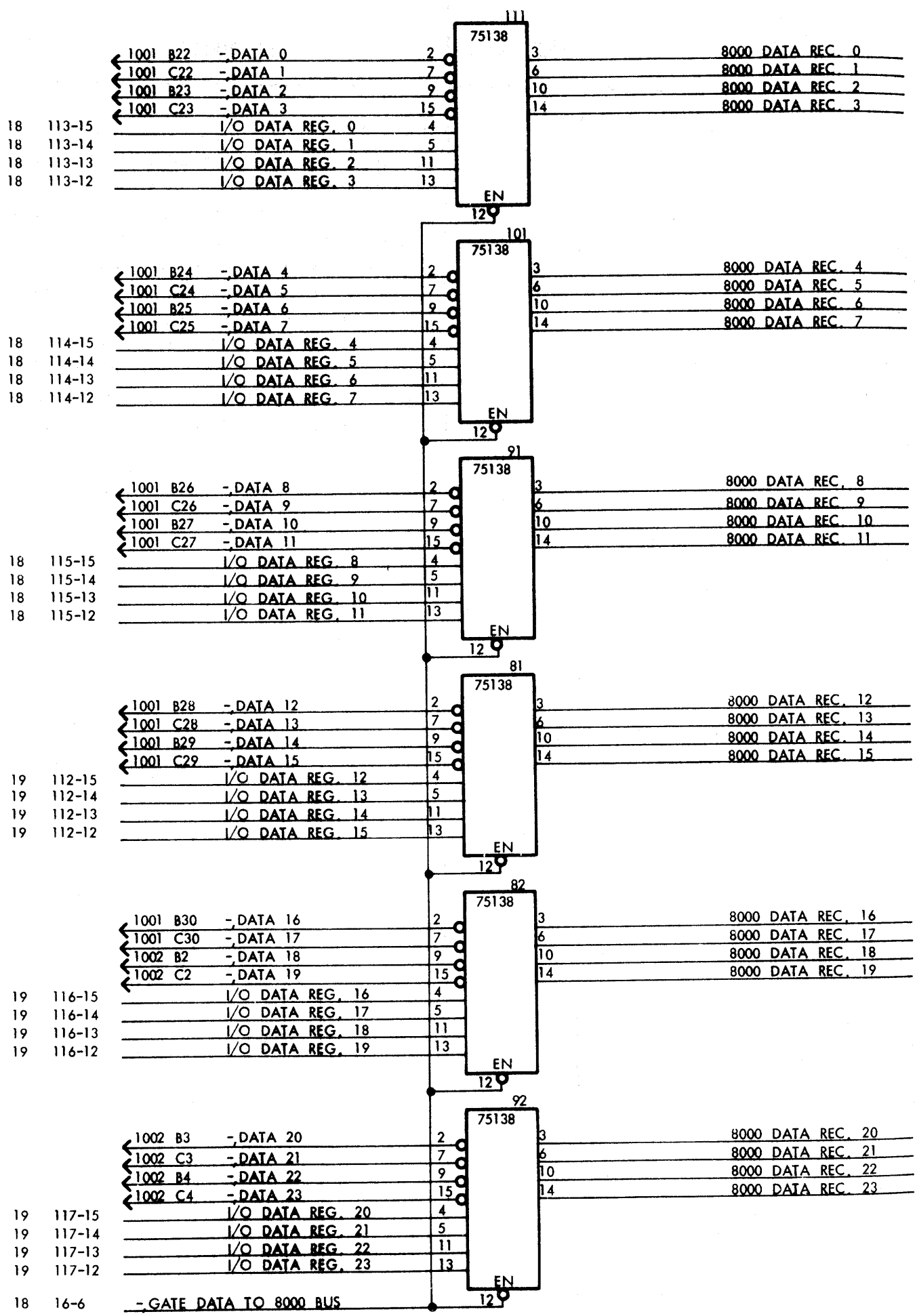
750927 VH. 770321 AMS. 770401 LLM. 770406 VH.



SIGNAL	DESTINATION	DESCRIPTION
8000 DATA REC 0 : 11 8000 DATA REC 12 : 23	18 19	The RC 8000 data bus is a bidirectional 24 bits wide bus. The bus is terminated with 2 x 120 E. 120E is placed in the BUS CONTROL UNIT and 120 E is placed near the last controller on the bus. The bus is driven by open collector circuits cape able of sinking ~ 60 mA. FPA 801 drives the bus by means of the SN 75138, which is a quad bus - transceiver.

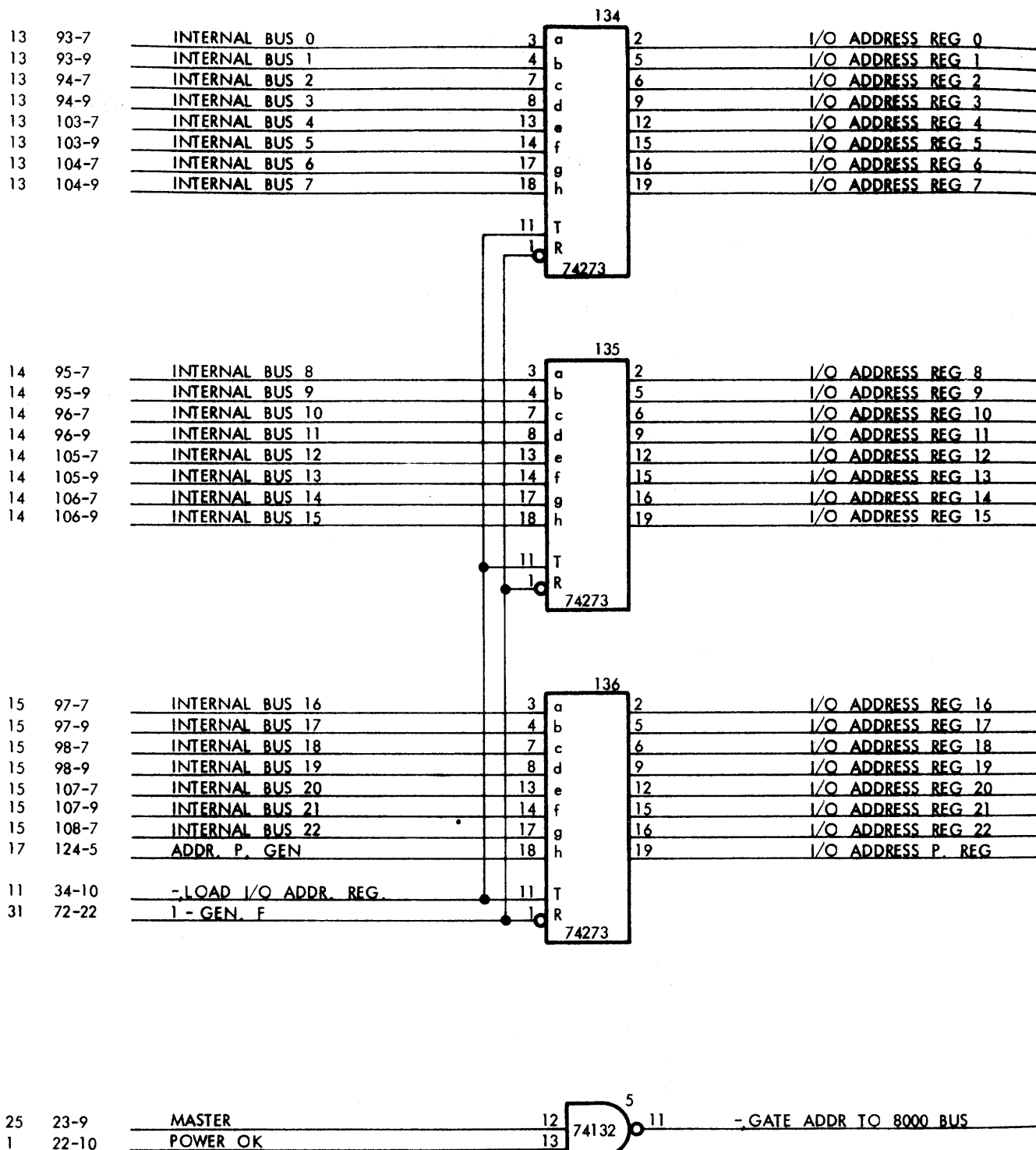
Unit	RC 8000 DATA BUS TRANSCEIVERS	20
FPA 801		
Dwg. No. A24731		

750924 VH, 770322 AMS, 770401 LLM 770406 VH.

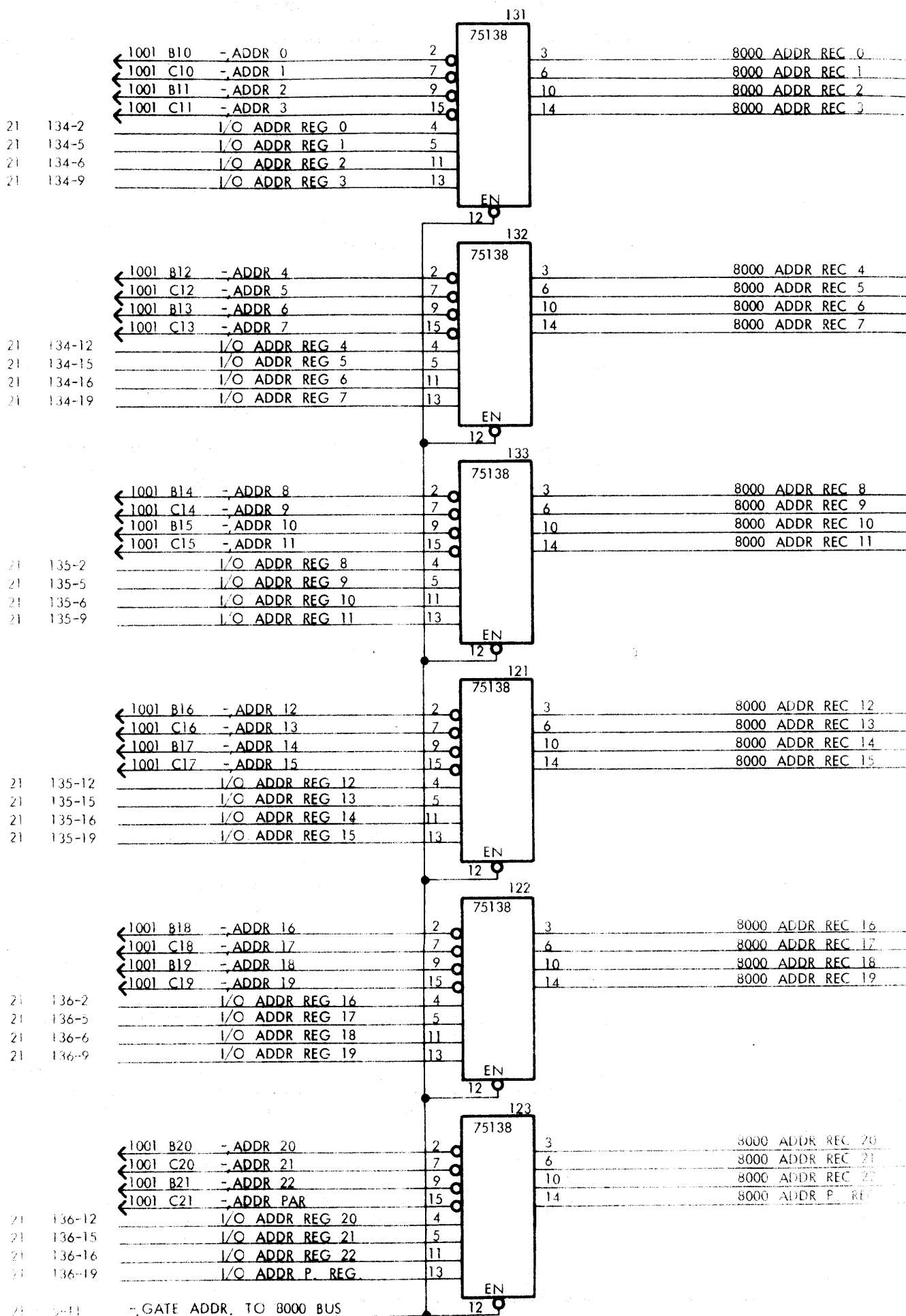


SIGNAL	DESTINATION	DESCRIPTION
I/O ADDRESS REG.	22	The FPA 801 I/O address register serves as buffer for the RC 8000 memory address during data transfers to and from FPA 801 and as buffer for the interrupt destination address during interrupt. A bus request procedure is always initiated simultaneously with the load of the I/O address register, and when FPA 801 becomes busmaster the I/O address register is gated to the RC 8000 bus via the address bus transceivers. The inputs of the I/O address register are connected to the FPA 801 internal bus.
Unit FPA 801	I/O ADDRESS REGISTER	
Dwg. No. A24732	21	

750927 VH, 770322 AMS, 770401 LLM 770406 VH.



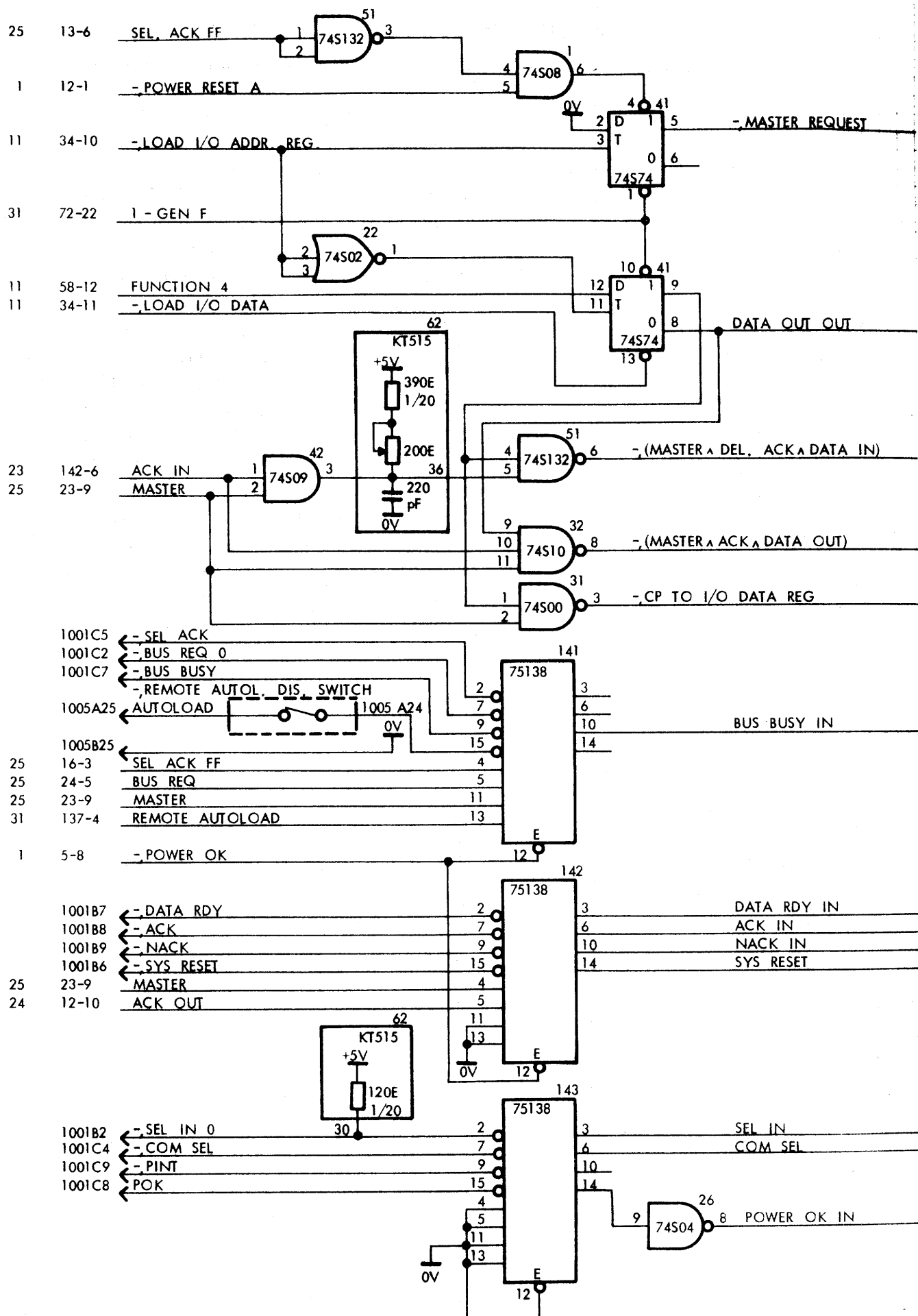
SIGNAL	DESTINATION	DESCRIPTION
8000 ADDR. REC 0 - 22	16	The RC 8000 address bus is a bidirectional bus 23 bits wide (excl parity bit). The address bus is driven and terminated as the data bus (refer to diagram 20).
8000 ADDR. P. REC	16	
Unit		RC 8000 ADDRESS TRANSCEIVERS
FPA 801		
Dwg. No.		
A24733		22



SIGNAL	DESTINATION	DESCRIPTION
ACK IN	25 24-9	The acknowledge in signal is a respond to the data ready signal. Ack in indicates: 1. Data in transfers: The slave has recognized the address and has placed data on the data lines. 2. Data out transfer: The slave has recognized the address and received data correctly.
BUS BUSY IN	25 24-8	Indicates to FPA 801 that the bus is being used by another busmaster.
COM SEL	25 13-1 25 14-12 25 23-3	The common select signal is lead to all controllers in parallel.
CP to I/O DATA REG	18 67-13	This signal loads I/O data register during data in transfers (refer to diagram 18).
DATA OUT OUT	17 102-13 18 16-3,113-10 18 114-10,115-10 19 116-10,117-10 19 118-10,112-10	This FF is set to logical 1 during data-out transfers and to logical 0 during data-in transfer. The FF controls the Data out transmitter to the 8000 bus and selects the proper data path to the I/O data register.
DATA RDY IN	24 7-4 24 42-10 24 51-13	The "and" of data ready in = "1" and master = "0" is delayed 150 nS and then "anded" with data out in = 1 and selected = 1 to form the load device function signal and the acknowledge out signal. The 150 nS compensation delay compensates for: a. skew in the BUS MASTER b. Transceiver skew c. Cable skew d. Address decoding in FPA 801
-(MASTER ^ ACK ^ DATA OUT)	24 14-2	This signal generates the bus ready signal during data out transfers (refer to diagram 24)
-(MASTER ^ DEL ACK ^ DATA IN)	24 14-1	This signal generates the bus ready signal during data in transfers. The acknowledge signal received from the slave is delayed 120 nS This delay compensates for: a. Skew in the SLAVE b. Transceiver skew c. Cable skew
-,MASTER REQUEST	25 23-2 25 24-12,24-13	This FF is set to logical 1 when FPA 801 requires access to the RC 8000 bus.
NACK IN	24 11-2 25 24-10	The not acknowledge signal from the slave causes set of the bus communication error signal.
POWER OK IN	1 42-12 1 42-13	This signal originates in the power supply of the CHS 802 chassis. After a delay this signal is used to generate the FPA 801 signal power ok, which is used to initializ the logic.
SEL. IN	25 13-2 25 14-13 25 23-3 25 13-9	The select signal is daisy chained through all controllers connected to the RC 8000 bus. If FPA 801 receives the select in signal after having requested bus access, the select out signal to the next controller is inhibited and the select acknowledge signal generated.
SYS RESET	1 12-3 1 12-5	

Unit		
FPA 801	DATA TRANSFER CONTROL LOGIC	
Dwg. No.		23
A12958		

770406 VH.
770324 AMS, 770401 LLM
750928 VH.



SIGNAL	DESTINATION	DESCRIPTION
ACK OUT	23 142-5	The upper part of this diagram shows the bus status circuits. The bus ready FF is cleared when FPA 801 requires access to the RC 8000 bus. The FF is set to logical 1 when FPA 801 becomes bus master and the slave has responded to the data ready signal by returning ack or nack. The bus ready FF is also set to logical 1 in case of bus time out i.e. no respond from the slave at all, however, in this case the bus time out FF is set to logical 1 too. If the slave returns a nack signal the the bus communication error FF is set. The or result of bus time out, bus communication error forms the bus error signal, which together with the bus ready and bus time out signals is wired to the condition selector to be used by the microprogram. The lower part of the diagram shows the FPA, 801 acknowledge circuits, which are used when FPA 801 is slave. The load device function signal loads the device function register thus starting a reset function or a new channel program. The ack out signal controls the ack - knowledge transmitter.
-,BUS COM ERROR	This diag.	
-,BUS ERROR	5 70-7	
-,BUS RDY	5 68-7 25 1-12	
-,BUS TIME OUT	This diag. 5 68-6	
-,SET BUS COM. ERROR	This diag.	
-,SET BUS RDY.	This diag.	
-,SET BUS TIME OUT	This diag.	
-,LOAD DEV. FUNCTION	2 2-14 2 3-14	

Unit	BUS STATUS		
FPA 801			
Dwg. No.			24
A24737			

SIGNAL	DESTINATION	DESCRIPTION
BUS REQ	23 141-5	The logic on this diagram generates the signals necessary in connection with the bus master selection procedure; which is initiated when FPA 801 sets the master request FF to logical 1. The master request FF causes a bus request signal to be send to the bus control unit (BCU). The BCU responds to the bus request by generating the comman select and select in signals, provided another selection phase is not in progress (SACK line = "1"). The select signal is daisy chained through all control- lers connected to the bus. A controller, which has not requested bus control, passes the signal to the next controller, FPA 801 does this by means of the enable FF. A controller which has requested bus control breaks the chain as set the select acknowledge signal to logical 1. The common select signal is connected to all controllers in parrallel. The select signals are cleared simultaneously. By connecting the common select signal to all controllers in parallel the termination of the bus request procedure is made as fast as possible, since the trailling edge of the select signal do not need to ripple through the units.
MASTER	18 16-4	
	21 5-12	
	23 31-2	
	23 32-11	
	23 42-2	
	23 141-11	
	23 142-4	
	24 11-1	
	24 42-4	
	24 42-5	
	This diag.	
- , MASTER	24 42-9	
	This diag.	
SEL ACK FF	23 51-1	
	23 51-2	
	23 141-4	
	This diag.	
- , SEL OUT 0	Plug 1001-B3	
Unit	BUS MASTER SELECTION LOGIC	
FPA 801		
Dwg. No.		
A24738		
	25	

750928 VH 770324 OKJ 770404 LL.M. 770406 VH.

COM SEL

23 143-6

1 12-1

FPA 801

A12883

- POWER RESET A

ENABLE FF

- MASTER REQUEST

23 41-5

1-GEN G

31 72-24

SEL IN

23 143-3

SEL ACK FF

1 12-1

- POWER RESET A

31 72-24

1-GEN G

23 143-3

SEL IN

23 143-3

1-GEN G

23 143-3

SEL IN

23 143-3

1-GEN G

23 143-3

SEL IN

23 143-3

1-GEN G

23 143-3

SEL IN

23 143-3

1-GEN G

23 143-3

SEL IN

23 143-3

1-GEN G

23 143-3

SEL IN

23 143-3

1-GEN G

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1-GEN G

23 143-3

SEL IN

23 143-3

1-GEN G

23 143-3

SEL IN

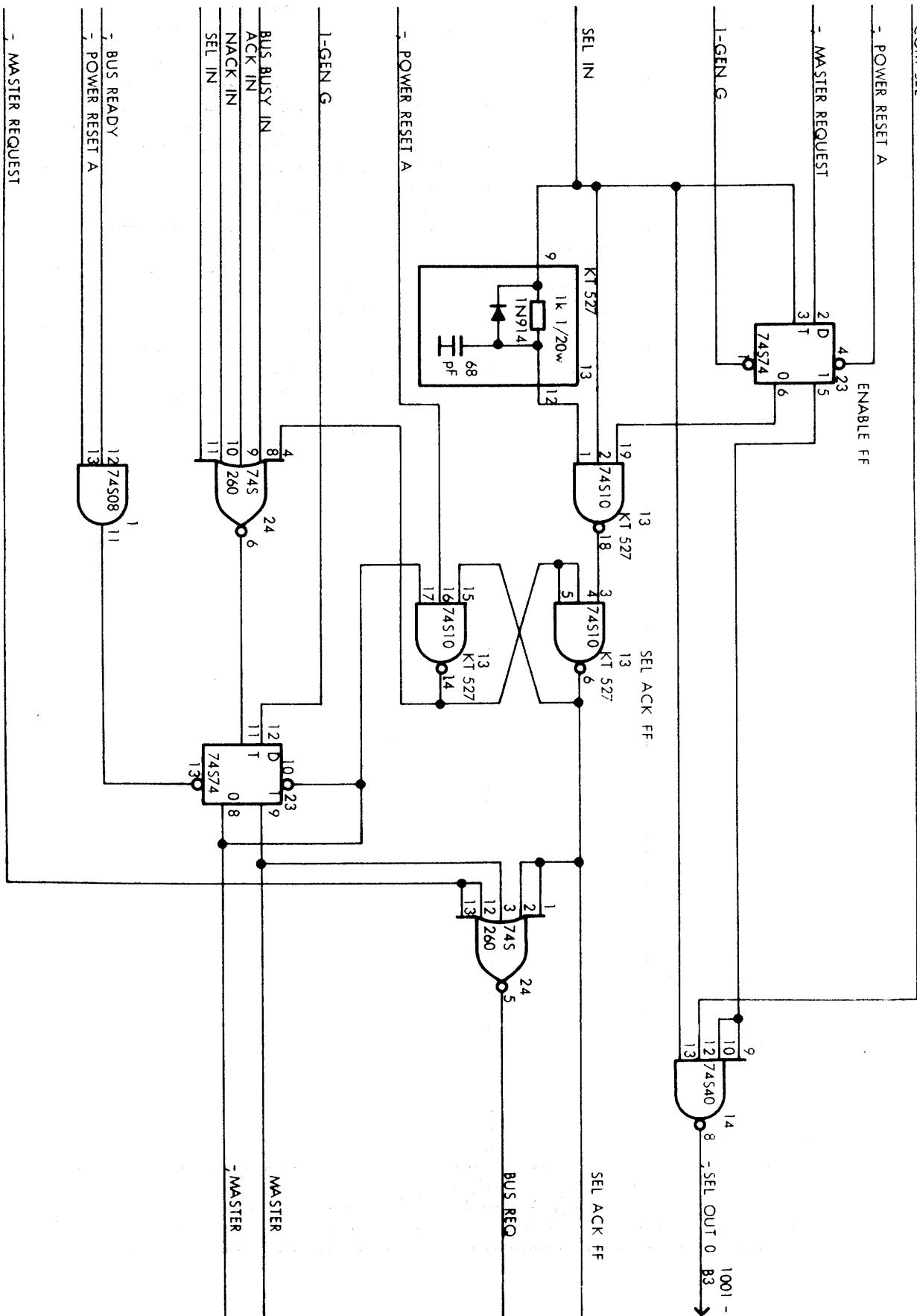
23 143-3

1-GEN G

23 143-3

SEL IN

23 143-3



Circuit Diagram

BUS MASTER SELECTION LOGIC

SIGNAL		DESTINATION	DESCRIPTION
AUTOLOAD OUT -,CHAR. RDY CLEAR TRM DONE END OF READ CHAIN -,INITIATE LAST CHAR. OUT REQUEST OUT -,REQUEST OUT SENSE TIMER TIMER STATUS -,TRM DONE TRANSMIT BLOCK END WAIT		30 50-1	When FPA 801 wants to transmit a character the signal clear transmitter done is generated by the microprogram. This signal loads the transmitter character buffer and starts the transmitter control circuits, which, if the previous request have been acknowledged by the opposite controller, causes the character to be placed on the data lines out, and the request FF to be set. When the character has been placed on the data out lines, i.e. transferred from the transmitter char. buffer to the transmitter char. register, the transmitter done FF is set to logical one. The done signal is lead to the condition selector and via the microprogram the next character is fetched and the transmitter char. buffer loaded again. When the opposite controller has recognized the request signal and stored the character, it responds to the request by raising the request acknowledge signal, which clears the FPA 801 request FF. To identify the last character, this character is accompanied by the last character signal. Included in the transmitter circuits is timer, which is started simultaneously with set of the request FF. This timer causes via the microprogram the time out status to be set, if the opposite controller does not respond to the request signal. The lower part of diagram 26 shows some 1 bits register of which 6 are used as internal status signals, which are connected to the condition selector. The microprogram senses these status bits in order to jump through the program correctly. The last register is used for the autoloader signal which is app. 1,2 uS wide.
		This diag. 27 49-11	
		This diag. 27 45-11 27 46-11	
		5 70-3 28 22-12	
		5 70-2	
		30 60-13	
		30 40-1 30 40-10	
		This diag.	
		5 68-1	
		This diag. 5 70-8	
		This diag. 5 68-20	
		5 68-8	
		This diag. 5 70-19	
		5 68-17	
Unit	FPA 801		
Dwg No.	TRANSMITTER CONTROL & TIMER -		
	TRM/REC INTERNAL STATUS		26
	A12959		

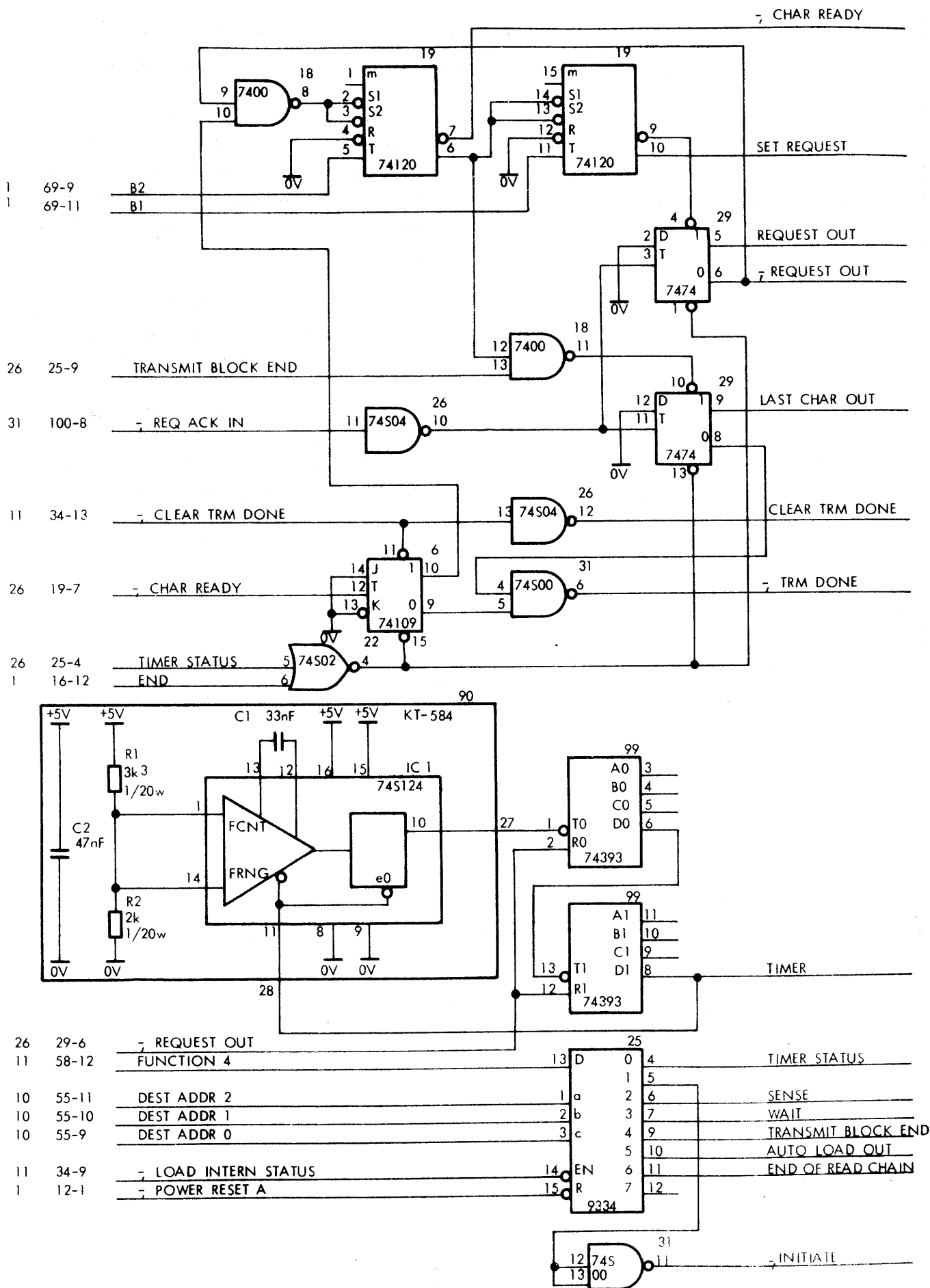
18-014, 018

770406 VH.

770330 LLM

770329 OKJ

770206 VH



SIGNAL	DESTINATION	DESCRIPTION
TRM CHAR REG 0-7 TRANSMITTER PARITY	This diag. 29 29 60-3	The transmitter char. buffer and the transmitter char register are two 8-bits registers capeable of storing two characters. The transmitter char. buffer has 3 input ports, which makes it possible to load the register from: 1. Internal bus bits 0-7 or 2. Internal bus bits 8-15 or 3. Internal bus bits 16-23. The transmitter char. register drives the data transmitters to the opposite controller and the parity generator (Refer also to transmitter control circuits diagram 26).
Unit	TRANSMITTER CHAR. BUFFER & REGISTER	
FPA 801		
Dwg. No.		
A24741		
	27	

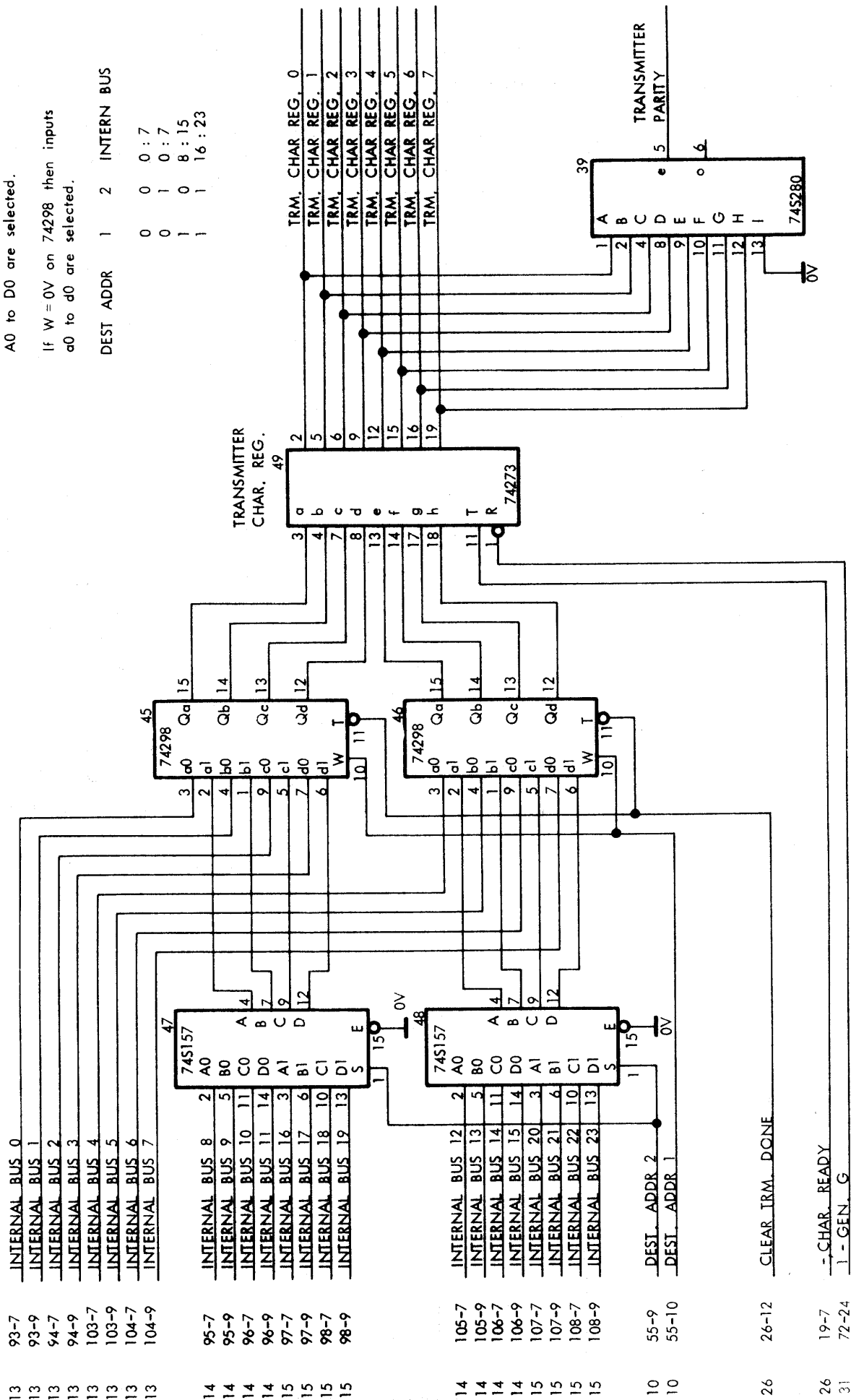
750925 VH. 770324 AMS. 770404 LLM. 770406 VH.

If SEL = 0V on 74157 then inputs
A0 to D0 are selected.

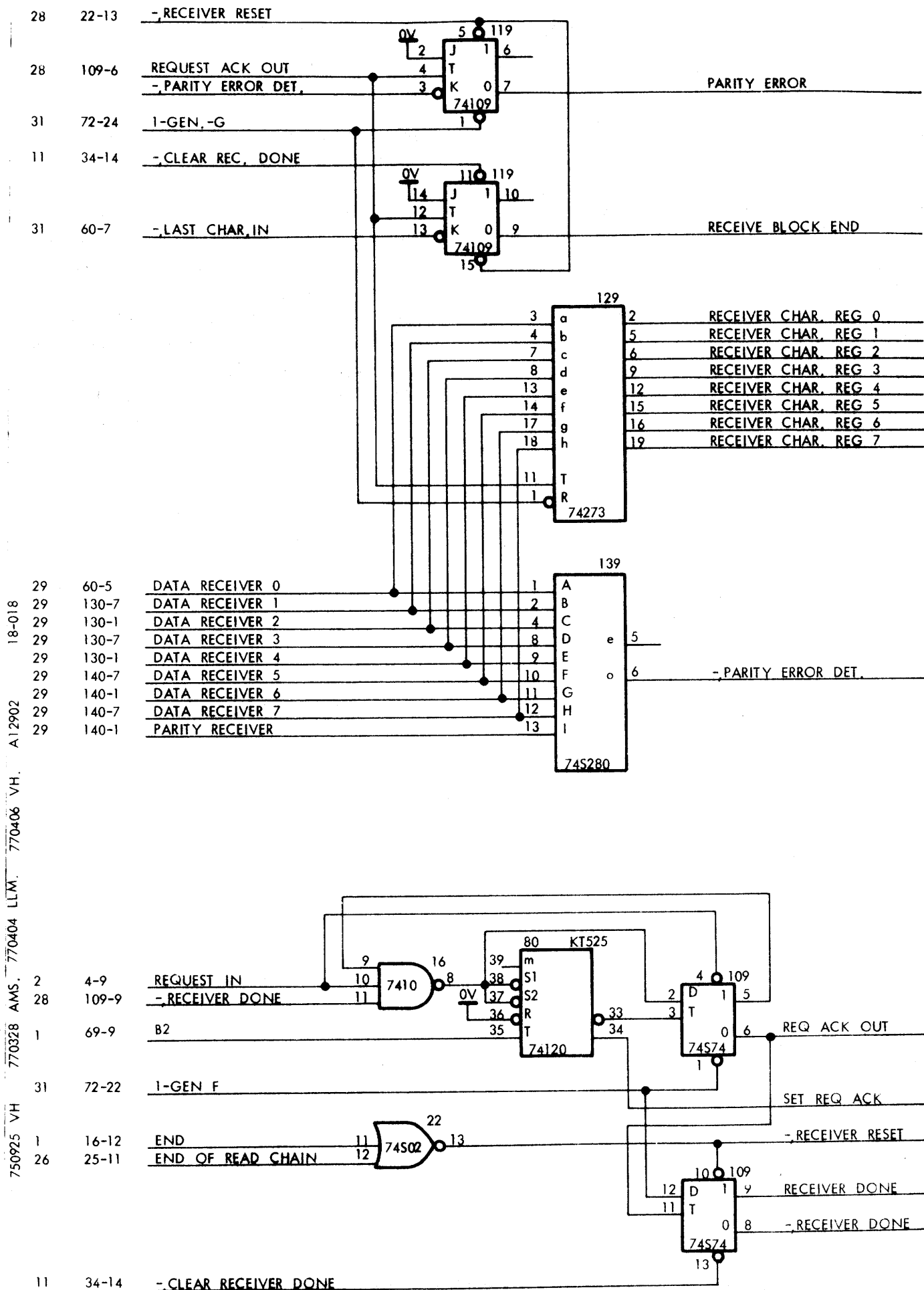
If W = 0V on 74298 then inputs
a0 to d0 are selected.

DEST ADDR 1 2 INTERN BUS

0 0 0 0 : 7
0 1 0 : 7
1 0 8 : 15
1 1 16 : 23

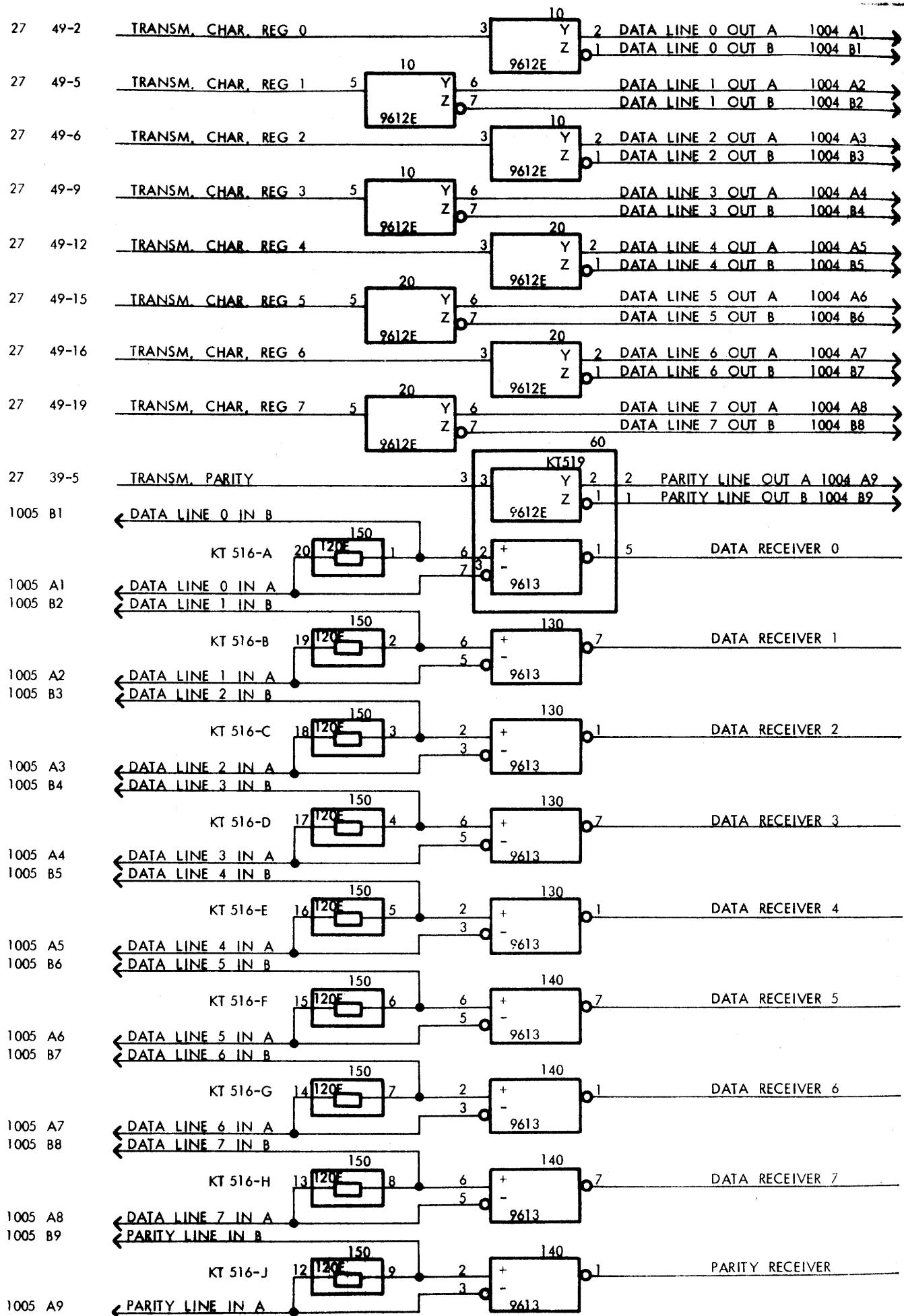


SIGNAL	DESTINATION	DESCRIPTION
PARITY ERROR -, PARITY ERROR DET RECEIVE BLOCK END RECEIVER CHAR. RECEIVER DONE -, RECEIVER DONE -, RECEIVER RESET REQ ACK OUT	5 70-4 This diag. 5 68-3 13,14,15. 5 68-4 This diag. This diag. This diag. 30 30-10	When FPA 801 enters the receive mode, the microprogram generates the signal clear receiver done, which clears the receive block end FF and the receiver done FF. Upon the reception of a request in signal from the opposite controller the request acknowledged FF is set, the receiver done FF set and the receiver char register loaded with the character from the data input lines. The receiver done signal notifies the microprogram that a character is ready in the receiver char. register. The microprogram stores the character in the RALU and clears the receiver done FF, thus enabling the reception of another character. The last character received must be accompanied by the last char in signal which causes the receive block end FF to be set. The receive block end signal is wired to the condition selector and in this way the microprogram detects the end of the block. The parity error FF is set if the parity of the received character is even, however, the parity error FF is not sensed by the microprogram untill receive block and. When 3 chars. has been stored in the RALU, a RC 8000 bus cycle is requested, and 3 characters transferred to RC 8000 memory.
Unit FPA 801 Dwg. No. A24742	RECEIVER CONTROL & RECEIVER CHAR. REGISTER	
		28



SIGNAL	DESTINATION	DESCRIPTION
DATA LINE OUT A & B 0 - 7 PARITY LINE OUT A & B DATA RECEIVER 0 - 7 PARITY RECEIVER	PLUG 1004 PLUG 1004 28 28	The line drivers used in FPA 801 provides differential output signals, and are used to drive a twisted pair line with an impedance of app. 120 E. The drivers are single supplied and uses only +5V. The line receivers used are designed to sense small differential signals in the presence of large common - mode noise; up to $\pm 15V$ common mode input voltage can be tolerated. The receivers are single supplied and uses only +5V. Bit 0 of the data lines is alway the most significant bit. The parity line makes the parity odd.
Unit FPA 801 Dwg. No. A24743	DATA LINES TO AND FROM FRONT END PROCESSOR	
		29

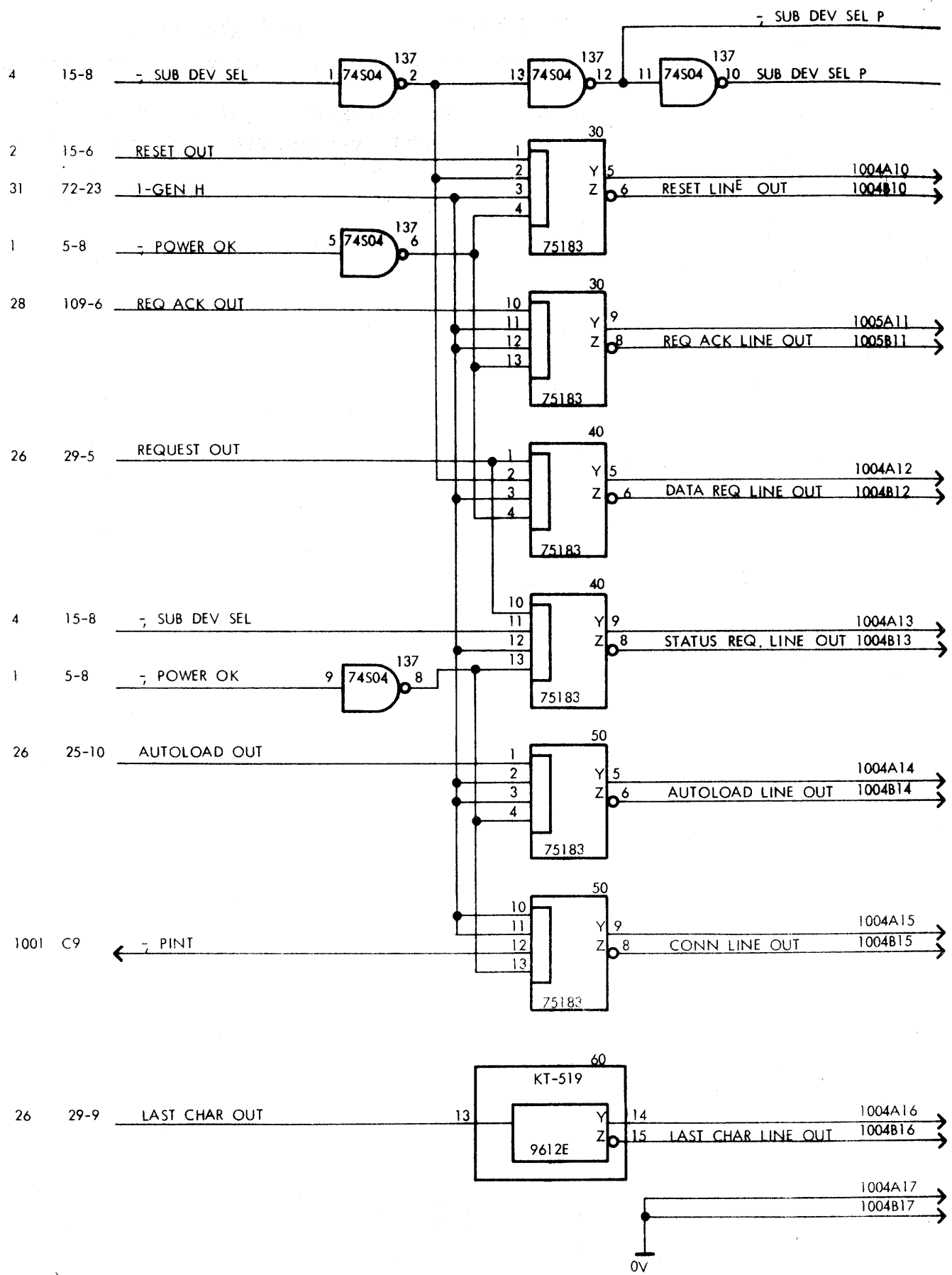
750929 VH. - 770328 AMS. 770404 LLM. - 770406 VH.



SIGNAL	DESTINATION	DESCRIPTION
RESET LINE OUT	PLUG 1004	This line when logical 1 indicates to the receiver in the opposite controller that the FPA 801 transmitter has been reset.
REQ ACK LINE OUT	PLUG 1005	When this signal changes from false to true state, it indicates to the transmitting unit that the character on the data lines has been stored in the receiving unit. Upon the reception of the rising edge of the acknowledge signal the transmitting unit is allowed to fetch the next character and place it on the data lines.
DATA REQ LINE OUT	PLUG 1004	This signal when logical 1 indicates to the receiving unit that a data character is ready on the data lines 0 : 7. The signal is generated by the transmitter in the transmitting unit.
STATUS REQ LINE OUT	PLUG 1004	This signal when logical 1 indicates to the receiving unit that a status character is ready on the data lines 0 : 7. The signal is generated by the receiver in the transmitting unit.
AUTOLOAD LINE OUT	PLUG 1004	This line is necessary to be able to initiate on auto-load procedure in the front-end computer under RC 8000 program control. Likewise, the front-end computer may use the line to initiate on autoloading procedure in RC 8000 (Autoload Line in).
CONNECTED LINE OUT	PLUG 1004	This line when logical 1 indicates to the receiving unit that power is on. The connected signal enables following signals in the receiving unit: RESET IN REQUEST ACK IN DATA REQUEST IN STATUS REQUEST IN REMOTE AUTO LOAD
LAST CHAR LINE OUT	PLUG 1004	When logical 1 this line indicates the end of the block. The last char. signal is generated simultaneously with the emission of the last character in the block.

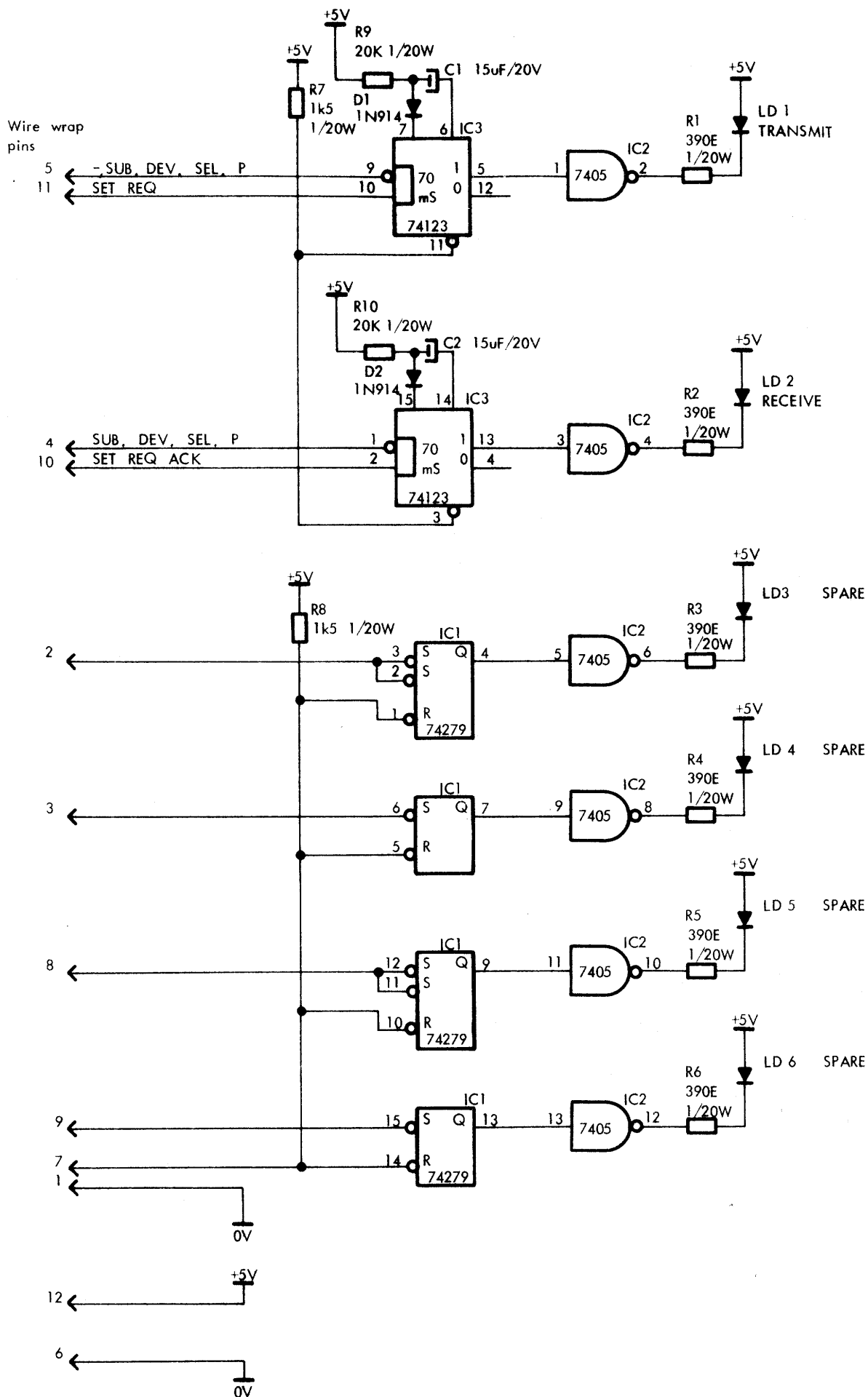
Unit			
FPA 801	CONTROL LINES TO FRONT END PROCESSOR		
Dwg. No.			30
A12960			

18-009
A12903
770406 VH.
770404 LLM.
770325 OKJ
770131 VH

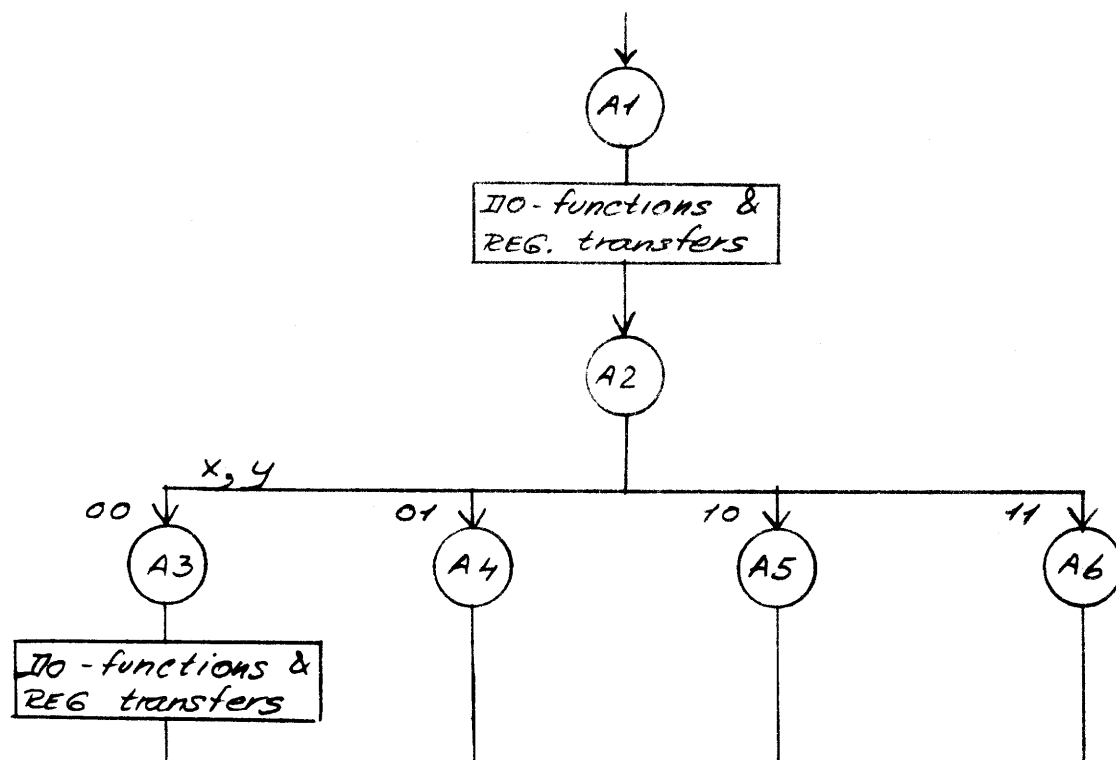


SIGNAL	DESTINATION	DESCRIPTION
- , RESET IN	2 6-5	Concerning the description of control signals received from front - end processor refer <u>to</u> the description of the control signals to front - end processor diagram 30.
- ,REQ ACK IN	26 26-11	
- ,DATA REQUEST IN	2 4-11	
- ,STATUS REQUEST IN	2 4-10	
REMOTE AUTOLOAD	23 141-13	
CONNECTED IN	31 100-4	
	31 100-10	
	31 110-4	
	31 110-10	
	31 120-4	
	12 26-5	
- ,LAST CHAR IN	28 119-13	

76040s VH, 770328 AMS, 770405 LLM, 770406 VH.



To understand the micro program flowcharts the following explanation is necessary:



The number in the circle is the actual micro address in oktal notation.

The micro program steps unconditional from A1 to A2. In A2 the condition x, y is selected, and if :

$x, y = 0, 0$, the micro program steps to A3

$x, y = 0, 1$, the micro program steps to A4

$x, y = 1, 0$, the micro program steps to A5

$x, y = 1, 1$, the microprogram steps to A6

Besides the circle the most important do-functions and register transfers are described in the boxes belonging to the circles.

INSTRUCTION

PROM 565								PROM 564				PROM 563				PROM 562			
REG. ALU FUNCTION												SOURCE ADDR.				DEST ADDR.			
17	16	15	14	13	11	10	Ci		0	1	2		0	1	2				

"0" ~ Select REG. ALU
 "1" ~ Select EXTERN

NEXT ADDRESS

PROM 561				PROM 560				PROM 559				PROM 558			
CONDITION SELECT 0				CONDITION SELECT 1				NEXT ADDRESS							
0	1	2	3	0	1	2	3	0	1	2	3	4	5	6	7

NEXT CONDITION 1

NEXT CONDITION 0

FUNCTIONS

PROM 557				PROM 556			
D	F1	F2	F3	F4	F5	F6	F7

FUNCTION 7
 FUNCTION 6
 FUNCTION 5
 FUNCTION 4
 FUNCTION 3
 FUNCTION 2
 FUNCTION 1
 -CHANGE DEVICE

CONSTANTS

PROM 555				PROM 554			
0	1	2	4	20	21	22	23

CONSTANT 2⁰
 CONSTANT 2¹
 CONSTANT 2²
 CONSTANT 2³
 CONSTANT 2¹⁰
 CONSTANT 2²¹
 CONSTANT 2²²
 CONSTANT 2²³

760203 VH, 770328 AMS, 770405 LLM, 770406 VH.

SOURCE		DESTINATION	
ADDR	SOURCE REGISTER	ADDR	FUNCTION
E 0 1 2		E 0 1 2	1 2 3 4 5 6 7
0	DESCRIPTION ADDRESS	0 0 0 0	1 1 1
1	CHANNEL PROGRAM ADDRESS	0 0 0 1	1 1 1
2	FIRST WORD ADDRESS	0 0 1 0	1 1 1
3	CHARACTER COUNTER	0 0 1 1	1 1 1
4	BUFFER	0 1 0 0	1 1 1
5	REMAINING CHAR COUNT	0 1 0 1	1 1 1
6	EVENT STATUS	0 1 1 0	1 1 1
7	COMMAND REGISTER	0 1 1 1	1 1 1
8	I/O DATA REGISTER	1 0 0 0	0 1 0
9	CONSTANT PROM	1 0 0 1	0 1 0
10	DEVICE NUMBER	1 0 1 0	0 1 0
11	RECEIVER CHARACTER REGISTER	1 0 1 1	0 1 0
12	EXTERNAL CONSTANTS	1 1 0 0	1 0 0
13		1 1 0 1	1 0 1
14		1 1 1 0	1 0 1
15		1 1 1 1	1 0 1
8		1 0 0 0	1 1 0
9		1 0 0 1	1 1 0
10		1 0 1 0	1 1 0
11		1 0 1 1	1 1 0
12		1 1 0 0	1 1 0
13		1 1 0 1	1 1 0
14		1 1 1 0	1 1 0
15		1 1 1 1	1 1 0

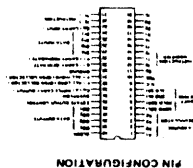
ADDR	DESTINATION REGISTER	COMMENTS
E 0 1 2		
0	DESCRIPTION ADDRESS	F1, 2 & 3 controls
1	CHANNEL PROGRAM ADDRESS	CP to Reg. ALU as follows:
2	FIRST WORD ADDRESS	1 2 3
3	CHARACTER COUNTER	No CP at all 0 0 0
4	BUFFER	CP to 16:23 0 0 1
5	REMAINING CHAR COUNT	CP to 8:15 0 1 0
6	EVENT STATUS	CP to 0:7 1 0 0
7	COMMAND REGISTER	CP to 0:23 1 1 1
8	TRANSMITTER CHARACTER BUFF 0:7	Function F5, 6, 7 being 0, 10 generates "CLEAR TRM DONE", which also loads TRM CHAR BUFF.
9	TRANSMITTER CHARACTER BUFF 0:7	
10	TRANSMITTER CHARACTER BUFF 8:15	
11	TRANSMITTER CHARACTER BUFF 16:23	
12	I/O DATA REGISTER	In fact the destination address is not used, since these registers are only loaded by F5, 6 & 7 being 100 or 101
13	I/O ADDRESS REG 0=WRITE, 1=READ	load of I/O ADDRESS causes start of bus.
14		Extern dest. function is infact not used, since these 1-bits registers are under control of the F5, 6 & 7 pulse = 110. Function 4 determines whether the register is set or cleared.
15		

FUNCTION 5, 6, & 7.

FUNG.		FUNCTION
5	6	7
0	0	0
0	0	1
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

	B I T				B I T
	0	1	2	4	
PARITY ERROR IN MEDIUM	0	1	0	0	2021 2223
RESET RECEIVED	0	1	0	0	0 0 0 0
BLOCK LENGTH ERROR	1	0	0	0	0 0 0 0
TIME-OUT	0	0	1	0	0 0 0 0
STATUS TRANSFER ERROR	0	0	1	0	0 0 0 0
BUS TIME OUT	0	0	0	0	1 0 0 0
BUS COM ERROR	0	0	0	0	0 1 0 0
BUS PARITY ERROR	0	0	0	0	1 0 0 0

INSTRUCTIONS & CONDITIONS

[illegible]

INSTRUCTION MODIFIERS IN THE 8 X 8 ROM --
POSITIVE LOGIC ($V_H \approx 3V$) INTERPRETATION

Y ₀	Y ₁	Y ₂	Y ₃	Y ₄	Y ₅	Y ₆	Y ₇	Y ₈	Y ₉	Y ₁₀	Y ₁₁	Y ₁₂	Y ₁₃	Y ₁₄	Y ₁₅	Y ₁₆	Y ₁₇	Y ₁₈	Y ₁₉	Y ₂₀	Y ₂₁	Y ₂₂	Y ₂₃	Y ₂₄	Y ₂₅	Y ₂₆	Y ₂₇	Y ₂₈	Y ₂₉	Y ₃₀	Y ₃₁	Y ₃₂	Y ₃₃	Y ₃₄	Y ₃₅	Y ₃₆	Y ₃₇	Y ₃₈	Y ₃₉	Y ₄₀	Y ₄₁	Y ₄₂	Y ₄₃	Y ₄₄	Y ₄₅	Y ₄₆	Y ₄₇	Y ₄₈	Y ₄₉	Y ₅₀	Y ₅₁	Y ₅₂	Y ₅₃	Y ₅₄	Y ₅₅	Y ₅₆	Y ₅₇	Y ₅₈	Y ₅₉	Y ₆₀	Y ₆₁	Y ₆₂	Y ₆₃	Y ₆₄	Y ₆₅	Y ₆₆	Y ₆₇	Y ₆₈	Y ₆₉	Y ₇₀	Y ₇₁	Y ₇₂	Y ₇₃	Y ₇₄	Y ₇₅	Y ₇₆	Y ₇₇	Y ₇₈	Y ₇₉	Y ₈₀	Y ₈₁	Y ₈₂	Y ₈₃	Y ₈₄	Y ₈₅	Y ₈₆	Y ₈₇	Y ₈₈	Y ₈₉	Y ₉₀	Y ₉₁	Y ₉₂	Y ₉₃	Y ₉₄	Y ₉₅	Y ₉₆	Y ₉₇	Y ₉₈	Y ₉₉	Y ₁₀₀	Y ₁₀₁	Y ₁₀₂	Y ₁₀₃	Y ₁₀₄	Y ₁₀₅	Y ₁₀₆	Y ₁₀₇	Y ₁₀₈	Y ₁₀₉	Y ₁₁₀	Y ₁₁₁	Y ₁₁₂	Y ₁₁₃	Y ₁₁₄	Y ₁₁₅	Y ₁₁₆	Y ₁₁₇	Y ₁₁₈	Y ₁₁₉	Y ₁₂₀	Y ₁₂₁	Y ₁₂₂	Y ₁₂₃	Y ₁₂₄	Y ₁₂₅	Y ₁₂₆	Y ₁₂₇	Y ₁₂₈	Y ₁₂₉	Y ₁₃₀	Y ₁₃₁	Y ₁₃₂	Y ₁₃₃	Y ₁₃₄	Y ₁₃₅	Y ₁₃₆	Y ₁₃₇	Y ₁₃₈	Y ₁₃₉	Y ₁₄₀	Y ₁₄₁	Y ₁₄₂	Y ₁₄₃	Y ₁₄₄	Y ₁₄₅	Y ₁₄₆	Y ₁₄₇	Y ₁₄₈	Y ₁₄₉	Y ₁₅₀	Y ₁₅₁	Y ₁₅₂	Y ₁₅₃	Y ₁₅₄	Y ₁₅₅	Y ₁₅₆	Y ₁₅₇	Y ₁₅₈	Y ₁₅₉	Y ₁₆₀	Y ₁₆₁	Y ₁₆₂	Y ₁₆₃	Y ₁₆₄	Y ₁₆₅	Y ₁₆₆	Y ₁₆₇	Y ₁₆₈	Y ₁₆₉	Y ₁₇₀	Y ₁₇₁	Y ₁₇₂	Y ₁₇₃	Y ₁₇₄	Y ₁₇₅	Y ₁₇₆	Y ₁₇₇	Y ₁₇₈	Y ₁₇₉	Y ₁₈₀	Y ₁₈₁	Y ₁₈₂	Y ₁₈₃	Y ₁₈₄	Y ₁₈₅	Y ₁₈₆	Y ₁₈₇	Y ₁₈₈	Y ₁₈₉	Y ₁₉₀	Y ₁₉₁	Y ₁₉₂	Y ₁₉₃	Y ₁₉₄	Y ₁₉₅	Y ₁₉₆	Y ₁₉₇	Y ₁₉₈	Y ₁₉₉	Y ₂₀₀	Y ₂₀₁	Y ₂₀₂	Y ₂₀₃	Y ₂₀₄	Y ₂₀₅	Y ₂₀₆	Y ₂₀₇	Y ₂₀₈	Y ₂₀₉	Y ₂₁₀	Y ₂₁₁	Y ₂₁₂	Y ₂₁₃	Y ₂₁₄	Y ₂₁₅	Y ₂₁₆	Y ₂₁₇	Y ₂₁₈	Y ₂₁₉	Y ₂₂₀	Y ₂₂₁	Y ₂₂₂	Y ₂₂₃	Y ₂₂₄	Y ₂₂₅	Y ₂₂₆	Y ₂₂₇	Y ₂₂₈	Y ₂₂₉	Y ₂₃₀	Y ₂₃₁	Y ₂₃₂	Y ₂₃₃	Y ₂₃₄	Y ₂₃₅	Y ₂₃₆	Y ₂₃₇	Y ₂₃₈	Y ₂₃₉	Y ₂₄₀	Y ₂₄₁	Y ₂₄₂	Y ₂₄₃	Y ₂₄₄	Y ₂₄₅	Y ₂₄₆	Y ₂₄₇	Y ₂₄₈	Y ₂₄₉	Y ₂₅₀	Y ₂₅₁	Y ₂₅₂	Y ₂₅₃	Y ₂₅₄	Y ₂₅₅	Y ₂₅₆	Y ₂₅₇	Y ₂₅₈	Y ₂₅₉	Y ₂₆₀	Y ₂₆₁	Y ₂₆₂	Y ₂₆₃	Y ₂₆₄	Y ₂₆₅	Y ₂₆₆	Y ₂₆₇	Y ₂₆₈	Y ₂₆₉	Y ₂₇₀	Y ₂₇₁	Y ₂₇₂	Y ₂₇₃	Y ₂₇₄	Y ₂₇₅	Y ₂₇₆	Y ₂₇₇	Y ₂₇₈	Y ₂₇₉	Y ₂₈₀	Y ₂₈₁	Y ₂₈₂	Y ₂₈₃	Y ₂₈₄	Y ₂₈₅	Y ₂₈₆	Y ₂₈₇	Y ₂₈₈	Y ₂₈₉	Y ₂₉₀	Y ₂₉₁	Y ₂₉₂	Y ₂₉₃	Y ₂₉₄	Y ₂₉₅	Y ₂₉₆	Y ₂₉₇	Y ₂₉₈	Y ₂₉₉	Y ₃₀₀	Y ₃₀₁	Y ₃₀₂	Y ₃₀₃	Y ₃₀₄	Y ₃₀₅	Y ₃₀₆	Y ₃₀₇	Y ₃₀₈	Y ₃₀₉	Y ₃₁₀	Y ₃₁₁	Y ₃₁₂	Y ₃₁₃	Y ₃₁₄	Y ₃₁₅	Y ₃₁₆	Y ₃₁₇	Y ₃₁₈	Y ₃₁₉	Y ₃₂₀	Y ₃₂₁	Y ₃₂₂	Y ₃₂₃	Y ₃₂₄	Y ₃₂₅	Y ₃₂₆	Y ₃₂₇	Y ₃₂₈	Y ₃₂₉	Y ₃₃₀	Y ₃₃₁	Y ₃₃₂	Y ₃₃₃	Y ₃₃₄	Y ₃₃₅	Y ₃₃₆	Y ₃₃₇	Y ₃₃₈	Y ₃₃₉	Y ₃₄₀	Y ₃₄₁	Y ₃₄₂	Y ₃₄₃	Y ₃₄₄	Y ₃₄₅	Y ₃₄₆	Y ₃₄₇	Y ₃₄₈	Y ₃₄₉	Y ₃₅₀	Y ₃₅₁	Y ₃₅₂	Y ₃₅₃	Y ₃₅₄	Y ₃₅₅	Y ₃₅₆	Y ₃₅₇	Y ₃₅₈	Y ₃₅₉	Y ₃₆₀	Y ₃₆₁	Y ₃₆₂	Y ₃₆₃	Y ₃₆₄	Y ₃₆₅	Y ₃₆₆	Y ₃₆₇	Y ₃₆₈	Y ₃₆₉	Y ₃₇₀	Y ₃₇₁	Y ₃₇₂	Y ₃₇₃	Y ₃₇₄	Y ₃₇₅	Y ₃₇₆	Y ₃₇₇	Y ₃₇₈	Y ₃₇₉	Y ₃₈₀	Y ₃₈₁	Y ₃₈₂	Y ₃₈₃	Y ₃₈₄	Y ₃₈₅	Y ₃₈₆	Y ₃₈₇	Y ₃₈₈	Y ₃₈₉	Y ₃₉₀	Y ₃₉₁	Y ₃₉₂	Y ₃₉₃	Y ₃₉₄	Y ₃₉₅	Y ₃₉₆	Y ₃₉₇	Y ₃₉₈	Y ₃₉₉	Y ₄₀₀	Y ₄₀₁	Y ₄₀₂	Y ₄₀₃	Y ₄₀₄	Y ₄₀₅	Y ₄₀₆	Y ₄₀₇	Y ₄₀₈	Y ₄₀₉	Y ₄₁₀	Y ₄₁₁	Y ₄₁₂	Y ₄₁₃	Y ₄₁₄	Y ₄₁₅	Y ₄₁₆	Y ₄₁₇	Y ₄₁₈	Y ₄₁₉	Y ₄₂₀	Y ₄₂₁	Y ₄₂₂	Y ₄₂₃	Y ₄₂₄	Y ₄₂₅	Y ₄₂₆	Y ₄₂₇	Y ₄₂₈	Y ₄₂₉	Y ₄₃₀	Y ₄₃₁	Y ₄₃₂	Y ₄₃₃	Y ₄₃₄	Y ₄₃₅	Y ₄₃₆	Y ₄₃₇	Y ₄₃₈	Y ₄₃₉	Y ₄₄₀	Y ₄₄₁	Y ₄₄₂	Y ₄₄₃	Y ₄₄₄	Y ₄₄₅	Y ₄₄₆	Y ₄₄₇	Y ₄₄₈	Y ₄₄₉	Y ₄₅₀	Y ₄₅₁	Y ₄₅₂	Y ₄₅₃	Y ₄₅₄	Y ₄₅₅	Y ₄₅₆	Y ₄₅₇	Y ₄₅₈	Y ₄₅₉	Y ₄₆₀	Y ₄₆₁	Y ₄₆₂	Y ₄₆₃	Y ₄₆₄	Y ₄₆₅	Y ₄₆₆	Y ₄₆₇	Y ₄₆₈	Y ₄₆₉	Y ₄₇₀	Y ₄₇₁	Y ₄₇₂	Y ₄₇₃	Y ₄₇₄	Y ₄₇₅	Y ₄₇₆	Y ₄₇₇	Y ₄₇₈	Y ₄₇₉	Y ₄₈₀	Y ₄₈₁	Y ₄₈₂	Y ₄₈₃	Y ₄₈₄	Y ₄₈₅	Y ₄₈₆	Y ₄₈₇	Y ₄₈₈	Y ₄₈₉	Y ₄₉₀	Y ₄₉₁	Y ₄₉₂	Y ₄₉₃	Y ₄₉₄	Y ₄₉₅	Y ₄₉₆	Y ₄₉₇	Y ₄₉₈	Y ₄₉₉	Y ₅₀₀	Y ₅₀₁	Y ₅₀₂	Y ₅₀₃	Y ₅₀₄	Y ₅₀₅	Y ₅₀₆	Y ₅₀₇	Y ₅₀₈	Y ₅₀₉	Y ₅₁₀	Y ₅₁₁	Y ₅₁₂	Y ₅₁₃	Y ₅₁₄	Y ₅₁₅	Y ₅₁₆	Y ₅₁₇	Y ₅₁₈	Y ₅₁₉	Y ₅₂₀	Y ₅₂₁	Y ₅₂₂	Y ₅₂₃	Y ₅₂₄	Y ₅₂₅	Y ₅₂₆	Y ₅₂₇	Y ₅₂₈	Y ₅₂₉	Y ₅₃₀	Y ₅₃₁	Y ₅₃₂	Y ₅₃₃	Y ₅₃₄	Y ₅₃₅	Y ₅₃₆	Y ₅₃₇	Y ₅₃₈	Y ₅₃₉	Y ₅₄₀	Y ₅₄₁	Y ₅₄₂	Y ₅₄₃	Y ₅₄₄	Y ₅₄₅	Y ₅₄₆	Y ₅₄₇	Y ₅₄₈	Y ₅₄₉	Y ₅₅₀	Y ₅₅₁	Y ₅₅₂	Y ₅₅₃	Y ₅₅₄	Y ₅₅₅	Y ₅₅₆	Y ₅₅₇	Y ₅₅₈	Y ₅₅₉	Y ₅₆₀	Y ₅₆₁	Y ₅₆₂	Y ₅₆₃	Y ₅₆₄	Y ₅₆₅	Y ₅₆₆	Y ₅₆₇	Y ₅₆₈	Y ₅₆₉	Y ₅₇₀	Y ₅₇₁	Y ₅₇₂	Y ₅₇₃	Y ₅₇₄	Y ₅₇₅	Y ₅₇₆	Y ₅₇₇	Y ₅₇₈	Y ₅₇₉	Y ₅₈₀	Y ₅₈₁	Y ₅₈₂	Y ₅₈₃	Y ₅₈₄	Y ₅₈₅	Y ₅₈₆	Y ₅₈₇	Y ₅₈₈	Y ₅₈₉	Y ₅₉₀	Y ₅₉₁	Y ₅₉₂	Y ₅₉₃	Y ₅₉₄	Y ₅₉₅	Y ₅₉₆	Y ₅₉₇	Y ₅₉₈	Y ₅₉₉	Y ₆₀₀	Y ₆₀₁	Y ₆₀₂	Y ₆₀₃	Y ₆₀₄	Y ₆₀₅	Y ₆₀₆	Y ₆₀₇	Y ₆₀₈	Y ₆₀₉	Y ₆₁₀	Y ₆₁₁	Y ₆₁₂	Y ₆₁₃	Y ₆₁₄	Y ₆₁₅	Y ₆₁₆	Y ₆₁₇	Y ₆₁₈	Y ₆₁₉	Y ₆₂₀	Y ₆₂₁	Y ₆₂₂	Y ₆₂₃	Y ₆₂₄	Y ₆₂₅	Y ₆₂₆	Y ₆₂₇	Y ₆₂₈	Y ₆₂₉	Y ₆₃₀	Y ₆₃₁	Y ₆₃₂	Y ₆₃₃	Y ₆₃₄	Y ₆₃₅	Y ₆₃₆	Y ₆₃₇	Y ₆₃₈	Y ₆₃₉	Y ₆₄₀	Y ₆₄₁	Y ₆₄₂	Y ₆₄₃	Y ₆₄₄	Y ₆₄₅	Y ₆₄₆	Y ₆₄₇	Y ₆₄₈	Y ₆₄₉	Y ₆₅₀	Y ₆₅₁	Y ₆₅₂	Y ₆₅₃	Y ₆₅₄	Y ₆₅₅	Y ₆₅₆	Y ₆₅₇	Y ₆₅₈	Y ₆₅₉	Y ₆₆₀	Y ₆₆₁	Y ₆₆₂	Y ₆₆₃	Y ₆₆₄	Y ₆₆₅	Y ₆₆₆	Y ₆₆₇	Y ₆₆₈	Y ₆₆₉	Y ₆₇₀	Y ₆₇₁	Y ₆₇₂	Y ₆₇₃	Y ₆₇₄	Y ₆₇₅	Y ₆₇₆	Y ₆₇₇	Y ₆₇₈	Y ₆₇₉	Y ₆₈₀	Y ₆₈₁	Y ₆₈₂	Y ₆₈₃	Y ₆₈₄	Y ₆₈₅	Y ₆₈₆	Y ₆₈₇	Y ₆₈₈	Y ₆₈₉	Y ₆₉₀	Y ₆₉₁	Y ₆₉₂	Y ₆₉₃	Y ₆₉₄	Y ₆₉₅	Y ₆₉₆	Y ₆₉₇	Y ₆₉₈	Y ₆₉₉	Y ₇₀₀	Y ₇₀₁	Y ₇₀₂	Y ₇₀₃	Y ₇₀₄	Y ₇₀₅	Y ₇₀₆	Y ₇₀₇	Y ₇₀₈	Y ₇₀₉	Y ₇₁₀	Y ₇₁₁	Y ₇₁₂	Y ₇₁₃	Y ₇₁₄	Y ₇₁₅	Y ₇₁₆	Y ₇₁₇	Y ₇₁₈	Y ₇₁₉	Y ₇₂₀	Y ₇₂₁	Y ₇₂₂	Y ₇₂₃	Y ₇₂₄	Y ₇₂₅	Y ₇₂₆	Y ₇₂₇	Y ₇₂₈	Y ₇₂₉	Y ₇₃₀	Y ₇₃₁	Y ₇₃₂	Y ₇₃₃	Y ₇₃₄	Y ₇₃₅	Y ₇₃₆	Y ₇₃₇	Y ₇₃₈	Y ₇₃₉	Y ₇₄₀	Y ₇₄₁	Y ₇₄₂	Y ₇₄₃	Y ₇₄₄	Y ₇₄₅	Y ₇₄₆	Y ₇₄₇	Y ₇₄₈	Y ₇₄₉	Y ₇₅₀	Y ₇₅₁	Y ₇₅₂	Y ₇₅₃	Y ₇₅₄	Y ₇₅₅	Y ₇₅₆	Y ₇₅₇	Y ₇₅₈	Y ₇₅₉	Y ₇₆₀	Y ₇₆₁	Y ₇₆₂	Y ₇₆₃	Y ₇₆₄	Y ₇₆₅	Y ₇₆₆	Y ₇₆₇	Y ₇₆₈	Y ₇₆₉	Y ₇₇₀	Y ₇₇₁	Y ₇₇₂	Y ₇₇₃	Y ₇₇₄	Y ₇₇₅	Y ₇₇₆	Y ₇₇₇	Y ₇₇₈	Y ₇₇₉	Y ₇₈₀	Y ₇₈₁	Y ₇₈₂	Y ₇₈₃	Y ₇₈₄	Y ₇₈₅	Y ₇₈₆	Y ₇₈₇	Y ₇₈₈	Y ₇₈₉	Y ₇₉₀	Y ₇₉₁	Y ₇₉₂	Y ₇₉₃	Y ₇₉₄	Y ₇₉₅	Y ₇₉₆	Y ₇₉₇	Y ₇₉₈	Y ₇₉₉	Y ₈₀₀	Y ₈₀₁	Y ₈₀₂	Y ₈₀₃	Y ₈₀₄	Y ₈₀₅	Y ₈₀₆	Y ₈₀₇	Y ₈₀₈	Y ₈₀₉	Y ₈₁₀	Y ₈₁₁	Y ₈₁₂	Y ₈₁₃	Y ₈₁₄	Y ₈₁₅	Y ₈₁₆	Y ₈₁₇	Y ₈₁₈	Y ₈₁₉	Y ₈₂₀	Y ₈₂₁	Y ₈₂₂	Y ₈₂₃	Y ₈₂₄	Y ₈₂₅	Y ₈₂₆	Y ₈₂₇	Y ₈₂₈	Y ₈₂₉	Y ₈₃₀	Y ₈₃₁	Y ₈₃₂	Y ₈₃₃	Y ₈₃₄	Y ₈₃₅	Y ₈₃₆	Y ₈₃₇	Y ₈₃₈	Y ₈₃₉	Y ₈₄₀	Y ₈₄₁	Y ₈₄₂	Y ₈₄₃	Y ₈₄₄	Y ₈₄₅	Y ₈₄₆	Y ₈₄₇	Y ₈₄₈	Y ₈₄₉	Y ₈₅₀	Y ₈₅₁	Y ₈₅₂	Y ₈₅₃	Y ₈₅₄	Y ₈₅₅	Y ₈₅₆	Y ₈₅₇	Y ₈₅₈	Y ₈₅₉	Y ₈₆₀	Y ₈₆₁	Y ₈₆₂	Y ₈₆₃	Y ₈₆₄	Y ₈₆₅	Y ₈₆₆	Y ₈₆₇	Y ₈₆₈	Y ₈₆₉	Y ₈₇₀	Y ₈₇₁	Y ₈₇₂	Y ₈₇₃	Y ₈₇₄	Y ₈₇₅	Y ₈₇₆	Y ₈₇₇	Y ₈₇₈	Y ₈₇₉	Y ₈₈₀	Y ₈₈₁	Y ₈₈₂	Y ₈₈₃	Y ₈₈₄	Y ₈₈₅	Y ₈₈₆	Y ₈₈₇	Y ₈₈₈	Y ₈₈₉	Y ₈₉₀	Y ₈₉₁	
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INSTRUCTIONS IN THE 32 x 9 ROM - POSITIVE LOGIC (1 = H $\approx$ 3 V) INTERPRETATION

CONDITION	SELECT	CONDITION 0	CONDITION 1
0	0 0 0 0	-TRANSMITTER DONE	TIMER
1	0 0 0 1	-BUS READY	-BUS ERROR
2	0 0 1 0	-BUS TIME OUT	-DATA P. OK
3	0 0 1 1	REQUEST	ATTENTION
4	0 1 0 0	RECEIVER DONE	PARITY ERROR IN MEDIUM
5	0 1 0 1	RECEIVE BLOCK END	-INITIATE
6	0 1 1 0	-START	-RESET
7	0 1 1 1	SENSE	SUB. DEV. SELECTOR
8	1 0 0 0	INTERN BUS 13	INTERN BUS 15
9	1 0 0 1	INTERN BUS 14	F = 0
10	1 0 1 0	TIMER STATUS	INTERN BUS 16
11	1 0 1 1		TRANSMIT BLOCK END
12	1 1 0 0	INTERN BUS 22	INTERN BUS 23
13	1 1 0 1	WAIT	
14	1 1 1 0		
15	1 1 1 1	NEXT CONDITION 0	NEXT CONDITION 1

FPA 801 COMMANDS.

COMMAND FIELD				CON-TINUE BIT 16	CHANNEL COMMAND WORD 1	FIRST WORD ADDRESS WORD 2	CHARACTER COUNT WORD 3
12	13	14	15				
X	0	0	0	X	SENSE	FIRST WORD ADDR	X
X	0	0	1	D	READ	FIRST WORD ADDR	CHAR COUNT
X	0	1	1	D	WRITE	FIRST WORD ADDR	CHAR COUNT
X	1	0	0	X	WAIT	X	X
X	1	1	0	X	CONTROL	X	X
X	1	1	1	X	STOP	X	X

X denotes parameters or bits not used.

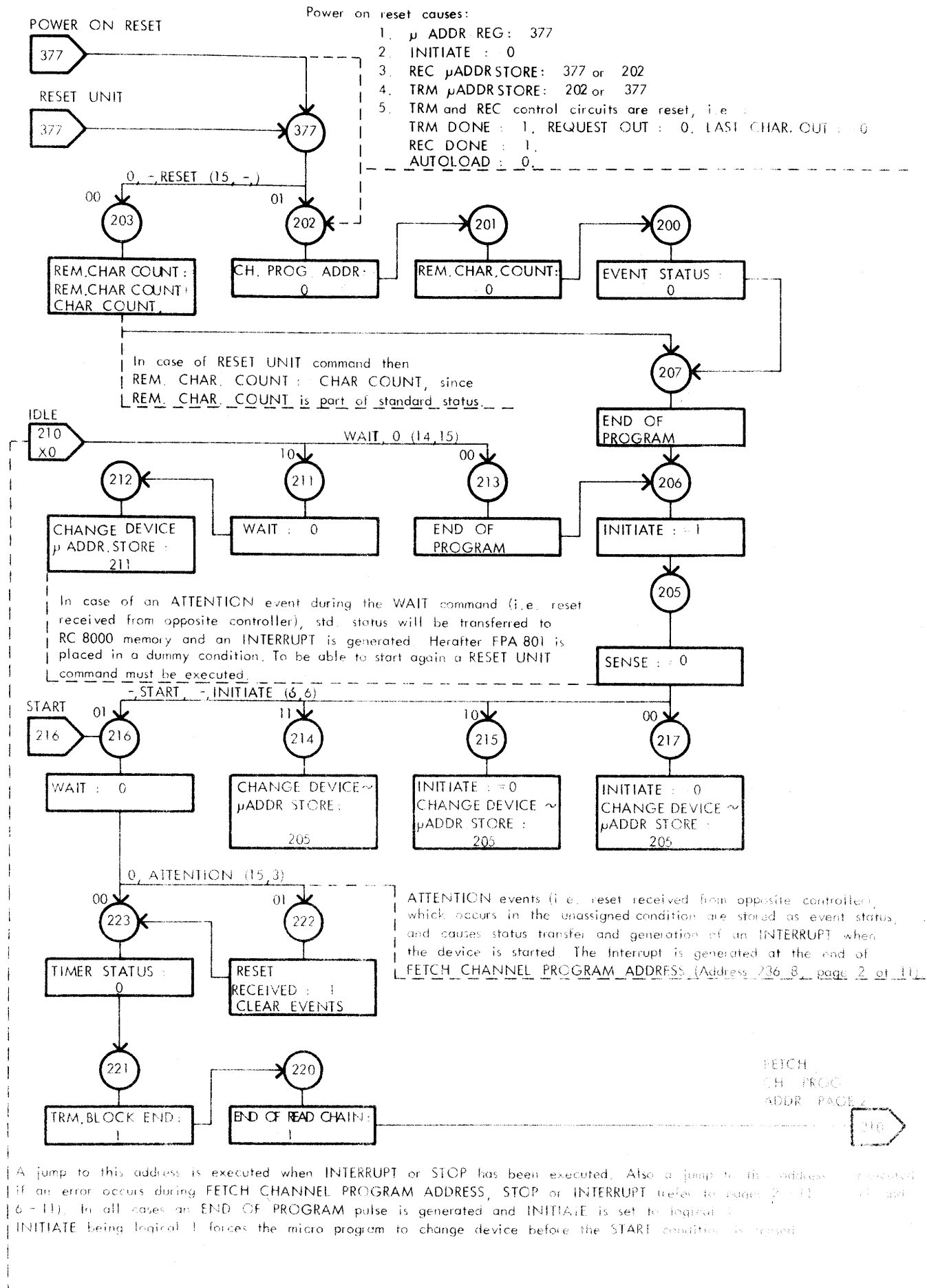
FPA 801 EVENT STATUS.

BIT	RECEIVER INTERPRETATION	TRANSMITTER INTERPRETATION
0	RESET RECEIVED	X
1	PARITY ERROR IN MEDIUM	PARITY ERROR IN MEDIUM
2	TIME - OUT	TIME - OUT
4	BLOCK LENGTH ERROR	BLOCK LENGTH ERROR
20	BUS PARITY ERROR	BUS PARITY ERROR
21	STATUS TRANSFER ERROR	STATUS TRANSFER ERROR
22	BUS TIME OUT	BUS TIME OUT
23	BUS COMMUNICATION ERROR	BUS COMMUNICATION ERROR

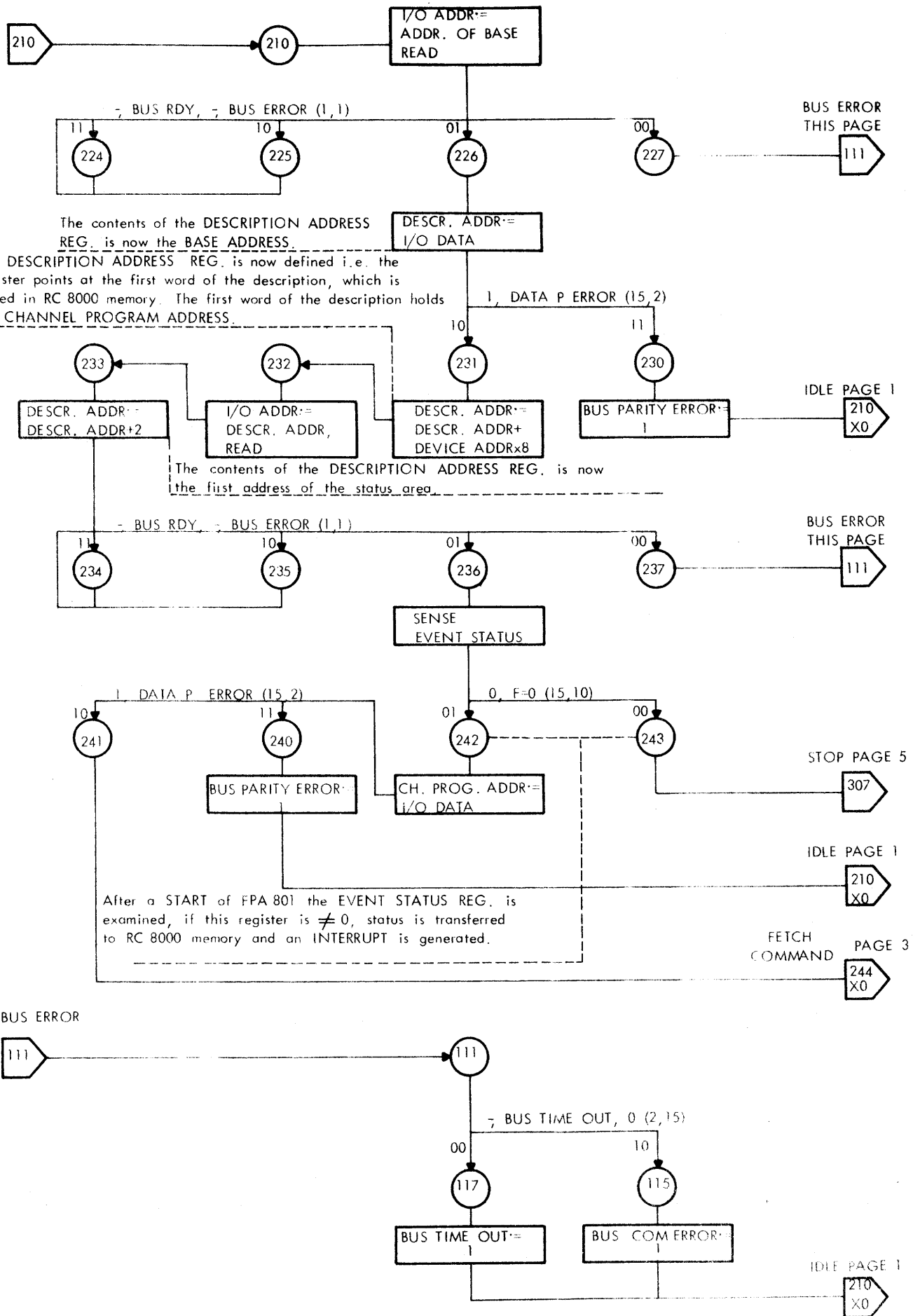
FPA 801 CURRENT STATUS.

BIT	RECEIVER INTERPRETATION	TRANSMITTER INTERPRETATION
0	FRONT END DISCONNECTED	FRONT END DISCONNECTED
21	DEVICE KIND = 0	DEVICE KIND = 1
23	BLOCK ORIENTATED = 1	BLOCK ORIENTATED = 1

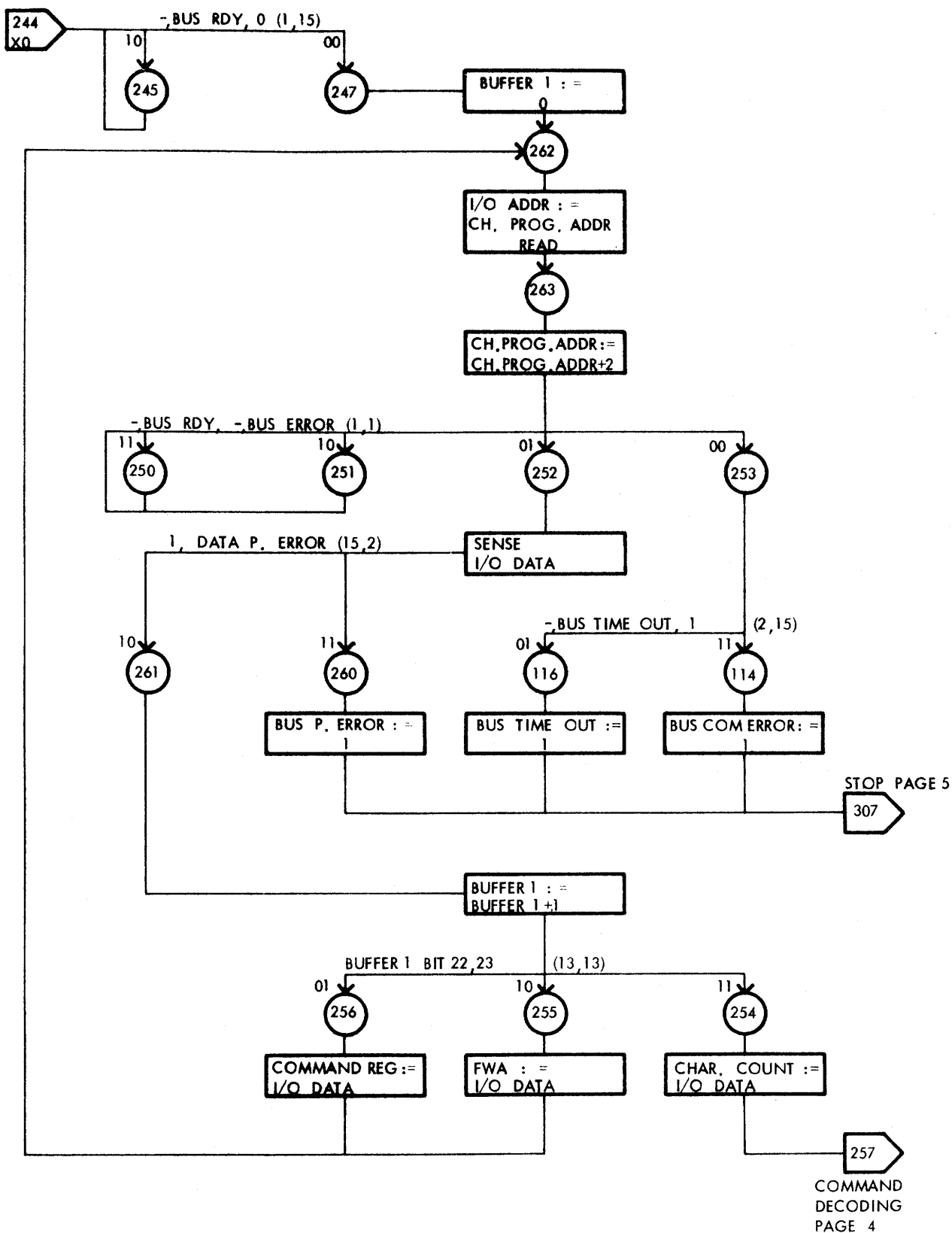
remaining bits are always zero.



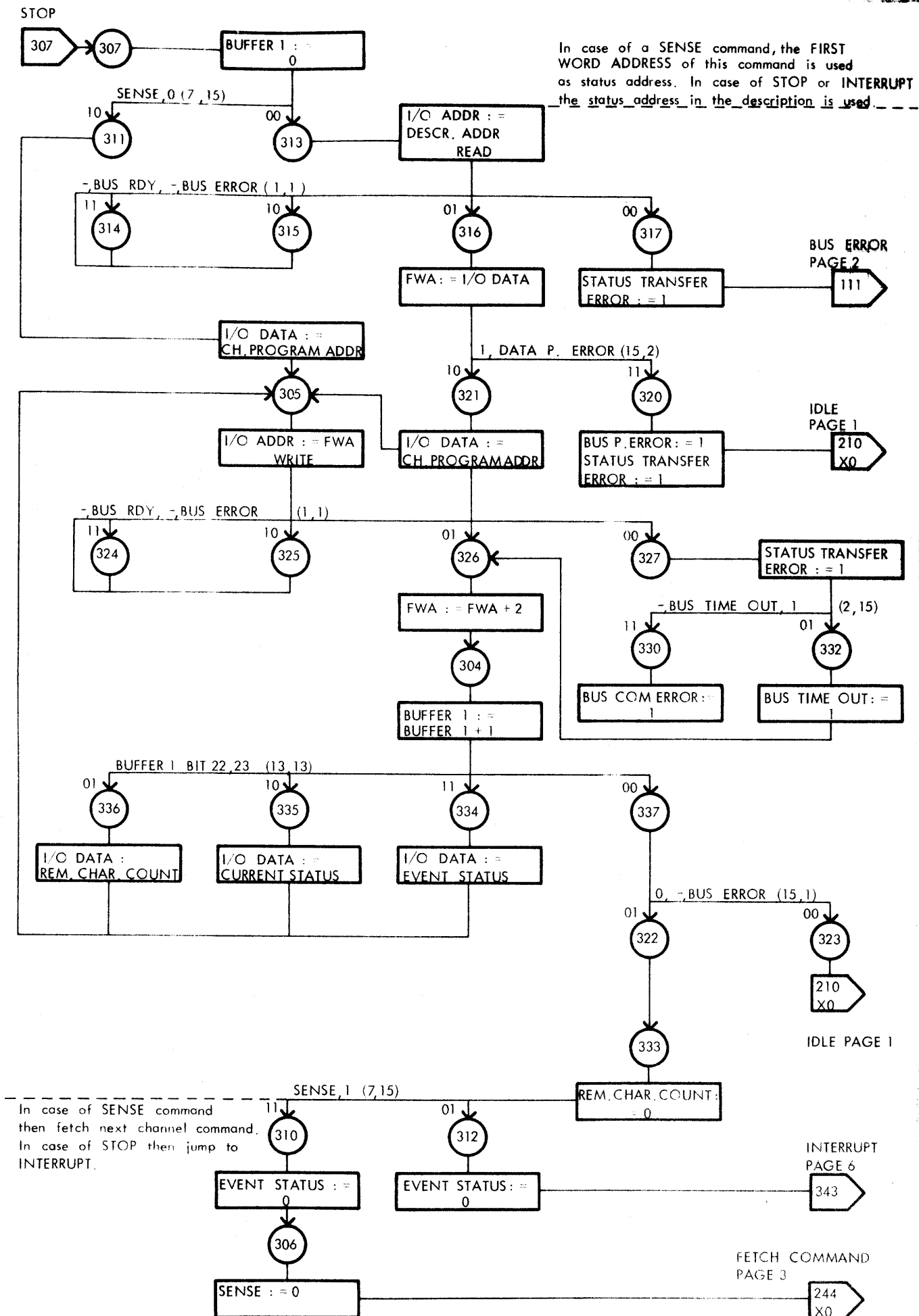
FETCH CHANNEL PROGRAM ADDRESS



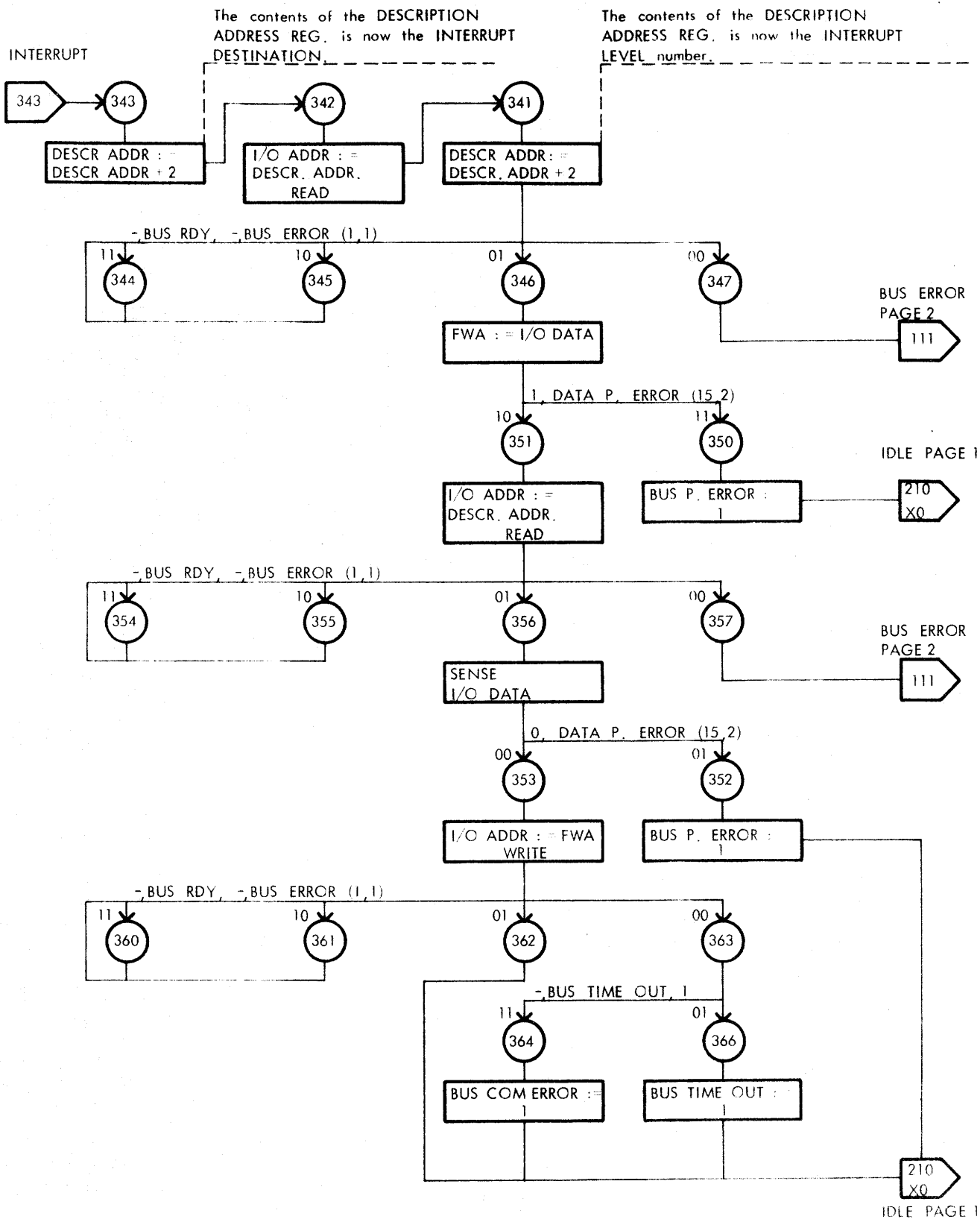
FETCH COMMAND



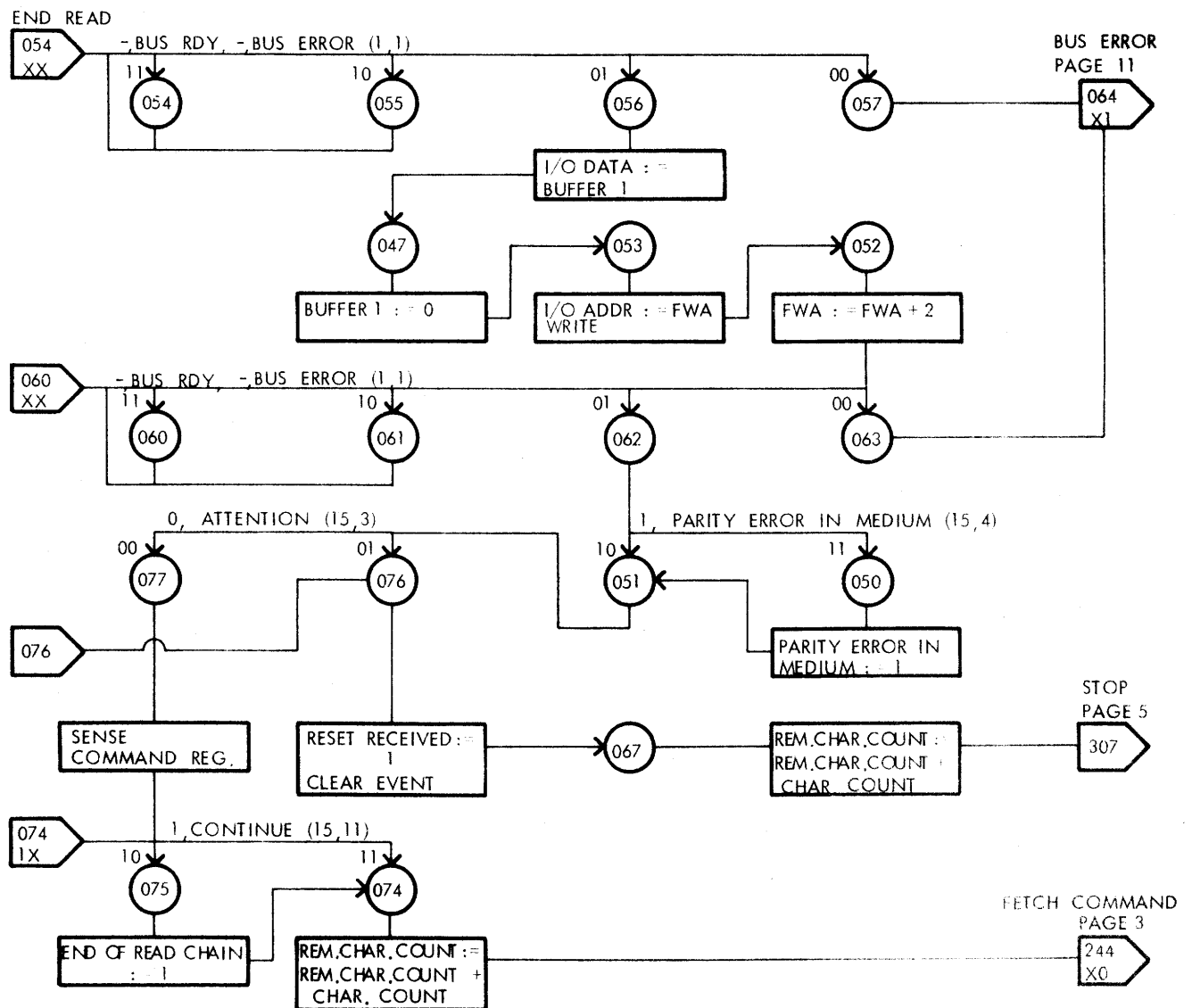
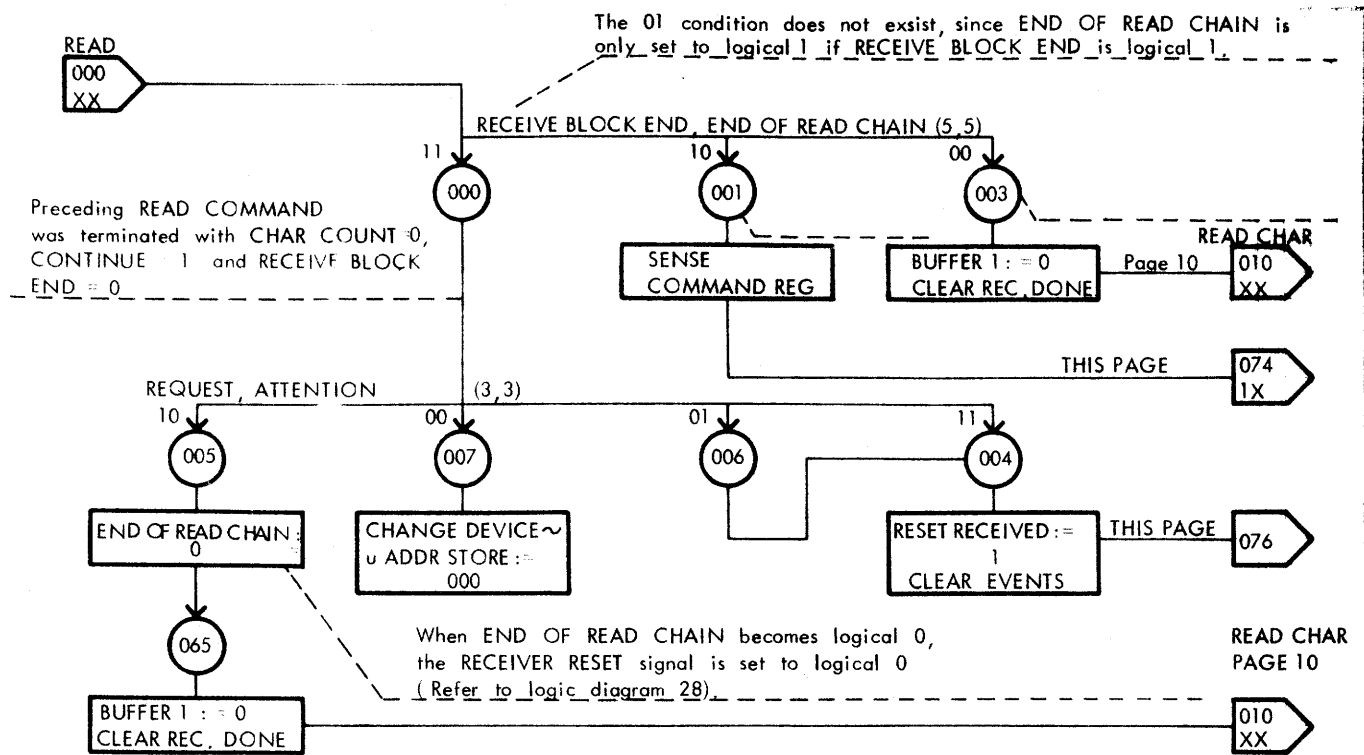
760130 VH, 770331 AMS, 770412 LLM, 770412 VH.



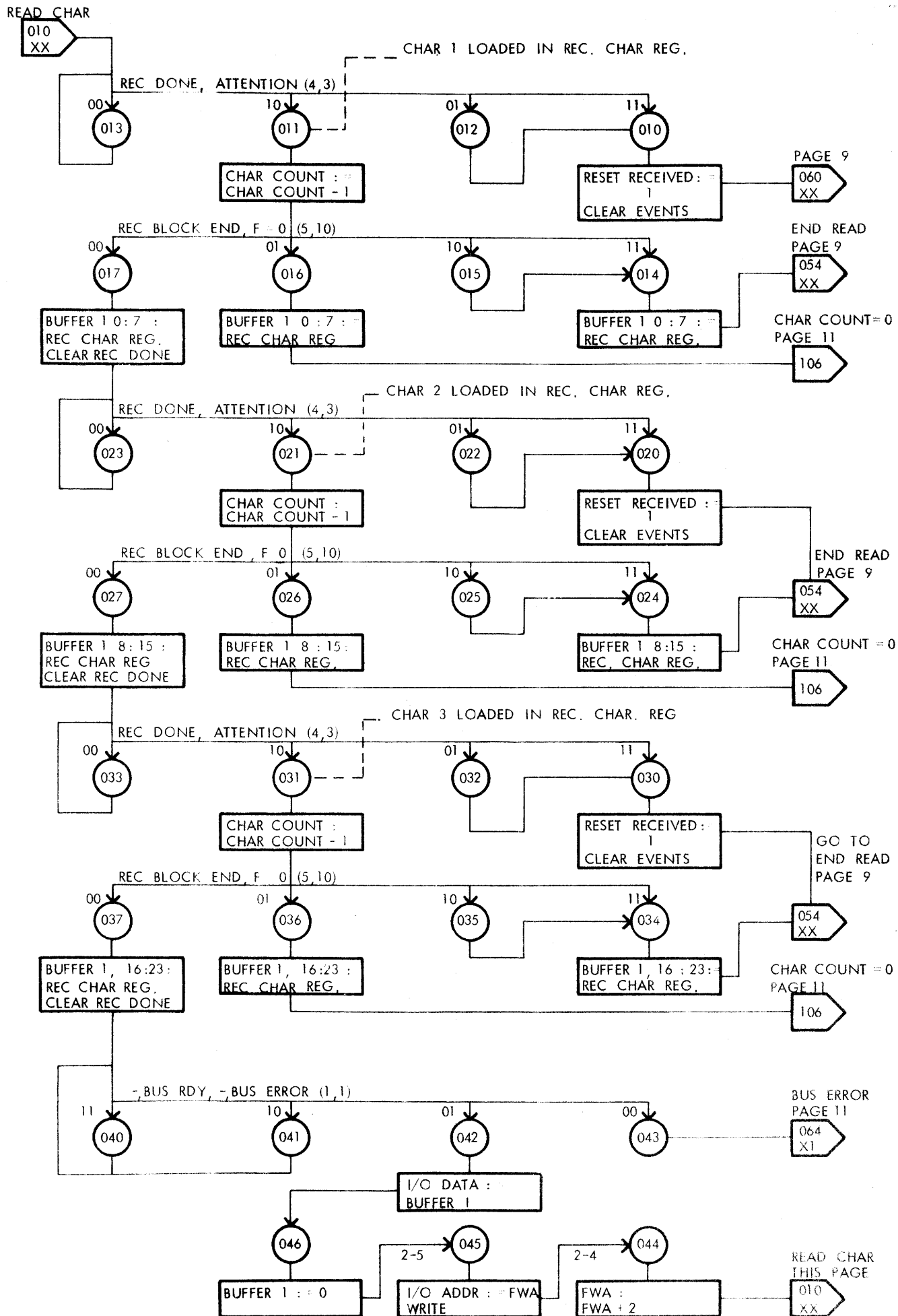
7751020 VH. 770406 AMS. 770412 LLM. 770412 VH.



7760203 VH, 770420 AMS, 770425 LLM 770425 VH

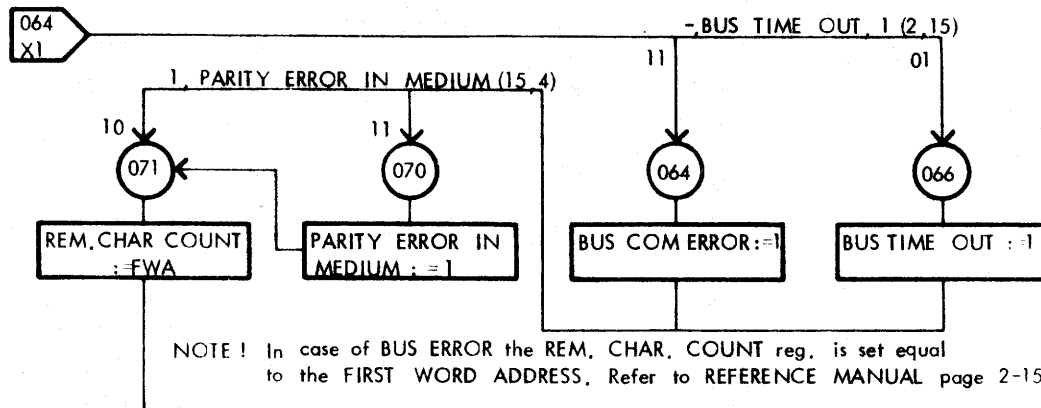


751015 VH, 770425 AMS, 770527 OKJ 770527 VH



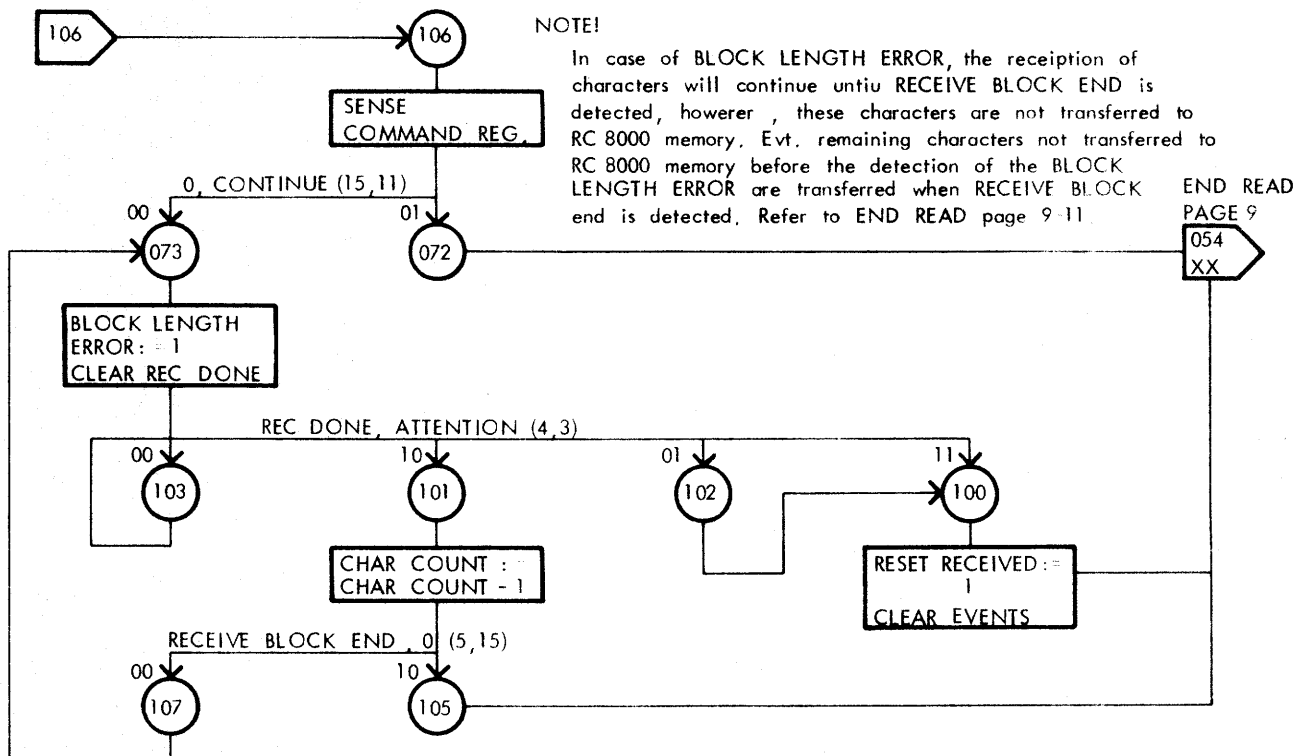
750919 VH. 770420 AMS. 770425 LLM 770425 VH

BUS ERROR



STOP PAGE 5

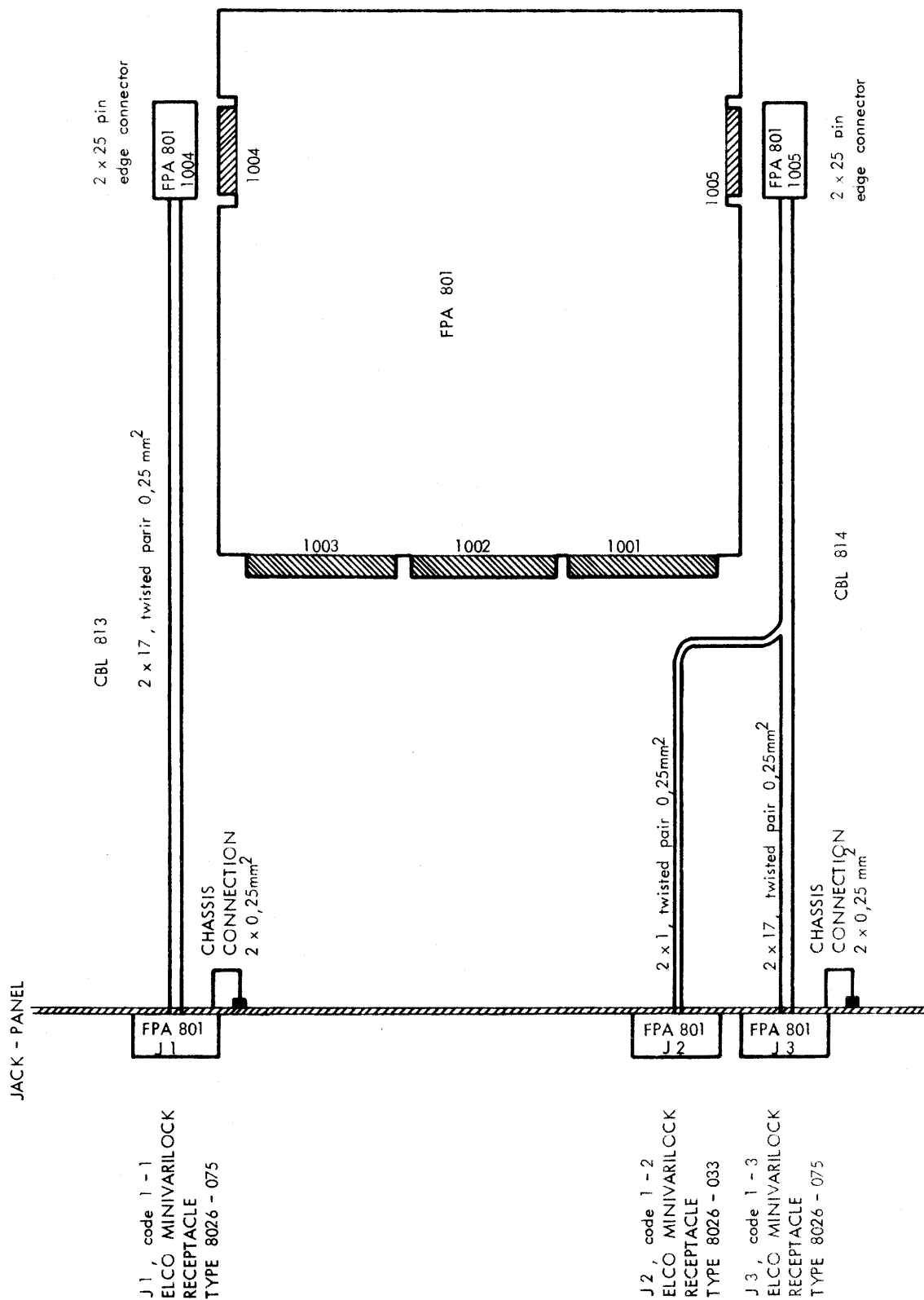
CHAR COUNT = 0



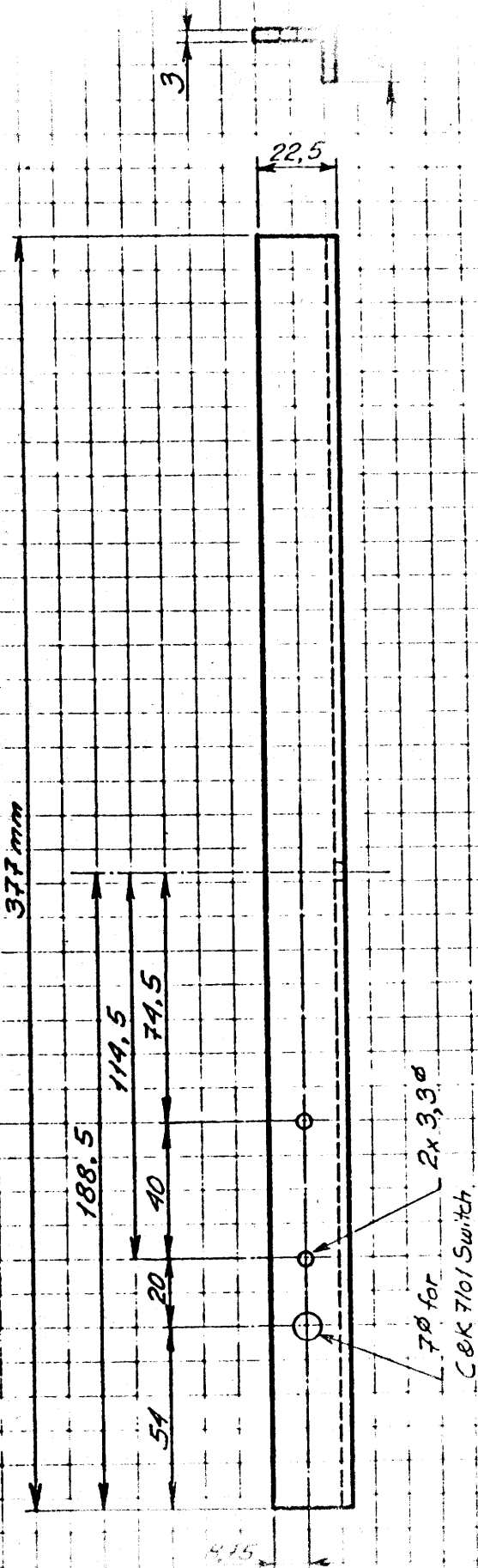
751015 VH. 770420 AMS. 770425 LLM 770425 VH

751021 VH. 770420 AMS. 770425 LLM 770425 VH

FPA 801
A12885



ASSEMBLY DRAWING



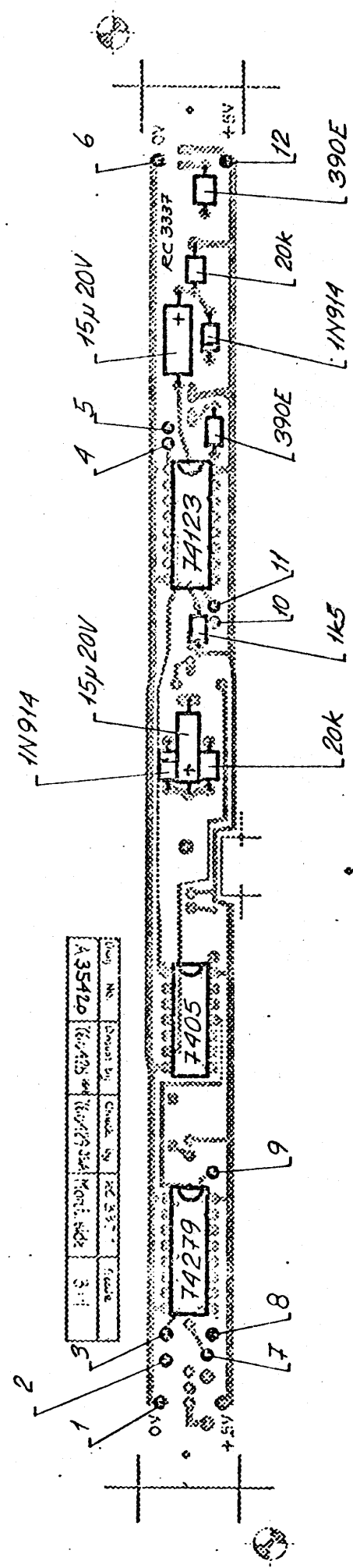
Alle mål i mm.

760505 VH 760901 IGH.

A24523

ALLE MODSTANDE 1/20 W

MONTERINGSTEGNING



MONTERINGSIDEN.

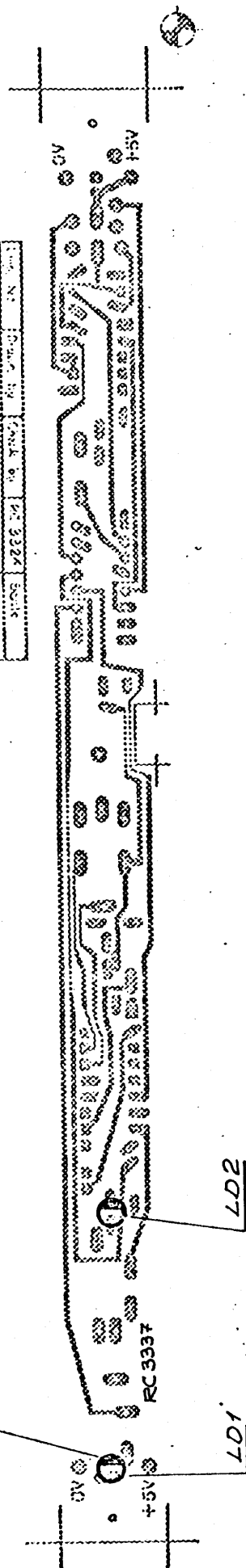
RC 3337
p 1 of 2.

760505 VH 760901 7644

A 24518

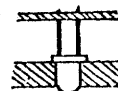
ALLE L4SDIØDER HAR
KATODEN TIL HØJRE

Line No.	Drawn by	Check by	Rev	Scale
135421	W. A. 125	W. A. 125	135421	3:1



LODDESIDE

L4SDIØDER. LODDES IKKE
FØR DE ER MONTERET I
FORPLADE VINKELEN.



MONTERINGSTEGNING

RC 3337
p 2 of 2.

A/S REGNECENTRALEN	Designed by	VH	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.
	2/12 - 76							

Unit

FPA 801

Dwg. No.

A24748

PLUG 1001

ON PRINTED CIRCUIT BOARD

PLUG 1001 A	SIGNAL	PLUG 1001 B	SIGNAL	PLUG 1001 C	SIGNAL
1	+5V	1	+5V	1	+5V
2	0V	2	7BSEL 0 in	2	7BREQ 0
3	0V	3	7BSEL 0 out	3	7BREQ 1
4	0V	4	7BSEL 1 in	4	7CSEL
5	0V	5	7BSEL 1 out	5	7SACK
6	0V	6	7SYS RESET	6	7IATA OUT
7	0V	7	7IATA RDY	7	7BBSY
8	0V	8	7ACK	8	7OK
9	0V	9	7NACK	9	7PINT
10	0V	10	7ADDR (0)	10	7ADDR (1)
11	0V	11	- (2)	11	- (3)
12	0V	12	- (4)	12	- (5)
13	0V	13	- (6)	13	- (7)
14	0V	14	- (8)	14	- (9)
15	0V	15	- (10)	15	- (11)
16	0V	16	- (12)	16	- (13)
17	0V	17	- (14)	17	- (15)
18	0V	18	- (16)	18	- (17)
19	0V	19	- (18)	19	- (19)
20	0V	20	- (20)	20	7ADDR (21)
21	0V	21	7ADDR (22)	21	7ADDR PAR
22	0V	22	7IATA (0)	22	7IATA (1)
23	0V	23	- (2)	23	- (3)
24	0V	24	- (4)	24	- (5)
25	0V	25	- (6)	25	- (7)
26	0V	26	- (8)	26	- (9)
27	0V	27	- (10)	27	- (11)
28	0V	28	- (12)	28	- (13)
29	0V	29	- (14)	29	- (15)
30	0V	30	7DATA (16)	30	7IATA (17)
31	Spec. voltage	31	Spec voltage	31	Spec. voltage
32	+5V	32	+5V	32	+5V

A/S REGNECENTRALEN		Designed by	VH	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	due to ECN	Replaced by Dwg. No.
		2/12 - 76							
PLUG 1002 A	SIGNAL	PLUG 1002 B	SIGNAL	PLUG 1002 C	SIGNAL				
1	+5V	1	+5V	1	+5V				
2	0V	2	0V	2	7 DATA (18)	2	7 DATA (19)		
3	0V	3	0V	3	- (20)	3	- (21)		
4	0V	4	0V	4	7 DATA (22)	4	7 DATA (23)		
5	0V	5	0V	5	7 DATA PAR (0)	5	7 DATA PAR (1)		
6	0V	6	0V	6	7 DATA PAR (2)	6			
7	0V	7	0V	7		7			
8	0V	8	0V	8		8			
9	0V	9	0V	9		9			
10	0V	10	0V	10		10			
11	0V	11	0V	11		11			
12	0V	12	0V	12		12			
13	0V	13	0V	13		13			
14	0V	14	0V	14		14			
15	0V	15	0V	15		15			
16	0V	16	0V	16		16			
17	0V	17	0V	17		17			
18	0V	18	0V	18		18			
19	0V	19	0V	19		19			
20	0V	20	0V	20		20			
21	0V	21	0V	21		21			
22	0V	22	0V	22		22			
23	0V	23	0V	23		23			
24	0V	24	0V	24		24			
25	0V	25	0V	25		25			
26	0V	26	0V	26		26			
27	0V	27	0V	27		27			
28	0V	28	0V	28		28			
29	0V	29	0V	29		29			
30	0V	30	0V	30		30			
31	Spec. Voltage +5V	31	Spec. Voltage +5V	31	Spec. Voltage +5V	31	Spec Voltage +5V		
32		32		32		32			

Unit
FPA 801

Dwg. No.
A24777

PLUG 1002
ON PRINTED CIRCUIT BOARD

A/S REGNECENTRALEN	Designed by	VH	Drawn by		Dwg. Office Check		Design Check		Replaces Dwg. No.		due to ECN		Replaced by Dwg. No.	
	1/12 - 76													

PLUG 1004 A	SIGNAL	PLUG 1004 B	SIGNAL
1	DATA LINE 0 OUT A	1	DATA LINE 0 OUT B
2	- 1 -	2	- 1 -
3	- 2 -	3	- 2 -
4	- 3 -	4	- 3 -
5	- 4 -	5	- 4 -
6	- 5 -	6	- 5 -
7	- 6 -	7	- 6 -
8	- 7 -	8	- 7 -
9	PARITY LINE OUT A	9	PARITY LINE OUT B
10	RESET LINE OUT A	10	RESET LINE OUT B
11	REQ ACK LINE IN A	11	REQ ACK LINE IN B
12	DATA REQ LINE OUT A	12	DATA REQ LINE OUT B
13	STATUS REQ LINE OUT A	13	STATUS REQ LINE OUT B
14	AUTOLOAD LINE OUT A	14	AUTOLOAD LINE OUT B
15	CONN. LINE OUT A	15	CONN. LINE OUT B
16	LAST CHAR. LINE OUT A	16	LAST CHAR. LINE OUT B
17	OV	17	OV
18		18	
19		19	
20		20	
21		21	
22		22	
23		23	
24		24	
25		25	

Unit
FPA 801

Dwg. No.

A24150

PLUG 1004
on PRINTED CIRCUIT BOARD

A/S REGNECENTRALEN

Designed by VH

Drawn by

Dwg. Office Check

Design Check

Replaces Dwg. No.

due to ECN

Replaced by Dwg. No.

'112-76

Unit

FPA 801

Dwg. No.

124151

PLUG 1005 A	SIGNAL	PLUG 1005 B	SIGNAL
1	DATA LINE 0 IN A	1	DATA LINE 0 IN B
2	- 1 -	2	- 1 -
3	- 2 -	3	- 2 -
4	- 3 -	4	- 3 -
5	- 4 -	5	- 4 -
6	- 5 -	6	- 5 -
7	- 6 -	7	- 6 -
8	- 7 -	8	- 7 -
9	PARITY LINE IN A	9	PARITY LINE IN B
10	RESET LINE IN A	10	RESET LINE IN B
11	REQ ACK LINE OUT A	11	REQ ACK LINE OUT B
12	DATA REQ LINE IN A	12	DATA REQ LINE IN B
13	STATUS REQ LINE IN A	13	STATUS REQ LINE IN B
14	AUTOLOAD LINE IN A	14	AUTOLOAD LINE IN B
15	CONN. LINE IN A	15	CONN. LINE IN B
16	LAST CHAR LINE IN A	16	LAST CHAR. LINE IN B
17	OV	17	OV
18		18	
19		19	
20		20	
21		21	
22		22	
23		23	
24		24	
25	REMOTE AUTOLOAD	25	OV

PLUG 1005
ON PRINTED CIRCUIT BOARD

STYKLISTE

Printplade umonteret RC 2301	1	
Forpladevinkel for FPA 801	1	
Skrue 3mm US, 8mm lang	3	
Fjerskive 3mm	3	
Møtrik 3mm	5	
Medbringertap	2	
Mini wire wrap pin	stk 3200	44913
Wirewrap tråd, AGW 30, rød	m 280	44910
Kondensator, keramisk, 47nF/12V	45	43911
Kondensator, tantal, 22uF/15V	3	11118
Kondensator, tantal, 68uF/15V	2	11119
Europa stik, plug 3*32 ben Elco 8237-096-000-053	3	46915
IC SU 7400 N	2	
IC SU 7402 N	1	
IC SU 7410 N	1	
IC SU 7437 N	1	
IC SU 7474 N	1	
IC SU 7492 AN	1	
IC SU 74109 N	2	
IC SU 74120 N	3	
IC SU 74150 N	2	
IC SU 74170 N	2	
IC SU 74273 N	5	
IC SU 74279 N	1	
IC SU 74298 N	11	
IC. SU 74393 N	1	

UDGAVE

21/2-76

NAVN FRONT-END PROCESSOR

NR.

FPA 801

BLAD

14

STYKLISTE

IC	SN 75138 N	16	
IC	SN 75183 N	3	
IC	SN 74800 N	2	
IC	SN 74802 N	1	
IC	SN 74804 N	2	
IC	SN 74808 N	1	
IC	SN 74809 N	1	
IC	SN 74810 N	2	
IC	SN 74840 N	1	
IC	SN 74874 N	3	
IC	SN 74886 N	1	
IC	SN 748113 N	2	
IC	SN 748132 N	1	
IC	SN 748138 N	1	
IC	SN 748157 N	3	
IC	SN 748158 N	1	
IC	SN 748182 N	2	
IC	SN 748260 N	2	
IC	SN 748280 N	7	
IC	SN 74132 N	1	
IC	9334	3	
IC	9612 E	5	
IC	9613	5	
IC	93546	2	
IC	935253	12	
IC	HMI 6701	6	

NAVN

NR.

BLAD

UDGAVE

24/2-74

STYKLISTE

	SU 75182 N	3	
IC	SU 74S124N	1	
IC	ROM 554 (SU 74S287)	1	
IC	ROM 555 — u —	1	
IC	ROM 556 — u —	1	
IC	ROM 557 — u —	1	
IC	ROM 558 — u —	1	
IC	ROM 559 — u —	1	
IC	ROM 560 — u —	1	
IC	ROM 561 — u —	1	
IC	ROM 562 — u —	1	
IC	ROM 563 — u —	1	
IC	ROM 564 — u —	1	
IC	ROM 565 — u —	1	
	SOKKEL FOR 40 BENS DIP	6	
	SOKKEL FOR 16 BENS DIP	13	
	SWITCH INTERDIL 9.16401.02	5	
SIL	DALE CSP-08 E-01-390 J	2	
SIL	216 CH 102 X 5 PD (SPRAGUE)	2	
MODSTAND	120 E 5% 1/20 W	11	
— u —	390 E 5% 1/20 W	5	
— u —	470 E 5% 1/20 W	2	
— u —	1 K 5% 1/20 W	6	
— u —	1 K 5 5% 1/20 W	6	
— u —	2 K 5% 1/20 W	1	
— u —	3 K 2 5% 1/20 W	1	

UDGAVE

24/2-76

21/5-76

15/3-77

NAVN

NR.

BLAD

FPA 201

3+

STYKLISTE

MODSTAND		
— 6k8 5% 1/20W	1	
KONDENSATOR 150 pF	3	
— " — 220 pF	2	
— " — 10 nF	1	
— " — 33 nF	1	
— " — 47 nF/6V TANTAL	1	
POTENTIOMETER 5K AMPHENOL ^{2900W}	2	
CBL 813	1	
CBL 814	1	
Sokkel for 8 bær DIP	1	
MODSTAND 4k7 5% 1/20W	1	
MODSTAND 1k 5% 1/8W	1	
KONDENSATOR 68 pF	1	
KONDENSATOR, TANTAL, 15 nF/20V	1	
DIODE 1N914	1	
IC SN 72 560 (TL 560 CP)	1	
47 nF 12V	1	
AGATRONIC OSCILLATOR CCO-2/8,000 MHz	1	
33 pF	6	

UDGAVE

4/2-76

1/5-76

15/3-77

1/7-77

NAVN

A24957

NR.

FPA 801

BLAD

44

LIST FPA801 PROMS. 76.05.10 KNEH
 ROM 565 * ROM 564 * ROM 563 * ROM 562 *

	* ALU				* SOURCE				* DEST			
	7	6	5	4	3	1	0	0	E	0	1	2
	12	11	10	9	12	11	10	9	12	11	10	9
ADDR000	1	1	1	1	1	1	1	1	1	1	1	1
ADDR001	1	0	0	1	1	0	1	1	0	1	1	1
ADDR002	1	1	1	1	1	1	1	1	1	1	1	1
ADDR003	0	0	0	0	0	0	0	1	0	1	0	0
ADDR004	0	0	1	0	0	0	0	1	1	0	1	0
ADDR005	1	1	1	1	1	1	1	1	1	1	1	0
ADDR006	1	1	1	1	1	1	1	1	1	1	1	1
ADDR007	1	1	1	1	1	1	1	1	1	1	1	1
ADDR010	0	0	1	0	0	0	0	1	1	0	1	0
ADDR011	1	0	0	1	1	0	0	0	0	0	1	1
ADDR012	1	1	1	1	1	1	1	1	1	1	1	1
ADDR013	1	1	1	1	1	1	1	1	1	1	1	1
ADDR014	1	0	1	0	0	0	0	1	1	0	1	0
ADDR015	1	1	1	1	1	1	1	1	1	1	1	1
ADDR016	1	0	1	0	0	0	0	1	1	0	1	0
ADDR017	1	0	1	0	0	0	0	1	1	0	1	0
ADDR020	0	0	1	0	0	0	0	1	1	0	1	0
ADDR021	1	0	0	1	1	0	0	0	0	0	1	1
ADDR022	1	1	1	1	1	1	1	1	1	1	1	1
ADDR023	1	1	1	1	1	1	1	1	1	1	1	1
ADDR024	1	0	1	0	0	0	0	1	1	0	1	0
ADDR025	1	1	1	1	1	1	1	1	1	1	1	1
ADDR026	1	0	1	0	0	0	0	1	1	0	1	0
ADDR027	1	0	1	0	0	0	0	1	1	0	1	0
ADDR030	0	0	1	0	0	0	0	1	1	0	1	0
ADDR031	1	0	0	1	1	0	0	0	0	0	1	1
ADDR032	1	1	1	1	1	1	1	1	1	1	1	1
ADDR033	1	1	1	1	1	1	1	1	1	1	1	1
ADDR034	1	0	1	0	0	0	0	1	1	0	1	0
ADDR035	1	1	1	1	1	1	1	1	1	1	1	1
ADDR036	1	0	1	0	0	0	0	1	1	0	1	0
ADDR037	1	0	1	0	0	0	0	1	1	0	1	0
ADDR040	1	1	1	1	1	1	1	1	1	1	1	1
ADDR041	1	1	1	1	1	1	1	1	1	1	1	1
ADDR042	1	0	0	1	1	0	1	1	0	1	0	0
ADDR043	1	1	1	1	1	1	1	1	1	1	1	1
ADDR044	1	1	0	0	0	0	0	0	1	0	0	1
ADDR045	1	0	0	1	1	0	1	1	0	0	1	0
ADDR046	0	0	0	0	0	0	0	1	0	1	0	0
ADDR047	0	0	0	0	0	0	0	1	0	1	0	0
ADDR050	0	0	1	0	0	0	0	1	1	0	1	0
ADDR051	1	1	1	1	1	1	1	1	1	1	1	1
ADDR052	1	1	0	0	0	0	0	0	1	0	0	1
ADDR053	1	0	0	1	1	0	1	1	0	0	1	0
ADDR054	1	1	1	1	1	1	1	1	1	1	1	1
ADDR055	1	1	1	1	1	1	1	1	1	1	1	1
ADDR056	1	0	0	1	1	0	1	1	0	1	0	0
ADDR057	1	1	1	1	1	1	1	1	1	1	1	1
ADDR060	1	1	1	1	1	1	1	1	1	1	1	1
ADDR061	1	1	1	1	1	1	1	1	1	1	1	1
ADDR062	1	1	1	1	1	1	1	1	1	1	1	1
ADDR063	1	1	1	1	1	1	1	1	1	1	1	1
ADDR064	0	0	1	0	0	0	0	1	1	0	1	0
ADDR065	0	0	0	0	0	0	0	1	0	1	0	0
ADDR066	0	0	1	0	0	0	0	1	1	0	1	0
ADDR067	1	0	1	1	1	0	0	0	1	0	1	0
ADDR070	0	0	1	0	0	0	0	1	1	0	1	0
ADDR071	1	0	0	1	1	0	1	1	0	0	1	0
ADDR072	1	1	1	1	1	1	1	1	1	1	1	1
ADDR073	0	0	1	0	0	0	0	1	1	0	1	0
ADDR074	1	0	1	1	1	0	0	0	0	1	1	0
ADDR075	1	1	1	1	1	1	1	1	1	1	1	0

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ADDR076	0	0	1	0	0	0	1	1	0	0	1	0	1	1	0
ADDR077	1	0	0	1	1	0	1	1	0	1	1	1	1	1	1
ADDR100	0	0	1	0	0	0	0	1	1	0	0	1	0	0	1
ADDR101	1	0	0	1	1	0	0	0	0	0	1	1	0	0	1
ADDR102	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR103	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR104	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR105	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR106	1	0	0	1	1	0	1	1	0	1	1	1	1	1	1
ADDR107	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR110	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR111	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR112	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
ADDR113	0	0	0	0	0	0	0	1	0	0	1	1	0	0	1
ADDR114	0	0	1	0	0	0	0	1	1	0	0	1	0	1	0
ADDR115	0	0	1	0	0	0	0	1	1	0	0	1	0	1	0
ADDR116	0	0	1	0	0	0	0	1	1	0	0	1	0	1	0
ADDR117	0	0	1	0	0	0	0	1	1	0	0	1	0	1	0
ADDR120	1	0	0	1	1	0	1	1	0	1	1	1	1	1	1
ADDR121	0	0	1	0	0	0	0	1	1	0	0	1	0	1	0
ADDR122	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR123	0	0	1	0	0	0	0	1	1	0	0	1	0	1	0
ADDR124	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR125	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR126	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR127	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR130	1	0	1	1	1	0	0	0	0	0	1	1	0	1	0
ADDR131	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR132	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR133	0	0	1	0	0	0	0	1	1	0	0	1	0	1	0
ADDR134	1	0	0	1	1	0	1	1	0	0	1	0	1	1	0
ADDR135	1	0	0	1	1	0	1	1	0	0	1	0	0	1	0
ADDR136	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR137	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR140	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR141	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR142	1	0	1	0	0	0	0	1	1	0	0	0	0	1	0
ADDR143	0	0	1	0	0	0	0	1	1	0	0	1	0	1	0
ADDR144	0	0	1	0	0	0	0	1	1	0	0	1	0	1	0
ADDR145	1	1	0	0	0	0	0	0	1	0	0	1	0	0	0
ADDR146	1	0	0	1	1	0	1	1	0	0	1	0	1	1	0
ADDR147	1	0	0	1	1	0	0	0	0	0	1	1	0	0	1
ADDR150	1	0	0	1	1	0	1	1	0	1	0	0	1	0	0
ADDR151	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR152	1	0	0	1	1	0	1	1	0	1	1	1	1	1	1
ADDR153	1	0	0	1	1	0	1	1	0	1	0	0	1	0	0
ADDR154	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR155	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR156	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR157	1	0	0	1	1	0	0	0	0	0	1	1	0	0	1
ADDR160	1	0	0	1	1	0	1	1	0	1	0	0	1	0	1
ADDR161	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
ADDR162	1	0	0	1	1	0	1	1	0	1	1	1	1	1	1
ADDR163	1	0	0	1	1	0	1	1	0	1	0	0	1	0	1
ADDR164	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR165	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR166	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR167	1	0	0	1	1	0	0	0	0	0	1	1	0	0	1
ADDR170	1	0	0	1	1	0	1	1	0	1	0	0	1	0	1
ADDR171	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
ADDR172	1	0	0	1	1	0	1	1	0	1	1	1	1	1	1
ADDR173	1	0	0	1	1	0	1	1	0	1	0	0	1	0	1
ADDR174	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR175	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR176	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR177	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR200	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0
ADDR201	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
ADDR202	0	0	0	0	0	0	0	1	0	0	0	1	0	0	1
ADDR203	1	0	1	1	1	0	0	0	0	0	1	1	0	1	0
ADDR204	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR205	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0

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ADDR206	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1
ADDR207	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR210	1	1	1	1	1	1	1	1	1	0	0	1	1	1	0	1
ADDR211	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
ADDR212	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR213	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR214	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR215	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1
ADDR216	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
ADDR217	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1
ADDR220	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
ADDR221	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
ADDR222	0	0	1	0	0	0	0	0	1	0	0	1	0	1	1	0
ADDR223	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
ADDR224	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR225	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR226	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0
ADDR227	0	0	1	0	0	0	0	0	1	1	0	0	1	0	1	0
ADDR230	0	0	1	0	0	0	0	0	1	1	0	0	1	0	1	0
ADDR231	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0
ADDR232	1	0	0	1	1	0	1	1	0	0	0	0	0	1	1	0
ADDR233	1	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0
ADDR234	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR235	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR236	1	0	0	1	1	0	1	1	0	1	1	0	1	1	1	1
ADDR237	0	0	1	0	0	0	0	0	1	1	0	0	1	0	1	0
ADDR240	0	0	1	0	0	0	0	0	1	1	0	0	1	0	1	0
ADDR241	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR242	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	1
ADDR243	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR244	1	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1
ADDR245	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR246	1	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1
ADDR247	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0
ADDR250	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR251	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR252	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1
ADDR253	0	0	1	0	0	0	0	0	1	1	0	0	1	0	1	0
ADDR254	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	1
ADDR255	1	0	1	0	0	0	0	0	1	1	0	0	0	0	0	1
ADDR256	1	0	1	0	0	0	0	0	1	1	0	0	0	0	1	1
ADDR257	1	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1
ADDR260	0	0	1	0	0	0	0	0	1	1	0	0	1	0	1	0
ADDR261	0	1	1	1	1	0	0	1	0	1	0	0	0	0	1	0
ADDR262	1	0	0	1	1	0	1	1	0	0	0	1	1	1	0	1
ADDR263	1	1	0	0	0	0	0	0	1	0	0	1	0	0	0	1
ADDR264	1	0	0	1	1	0	1	1	0	0	1	1	1	1	1	1
ADDR265	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR266	1	0	0	1	1	0	1	1	0	0	1	1	1	1	1	1
ADDR267	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0
ADDR270	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR271	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR272	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR273	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR274	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR275	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR276	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR277	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR300	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
ADDR301	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR302	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR303	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR304	0	1	1	1	1	0	0	1	0	1	0	0	0	0	1	0
ADDR305	1	0	0	1	1	0	1	1	0	0	1	0	1	1	0	1
ADDR306	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0
ADDR307	0	0	0	0	0	0	0	0	1	0	1	0	0	0	1	0
ADDR310	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0
ADDR311	1	0	0	1	1	0	1	1	0	0	0	1	1	1	0	0
ADDR312	0	0	0	0	0	0	0	0	1	0	1	1	0	0	1	0
ADDR313	1	0	0	1	1	0	1	1	0	0	0	0	1	1	0	1
ADDR314	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR315	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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ADDR316	1	0	1	0	0	0	C	1	1	0	0	0	0	0	1	0
ADDR317	0	0	1	0	0	0	C	1	1	0	0	1	0	0	1	0
ADDR320	0	0	1	0	0	0	C	1	1	0	0	1	0	1	1	0
ADDR321	1	0	0	1	1	0	1	1	0	0	0	1	1	1	0	0
ADDR322	0	0	0	0	0	0	C	1	0	0	0	1	0	0	0	1
ADDR323	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR324	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR325	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR326	1	1	0	0	0	0	C	0	1	0	0	1	0	0	1	0
ADDR327	0	0	1	0	0	0	C	1	1	0	0	1	0	1	1	0
ADDR330	0	0	1	0	0	0	C	1	1	0	0	1	0	1	1	0
ADDR331	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR332	0	0	1	0	0	0	C	1	1	0	0	1	0	1	1	0
ADDR333	0	0	0	0	0	0	C	1	0	1	0	1	0	1	0	1
ADDR334	1	0	0	1	1	0	1	1	0	1	1	0	1	1	0	0
ADDR335	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	0
ADDR336	1	0	0	1	1	0	1	1	0	1	0	1	1	1	0	0
ADDR337	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR340	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR341	1	1	0	0	0	0	C	0	1	0	0	1	0	0	0	0
ADDR342	1	0	0	1	1	0	1	1	0	0	0	0	1	1	0	1
ADDR343	1	1	0	0	0	0	C	0	1	0	0	1	0	0	0	0
ADDR344	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR345	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR346	1	0	1	0	0	0	C	1	1	0	0	0	0	0	1	0
ADDR347	0	0	1	0	0	0	C	1	1	0	0	1	0	1	1	0
ADDR350	0	0	1	0	0	0	C	1	1	0	0	1	0	1	1	0
ADDR351	1	0	0	1	1	0	1	1	0	0	0	0	1	1	0	1
ADDR352	0	0	1	0	0	0	C	1	1	0	0	1	0	1	1	0
ADDR353	1	0	0	1	1	0	1	1	0	0	1	0	1	1	0	1
ADDR354	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR355	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR356	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1	1
ADDR357	0	0	1	0	0	0	C	1	1	0	0	1	0	1	1	0
ADDR360	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR361	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR362	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR363	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR364	0	0	1	0	0	0	C	1	1	0	0	1	0	1	1	0
ADDR365	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
ADDR366	0	0	1	0	0	0	C	1	1	0	0	1	0	1	1	0
ADDR367	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR370	0	0	1	0	0	0	C	1	1	0	0	1	0	1	1	0
ADDR371	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR372	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR373	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR374	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR375	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR376	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR377	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

LIST FPA801 PROMS	76.05.10	KNEH	
ROM 561	ROM 560	ROM 559	ROM 558
* NEXT	ADDRESS	* CON 0	* CON 1
0 1 2 3	4 5 CC C4	0 1 2 3	0 1 2 3

	12	11	10	9	12	11	10	9	12	11	10	9	12	11	10	9
ADDR000	0	0	0	0	0	1	1	1	0	0	1	1	0	0	1	1
ADDR001	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
ADDR002	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR003	0	0	0	0	1	0	1	1	0	1	0	0	0	0	1	1
ADDR004	0	0	1	1	1	1	C	1	1	1	1	1	1	1	1	1
ADDR005	0	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1
ADDR006	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1
ADDR007	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR010	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1
ADDR011	0	0	0	0	1	1	1	1	0	1	0	1	1	0	1	0
ADDR012	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
ADDR013	0	0	0	0	1	0	1	1	0	1	0	0	0	0	1	1
ADDR014	0	0	1	0	1	1	1	1	0	0	0	1	0	0	0	1
ADDR015	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

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ADDR016	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1
ADDR017	0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	1
ADDR020	0	0	1	0	1	1	1	1	0	0	0	1	0	0	0	1
ADDR021	0	0	0	1	0	1	1	1	0	1	0	1	1	0	1	0
ADDR022	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
ADDR023	0	0	0	1	0	0	1	1	0	1	0	0	0	0	1	1
ADDR024	0	0	1	0	1	1	1	1	0	0	0	1	0	0	0	1
ADDR025	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1
ADDR026	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1
ADDR027	0	0	0	1	1	0	1	1	0	1	0	0	0	0	1	1
ADDR030	0	0	1	0	1	1	1	1	0	0	0	1	0	0	0	1
ADDR031	0	0	0	1	1	1	1	1	0	1	0	1	1	0	1	0
ADDR032	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1
ADDR033	0	0	0	1	1	0	1	1	0	1	0	0	0	0	1	1
ADDR034	0	0	1	0	1	1	1	1	0	0	0	1	0	0	0	1
ADDR035	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR036	0	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1
ADDR037	0	0	1	0	0	0	1	1	0	0	0	1	0	0	0	1
ADDR040	0	0	1	0	0	0	1	1	0	0	0	1	0	0	0	1
ADDR041	0	0	1	0	0	0	1	1	0	0	0	1	0	0	0	1
ADDR042	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1
ADDR043	0	0	1	1	0	1	1	1	0	1	1	0	1	1	1	1
ADDR044	0	0	0	0	1	0	1	1	0	1	0	0	0	0	1	1
ADDR045	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
ADDR046	0	0	1	0	0	1	1	0	1	1	1	1	1	1	1	1
ADDR047	0	0	1	0	1	0	0	0	1	1	1	1	1	1	1	1
ADDR050	0	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1
ADDR051	0	0	1	1	1	1	0	1	1	1	1	1	0	0	1	1
ADDR052	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1
ADDR053	0	0	1	0	1	0	0	1	1	1	1	1	1	1	1	1
ADDR054	0	0	1	0	1	1	1	1	0	0	0	1	0	0	0	1
ADDR055	0	0	1	0	1	1	1	1	0	0	0	1	0	0	0	1
ADDR056	0	0	1	0	0	1	0	0	1	1	1	1	1	1	1	1
ADDR057	0	0	1	1	0	1	1	1	0	0	1	0	1	1	1	1
ADDR060	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1
ADDR061	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1
ADDR062	0	0	1	0	1	0	1	1	1	1	1	1	0	1	0	0
ADDR063	0	0	1	1	0	1	1	1	0	0	1	0	1	1	1	1
ADDR064	0	0	1	1	1	0	1	1	1	1	1	1	0	1	0	0
ADDR065	0	0	0	0	1	0	1	1	0	1	0	0	0	0	1	1
ADDR066	0	0	1	1	1	0	1	1	1	1	1	1	0	1	0	0
ADDR067	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1
ADDR070	0	0	1	1	1	0	1	0	1	1	1	1	1	1	1	1
ADDR071	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1
ADDR072	0	0	1	0	1	1	1	1	0	0	0	1	0	0	0	1
ADDR073	0	1	0	0	0	0	1	1	0	1	0	0	0	0	1	1
ADDR074	1	0	1	0	0	1	1	0	0	0	0	1	1	1	1	1
ADDR075	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR076	0	0	1	1	0	1	0	0	1	1	1	1	1	1	1	1
ADDR077	0	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
ADDR100	0	0	1	0	1	1	1	1	0	0	0	1	0	0	0	1
ADDR101	0	1	0	0	0	1	1	0	0	1	0	1	1	1	1	1
ADDR102	0	1	0	0	0	0	1	1	1	1	1	1	1	1	1	1
ADDR103	0	1	0	0	0	0	1	1	0	1	0	0	0	0	1	1
ADDR104	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR105	0	0	1	0	1	1	1	1	0	0	0	1	0	0	0	1
ADDR106	0	0	1	1	1	0	0	1	1	1	1	1	1	0	1	1
ADDR107	0	0	1	1	1	0	0	0	1	1	1	1	1	1	1	1
ADDR110	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR111	0	1	0	0	1	1	1	0	0	0	1	0	1	1	1	1
ADDR112	1	1	0	0	0	0	0	0	1	1	1	1	1	1	1	1
ADDR113	0	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1
ADDR114	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1
ADDR115	1	0	0	0	1	0	1	0	1	1	1	0	1	1	1	1
ADDR116	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1
ADDR117	1	0	0	0	1	0	1	0	1	1	1	0	1	1	1	1
ADDR120	0	1	0	1	1	0	1	1	1	1	1	1	1	0	1	1
ADDR121	0	1	0	1	1	1	0	0	1	1	1	1	1	1	1	1
ADDR122	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR123	0	1	0	1	1	1	0	0	1	1	1	1	1	1	1	1
ADDR124	0	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1
ADDR125	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0

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ADDR126	0	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1
ADDR127	1	0	1	0	0	1	1	0	0	0	0	1	1	1	1	1
ADDR130	1	0	1	0	0	1	1	0	0	0	0	1	1	1	1	1
ADDR131	0	1	0	1	1	0	0	1	1	1	1	1	1	1	1	1
ADDR132	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1
ADDR133	0	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1
ADDR134	0	1	1	0	0	0	1	1	0	0	0	1	0	0	0	1
ADDR135	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1
ADDR136	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1	1
ADDR137	0	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1
ADDR140	0	1	1	0	0	0	1	1	0	0	0	1	0	0	0	1
ADDR141	0	1	1	0	0	0	1	1	0	0	0	1	0	0	0	1
ADDR142	0	1	1	0	0	1	1	1	1	1	1	1	0	0	1	0
ADDR143	0	1	0	1	0	0	1	0	0	0	1	0	1	1	1	1
ADDR144	0	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1
ADDR145	0	1	1	0	0	1	0	1	1	1	1	1	1	1	1	1
ADDR146	0	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1
ADDR147	0	1	1	0	1	0	0	1	1	1	1	1	1	0	1	0
ADDR150	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0
ADDR151	0	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1
ADDR152	0	1	1	0	1	0	1	1	1	1	1	1	1	0	1	1
ADDR153	0	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
ADDR154	0	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1
ADDR155	0	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
ADDR156	0	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1
ADDR157	0	1	1	1	0	0	0	1	1	1	1	1	1	0	1	0
ADDR160	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0
ADDR161	0	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1
ADDR162	0	1	1	1	0	0	1	1	1	1	1	1	1	0	1	1
ADDR163	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0
ADDR164	0	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1
ADDR165	0	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0
ADDR166	0	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1
ADDR167	0	1	1	1	1	0	0	1	1	1	1	1	1	0	1	0
ADDR170	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0
ADDR171	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
ADDR172	0	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1
ADDR173	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
ADDR174	0	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1
ADDR175	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
ADDR176	0	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1
ADDR177	0	1	1	0	0	0	1	1	0	0	0	1	0	0	0	1
ADDR200	1	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1
ADDR201	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
ADDR202	1	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1
ADDR203	1	0	0	0	0	1	0	0	1	1	1	1	1	1	1	1
ADDR204	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR205	1	0	0	0	1	1	1	1	0	1	1	0	0	1	1	0
ADDR206	1	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1
ADDR207	1	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1
ADDR210	1	0	0	1	0	1	1	1	0	0	0	1	0	0	0	1
ADDR211	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1	1
ADDR212	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR213	1	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1
ADDR214	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR215	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR216	1	0	0	1	0	0	0	1	1	1	1	1	0	0	1	1
ADDR217	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR220	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1
ADDR221	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
ADDR222	1	0	0	1	0	0	0	0	1	1	1	1	1	1	1	1
ADDR223	1	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1
ADDR224	1	0	0	1	0	1	1	1	0	0	0	1	0	0	0	1
ADDR225	1	0	0	1	0	1	1	1	0	0	0	1	0	0	0	1
ADDR226	1	0	0	1	1	0	1	1	1	1	1	1	0	0	1	0
ADDR227	0	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1
ADDR230	1	0	0	0	1	0	1	0	1	1	1	0	1	1	1	1
ADDR231	1	0	0	1	1	0	0	1	1	1	1	1	1	1	1	1
ADDR232	1	0	0	1	1	0	0	0	1	1	1	1	1	1	1	1
ADDR233	1	0	0	1	1	1	1	1	0	0	0	1	0	0	0	1
ADDR234	1	0	0	1	1	1	1	1	0	0	0	1	0	0	0	1
ADDR235	1	0	0	1	1	1	1	1	0	0	0	1	0	0	0	1

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ADDR236	1	0	1	0	0	0	0	1	1	1	1	1	0	1	0
ADDR237	0	1	0	0	1	0	1	0	1	1	1	1	1	1	1
ADDR240	1	0	0	0	1	0	1	0	1	1	1	0	1	1	1
ADDR241	1	0	1	0	0	1	1	0	0	0	0	1	1	1	1
ADDR242	1	0	1	0	0	0	1	1	1	1	1	1	0	0	1
ADDR243	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1
ADDR244	1	0	1	1	1	1	1	1	1	0	0	1	1	0	1
ADDR245	1	0	1	0	0	1	1	0	0	0	0	1	1	1	1
ADDR246	1	0	1	1	0	1	1	1	1	0	0	1	1	0	1
ADDR247	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1
ADDR250	1	0	1	0	1	0	1	1	0	0	0	1	0	0	1
ADDR251	1	0	1	0	1	0	1	1	0	0	0	1	0	0	1
ADDR252	1	0	1	1	0	0	1	1	1	1	1	1	0	0	1
ADDR253	0	1	0	0	1	1	1	1	0	0	1	0	1	1	1
ADDR254	1	0	1	0	1	1	0	0	1	1	1	1	1	1	1
ADDR255	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1
ADDR256	1	0	1	1	0	0	0	1	1	1	1	1	1	1	1
ADDR257	1	0	1	0	0	1	1	1	1	0	0	0	1	1	1
ADDR260	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1
ADDR261	1	0	1	0	1	1	1	1	1	1	0	1	1	1	1
ADDR262	1	0	1	1	0	0	0	0	1	1	1	1	1	1	1
ADDR263	1	0	1	0	1	0	1	1	0	0	0	1	0	0	1
ADDR264	1	0	1	1	1	0	1	1	1	1	1	1	1	0	1
ADDR265	1	0	1	0	0	1	1	0	0	0	0	1	1	1	1
ADDR266	1	0	1	1	1	0	0	1	1	1	1	1	1	0	1
ADDR267	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1
ADDR270	1	0	1	0	0	1	1	0	0	0	0	1	1	1	1
ADDR271	0	1	0	1	0	0	1	1	1	0	1	1	1	1	1
ADDR272	1	0	1	0	0	1	1	0	0	0	0	1	1	1	1
ADDR273	0	0	0	0	0	0	1	1	0	1	0	1	0	1	1
ADDR274	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1
ADDR275	0	1	0	0	1	0	0	1	1	1	1	1	1	0	0
ADDR276	1	0	1	0	0	1	1	0	0	0	0	1	1	1	1
ADDR277	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1
ADDR300	1	0	1	0	0	1	1	0	0	0	0	1	1	1	1
ADDR301	1	1	0	0	0	0	1	1	1	1	1	1	1	1	1
ADDR302	1	1	0	0	0	0	1	0	1	1	1	1	1	1	1
ADDR303	1	1	0	0	0	0	0	1	1	1	1	1	1	1	1
ADDR304	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1
ADDR305	1	1	0	1	0	1	1	1	0	0	0	1	0	0	1
ADDR306	1	0	1	0	0	1	1	0	0	0	0	1	1	1	1
ADDR307	1	1	0	0	1	0	1	0	0	1	1	1	1	1	1
ADDR310	1	1	0	0	0	1	0	1	1	1	1	1	1	1	1
ADDR311	1	1	0	0	0	1	1	0	1	1	1	1	1	1	1
ADDR312	1	1	1	0	0	0	0	0	1	1	1	1	1	1	1
ADDR313	1	1	0	0	1	1	1	1	0	0	0	1	0	0	1
ADDR314	1	1	0	0	1	1	1	1	0	0	0	1	0	0	1
ADDR315	1	1	0	0	1	1	1	1	0	0	0	1	0	0	1
ADDR316	1	1	0	1	0	0	1	1	1	1	1	1	0	0	1
ADDR317	0	1	0	0	1	0	1	0	1	1	1	1	1	1	1
ADDR320	1	0	0	0	1	0	1	0	1	1	1	0	1	1	1
ADDR321	1	1	0	0	0	1	1	0	1	1	1	1	1	1	1
ADDR322	1	1	0	1	1	0	0	0	1	1	1	1	1	1	1
ADDR323	1	0	0	0	1	0	1	0	1	1	1	0	1	1	1
ADDR324	1	1	0	1	0	1	1	1	0	0	0	1	0	0	1
ADDR325	1	1	0	1	0	1	1	1	0	0	0	1	0	0	1
ADDR326	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
ADDR327	1	1	0	1	1	0	1	1	0	0	1	0	1	1	1
ADDR330	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1
ADDR331	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR332	1	1	0	1	0	1	0	1	1	1	1	1	1	1	1
ADDR333	1	1	0	0	1	0	1	1	0	1	1	1	1	1	1
ADDR334	1	1	0	0	0	1	1	0	1	1	1	1	1	1	1
ADDR335	1	1	0	0	0	1	1	0	1	1	1	1	1	1	1
ADDR336	1	1	0	0	0	1	1	0	1	1	1	1	1	1	1
ADDR337	1	1	0	1	0	0	0	1	1	1	1	1	0	0	1
ADDR340	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR341	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1
ADDR342	1	1	1	0	0	0	1	0	1	1	1	1	1	1	1
ADDR343	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1
ADDR344	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1
ADDR345	1	1	1	0	0	1	1	1	0	0	0	1	0	0	1

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ADDR346	1	1	1	0	1	0	1	1	1	1	1	1	0	0	1	0
ADDR347	0	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1
ADDR350	1	0	0	0	1	0	1	0	1	1	1	0	1	1	1	1
ADDR351	1	1	1	0	1	1	1	1	0	0	0	1	0	0	0	1
ADDR352	1	0	0	0	1	0	1	0	1	1	1	0	1	1	1	1
ADDR353	1	1	1	1	0	0	1	1	0	0	0	1	0	0	0	1
ADDR354	1	1	1	0	1	1	1	1	0	0	0	1	0	0	0	1
DR355	1	1	1	0	1	1	1	1	0	0	0	1	0	0	0	1
ADDR356	1	1	1	0	1	0	0	1	1	1	1	1	0	0	1	0
ADDR357	0	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1
ADDR360	1	1	1	1	0	0	1	1	0	0	0	1	0	0	0	1
ADDR361	1	1	1	1	0	0	1	1	0	0	0	1	0	0	0	1
ADDR362	1	0	0	0	1	0	1	0	1	1	1	0	1	1	1	1
ADDR363	1	1	1	1	0	1	1	1	0	0	1	0	1	1	1	1
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ADDR365	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1	1
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ADDR376	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR377	1	0	0	0	0	0	0	1	1	1	1	1	0	1	1	1

FPA 801
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LIST FPA801 PROMS. 76.05.10 KNEH

ROM 557 * ROM 556 *								ROM 555 * ROM 554 *								
FUNCTIONS								CONSTANTS								
	0	1	2	3	4	5	6	7	0	1	2	4	20	21	22	23
	12	11	10	9	12	11	10	9	12	11	10	9	12	11	10	9
ADDR000	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR001	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
ADDR002	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR003	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1
ADDR004	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0
ADDR005	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1
ADDR006	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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ADDR010	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0
ADDR011	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR012	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR013	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR014	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1
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ADDR030	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0
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ADDR032	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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ADDR041	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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ADDR046	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR047	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR050	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0
ADDR051	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR052	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0
ADDR053	1	0	0	0	0	1	0	1	1	1	1	1	1	1	1	1
ADDR054	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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ADDR057	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR060	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR061	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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ADDR065	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1
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ADDR067	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR070	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0
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ADDR072	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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ADDR074	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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ADDR076	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0
ADDR077	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
ADDR100	1	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0
ADDR101	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR102	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR103	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR104	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR105	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR106	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
ADDR107	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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ADDR111	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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ADDR113	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR114	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1
ADDR115	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1
ADDR116	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
ADDR117	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
ADDR120	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
ADDR121	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1
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ADDR123	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
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ADDR142	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR143	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
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ADDR146	1	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1
ADDR147	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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ADDR162	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
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ADDR167	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR170	1	0	0	0	1	0	1	0	1	1	1	1	1	1	1	1
ADDR171	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
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ADDR316	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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ADDR320	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	0	0
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ADDR372	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR373	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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ADDR376	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
ADDR377	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

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Unit

Dwg. No.

A25049

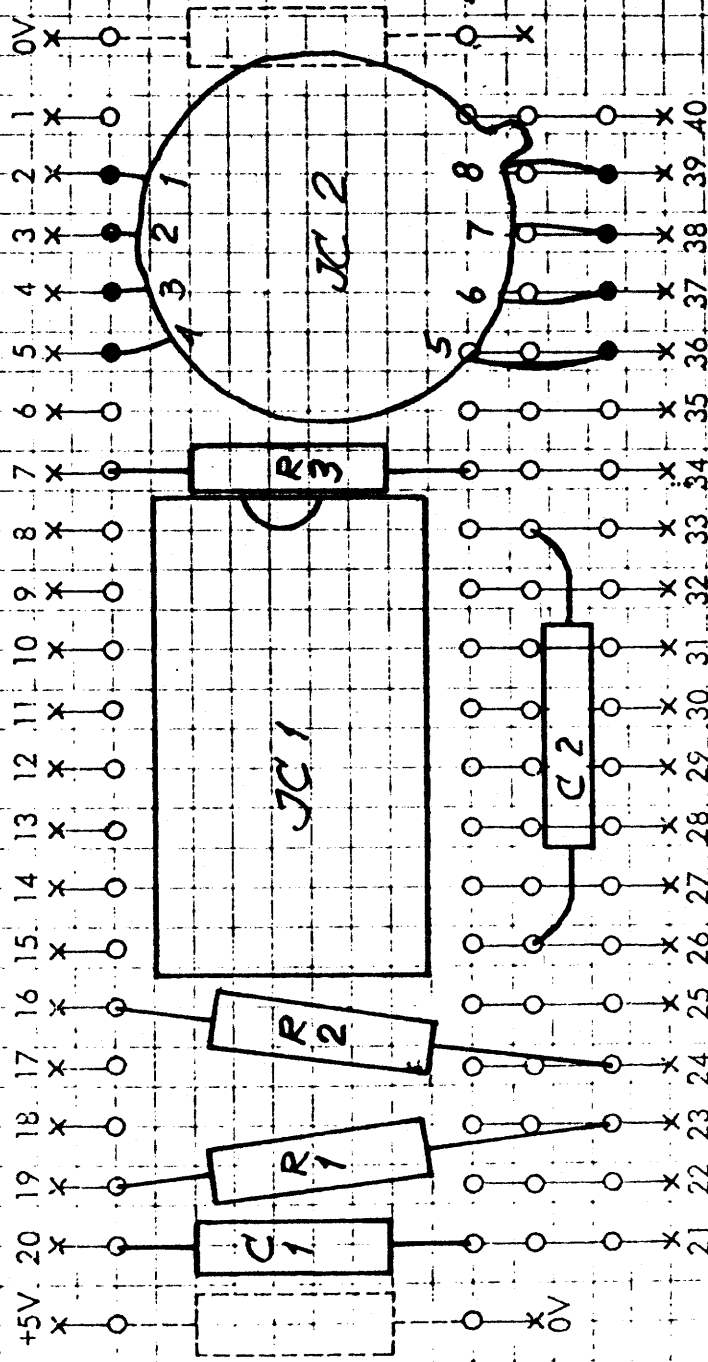
Kredsløb: KT-585 8 MHz and 30 kHz oscillator

Montage:

Set fra komponentsiden

Intern tråkning:

+5V - 39
+5V - 34
34 - 33
33 - 32
32 - 23
0V - 5
0V - 15
15 - 16
0V - 26
29 - 20
30 - 21
19 - 8
8 - 31
31 - 24
7 - 13



Komponenter:

JC1: 74S124

C1: 33nF

C2: 47nF (benene isoleres med teflon)

R1: 3k3 1/20W

R2: 2k 1/20W

JC2: AGATRON/C OSCILLATOR CCO-8/8MHz

R3: 1k5 1/20W

751024 JSA

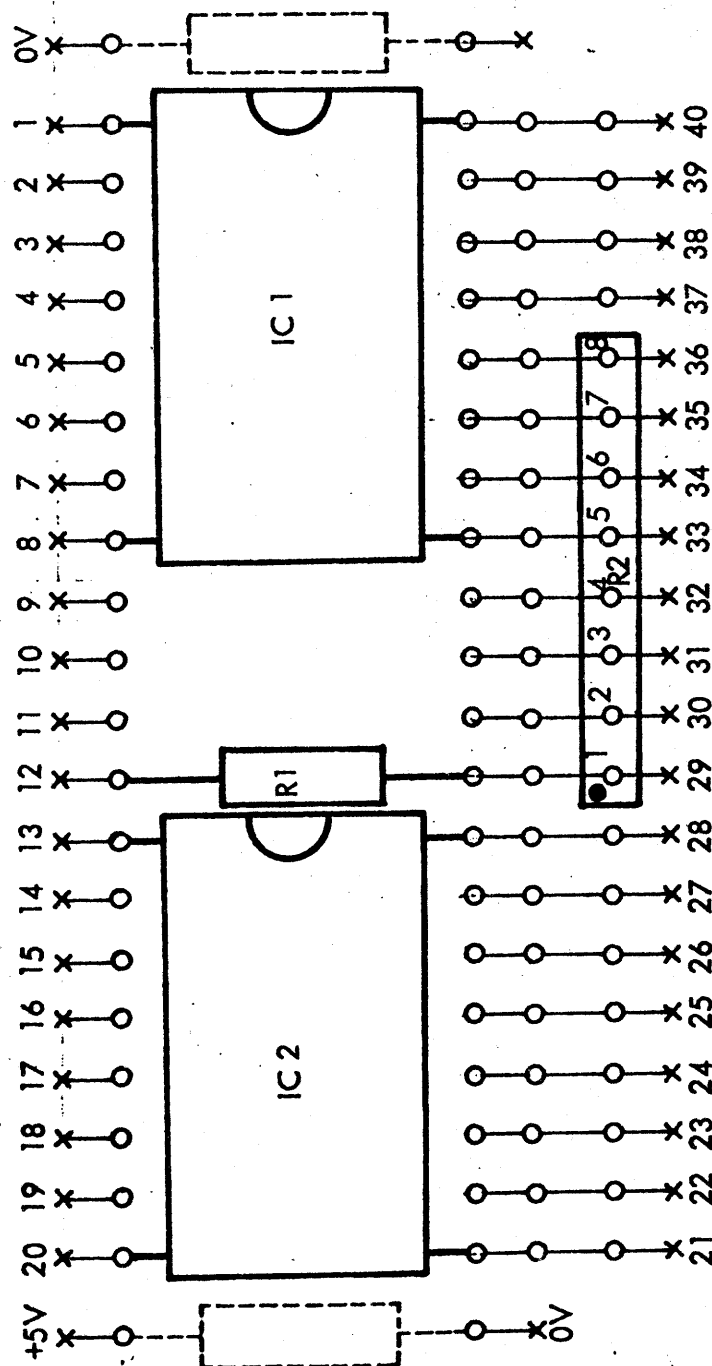
Kredsløb: KT - 513

Montage:

Set fra komponentsiden

Intern trådning:

+5V	-	40
40	-	29
29	-	28
0V	-	8
0V	-	20
32	-	19
31	-	21
30	-	16
12	-	15
0V	-	37
13	-	35
14	-	36



Komponenter:

- IC 1: ROM XXX Monteres i sokkel.
- IC 2: SN 74298
- R 1: MODSTAND 390 E 5% 1/20W
- R 2: SIL RESISTOR 7 x 390 E 1/20W DALE CSP - 08

A24769

A/S REGNECENTRALEN

Designed by

751022 JSA

Drawn by

Dwg. Office Check

Design Check

Replaces Dwg. No.

due to ECN

Replaced by Dwg. No.

Unit

Dwg. No.

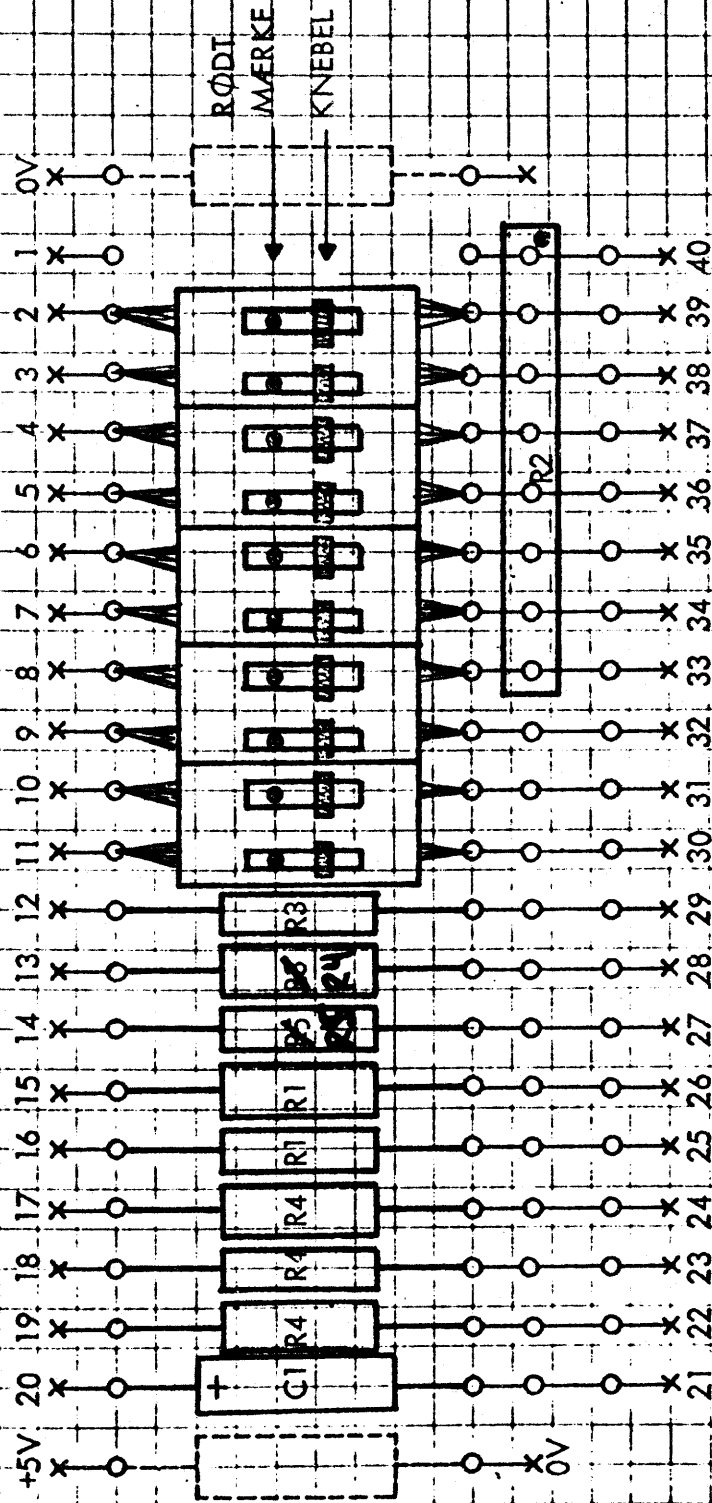
A24770

Kredsløb: KT-514

Montage:

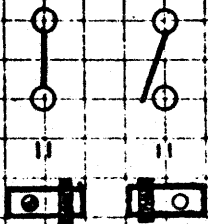
Set fra komponentsiden

Intern tråkning:



Komponenter:

- S1: 5 x INTERDIL 09 16401.02
- R1: MODSTAND 1k 5 % 1/20W
- R2: SIL RESISTOR 7 x 1k 1/20W DALE CSP - 08
- R3: MODSTAND 390E 5 % 1/20W
- R4: MODSTAND 1k5 5 % 1/20W
- C1: TANTAL 47uF / 6V
- R5: MODSTAND 6k8 5 % 1/20W



Unit

Dwg. No.

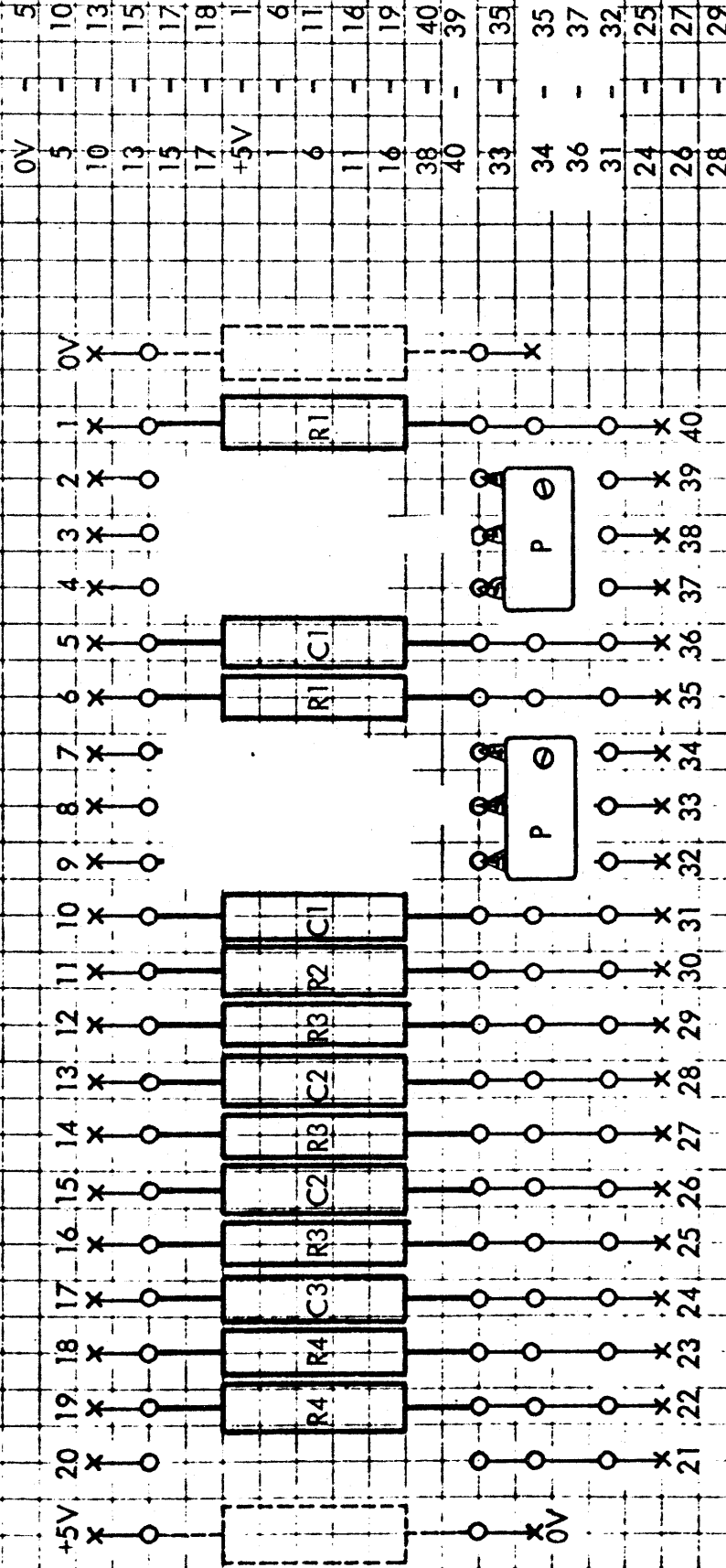
A24771

Kredsløb: KT - 515

Montage:

Set fra komponentsiden

Intern trådning:



Komponenter:

- R1: MODSTAND 390E 5% 1/20W
- R2: 120E
- R3: 1k
- R4: 470E
- C1: KONDENSATOR 220pF
- C2: 150pF
- C3: 10nF
- P: POTENTIOMETER 5k AMPHENOL 2900W (BENENE ISOLERES MED TEFLON)

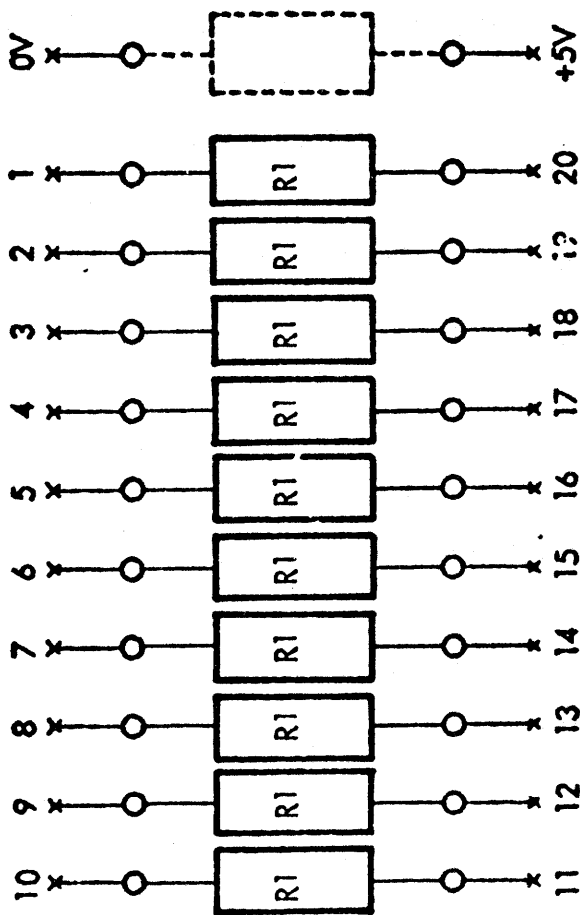
A24772

Kredsløb: KT - 516

Intern trådning:

Set fra komponentsiden

Montage:



Komponenter:

R1: MODSTAND 120E 5% 1/20W

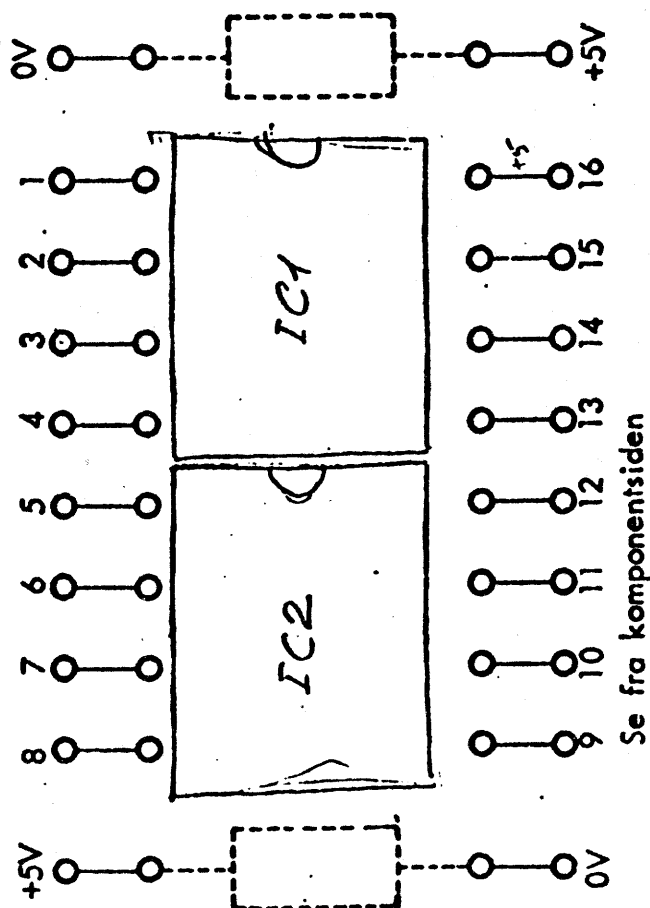
751028 J8A

Kredsløb: KT - 519

Montage:

Intern trædning:

0V - 4
4 - 8
+5V - 16
16 - 12



Komponenter:

IC1: 9612E

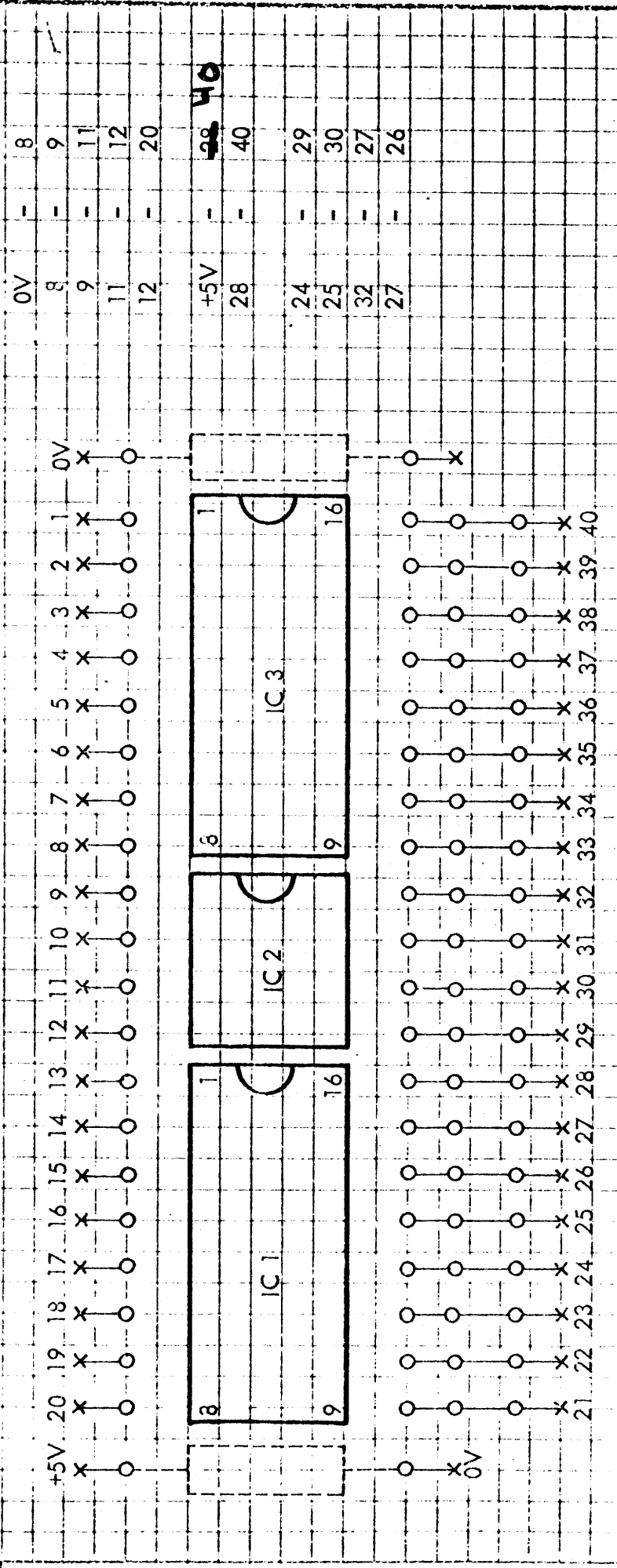
IC2: 9613

A24773

10-10-74

AUS REGNECENTRALEN	Designed by	Drawn by	Dwg. Office Check	Design Check	Replaces Dwg. No.	Due to ECN	Replaced by Dwg. No.
	760206 VH	760511 IGH					

Kredsløb:	KT - 525
Montage:	Set fra komponentsiden
Intern trådning:	



Komponenter:	IC 1 og IC 3 : 74120
	IC 2 : 8 pins DIP socket

Dwg. No.	A24774
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1802. CRES/1477

760312 VH 76A323 16H.

Kredsløb: KT - 527

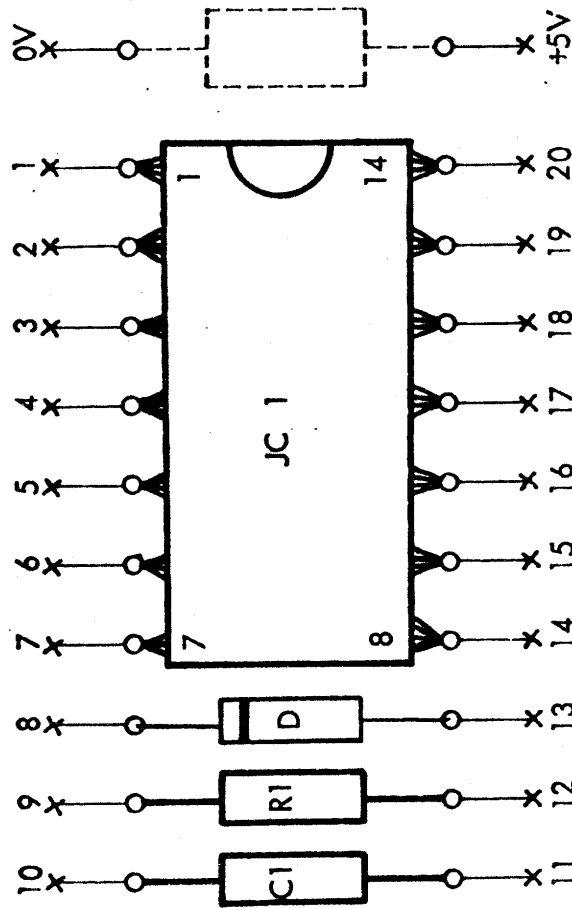
A24775

Montage:

Set fra komponentsiden

Intern trådning:

0V - 7
0V - 10
11 - 12
12 - 13
9 - 8
+5V - 20



Komponenter:

JC 1 : 74S10
C1 : 68pF Styroflex
R1 : 1k 1/8W
D : Diode 1N914

760512 VH 760512 IGH

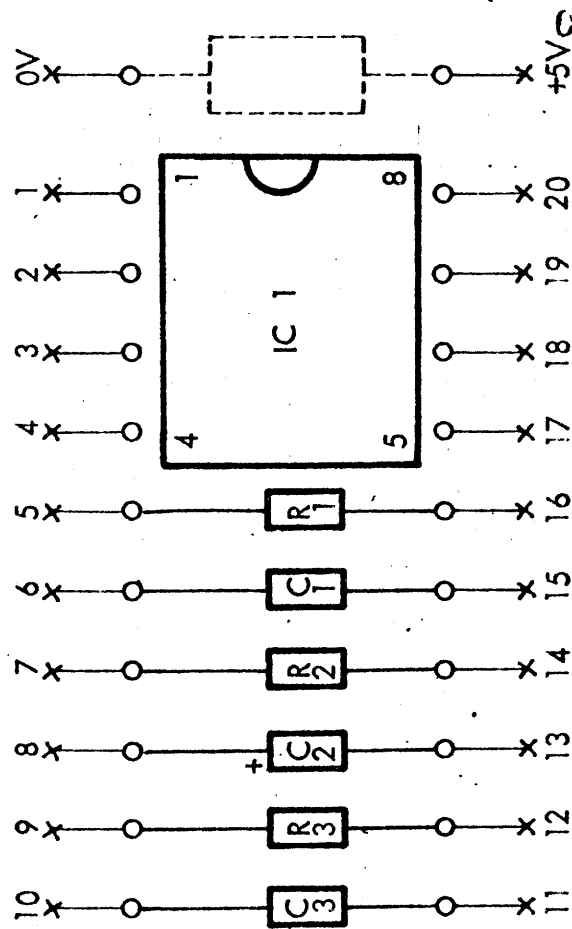
Kredsløb: KT - 532 POWER RESET

A24776

Montage:

Set fra komponentsiden

Intern tråkning:



Komponenter:

- R1, R3 : 1k 1/20W
- R2 : 4k7 1/20W
- C1, C3 : 150pF
- C2 : 15uF / 20V TANTAL
- IC 1 : TEXAS 72D560

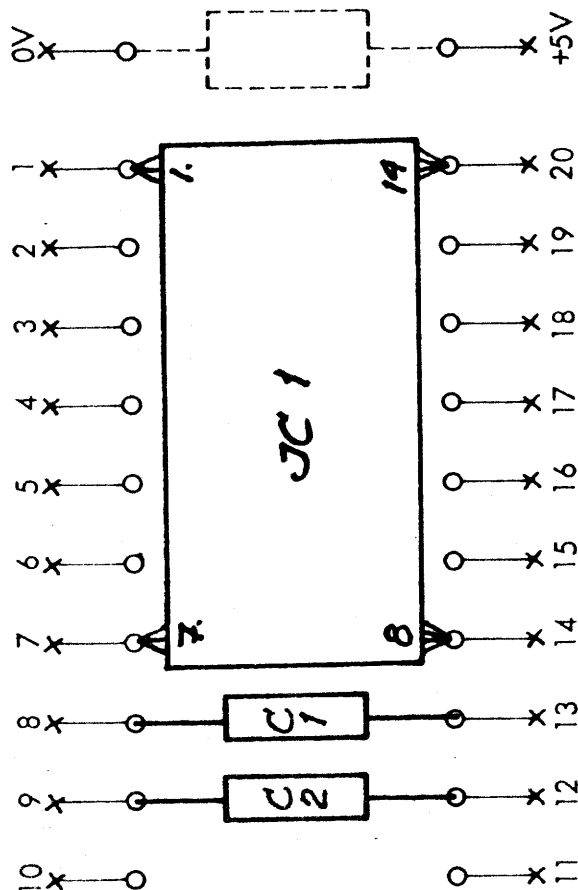
770527 VH 770609 16H.

Kredsløb: **KT-614**

A25050

Montage:

Set fra komponentsiden



Intern trådning:

0V	-	7
7	-	8
8	-	9
+5V	-	20
13	-	15
12	-	5

Komponenter:

JC 1 : 75182

C1, C2 : 33 pF, Styroflex 0080-02-018

Unit

FPA 801

Dwg. No.

Dwg. No.
A12886

TRANSMITTER JACK

71

ELCO MINI VARI/LOCK, RECEPTACLE, TYPE 8026-025, CODE 1 - 1		
PIN.	GEN. ADR	SIGNAL NAME
A1		DATA LINE 0 OUT A
A2		- 0 - B
A3		- 1 - A
A4		- 1 - B
A5		- 2 - A
A6		- 2 - B
A7		- 3 - A
B7		- 3 - B
B6		- 4 - A
B5		- 4 - B
B4		- 5 - A
B3		- 5 - B
B2		- 6 - A
B1		- 6 - B
C1		- 7 - A
C2		- 7 - B
C3		PARITY LINE OUT A
C4		- B
C5		RESET LINE OUT A
C6		- B
C7		REQ ACK LINE IN A
D7		- B
D6		DATA REQ LINE OUT A
D5		- B
D4		STATUS REQ LINE OUT A
D3		- B
D2		AUTOLOAD LINE OUT A
E1		- B
E2		CONN. LINE OUT A
E3		- B
E5		LAST CHARG. LINE OUT A
E6		- B
F7		
F7		
F6		
F2		
F1		
H1		
J1		
J2		
J6		
J7		
K7		
K6		0 VOLT
K5		-
K3		

[illegible]

J2

ELCO MINIVABILOCK, RECEPTACLE, TYPE 8026-033, CODE 1-2

PIN	GEN. ADDR.	SIGNAL NAME
A2		REMOTE AUTOLOAD
A3		OV
A4		
A5		
A6		
A7		
B1		
B2		
B3		
B5		
B6		
B7		
C1		
C2		
C6		
C7		
D1		
E1		
E2		
E6		
E7		
F1		
F2		
F3		
F5		
F6		
F7		
H2		
H3		
H4		
H5		
H6		
H7		

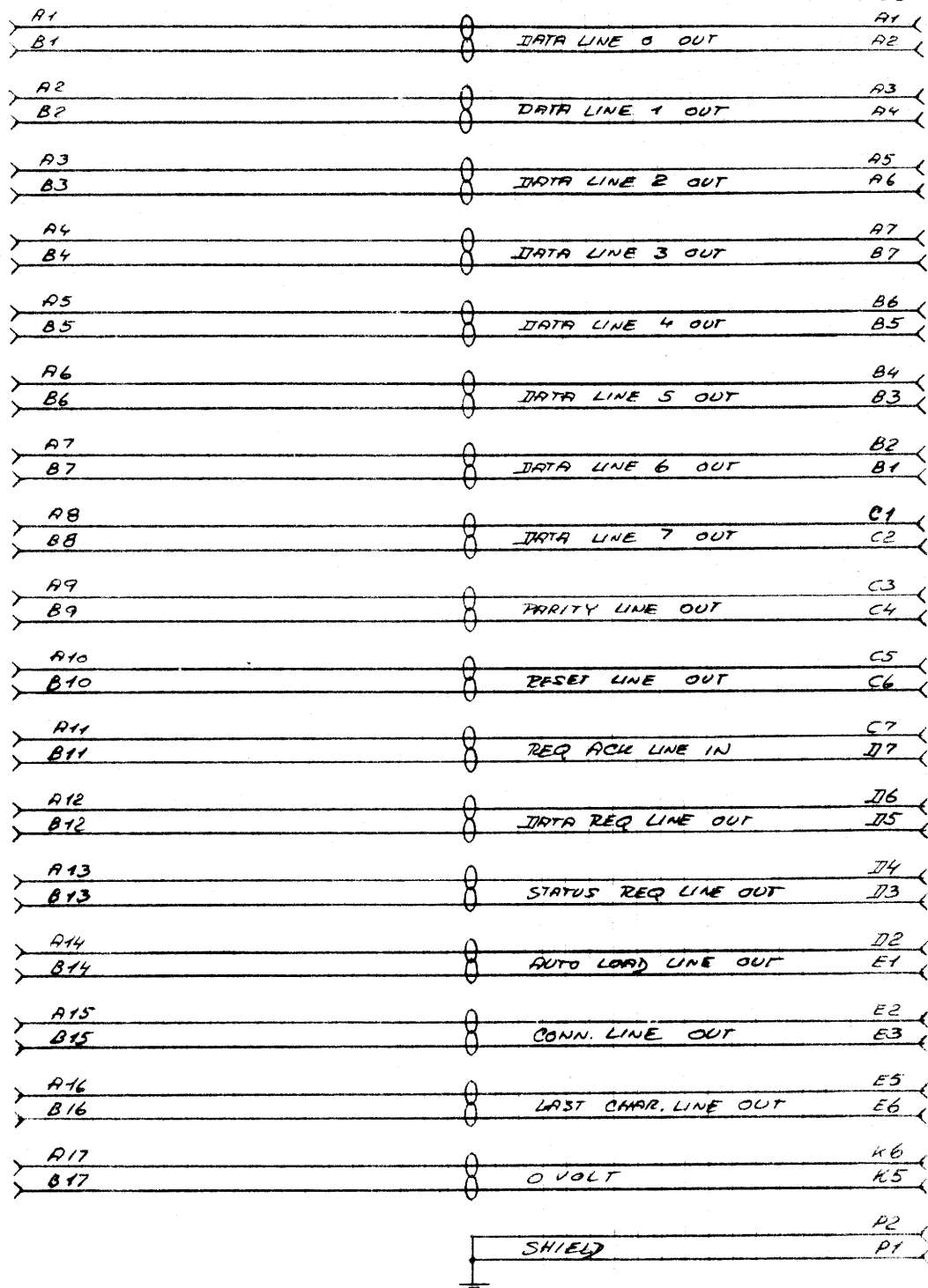
2110-754

JACK for AUTOLOAD SIGNAL

A 29703

J1004

J 1 , code 1-1
ELCO MINIVARILOCK
RECEPTACLE
TYPE 8026-075



Replaced by Dwg. No.

due to ECN

Replaces Dwg. No.

Design Check

Dwg. Office Check

Drawn by

Designed by V/H
20/10 - 75

A/S REGNENTRALEN

Unit

FPA 801

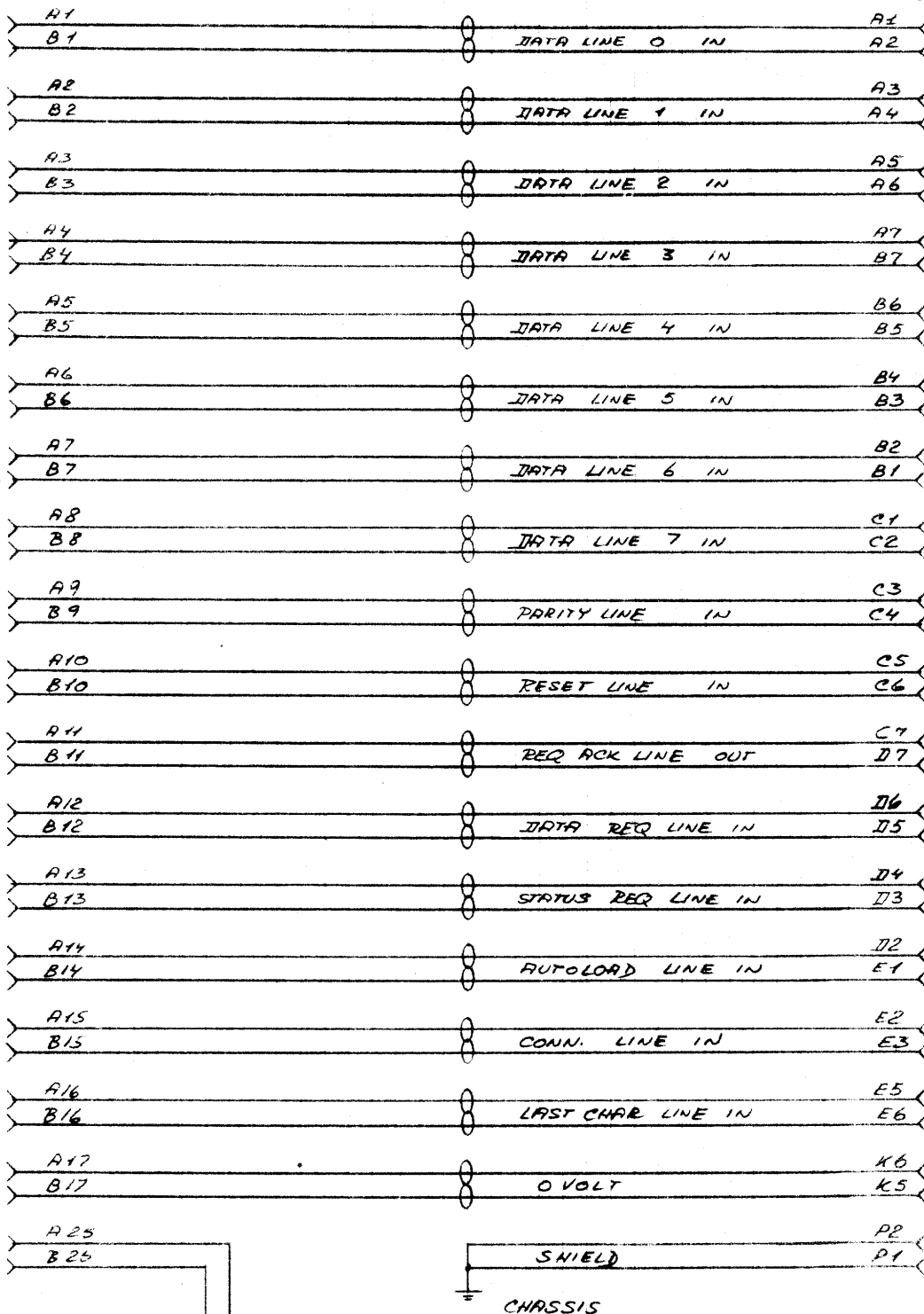
Dwg. No.

A1288E

TRANSMITTER - MELLEMIKABEL
CBL 013

J 1005

J 3 , CODE 1-3
ELCO MINIVARILOCK
RECEPTACLE
TYPE 8026-075



J 2 , CODE 1-2
ELCO MINIVARILOCK
RECEPTACLE
TYPE 8086-033

A/S REGNECENTRALEN	Designed by	VH	20/10-75
	Drawn by		
	Dwg. Office Check		
	Design Check		
	Replaces Dwg. No.		
	due to ECN		
	Replaced by Dwg. No.		

Unit	FPA 801
Dwg. No.	A12889

RECEIVER - HELLEMKABEL.
CBL 814

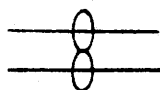
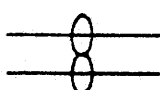
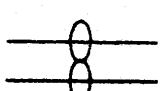
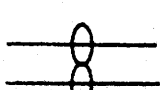
CONNECTOR I: ELCO PLUG 8026-033-000-725

CONNECTOR II: ELCO PLUG 8026-033-000-725

CABLE : $5 \times 2 \times 0,25 \text{ mm}^2$

LENGTH : 150 cm

Hc

I PIN	WIRE	II PIN
A2 A3		A2 A3
A4 A5		A4 A5
A6 A7		A6 A7
B7 B6		B7 B6
B5 B3		B5 B3

7.10.75

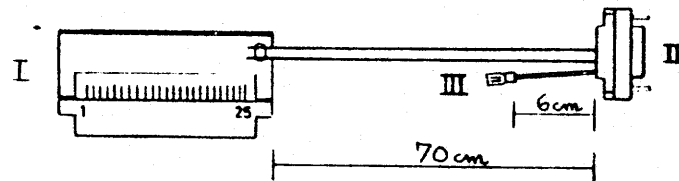
R 21214

CBL 803

~~BLAD 2~~

CONNECTOR I : ELCO KANTSTIK 2x25 POL LODDE
 CONNECTOR II : ELCO RECEPT 8026-075-000-801
 CONNECTOR III : SPADESKO 6,3mm, FORTIN., RØD
 CABLE : 18 x 2 x 0,14 mm²

HC



I	WIRE	II
A1		A1
B1		A2
A2		A3
B2		A4
A3		A5
B3		A6
A4		A7
B4		B7
A5		B6
B5		B5
A6		B4
B6		B3
A7		B2
B7		B1
A8		C1
B8		C2
A9		C3
B9		C4
A10		C5
B10		C6
A11		C7
B11		D7
A12		D6
B12		D5
A13		D4
B13		D3
A14		D2
B14		E1
A15		E2
B15		E3
A16		E5
B16		E6
A17		K6
B17		K5
III		P2
		P1

BEMÆRK:

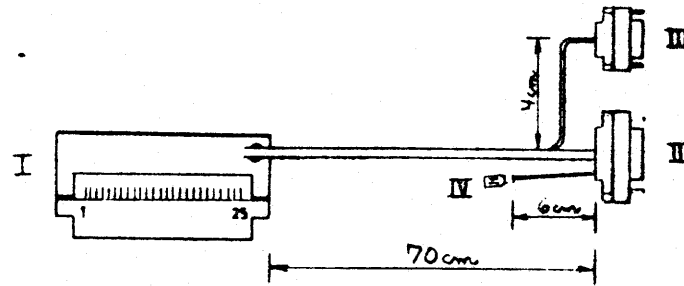
OPSPÆNDINGSPLADE CHS 801-19
 PÅSKRUES ELCO RECEPT, INDEEN
 TRÅDNING A STIK.

11.2.76

6.4.76

CONNECTOR I : ELCO KANTSTIK 2x25 POL. LODDE
CONNECTOR II : ELCO RECEPT 8026-075-000-801
CONNECTOR III : ELCO RECEPT 8026-033-000-801
CONNECTOR IV : SPADESKO 6,3mm, FORTIN. RØD.
CABLE : $19 \times 2 \times 0,14 \text{ mm}^2$

Hc

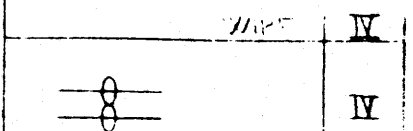
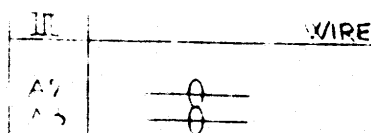


I	WIRE	II
A1	○	A1
B1	○	A2
A2	○	A3
B2	○	A4
A3	○	A5
B3	○	A6
A4	○	A7
B4	○	B7
A5	○	B6
B5	○	B5
A6	○	B4
B6	○	B3
A7	○	B2
B7	○	B1
A8	○	C1
B8	○	C2
A9	○	C3
B9	○	C4
A10	○	C5
B10	○	C6
A11	○	C7
B11	○	D7
A12	○	D6
B12	○	D5
A13	○	D4
B13	○	D3
A14	○	D2
B14	○	E1
A15	○	E2
B15	○	E3
A16	○	E5
B16	○	E6
A17	○	K6
B17	○	K5
A25	○	P2
B25	○	P1

BEMÆRK:

OPSPÆNDINGSPLADE CHS 801-20
PÅSKRUES ELCO RECEPT INDEN
TRÅDNING AF STIK.

11.2.76
6.4.76



Hc

I PIN	WIRE	II PIN
A1	HVID	1
A2	GRÅ	2
A3	HVID	3
A4	SORT	4
A5	GRÅ	5
A6	BLÅ	6
A7	HVID	7
B7	ORANGE	8
B6	GRØN	9
B5	ORANGE	10
B4	BRUN	11
B3	ORANGE	12
B2	GRÅ	13
B1	ORANGE	14
C1	GRØN	15
C2	HVID	16
C3	GRØN	17
C4	BRUN	35
C5	GRÅ	34
C6	GRØN	33
C7	HVID	32
D7	BRUN	31
D6	GRÅ	30
D5	BRUN	29
D4	SORT	28
D3	BRUN	27
D2	GRÅ	26
E1	SORT	25
E2	BLÅ	24
E3	HVID	23
E5	BLÅ	22
E6	ORANGE	21
E7	BLÅ	37
F7	GRØN	38
F2	BLÅ	39
F1	BRUN	40
H1	SORT	41
J1	GRØN	42
K6	SORT/BLÅ	20
K5	SORT/ORANGE	19
P2	SHIELD	51
P1	SHIELD	52

CONNECTOR I: ELCO PLUG 8026 - 075-000-701

CONNECTOR II: CANNON DB 52P

CABLE TYPE: PARSNOET 24 x 2 x 0.14 mm² M SHIELD

LENGTH: 5 m.

11.2.76
29.3.76



821017