
Title:

CPU 810

GENERAL INFORMATION

 **REGNECENTRALEN**

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Author: Aage Jørgensen

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Abstract: This manual contains specifications, installation, and operating instructions for the CPU 810 Central Processing Unit and the Technicians Console.

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1. GENERAL DESCRIPTION.

1.

CPU 810 is a very compact medium performance processor. The entire CPU occupies only a single printed circuit board, approximately 36 x 37 cm. The processor has the following characteristics:

24-bit single address instruction format with 64 basic instructions. Each instruction works on 4 registers (accumulators), has a 12-bit displacement, and 16 address modifications including relative, indexed, and indirect addressing.

Data formats comprise 12-bit half words, 24-bit words for integer arithmetic, and 48-bit double words for integer and floating point arithmetic.

Dynamic program relocation through use of a modified base register technique.

Microprogrammed implementation of instructions set.

Protection system consisting of memory protection by means of limit address registers, and privileged instructions executable only in monitor mode.

Interrupt system with 8 internal and 8 external (for devices) interrupt levels.

Autoload via disc channel or front-end processor.

Real time clock with 0.1 millisecon. resolution and interrupt generating 25.6 millisecon. interval timer.

An unified bus employing an asynchronous, fully interlocked request/acknowledge technique connects CPU, main storage, and

peripheral device controller. One bus cycle transfers:

23 address bits + 1 parity bit and

24 data bits + 3 parity bits.

2. SPECIFICATIONS.

2.

2.1 Performance Specifications.

2.1

Instruction Execution Times	See section 2.5
Microinstr. Execution Time	200 nanosec.
Microinstr. Word Length	35 bits + 1 parity bit
Control Store Size	2048 words x 36 bits
Internal Interrupt Levels	8
External Interrupt Levels	8 (for device interrupts)
Real Time Clock	
Resolution	0.1 millisecc.
Stability	Better than 4 sec/24 hours
Interval Timer	Interrupt every 25.6 millisecc.

2.2 Electrical Specifications.

2.2

Supply Voltage	5 V dc $\pm$ 5 percent
Current Requirement	11A

2.3 Environmental Specifications.

2.3

Ambient Temperature	10-35 degrees C
Relative Humidity	20-80 percent without condensation
Heat Dissipation	55W

2.4 Physical Specifications.

2.4

Space Requirements	1 slot in a RC8000 CPU chassis
Weight	1.25 kg (2.8 lbs)

2.5 Instruction Execution Times.

2.5

The listed instruction execution times are based on the following assumptions:

Memory access time: 550 ns to 700 ns
 Memory cycle time: < 900 ns
 Memory address within lower and upper limits
 No pending interrupts
 System Bus not used by other units.

The instruction times apply to direct addressing. Times for address modifications are listed separately.

<u>INSTRUCTION</u>	<u>EXECUTION TIME IN MICROSEC</u>
AM	3.0
AL	2.8
AC	3.4
HL left/right halfword	5.6/5.4
HS	7.2
RL	4.6
RS	5.4
RX	6.4
DL	6.6
DS	7.2
XL left/right halfword	5.6/5.4
XS left/right halfword	7.4/7.2
BZ left/right halfword	5.0/4.8
BL left/right halfword	5.0/4.8
BA left/right halfword	5.8/5.6
BS left/right halfword	5.8/5.6
WA	5.2
WS	5.2
WM	15.0
WD	18.8
AA	7.6
SS	7.6

<u>INSTRUCTION</u>	<u>EXECUTION TIME IN MICROSEC</u>	
CI	$8.6 + n \times 0.6$	1)
CF	$6.4 + n \times 0.4$	2)
FA	$16.8 + n \times 0.4$	3)
FS	$16.8 + n \times 0.4$	3)
FM	45.6	
FD	36.6	
LA	4.6	
LO	4.6	
LX	4.6	
AS left shift	$5.0 + n \times 0.6$	1)
right shift	$4.4 + n \times 0.4$	1)
AD left shift	$5.6 + n \times 0.6$	1)
right shift	$4.8 + n \times 0.4$	1)
LS	$4.4 + n \times 0.4$	1)
LD	$4.4 + n \times 0.4$	1)
NS left/right halfword	$8.2/8.0 + n \times 0.6$	1)
ND left/right halfword	$9.2/9.0 + n \times 0.6$	1)
JL without/with link	4.0/4.2	
SH no skip/skip	3.2/3.6	
SL no skip/skip	3.2/3.6	
SE no skip/skip	3.0/3.4	
SN no skip/skip	3.0/3.4	
SO no skip/skip	3.2/3.6	
SZ no skip/skip	3.0/3.4	
SX no skip/skip	3.4/3.8	
SP no skip/skip	4.2/4.6	
RE	38.8	
JE without/with link	5.2/5.4	
JD without/with link	5.8/6.0	
RI	45.8	
GP	6.2	
GG	6.2	
DO	5.4	4)
DI	5.4	4)

- 1) n = number of shifts
- 2) n = binary exponent of the FP number
- 3) n = difference between the binary exponents
- 4) Time depends on the response time of the addressed device. Specified time is for memory reference.

For address modifications add the following times to the instruction times.

ADDRESS		After AM,
<u>MODIFICATION</u>	<u>Add Microsec</u>	<u>Add Microsec</u>
None	0	0.4
Relative	0.2	0.6
Indexing	0.2	0.6
Relative +		
Indexing	0.2	0.8
Indirect	2.8	2.8

3. INSTALLATION.

3.

3.1 Installation of CPU 810.

3.1

The CPU 810 is installed in a standard RC8000 chassis, CHS 805 or equivalent. Signal cables to Operators Control Panel (OCP 802), Front-End Processor Adapter (FPA), and possibly Technicians Console Adapter (TCA 801) are connected as shown on fig. 3.1. The TCA 801 is not intended for permanent connection to the CPU 810 as it requires that the chassis is pulled a little out of the cabinet.

3.2 CPU Device Address.

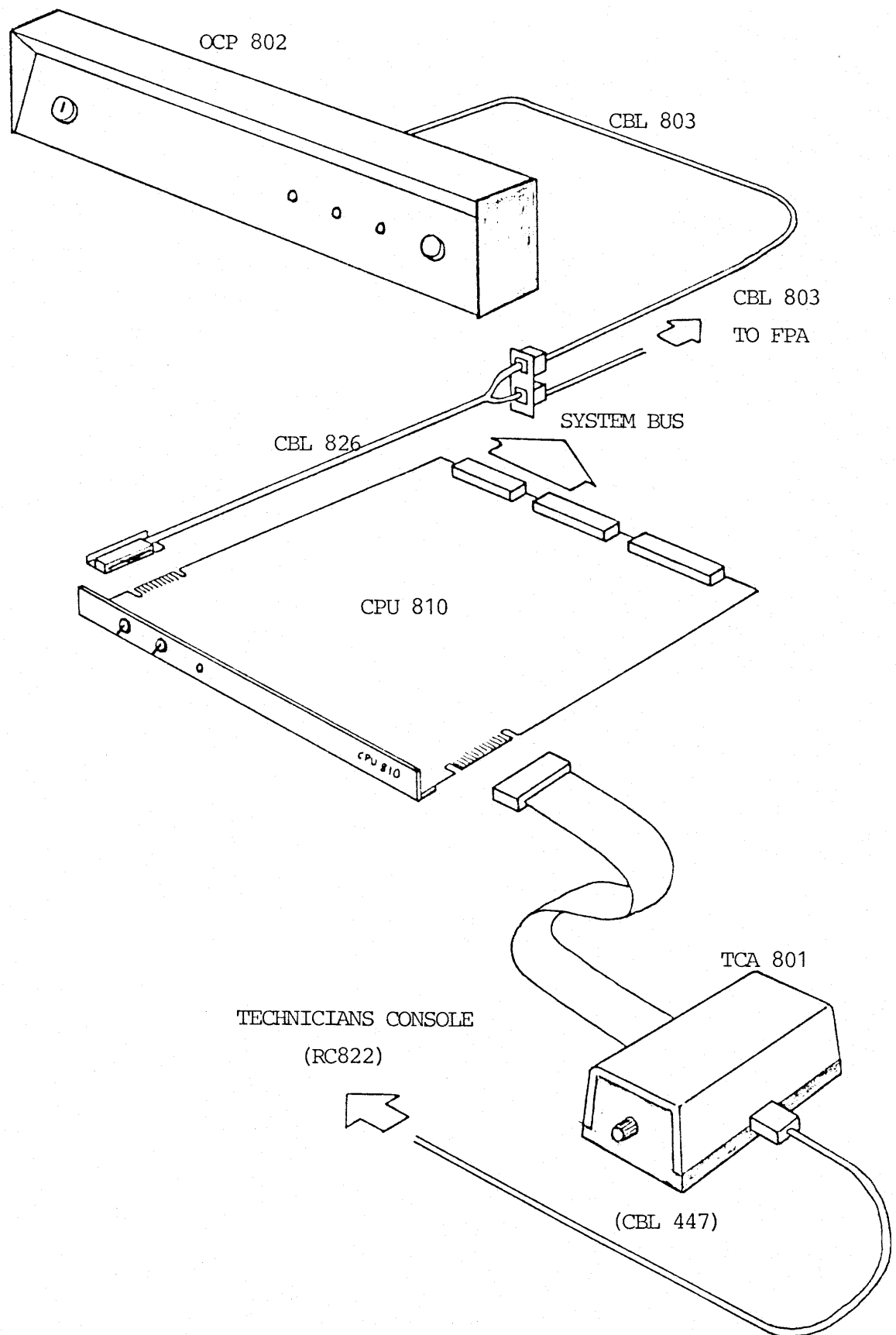
3.2

Switches for selection of the CPU device address are located on the PCBA and marked: S1, S2, and S3. Only address bits (18:22) and the address parity bit are selectable. Address bits (0:17) are fixed.

Address bits (0:17)=100 000 000 000 000 000

The CPU address (interrupt destination) is set up by means of the switches as shown in figure 3.2.

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Figure 3.1 CPU 810 interconnections

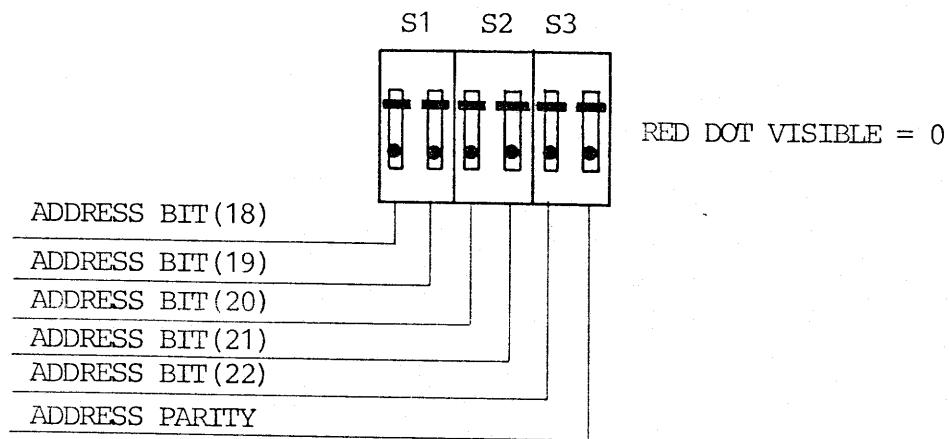


Figure 3.2 Device address selection switches.

The standard CPU device address is:

Address bits (18:22) = 00 000

Address parity = 0 (odd parity is used)

3.3 Deskew Delay Adjustments.

3.3

The deskew delays for DATARDY, SELIN, and ACK are adjusted by means of the potentiometers P1, P2, and P3 on the PCBA. See figure 3.3

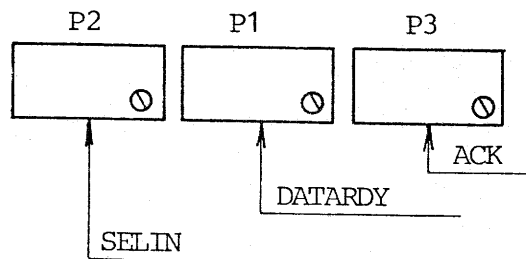


Figure 3.3 Potentiometers for deskew delay adjustments.

The delays are activated by means of a microprogrammed test loop, which continuously writes zeros into memory location 8. A Technicians Console (TC) is required to start the loop. The loop is started by typing the following commands at the TC. The commands are terminated by a RETURN.

T 4

0 < address (SIZEM) >

Address (SIZEM) is the microprogram address corresponding to the label SIZEM. Refer to microprogram listing for address.

The following procedure is recommended for an initial adjustment of the delays.

1. Turn the potentiometers fully clockwise (maximum delay).
2. Start the test loop.
3. Adjust the delays according to figure 3.4

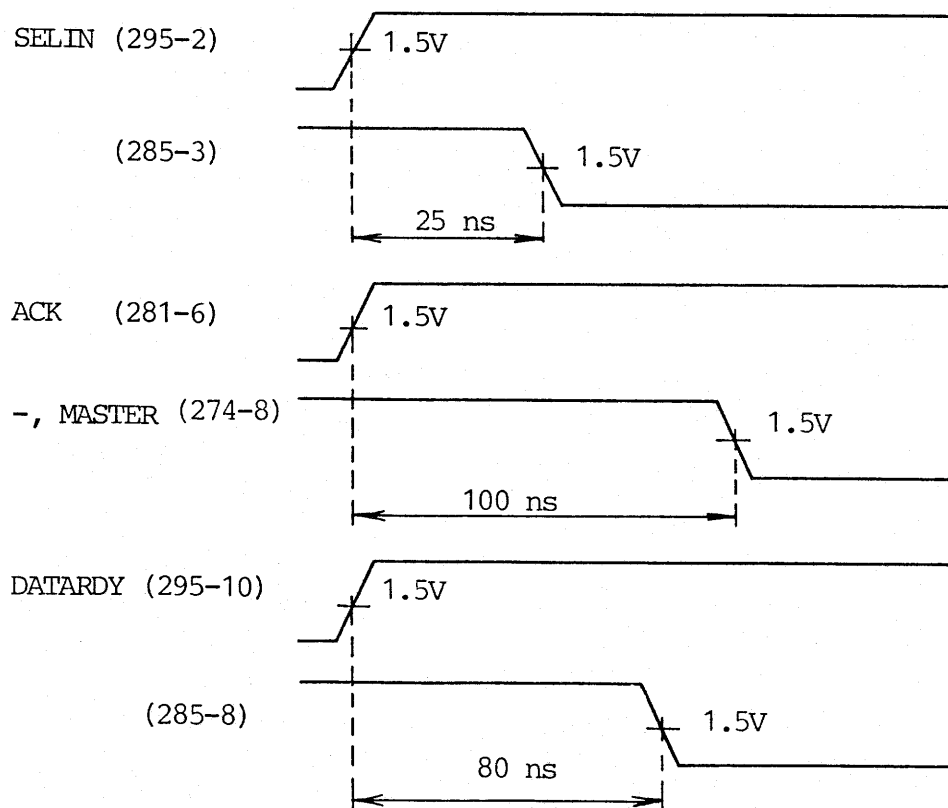


Figure 3.4 CPU 810 deskew delays.

3.4 PCBA Front Panel Switches.

3.4

The TEST and TEST MODE switches on the PCBA front panel are used to control execution of the microdiagnostics for CPU and main memory when started by means of the AUTOLOAD push button on the OCP.

TEST = ON

The microdiagnostics are started when the AUTOLOAD push button is activated. TEST MODE switch selects test mode.

TEST = OFF

Autoload is performed without start of microdiagnostics. Position of TEST MODE switch is irrelevant.

TEST MODE = SHORT

The CPU diagnostic and the short mode memory diagnostic are run before autoload.

TEST MODE = CONTINUOUS

The CPU and the normal mode memory diagnostics are repeated until stopped by operator intervention or by an error.

Detection of an error in the microdiagnostics is indicated by flashing of the AUTOLOADING lamp.

4. TECHNICIANS CONSOLE.

4.

The technicians console may be used to display and modify the contents of CPU registers and storage locations. In addition a number of other functions may be controlled from the console. E.g. single instruction stepping and start and control of diagnostic programs. The technicians console is not necessary for normal operation of the CPU, but it may facilitate trouble shooting.

4.1 Installation of Technicians Console.

4.1

A TTY compatible terminal with V.24 interface may be used as a technicians console. The terminal must be able to operate at one of the following transmission speeds: 110, 300, 1200, 2400, or 9600 bps. The console is connected to CPU 810 by means of an adapter, TCA 801, as shown on figure 3.1. The flat-cable from the adapter is connected directly to connector 1004 on the PCBA. Transmission speed is selected by means of a rotary switch on the TCA 801. The cable type which is used to connect adapter and console depends on the type of the console. For connection of an RC822 terminal cable type CBL 447 may be used.

4.2 Console Commands.

4.2

The formats of the console commands are described below. Parameters typed by the operator is shown as <parameter>. For some commands, e.g. LOAD NEXT, the processor calculates and displays a parameter. This is shown as (parameter). Octal number representation is used for addresses and contents of registers and memory locations. In the description of the commands cr = carriage return and sp = space.

XR<sp><register address>:

EXAMINE REGISTER. Displays the contents of the addressed register.

LR<sp><register address>: (sp) (sp) <contents> <cr>

LOAD REGISTER. The addressed register is loaded with <contents>.

XM<sp><memory address> <cr>

EXAMINE MEMORY. Displays the contents of the addressed memory location.

XN<sp><number of memory locations> <cr>

EXAMINE NEXT. Displays the selected number of consecutive memory locations following the last referenced location.

LM<sp><memory address>: (sp) (sp) <contents> <cr>

LOAD MEMORY. The addressed memory location is loaded with <contents>.

LN<sp>(next memory address) (:) (sp) (sp) <contents> <cr>

LOAD NEXT. The memory location following the last referenced location is loaded with <contents>.

S<cr>

SINGLE INSTRUCTION. The instruction addressed by PC is executed and the contents of the following registers is displayed: W0, W1, W2, W3, STATUS, IC, CAUSE, and SB.

C<cr>

CONTINUE. Starts instruction execution in the memory location addressed by PC.

R<sp><control store address><cr>

RUN. Starts microinstruction execution in the addressed control store location.

XS<sp><control store address><cr>

EXECUTE SUBROUTINE. Executes the addressed microprogram subroutine.

T<sp><test number><cr>

TEST. This command is used to start one of the following microprogram tests.

<u>TEST No.</u>	<u>TEST</u>
0	CPU test and memory test in normal mode.
1	CPU test.
2	Memory test, normal mode.
3	Memory test, short mode.
4	Initialize registers for test.
5	Clear and size memory.

For a detailed description of the test is referred to in the publication:

CPU 810 MICROPROGRAMMED TESTS
Users Manual

O<sp><control store address><cr>

LOOP. The command is used to start testloops in the microprogrammed tests in loop mode. The addressed loop is continuously repeated.

ESC

Activation of the ESCAPE key may be used to cancel a typed command. The processor responds to the command by displaying a ?.

Commands using the System Bus indicates a buserror by displaying a ?.

4.3 Register Addresses.

Addresses (octal) of CPU registers accessible by means of the XR and LR commands are listed below. The applicable commands are indicated for each register.

<u>ADDRESS</u>	<u>COMMAND</u>	<u>REGISTER</u>
0	XR,LR	GR(0) = W0
1	XR,LR	GR(1) = W1
2	XR,LR	GR(2) = W2
3	XR,LR	GR(3) = W3
4	XR,LR	GR(4) = STAT
5	XR,LR	GR(5) = IC
6	XR,LR	GR(6) = CAUSE
7	XR,LR	GR(7) = SB
10	XR,LR	SP(0) = CPA
11	XR,LR	SP(1) = BASE
12	XR,LR	SP(2) = LLIM
13	XR,LR	SP(3) = ULIM
14	XR,LR	SP(4) = ILIM COPY
15	XR,LR	SP(5) = INF
16	XR,LR	GR(10) = PC
17	XR,LR	SP(6) = SIZE
20	XR,LR	SP(7) = MONT
21	LR	SP(16)
22	LR	SP(17)
57	LR	Clear Interrupt Bit
60	XR	SP(16)
61	XR	SP(17)
62	XR	SP(10) = RTC

GR = General Register

SP = Scratchpad Memory.

5. CHECK-OUT PROCEDURES.

5.

Initial check-out of CPU 810 and main memory may be performed by means of the microprogrammed tests. The tests may be operated from either the OCP 802 or from the Technicians Console. Operation from the Technicians Console provides better error information and the possibility of looping on errors, etc. The CPU and the normal mode memory test should be run long enough to ensure at least 2 complete passes. The time for a pass depends on the memory size.

For a detailed description of the tests and operation of the tests from the Technicians Console is referred to:

CPU 810 MICROPROGRAMMED TESTS
Users Manual
RCSL No.: 30-M167

5.1 Test Operation from OCP.

5.1

The tests are started in the following way:

TEST switch in position ON.
TEST MODE switch in position CONTINUOUS.
Activate AUTOLOAD push button.

The AUTOLOADING lamp will be lit and the CPU test and the normal mode memory test are repeated until an error is detected or until stopped by operator intervention. Detection of an error is indicated by flashing of the AUTOLOADING lamp.

