
Title:

CPU 810

TECHNICAL MANUAL

 **REGNECENTRALEN**

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Abstract: This manual contains block diagrams, timing diagrams, logic diagrams, functional description, assembly drawing, and plug lists for the CPU 810 Central Processing Unit.

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1. INTRODUCTION.

1.

CPU 810 is a central processing unit which is used in the RC8000 processors: RC8002, RC8003, and RC8004.

CPU 810 is a microprogrammed processor with a 36-bit microinstruction format and a microinstruction execution time of 200 ns.

The 24-bit wide arithmetic section is designed around 6 cascaded Am 2901A 4-bit slice processor elements. The microprogram sequence control uses 3 cascaded Am 2911 4-bit slice microprogram sequencers which provides a 12-bit control store address. PROM's are used for the control store which has a capacity of 2048 36-bit words.

In addition to the routines for execution of the RC8000 instruction set the microprogram contain diagnostic routines for CPU and main memory, and routines for support of the technicians console.

It is assumed that the reader of this manual is familiar with RC8000 architecture, instruction format, and data formats. Such information may be found in:

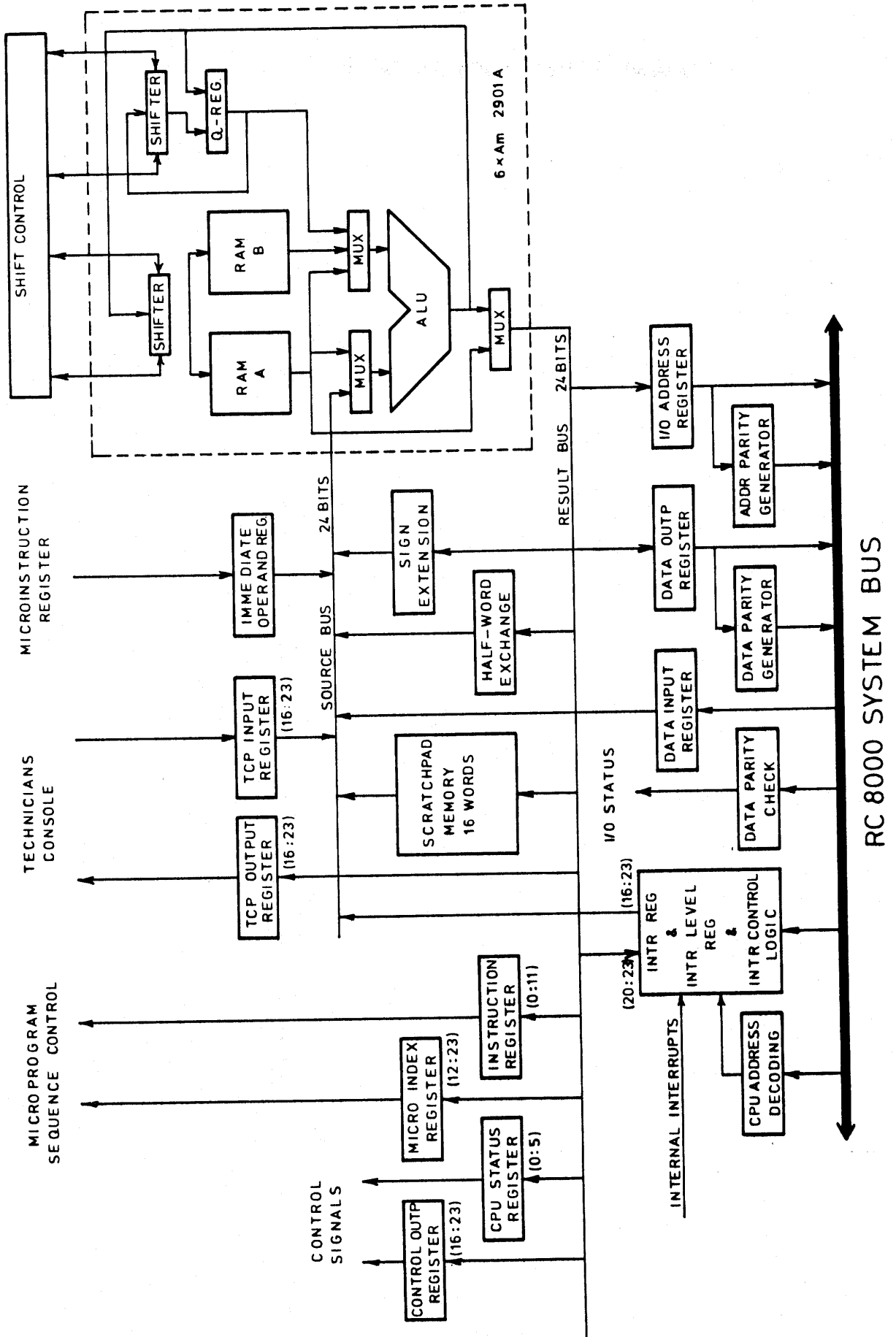
RC8000 COMPUTER REFERENCE MANUAL

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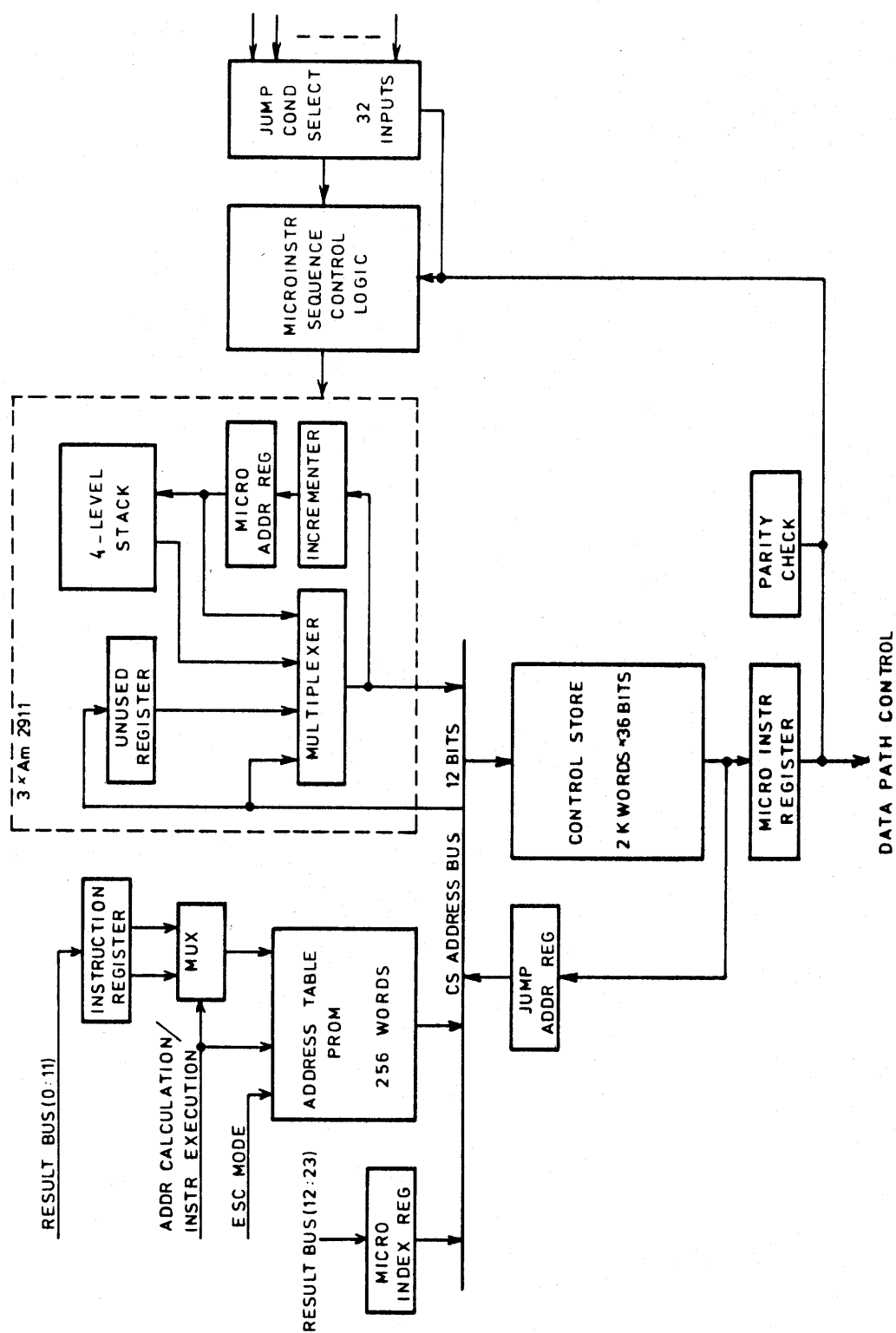
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CPU 810

CPU 810 DATA PATHS



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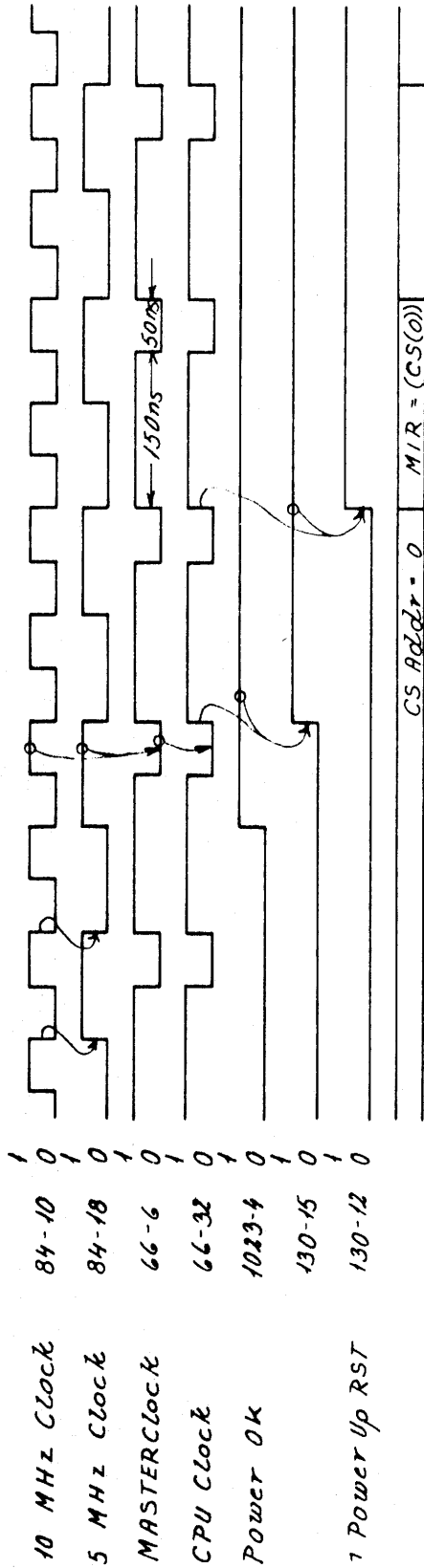
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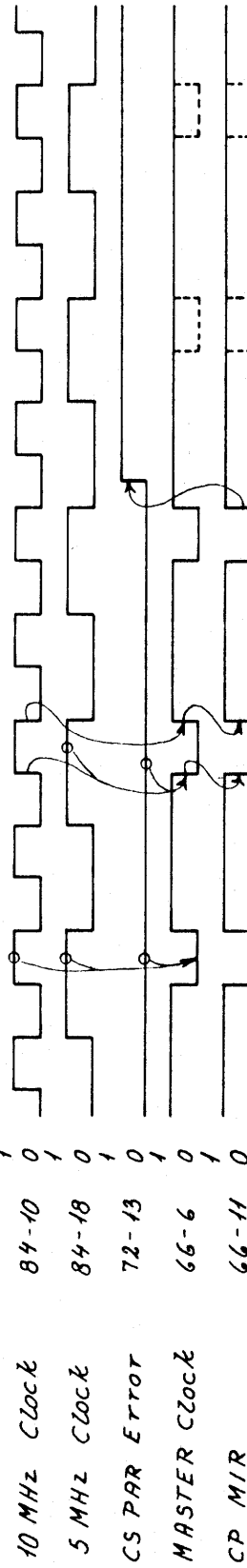
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Power Up

MIR is loaded with the contents of CS location 0 after Power UP.



Control Store Parity Error



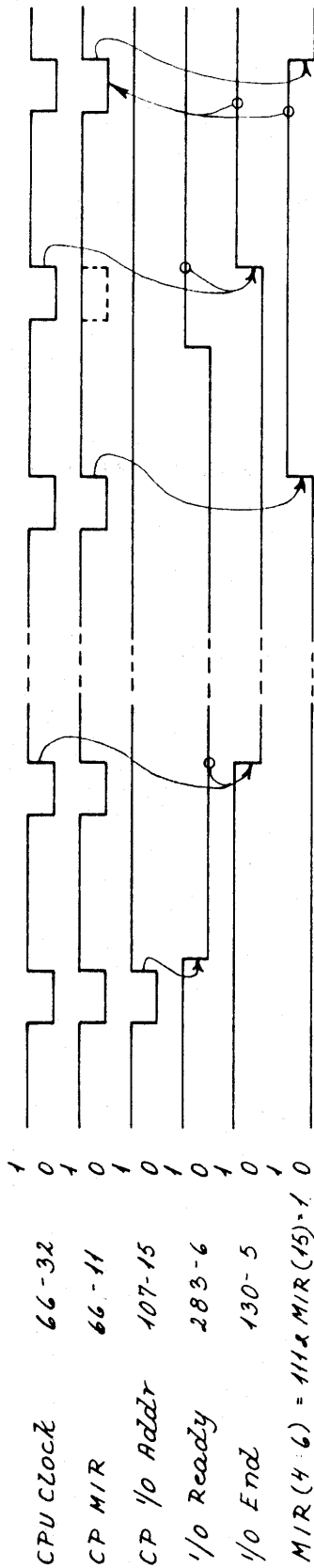
CPU 810
R12580

Timing Diagram for
Power Up and Control Store Parity Error

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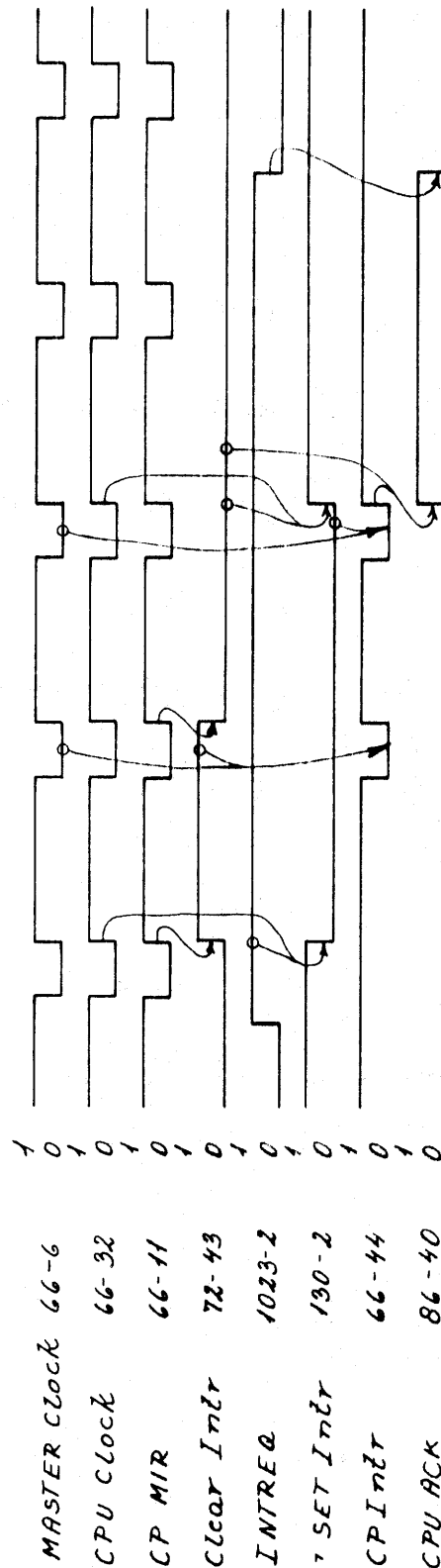
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I/O Synchronization



External Interrupt

Timing is shown for an external interrupt coincident with clear of an interrupt.



4. FUNCTIONAL DESCRIPTION.

Symbols and abbreviations used in the description are listed below.

(A)	Contents of A.
A(i)	Bit i in register A.
A(i:j)	Bits i to j including i and j in register A.
A(i,j)	Bits i and j in register A.
con	Concatenating operator.
ext	Extension operator. N ext P means P repeated N times.
+	Binary arithmetic addition.
-	Binary arithmetic 2's complement subtraction.
~,	Logical COMPLEMENT.
&	Logical AND.
!	Logical OR.
exor	Logical EXCLUSIVE OR.

When the logical operators are used on bit strings, the logical operation is performed on individual bits.

4.1 Data Paths.

4.1

The principal data paths in the CPU 810 are 24-bit wide and is shown on the block diagram on page 3 . An array of 6 Am 2901A 4-bit slice processing elements constitutes the kernel of the CPU 810 data path structure. It contains the General Registers (accumulators), the Q-register, and an arithmetic logic unit. The 2901 array receives data from external registers via the Source Bus (SBUS), which is a tri-state bus. Data to external registers is transferred via the Result Bus (RESBUS).

The following subsections gives a short description of the CPU 810 registers. The registers may be divided into the following groups: Registers located inside the 2901, external source registers connected to the SBUS, and external destination registers connected to the RESBUS.

4.1.1 General Registers.

4.1.1

The 16 General Registers in the 2901 are located in a 2-port RAM. The contents of 2 General Registers may simultaneously be accessed via the A-port, GRA, and the B-port, GRB. GRA and GRB may be used as inputs to the ALU and GRA may be transferred directly to the RESBUS. The General Registers may be loaded with the output from the ALU. A shift network at the input to the General Registers may pass or shift the ALU output 1 bit position left or right before it is loaded.

4.1.2 Q-Register.

4.1.2

The Q-register which is located in the 2901 may be used as an accumulator and as an extension to the General Registers in shift operations for shifting 48-bit operands. In the latter case Q holds the least significant 24-bit of the 48-bit operand. It is only possible to shift Q in conjunction with a General Register.

4.1.3 Scratchpad.

The Scratchpad (SCRATCHP) is an external register file with 16 24-bit words. It may be used as both source and destination, but not in the same microinstruction. When it is used as source the complement of the data loaded into the addressed location is transferred to the SBUS. The SBUS cannot be used in microinstructions where the SCRATCHP is used as destination because the SCRATCHP transfers data to it during part of the cycle.

4.1.4 Immediate Operand Register.

The Immediate Operand Register is a 24-bit source register. It may be loaded by means of an immediate operand microinstruction.

4.1.5 Sign Extension Module.

The Sign Extension Module (SIGNEXT) is a combinatorial array which may be addressed in the same way as a 24-bit source register. When it is addressed the contents of the RESBUS is transferred to the SBUS with sign extension as defined below.

$$SBUS(0:23) := 12 \text{ ext } RESBUS(12) \text{ con } RESBUS(12:23)$$

4.1.6 Half-Word Rotate Module.

The Half-Word Rotate Module (ROTATE) is a combinatorial array which may be addressed as a 24-bit source register. When it is addressed the two half-words on the RESBUS are exchanged and transferred to the SBUS as defined below.

$$SBUS(0:23) := RESBUS(12:23) \text{ con } RESBUS(0:11)$$

4.1.7 Data In Register.

4.1.7

The Data In Register (DATAIN) is a 24-bit source register used as buffer register for data received via the System Bus in input operations initiated by the CPU. The contents of the register is undefined from the start of an input operation until termination of the operation. If an input operation is terminated by a NACK or a TIME OUT DATAIN will be loaded with the current data on the System Bus.

4.1.8 Interrupt Level Register.

4.1.8

The Interrupt Level Register (INTRLEV) is an 8-bit source register. When the jump condition INTERRUPT = 1 INTRLEV contains the level of the interrupt with the highest priority. The contents of INTRLEV is transferred to the SBUS as defined below

SBUS(0:15) undefined

SBUS(16:23): = INTRLEV(0:7)

The assignment of the interrupt levels is defined in the table below. Level 0 has the highest priority.

<u>LEVEL</u>	<u>INTERRUPT SOURCE</u>
0	Unused
1	TCP input ready (TCPINRDY)
2	Single instruction (SINGLEINSTR)
3	OCP autoloading (RESTARTEN)
4	Remote autoloading (REMAUTOLOAD)
5	0.1 ms timer (10 KHZ clock)
6	Power low warning (PINT)
7	Interval timer
8:15	Device controllers

4.1.9 TCP Data Input Register.

The TCP Data Input Register (TCPDATAIN) is an 8-bit source register used as buffer register for data received from the Technicians Console.

The contents of TCPDATAIN is transferred to the SBUS as defined below.

SBUS(0:15) undefined
SBUS(16:23): = TCPDATAIN(0:7)

4.1.10 CPU Status Register.

The CPU Status Register (CPUT) is a 6-bit destination register which is used to hold bits (0:5) of the CPU Status Word. The register is loaded from the RESBUS as defined below.

MONITOR MODE: =	RESBUS(0)
ESCAPE MODE: =	RESBUS(1)
AFTER AM: =	RESBUS(2)
AFTER ESCAPE: =	RESBUS(3)
INTEGER MASK: =	RESBUS(4)
FLOATING POINT MASK: =	RESBUS(5)

The contents of the register is used for instruction decoding and as jump conditions.

4.1.11 I/O Address Register.

4.1.11

The I/O Address Register (I/O ADDR) is a 24-bit destination which is used to hold the I/O address during data transfers on the System Bus initiated by the CPU.

Addressing of I/O ADDR has two purposes. The register is loaded with the contents of the SBUS and a data transfer on the System Bus is initiated. A separate field in the microinstruction controls the direction of the data transfer. The contents of the register must not be altered during an I/O operation in progress.

4.1.12 Data Out Register.

4.1.12

The Data Out Register (DATAOUT) is a 24-bit destination register used as output buffer register for data to be transferred via the System Bus from the CPU to the addressed destination. Once an output operation has been started the contents of the register must not be altered before termination of the operation.

4.1.13 Control Output Register.

4.1.13

The Control Output Register (CONTROLOUT) is an 8-bit destination register which is used for different control purposes in the CPU. The register is loaded from the RESBUS as defined below.

$$\text{CONTROLOUT}(0:7) := \text{RESBUS}(16:23)$$

The contents of the register is used in the following way:

<u>BIT</u>	<u>CONTROL FUNCTION</u>
0	CPUSYSRST. Controls the SYSTEM RESET signal on the System Bus.
1	RUN. Controls the RUN lamp on the Operators Control Panel (OCP).
2	AUTOLOADING. Controls the AUTOLOAD lamp on the OCP.
3	SINGLEINSTR. Used for single instruction execution controlled from the Technicians Console (TCP). The signal generates a level 2 interrupt.
4	SETIVTIMER. The interval timer interrupt is set when the signal changes from 0 to 1.
5	TCPINACK. Acknowledge signal from CPU to TCP. The TCPDATAIN register is loaded with new data from the TCP when TCPINACK changes from 0 to 1.
6	TCPOUTRDY. Control signal from CPU to TCP. Used to indicate that data is available in the TCPDATAOUT register.
7	TSTSYNC. Used by the microdiagnostic routines for oscilloscope triggering in error loops.

4.1.14 TCP Data Out Register.

4.1.14

The TCP Data Out Register (TCPDATAOUT) is an 8-bit destination register used as buffer register for data to the TCP. The register is loaded from the RESBUS as defined below.

$$\text{TCPDATAOUT}(0:7) := \text{RESBUS}(16:23)$$

4.1.15 Instruction Register.

4.1.15

The Instruction Register (INSTRREG) is a 12-bit destination register. It is used to hold bits (0:11) of the RC8000 instruction which is being executed. The register is loaded from the RESBUS as defined below:

$$\begin{aligned} \text{FFIELD}(0:5) &:= \text{RESBUS}(0:5) \\ \text{WFIELD}(0:1) &:= \text{RESBUS}(6:7) \\ \text{RFIELD} &:= \text{RESBUS}(8) \\ \text{IFIELD} &:= \text{RESBUS}(9) \\ \text{XFIELD} &:= \text{RESBUS}(10:11) \end{aligned}$$

4.1.16 Micro Index Register.

4.1.16

The Micro Index Register (MIX) is a 12-bit destination register. The contents of MIX may be used as control store address in JUMP microinstructions.

4.1.17 Interrupt Register.

The Interrupt Register (INTR) is a 15-bit register in which interrupt requests are stored. INTR may be addressed as a destination register for clearing of interrupt requests. A microinstruction addressing INTR will clear the request at the level indicated by RESBUS(20:23). Requests at the levels (1:3) cannot be cleared in this way.

The INTR register may be addressed via the System Bus in order to set an interrupt request. Data bits (20:23) on the System Bus determines at which level the request will be set. Only interrupt requests at the levels 8 to 15 may be set from the System Bus.

4.2 Control Store Addressing.

The block diagram on page 5 shows the control store and the associated address paths. The Control Store (CS) is addressed via a 12-bit tri-state bus, the Control Store Address Bus (CSADDR). The contents of the addressed CS location is loaded into the Microinstruction Register (MIR), which holds the microinstruction during its execution. The next microinstruction to be executed is fetched from CS during the execution of the current microinstruction in order to minimize microinstruction cycle time. The CSADDR may be selected from a number of sources which are described in the following subsections.

4.2.1 Microinstruction Address Register.

4.2.1

The Microinstruction Address Register (MAR) is used for sequential addressing of control store locations. In each microcycle MAR is loaded with CSADDR + 1.

4.2.2 Subroutine Return Stack.

4.2.2

The Subroutine Return Stack (STACK) is a 4-word register file, which operates as a push-pop stack, i.e. a last in/first out (LIFO) structure. The STACK is used for saving of subroutine return addresses and for microprogram loop control. Associated with the STACK is a stack pointer (SP), which points at the word on the top of the STACK. The word on the top of the stack STACK(SP) may be transferred to CSADDR bus.

4.2.3 Micro Jump Address Register.

4.2.3

The Micro Jump Address Register (JUMP) may be used as control store address source in jump microinstructions. JUMP is loaded from CS in parallel with MIR and the contents of JUMP is identical to the contents of that part of MIR, which contains the jump address field.

4.2.4 Micro Index Register.

4.2.4

The Micro Index Register (MIX) may be used as CS address source in jump microinstructions. MIX is loaded from the RESBUS and may e.g. be used for table look-up in control store.

4.2.5 Instruction Decoding Table.

An RC8000 instruction is decoded and executed in two steps: Calculation of the effective address and execution of the function of the instruction. Microprogram start addresses for address calculation and instruction execution subroutines are stored in the Instruction Decoding Table (TABLE), which is a 256 words x 12 bits PROM. TABLE is divided into 2 blocks, 128 words for address calculation entries and 128 words for instruction execution entries. A 2-input multiplexer controlled from the microinstructions selects address inputs to TABLE as described below.

ADDRESS CALCULATION DECODING

<u>ADDRESS BIT</u>	<u>ADDRESS SOURCE</u>
0	= 0, controlled by MIR(3)
1	ESCAPE MODE
2	FFIELD(0)
3	FFIELD(1)
4	AFTER AM
5	RFIELD
6	XFIELD(0)
7	XFIELD(1)

INSTRUCTION EXECUTION DECODING

<u>ADDRESS BIT</u>	<u>ADDRESS SOURCE</u>
0	= 1, controlled by MIR(3)
1	ESCAPE MODE
2	FFIELD(0)
3	(1)
4	(2)
5	(3)
6	(4)
7	(5)

4.3 Microinstructions.

4.3

All microinstructions are 36 bits in length and the microinstruction repertoire comprises 8 different formats as shown in figure 4.1. The Microinstruction Register (MIR) holds the microinstruction during its execution. The execution time is 200 ns for all microinstruction formats.

4.3.1 Microinstruction Fields.

4.3.1

A microinstruction consists of a number of fields. This section describes the fields, which are common to several microinstructions. Fields referring to a single format are described in connection with that format.

4.3.1.1 P Field = MIR(0).

4.3.1.1

The P field contains the parity bit for the microinstruction. Odd parity is used. In case of a parity error the processor stops immediately and the indicator 'CONTROL STORE PARITY ERROR' on the PCBA front panel will be lit. MIR contains the faulty microinstruction, which is not executed. The CSADDR depends on the NEXT field of the faulty microinstruction. In order to proceed after control store parity error it is necessary to turn power off and then on again.

4.3.1.2 NEXT Field = MIR(1 : 3).

4.3.1.2

The NEXT field defines the control store address for the next microinstruction to be executed as described on the next page.

<u>NEXT</u>	<u>FUNCTION</u>
000	CSADDR: = MAR; MAR: = MAR+1 The next sequential microinstruction is executed.
001	Unused.
010	CSADDR: = MAR; SP: = SP+1; STACK(SP): = MAR; MAR: = MAR+1 The next sequential microinstruction is executed and its address is pushed on to the STACK. Is used for loop set-up.
011	CSADDR: = MAR; SP: = SP-1; MAR: = MAR+1 The next sequential microinstruction is executed and the address on the top of the STACK is removed (pop).
100	CSADDR: = STACK (SP); SP: = SP-1; MAR: = STACK (SP)+1 The address on the top of the STACK is selected as next address and is removed from the STACK. Is used for subroutine return.
101	TESTCOND=0: CSADDR: = STACK(SP); MAR: = STACK(SP)+1 TESTCOND=1: CSADDR: = MAR; SP: = SP-1; MAR: = MAR+1 Is used for microprogram loop control. If the selected condition (TESTCOND) is false top of STACK is selected as next microinstruction address and the loop is repeated. If TESTCOND is true the next sequential microinstruction is executed and top of STACK is removed (loop exit).
110	CSADDR: = TABLE (ADDR); SP: = SP+1; STACK(SP): = MAR; MAR: = TABLE(ADDR)+1 Is used to call subroutines for calculation of the effective address of an RC8000 instruction. See also point 4.2.5.

<u>NEXT</u>	<u>FUNCTION</u>
111	CSADDR: = TABLE(EXEC); SP: = SP+1; STACK(SP): = MAR; MAR: = TABLE(EXEC)+1 Used to call subroutines for execution of an RC8000 instruction. See also point 4.2.5.

4.3.1.3 FORM Field = MIR(4:6).

4.3.1.3

The FORM field defines the microinstruction format and thereby the usage of bits (10:35) of the microinstruction. See figure 4.1.

4.3.1.4 ALU DEST Field = MIR(7:9).

4.3.1.4

The ALU DEST field selects destination for the ALU output (F) and controls the shift networks for the General Registers and the Q register. In addition it selects data source for the RESBUS.

<u>ALU DEST</u>	<u>FUNCTION</u>
000	Q: = F; RESBUS: = F
001	RESBUS: = F
010	GRB: = F; RESBUS: = GRA
011	GRB: = F; RESBUS: = F
100	GRB con Q: = SHIN con F con Q(0:22); RESBUS: = F
101	GRB: = SHIN con F(0:22); RESBUS: = F
110	GRB con Q: = F(1:23) con Q con SHIN; RESBUS: = F
111	GRB: = F(1:23) con SHIN; RESBUS: = F

SHIN is shift input defined by SI field.

4.3.1.5 ALU OP Field = MIR(10:12).

The ALU OP field selects the two operands, R and S, for the ALU.

<u>ALU OP</u>	<u>OPERAND R</u>	<u>OPERAND S</u>
000	GRA	Q
001	GRA	GRB
010	ZERO	Q
011	ZERO	GRB
100	ZERO	GRA
101	SBUS	GRA
110	SBUS	Q
111	SBUS	ZERO

4.3.1.6 ALU FUNC Field = MIR(13:15).

The ALU can perform three arithmetic and five logic functions controlled by the ALU FUNC field. Cin is the carry input to the least significant position of the ALU.

<u>ALU FUNC</u>	<u>ALU FUNCTION</u>
000	$R + S + \text{Cin}$
001	$-R + S - 1 + \text{Cin}$
010	$R - S - 1 + \text{Cin}$
011	$R \div S$
100	$R \& S$
101	$\neg, R \& S$
110	$R \text{ exor } S$
111	$\neg, (R \text{ exor } S)$

4.3.1.7 C Field = MIR(16:17).

4.3.1.7

The C field controls the carry input to the least significant position, bit (23), of the ALU.

<u>C</u>	<u>CARRY INPUT, Cin</u>
00	0
01	1
10	CARRY
11	ADDCOND

4.3.1.8 I/O Field = MIR(18:19).

4.3.1.8

The I/O field controls the data transfer direction on the System Bus, when the CPU is busmaster. In addition it may specify validity check of the I/O ADDRESS before an I/O operation is initiated.

<u>I/O</u>	<u>I/O FUNCTION</u>
00	READ
01	READ if I/O ADDRESS $\geq$ 8
10	WRITE
11	WRITE if I/O ADDRESS $\geq$ 8

READ means data transfer from slave to CPU and WRITE means data transfer from CPU to slave.

4.3.1.9 DEST REG Field = MIR(20:23).

The register addressed by the DEST REG field is loaded with the contents of the RESBUS.

<u>DEST REG</u>	<u>REGISTER</u>
0000	No load
0001	CPU status
0010	I/O Address, Start I/O
0011	Data Out
0100	Control Output
0101	TCP Data Out
0110	Instruction Register
0111	Micro Index Register
1xxx	Interrupt Register

x = Don't care.

4.3.1.10 SOURCE REG Field = MIR(24:27).

The contents of the register addressed by the SOURCE REG field is transferred to the SBUS.

<u>SOURCE REG</u>	<u>REGISTER</u>
0000	Immediate Operand
0001	Sign Extension
0010	Half-Word Rotate
0011	Data In
0100	Interrupt Level
0101	TCP Data In

Remaining addresses are unused.

4.3.1.11 SPADDR Field = MIR(24:27).

4.3.1.11

The SPADDR field addresses 1 of the 16 words in the Scratchpad file. The microinstruction format determines whether the Scratchpad is used as source or destination.

4.3.1.12 A Field = MIR(28:31).

4.3.1.12

The A field addresses 1 of the 16 General Registers, GRA. The addressed register may only be used as source and the usage is controlled by the ALU DEST and ALU OP fields.

4.3.1.13 B Field = MIR(32:35).

4.3.1.13

The B field addresses 1 of the 16 General Registers, GRB. The addressed register may be used as both source and destination. The usage is controlled by the ALU DEST and ALU OP fields.

4.3.1.14 T Field = MIR(18).

4.3.1.14

The T field is used in connection with the condition select field, COND SEL, to specify whether the true or the complemented value of the selected condition, SELCOND, is used as test condition, TESTCOND.

T = 0: TESTCOND = -, SELCOND

T = 1: TESTCOND = SELCOND

4.3.1.15 COND SEL Field = MIR(19:23).

The COND SEL field is used to select 1 of 32 condition bits for control of conditional jumps and microprogram loops.

<u>COND SEL</u>	<u>SELECTED CONDITION, SELCOND</u>
00 000	0
00 001	NNEG (F >= 0)
00 010	NZERO (F < > 0)
00 011	OVFL (arithmetic overflow)
00 100	CARRY (Carry from ALU bit(0))
00 101	NORM (RESBUS(0) < > RESBUS(1))
00 110	Unused
00 111	Unused
01 000	MONITOR MODE
01 001	ESCAPE MODE
01 010	AFTER AM
01 011	AFTER ESCAPE
01 100	INTEGER MASK
01 101	FLOATING POINT MASK
01 110	IFIELD
01 111	LINK (WFIELD(0) < > WFIELD(1))
10 000	-, MEMADDR (I/O ADDR < 8)
10 001	-, WADDR (I/O ADDR < 0 : I/O ADDR >= 8)
10 010	ODD (I/O ADDR(23))
10 011	Unused
10 100	BUS ERROR
10 101	BUS TIMEOUT
10 110	BUS NACK
10 111	BUS PARITY
11 000	INTERRUPT
11 001	-, TCPINRDY
11 010	TPACK (TCP OUT ACK)
11 011	RESTART ENABLE (-, OCP AUTOLOAD)
11 100	SHORT (TEST MODE switch SHORT)
11 101	TSTON (TEST switch ON)
11 110	PLOW (Power low warning)
11 111	Unused

It should be noted that the conditions NNEG, NZERO, OVFL, CARRY, and NORM are updated by all microinstruction formats with the exception of formats 0 and 7. The above mentioned conditions are delayed one microcycle due to buffering, they may therefore be tested by the microinstruction following the microinstruction that generates the condition.

4.3.1.16 SI Field = MIR(24:25).

4.3.1.16

The SI field controls the input (SHIN) to the vacated position in shift microinstructions. SHIN depends on both the SI field and the shift direction.

<u>SI</u>	<u>SHIFT INPUT, SHIN</u>
00	0
01	SHLINK (shift link)
10	Right shift: ADDCOND Left shift: SIGN EXTENSION
11	Unused

SIGN EXTENSION requires that the ALU OP field specifies an arithmetic operation.

4.3.1.17 TST Field = MIR(26:27).

4.3.1.17

The TST field controls ADDCOND and DIVSIGN, which are conditions intended to be used in multiply and divide microinstructions. These conditions are only affected by format 4, 5, and 6 microinstructions.

FORMAT 0: Load Immediate

0 1		3 4		6 7		9 10		11 12		35																					
P	NEXT			FORM			0 0 0			0 0 1			0 0			IMMEDIATE OPERAND															

FORMAT 1: Load Scratchpad

0	1	3	4	6	7	9	10	12	13	15	16	17	18	23	24	27	28	31	32	35								
P	NEXT			FORM			ALU DEST			ALU OP			ALU FUNC			C	0 0 0 0 0 0			SPADDR			A			B		

FORMAT 2: Read Scratchpad/Load Register

0	1	3	4	6	7	9	10	12	13	15	16	17	18	19	20	23	24	27	28	31	32	35							
P	NEXT			FORM 0 1 0			ALU DEST			ALU OP			ALU FUNC			C	I/O	DEST REG			SPADDR			A			B		

FORMAT 3: Read/Load Register

0	1	3	4	6	7	9	10	12	13	15	16	17	18	19	20	23	24	27	28	31	32	35	
P	NEXT		FORM 0 1 1		ALU DEST		ALU OP		ALU FUNC		C	I/O	DEST REG		SOURCE REG			A			B		

FORMAT 4: Shift

0	1	3	4	6	7	9	10	12	13	15	16	17	18	19	23	24	25	26	27	28	31	32	35			
P	NEXT			FORM 1 0 0			ALU DEST			ALU OP			ALU FUNC			C	T	COND SEL			SI	TST	A		B	

FORMAT 5: Multiply

0	1	3	4	6	7	9	10	12	13	15	16	17	18	19	23	24	27	28	31	32	35							
P	NEXT			FORM 1 0 1			ALU DEST			ALU OP			ALU FUNC			C	T	COND SEL			SI	TST	A			B		

FORMAT 6: Divide

0	1	3	4	6	7	9	10	12	13	15	16	17	18	19	23	24	27	28	31	32	35					
P	NEXT			FORM 1 1 0			ALU DEST			ALU OP			ALU FUNC			C	T	COND SEL			SI	TST	A		B	

FORMAT 7: Conditional Jump

0	1	3	4	6	7	9	10	14	15	16	17	18	19	23	24	35								
P	NEXT			FORM						W			S	X	T	COND SEL		JUMP ADDR						
				1 1 1			0 0 0			0 0 0 0 0														

Figure 4.1 Microinstruction Formats.

<u>TST</u>	<u>FUNCTION</u>
00	CONDITIONS UNCHANGED
01	ADDCOND: = -, Q(23), ALU DEST = 100
10	ADDCOND: = F(0) exor -, DIVSIGN
11	DIVSIGN: = F(0)

4.3.2 Microinstruction Formats.

4.3.2

The following subsections gives a short description of the characteristics of each of the eight microinstruction formats shown on fig.

4.1. The more detailed function of a microinstruction will normally appear from the description of the fields in section 4.3.1.

4.3.2.1 Format 0: Load Immediate.

4.3.2.1

The Immediate Operand Register (IMOP) is loaded with the contents of the 24-bit IMMEDIATE OPERAND field of the microinstruction.

$$\text{IMOP} := \text{MIR}(12:35)$$

The execution of this microinstruction does not change conditions.

4.3.2.2 Format 1: Load Scratchpad.

4.3.2.2

This format operates on the General Registers, the Q-register, and the Scratchpad. The addressed Scratchpad location is loaded with the contents of the RESBUS.

$$\text{SCRATCHP}(\text{SPADDR}) := \text{RESBUS}$$

Shifts cannot be specified with this format.

$$\text{ALU DEST} = 000, 001, 010, \text{ or } 011.$$

4.3.2.3 Format 2: Read Scratchpad/Load Register.

This microinstruction type operates on the General Registers, the Q-register, the Scratchpad, and the Destination Registers. The complement of the contents of the addressed Scratchpad location is transferred to the SBUS. The addressed Destination Register is loaded with the contents of the RESBUS.

SBUS : = -, SCRATCHP (SPADDR)

Register (DEST REG) : = RESBUS

Shifts cannot be specified with this format.

ALU DEST = 000, 001, 010, or 011.

4.3.2.4 Format 3: Read/Load Register.

This format operates on: General Registers, Q-register, Source Registers, and Destination Registers. The contents of the addressed Source Register is transferred to the SBUS. The addressed Destination Register is loaded with the contents of the RESBUS.

SBUS : = Register (SOURCE REG)

Register (DEST REG) : = RESBUS

Shifts cannot be specified with this format.

ALU DEST = 000, 001, 010, or 011.

4.3.2.5 Format 4: Shift.

4.3.2.5

The microinstruction operates on the General Registers and the Q-register, and is primarily intended to be used for shift operations. As the format includes the T and COND SEL fields it may be used with NEXT = 101 (loop return).

4.3.2.6 Format 5: Multiply.

4.3.2.6

This format operates on the General Registers and the Q-register, and is primarily intended to be used for multiplication routines. Selection of the ALU operands are controlled by the ALU OP field and by ADDCOND.

<u>ALU OP</u>	<u>ADDCOND</u>	<u>OPERAND R</u>	<u>OPERAND S</u>
0X0	0	GRA	Q
	1	ZERO	Q
0X1 x)	0	GRA	GRB
	1	ZERO	GRB
1X0	0	ZERO	GRA
	1	SBUS	Q
1X1	0	SBUS	GRA
	1	SBUS	ZERO

x) 'Normal' value for multiplication.

4.3.2.7 Format 6: Divide.

The microinstruction operates on the General Registers and the Q-register, and is primarily intended to be used for division routines. The ALU function is controlled by the ALU FUNC field and by ADDCOND.

<u>ALU FUNC</u>		<u>ADDCOND</u>	<u>ALU FUNCTION</u>
00X	x)	0	$R + S + \text{Cin}$
		1	$- R + S - 1 + \text{Cin}$
01X		0	$R - S - 1 + \text{Cin}$
		1	$R \div S$
10X		0	$R \& S$
		1	$-, R \& S$
11X		0	$R \text{ exor } S$
		1	$-, (R \text{ exor } S)$

x) 'Normal' value for division.

4.3.2.8 Format 7: Conditional Jump.

This microinstruction executes conditional jumps and conditional subroutine calls. In addition it may be used for synchronization with I/O operations on the System Bus. The function of the microinstruction is controlled by the W, S, and X fields, MIR (15, 16, 17), which respectively specifies: I/O synchronization, subroutine call, and jump address equal to contents of MIX.

W = 0: No synchronization

W = 1: The execution of the microinstructions is delayed (clock stopped) until I/O is ready. Synchronization cannot be specified in a microinstruction immediately following the microinstruction starting an I/O operation. I/O Ready is delayed one clock period.

The selected condition (TEST COND) determines how the next microinstruction address is derived.

- TESTCOND = 0: Next address selected by NEXT field as specified in 4.3.1.2.
- TESTCOND = 1: A jump is executed and next address is controlled by S and X fields as specified below.

S, X FUNCTION for TESTCOND = 1

- 00 CSADDR: = JUMP ADDR; MAR: = JUMP ADDR + 1
- 01 CSADDR: = MIX; MAR: = MIX + 1
- 10 CSADDR: = JUMP ADDR; SP: = SP + 1;
 STACK (SP): = MAR; MAR: = JUMP ADDR + 1
- 11 CSADDR: = MIX; SP: = SP + 1; STACK (SP): = MAR
 MAR: = MIX + 1

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5.

LOGIC DIAGRAMS and SIGNAL DESCRIPTIONS.

5.

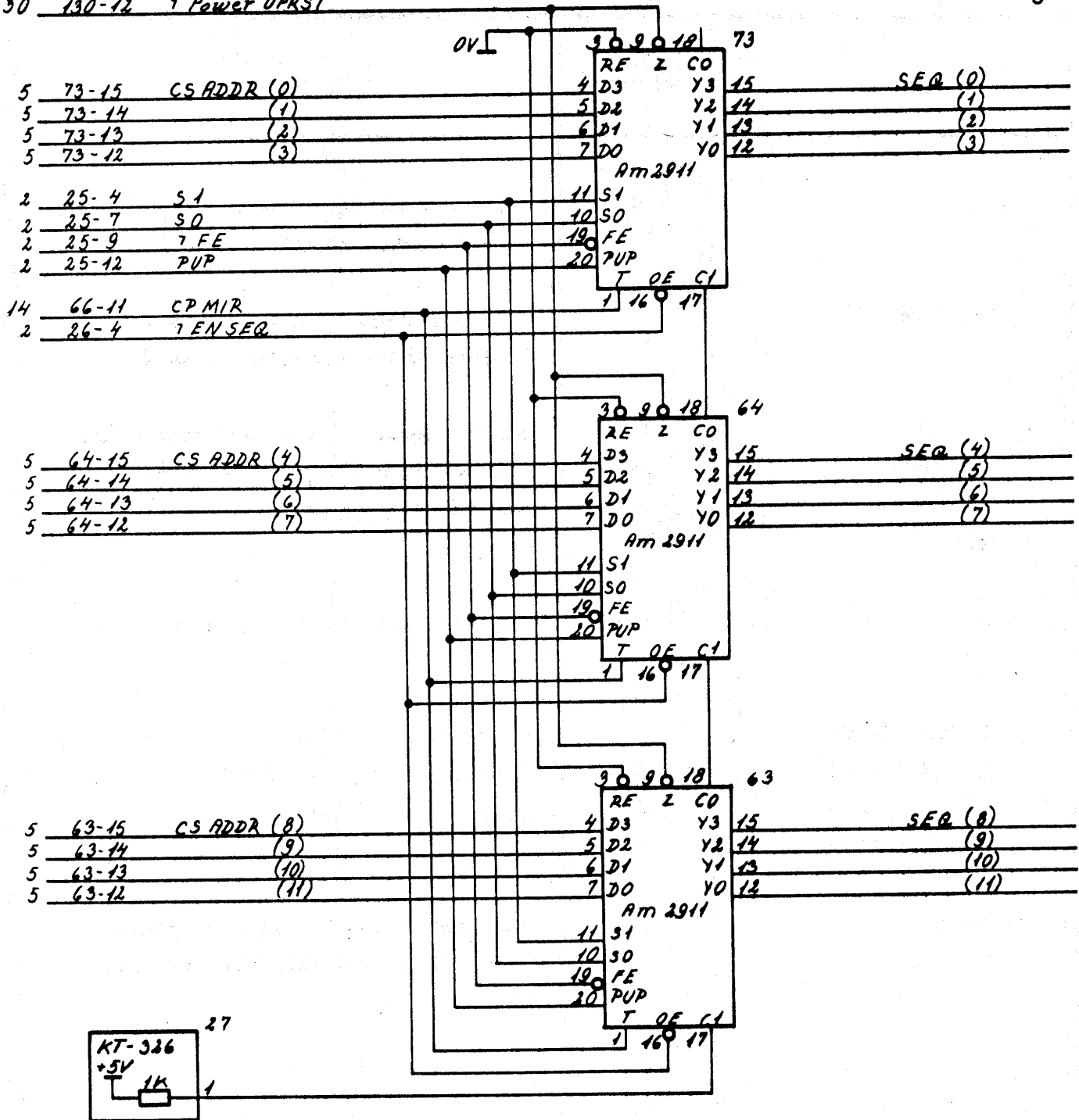
The logic diagrams are placed on the right hand pages (odd page numbers). The signal description belonging to a diagram is placed on the corresponding left hand page.

The signal description consists of a listing of the signals, which are generated on the logic diagram and which are transferred to other diagrams. For each signal is indicated on which diagrams it is used, and its function is shortly described.

References between logic diagrams use the diagram number placed in the lower right hand corner of the diagram.

SIGNAL		DESTI- NATION	DESCRIPTION
SEQ (0:11)		5	Control Store Address from Microprogram Sequencer. Tri-state outputs.
Unit			1A

30 130-12 1 Power UPRST

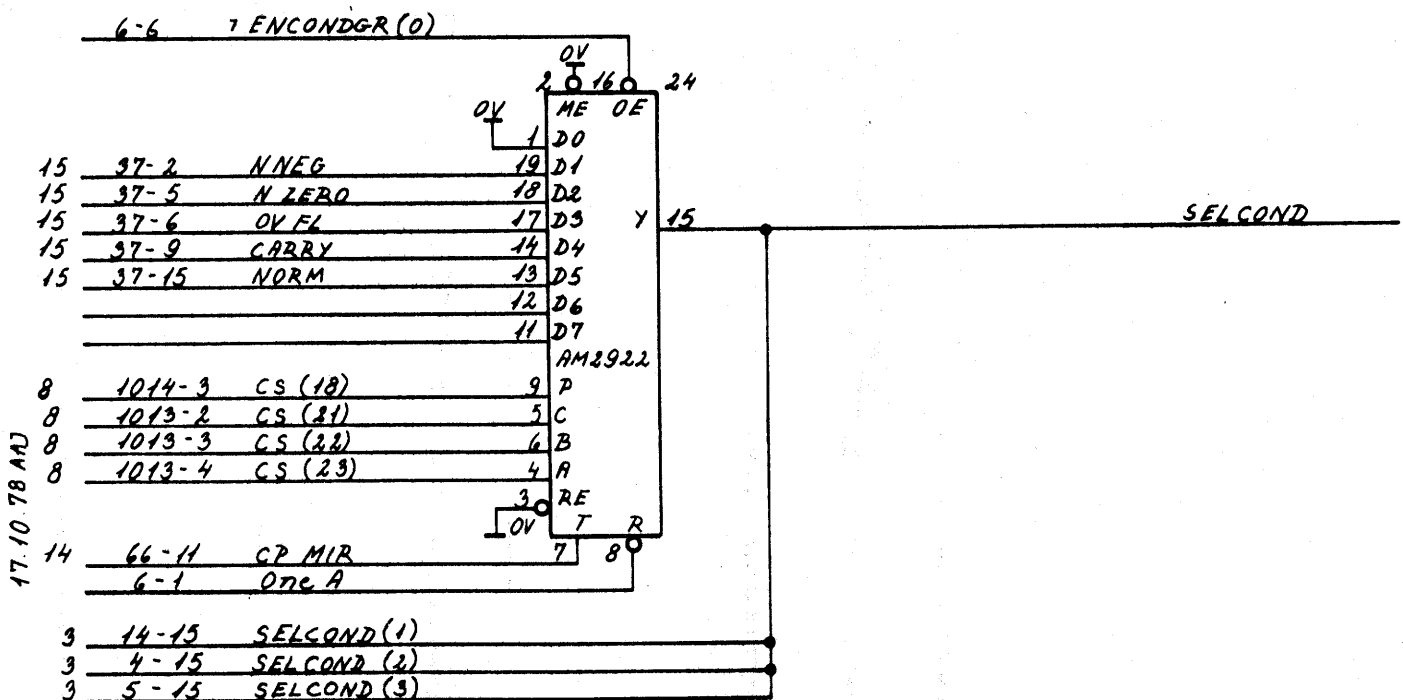
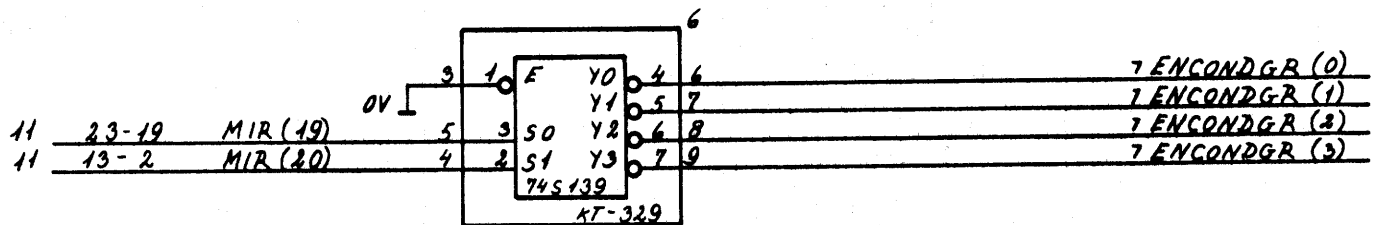
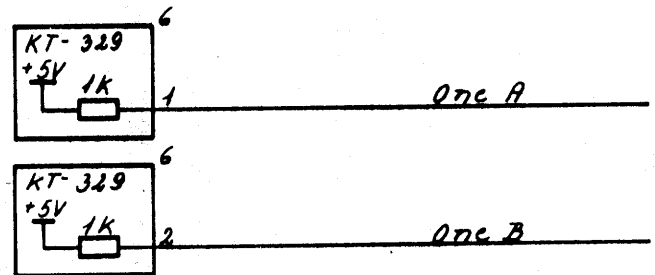
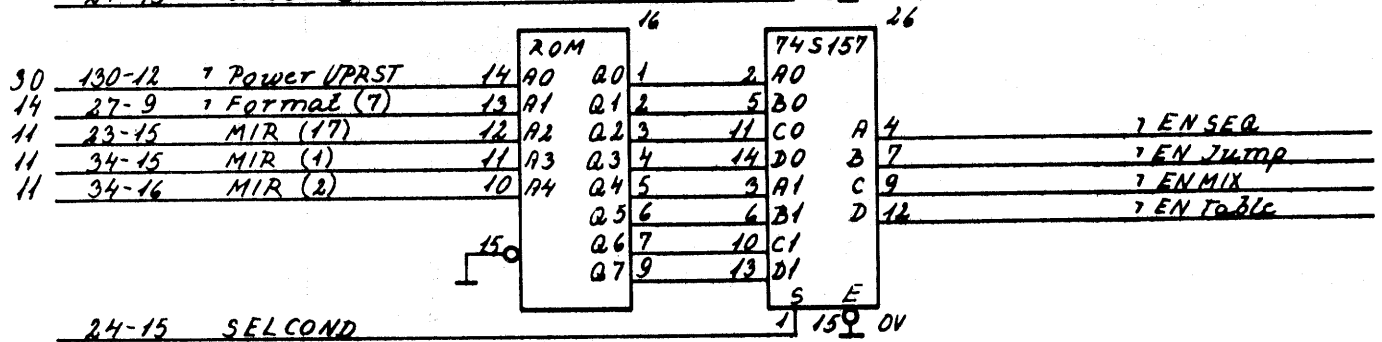
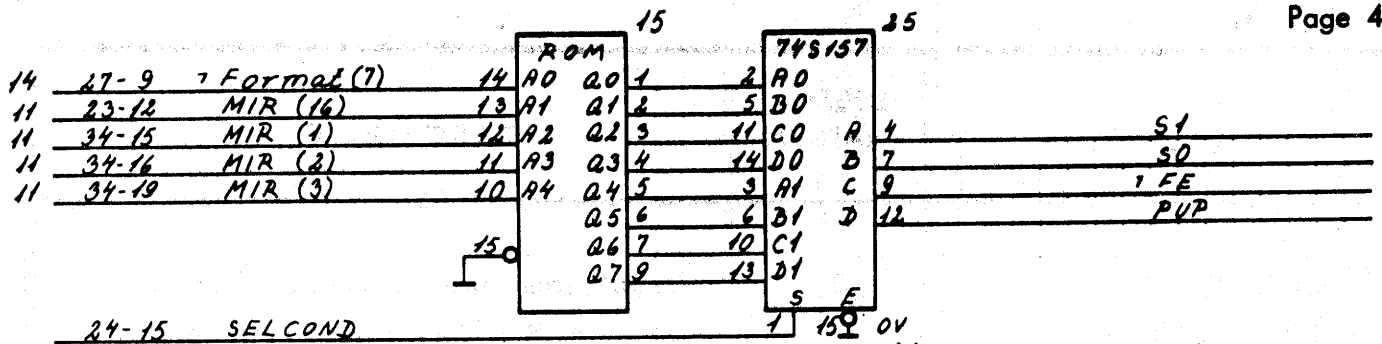


17.10.78 ANJ

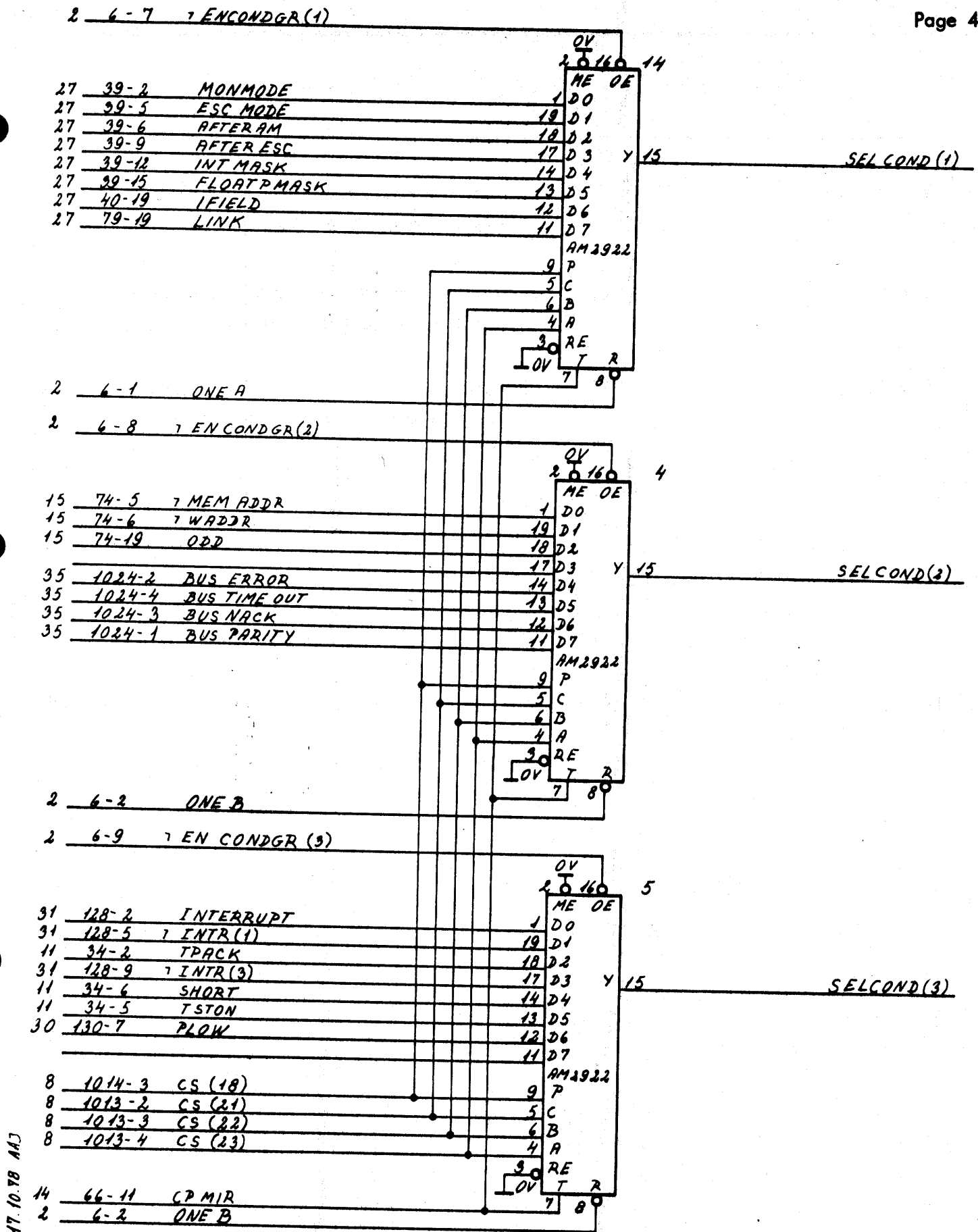
SIGNAL		DESTINATION	DESCRIPTION
S1, S0		1	Control signals for microprogram sequencer. Selects address source.
-, FE, PUP		1	Control signals for microprogram sequencer. Controls the subroutine return stack.
-, ENSEQ		1	Enable signals which control the address
-, ENJUMP		4	sources for the control store address bus,
-, ENMIX		4	CSADDR (0:11).
-, ENTABLE		4	
ONEA		1,3	Logic one generators for unused inputs.
ONEB		3	
-, ENCONDGR (0)		2	Enable signals for jump condition selectors.
-, ENCONDGR (1)		3	Selects respectively conditions (0:7), (8:15),
-, ENCONDGR (2)		3	(16:23), and (24:31).
-, ENCONDGR (3)		3	
SELCOND		2	The jump condition selected by micro-instruction bits (18:23). Tri-state output.

Unit

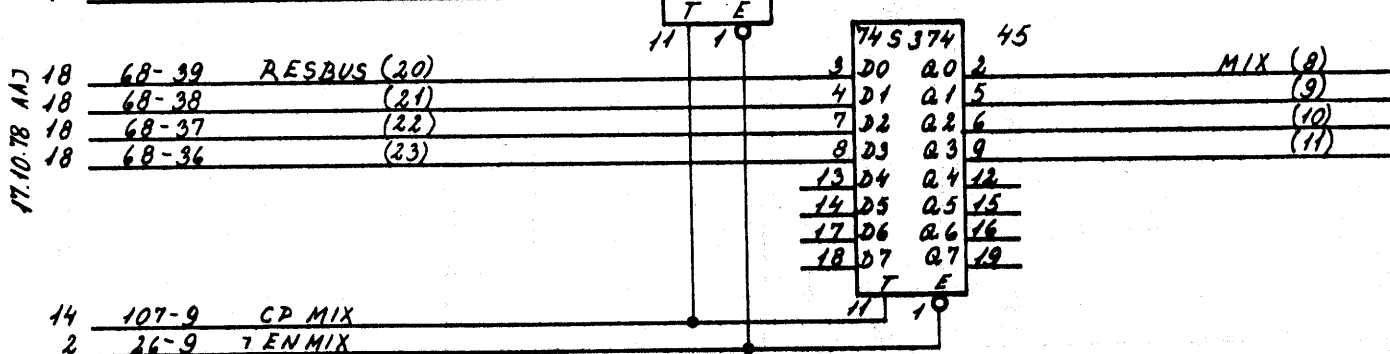
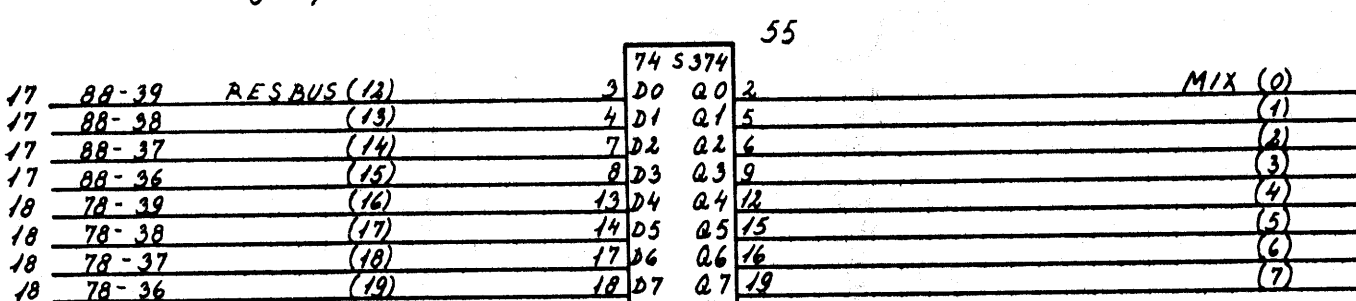
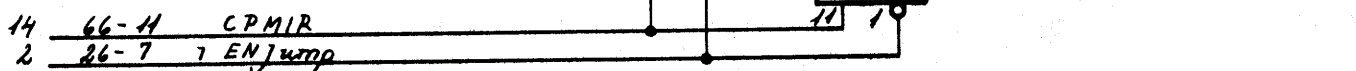
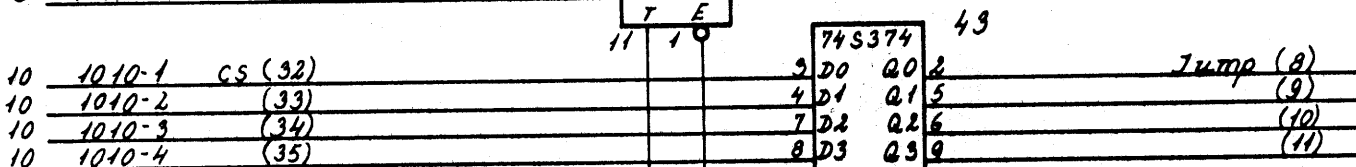
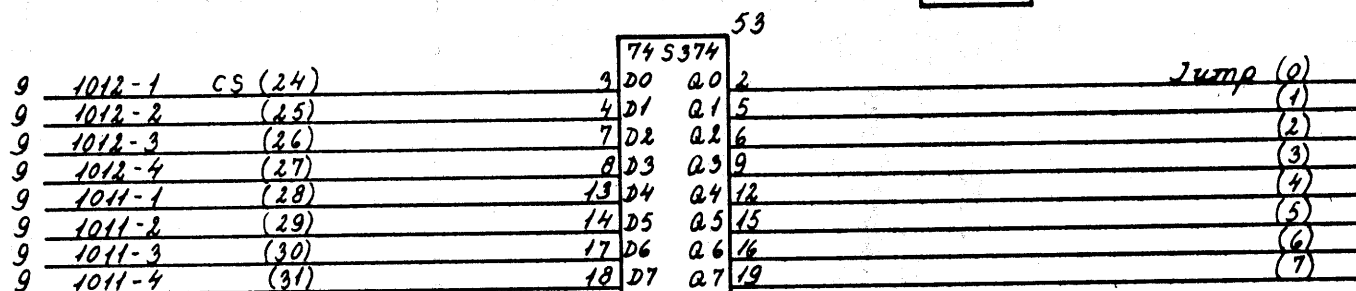
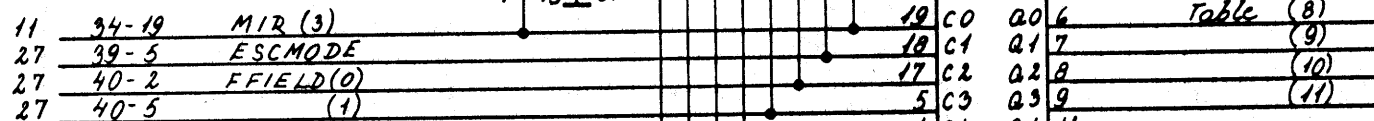
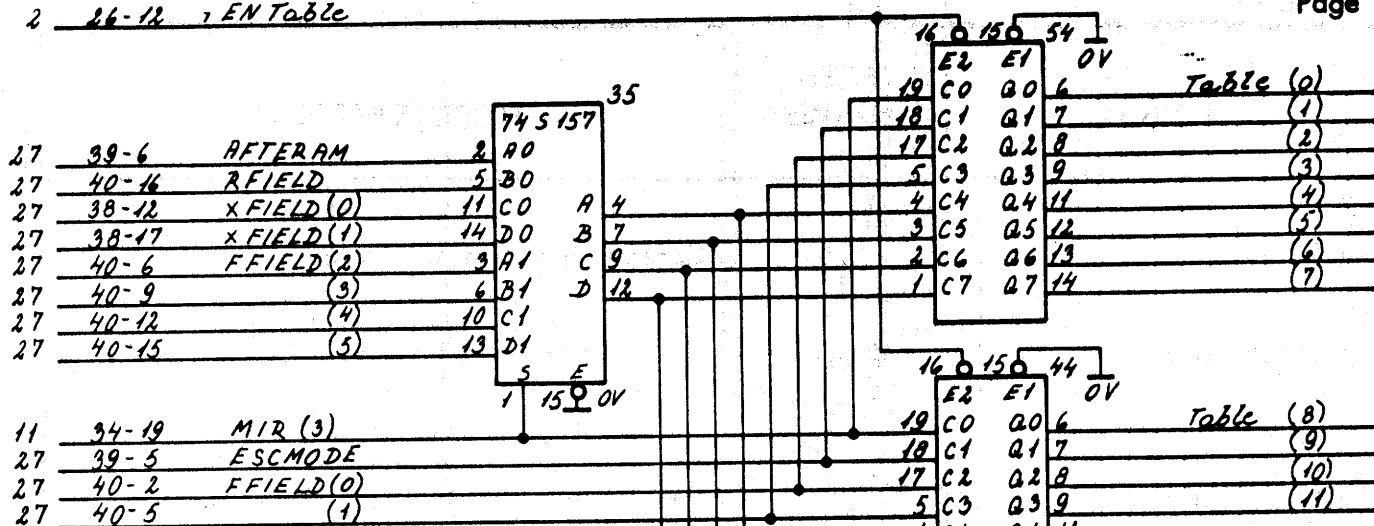
2A



SIGNAL		DESTI- NATION	DESCRIPTION
SELCOND (1)		2	Outputs from jump condition selectors for conditions 8 : 15, 16 : 23, and 24 : 31. Tri-state outputs.
SELCOND (2)		2	
SELCOND (3)		2	
Unit			
		3A	



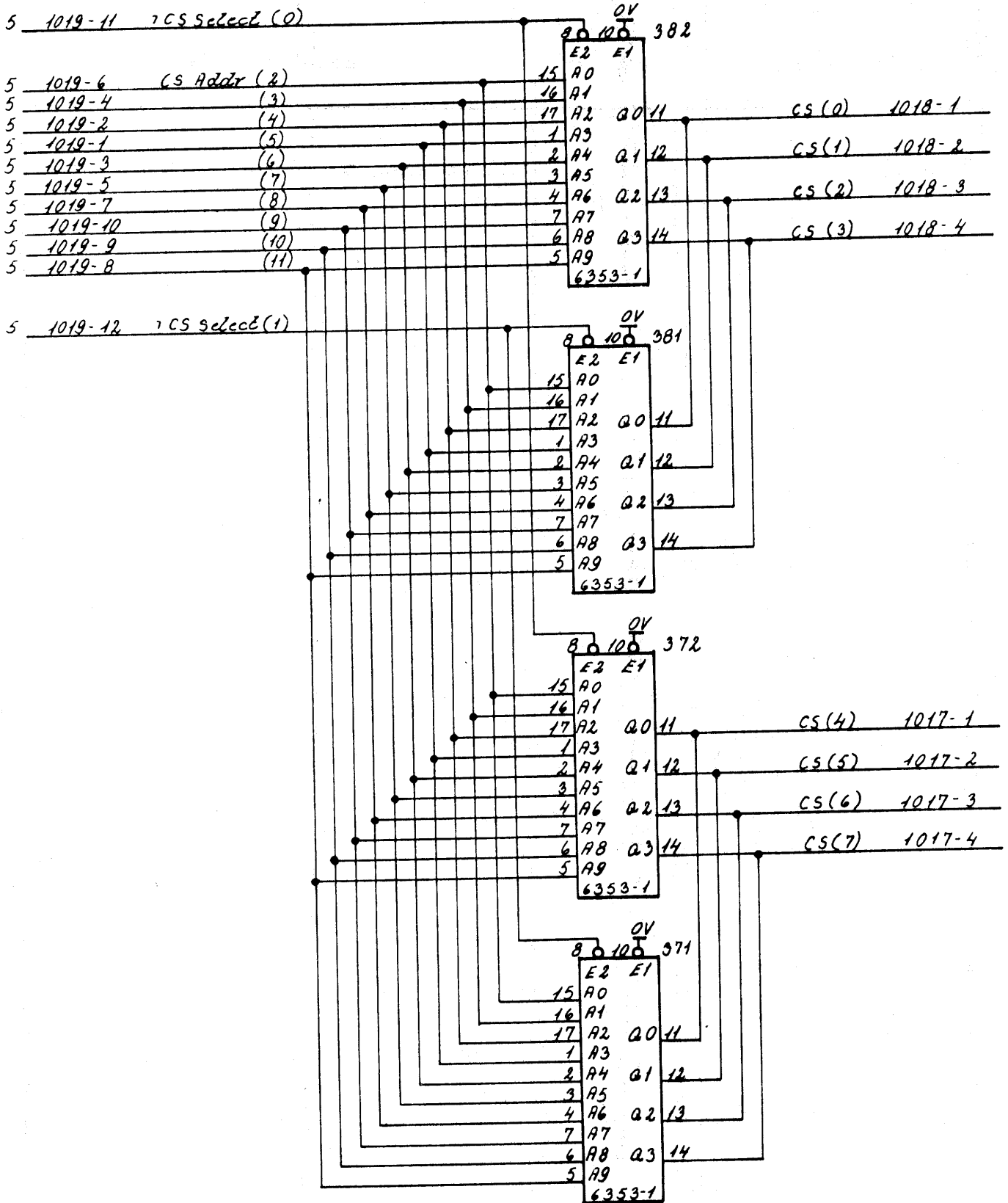
SIGNAL		DESTI- NATION	DESCRIPTION
TABLE (0:11)		5	Control store address from instruction de- coding table. Tri-state outputs.
JUMP (0:11)		5	Control store address from microprogram jump address register. Tri-state outputs.
MIX (0:11)		5	Control store address from microprogram index register. Tri-state outputs.
Unit			
		4A	



SIGNAL	DESTI- NATION	DESCRIPTION
CSADDR (0:1)	1,4,5	Control store address, bits (0:1)
CSADDR (2:11)	1,4,6,7 8,9,10	Control store address, bits (2:11)
-, CSSELECT (0)	6,7,8 9,10	Enable signal for control store addresses (0:1023)
-, CSSELECT (1)	6,7,8 9,10	Enable signal for control store addresses (1024:2047).
Unit		
5A		



SIGNAL		DESTI- NATION	DESCRIPTION
CS (0:7)		11	Control store, bits (0:7)
Unit			
			6A



17.10.78 AAJ

CPU 810

Control Store, BITS (0-7)

R12370

SIGNAL	DESTI- NATION	DESCRIPTION
CS (8:15)	11	Control store, bits (8:15)
Unit		

7A

5 1019-11 7 CS Select (0)

5 1019-6 CS Addr (2)

5 1019-4 (3)

5 1019-2 (4)

5 1019-1 (5)

5 1019-3 (6)

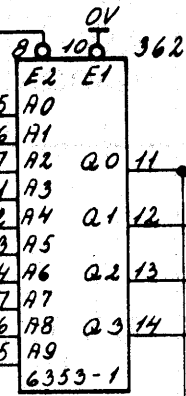
5 1019-5 (7)

5 1019-7 (8)

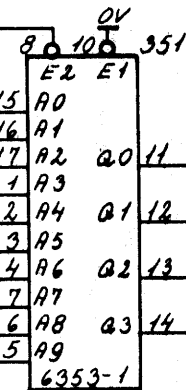
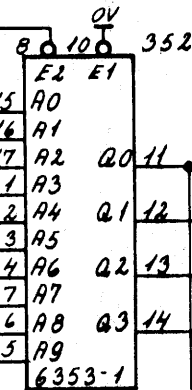
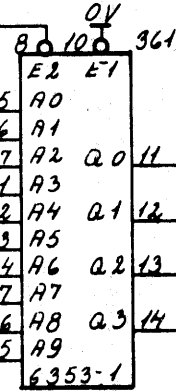
5 1019-10 (9)

5 1019-9 (10)

5 1019-8 (11)



5 1019-12 7 CS Select (1)



47-10-78 AAJ

SIGNAL	DESTI- NATION	DESCRIPTION
CS (16:17)	11	Control store, bits (16:17)
CS (18)	2, 3, 11	Control store, bit (18)
CS (19:20)	11	Control store, bits (19:20)
CS (21:23)	2, 3, 11	Control store, bits (21:23)
Unit		
8A		

5 1019-11 7CS Select (0)

5 1019-6 CS Addr (2)

5 1019-4 (3)

5 1019-2 (4)

5 1019-1 (5)

5 1019-3 (6)

5 1019-5 (7)

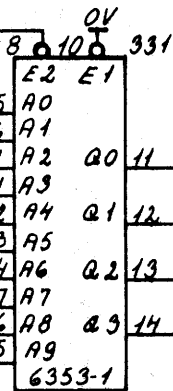
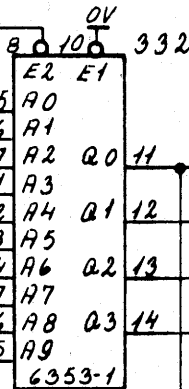
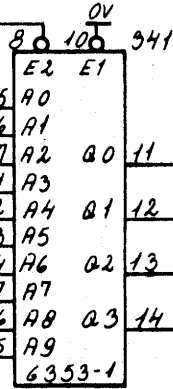
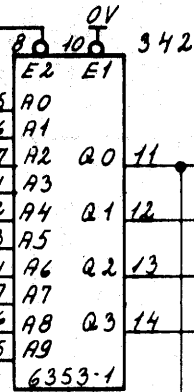
5 1019-7 (8)

5 1019-10 (9)

5 1019-9 (10)

5 1019-8 (11)

5 1019-12 7CS Select (1)



17-10 78 AAJ

CPU810

Control Store, BITS (16-23)

R 12372

SIGNAL		DESTI- NATION	DESCRIPTION
CS (24:31)		4,11	Control store, bits (24:31)
Unit			
			9A

5 1019-11 1 CS Select (0)

5 1019-6 CS Addr (2)

5 1019-4 (3)

5 1019-2 (4)

5 1019-1 (5)

5 1019-3 (6)

5 1019-5 (7)

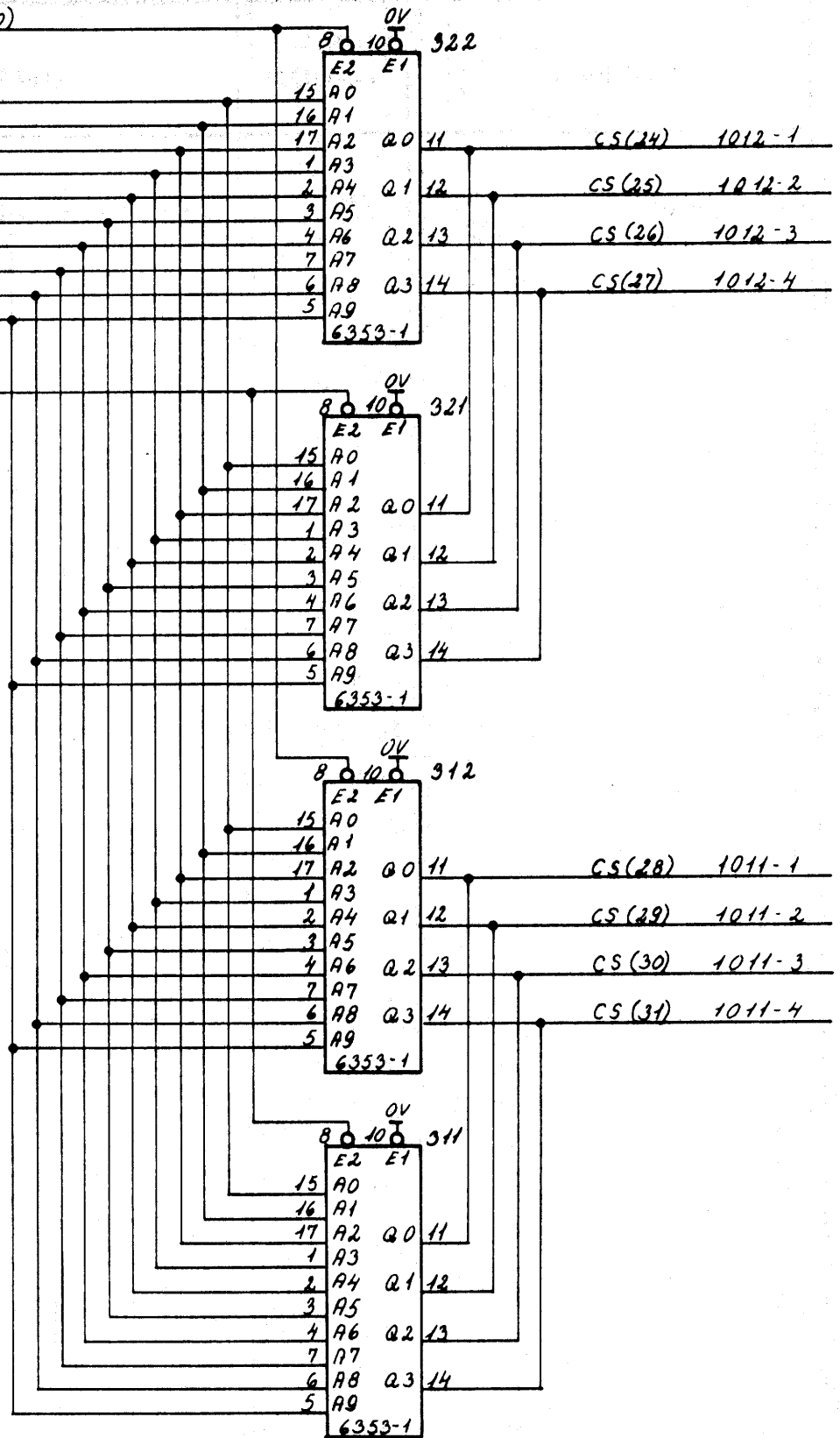
5 1019-7 (8)

5 1019-10 (9)

5 1019-9 (10)

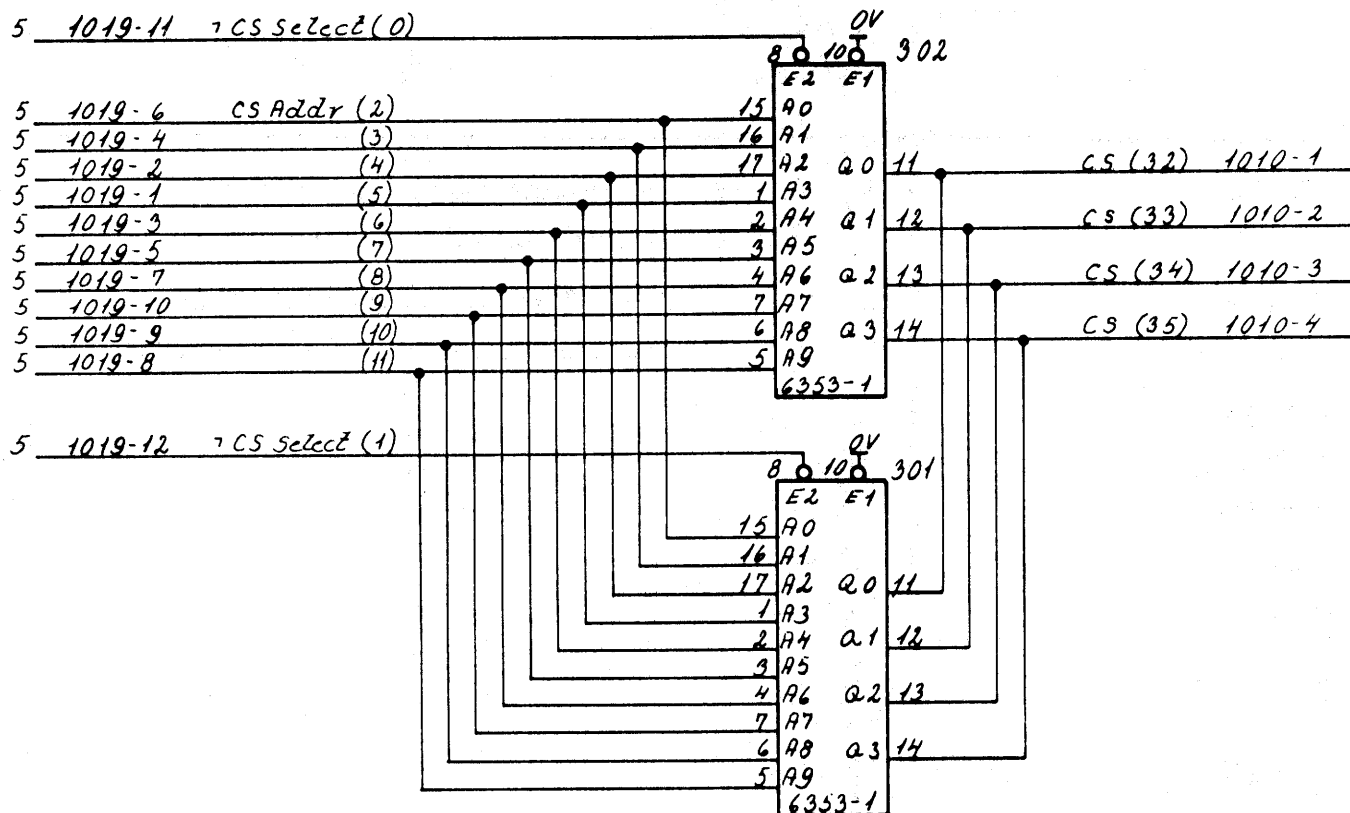
5 1019-8 (11)

5 1019-12 1 CS Select (1)



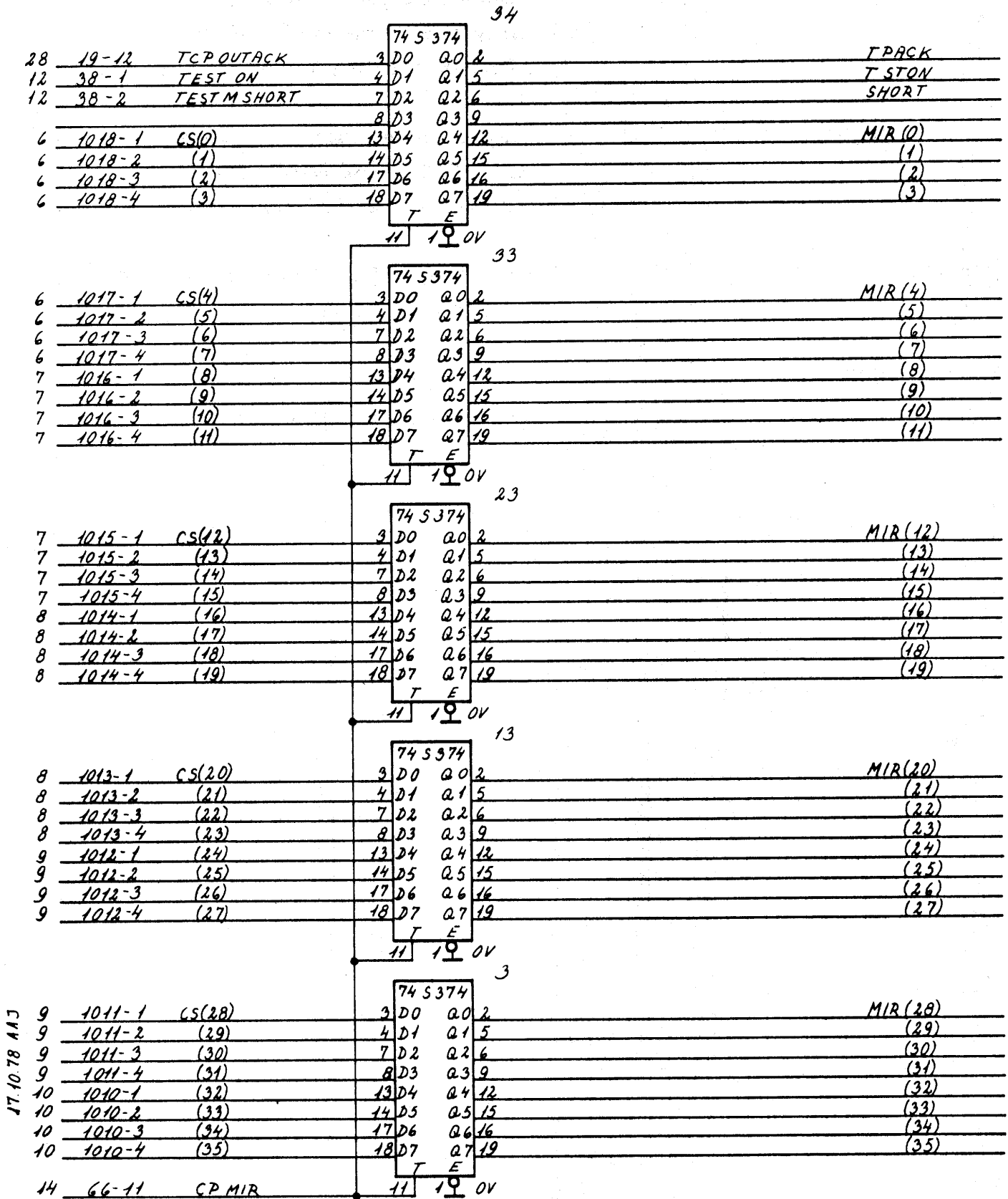
17 10.78 AAJ

SIGNAL		DESTINATION	DESCRIPTION
CS (32:35)		4,11	Control store, bits (32:35)
Unit			
			10A

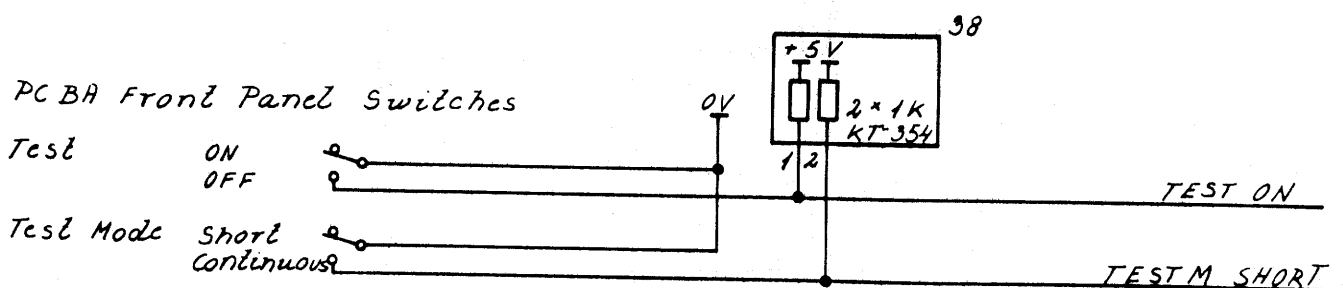
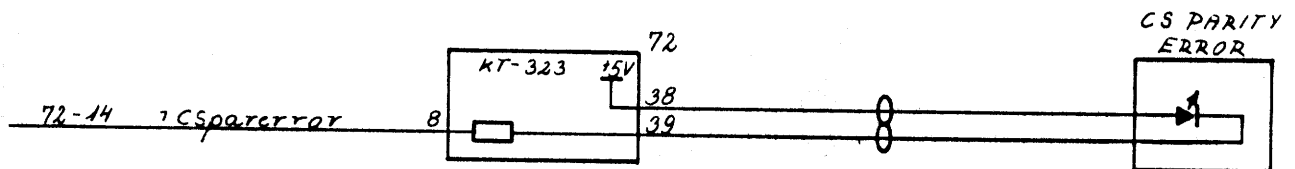
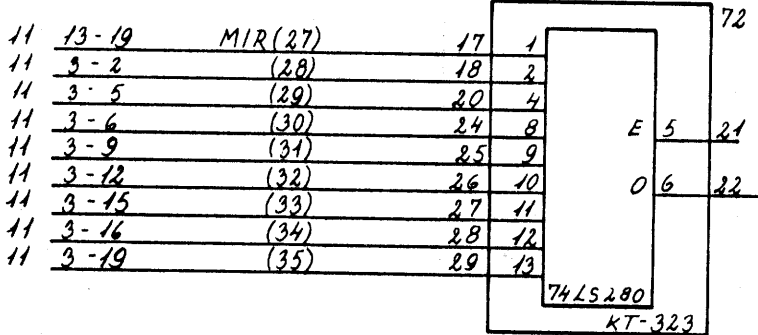
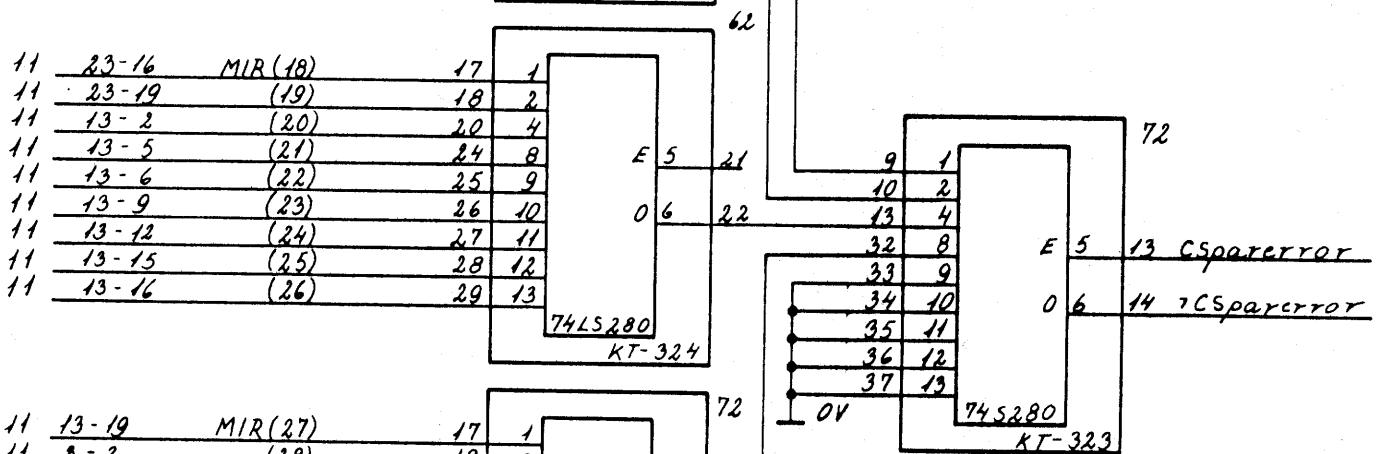
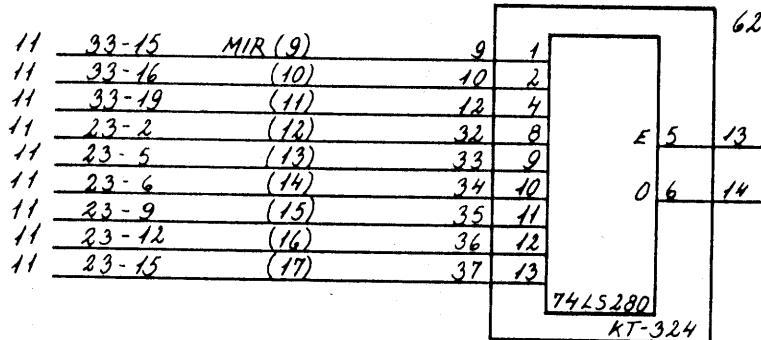
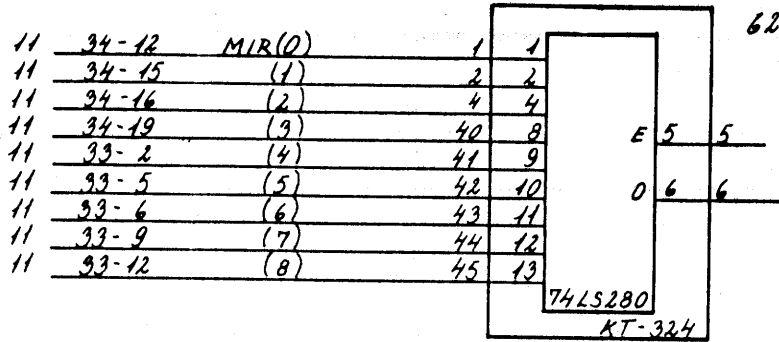


17.10.78 AAJ

SIGNAL		DESTI- NATION	DESCRIPTION
TPACK		3	Acknowledge signal from TCA 801 synchronized with CPU clock.
TSTON		3	Signals from the switches 'TEST' and 'TEST MODE' on the PCBA front panel.
SHORT		3	
MIR (0)		12	Microinstruction register, bits (0:35)
MIR (1:2)		2,12	
MIR (3)		2,4,12	
MIR (4:6)		12,14	
MIR (7)		12,16,17, 18	
MIR (8:9)		12,16,17, 18,20	
MIR (10)		12,16,17, 18	
MIR (11)		12,19	
MIR (12:14)		12,16,17, 18,25	
MIR (15)		12,14,19, 25	
MIR (16:17)		2,12,19, 25	
MIR (18)		12,15,25	
MIR (19)		2,12,15 25	
MIR (20)		2,12,14 25	
MIR (21:23)		12,14,25	
MIR (24:25)		12,14,20, 24,25	
MIR (26:27)		12,14,24, 25	
MIR (28:31)		12,16,17 18,25	
MIR (32:33)		12,16,17 18,19,25	
MIR (34:35)		12,19,25	
Unit			11A



SIGNAL	DESTI- NATION	DESCRIPTION
CSPARERROR	13	Control store parity error. Indicates parity error in the word contained in the microinstruction register. Odd parity is used.
-, CSPARERROR	12	Same as above. Used to drive the 'CONTROL STORE PARITY ERROR' indicator on the PCBA front panel.
TESTON	11	Control signal from the switch 'TEST' on the PCBA front panel.
TESTM SHORT	11	Control signal from the switch 'TEST MODE' on the PCBA front panel.
Unit		
	12A	



SIGNAL		DESTI- NATION	DESCRIPTION
MASTERCLOCK		14,30	5 MHz primary clock signal. All other clock signals are derived from this clock signal.
10 KHZCLOCK		31	10 kHz clock signal used to control the Real Time Clock by generating interrupt every 0.1 millisecond.
Unit			
			13A

12 72-13 CS PAR ERROR
30 130-12 7 POWER UPRST

25 9
26 10

749
00

KT-320

66 24

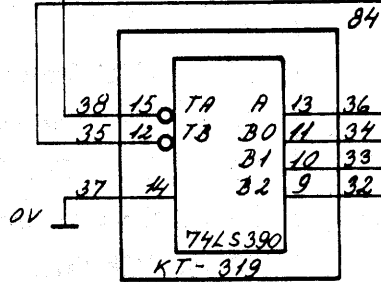
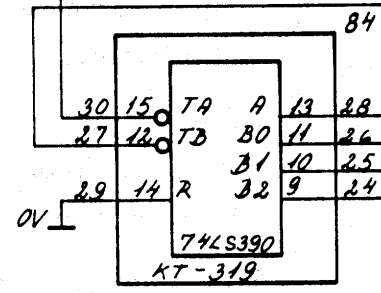
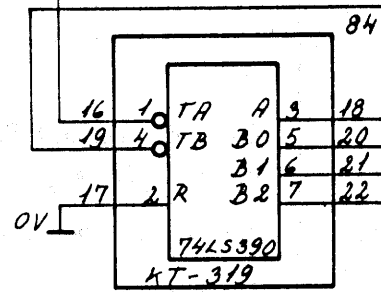
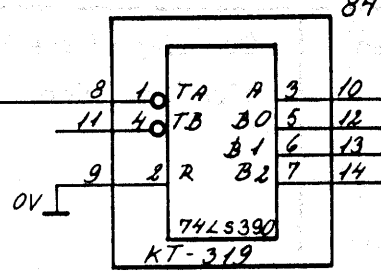
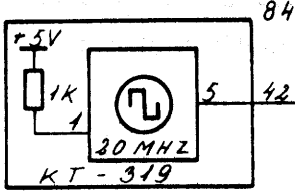
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Master Clock



10 KHZ Clock

17.10.78 AAJ

CPU 810

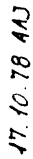
Master Clock and 10 KHZ Clock

R12377

13

SIGNAL	DESTI- NATION	DESCRIPTION
- , FORMAT (0)	Unused	Decoding of the format-field of the microinstruction.
- , FORMAT (1)	14	
- , FORMAT (2)	14	
- , FORMAT (3)	Unused	
- , FORMAT (4)	Unused	
- , FORMAT (5)	19	
- , FORMAT (6)	19	
- , FORMAT (7)	2	
CPINTR	30	CP for Interrupt Register.
CPUCLOCK	16,17,18 30,31	CP for 2901A's, Interrupt level Register, and some auxiliary registers.
CPMIR	1,2,3,4, 11	CP for Microinstruction Register, micro-program sequencer, jump condition selectors, and Microprogram Jump Address Register.
CPIMOP	25	CP for immediate Operand Register.
CPCOND	15	CP for Condition Register.
CPSCRATCHP	24	CP for Scratchpad Memory.
ENCPREG	14	Enable for CP to destination registers.
CONDL D (0,1)	15	Control load of ADDCOND and - ,DIVSIGN.
CPCPUSTATUS	27	CP for CPU Status Register
CPI/OADDR	15,32	CP for I/O Address Register
CPDATAOUT	33	CP for Data Out Register
CPCONTROLOUT	25	CP for Control Output Register
CPTCPDATAOUT	28	CP for TCP Data Out Register
CPINSTRREG	27	CP for Instruction Register
CPMIX	4	CP for Microprogram Index Register
CLEARINTR	30	Interrupt Register is addressed to clear an interrupt bit.
- , CLEARINTR	14,30	
- , ENSCRATCHP	24	
- , ENIMOP	25	
- , ENSIGNEXT	26	
- , ENROTATE	26	
- , ENDATAIN	34	
- , ENINTRLEV	31	
- , ENTCPDATAIN	28	

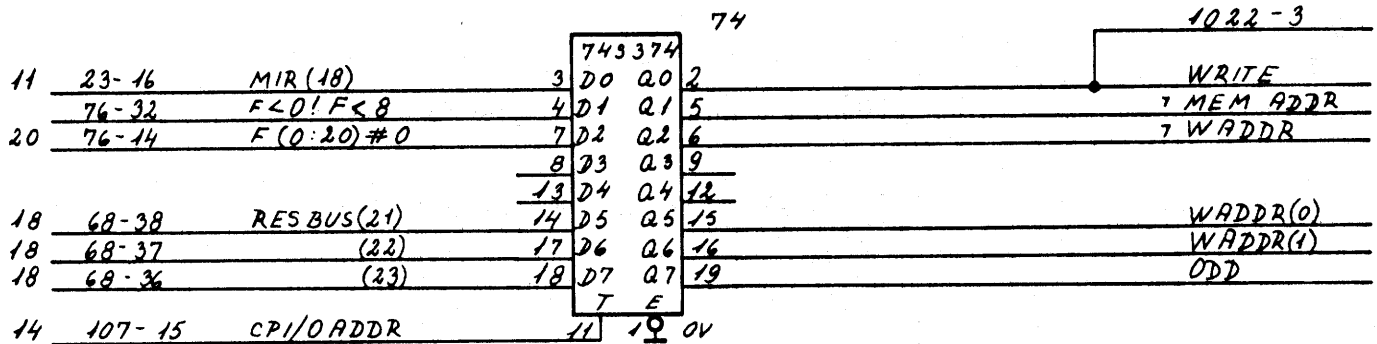
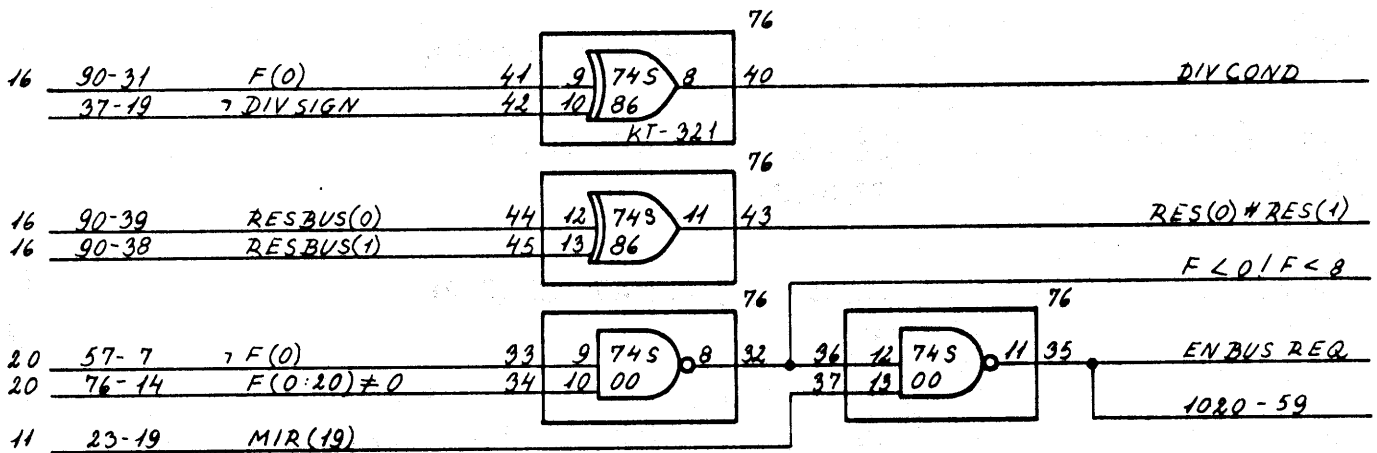
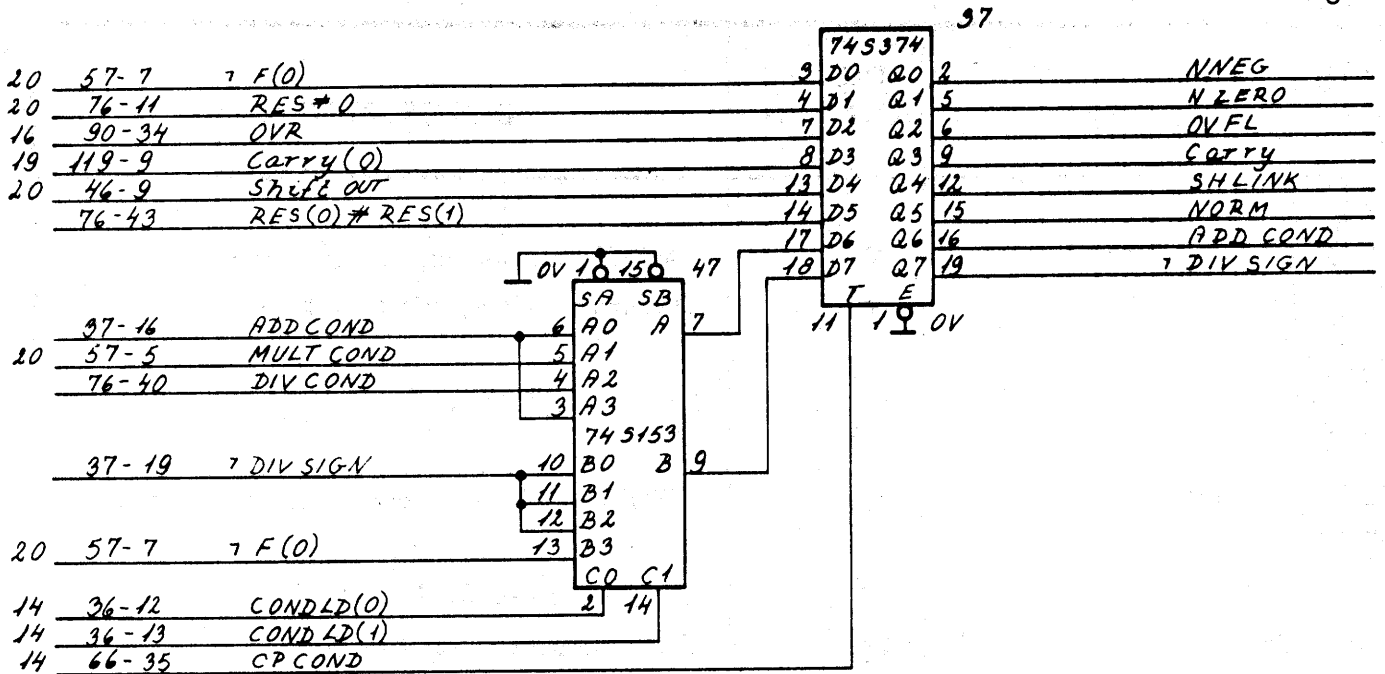
Unit		14A



Page 60

SIGNAL	DESTI- NATION	DESCRIPTION
JUMP CONDITIONS AND STATUS BITS:		
NNEG	2	RESULT >= 0
NZERO	2	RESULT <> 0
OVFL	2	Arithmetic overflow
CARRY	2,19	Carry out of bit (0) of ALU
SHLINK	20	Bit shifted out in shift instruction.
NORM	2	RESULT normalized
ADDCOND	15,19,20	Controls ALU operands in multiply and ALU function in divide microinstructions.
-, DIVSIGN	15	Used to store divisor sign in divide operations.
DIVCOND	15	DIVCOND = RESULT (0) exor -, DIVSIGN
RES (0) ≠ RES (1)	15	RESULT (0) <> RESULT (1)
F < 0 ! F < 8	15	RESULT < 8
ENBUSREQ	36	-, MIR (19) or RESULT >=8
WRITE	36	Control signal for I/O operations. Indicates data transfer from CPU to slave.
-, MEMADDR	3	I/O ADDRESS < 8
-, WADDR	3	I/O ADDRESS < 0 or I/O ADDR >= 8
WADDR (0,1)	19	WADDR (0,1) = I/O ADDR (21,22). Used as register address.
ODD	3	I/O ADDRESS is an odd number.

Unit		
		15A



17.10.78 AAS

SIGNAL		DESTINATION	DESCRIPTION
SHIFT I/O R (0)		20	RAM-Shifter in/out, bit (0), tri-state
SHIFT I/O Q (0)		20	Q-shifter in/out, bit (0), tri state
F(0)		15,20	F(0) = RESULT (0)
F(0:3) = 0		20	RESULT (0:3) = 0, open collector output.
-, G(0)		19	Carry generate for bits (0:3)
-, P(0)		19	Carry propagate for bits (0:3)
OVR		15,20	Arithmetic overflow.
RESBUS (0:1)		15,24,26, 27,32,33	RESULT BUS (0:1)
RESBUS (2:3)		24,26,27, 32,33	RESULT BUS (2:3)
F(4:7) = 0		20	RESULT (4:7) = 0, open collector output.
-, G(1)		19	Carry generate for bits (4:7)
-, P(1)		19	Carry propagate for bits (4:7)
RESBUS (4:7)		24,26,27, 32,33	RESULT BUS (4:7)

Unit

16A

20 56-7 RightshunR(0)
20 57-16 RightshunQ(0)

Shift 1/Q R(0)
Shift 1/Q Q(0)

11 33-9 MIR(7) 6 18
11 33-12 (8) 7 17
11 33-15 (9) 5 16
11 23-5 (13) 27 15
11 23-6 (14) 28 14
19 30-11 13 26 13
11 33-16 MIR(10) 14 12
19 30-9 11 13 11
11 23-2 MIR(12) 12 10

11 3-2 MIR(28) 4 A0
11 3-5 (29) 3 A1
11 3-6 (30) 2 A2
11 3-9 (31) 1 A3

11 3-12 MIR(32) 17 B0
11 3-12 (33) 18 B1
19 28-7 BADDR(2) 19 B2
19 28-9 (3) 20 B3

21 60-5 SBUS(0) 22 D3
21 60-7 (1) 23 D2
21 60-9 (2) 24 D1
21 60-11 (3) 25 D0

14 66-32 CPUCLOCK 15 T

19 119-11 Carry(4)

OV 40 OE
Cn R53 Q53

F3 31 F(0)
F=0 11 F(0 3)-0
G 32 7 G(0)
P 35 7 P(0)
OVR 34 OVR

Y3 39 RESBUS(0)
Y2 38 (1)
Y1 37 (2)
Y0 36 (3)
1020-37/65
1020-36/66
1020-35/67
1020-68

11 33-9 MIR(7) 6 18
11 33-12 (8) 7 17
11 33-15 (9) 5 16
11 23-5 (13) 27 15
11 23-6 (14) 28 14
19 30-11 13 26 13
11 33-16 MIR(10) 14 12
19 30-9 11 13 11
11 23-2 MIR(12) 12 10

11 3-2 MIR(28) 4 A0
11 3-5 (29) 3 A1
11 3-6 (30) 2 A2
11 3-9 (31) 1 A3

11 3-12 MIR(32) 17 B0
11 3-15 (33) 18 B1
19 28-7 BADDR(2) 19 B2
19 28-9 (3) 20 B3

21 50-5 SBUS(4) 22 D3
21 50-7 (5) 23 D2
21 50-9 (6) 24 D1
21 50-11 (7) 25 D0

14 66-32 CPUCLOCK 15 T

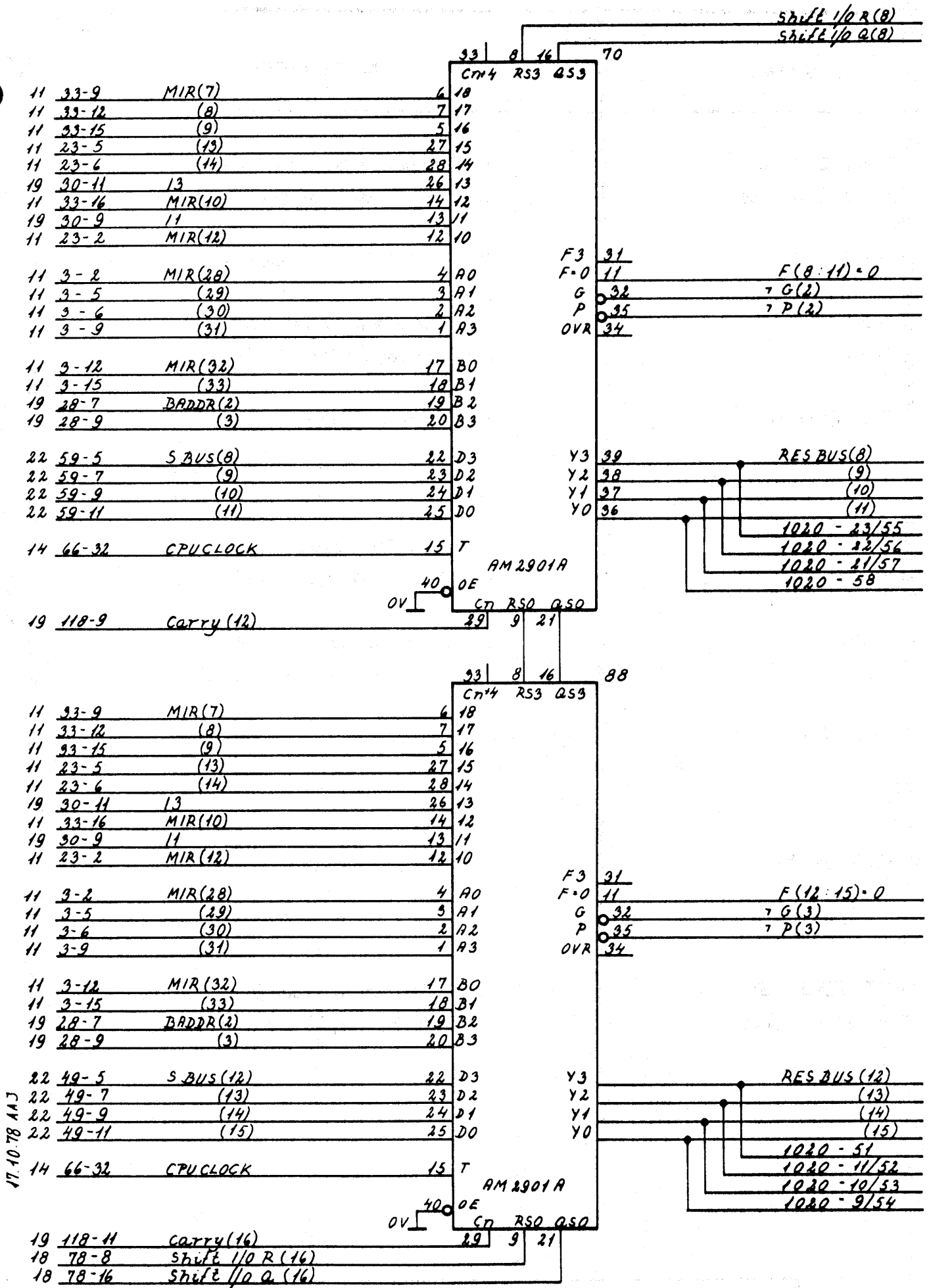
19 119-12 Carry(8)
17 70-8 Shift 1/Q R(8)
17 70-16 Shift 1/Q Q(8)

OV 40 OE
Cn R53 Q53

F3 31 F(4:7)-0
F=0 11
G 32 7 G(1)
P 35 7 P(1)
OVR 34

Y3 39 RESBUS(4)
Y2 38 (5)
Y1 37 (6)
Y0 36 (7)
1020-61
1020-26/62
1020-25/63
1020-24/64

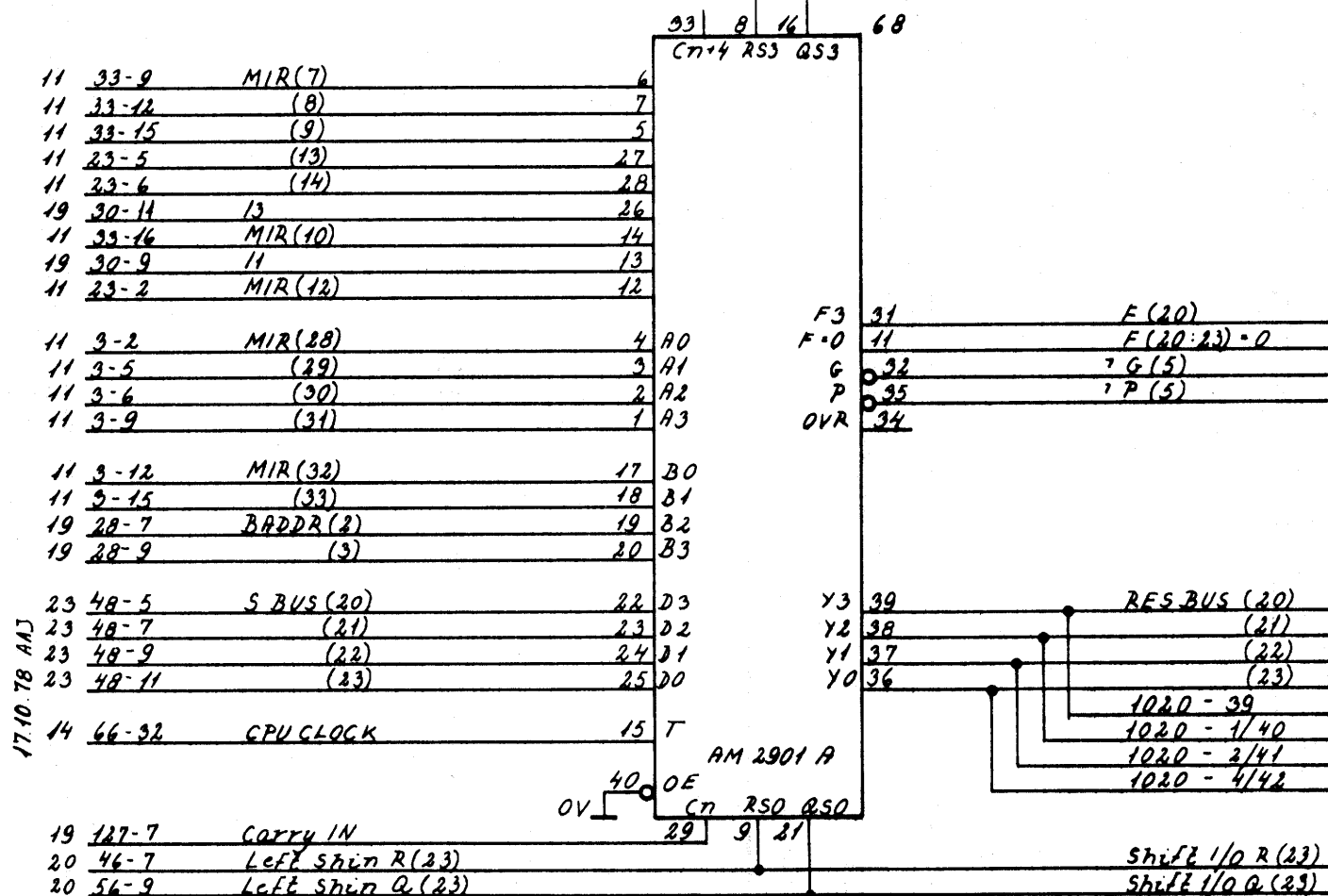
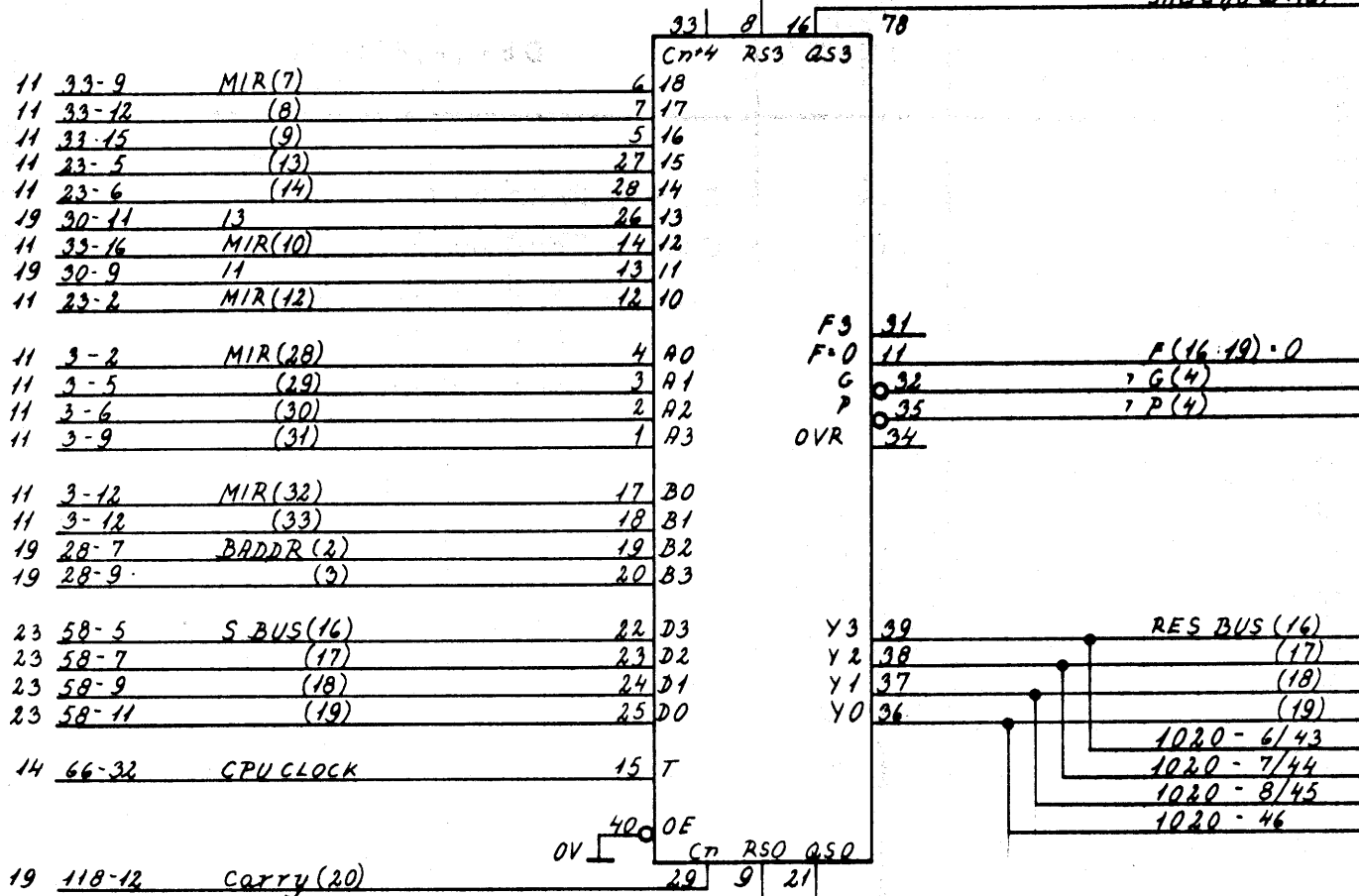
SIGNAL	DESTI- NATION	DESCRIPTION
SHIFT I/O R (8)	16	RAM-shifter in/out, bit (8), tri-state
SHIFT I/O Q (8)	16	Q-shifter in/out, bit (8), tri-state.
F(8:11) = 0	20	RESULT (8:11) = 0, open collector output.
-, G(2)	19	Carry generate for bits (8:11)
-, P(2)	19	Carry propagate for bits (8:11)
RESBUS (8:11)	24,26,27, 32,33	RESULT BUS (8:11)
F(12:15) = 0	20	RESULT (12:15) = 0, open collector output.
-, G(3)	19	Carry generate for bits (12:15)
-, P(3)	19	Carry propagate for bits (12:15).
RESBUS (12:15)	4,24,26, 32,33	RESULT BUS (12:15)
Unit		
	17A	



SIGNAL		DESTI- NATION	DESCRIPTION
SHIFT I/O R (16)		17	RAM-shifter in/out, bit (16), tri-state
SHIFT I/O Q (16)		17	Q-shifter in/out, bit (16), tri-state
F(16:19) = 0		20	RESULT (16:19) = 0, open collector output.
-, G(4)		19	Carry generate for bits (16:19)
-, P(4)		19	Carry propagate for bits (16:19)
RESBUS (16:19)		4, 24, 25, 26, 28, 32 33	RESULT BUS (16:19)
F(20)		20	F(20) = RESULT (20)
F(20:23) = 0		20	RESULT (20:23) = 0, open collector output.
-, G(5)		19	Carry generate for bits (20:23)
-, P(5)		19	Carry propagate for bits (20:23)
RESBUS (20)		4, 24, 25, 26, 28, 30, 32, 33	RESULT BUS (20)
RESBUS (21:23)		4, 15, 24, 25, 26, 28, 30, 32, 33	RESULT BUS (21:23)
SHIFT I/O R (23)		20	RAM-shifter in/out, bit (23), tri-state
SHIFT I/O Q (23)		20	Q-shifter in/out, bit (23), tri-state.
Unit			18A

Shift I/O R (16)

Shift I/O Q (16)



SIGNAL		DESTI- NATION	DESCRIPTION
CARRY (4)		16	Carry to 2901A bit (3)
CARRY (8)		16	Carry to 2901A bit (7)
CARRY (12)		17	Carry to 2901A bit (11)
CARRY (16)		17	Carry to 2901A bit (15)
CARRY (20)		18	Carry to 2901A bit (19)
CARRY IN		18,19	Output from carry selector. Carry to 2901A bit (23).
11		16,17,18	Controls ALU operands in multiply micro-instructions.
13		16,17,18	Controls ALU function in divide micro-instructions.
BADDR (2:3)		16,17,18	Two least significant bits of B address to 2901A.
Unit			19A



Carry Look-Ahead Control
Multiply, Divide, and B-Address Control for 2901

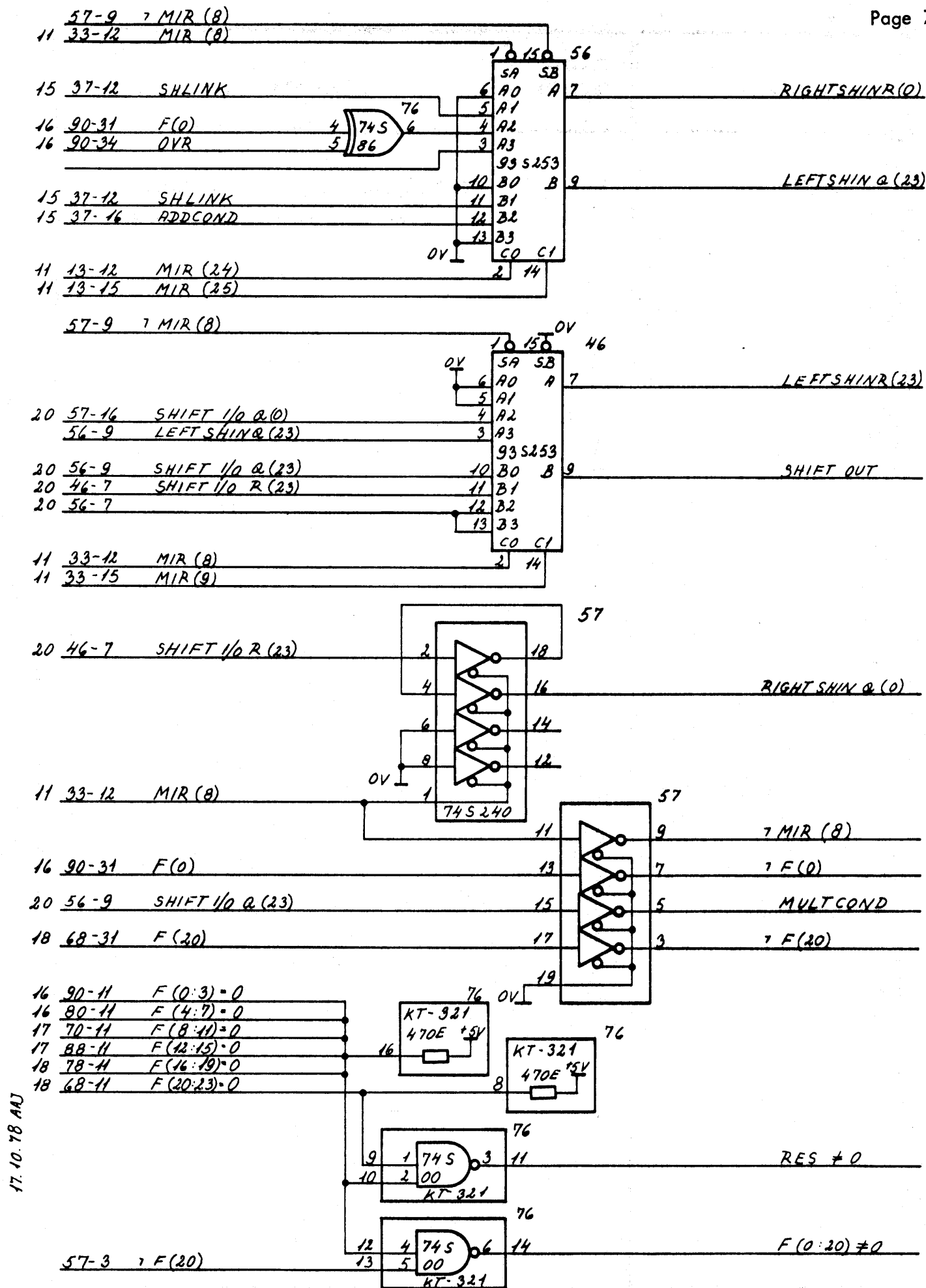
19

R 12383

SIGNAL	DESTINATION	DESCRIPTION
RIGHT SHIN R (0)	16,20	Shift input to RAM-shifter bit (0) for right shifts. Tri-state signal.
LEFT SHIN Q (23)	18,20	Shift input to Q-shifter bit (23) for left shifts. Tri-state signal.
LEFT SHIN R (23)	18,20	Shift input to RAM-shifter bit (23) for left shifts. Tri-state signal.
SHIFTOUT	15	Bit shifted out of RAM or Q-shifter in shift operations.
RIGHT SHIN Q (0)	16,20	Shift input to Q-shifter bit (0) for right shifts. Tri-state signal.
-, MIR (8)	20	Control tri-state output of multiplexers for shift control.
-, F(0)	15	-, F(0) = -, RESULT (0)
MULTCOND	15	MULTCOND = -, Q(23) in right shifts.
-, F(20)	20	-, F(20) = -, RESULT (20)
RES $\neq$ 0	15	RESULT $\neq$ 0
F(0:20) $\neq$ 0	15	RESULT < 0 or RESULT $\geq$ 8

Unit

20A



SIGNAL	DESTI- NATION	DESCRIPTION
SBUS (0:7)	16	SOURCE BUS (0:7). Input to 2901A from external source registers. Tri-state bus.
Unit		

21A

24	60-5	SCRATCHP(0)	S BUS(0)
25	18-2	IMOP(0)	
26	100-2	SIGNEXT(0)	
26	109-2	ROTATE(0)	
34	1020-31	DATA IN(0)	
24	60-7	SCRATCHP(1)	S BUS(1)
25	18-5	IMOP(1)	
26	100-5	SIGNEXT(1)	
26	109-5	ROTATE(1)	
34	1020-32	DATA IN(1)	
24	60-9	SCRATCHP(2)	S BUS(2)
25	18-6	IMOP(2)	
26	100-6	SIGNEXT(2)	
26	109-6	ROTATE(2)	
34	1020-33	DATA IN(2)	
24	60-11	SCRATCHP(3)	S BUS(3)
25	18-9	IMOP(3)	
26	100-9	SIGNEXT(3)	
26	109-9	ROTATE(3)	
34	1020-34	DATA IN(3)	
24	50-5	SCRATCHP(4)	S BUS(4)
25	18-12	IMOP(4)	
26	100-12	SIGNEXT(4)	
26	109-12	ROTATE(4)	
34	1020-27	DATA IN(4)	
24	50-7	SCRATCHP(5)	S BUS(5)
25	18-15	IMOP(5)	
26	100-15	SIGNEXT(5)	
26	109-15	ROTATE(5)	
34	1020-28	DATA IN(5)	
24	50-9	SCRATCHP(6)	S BUS(6)
25	18-16	IMOP(6)	
26	100-16	SIGNEXT(6)	
26	109-16	ROTATE(6)	
34	1020-29	DATA IN(6)	
24	50-11	SCRATCHP(7)	S BUS(7)
25	18-19	IMOP(7)	
26	100-19	SIGNEXT(7)	
26	109-19	ROTATE(7)	
34	1020-30	DATA IN(7)	

J7.10.78 MAJ

SIGNAL		DESTI- NATION	DESCRIPTION
SBUS (8:15)		17	SOURCE BUS (8:15). Input to 2901A from external source registers. Tri-state bus.
Unit			22A

24	59-5	1SCRATCHP(8)	15 BUS (8)
25	17-2	1MOP(8)	
26	110-2	SIGNEXT(8)	
26	98-2	ROTATE(8)	
34	1020-18	DATA IN(8)	

24	59-7	SCRATCHP(9)	S BUS (9)
25	17-5	1MOP(9)	
26	110-5	SIGNEXT(9)	
26	98-5	ROTATE(9)	
34	1020-17	DATA IN(9)	

24	59-9	SCRATCHP(10)	S BUS (10)
25	17-6	1MOP(10)	
26	110-6	SIGNEXT(10)	
26	98-6	ROTATE(10)	
34	1020-19	DATA IN(10)	

24	59-11	SCRATCHP(11)	S BUS (11)
25	17-9	1MOP(11)	
26	110-9	SIGNEXT(11)	
26	98-9	ROTATE(11)	
34	1020-20	DATA IN(11)	

24	49-5	SCRATCHP(12)	S BUS (12)
25	17-12	1MOP(12)	
26	110-12	SIGNEXT(12)	
26	98-12	ROTATE(12)	
34	1020-13	DATA IN(12)	

24	49-7	SCRATCHP(13)	S BUS (13)
25	17-15	1MOP(13)	
26	110-15	SIGNEXT(13)	
26	98-15	ROTATE(13)	
34	1020-14	DATA IN(13)	

24	49-9	SCRATCHP(14)	S BUS (14)
25	17-16	1MOP(14)	
26	110-16	SIGNEXT(14)	
26	98-16	ROTATE(14)	
34	1020-15	DATA IN(14)	

24	49-11	SCRATCHP(15)	S BUS (15)
25	17-19	1MOP(15)	
26	110-19	SIGNEXT(15)	
26	98-19	ROTATE(15)	
34	1020-16	DATA IN(15)	

17.10.78 AAJ

SIGNAL	DESTI- NATION	DESCRIPTION
SBUS (16:23)	18	SOURCE BUS (16:23). Input to 2901A from external source registers. Tri-state bus.
Unit		
		23A

24	58-5	SCRATCHP(16)	S BUS(16)
25	7-2	IMOP(16)	
26	99-2	SIGNEXT(16)	
26	108-2	ROTATE(16)	
34	1021-8	DATA IN(16)	
31	97-2	INTRLEV(0)	
28	20-2	TCPDATA IN(0)	

24	58-7	SCRATCHP(17)	S BUS(17)
25	7-5	IMOP(17)	
26	99-5	SIGNEXT(17)	
26	108-5	ROTATE(17)	
34	1021-7	DATA IN(17)	
31	97-5	INTRLEV(1)	
28	20-5	TCPDATA IN(1)	

24	58-9	SCRATCHP(18)	S BUS(18)
25	7-6	IMOP(18)	
26	99-6	SIGNEXT(18)	
26	108-6	ROTATE(18)	
34	1021-4	DATA IN(18)	
31	97-6	INTRLEV(2)	
28	20-6	TCPDATA IN(2)	

24	58-11	SCRATCHP(19)	S BUS(19)
25	7-9	IMOP(19)	
26	99-9	SIGNEXT(19)	
26	108-9	ROTATE(19)	
34	1021-3	DATA IN(19)	
31	97-9	INTRLEV(3)	
28	20-9	TCPDATA IN(3)	

24	48-5	SCRATCHP(20)	S BUS(20)
25	7-12	IMOP(20)	
26	99-12	SIGNEXT(20)	
26	108-12	ROTATE(20)	
34	1021-2	DATA IN(20)	
31	97-12	INTRLEV(4)	
28	20-12	TCPDATA IN(4)	

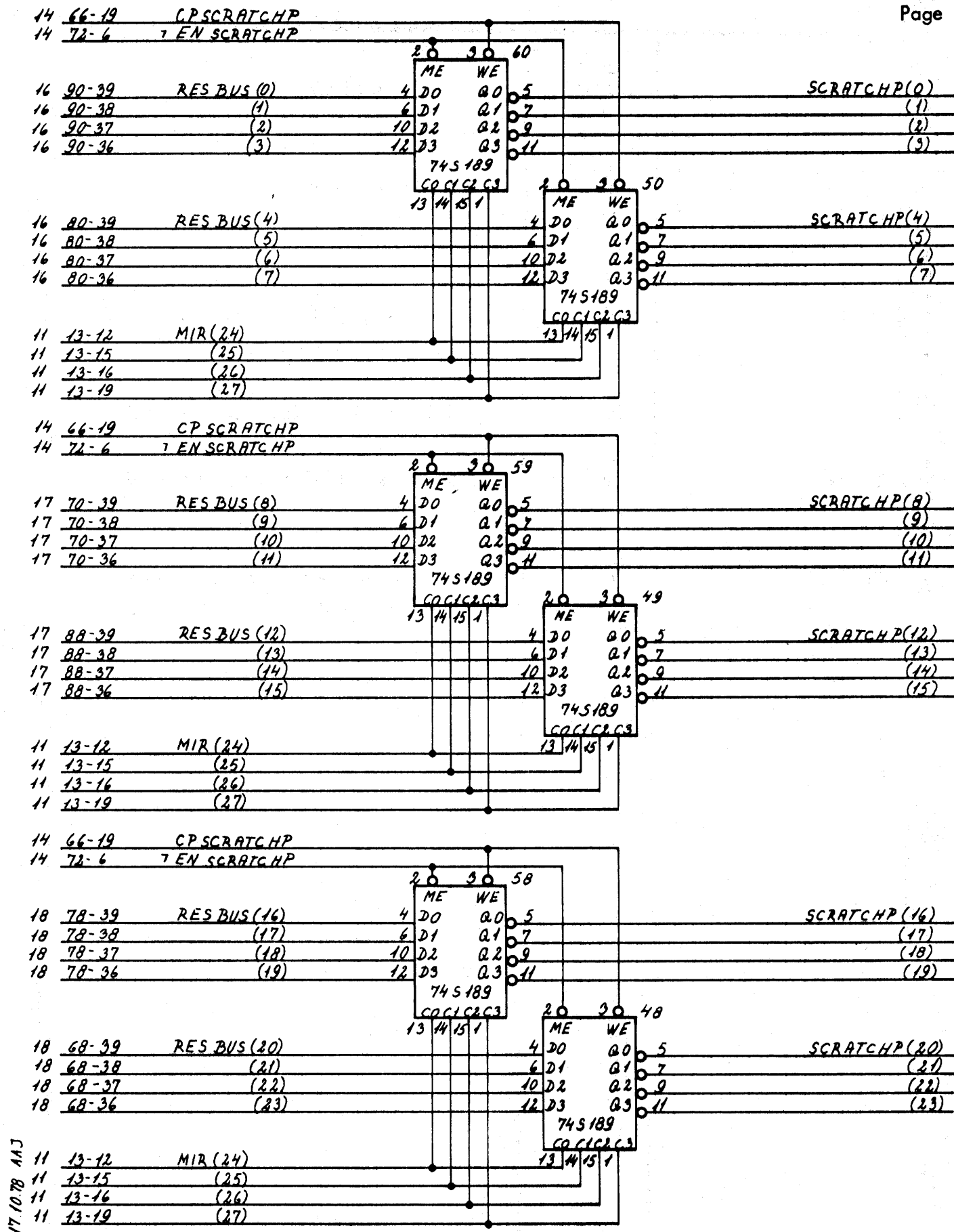
24	48-7	SCRATCHP(21)	S BUS(21)
25	7-15	IMOP(21)	
26	99-15	SIGNEXT(21)	
26	108-15	ROTATE(21)	
34	1021-5	DATA IN(21)	
31	97-15	INTRLEV(5)	
28	20-15	TCPDATA IN(5)	

24	48-9	SCRATCHP(22)	S BUS(22)
25	7-16	IMOP(22)	
26	99-16	SIGNEXT(22)	
26	108-16	ROTATE(22)	
34	1021-6	DATA IN(22)	
31	97-16	INTRLEV(6)	
28	20-16	TCPDATA IN(6)	

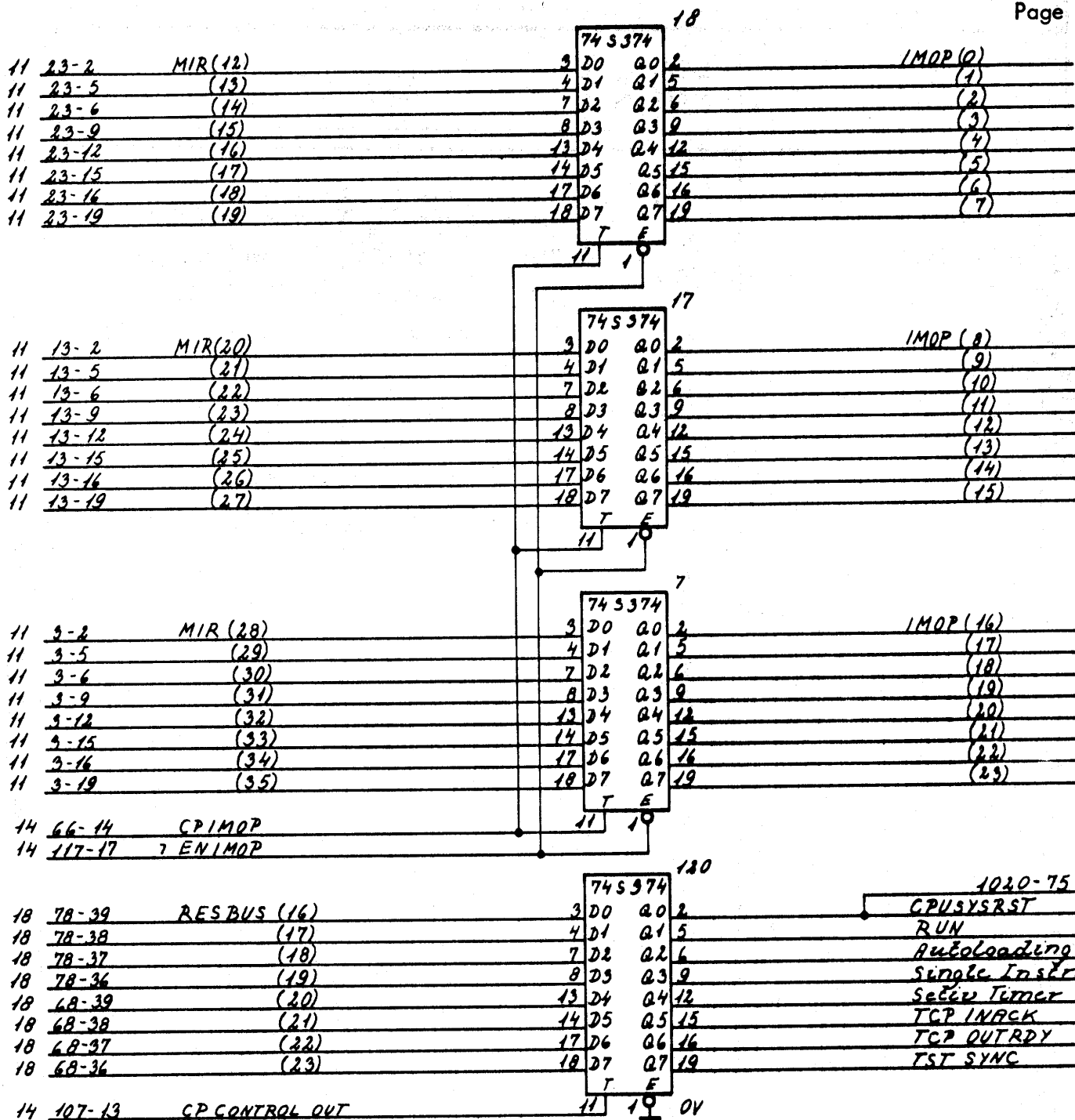
24	48-11	SCRATCHP(23)	S BUS(23)
25	7-19	IMOP(23)	
26	99-19	SIGNEXT(23)	
26	108-19	ROTATE(23)	
34	1021-9	DATA IN(23)	
31	97-19	INTRLEV(7)	
28	20-19	TCPDATA IN(7)	

17.10.78 AAJ

SIGNAL		DESTI- NATION	DESCRIPTION
SCRATCHP (0:7)		21	16 word Scratchpad Memory.
SCRATCHP (8:15)		22	Connected to SOURCE BUS.
SCRATCHP (16:23)		23	Tri-state outputs.
Unit		24A	

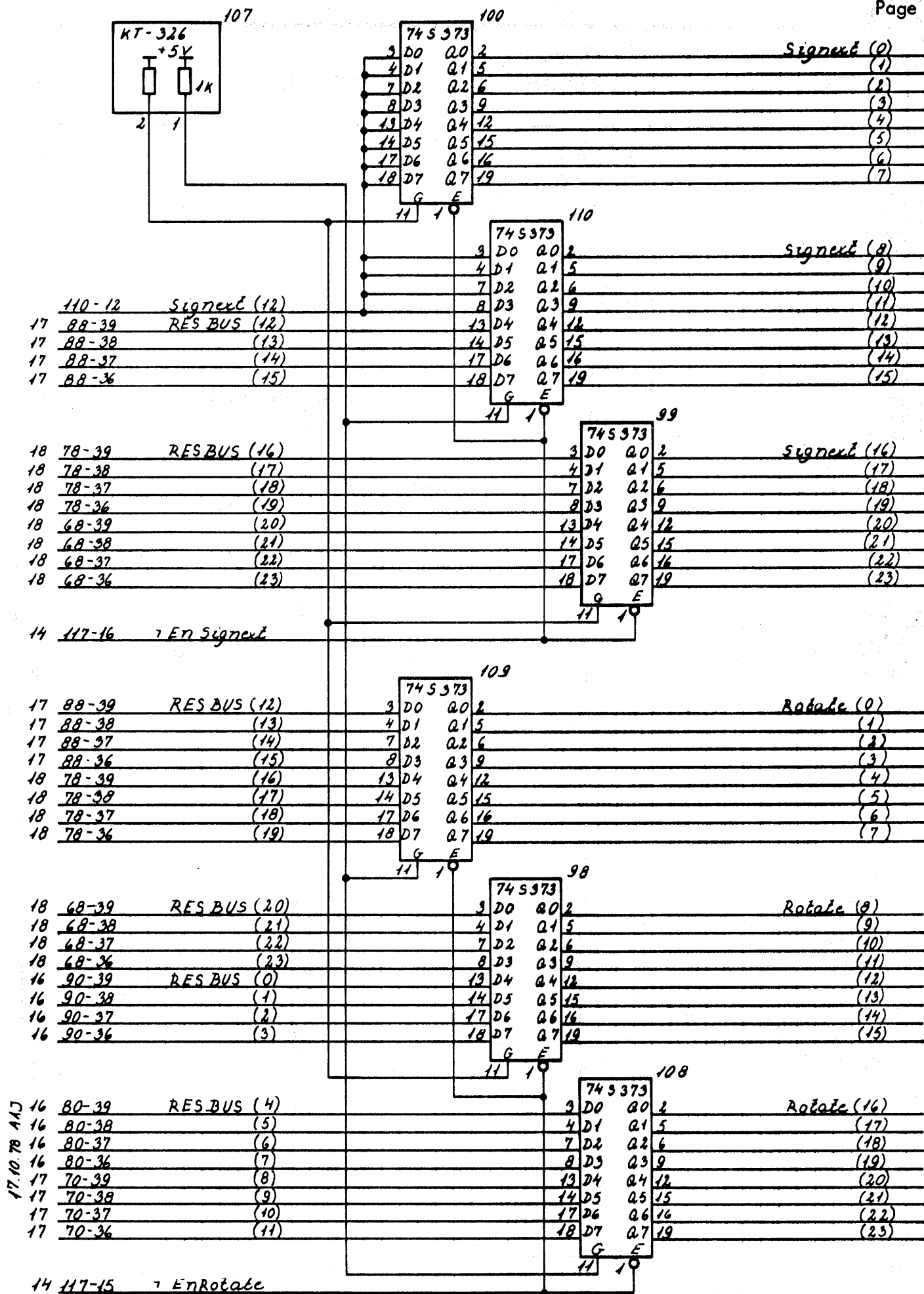


SIGNAL		DESTI- NATION	DESCRIPTION
IMOP (0:7)		21	Immediate Operand Register.
IMOP (8:15)		22	Connected to SOURCE BUS.
IMOP (16:23)		23	Tri-state outputs.
CPUSYSRST		39	System Reset signal generated by CPU 810. Connected to System Bus.
RUN		29	Controls the 'RUN' lamp on the OCP.
AUTOLOADING		29	Controls the 'AUTOLOAD' lamp on the OCP.
SINGLEINSTR		28	Interrupt signal used to control single instruction execution.
SET IV TIMER		31	Used to set the Interval Timer interrupt flip-flop.
TCPINACK		28	Acknowledge signal from CPU to TCA.
TCPOUTRDY		28	Ready signal from CPU to TCA.
TSTSYNC		-	Synchronization signal controlled by micro-diagnostic routines. Intended as scope trigger.
Unit			25A



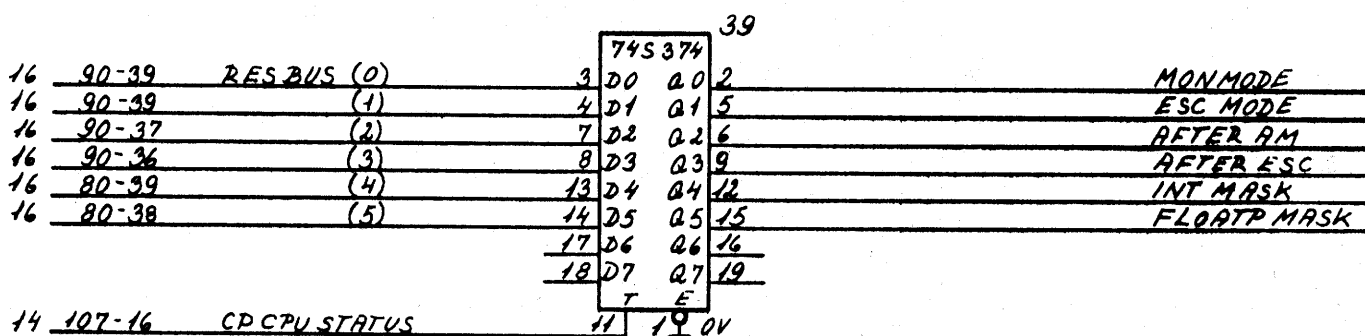
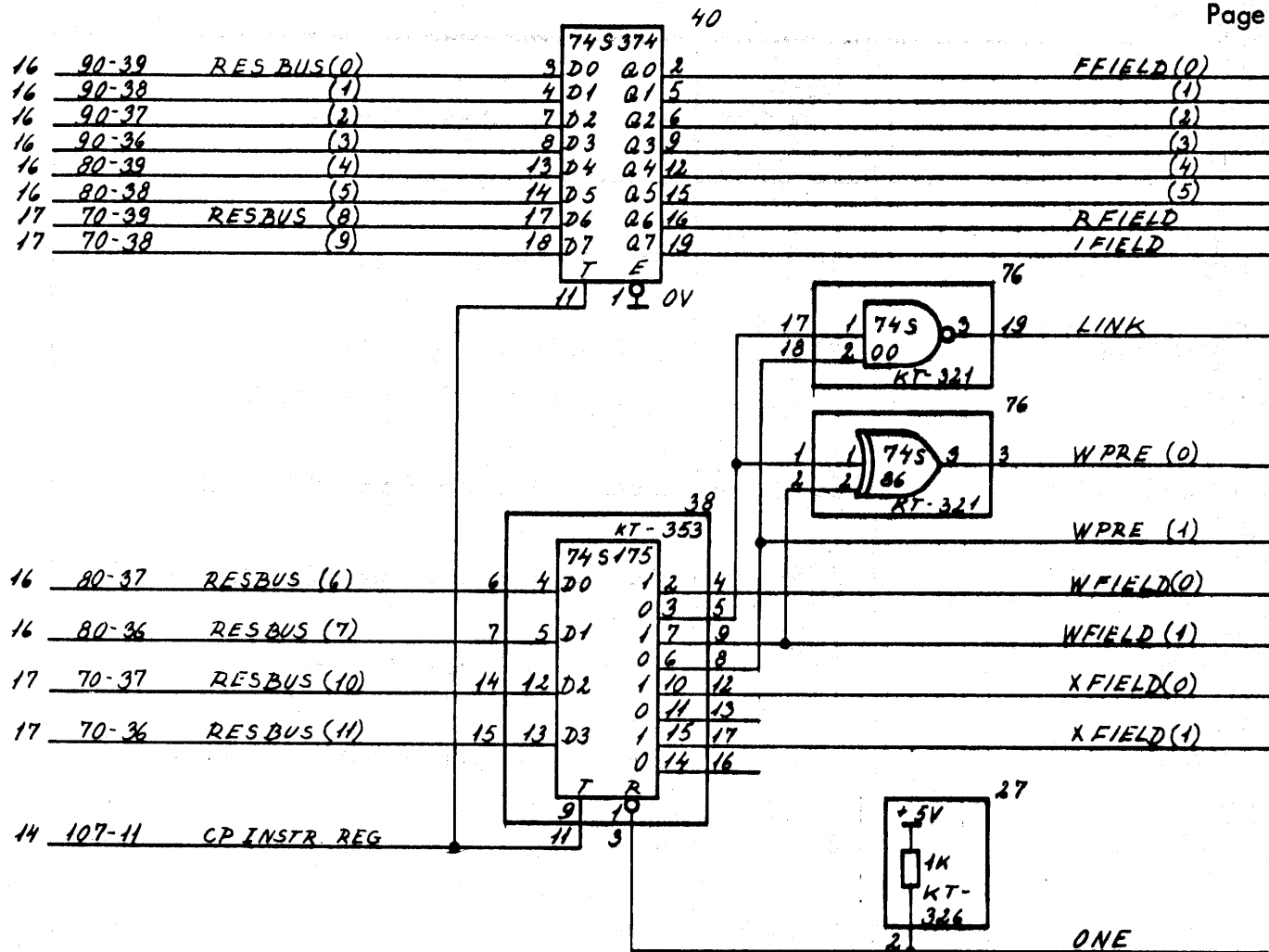
17.10.78 AMJ

SIGNAL		DESTI- NATION	DESCRIPTION
SIGNEXT (0:7)		21	Transfers bits (12:23) from the RESULT BUS to the SOURCE BUS with bit (12) extended as sign. SIGNEXT (0:23) = 12 ext RESBUS (12) con RESBUS (12:23).
SIGNEXT (8:15)		22	
SIGNEXT (16:23)		23	
ROTATE (0:7)		21	The contents of the RESULT BUS is rotated 12 bits and transferred to the SOURCE BUS. ROTATE(0:23) = RESBUS(12:23) con (RESBUS(0:11)
ROTATE (8:15)		22	
ROTATE (16:23)		23	
Unit			
		26A	



SIGNAL	DESTI- NATION	DESCRIPTION
FFIELD (0:5)	4	Instruction Register bits (0:5). Contains the function code of the instruction being executed.
RFIELD	4	Instruction Register bit (8). Relative addressing.
IFIELD	3	Instruction Register bit (9). Indirect addressing.
LINK	3	W-FIELD <> 0
WPRE (0,1)	19	WPRE selects first register of a double register.
WFIELD (0)	19	Instruction Register bits (6,7). Selects working register.
WFIELD (1)	19,27	
XFIELD (0,1)	4,19	Instruction Register bits (10,11). Selects index register.
ONE	14,27	Logic one generator for unused inputs.
MONMODE	3	Copy of bit (0:5) of STATUS word. Used as jump conditions and in instruction decoding.
ESCMODE	3,4	
AFTERAM	3,4	
AFTERESC	3	
INTMASK	3	
FLOATPMASK	3	
Unit		
	27A	

27A



17.10.78 MJ

CPU 810

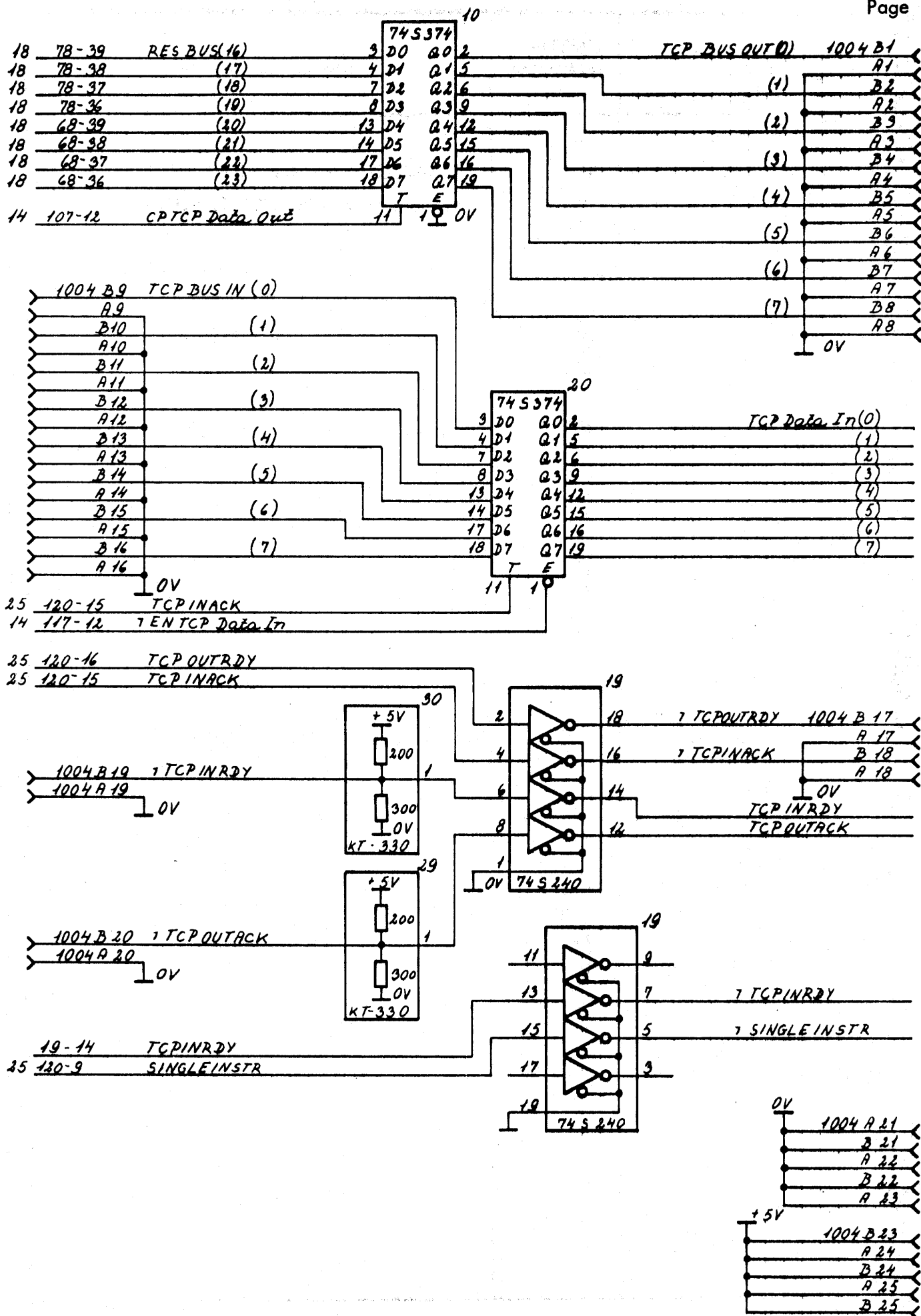
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Instruction Register
CPU Status Register

27

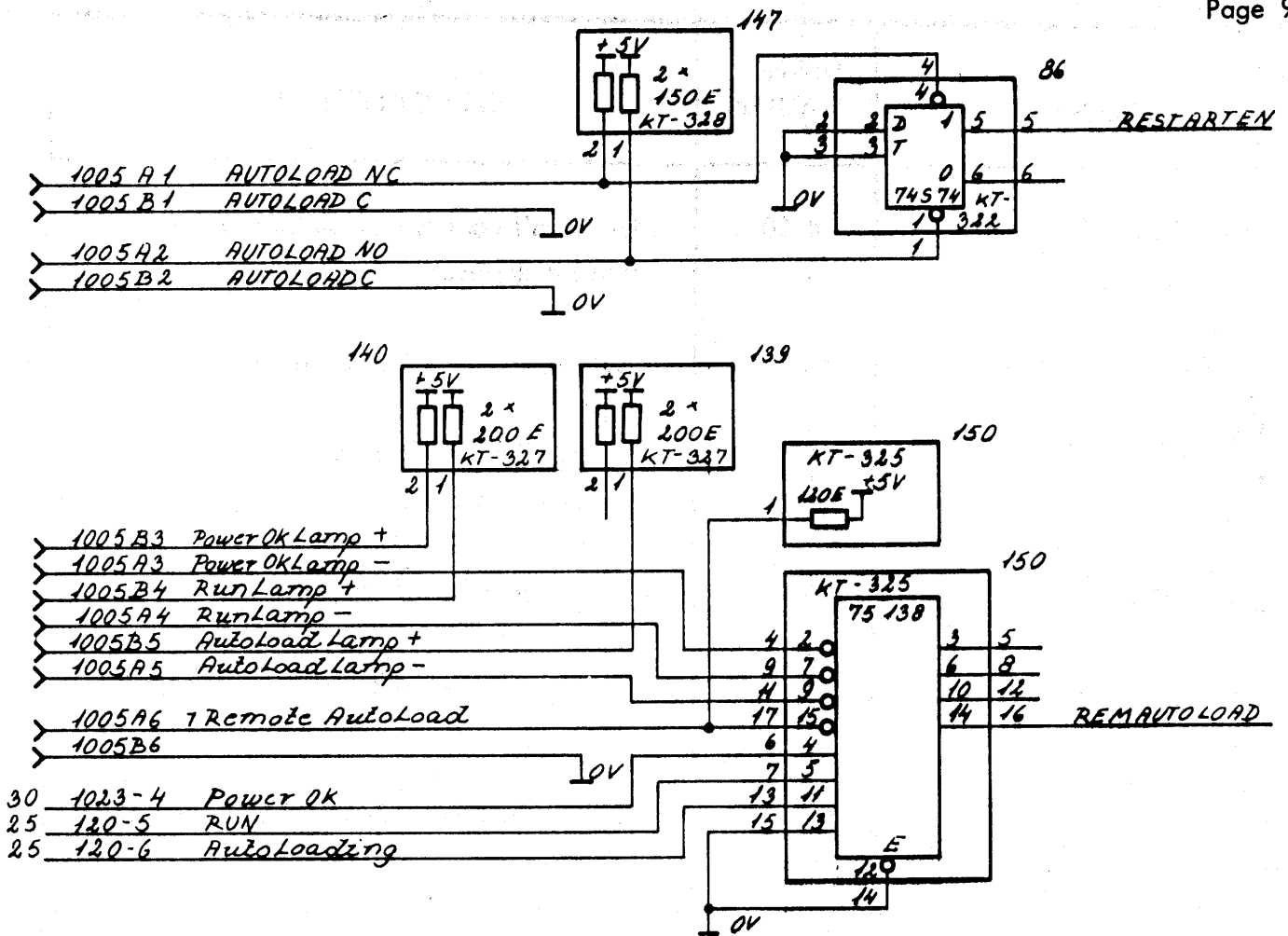
SIGNAL	DESTI- NATION	DESCRIPTION
TCPBUSOUT (0:7)	TCA	Data bus for data from CPU to TCA.
TCPDATAIN (0:7)	23	Data received from TCA. Connected to SBUS (16:23). Tri-state outputs.
-, TCPOUTRDY	TCA	Data ready signal from CPU to TCA.
-, TCPINACK	TCA	Acknowledge signal from CPU to TCA.
TCPINRDY	28	Ready signal received from TCA.
TCPOUTACK	3	Acknowledge signal received from TCA.
-, TCPINRDY	31	Ready signal received from TCA. Generates interrupt.
-, SINGLEINSTR	31	Interrupt signal. Controls single instruction execution.
1024 A21, B21, A22, B22, A23		0 volt supply to TCA.
1024 B23, A24, B24, A25, B25		+5 volts supply to TCA.
Unit		

28A



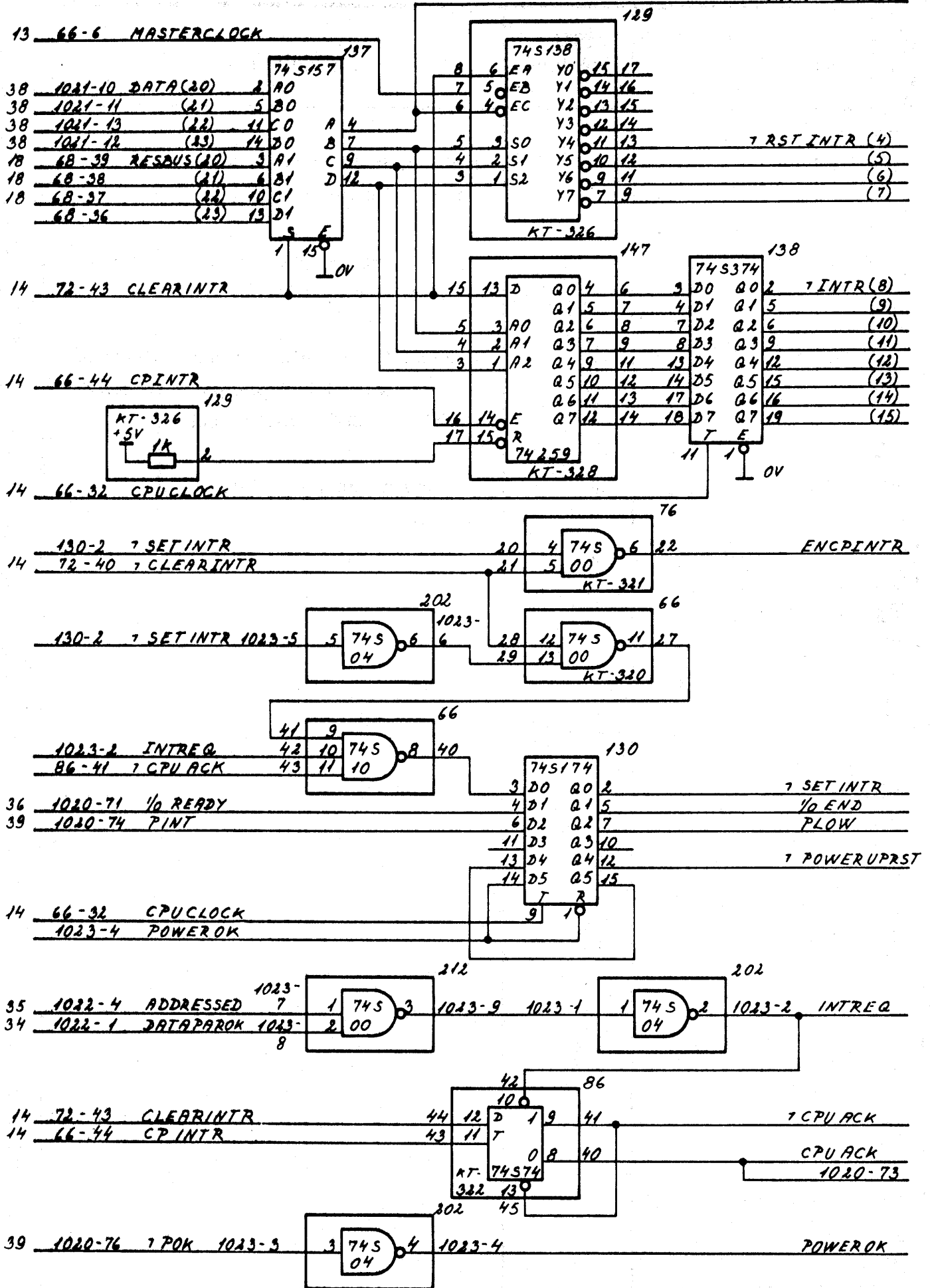
17.10.78 ANJ

SIGNAL	DESTI- NATION	DESCRIPTION
RESTARTEN	31	RESTARTEN = 0 when the 'AUTOLOAD' push-button on the OCP is activated.
REMAUTOLOAD	31	Autoload signal from external device.
POWEROKLAMP + POWEROKLAMP -	OCP OCP	Controls 'POWER OK' lamp on OCP.
RUN LAMP + RUN LAMP -	OCP OCP	Controls 'RUN' lamp on OCP.
AUTOLOADLAMP + AUTOLOADLAMP -	OCP OCP	Controls 'AUTOLOAD LAMP' on OCP.
Unit		
29A		



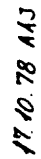
17.10.78 ANJ

SIGNAL	DESTINATION	DESCRIPTION
INTRADDR (20)	14, 30	Most significant bit of address to Interrupt Register.
-, RSTINTR (4:7)	31	Reset signals to interrupt flip-flops.
-, INTR (8:15)	31	Interrupt Register bits (8:15). An interrupt is represented by a 0.
ENCPINTR	14	Enable signal for CP to Interrupt Register.
-, SETINTR	30	External interrupt request synchronized with CPUCLOCK.
I/O END	14	Indicates that an I/O transfer has been completed.
PLOW	3	Power low interrupt from power supply. Mains below app. 180 V.
-, POWERUPRST	1, 2, 13, 14	Reset signal used to initialize logic when power is turned on. The signal is low for min. 1 clock period (200 ns) after power on.
INTREQ	30	External interrupt request.
-, CPUACK	30	Acknowledge signal from CPU to external device which sends an interrupt request.
CPUACK	39	
POWEROK	30	Power ok signal from power supply.



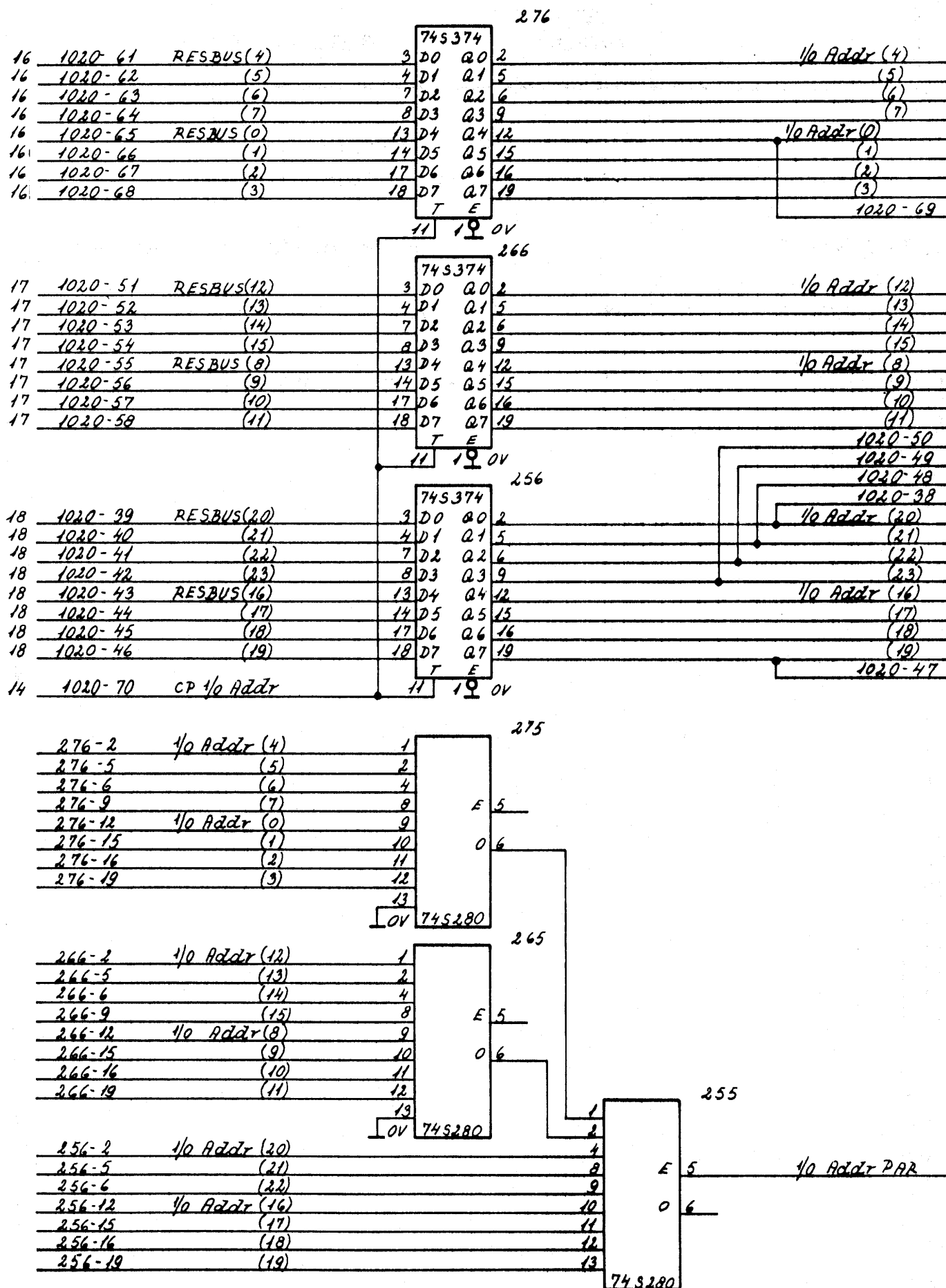
SIGNAL	DESTI- NATION	DESCRIPTION
INTERRUPT	3	Indicates that one or more bits in the Interrupt Register is 0.
-, INTR (1:7)	31	Interrupt Register bits (1:7). An interrupt is represented by a 0.
INTRLEV (0:7)	23	Interrupt Level Register. Contains level of interrupt with highest priority. Connected to SOURCE BUS. Tri-state outputs.
INTR	31	Interrupt output from interrupt priority encoder.
Unit		

31A



SIGNAL	DESTI- NATION	DESCRIPTION
I/O ADDR (0:22)	37	I/O Address Register. Used to hold the I/O address during input/output operations.
I/O ADDRPAR	37	Parity bit for I/O address. Odd parity is used.
Unit		

32A



17.10.78 AAJ

SIGNAL	DESTI- NATION	DESCRIPTION
DATAOUT (0:23)	38	Data Out Register. Contains data to be transmitted via the System Bus.
DATAOUTPAR (0)	39	Parity bit for DATAOUT (0:7). Odd parity.
DATAOUTPAR (1)	39	Parity bit for DATAOUT (8:15). Odd parity.
DATAOUTPAR (2)	39	Parity bit for DATAOUT (16:23). Odd parity.
Unit		
33A		

246

16	1020-61	RES BUS (4)	9	D0	Q0	2	
16	1020-26	(5)	4	D1	Q1	5	Data Out (4)
16	1020-25	(6)	7	D2	Q2	6	(5)
16	1020-24	(7)	8	D3	Q3	9	(6)
16	1020-37	RES BUS (0)	13	D4	Q4	12	(7)
16	1020-36	(1)	14	D5	Q5	15	Data Out (0)
16	1020-35	(2)	17	D6	Q6	16	(1)
16	1020-68	(3)	18	D7	Q7	19	(2)
				T	E		(3)

236

17	1020-51	RES BUS (12)	3	D0	Q0	2	
17	1020-11	(13)	4	D1	Q1	5	Data Out (12)
17	1020-10	(14)	7	D2	Q2	6	(13)
17	1020-9	(15)	8	D3	Q3	9	(14)
17	1020-23	RES BUS (8)	13	D4	Q4	12	(15)
17	1020-22	(9)	14	D5	Q5	15	Data Out (8)
17	1020-21	(10)	17	D6	Q6	16	(9)
17	1020-58	(11)	18	D7	Q7	19	(10)
				T	E		(11)

226

18	1020-39	RES BUS (20)	3	D0	Q0	2	
18	1020-1	(21)	4	D1	Q1	5	Data Out (20)
18	1020-2	(22)	7	D2	Q2	6	(21)
18	1020-4	(23)	8	D3	Q3	9	(22)
18	1020-6	RES BUS (16)	13	D4	Q4	12	(23)
18	1020-7	(17)	14	D5	Q5	15	Data Out (16)
18	1020-8	(18)	17	D6	Q6	16	(17)
18	1020-46	(19)	18	D7	Q7	19	(18)
				T	E		(19)

14 1020-5 CP Data Out

243

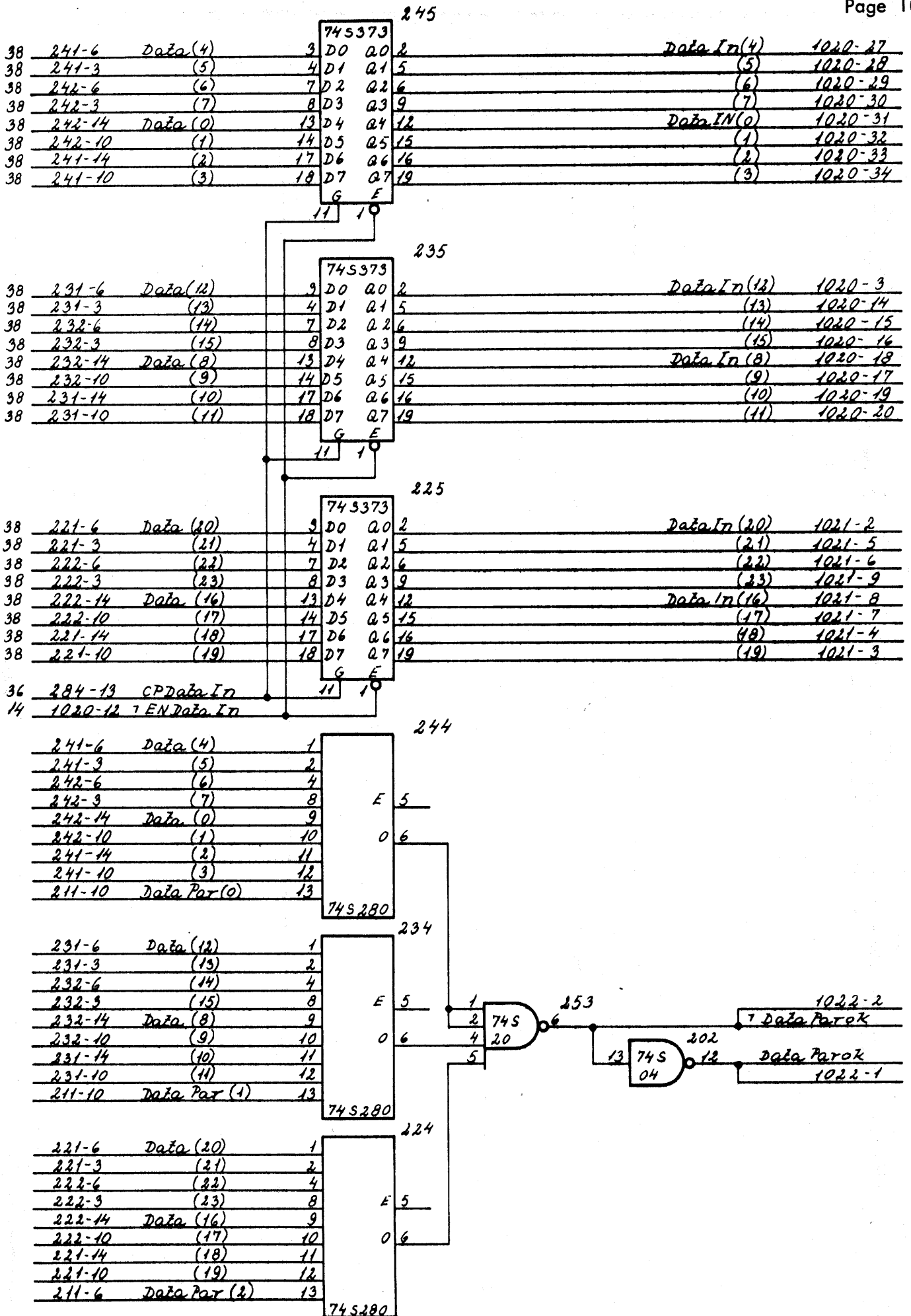
246-2	Data Out (4)	1					
246-5	(5)	2					
246-6	(6)	4					
246-9	(7)	8					
246-12	Data Out (0)	9		E	5		Data Out Par (0)
246-15	(1)	10		O	6		
246-16	(2)	11					
246-19	(3)	12					
		13					
		OV	74S280				

236-2	Data Out (12)	1					
236-5	(13)	2					
236-6	(14)	4					
236-9	(15)	8					
236-12	Data Out (8)	9		E	5		Data Out Par (1)
236-15	(9)	10		O	6		
236-16	(10)	11					
236-19	(11)	12					
		13					
		OV	74S280				

223

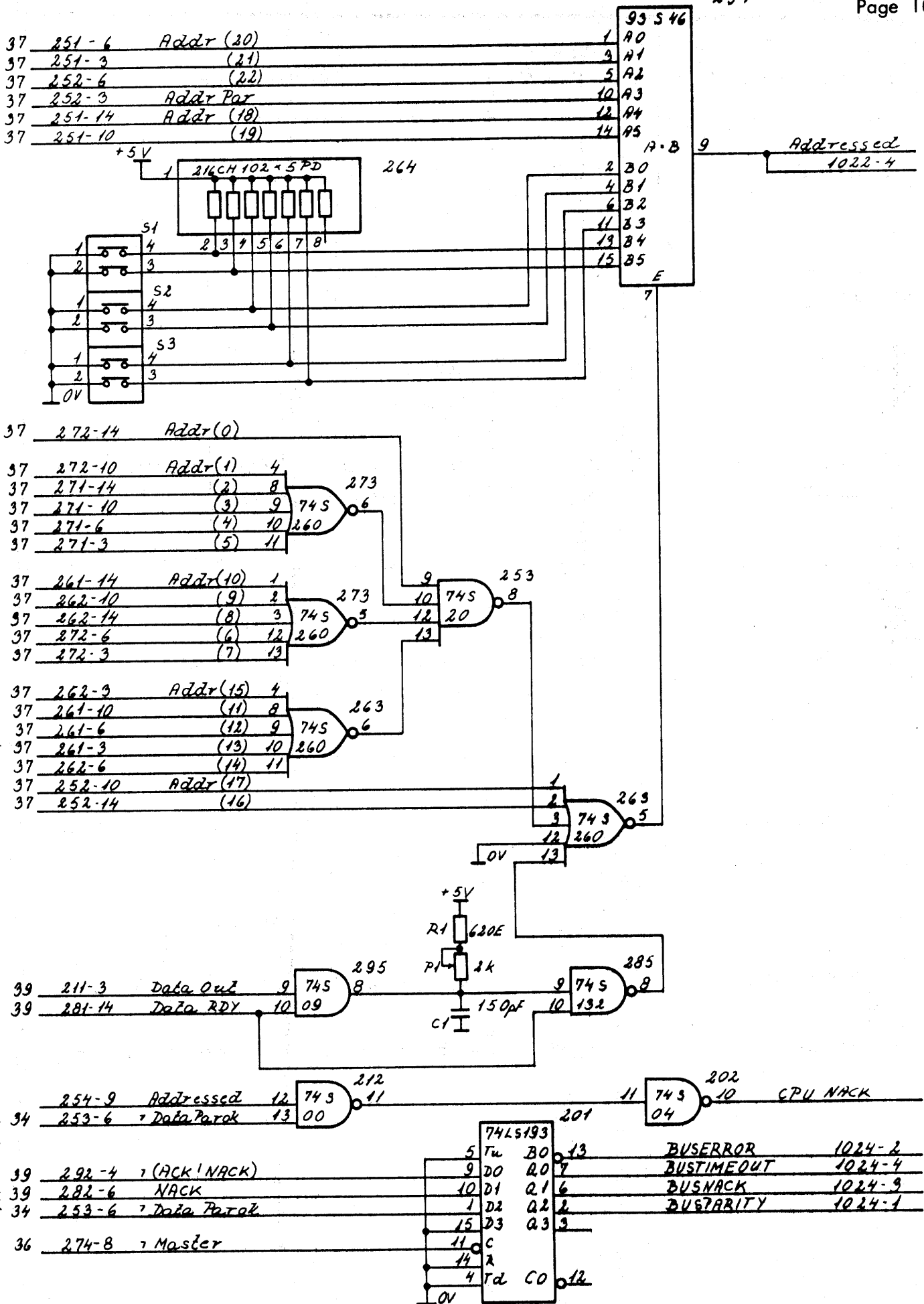
226-2	Data Out (20)	1					
226-5	(21)	2					
226-6	(22)	4					
226-9	(23)	8					
226-12	Data Out (16)	9		E	5		Data Out Par (2)
226-15	(17)	10		O	6		
226-16	(18)	11					
226-19	(19)	12					
		13					
		OV	74S280				

SIGNAL	DESTI- NATION	DESCRIPTION
DATAIN (0:7)	21	Data In Register. Contains data received via the System Bus. Connected to SOURCE BUS. Tri-state outputs.
DATAIN (8:15)	22	
DATAIN (16:23)	23	
- , DATAPAROK	35	Parity check of data received via the System Bus.
DATAPAROK	30	
Unit		
	34A	



SIGNAL	DESTINATION	DESCRIPTION
ADDRESSED	30, 35	Indicates that the CPU is addressed via the System Bus.
CPUNACK	39	Negative response to interrupt addressing due to parity error in received data.
BUSERROR	3	Indicates that at least one of the status bits for I/O transfer is set.
BUSTIMEOUT	3	Indicates that the addressed unit did not respond within approximately 4 microseconds.
BUSNACK	3	Indicates that the addressed unit responded with a NACK.
BUSPARITY	3	Indicates parity error in the received data word.
Unit		
	35A	

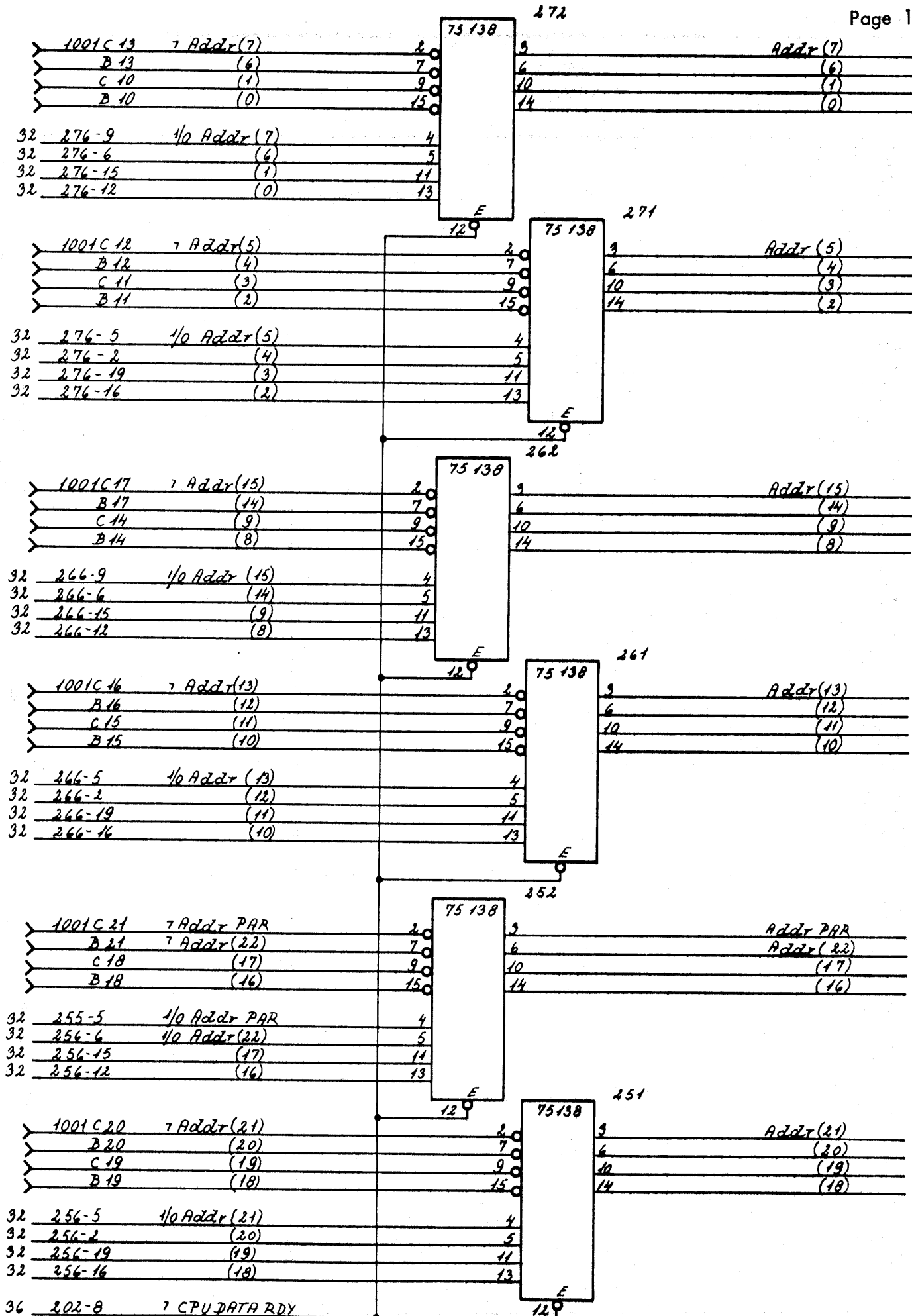
254



SIGNAL	DESTI- NATION	DESCRIPTION
CPUBUSREQ	36, 39	Indicates that the CPU wants to obtain bus master status.
CPUSELOUT CPUSELACK	39 39	Bus master selection control signals.
I/O READY	30	Indicates that an I/O transfer has been completed.
MASTER -, MASTER	36 36	Indicates that the CPU has obtained master status on the System Bus.
CPUDATARDY	39	Generates DATARDY and BUSBUSY on the System Bus.
-, DELACK	36	A 0 indicates that an ACK or NACK has been received while the CPU is bus master. The signal is delayed to compensate for skew between data and ACK/NACK.
-, TIMEOUT	36	A 0 indicates that the CPU has been bus master for approx. 4 microsec.
CPDATAIN	34	CP for the Data In Register.
-, CPUDATARDY	37	Enable signal for bus transceivers for address.
-, SENDDATA	38, 39	Enable signal for bus transceivers for data.
Unit		
	36A	

SIGNAL	DESTI- NATION	DESCRIPTION
ADDR (0:22)	35	Address received via the System Bus.
ADDRPAR	35	Parity bit for the received address. Odd parity is used.
Unit		
	37A	

17.10.78 ANJ



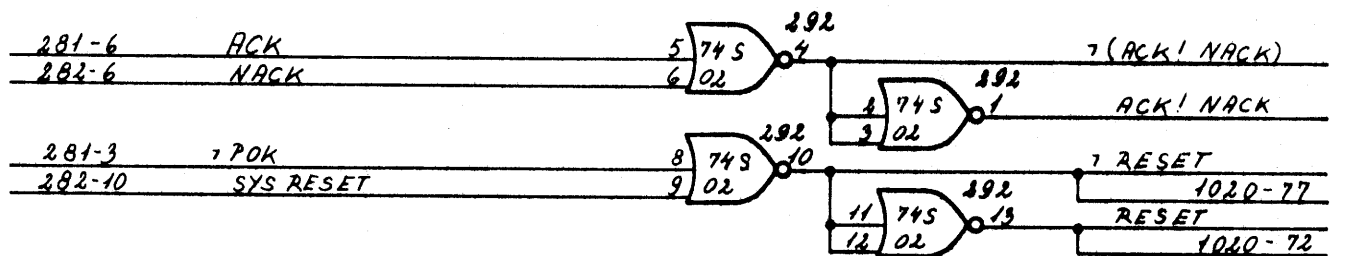
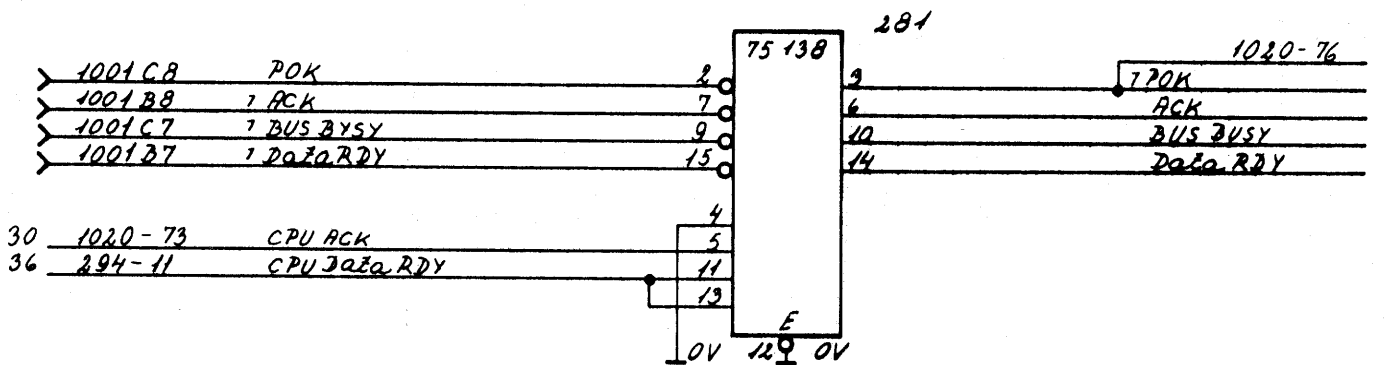
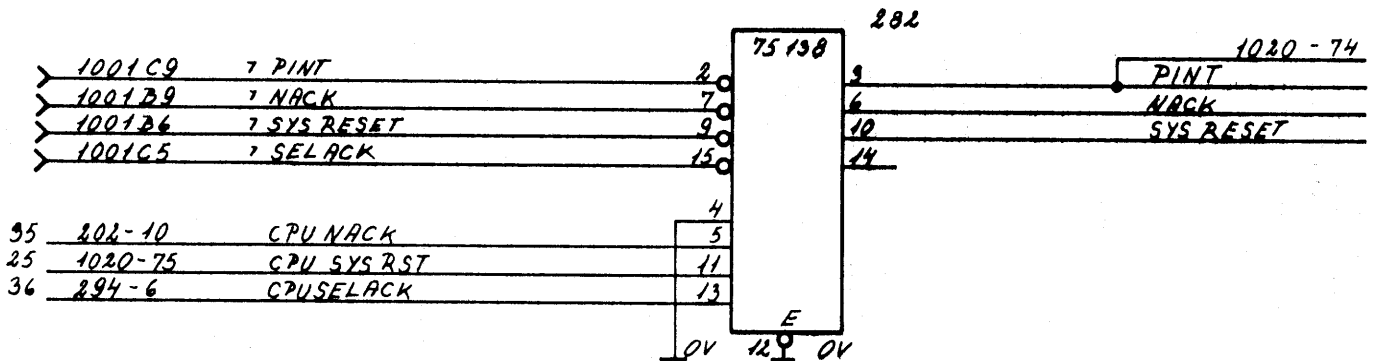
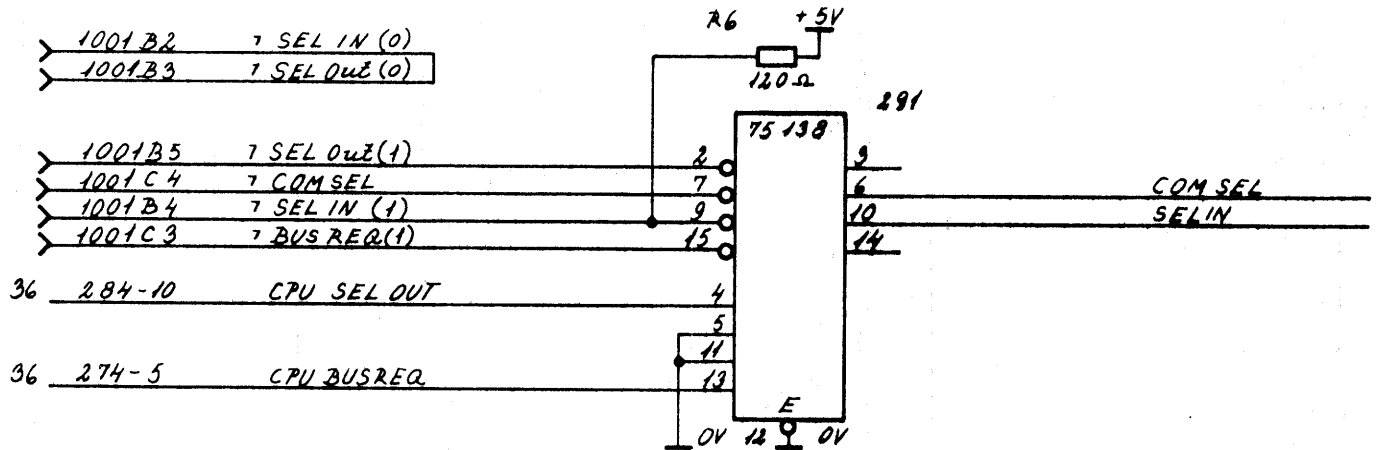
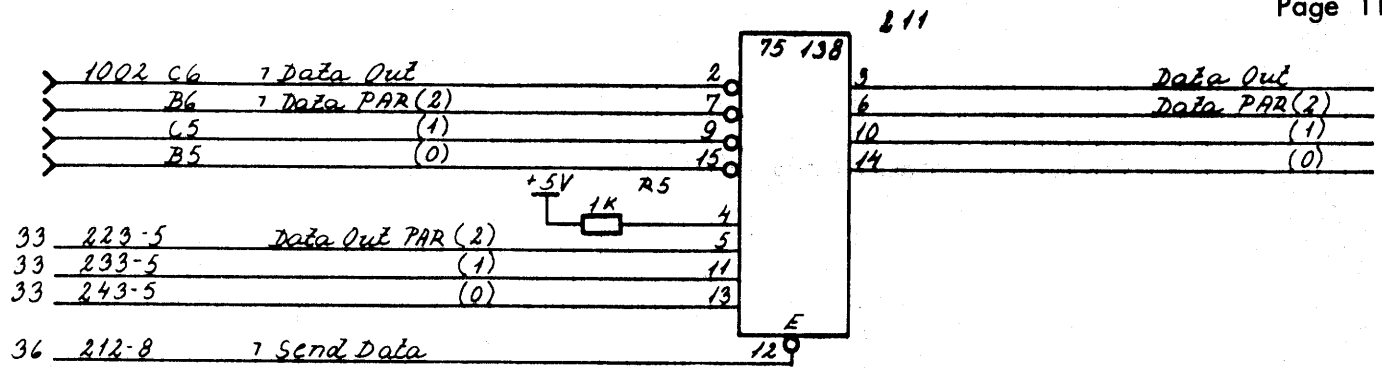
SIGNAL		DESTI- NATION	DESCRIPTION
DATA (0:19) DATA (20:23)		34 30, 34	Data received via the System Bus. Connected to the Data In Register. Bits (20:23) selects interrupt level.
Unit			38A



SIGNAL		DESTINATION	DESCRIPTION
	DATAOUT	35	Indicates data transfer from MASTER TO SLAVE.
	DATAPAR (2)	34	Parity bit for received data bits (16:23).
	DATAPAR (1)	34	Parity bit for received data bits (8:15).
	DATAPAR (0)	34	Parity bit for received data bits (0:7).
	COMSEL	36	Bus master selection control signals.
	SELIN	36	
	PINT	30, 31	Power low warning signal from power supply.
	NACK	35, 36, 39	Data transfer control signal.
	SYSRESET	39	Master reset signal received via System Bus.
	-, POK	30, 39	Power ok signal from power supply. A 0 indicates that the dc voltages are within their limits.
	ACK	36, 39	
	BUSBUSY	36	Data transfer control signals.
	DATARDY	36	
	-, (ACK ! NACK)	35	Controls the BUSTIMEOUT status bit.
	ACK ! NACK	36	ACK or NACK received via the System Bus.
	-, RESET	36	Reset signals generated from System Reset
	RESET	36	and Power Ok signals.

Unit

39A



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ADDRESS					OUTPUT Q(0:7)			
OCTAL	7 FORMAT (7) MIR (16) MIR (1) MIR (2) MIR (3)				SELCOND = 0		SELCOND = 1	
					S1 S0 7FE PUP		S1 S0 7FE PUP	
0	0 0	0 0 0			0 0 1 0		1 1 1 0	
1	0 0	0 0 1			0 0 0 0		1 1 1 0	
2	0 0	0 1 0			0 0 0 1		1 1 1 0	
3	0 0	0 1 1			0 0 0 0		1 1 1 0	
4	0 0	1 0 0			1 0 0 0		1 1 1 0	
5	0 0	1 0 1			1 0 1 0		1 1 1 0	
6	0 0	1 1 0			1 1 0 1		1 1 1 0	
7	0 0	1 1 1			1 1 0 1		1 1 1 0	
10	0 1	0 0 0			0 0 1 0		1 1 0 1	
11	0 1	0 0 1			0 0 0 0		1 1 0 1	
12	0 1	0 1 0			0 0 0 1		1 1 0 1	
13	0 1	0 1 1			0 0 0 0		1 1 0 1	
14	0 1	1 0 0			1 0 0 0		1 1 0 1	
15	0 1	1 0 1			1 0 1 0		1 1 0 1	
16	0 1	1 1 0			1 1 0 1		1 1 0 1	
17	0 1	1 1 1			1 1 0 1		1 1 0 1	
20	1 0	0 0 0			0 0 1 0		0 0 1 0	
21	1 0	0 0 1			0 0 0 0		0 0 0 0	
22	1 0	0 1 0			0 0 0 1		0 0 0 1	
23	1 0	0 1 1			0 0 0 0		0 0 0 0	
24	1 0	1 0 0			1 0 0 0		1 0 0 0	
25	1 0	1 0 1			1 0 1 0		0 0 0 0	
26	1 0	1 1 0			1 1 0 1		1 1 0 1	
27	1 0	1 1 1			1 1 0 1		1 1 0 1	
30	1 1	0 0 0			0 0 1 0		0 0 1 0	
31	1 1	0 0 1			0 0 0 0		0 0 0 0	
32	1 1	0 1 0			0 0 0 1		0 0 0 1	
33	1 1	0 1 1			0 0 0 0		0 0 0 0	
34	1 1	1 0 0			1 0 0 0		1 0 0 0	
35	1 1	1 0 1			1 0 1 0		0 0 0 0	
36	1 1	1 1 0			1 1 0 1		1 1 0 1	
37	1 1	1 1 1			1 1 0 1		1 1 0 1	

ADDRESS					OUTPUT Q(0:7)			
OCTAL	7 POWERUPST 7 FORMAT (7) MIR (17) MIR (1) MIR (2)				SELCOND = 0		SELCOND = 1	
					7ENSEQ 7ENJUMP 7ENMIX 7ENTAB		7ENSEQ 7ENJUMP 7ENMIX 7ENTAB	
0	0 0	0 0 0			0 1 1 1		0 1 1 1	
1	0 0	0 0 1			0 1 1 1		0 1 1 1	
2	0 0	0 1 0			0 1 1 1		0 1 1 1	
3	0 0	0 1 1			0 1 1 1		0 1 1 1	
4	0 0	1 0 0			0 1 1 1		0 1 1 1	
5	0 0	1 0 1			0 1 1 1		0 1 1 1	
6	0 0	1 1 0			0 1 1 1		0 1 1 1	
7	0 0	1 1 1			0 1 1 1		0 1 1 1	
10	0 1	0 0 0			0 1 1 1		0 1 1 1	
11	0 1	0 0 1			0 1 1 1		0 1 1 1	
12	0 1	0 1 0			0 1 1 1		0 1 1 1	
13	0 1	0 1 1			0 1 1 1		0 1 1 1	
14	0 1	1 0 0			0 1 1 1		0 1 1 1	
15	0 1	1 0 1			0 1 1 1		0 1 1 1	
16	0 1	1 1 0			0 1 1 1		0 1 1 1	
17	0 1	1 1 1			0 1 1 1		0 1 1 1	
20	1 0	0 0 0			0 1 1 1		1 0 1 1	
21	1 0	0 0 1			0 1 1 1		1 0 1 1	
22	1 0	0 1 0			0 1 1 1		1 0 1 1	
23	1 0	0 1 1			1 1 1 0		1 0 1 1	
24	1 0	1 0 0			0 1 1 1		1 1 0 1	
25	1 0	1 0 1			0 1 1 1		1 1 0 1	
26	1 0	1 1 0			0 1 1 1		1 1 0 1	
27	1 0	1 1 1			1 1 1 0		1 1 0 1	
30	1 1	0 0 0			0 1 1 1		0 1 1 1	
31	1 1	0 0 1			0 1 1 1		0 1 1 1	
32	1 1	0 1 0			0 1 1 1		0 1 1 1	
33	1 1	0 1 1			1 1 1 0		1 1 1 0	
34	1 1	1 0 0			0 1 1 1		0 1 1 1	
35	1 1	1 0 1			0 1 1 1		0 1 1 1	
36	1 1	1 1 0			0 1 1 1		0 1 1 1	
37	1 1	1 1 1			1 1 1 0		1 1 1 0	

Replaces by Dwg. No.

due to ECN

Replaces Dwg. No.

Design Check

Dwg. Office Check

Drawn by

Designed by

780410 AAT

A/S REGNENCENTRALEN

Unit

CPU810

Dwg. No.

R 12 404

SEQUENCE CONTROL PROM'S

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ADDRESS								OUTPUT Q(0:7)							
OCTAL	POWERUPST MIR (4)	(5)	(6)	MIR (15)	I/O END	MIR (26)	(27)	ENCPMIR	ENCPIMOP	ENCPOOND	ENCPCATCHP	ENCPCREG	CONDL(0)	CONDL(1)	UNUSED
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1
1															
2															
3															
4															
5															
6															
7															
10	0	0	0	0	1	0	0	1	0	0	0	0	0	0	1
11															
12															
13															
14															
15															
16															
17															
20	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1
21															
22															
23															
24															
25															
26															
27															
30	0	0	0	1	1	0	0	1	0	0	0	0	0	0	1
31															
32															
33															
34															
35															
36															
37															
40	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1
41															
42															
43															
44															
45															
46															
47															
50	0	0	1	0	1	0	0	1	0	0	0	0	0	0	1
51															
52															
53															
54															
55															
56															
57															
60	0	0	1	1	0	0	0	1	0	0	0	0	0	0	1
61															
62															
63															
64															
65															
66															
67															
70	0	0	1	1	1	0	0	1	0	0	0	0	0	0	1
71															
72															
73															
74															
75															
76															
77															

ADDRESS								OUTPUT Q(0:7)							
OCTAL	POWERUPST MIR (4)	(5)	(6)	MIR (15)	I/O END	MIR (26)	(27)	ENCPMIR	ENCPIMOP	ENCPOOND	ENCPCATCHP	ENCPCREG	CONDL(0)	CONDL(1)	UNUSED
100	0	1	0	0	0	0	0	1	0	0	0	0	0	0	1
101															
102															
103															
104															
105															
106															
107															
110	0	1	0	0	1	0	0	1	0	0	0	0	0	0	1
111															
112															
113															
114															
115															
116															
117															
120	0	1	0	1	0	0	0	1	0	0	0	0	0	0	1
121															
122															
123															
124															
125															
126															
127															
130	0	1	0	1	1	0	0	1	0	0	0	0	0	0	1
131															
132															
133															
134															
135															
136															
137															
140	0	1	1	0	0	0	0	1	0	0	0	0	0	0	1
141															
142															
143															
144															
145															
146															
147															
150	0	1	1	0	1	0	0	1	0	0	0	0	0	0	1
151															
152															
153															
154															
155															
156															
157															
160	0	1	1	1	0	0	0	1	0	0	0	0	0	0	1
161															
162															
163															
164															
165															
166															
167															
170	0	1	1	1	1	0	0	1	0	0	0	0	0	0	1
171															
172															
173															
174															
175															
176															
177															

Unit
CPU810Dwg. No.
R 12405CONTROL PROM FOR CLOCK SIGNALS
ADDRESS (0:127)

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ADDRESS								OUTPUT Q(0:7)								
OCTAL	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
200	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1
201					0	0	0	1	1	1	0	0	0	0	0	1
202					0	0	1	0	1	1	0	0	0	0	0	1
203					0	0	1	1	1	1	0	0	0	0	0	1
204					0	1	0	0	1	1	0	0	0	0	0	0
205					0	1	0	1	1	1	0	0	0	0	0	1
206					0	1	1	0	1	1	0	0	0	0	0	1
207					0	1	1	1	1	1	0	0	0	0	0	1
210	1	0	0	0	0	1	0	0	0	1	1	0	0	0	0	1
211					1	0	0	1	1	1	0	0	0	0	0	1
212					1	0	1	0	1	1	0	0	0	0	0	1
213					1	0	1	1	1	1	0	0	0	0	0	1
214					1	1	0	0	1	1	0	0	0	0	0	1
215					1	1	0	1	1	1	0	0	0	0	0	1
216					1	1	1	0	1	1	0	0	0	0	0	1
217					1	1	1	1	1	1	0	0	0	0	0	1
220	1	0	0	0	1	0	0	0	0	1	0	1	1	0	0	0
221					0	0	0	1	1	0	1	1	0	0	0	0
222					0	0	1	0	1	0	1	1	0	0	0	0
223					0	0	1	1	1	0	1	1	0	0	0	0
224					0	1	0	0	1	0	1	1	0	0	0	1
225					0	1	0	1	1	0	1	1	0	0	0	1
226					0	1	1	0	1	0	1	1	0	0	0	1
227					0	1	1	1	1	0	1	1	0	0	0	1
230	1	0	0	0	1	1	0	0	0	1	0	1	1	0	0	0
231					1	0	0	1	1	0	1	1	0	0	0	0
232					1	0	1	0	1	0	1	1	0	0	0	0
233					1	0	1	1	1	0	1	1	0	0	0	0
234					1	1	0	0	1	0	1	1	0	0	0	0
235					1	1	0	1	1	0	1	1	0	0	0	0
236					1	1	1	0	1	0	1	1	0	0	0	0
237					1	1	1	1	1	0	1	1	0	0	0	0
240	1	0	1	0	0	0	0	0	0	1	0	1	0	1	0	0
241					0	0	0	1	1	0	1	0	1	0	0	0
242					0	0	1	0	1	0	1	0	1	0	0	0
243					0	0	1	1	1	0	1	0	1	0	0	0
244					0	1	0	0	1	0	1	0	1	0	0	0
245					0	1	0	1	1	0	1	0	1	0	0	0
246					0	1	1	0	1	0	1	0	1	0	0	0
247					0	1	1	1	1	0	1	0	1	0	0	0
250	1	0	1	0	1	0	0	0	0	1	0	1	0	1	0	0
251					1	0	0	1	1	0	1	0	1	0	0	0
252					1	0	1	0	1	0	1	0	1	0	0	0
253					1	0	1	1	1	0	1	0	1	0	0	0
254					1	1	0	0	1	0	1	0	1	0	0	0
255					1	1	0	1	1	0	1	0	1	0	0	0
256					1	1	1	0	1	0	1	0	1	0	0	0
257					1	1	1	1	1	0	1	0	1	0	0	0
260	1	0	1	1	0	0	0	0	0	1	0	1	0	1	0	0
261					0	0	0	1	1	0	1	0	1	0	0	0
262					0	0	1	0	1	0	1	0	1	0	0	0
263					0	0	1	1	1	0	1	0	1	0	0	0
264					0	1	0	0	1	0	1	0	1	0	0	0
265					0	1	0	1	1	0	1	0	1	0	0	0
266					0	1	1	0	1	0	1	0	1	0	0	0
267					0	1	1	1	1	0	1	0	1	0	0	0
270	1	0	1	1	1	0	0	0	0	1	0	1	0	1	0	0
271					1	0	0	1	1	0	1	0	1	0	0	0
272					1	0	1	0	1	0	1	0	1	0	0	0
273					1	0	1	1	1	0	1	0	1	0	0	0
274					1	1	0	0	1	0	1	0	1	0	0	0
275					1	1	0	1	1	0	1	0	1	0	0	0
276					1	1	1	0	1	0	1	0	1	0	0	0
277					1	1	1	1	1	0	1	0	1	0	0	0

ADDRESS		OUTPUT Q(0:7)									
OCTAL	7 POWERUPRST MIR(4) (5) (6) MIR(15) I/O END MIR(26) (27)	ENCMPR ENCMPOP ENCPOND ENCPSRATCHP ENCPRG CONDLD(0) CONDLD(1) UNUSED									
300	1 1 0 0	0 0 0 0	1 0 1 0	0 0 0 0	1						
301		0 0 0 1	1 0 1 0	0 0 0 1	1						
302		0 0 1 0	1 0 1 0	0 0 1 0	1						
303		0 0 1 1	1 0 1 0	0 0 1 1	1						
304		0 1 0 0	1 0 1 0	0 0 0 0	1						
305		0 1 0 1	1 0 1 0	0 0 0 1	1						
306		0 1 1 0	1 0 1 0	0 0 1 0	1						
307		0 1 1 1	1 0 1 0	0 0 1 1	1						
310	1 1 0 0	1 0 0 0	1 0 1 0	0 0 0 0	1						
311		1 0 0 1	1 0 1 0	0 0 0 1	1						
312		1 0 1 0	1 0 1 0	0 0 1 0	1						
313		1 0 1 1	1 0 1 0	0 0 1 1	1						
314		1 1 0 0	1 0 1 0	0 0 0 0	1						
315		1 1 0 1	1 0 1 0	0 0 0 1	1						
316		1 1 1 0	1 0 1 0	0 0 1 0	1						
317		1 1 1 1	1 0 1 0	0 0 1 1	1						
320	1 1 0 1	0 0 0 0	1 0 1 0	0 0 0 0	1						
321		0 0 0 1	1 0 1 0	0 0 0 1	1						
322		0 0 1 0	1 0 1 0	0 0 1 0	1						
323		0 0 1 1	1 0 1 0	0 0 1 1	1						
324		0 1 0 0	1 0 1 0	0 0 0 0	1						
325		0 1 0 1	1 0 1 0	0 0 0 1	1						
326		0 1 1 0	1 0 1 0	0 0 1 0	1						
327		0 1 1 1	1 0 1 0	0 0 1 1	1						
330	1 1 0 1	1 0 0 0	1 0 1 0	0 0 0 0	1						
331		1 0 0 1	1 0 1 0	0 0 0 1	1						
332		1 0 1 0	1 0 1 0	0 0 1 0	1						
333		1 0 1 1	1 0 1 0	0 0 1 1	1						
334		1 1 0 0	1 0 1 0	0 0 0 0	1						
335		1 1 0 1	1 0 1 0	0 0 0 1	1						
336		1 1 1 0	1 0 1 0	0 0 1 0	1						
337		1 1 1 1	1 0 1 0	0 0 1 1	1						
340	1 1 1 0	0 0 0 0	1 0 1 0	0 0 0 0	1						
341		0 0 0 1	1 0 1 0	0 0 0 1	1						
342		0 0 1 0	1 0 1 0	0 0 1 0	1						
343		0 0 1 1	1 0 1 0	0 0 1 1	1						
344		0 1 0 0	1 0 1 0	0 0 0 0	1						
345		0 1 0 1	1 0 1 0	0 0 0 1	1						
346		0 1 1 0	1 0 1 0	0 0 1 0	1						
347		0 1 1 1	1 0 1 0	0 0 1 1	1						
350	1 1 1 0	1 0 0 0	1 0 1 0	0 0 0 0	1						
351		1 0 0 1	1 0 1 0	0 0 0 1	1						
352		1 0 1 0	1 0 1 0	0 0 1 0	1						
353		1 0 1 1	1 0 1 0	0 0 1 1	1						
354		1 1 0 0	1 0 1 0	0 0 0 0	1						
355		1 1 0 1	1 0 1 0	0 0 0 1	1						
356		1 1 1 0	1 0 1 0	0 0 1 0	1						
357		1 1 1 1	1 0 1 0	0 0 1 1	1						
360	1 1 1 1	0 0 0 0	1 0 0 0	0 0 0 0	1						
361		0 0 0 1	1 0 0 0	0 0 0 1	1						
362		0 0 1 0	1 0 0 0	0 0 0 0	1						
363		0 0 1 1	1 0 0 0	0 0 0 1	1						
364		0 1 0 0	1 0 0 0	0 0 0 0	1						
365		0 1 0 1	1 0 0 0	0 0 0 0	1						
366		0 1 1 0	1 0 0 0	0 0 0 1	1						
367		0 1 1 1	1 0 0 0	0 0 0 1	1						
370	1 1 1 1	1 0 0 0	0 0 0 0	0 0 0 0	1						
371		1 0 0 1	0 0 0 0	0 0 0 0	1						
372		1 0 1 0	0 0 0 0	0 0 0 0	1						
373		1 0 1 1	0 0 0 0	0 0 0 0	1						
374		1 1 0 0	1 0 0 0	0 0 0 0	1						
375		1 1 0 1	1 0 0 0	0 0 0 0	1						
376		1 1 1 0	1 0 0 0	0 0 0 0	1						
377		1 1 1 1	1 0 0 0	0 0 0 0	1						

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ROM No.	POS No.	USAGE	
ROA005	15	Microprogram sequence control	
006	16		
007	36		
ROA008	54	Clock Signal Control	
009	44		
ROA040	382	Control store (0:1023)	(0:3)
041	372		(4:7)
042	362		(8:11)
043	352		(12:15)
044	342		(16:19)
045	332		(20:23)
046	322		(24:27)
047	312		(28:31)
048	302		(32:35)
ROA151	381	Control store (1024:2047)	(0:3)
152	371		(4:7)
153	361		(8:11)
154	351		(12:15)
155	341		(16:19)
156	331		(20:23)
157	321		(24:27)
158	311		(28:31)
159	301		(32:35)

Unit	CPU810	PROM's USED ON CPU 810	43
Dwg. No.	R21246		

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A/S REGENTRALEN	Designed by	Drawn by	Dwg. Office	Design Check	Replaces Dwg. No.	due to ECN	Revised by Dwg. No.
	781002 AAJ						

CONNECTOR: 1001

PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME
A1		+5 VOLTS	B1		+5 VOLTS	C1		+5 VOLTS
A2		0 VOLT	B2		SELIN (0)	C2		BUSREQ (0)
A3		0 VOLT	B3		SELOUT (0)	C3	291-15	BUSREQ (1)
A4		0 VOLT	B4		SELIN (1)	C4		COMSEL
A5		0 VOLT	B5		SELOUT (1)	C5	282-15	SELACK
A6		0 VOLT	B6	291-2	SYS RESET	C6		POB
A7		0 VOLT	B7	282-9	DATA RY	C7	281-9	BUSBUSY
A8		0 VOLT	B8	281-15	ACK	C8		POK
A9		0 VOLT	B9	281-7	NACK	C9		PINT
A10		0 VOLT	B10	282-7	ADDR (0)	C10	272-9	ADDR (1)
A11		0 VOLT	B11	272-15	ADDR (2)	C11	271-9	ADDR (3)
A12		0 VOLT	B12	271-15	ADDR (4)	C12	271-2	ADDR (5)
A13		0 VOLT	B13	271-7	ADDR (6)	C13	272-2	ADDR (7)
A14		0 VOLT	B14	272-7	ADDR (8)	C14	262-9	ADDR (9)
A15		0 VOLT	B15	262-15	ADDR (10)	C15	261-9	ADDR (11)
A16		0 VOLT	B16	261-15	ADDR (12)	C16	261-2	ADDR (13)
A17		0 VOLT	B17	261-7	ADDR (14)	C17	262-2	ADDR (15)
A18		0 VOLT	B18	262-7	ADDR (16)	C18	252-9	ADDR (17)
A19		0 VOLT	B19	252-15	ADDR (18)	C19	251-9	ADDR (19)
A20		0 VOLT	B20	251-15	ADDR (20)	C20	251-2	ADDR (21)
A21		0 VOLT	B21	252-7	ADDR (22)	C21	252-2	ADDRPAR
A22		0 VOLT	B22	242-15	DATA (0)	C22	242-9	DATA (1)
A23		0 VOLT	B23	241-15	DATA (2)	C23	241-9	DATA (3)
A24		0 VOLT	B24	241-7	DATA (4)	C24	241-2	DATA (5)
A25		0 VOLT	B25	242-7	DATA (6)	C25	242-2	DATA (7)
A26		0 VOLT	B26	232-15	DATA (8)	C26	232-9	DATA (9)
A27		0 VOLT	B27	231-15	DATA (10)	C27	231-9	DATA (11)
A28		0 VOLT	B28	231-7	DATA (12)	C28	231-2	DATA (13)
A29		0 VOLT	B29	232-7	DATA (14)	C29	232-2	DATA (15)
A30		0 VOLT	B30	222-15	DATA (16)	C30	222-9	DATA (17)
A31		NOT USED	B31		NOT USED	C31		NOT USED
A32		+5 VOLTS	B32		+5 VOLTS	C32		+5 VOLTS

CONNECTOR: 1002

PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME
A1		+5 VOLTS	B1		+5 VOLTS	C1		+5 VOLTS
A2		0 VOLT	B2	221-15	DATA (18)	C2	221-9	DATA (19)
A3		0 VOLT	B3	221-7	DATA (20)	C3	221-2	DATA (21)
A4		0 VOLT	B4	222-7	DATA (22)	C4	222-2	DATA (23)
A5		0 VOLT	B5	211-15	DATAPAR (0)	C5	211-9	DATAPAR (1)
A6		0 VOLT	B6	211-7	DATAPAR (2)	C6	211-2	DATAPAR (2)

Unit
CPU 810

Dwg. No.
R12577

PLUG LIST FOR RC8000 SYSTEM BUS

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CONNECTOR: 1004					
PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME
A1		0 VOLT	B1	10-2	TCPBUSOUT (0)
A2		0 VOLT	B2	10-5	(1)
A3		0 VOLT	B3	10-6	(2)
A4		0 VOLT	B4	10-9	(3)
A5		0 VOLT	B5	10-12	(4)
A6		0 VOLT	B6	10-15	(5)
A7		0 VOLT	B7	10-16	(6)
A8		0 VOLT	B8	10-19	(7)
A9		0 VOLT	B9	TCA 801	TCPDATAIN (0)
A10		0 VOLT	B10	TCA 801	(1)
A11		0 VOLT	B11	TCA 801	(2)
A12		0 VOLT	B12	TCA 801	(3)
A13		0 VOLT	B13	TCA 801	(4)
A14		0 VOLT	B14	TCA 801	(5)
A15		0 VOLT	B15	TCA 801	(6)
A16		0 VOLT	B16	TCA 801	(7)
A17		0 VOLT	B17	19-18	-, TCPOUTRDY
A18		0 VOLT	B18	19-16	-, TCPINACK
A19		0 VOLT	B19	TCA 801	-, TCPINRDY
A20		0 VOLT	B20	TCA 801	-, TCPOUTACK
A21		0 VOLT	B21		0 VOLT
A22		0 VOLT	B22		0 VOLT
A23		0 VOLT	B23		+5 VOLTS
A24		+5 VOLTS	B24		+5 VOLTS
A25		+5 VOLTS	B25		+5 VOLTS

CONNECTOR: 1005					
PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME
A1	147-2	AUTOLOAD NC	B1		AUTOLOAD C (0 VOLT)
A2	147-1	AUTOLOAD NO	B2		AUTOLOAD C (0 VOLT)
A3	150-4	POWER OK LAMP -	B3	140-2	POWER OK LAMP +
A4	150-9	RUN LAMP -	B4	140-1	RUN LAMP +
A5	150-11	AUTOLOAD LAMP -	B5	139-1	AUTOLOAD LAMP +
A6		-, REMOTE AUTOLOAD	B6		0 VOLT
A7		UNUSED	B7		UNUSED
A8		-"	B8		-"
A9		-"	B9		-"
A10		-"	B10		-"
A11		-"	B11		-"
A12		-"	B12		-"
A13		-"	B13		-"
A14		-"	B14		-"
A15		-"	B15		-"
A16		-"	B16		-"
A17		-"	B17		-"
A18		-"	B18		-"
A19		-"	B19		-"
A20		-"	B20		-"
A21		-"	B21		-"
A22		-"	B22		-"
A23		-"	B23		-"
A24		-"	B24		-"
A25		-"	B25		-"

Unit
CPU 810

PLUG LIST FOR

Dwg. No.

CPU 810 CONNECTIONS TO QCP 802 and TCA 801

R12578

Rep. by Dwg. No.

due to ECN

Replaces Dwg. No.

Design Check

Dwg. Office

Drawn by

Designed by

781012 AAJ

A/S REGNENTRALEN

dec 18 140

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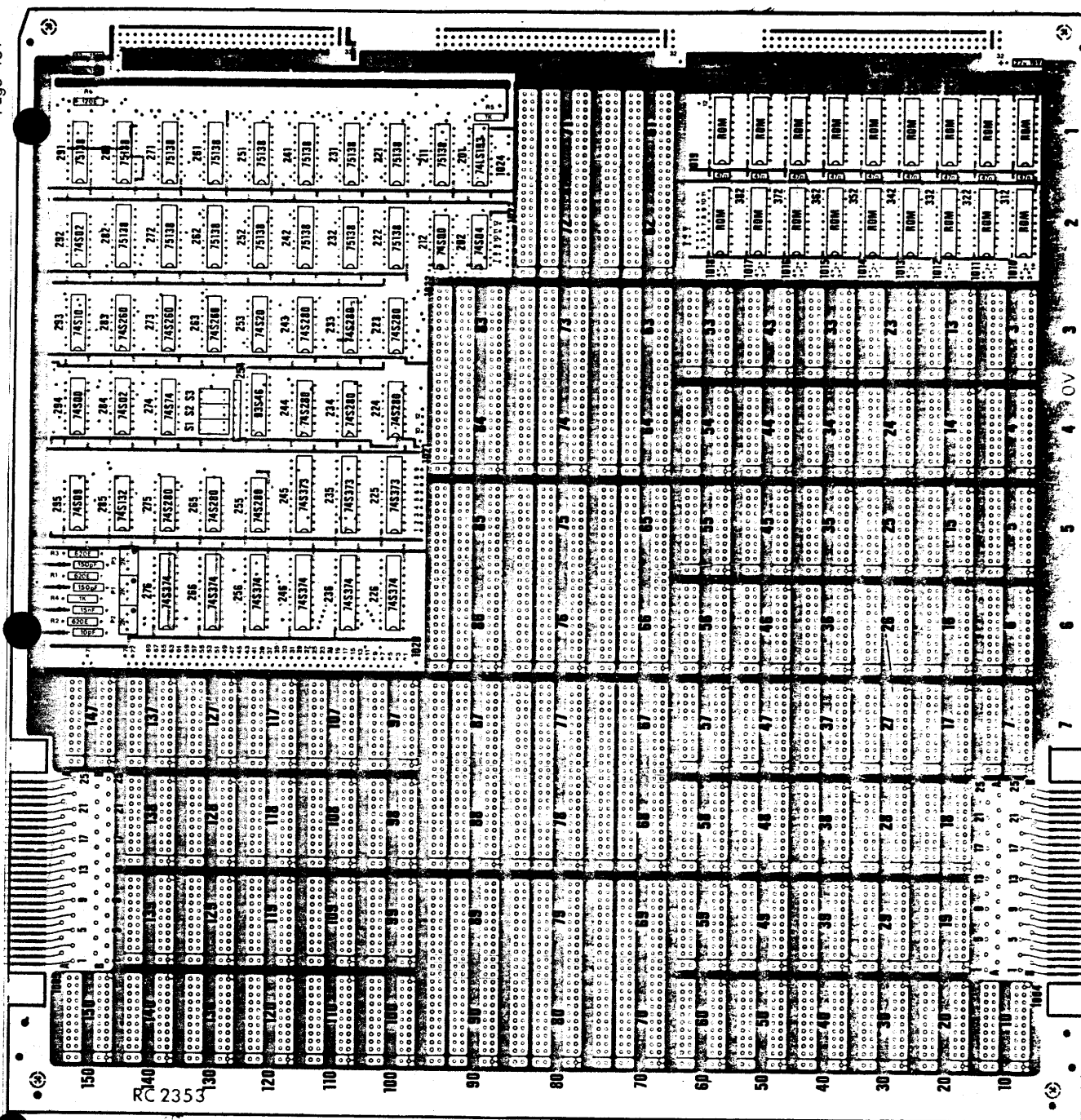
Connector I: ELCO Receptacle 8026-033-000-801
Connector II: ELCO Receptacle 8026-033-000-801
Connector III: Edge connector 2 x 25 contacts, solder
Cable: 6 x 2 x 0.14 mm²
Length: 0.75 m

I PIN	WIRE	III PIN	SIGNAL NAME
A2		A1	AUTOLOAD NC
A3		B1	AUTOLOAD C
A4		A2	AUTOLOAD NO
A5		B2	AUTOLOAD C
A6		A3	POWER OK LAMP -
A7		B3	POWER OK LAMP +
B7		A4	RUN LAMP -
B6		B4	RUN LAMP +
B5		A5	AUTOLOAD LAMP -
B3		B5	AUTOLOAD LAMP +
II PIN			
A2		A6	-, REMOTE AUTOLOAD
A3		B6	0 VOLT

Replaced by Dwg. No.
due to ECN
Replaces Dwg. No.
Design Check
Dwg. Office Check
Drawn by
Designed by
781022 AAJ
A/S REGN. CENTRALEN

Unit	CPU 810	CBL 826	
Dwg. No.	R 12579	INTERNAL CABLE FOR CPU 810	

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CPU 810:

Components at Wire-
Wrap Areas - se
Diagrams.

Resistors:

R1 to R5
5% 1/8W Carbon
R6:
2% 0.4W Metalfilm.

POS 254 SIL

216CH102X5PD
7 x 1K, +5V Pin 1

Switches S1, S2, S3,

Device Code Selection (Diagram 35)

Red dot = 0

White dot = 1

POT Meter:

Bourns 2K

Funktion see

Diagram 35 and 36.

ROM's:

POS 301 to 382

ROM Numbers are

listed separately

se Diagram 43.

RC 2353 PCB ASSEMBLY DRAWING.

Kunnen een bryker og heftes on. en chip dit den brænde
Kor der dit allerede. er en begyning dit ad nedfotografere. I gøres dette-og
manuallene skal ikke heftes - Kun der 1 stk. Briløst papir indlæses bryet.

CPU 810:

Components at Wire-
Wrap Areas - see
Diagrams.

Resistors:

R1 to R5
5% 1/8W Carbon
R6:
2% 0.4W Metallfilm.

POS 254 SIL

216CH102X 5PD
7 x 1K, +5V Pin 1

Switches S1, S2, S3,

Device Code Selection (Diagram 35)

Red dot = 0

White dot = 1

POT Meter:

Bourns 2K

Funktion see

Diagram 35 and 36.

ROM's:

POS 301 to 382
ROM Numbers are
listed separately
see Diagram 43.

