
Title:

BCU802, BTU802, and BTU803
TECHNICAL MANUAL

 **REGNECENTRALEN**

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Abstract:

This manual contains block diagram, timing diagram, logic diagram, functional description, assembly drawings, and plug lists for the BCU802, the BTU802, and the BTU803 Bus Control and Bus Termination Units.

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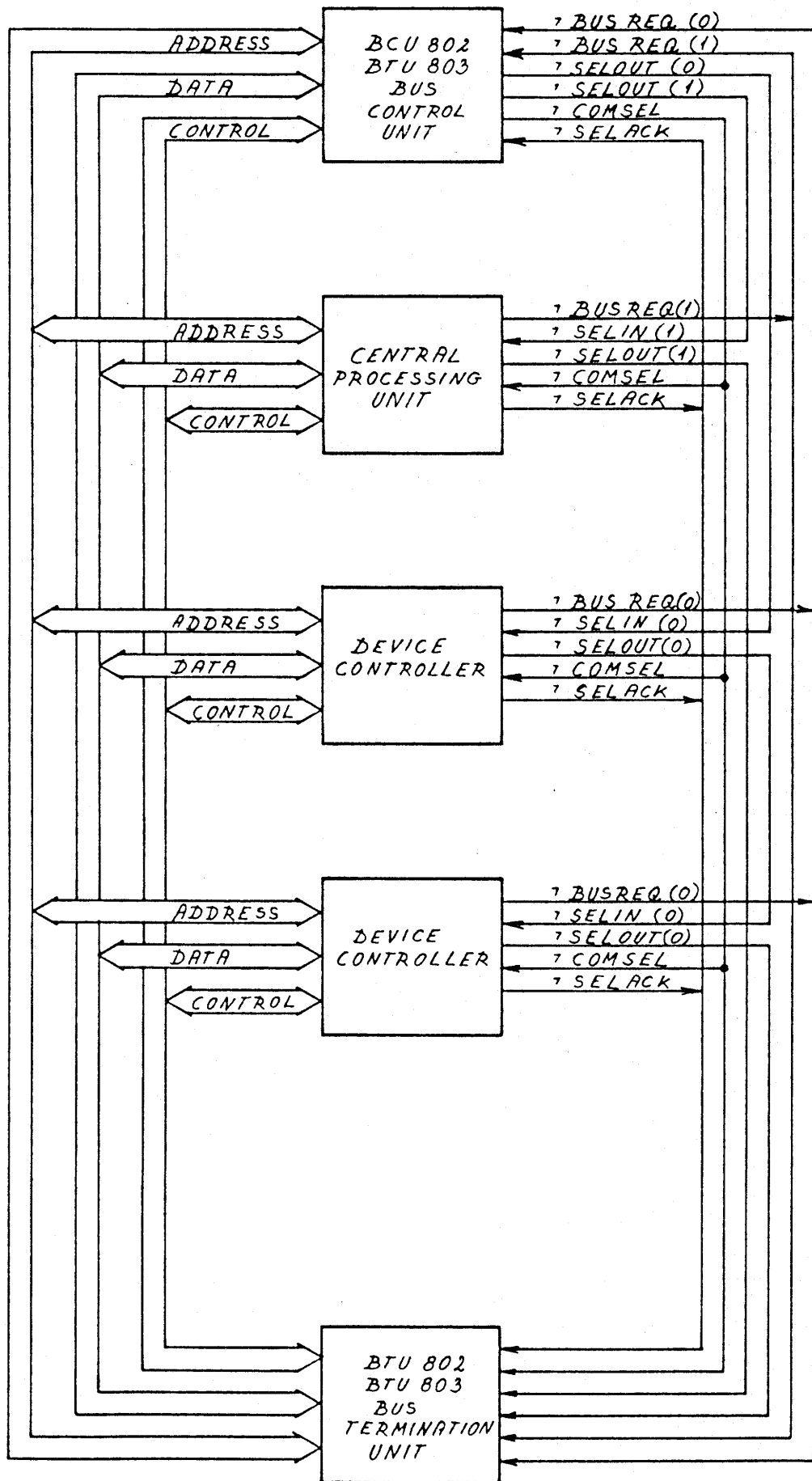
1. INTRODUCTION.

1.

The RC8000 System Bus is a unified bus interconnecting the control processing unit, the main memory and the device controllers. None of the units connected to the System Bus have any special status. Communication between two units on the bus takes place in a master-slave relationship. During any bus operation one unit, the bus master, controls the bus and receives data from or transmits data to the addressed unit, the slave. The Bus Control Unit BCU802 controls the bus master selection, and together with the Bus Termination Unit BTU803 it terminates one end of the bidirectional address, data, and control signals. The other end is terminated by the Bus Termination Units BTU802 and BTU803.

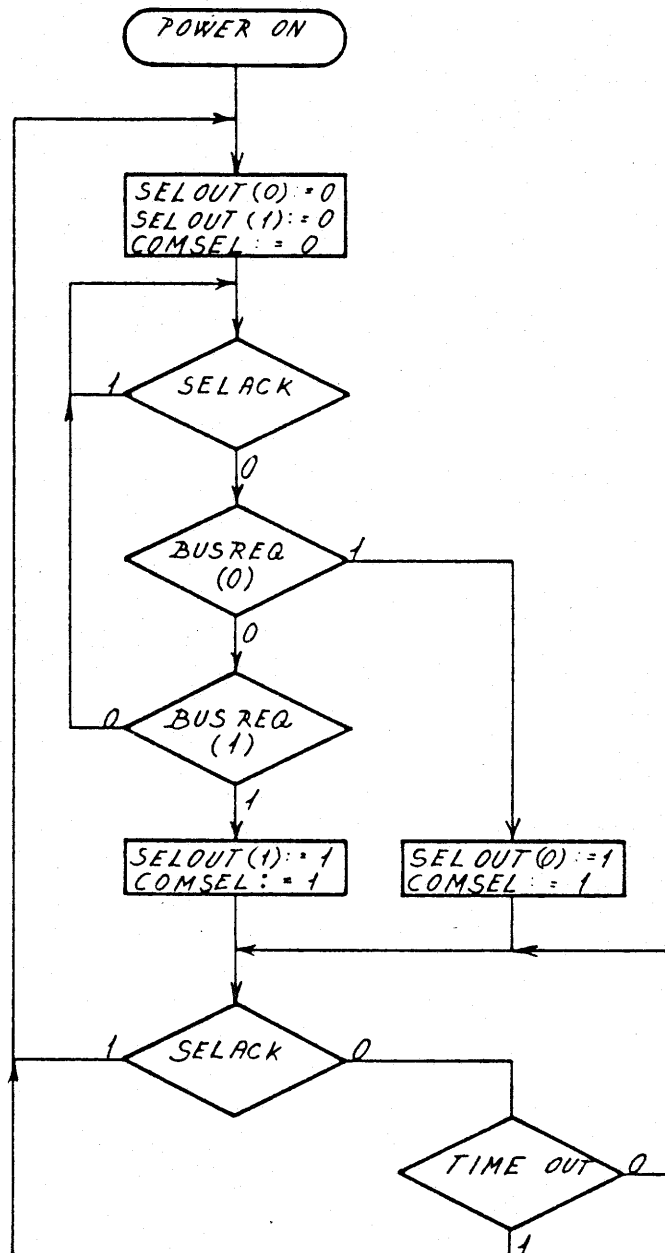
Termination of the end of the System Bus, which is opposite to the end with the Bus Control Unit (BCU802, BTU803), may be omitted in small systems consisting of one 5-slot chassis.

BUS MASTER SELECTION CONTROL SIGNALS



May be omitted in small systems consisting of one 5-slot chassis.

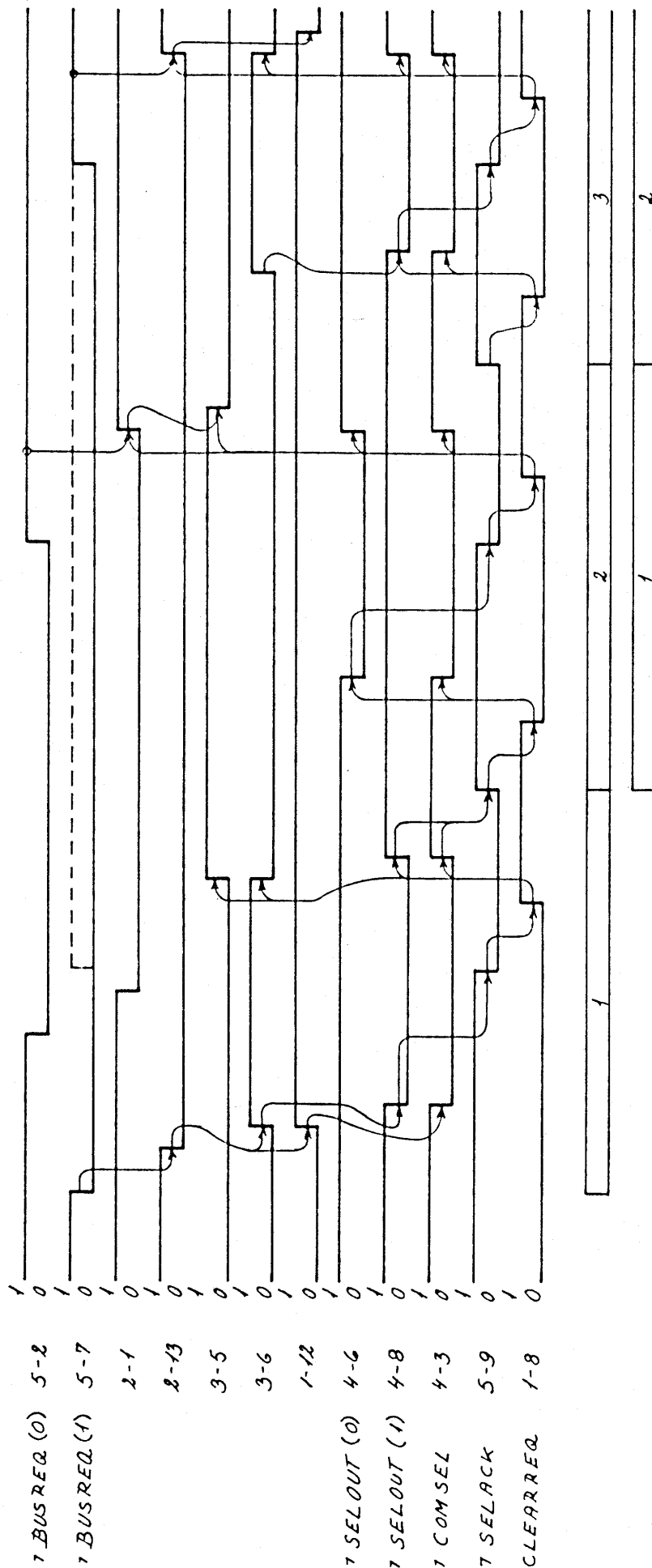
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TIME OUT: COMSEL = 1 and SELACK = 0 for more than approximately 5 microseconds

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The diagram shows the sequence of control signals to and from BC802 for selection of 3 busmasters. Number 1 and 3 uses BUSREQ(1) and number 2 uses BUSREQ(1). BUSREQ(0) has higher priority than BUSREQ(1).

5. FUNCTIONAL DESCRIPTION.

5.

A unit which wants to become bus master sends a bus request on one of the two bus request lines, BUSREQ(0) and BUSREQ(1). Requests on the BUSREQ(0) line have the highest priority and is answered before requests on the BUSREQ(1) line. The BCU802 answers a request by sending the corresponding select out signal, SELOUT(0) or SELOUT(1). SELOUT(0) and SELOUT(1) is daisy chained through the units as shown on the block diagram. The select out signal ripples through the units until it reaches a unit which is requesting bus control. This unit breaks the chain and sends a selection acknowledge signal, SELACK to the BCU802. This causes the BCU802 to clear the select out signal. The unit which sends the SELACK signal now waits until the current data transfer is terminated and then clears SELACK and starts its data transfer. When SELACK is cleared the BCU802 begins the selection of the next bus master if there is a bus request. The selection of the next bus master is thus executed in parallel with the current data transfer. A common select signal, is send to all units (not daisy chained) simultaneously with SELOUT(0) or SELOUT(1). The purpose of COMSEL is to reduce the delay in the daisy chain when SELOUT(0) or SELOUT(1) is cleared.

If the BCU802 not has received a SELACK within approximately 5 microseconds after it has send a SELOUT(0) or a SELOUT(1) it terminates the current bus master selection and looks for new bus requests.

Flow diagram and timing diagram for the bus master selection control sequence is shown in section 3 and 4 of this manual.

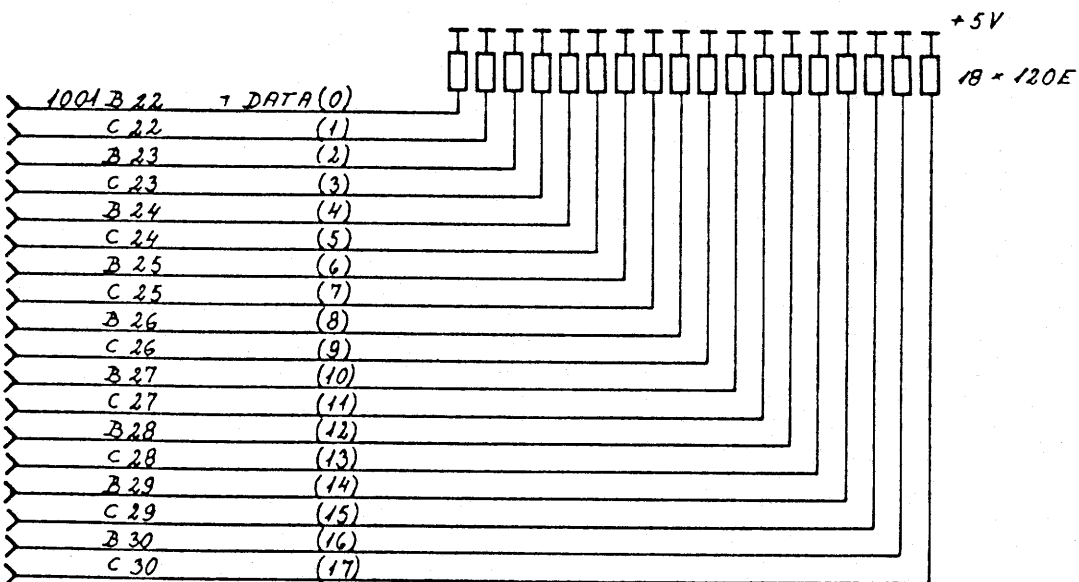
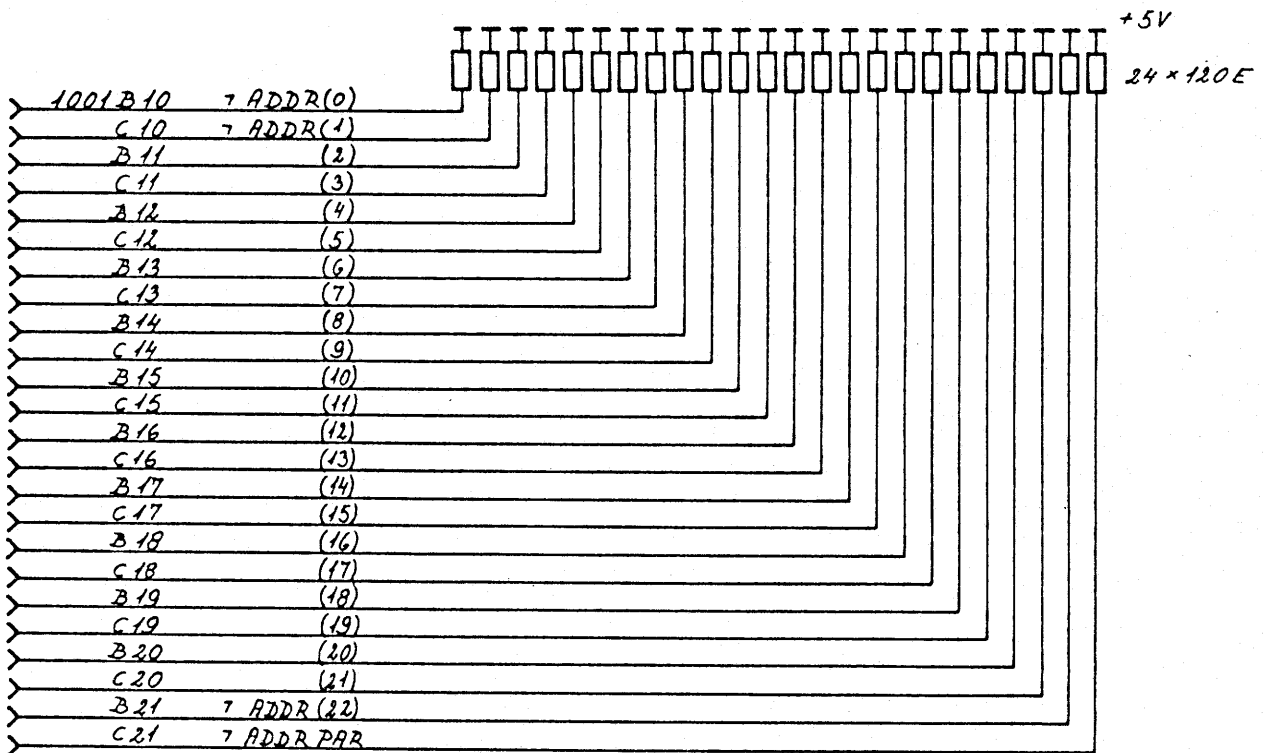
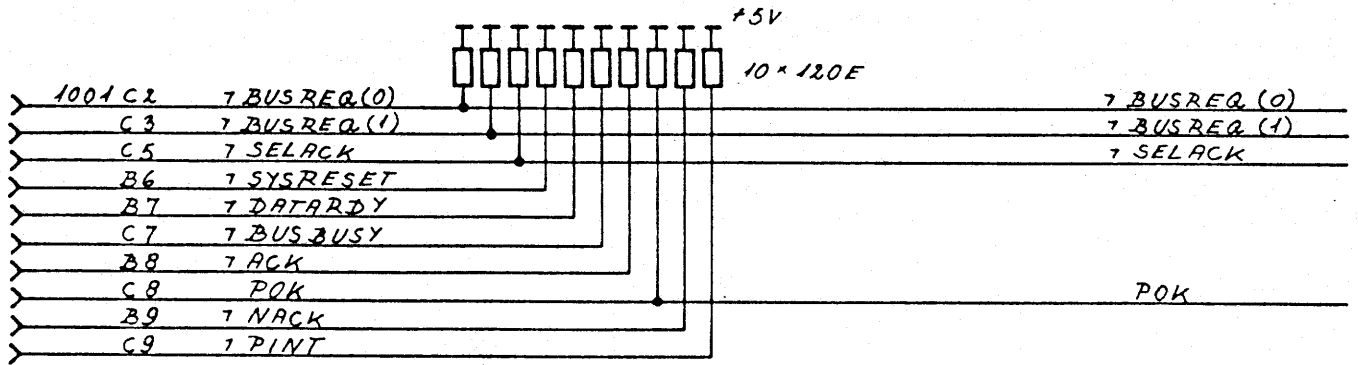
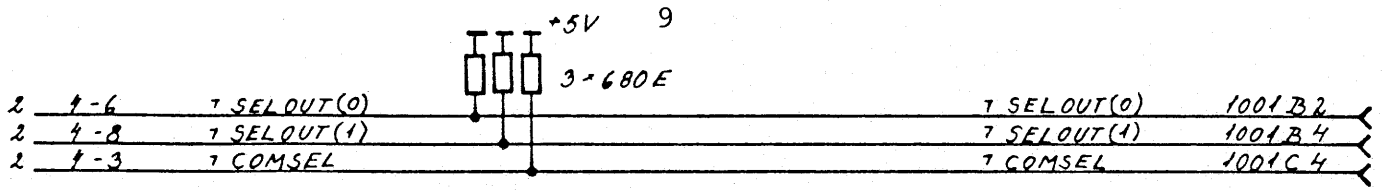
6. LOGIC DIAGRAMS AND SIGNAL DESCRIPTIONS.

6.

The logic diagrams are placed on the right hand pages (odd page numbers). The signal description belonging to a diagram is placed on the corresponding left hand page.

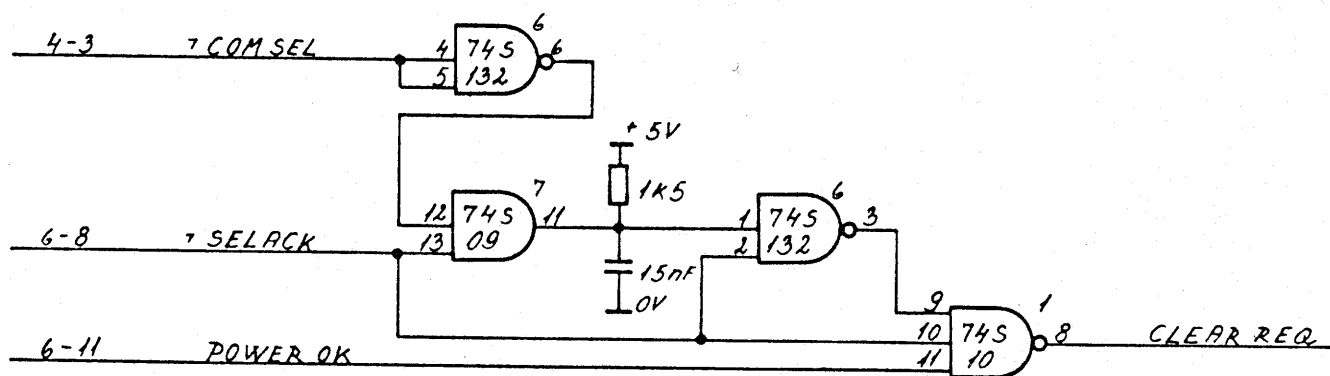
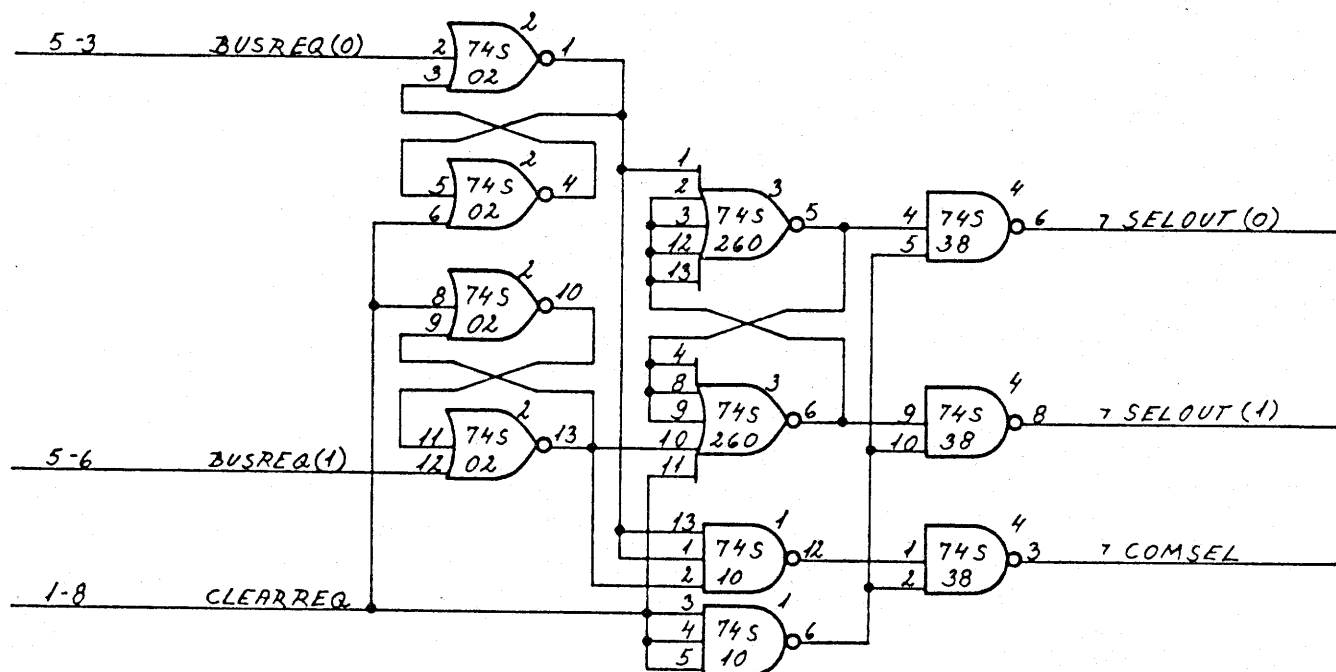
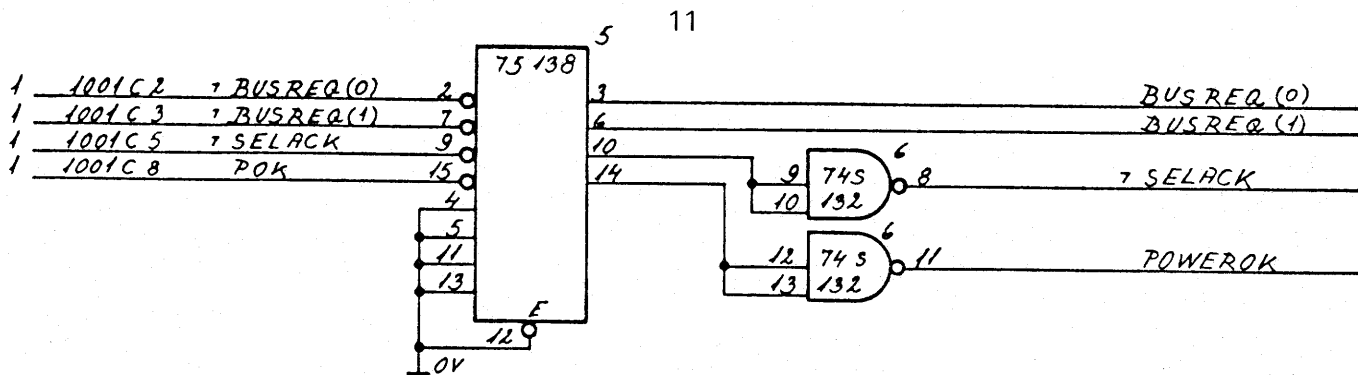
The signal description consists of a listing of the signals, which are generated on the logic diagram and which are transferred to other diagrams. For each signal is indicated on which diagrams it is used, and its function is shortly described.

References between logic diagrams use the diagram number placed in the lower right corner of the diagram.



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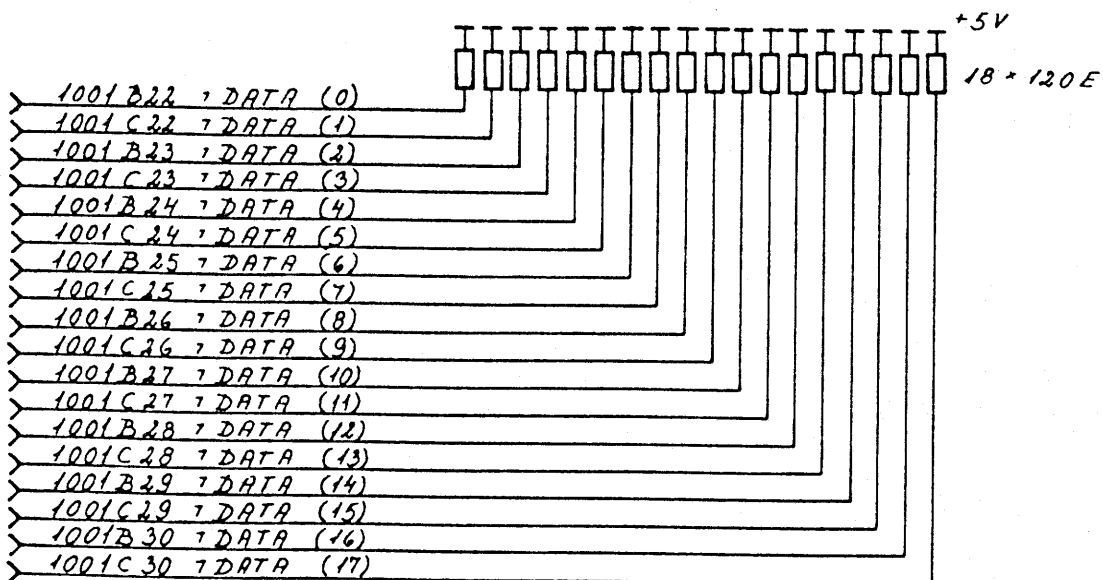
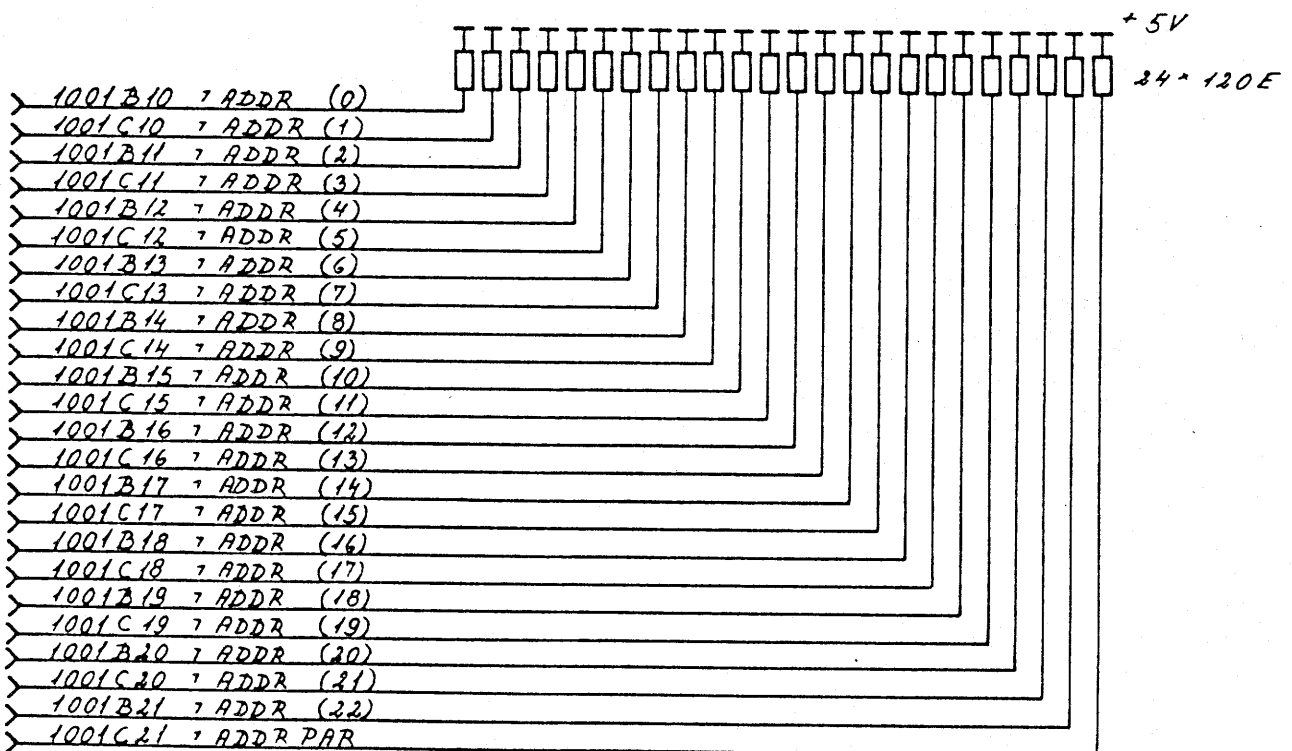
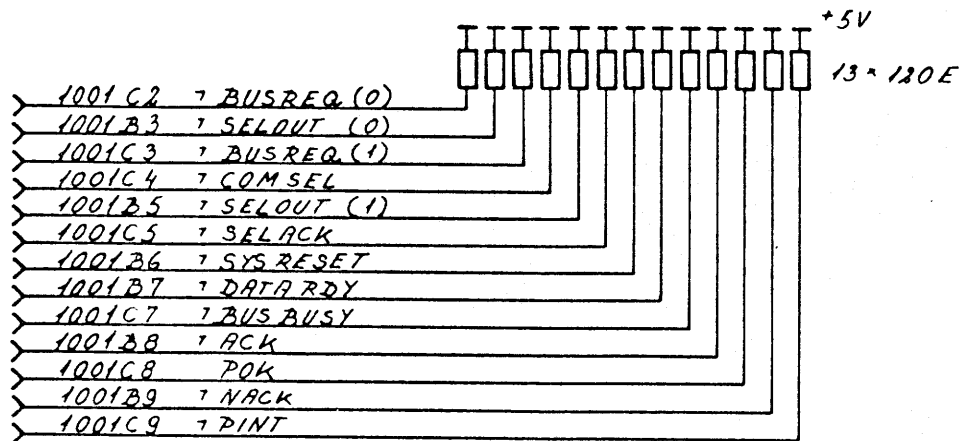
SIGNAL	DESTI- NATION	DESCRIPTION
BUSREQ(0)	2	Bus request with the highest priority.
BUSREQ(1)	2	Bus request with the lowest priority.
7SELACK	2	Selection acknowledge signal from the unit which has been selected as the next bus master.
POWEROK	2	Indicates that the dc voltages are within their limits.
7SELOUT(0)	1	Generated by BCU when a BUSREQ(0) is received.
7SELOUT(1)	1	Generated by BCU when a BUSREQ(1) is received.
7COMSEL	1	Generated simultaneously with SELOUT(0) and SELOUT(1).
CLEARREQ	2	Reset signal for bus request latches.
Unit BCU802		2A



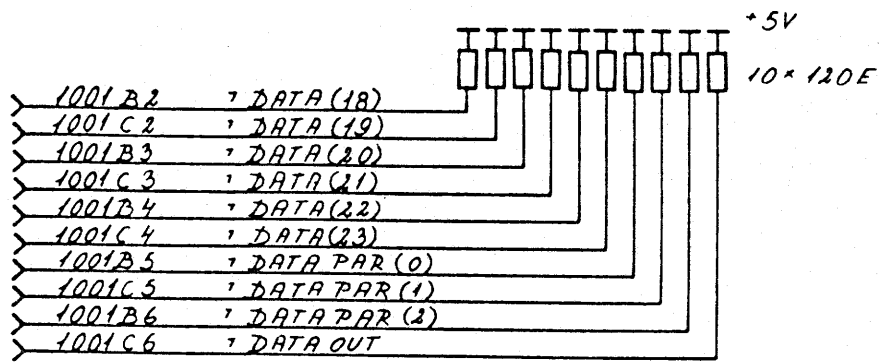
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BCU802
R12661

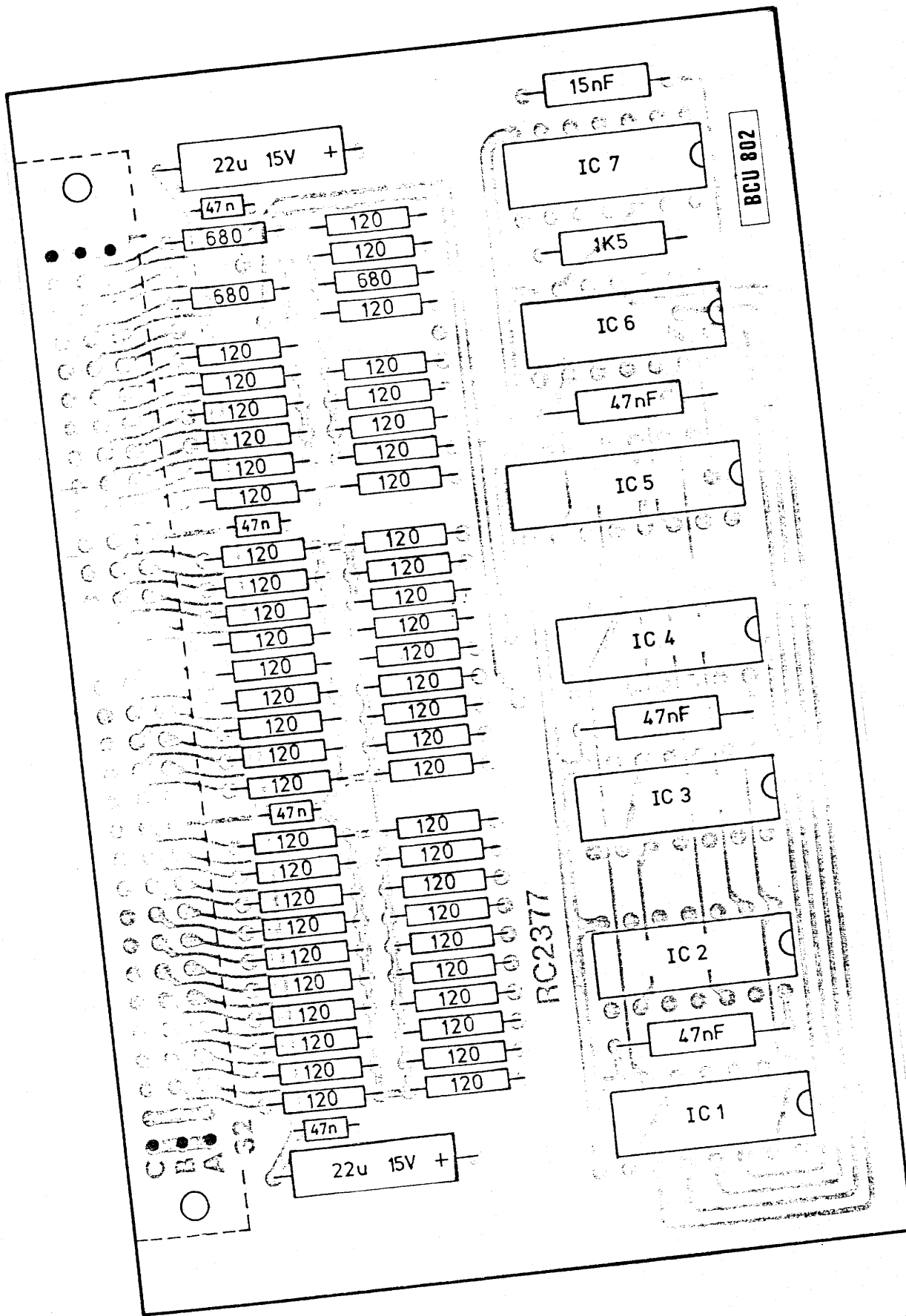
BUS MASTER SELECTION CONTROL LOGIC



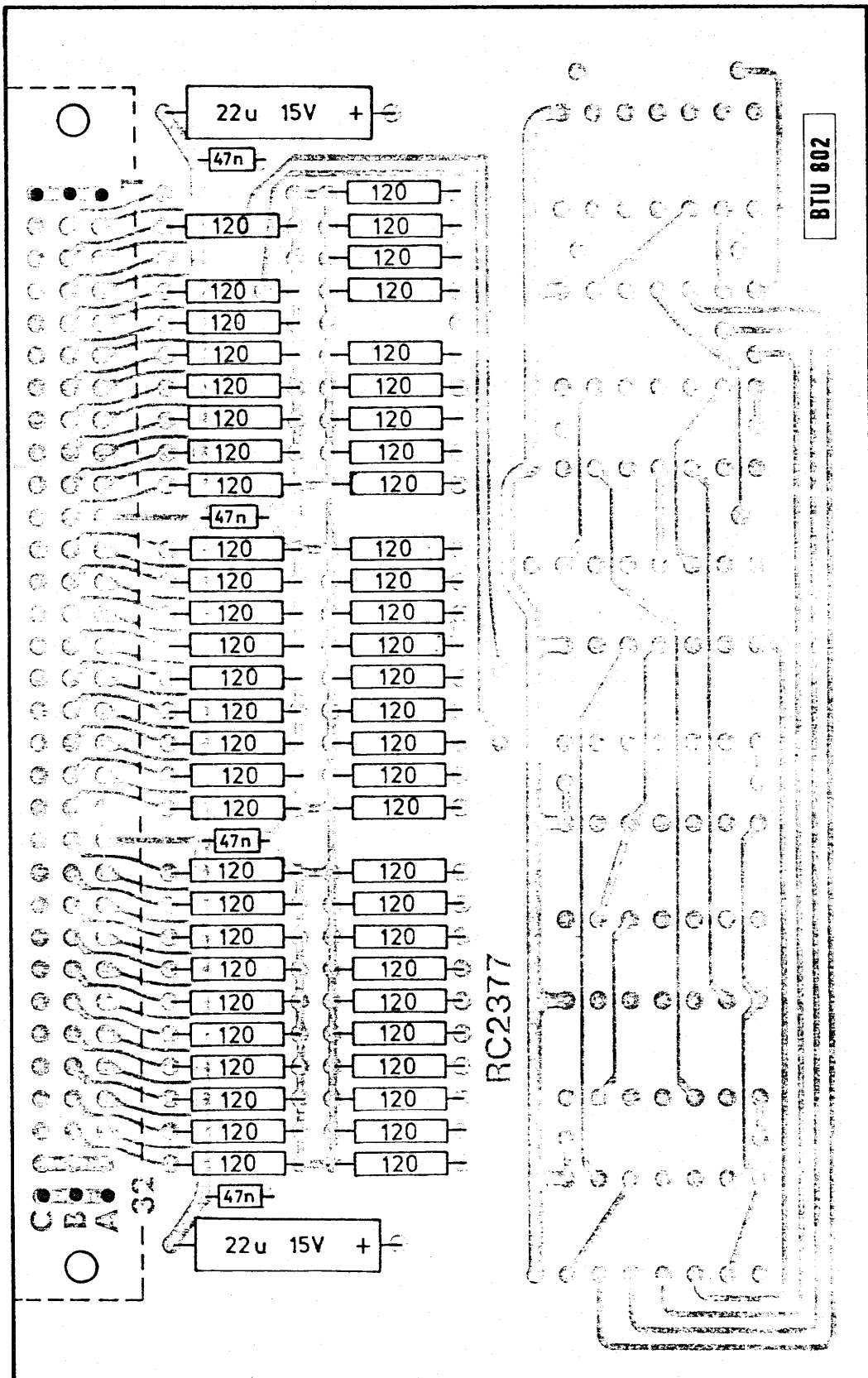
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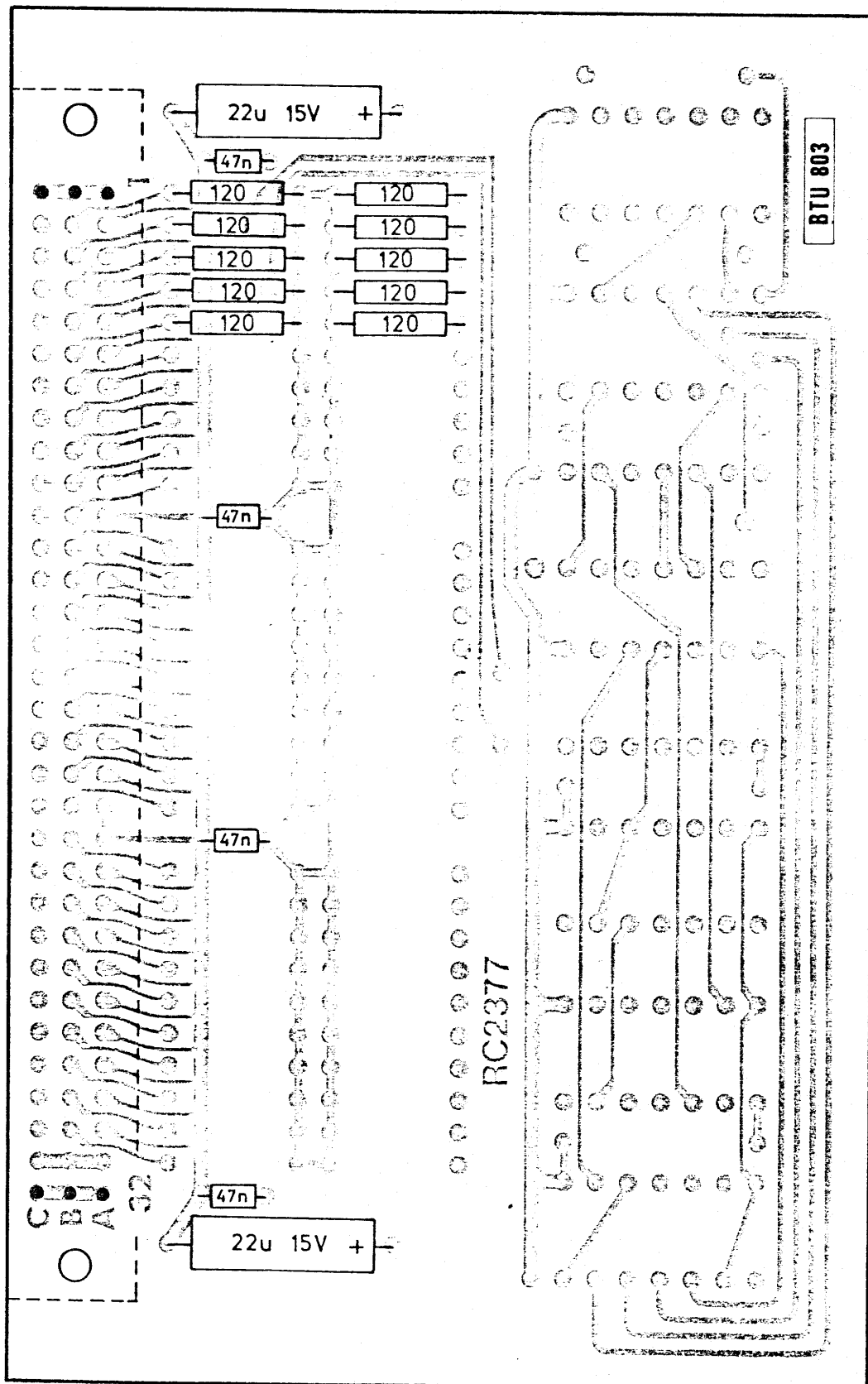
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BCU802 ASSEMBLY DRAWING



BTU802 ASSEMBLY DRAWING



BTU803 ASSEMBLY DRAWING

CONNECTOR: 1001					
PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME
A1		+5 VOLTS	B1	4 - 6	+5 VOLTS
A2		0 VOLT	B2		- , SELOUT (0)
A3		0 VOLT	B3		NOT USED
A4		0 VOLT	B4	4 - 8	- , SELOUT (1)
A5		0 VOLT	B5		NOT USED
A6		0 VOLT	B6		- , SYSRESET
A7		0 VOLT	B7		- , DATARDY
A8		0 VOLT	B8		- , ACK
A9		0 VOLT	B9		- , NACK
A10		0 VOLT	B10		- , ADDR (0)
A11		0 VOLT	B11		(2)
A12		0 VOLT	B12		(4)
A13		0 VOLT	B13		(6)
A14		0 VOLT	B14		(8)
A15		0 VOLT	B15		(10)
A16		0 VOLT	B16		(12)
A17		0 VOLT	B17		(14)
A18		0 VOLT	B18		(16)
A19		0 VOLT	B19		(18)
A20		0 VOLT	B20		(20)
A21		0 VOLT	B21		(22)
A22		0 VOLT	B22		- , DATA (0)
A23		0 VOLT	B23		(2)
A24		0 VOLT	B24		(4)
A25		0 VOLT	B25		(6)
A26		0 VOLT	B26		(8)
A27		0 VOLT	B27		(10)
A28		0 VOLT	B28		(12)
A29		0 VOLT	B29		(14)
A30		0 VOLT	B30		(16)
A31		NOT USED	B31		NOT USED
A32		+5 VOLTS	B32		+5 VOLTS
C1			C1		
C2			C2		
C3			C3		
C4			C4		
C5			C5		
C6			C6		
C7			C7		
C8			C8		
C9			C9		
C10			C10		
C11			C11		
C12			C12		
C13			C13		
C14			C14		
C15			C15		
C16			C16		
C17			C17		
C18			C18		
C19			C19		
C20			C20		
C21			C21		
C22			C22		
C23			C23		
C24			C24		
C25			C25		
C26			C26		
C27			C27		
C28			C28		
C29			C29		
C30			C30		
C31			C31		
C32			C32		

CONNECTOR: 1001									
PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME	GENERATOR ADDRESS
A1		+5 VOLTS	B1		+5 VOLTS	C1		+5 VOLTS	
A2		0 VOLT	B2		NOT USED	C2		- , BUSREQ (0)	
A3		0 VOLT	B3		- , SELOUT (0)	C3		- , BUSREQ (1)	
A4		0 VOLT	B4		NOT USED	C4		- , COMSEL	
A5		0 VOLT	B5		- , SELOUT (1)	C5		- , SELACK	
A6		0 VOLT	B6		- , SYSRESET	C6		NOT USED	
A7		0 VOLT	B7		- , DATARDY	C7		- , BUSBUSY	
A8		0 VOLT	B8		- , ACK	C8		POK	
A9		0 VOLT	B9		- , NACK	C9		- , PINT	
A10		0 VOLT	B10		- , ADDR (0)	C10		- , ADDR (1)	
A11		0 VOLT	B11		- , ADDR (2)	C11		- , ADDR (3)	
A12		0 VOLT	B12		- , ADDR (4)	C12		- , ADDR (5)	
A13		0 VOLT	B13		- , ADDR (5)	C13		- , ADDR (7)	
A14		0 VOLT	B14		- , ADDR (8)	C14		- , ADDR (9)	
A15		0 VOLT	B15		- , ADDR (10)	C15		- , ADDR (11)	
A16		0 VOLT	B16		- , ADDR (12)	C16		- , ADDR (13)	
A17		0 VOLT	B17		- , ADDR (14)	C17		- , ADDR (15)	
A18		0 VOLT	B18		- , ADDR (16)	C18		- , ADDR (17)	
A19		0 VOLT	B19		- , ADDR (18)	C19		- , ADDR (19)	
A20		0 VOLT	B20		- , ADDR (20)	C20		- , ADDR (21)	
A21		0 VOLT	B21		- , DATA (0)	C21		- , ADDRPAR	
A22		0 VOLT	B22		- , DATA (2)	C22		- , DATA (1)	
A23		0 VOLT	B23		- , DATA (4)	C23		- , DATA (3)	
A24		0 VOLT	B24		- , DATA (6)	C24		- , DATA (5)	
A25		0 VOLT	B25		- , DATA (8)	C25		- , DATA (7)	
A26		0 VOLT	B26		- , DATA (10)	C26		- , DATA (9)	
A27		0 VOLT	B27		- , DATA (12)	C27		- , DATA (11)	
A28		0 VOLT	B28		- , DATA (14)	C28		- , DATA (13)	
A29		0 VOLT	B29		- , DATA (16)	C29		- , DATA (15)	
A30		0 VOLT	B30		NOT USED	C30		- , DATA (17)	
A31		NOT USED	B31		+5 VOLTS	C31		NOT USED	
A32		+5 VOLTS	B32			C32		+5 VOLTS	

CONNECTOR: 1002

CONNECTOR: 1002					
PIN	GENERATOR ADDRESS	SIGNAL NAME	PIN	GENERATOR ADDRESS	SIGNAL NAME
A1		+5 VOLTS	B1		+5 VOLTS
A2		0 VOLT	B2		- , DATA (18)
A3		0 VOLT	B3		(20)
A4		0 VOLT	B4		(22)
A5		0 VOLT	B5		- , DATAPAR (0)
A6		0 VOLT	B6		(2)
A7		0 VOLT	B7		NOT USED
A8		0 VOLT	B8		-
A9		0 VOLT	B9		-
A10		0 VOLT	B10		-
A11		0 VOLT	B11		-
A12		0 VOLT	B12		-
A13		0 VOLT	B13		-
A14		0 VOLT	B14		-
A15		0 VOLT	B15		-
A16		0 VOLT	B16		-
A17		0 VOLT	B17		-
A18		0 VOLT	B18		-
A19		0 VOLT	B19		-
A20		0 VOLT	B20		-
A21		0 VOLT	B21		-
A22		0 VOLT	B22		-
A23		0 VOLT	B23		-
A24		0 VOLT	B24		-
A25		0 VOLT	B25		-
A26		0 VOLT	B26		-
A27		0 VOLT	B27		-
A28		0 VOLT	B28		-
A29		0 VOLT	B29		-
A30		0 VOLT	B30		-
A31		NOT USED	B31		NOT USED
A32		+5 VOLTS	B32		+5 VOLTS
C1			C1		
C2			C2		
C3			C3		
C4			C4		
C5			C5		
C6			C6		
C7			C7		
C8			C8		
C9			C9		
C10			C10		
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