
Title:

Technical Manual for Chassis CHS 803 - 804 - 805

 **REGNECENTRALEN**

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Abstract:

This manual contains the technical descriptions and diagrams of the internal wiring in the chassis.

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CHASSIS DESCRIPTION

1. MATERIALS.

1.

Cold-rolled steelplate, zincplated Frontplate, anodized aluminium profiles.

2. MAIN COMPONENTS.

2.

The Chassis is made up of 3 main parts. The main chassis for the controller boards, the power chassis for the power modules and the bottom chassis for the internal cables.

The power chassis is fixed to the main chassis with hinges, and can be turned up to a horizontal position. The chassis is held in its working position by 3 screws. The bottom plate in the bottom chassis can be pilled out, when the 2 screws in the front-plate are removed.

3. FANS.

3.

The main chassis is cooled by 2 axial fans delivering about $80 \text{ m}^3/\text{h}$ each. The power chassis is cooled by 1 fan, delivering about $80 \text{ m}^3/\text{h}$. (NOTE: The power chassis should not be left running with the rear-cover removed, as this will cause overheating of the power modules.

The fans have ball-bearings and are lubricated for life.

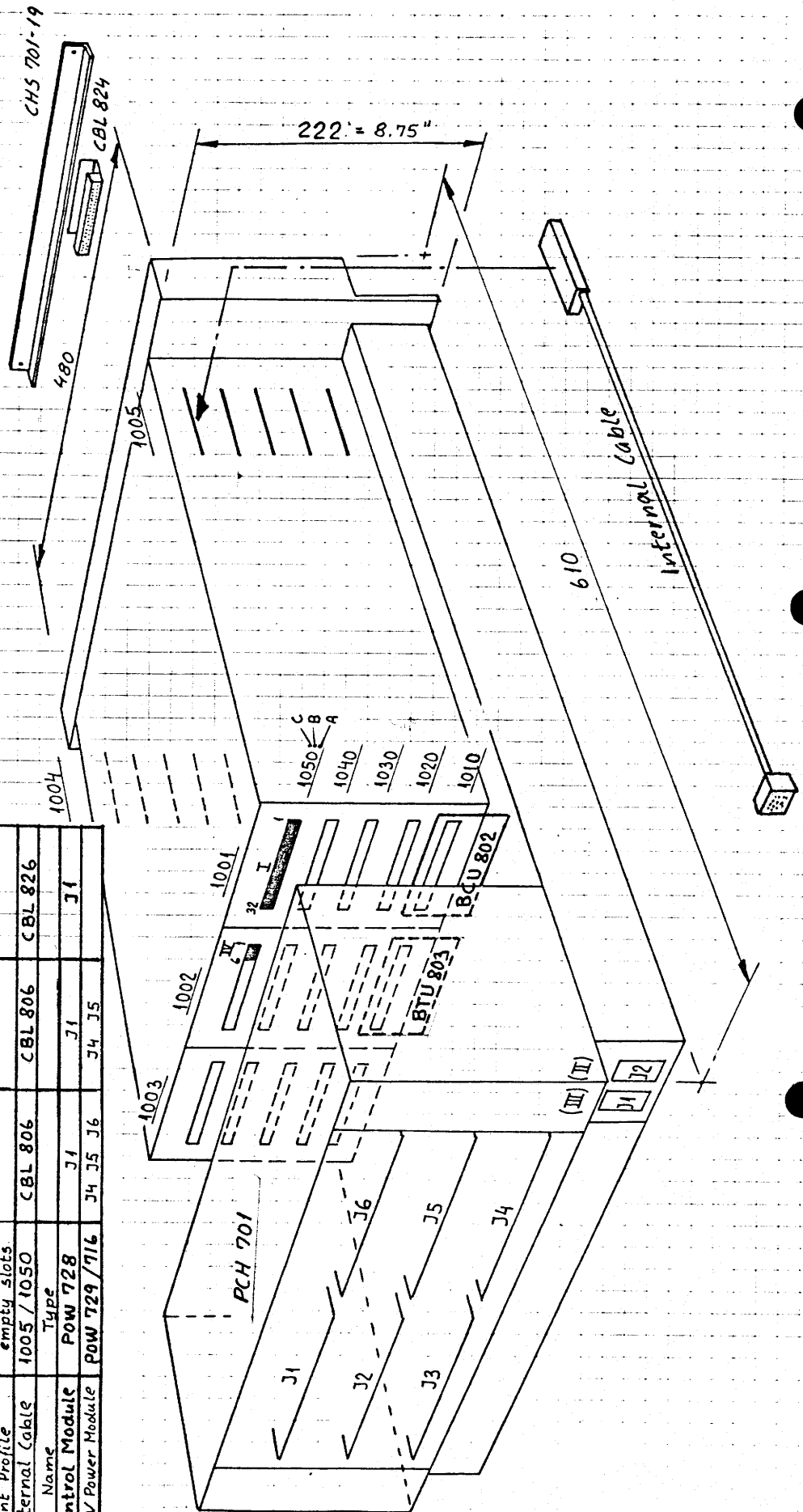
A/S REGJECENTRALEN 77.04.20 NT

Drawn by: Design Check: Replaces (see J.F.): Replaces by (see J.F.):

Main Chassis

Name	Pos.	CHS 803	CHS 804	CHS 805
Motherboard	1001	CBL 807	CBL 808	CBL 807
"	1002	CBL 809	CBL 810	CBL 810
"	1003	CBL 809	CBL 811	CBL 811
Internal Bus Cable	1001/1050 - J1/J2	CBL 815	CBL 816	
Dummy Plug	empty 1001's		CBL 824	
Front Profile	empty slots			
Internal Cable	1005 / 1050	CBL 806	CBL 806	CBL 826
Name	Type			
Control Module	POW 728	J1	J1	J1
+5V Power Module	POW 729 / 716	J4 J5 J6	J4 J5	J5

CHS 803	CHS 804	CHS 805
BTU 803+BCU	BTU 803 + 802 last chassis	BTU 803 + BCU



CHASSIS CHS 803 - 804 - 805

Connector I : BERG Minilatchhousing, 0.1 inch, 3 x 32 contacts
 Connector II : ELCO Receptacle 8026-075-000-801 (J1)
 Connector III : ELCO Receptacle 8026-075-000-801 (J2)
 Connector IV : BERG Minilatchhousing, 0.1 inch, 3 x 6 contacts
 Cable : 66 x 2 x 0.14mm²
 Length : 0.5m

(J1)

I PIN	WIRE	II PIN	SIGNAL NAME
C2		A1	-,BUSREQ (0)
A2		A2	0 VOLT
B3		A3	-,SELOUT (0)
A3		A4	0 VOLT
C3		A5	-,BUSREQ (1)
A3		A6	0 VOLT
C4		A7	-,COMSEL
A4		B7	0 VOLT
B5		B6	-,SELOUT (1)
A5		B5	0 VOLT
C5		B4	-,SELACK
A5		B3	0 VOLT
B6		B2	-,SYSRESET
A6		B1	0 VOLT
C6		C1	POB
A6		C2	0 VOLT
B7		C3	-,DATARDY
A7		C4	0 VOLT
C7		C5	-,BUSBUSY
A7		C6	0 VOLT
B8		C7	-,ACK
A8		D7	0 VOLT
C8		D6	POK
A8		D5	0 VOLT
B9		D4	-,NACK
A9		D3	0 VOLT
C9		D2	-,PINT
A9		E1	0 VOLT
B10		E2	-,ADDR (0)
A10		E3	0 VOLT
C10		E5	-,ADDR (1)
A10		E6	0 VOLT

(J1)

I PIN	WIRE	II PIN	SIGNAL NAME
B11		E7	-,ADDR (2)
A11		F7	0 VOLT
C11		F2	-,ADDR (3)
A11		F1	0 VOLT
B12		H1	-,ADDR (4)
A12		J1	0 VOLT
C12		J2	-,ADDR (5)
A12		J6	0 VOLT
B13		J7	-,ADDR (6)
A13		K7	0 VOLT
C13		K6	-,ADDR (7)
A13		K5	0 VOLT
B14		K3	-,ADDR (8)
A14		K2	0 VOLT
C14		K1	-,ADDR (9)
A14		L2	0 VOLT
B15		L3	-,ADDR (10)
A15		L4	0 VOLT
C15		L5	-,ADDR (11)
A15		L6	0 VOLT
B16		L7	-,ADDR (12)
A16		M7	0 VOLT
C16		M6	-,ADDR (13)
A16		M5	0 VOLT
B17		M4	-,ADDR (14)
A17		M3	0 VOLT
C17		M2	-,ADDR (15)
A17		M1	0 VOLT
B18		N1	-,ADDR (16)
A18		N2	0 VOLT
C18		N3	-,ADDR (17)
A18		N4	0 VOLT

770414 AAJ 770415 AOB

770414 AAJ 770415 AOB

(J2)			
I PIN	WIRE	III PIN	SIGNAL NAME
B19 A19		A1 A2	-,ADDR (18) 0 VOLT
C19 A19		A3 A4	-,ADDR (19) 0 VOLT
B20 A20		A5 A6	-,ADDR (20) 0 VOLT
C20 A20		A7 B7	-,ADDR (21) 0 VOLT
B21 A21		B6 B5	-,ADDR (22) 0 VOLT
C21 A21		B4 B3	-,ADDRPAR 0 VOLT
B22 A22		B2 B1	-,DATA (0) 0 VOLT
C22 A22		C1 C2	-,DATA (1) 0 VOLT
B23 A23		C3 C4	-,DATA (2) 0 VOLT
C23 A23		C5 C6	-,DATA (3) 0 VOLT
B24 A24		C7 D7	-,DATA (4) 0 VOLT
C24 A24		D6 D5	-,DATA (5) 0 VOLT
B25 A25		D4 D3	-,DATA (6) 0 VOLT
C25 A25		D2 E1	-,DATA (7) 0 VOLT
B26 A26		E2 E3	-,DATA (8) 0 VOLT
C26 A26		E5 E6	-,DATA (9) 0 VOLT
B27 A27		E7 F7	-,DATA (10) 0 VOLT
C27 A27		F2 F1	-,DATA (11) 0 VOLT

(J2)			
I PIN	WIRE	III PIN	SIGNAL NAME
B28 A28		H1 J1	-,DATA (12) 0 VOLT
C28 A28		J2 J6	-,DATA (13) 0 VOLT
B29 A29		J7 K7	-,DATA (14) 0 VOLT
C29 A29		K6 K5	-,DATA (15) 0 VOLT
B30 A30		K3 K2	-,DATA (16) 0 VOLT
C30 A30		K1 L2	-,DATA (17) 0 VOLT
IV PIN			
B2 A2		L3 L4	-,DATA (18) 0 VOLT
C2 A2		L5 L6	-,DATA (19) 0 VOLT
B3 A3		L7 M7	-,DATA (20) 0 VOLT
C3 A3		M6 M5	-,DATA (21) 0 VOLT
B4 A4		M4 M3	-,DATA (22) 0 VOLT
C4 A4		M2 M1	-,DATA (23) 0 VOLT
B5 A5		N1 N2	-,DATAPAR (24) 0 VOLT
C5 A5		N3 N4	-,DATAPAR (1) 0 VOLT
B6 A6		N5 N6	-,DATAPAR (2) 0 VOLT
C6 A6		N7 P7	-,DATAOUT 0 VOLT

Connector I : BERG Minilatchhousing, 0.1 inch, 3 x 32 contacts
 Connector II : ELCO Receptacle 8026-075-000-801 (J1)
 Connector III : ELCO Receptacle 8026-075-000-801 (J2)
 Connector IV : BERG Minilatchhousing, 0.1 inch, 3 x 6 contacts
 Cable : 66 x 2 x 0.14 mm²
 Length : 0.5m

(J1)			
I PIN	WIRE	II PIN	SIGNAL NAME
C2		A1	-,BUSREQ (0)
A2		A2	0 VOLT
B2		A3	-,SELIN (0)
A2		A4	0 VOLT
C3		A5	-,BUSREQ (1)
A3		A6	0 VOLT
C4		A7	-,COMSEL
A4		B7	0 VOLT
B4		B6	-,SELIN (1)
A4		B5	0 VOLT
C5		B4	-,SELACK
A5		B3	0 VOLT
B6		B2	-,SYSRESET
A6		B1	0 VOLT
C6		C1	POB
A6		C2	0 VOLT
B7		C3	-,DATARDY
A7		C4	0 VOLT
C7		C5	-,BUSBUSY
A7		C6	0 VOLT
B8		C7	-,ACK
A8		D7	0 VOLT
C8		D6	POK
A8		D5	0 VOLT
B9		D4	-,NACK
A9		D3	0 VOLT
C9		D2	-,PINT
A9		E1	0 VOLT
B10		E2	-,ADDR (0)
A10		E3	0 VOLT
C10		E5	-,ADDR (1)
A10		E6	0 VOLT

(J1)			
I PIN	WIRE	II PIN	SIGNAL NAME
B11		E7	-,ADDR (2)
A11		F7	0 VOLT
C11		F2	-,ADDR (3)
A11		F1	0 VOLT
B12		H1	-,ADDR (4)
A12		J1	0 VOLT
C12		J2	-,ADDR (5)
A12		J6	0 VOLT
B13		J7	-,ADDR (6)
A13		K7	0 VOLT
C13		K6	-,ADDR (7)
A13		K5	0 VOLT
B14		K3	-,ADDR (8)
A14		K2	0 VOLT
C14		K1	-,ADDR (9)
A14		L2	0 VOLT
B15		L3	-,ADDR (10)
A15		L4	0 VOLT
C15		L5	-,ADDR (11)
A15		L6	0 VOLT
B16		L7	-,ADDR (12)
A16		M7	0 VOLT
C16		M6	-,ADDR (13)
A16		M5	0 VOLT
B17		M4	-,ADDR (14)
A17		M3	0 VOLT
C17		M2	-,ADDR (15)
A17		M1	0 VOLT
B18		N1	-,ADDR (16)
A18		N2	0 VOLT
C18		N3	-,ADDR (17)
A18		N4	0 VOLT

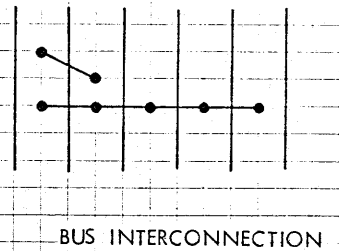
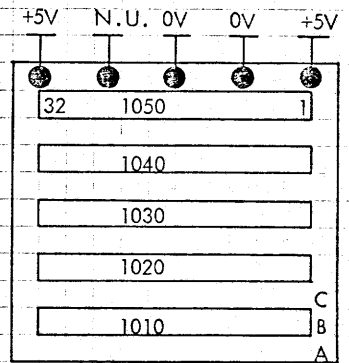
770414 AAJ 770415 AOB

770414 AAJ 770415 AOB

(J2)			
I PIN	WIRE	III PIN	SIGNAL NAME
B19 A19		A1 A2	-,ADDR (18) 0 VOLT
C19 A19		A3 A4	-,ADDR (19) 0 VOLT
B20 A20		A5 A6	-,ADDR (20) 0 VOLT
C20 A20		A7 B7	-,ADDR (21) 0 VOLT
B21 A21		B6 B5	-,ADDR (22) 0 VOLT
C21 A21		B4 B3	-,ADDRPAR 0 VOLT
B22 A22		B2 B1	-,DATA (0) 0 VOLT
C22 A22		C1 C2	-,DATA (1) 0 VOLT
B23 A23		C3 C4	-,DATA (2) 0 VOLT
C23 A23		C5 C6	-,DATA (3) 0 VOLT
B24 A24		C7 D7	-,DATA (4) 0 VOLT
C24 A24		D6 D5	-,DATA (5) 0 VOLT
B25 A25		D4 D3	-,DATA (6) 0 VOLT
C25 A25		D2 E1	-,DATA (7) 0 VOLT
B26 A26		E2 E3	-,DATA (8) 0 VOLT
C26 A26		E5 E6	-,DATA (9) 0 VOLT
B27 A27		E7 F7	-,DATA (10) 0 VOLT
C27 A27		F2 F1	-,DATA (11) 0 VOLT

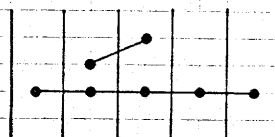
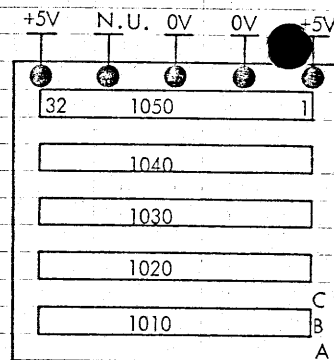
(J2)			
I PIN	WIRE	III PIN	SIGNAL NAME
B28 A28		H1 J1	-,DATA (12) 0 VOLT
C28 A28		J2 J6	-,DATA (13) 0 VOLT
B29 A29		J7 K7	-,DATA (14) 0 VOLT
C29 A29		K6 K5	-,DATA (15) 0 VOLT
B30 A30		K3 K2	-,DATA (16) 0 VOLT
C30 A30		K1 L2	-,DATA (17) 0 VOLT
IV PIN			
B2 A2		L3 L4	-,DATA (18) 0 VOLT
C2 A2		L5 L6	-,DATA (19) 0 VOLT
B3 A3		L7 M7	-,DATA (20) 0 VOLT
C3 A3		M6 M5	-,DATA (21) 0 VOLT
B4 A4		M4 M3	-,DATA (22) 0 VOLT
C4 A4		M2 M1	-,DATA (23) 0 VOLT
B5 A5		N1 N2	-,DATAPAR (1) 0 VOLT
C5 A5		N3 N4	-,DATAPAR (1) 0 VOLT
B6 A6		N5 N6	-,DATAPAR (2) 0 VOLT
C6 A6		N7 P7	-,DATAOUT 0 VOLT

					SIGNAL NAME	PIN ROW	PIN	1050	1040	1030	1020	1010
Replaced by Dwg. No. due to ECN Replaces Dwg. No. Design Check Dwg. Office Check Drawn by Designed by 770614 NT A/S RECENTRALEN	Unit	CHS801	Dwg. No.	R 12038	+5V	A	1	•	•	•	•	•
					0V		2-30	•	•	•	•	•
					Not used		31	•	•	•	•	•
					+ 5V		32	•	•	•	•	•
					+5V	B	1	•	•	•	•	•
					-,SELIN(0)		2	•	•	•	•	•
					-,SELOUT(0)		3	•	•	•	•	•
					-,SELIN(1)		4	•	•	•	•	•
					-,SELOUT(1)		5	•	•	•	•	•
					-,SYSRESET		6	•	•	•	•	•
					-,DATARDY		7	•	•	•	•	•
					-,ACK		8	•	•	•	•	•
					-,NACK		9	•	•	•	•	•
					-,ADDR(0)		10	•	•	•	•	•
					-,ADDR(2)		11	•	•	•	•	•
					-,ADDR(4)		12	•	•	•	•	•
					-,ADDR(6)		13	•	•	•	•	•
					-,ADDR(8)		14	•	•	•	•	•
					-,ADDR(10)		15	•	•	•	•	•
					-,ADDR(12)		16	•	•	•	•	•
					-,ADDR(14)		17	•	•	•	•	•
					-,ADDR(16)		18	•	•	•	•	•
					-,ADDR(18)		19	•	•	•	•	•
					-,ADDR(20)		20	•	•	•	•	•
					-,ADDR(22)		21	•	•	•	•	•
					-,DATA(0)		22	•	•	•	•	•
					-,DATA(2)		23	•	•	•	•	•
					-,DATA(4)		24	•	•	•	•	•
					-,DATA(6)		25	•	•	•	•	•
					-,DATA(8)		26	•	•	•	•	•
					-,DATA(10)		27	•	•	•	•	•
					-,DATA(12)		28	•	•	•	•	•
					-,DATA(14)		29	•	•	•	•	•
					-,DATA(16)		30	•	•	•	•	•
					Voltage Bus, not used		31	•	•	•	•	•
					+5V		32	•	•	•	•	•
					+5V	C	1	•	•	•	•	•
					-,BUSREQ(0)		2	•	•	•	•	•
					-,BUSREQ(1)		3	•	•	•	•	•
					-,COMSEL		4	•	•	•	•	•
					-,SELACK		5	•	•	•	•	•
					POB		6	•	•	•	•	•
					-,BUSBUSY		7	•	•	•	•	•
					POK		8	•	•	•	•	•
					-,PINT		9	•	•	•	•	•
					-,ADDR(1)		10	•	•	•	•	•
					-,ADDR(3)		11	•	•	•	•	•
					-,ADDR(5)		12	•	•	•	•	•
					-,ADDR(7)		13	•	•	•	•	•
					-,ADDR(9)		14	•	•	•	•	•
					-,ADDR(11)		15	•	•	•	•	•
					-,ADDR(13)		16	•	•	•	•	•
					-,ADDR(15)		17	•	•	•	•	•
					-,ADDR(17)		18	•	•	•	•	•
					-,ADDR(19)		19	•	•	•	•	•
					-,ADDR(21)		20	•	•	•	•	•
					-,ADDRPAR		21	•	•	•	•	•
					-,DATA(1)		22	•	•	•	•	•
					-,DATA(3)		23	•	•	•	•	•
					-,DATA(5)		24	•	•	•	•	•
					-,DATA(7)		25	•	•	•	•	•
					-,DATA(9)		26	•	•	•	•	•
					-,DATA(11)		27	•	•	•	•	•
					-,DATA(13)		28	•	•	•	•	•
					-,DATA(15)		29	•	•	•	•	•
					-,DATA(17)		30	•	•	•	•	•
					Voltage Bus, not used		31	•	•	•	•	•
					+5V		32	•	•	•	•	•



A/S REGNENTRALEN	Designed by	770614-17
	Drawn by	
	Dwg. Office Check	
	Design Check	
	Replaces Dwg. No.	
	due to ECN	
	Replaced by Dwg. No.	

SIGNAL NAME	PIN ROW	PIN	1050	1040	1030	1020	1010
+ 5V	A	1	•	•	•	•	•
0V		2-30	•	•	•	•	•
not used		31	•	•	•	•	•
+ 5V		32	•	•	•	•	•
+5V	B	1	•	•	•	•	•
-,SELIN(0)		2	•	•	•	•	•
-,SELOUT(0)		3	•	•	•	•	•
-,SELIN(1)		4	•	•	•	•	•
-,SELOUT(1)		5	•	•	•	•	•
-,SYSRESET		6	•	•	•	•	•
-,DATARDY		7	•	•	•	•	•
-,ACK		8	•	•	•	•	•
-,NACK		9	•	•	•	•	•
-,ADDR(0)		10	•	•	•	•	•
-,ADDR(2)		11	•	•	•	•	•
-,ADDR(4)		12	•	•	•	•	•
-,ADDR(6)		13	•	•	•	•	•
-,ADDR(8)		14	•	•	•	•	•
-,ADDR(10)		15	•	•	•	•	•
-,ADDR(12)		16	•	•	•	•	•
-,ADDR(14)		17	•	•	•	•	•
-,ADDR(16)		18	•	•	•	•	•
-,ADDR(18)		19	•	•	•	•	•
-,ADDR(20)		20	•	•	•	•	•
-,ADDR(22)		21	•	•	•	•	•
-,DATA(0)		22	•	•	•	•	•
-,DATA(2)		23	•	•	•	•	•
-,DATA(4)		24	•	•	•	•	•
-,DATA(6)		25	•	•	•	•	•
-,DATA(8)		26	•	•	•	•	•
-,DATA(10)		27	•	•	•	•	•
-,DATA(12)		28	•	•	•	•	•
-,DATA(14)		29	•	•	•	•	•
-,DATA(16)		30	•	•	•	•	•
not used		31	•	•	•	•	•
+ 5 V		32	•	•	•	•	•
+ 5 V	C	1	•	•	•	•	•
-,BUSREQ(0)		2	•	•	•	•	•
-,BUSREQ(1)		3	•	•	•	•	•
-,COMSEL		4	•	•	•	•	•
-,SELACK		5	•	•	•	•	•
POB		6	•	•	•	•	•
-,BUSBUSY		7	•	•	•	•	•
POK		8	•	•	•	•	•
-,PINT		9	•	•	•	•	•
-,ADDR(1)		10	•	•	•	•	•
-,ADDR(3)		11	•	•	•	•	•
-,ADDR(5)		12	•	•	•	•	•
-,ADDR(7)		13	•	•	•	•	•
-,ADDR(9)		14	•	•	•	•	•
-,ADDR(11)		15	•	•	•	•	•
-,ADDR(13)		16	•	•	•	•	•
-,ADDR(15)		17	•	•	•	•	•
-,ADDR(17)		18	•	•	•	•	•
-,ADDR(19)		19	•	•	•	•	•
-,ADDR(21)		20	•	•	•	•	•
-,ADDRPAR		21	•	•	•	•	•
-,DATA(1)		22	•	•	•	•	•
-,DATA(3)		23	•	•	•	•	•
-,DATA(5)		24	•	•	•	•	•
-,DATA(7)		25	•	•	•	•	•
-,DATA(9)		26	•	•	•	•	•
-,DATA(11)		27	•	•	•	•	•
-,DATA(13)		28	•	•	•	•	•
-,DATA(15)		29	•	•	•	•	•
-,DATA(17)		30	•	•	•	•	•
not used		31	•	•	•	•	•
+ 5 V		32	•	•	•	•	•



BUS INTERCONNECTION

Unit
CHS802

Dwg. No.
R 12041

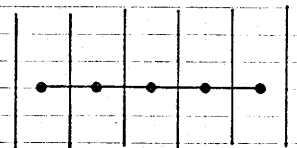
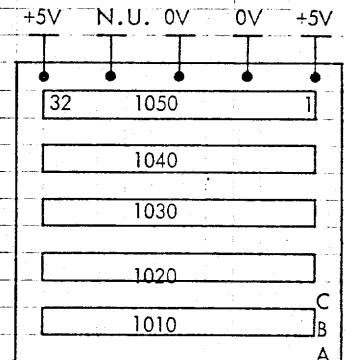
CBL 808

BUSMOTHERBOARD FOR CHS802 / 804

POS. 1001

A/S RECENTRALEN	Designed by	7706/4 UT
	Drawn by	
	Dwg. Office Check	
	Design Check	
	Replaces Dwg. No.	
due to ECN	Replaced by Dwg. No.	

SIGNAL NAME	Pin Row	PIN	1050	1040	1030	1020	1010
+ 5V	A	1	•	•	•	•	•
0V		2-30	•	•	•	•	•
not used		31	•	•	•	•	•
+ 5V		32	•	•	•	•	•
+ 5V	B	1	•	•	•	•	•
-, DATA(18)		2	•	•	•	•	•
-, DATA(20)		3	•	•	•	•	•
-, DATA(22)		4	•	•	•	•	•
-, DATAPAR(0)		5	•	•	•	•	•
-, DATAPAR(2)		6	•	•	•	•	•
not used		7	•	•	•	•	•
not used		8	•	•	•	•	•
not used		9	•	•	•	•	•
-, READ(0)		10	•	•	•	•	•
-, READ(2)		11	•	•	•	•	•
not used		12	•	•	•	•	•
-, CPUSYSRST		13	•	•	•	•	•
-, POWERFAIL		14	•	•	•	•	•
-, SELCOND(0)		15	•	•	•	•	•
-, SELCOND(2)		16	•	•	•	•	•
-, I/O READY		17	•	•	•	•	•
-, INSTRREADY		18	•	•	•	•	•
-, INTERRUPT		19	•	•	•	•	•
MONITORMODE		20	•	•	•	•	•
AFTER AM		21	•	•	•	•	•
PREFIR(0)		22	•	•	•	•	•
PREFIR(2)		23	•	•	•	•	•
PREFIR(4)		24	•	•	•	•	•
PREFIR(6)		25	•	•	•	•	•
PREFIR(8)		26	•	•	•	•	•
PREFIR(10)		27	•	•	•	•	•
-, LOADMIR		28	•	•	•	•	•
MASTERCLOCK		29	•	•	•	•	•
-, WRITE		30	•	•	•	•	•
Voltage Bus not used		31	•	•	•	•	•
+ 5V		32	•	•	•	•	•
+ 5V	C	1	•	•	•	•	•
-, DATA(19)		2	•	•	•	•	•
-, DATA(21)		3	•	•	•	•	•
-, DATA(23)		4	•	•	•	•	•
-, DATAPAR(1)		5	•	•	•	•	•
-, DATAOUT		6	•	•	•	•	•
not used		7	•	•	•	•	•
not used		8	•	•	•	•	•
not used		9	•	•	•	•	•
-, READ(1)		10	•	•	•	•	•
-, READ(3)		11	•	•	•	•	•
-, SETTIMERINTR		12	•	•	•	•	•
not used		13	•	•	•	•	•
-, CPUPOWERROK		14	•	•	•	•	•
-, SELCOND(1)		15	•	•	•	•	•
-, SELCOND(3)		16	•	•	•	•	•
I/O EXCEPTION		17	•	•	•	•	•
-, PREFEXC		18	•	•	•	•	•
CONDFALSE		19	•	•	•	•	•
ESCAPE MODE		20	•	•	•	•	•
AFTER ESC		21	•	•	•	•	•
PREFIR(1)		22	•	•	•	•	•
PREFIR(3)		23	•	•	•	•	•
PREFIR(5)		24	•	•	•	•	•
PREFIR(7)		25	•	•	•	•	•
PREFIR(9)		26	•	•	•	•	•
PREFIR(11)		27	•	•	•	•	•
-, LOADCONDSEL		28	•	•	•	•	•
CPUCLOCK		29	•	•	•	•	•
-, LOAD		30	•	•	•	•	•
Voltage Bus not used		31	•	•	•	•	•
+ 5V		32	•	•	•	•	•



BUS INTERCONNECTION

Unit
CHS801Dwg. No.
R 12039

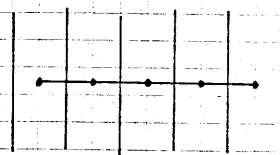
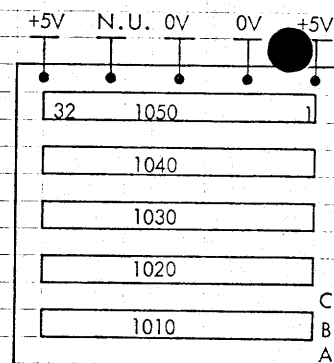
CBL 809.

BUSMOTHERBOARD FOR CHS801 / 803

POS 1002

A/S REGNECENTRALEN	Designed by	7706/4	47
	Drawn by		
	Dwg. Office Check		
	Design Check		
	Replaces Dwg. No.		
	due to ECN		
	Replaced by Dwg. No.		

SIGNAL NAME	PIN ROW	PIN	1050	1040	1030	1020	1010
+ 5V	A	1					
0V		2-30					
not used		31					
+ 5V		32					
+ 5V	B	1					
-, DATA (18)		2					
-, DATA (20)		3					
-, DATA (22)		4					
-, DATAPAR (0)		5					
-, DATAPAR (2)		6					
Voltage Bus not used	C	31					
+ 5V		32					
+ 5V	C	1					
-, DATA (19)		2					
-, DATA (21)		3					
-, DATA (23)		4					
-, DATAPAR (1)		5					
-, DATAOUT		6					
Voltage Bus not used	C	31					
+ 5V		32					



BUS INTERCONNECTION

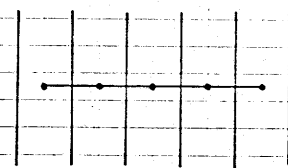
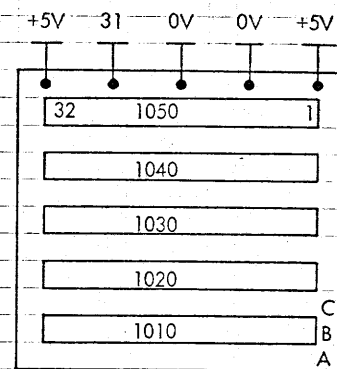
Unit
CHS802

Dwg. No.
R 12042

CBL 810
BUSMOTHERBOARD (PARTIAL) FOR CHS802/804/805
POS. 1002

A/S REGNECENTRALEN	Designed by	770614	Drawn by		Dwg. Office Check		Design Check		Replaces Dwg. No.		due to ECN		Replaced by Dwg. No.	

SIGNAL NAME	PIN ROW	PIN	1050	1040	1030	1020	1010
+ 5 VOLT	A	1	•	•	•	•	•
0 VOLT		2-30	•	•	•	•	•
Voltage Bus, not used		31	•	•	•	•	•
+ 5 VOLT		32	•	•	•	•	•
+ 5 VOLTS	B	1	•	•	•	•	•
PINS 2 to 30 AVAILABLE		2					
		3					
		4					
		5					
		6					
		7					
		8					
		9					
		10					
		11					
		12					
		13					
		14					
15							
16							
17							
18							
19							
20							
21							
22							
23							
24							
25							
26							
27							
28							
29							
30							
Voltage Bus, not used		31	•	•	•	•	•
+ 5 VOLTS		32	•	•	•	•	•
+ 5 VOLT	C	1	•	•	•	•	•
PINS 2 to 30 AVAILABLE		2					
		3					
		4					
		5					
		6					
		7					
		8					
		9					
		10					
		11					
		12					
		13					
		14					
15							
16							
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18							
19							
20							
21							
22							
23							
24							
25							
26							
27							
28							
29							
30							
Voltage Bus, not used		31	•	•	•	•	•
+ 5 VOLTS		32	•	•	•	•	•



BUS INTERCONNECTION

Unit
CHS802

Dwg. No.

R 12043

CBL 811
CONNECTORBOARD FOR CHS802 / 804 / 805
POS. 1003

NT 12-358-22

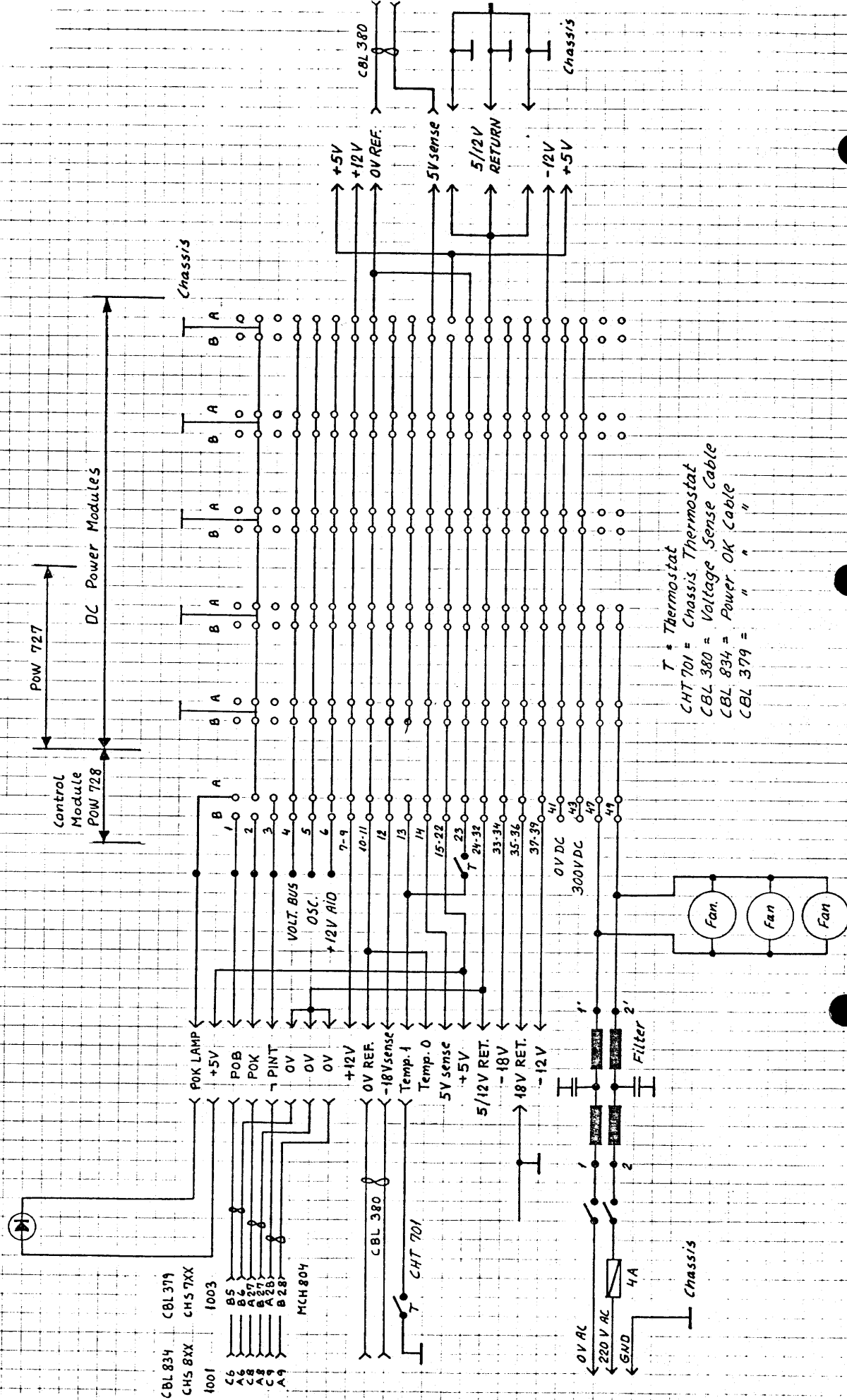
A/S REGNENCENTRALEN	Designed by NT/PKA	Drawn by NT	Dwg. Office Check 78.06.12	Design Check	Replaces Dwg. No.	due to ECH	Replaced by Dwg. No.
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PCH 701

Dwg. No.

R12 358

POWER CHASSIS MOTHERBOARD



T = Thermistor
 CHT 701 = Chassis Thermistor
 CBL 380 = Voltage Sense Cable
 CBL 834 = Power OK Cable
 CBL 379 = " " " "

PKA

AB 49 + 300 V
DC

AB 49

220V AC

AB 47

AB 45

AB 41 300V RTM.

AB 6 + 15V AUX.

AB 5 REF. OSCL.

AB 23 0V

AB 13 Thermosw

AB 14 + 5V SENSE
B1 P0B

AB 3 7 PINT

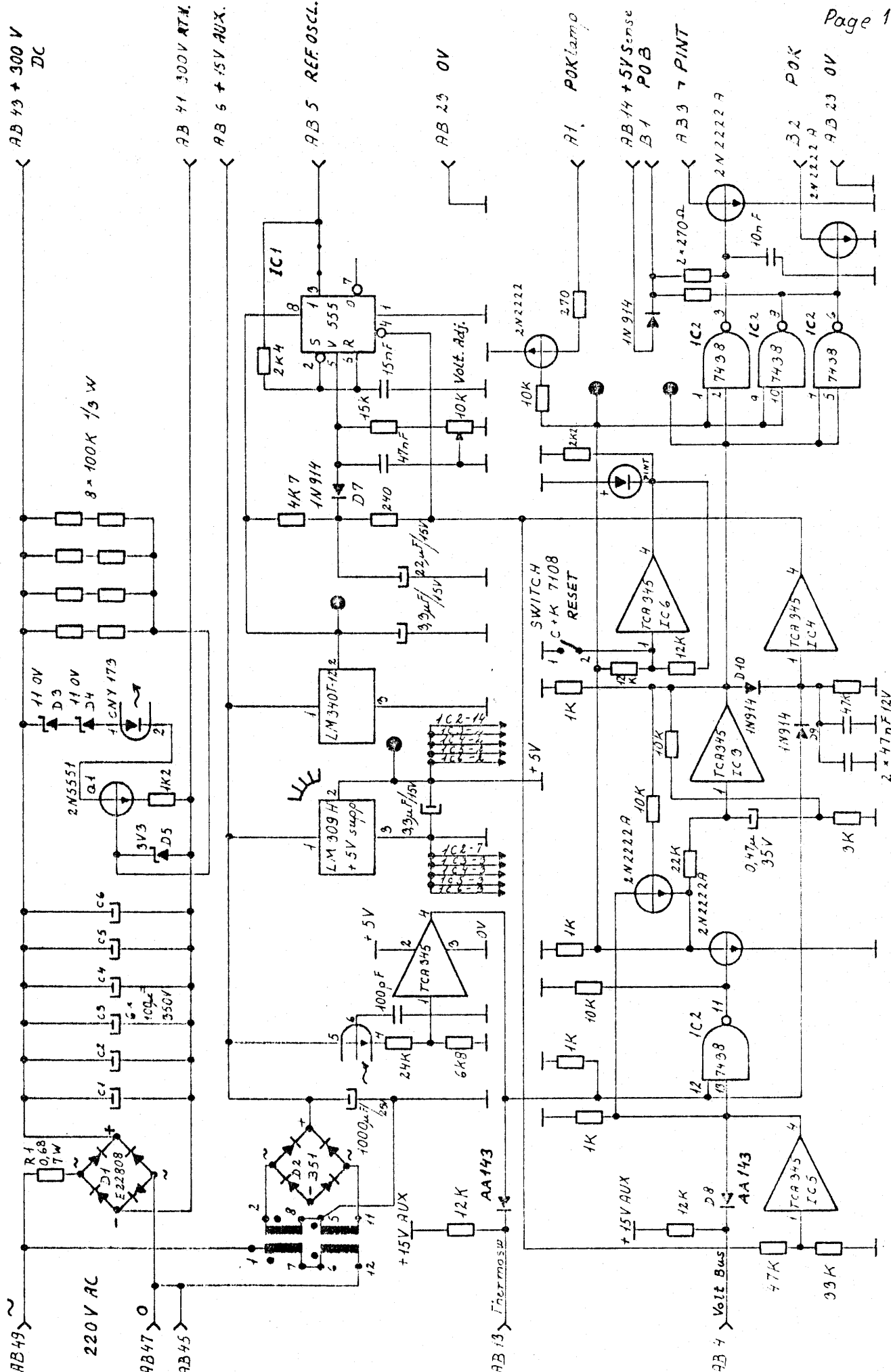
AB 23 0V

POW 728

R 12567

CONTROL MODULE

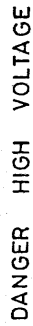
POW 728

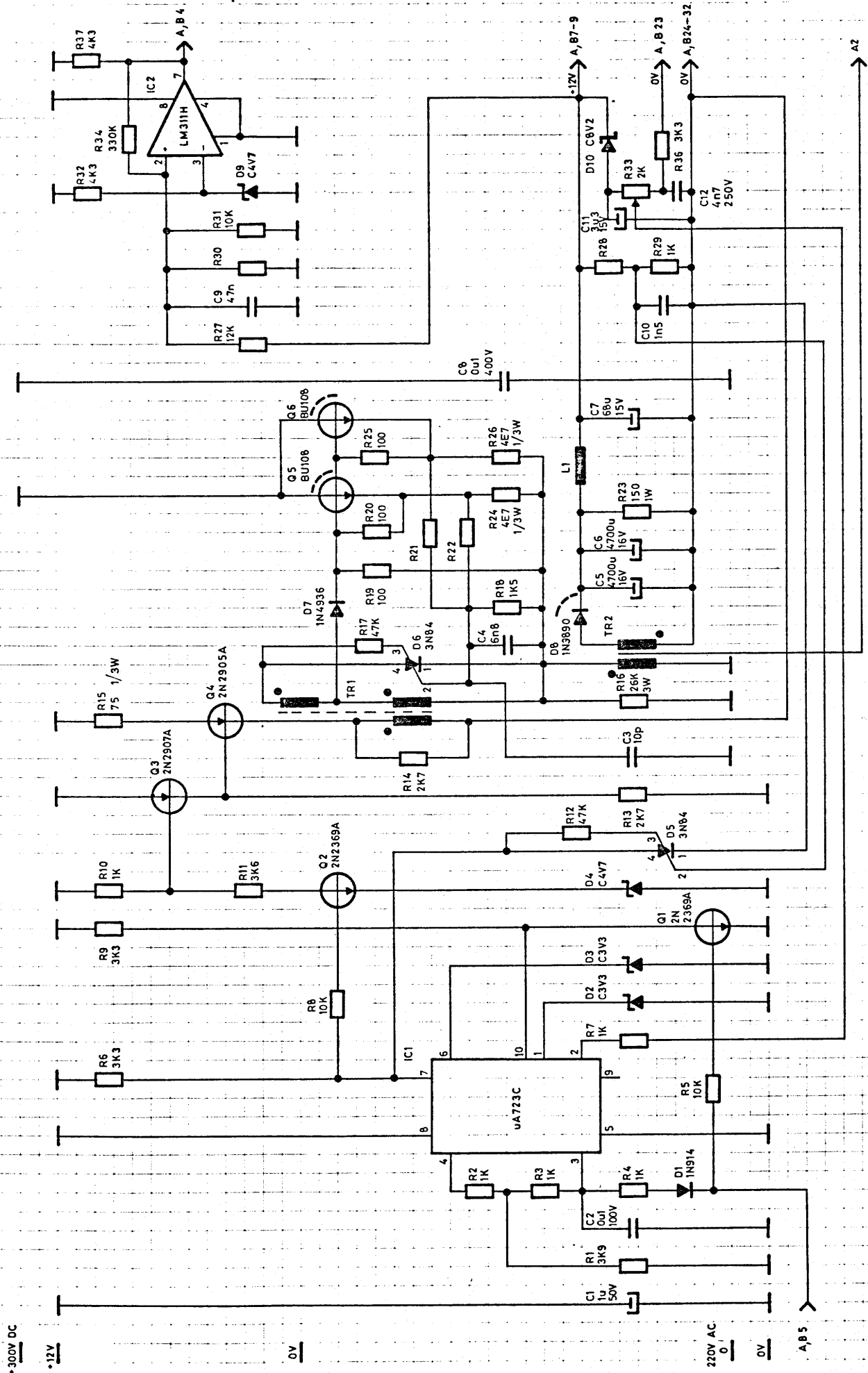


300V D.C. A.B 43

V13773

300V Dc : A, B 43
220V ACo : A, B 41
+12V : A, B 6





DANGER HIGH VOLTAGE

Designed by
666974-UFL

Drawn by

Way

Use to LCN

Approved by

Approved by

Approved by

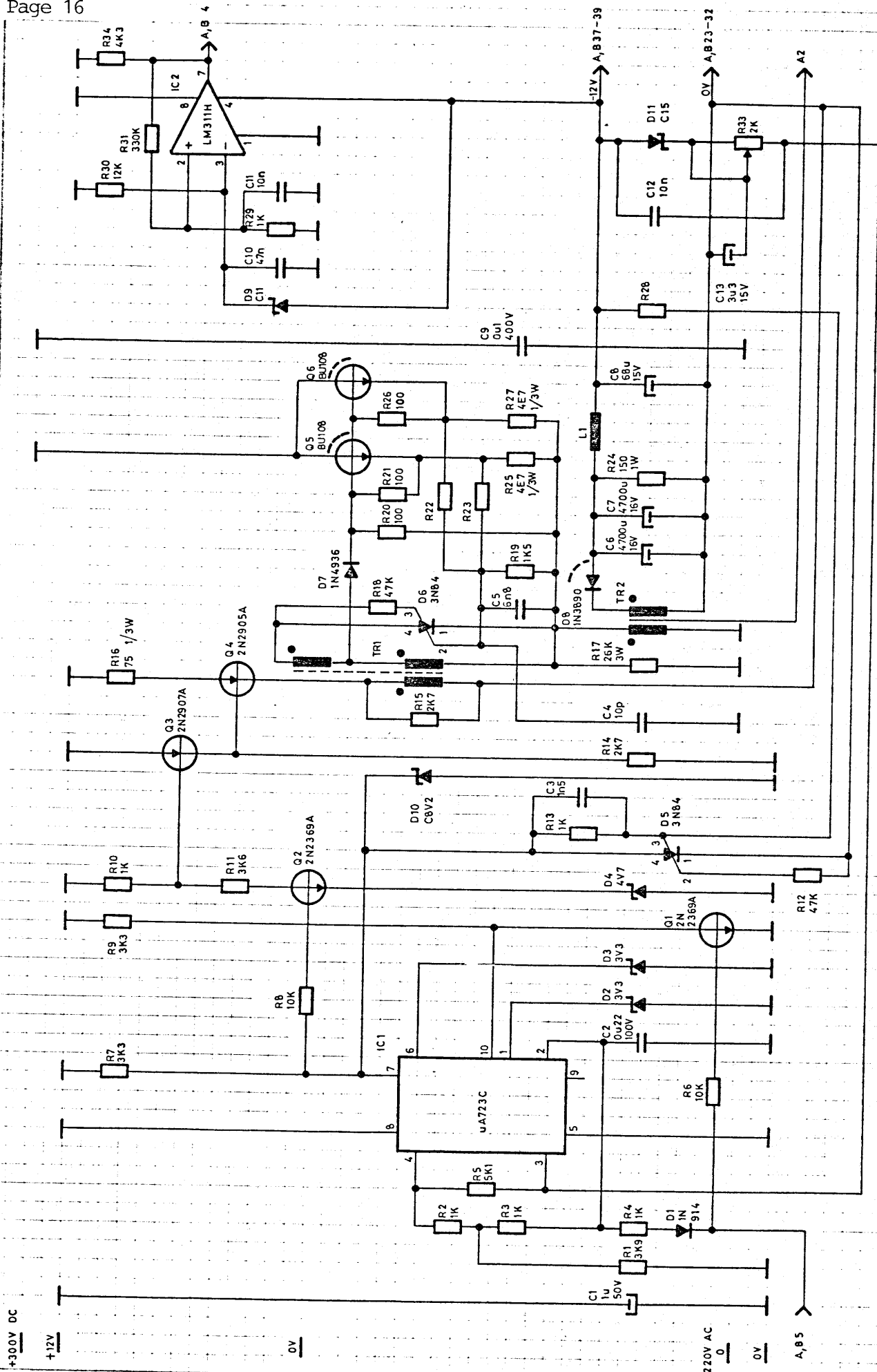
Approved by

Approved by

Unit
POW717
Circuit No.
V13774

+12V POWER MODULE

RECEIVED
A/S RE
CENTRALEN

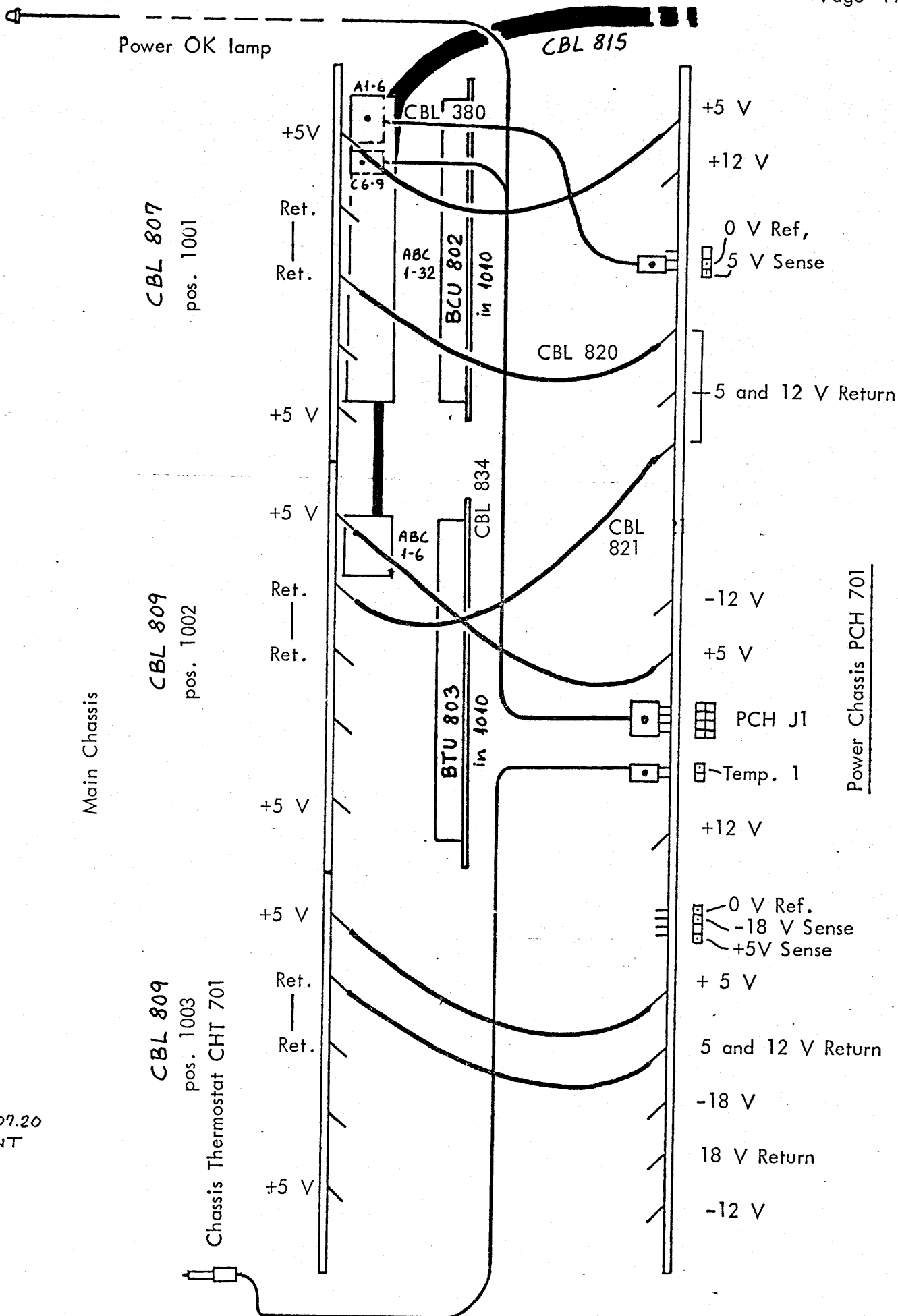


DANGER HIGH VOLTAGE

POW718

V13775

-12V POWER MODULE



78.07.20
NT

CABLE CONNECTIONS FOR POWER CHASSIS

CHS 803

Power OK lamp

Main Chassis

CBL 808
pos. 1001

CBL 810
pos. 1002

CBL 811
pos. 1003
Chassis Thermostat CHT 701

A1-6

CBL 380

ABC
1-32

ABC
1-6

CBL 834

CBL 816

CBL 820

CBL 821

+5 V

+12 V

0 V Ref,
5 V Sense

5 and 12 V Return

-12 V

+5 V

PCH J1

-Temp. 1

+12 V

0 V Ref.
-18 V Sense
+5V Sense

+ 5 V

5 and 12 V Return

-18 V

18 V Return

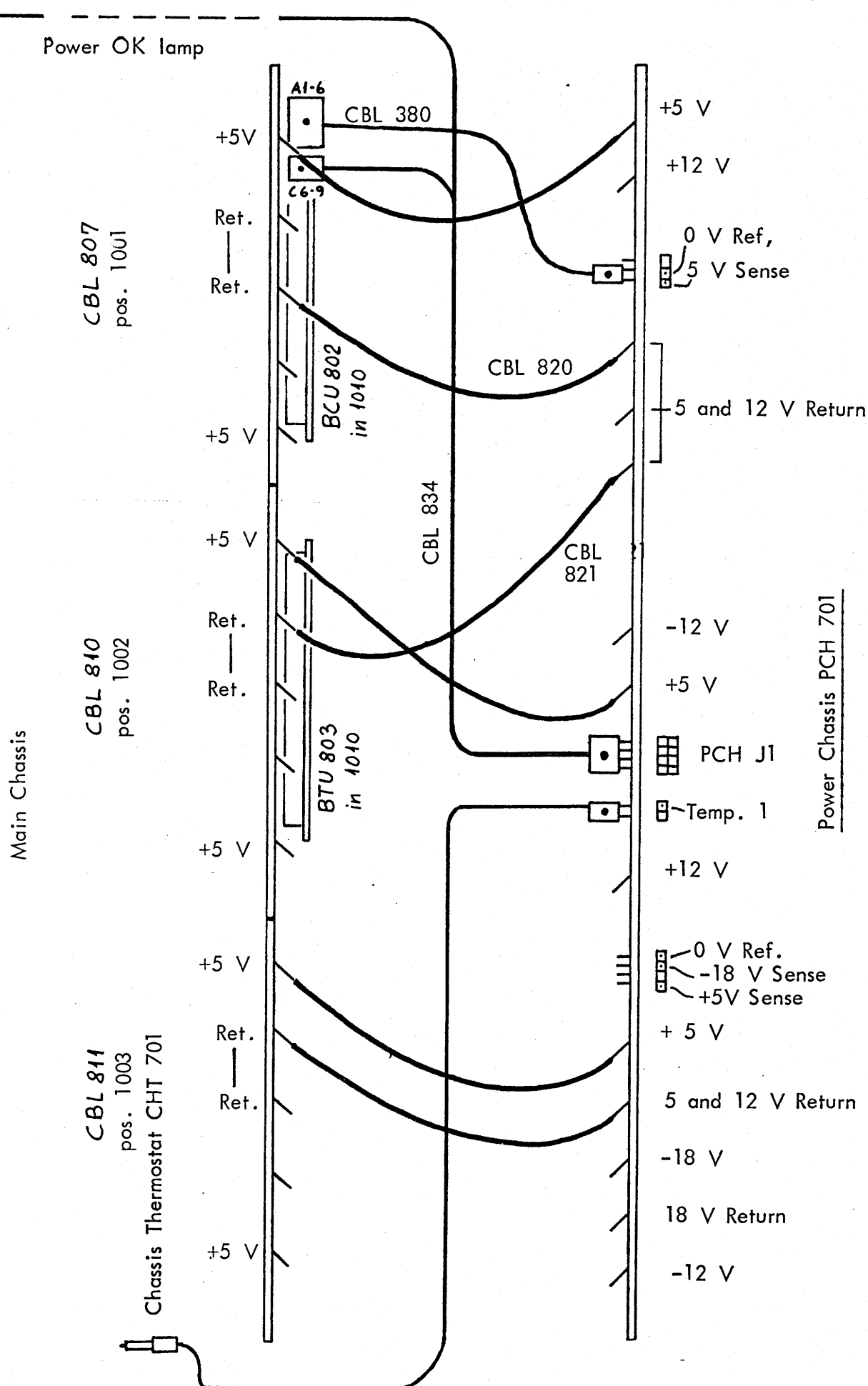
-12 V

Power Chassis PCH 701

CABLE CONNECTIONS FOR POWER CHASSIS

CHS 804

78.07.20
NT



78.07.20
NT

CABLE CONNECTIONS FOR POWER CHASSIS

CHS 805

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